WE310K6-P EVB (CS2446a-A)

Hardware User Guide

1VV0301859 Rev 0
2023-08-31
Draft
Public

Technical Documentation

Contents

1 Applicability Table

Table 1: Applicability Table

PRODUCTS
WE310K6-P
WE310K6-P M.2

2 Introduction

2.1 Scope

The aim of this document is the handling description of the WE310K6-P EVB (Evaluation Board).

2.2 Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit module.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: https://www.telit.com/contact-us/

Product information and technical documents are accessible 24/7 on our website: https://www.telit.com

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

ESD Risk: Notifies the user to take proper grounding precautions before handling the product.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to https://www.telit.com/hardware-terms-conditions/.

2.6 Disclaimer

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3 General Product Description

3.1 Overview

The Telit EVB is a rapid IoT Development Kit, in other words, it reduces the duration of IoT prototyping cycles from a matter of weeks or months to mere hours - all by capitalizing on the combination of embedded IoT software and hardware. The board was designed to provide a complete development environment to the user intended to integrage the Telit WE310K6-P module in the end product.

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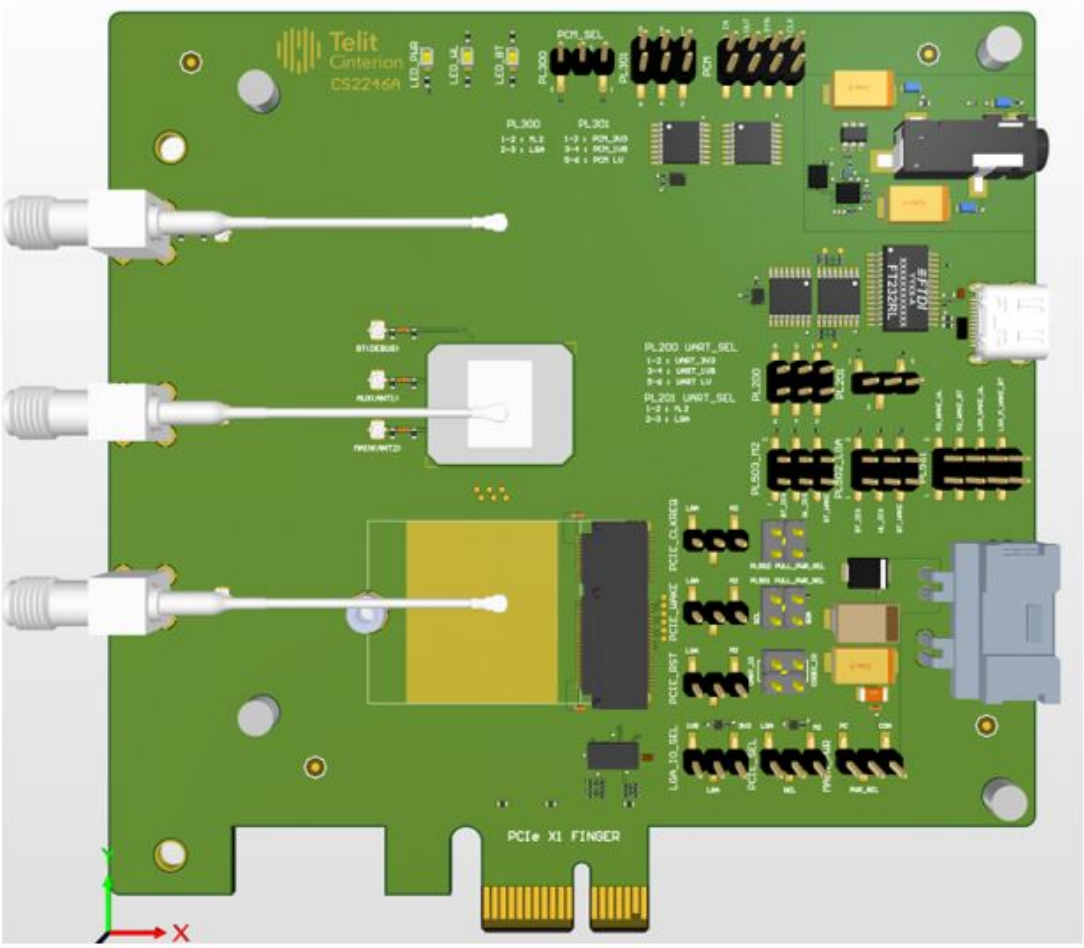
4 WE310K6-P Interface Description

4.1 WE310K6-P Development Kit

There is provision to mount both WE310K6 LGA module and WE310K6 M.2 card on to EVB. To route signals from any one of these modules to connectors is done by placing jumpers.

WE310K6-P EVB screenshots are given below:



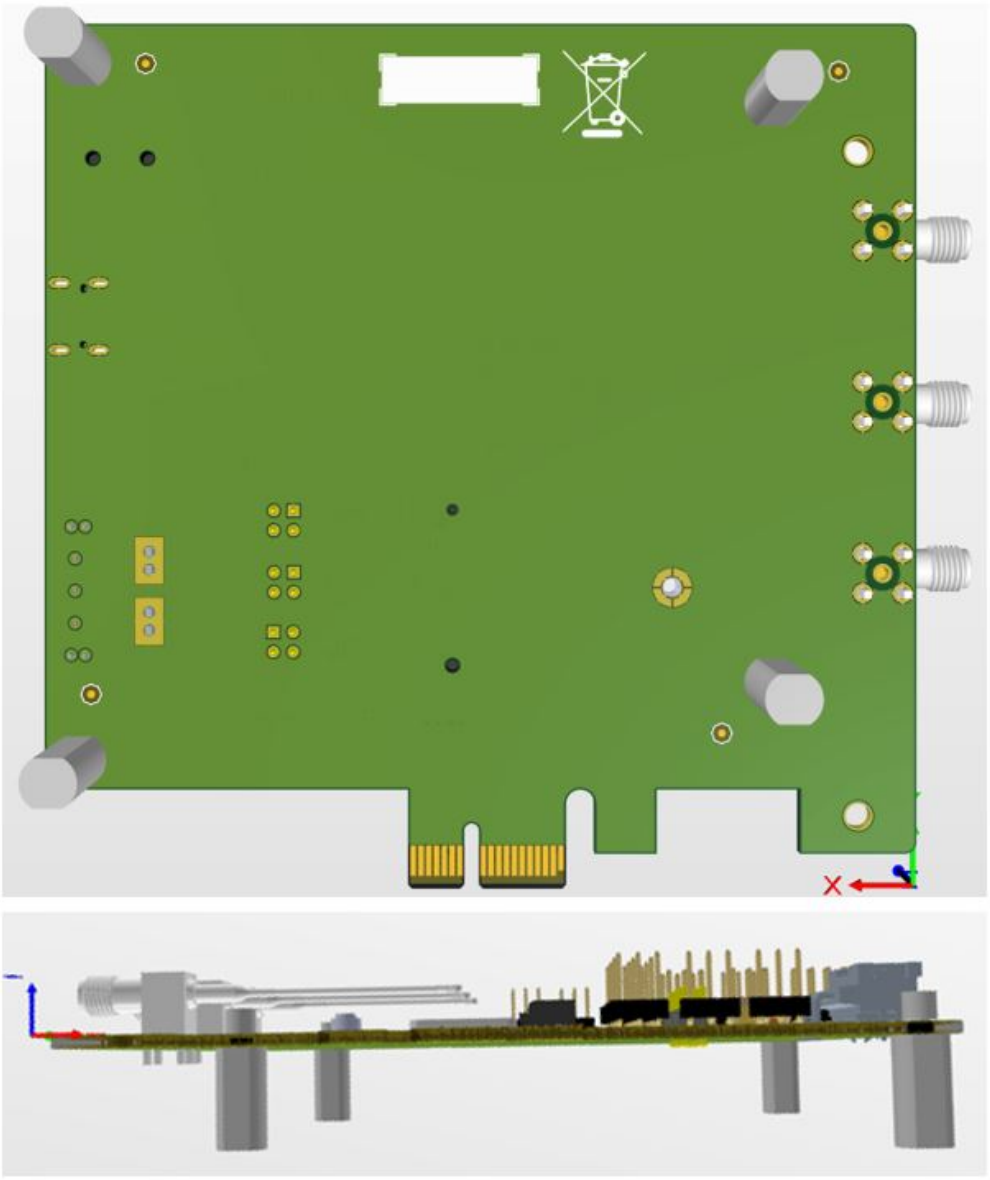


Figure 1: WE310K6-P EVB

This table lists the information related to WE310K6-P Kitting Parts.

Table 2: WE310K6 Kitting Parts

Description	Quantity
EVB Board	1
Power cable	1
USB Type-C cable	1
Wi-Fi/BT Antenna	2

4.2 Evaluation Board Description

Note that both WE310K6 LGA module and WE310K6 M.2 cannot be used together in EVB. Only one can be used at a time.

5 WE310K6-P Interface Description

5.1 WE310K6-P Development Kit

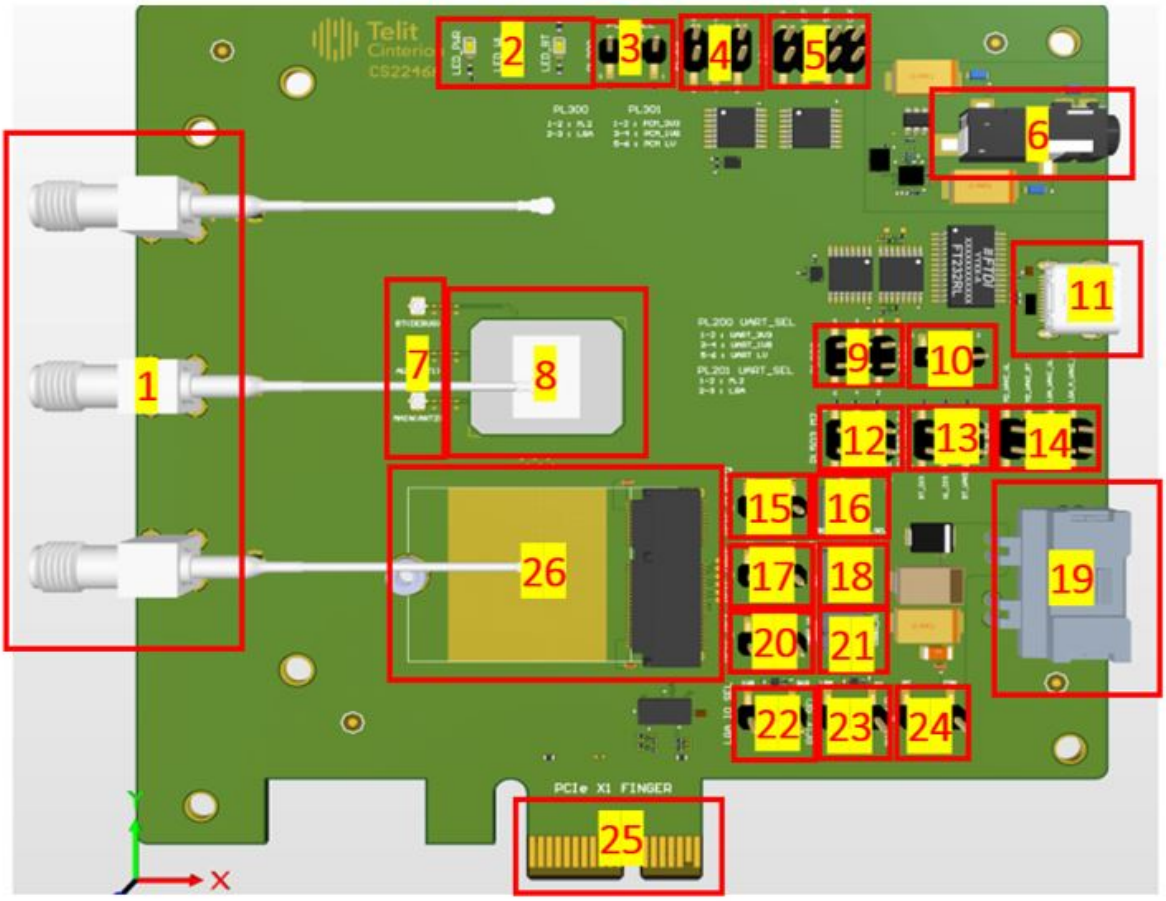


Figure 2: WE310K6-P EVB Top View

Table 3: EVB Description

1	SMA Antenna Connector	14	BT/WL WAKE option LGA or M.2 (PL501)
2	LED's	15	PCIe CLKREQ option LGA or M.2 (PL404)
3	PCM option LGA or M.2 (PL300)	16	Pull-up voltage option for BT WAKE LGA (PL504)
4	PCM I/0 level option (PL301)	17	PCIe WAKE option LGA or M.2 (PL403)
5	PCM Connector at codec (PL302)	18	Codec I2C, VDDIO LGA (PL500)
6	Audio Jack	19	Power Supply Connector
7	MHF Antenna Connector	20	PCIe RESET option LGA or M.2 (PL402)
8	WE310K6-P LGA Module	21	1.8V I/O for codec and FTDI chip (PL100)
9	UART I/0 level option (PL200)	22	I/O level option for LGA (PL101)
10	UART option LGA or M.2 (PL201)	23	PCIe option LGA or M.2 (PL401)

11	USB type-C connector	24	Power source selection (PL400)
12	M.2 BT/WL Enable option (PL503)	25	PCIe x1 finger
13	LGA BT/WL Enable option (PL502)	26	WE310K6-P M.2(Key-E) slot

5.2 Anteena Connector

Insert the antenna cable assembly into the respective SMD type MHF Antenna connector. Antenna cable assembly is common for both LGA and M.2 card.

Connect the Antenna into the SMA connector.

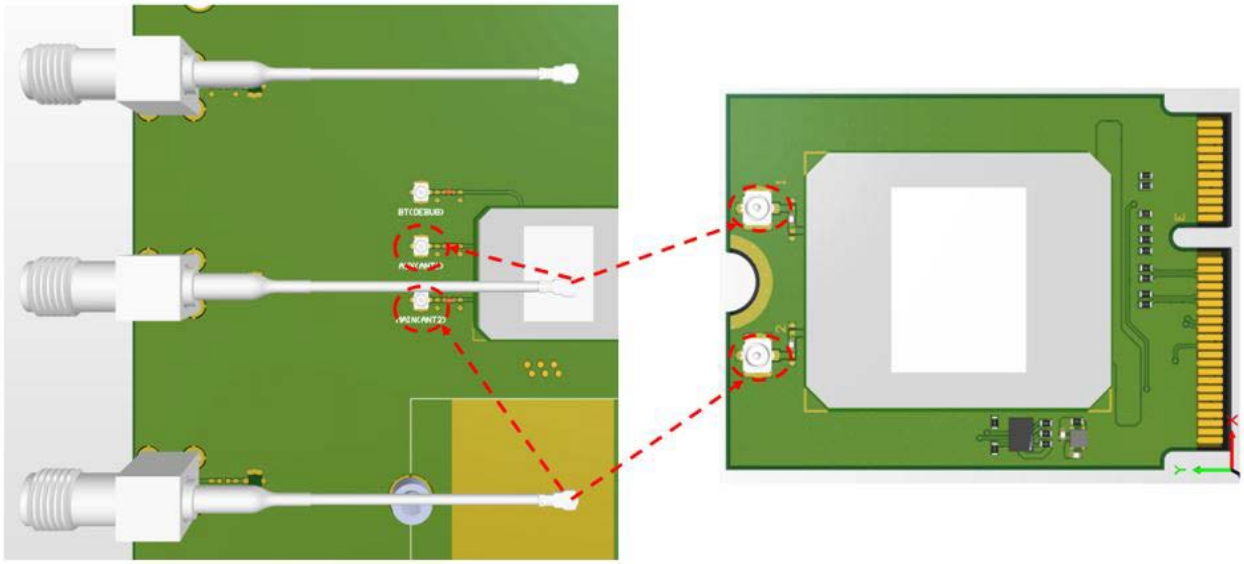


Figure 3: Antenna Connectors

5.3 UART

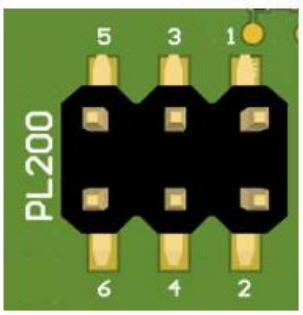


Figure 4: PL200 UART I/O Level Header

PL200 1-2: UART I/O Level is 3.3V.

PL200 3-4: UART I/O Level is 1.8V (Default jumper config).

PL200 5-6: UART Voltage-Level Translator 1.8V input pin. Insert a jumper when setting the I/O level to 3.3V.

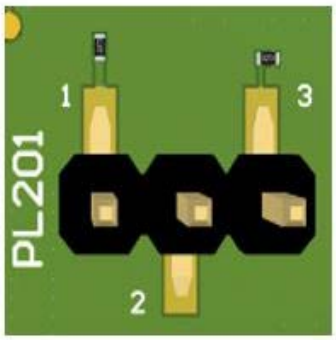


Figure 5: PL201 UART Selection Header

PL201 1-2: UART signals to M.2 card.

PL201 2-3: UART signals to LGA Module (Default jumper config).

5.4 PCM

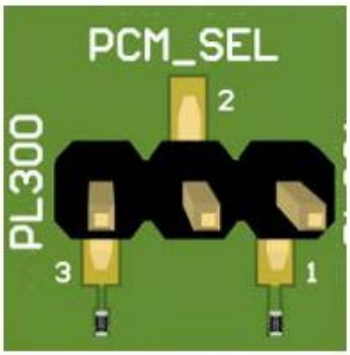


Figure 6: PL300 PCM Selection Header

PL300 1-2: PCM signals to M.2 card.

PL300 2-3: PCM signals to LGA Module (Default jumper config).

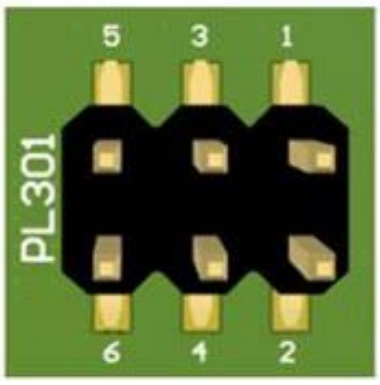


Figure 7: PL301 PCM I/O Level Header

PL301 1-2: PCM I/O Level 3.3V.

PL301 3-4: PCM I/O Level 1.8V (Default jumper config)

PL301 5-6: PCM Voltage-Level Translator 1.8V input pin. Insert a jumper when setting the I/O level to 3.3V.

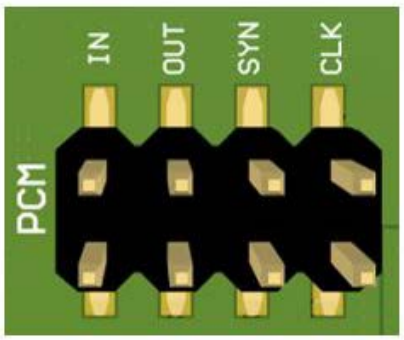


Figure 8: PL302 PCM signals Isolation Header at Codec

PL302 1-2: PCM CLK pin. (Default jumper config)

PL302 3-4: PCM SYNC pin. (Default jumper config)

PL302 5-6: PCM TX pin. (Default jumper config)

PL302 7-8: PCM RX pin. (Default jumper config)

5.5 Audio Jack

Audio from/to codec MAX9867EWV+T (from analog devices) is routed to the 3.5mm audio Jack SO300.

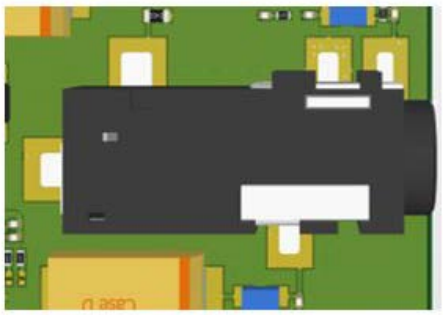


Figure 9: SO300 Audio jack

5.6 LED

There are three LEDs on the EVB.

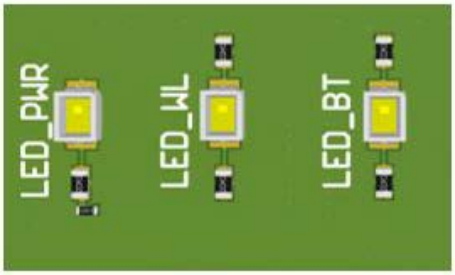


Figure 10: LED Indicate

LED_PWR: Indicates 3.3 supply is present.

LED_WL: Indicates Wi-Fi is enabled.

LED_BT: Indicates Bluetooth is enabled.

5.7 USB

The USB type-C is connected to USB to UART converter FTDI chip. This is useful to connect the WE310K6 UART port to PC for testing Bluetooth.

Connect the USB Type-C cable included with the EVB into the USB connector.

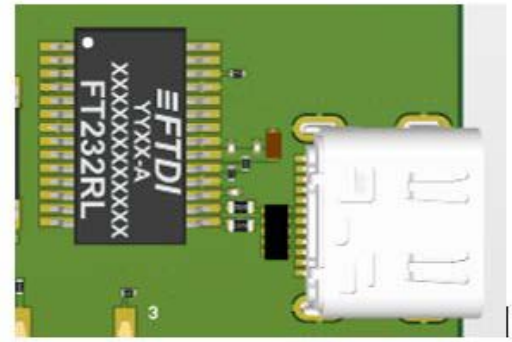


Figure 11: USB Type-C port

Figure 12: USB Type-C cable

5.8 PCIe

Insert EVB's PCIe finger into the host PCIe slot. As per the PL401 jumper setting, the host PCIe signals are routed to LGA module or M.2 card.

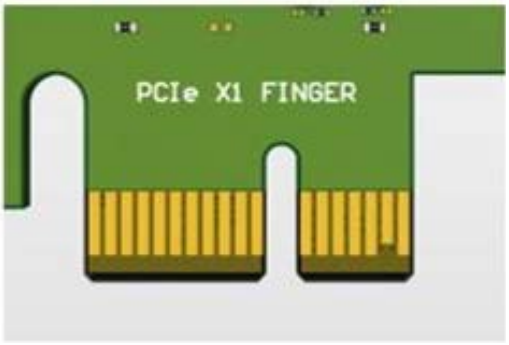


Figure 13: PCIe finger

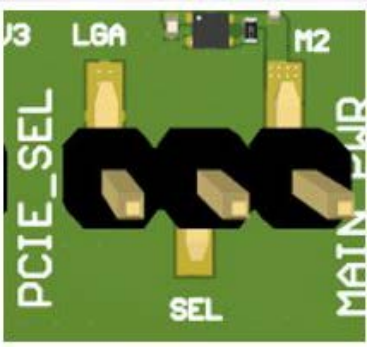


Figure 14: PL401 PCIe Signal Routing Selection Header

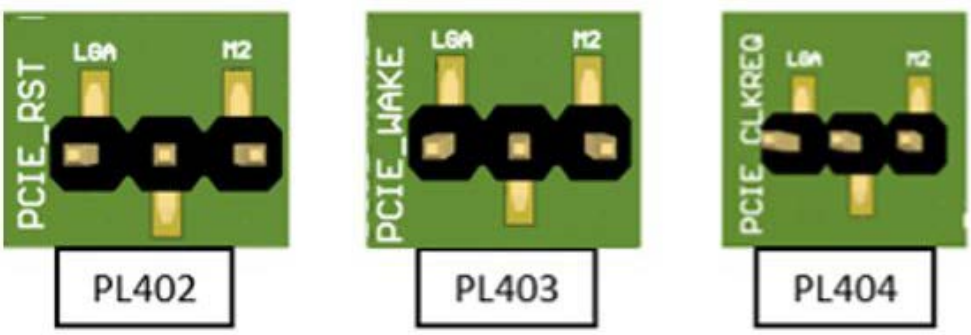


Figure 15: PCIe Control Signals Routing Headers

PL402 1-2: PCIe reset signal to LGA module (Default jumper config).

PL402 2-3: PCIe reset signal to M.2 card.

PL403 1-2: PCIe WAKE signal to LGA module (Default jumper config).

PL403 2-3: PCIe WAKE signal to M.2 card.

PL404 1-2: PCIe CLKREQ signal to LGA module (Default jumper config).

PL404 2-3: PCIe CLKREQ signal to M.2 card.

5.9 EVB Power Supply Configuration

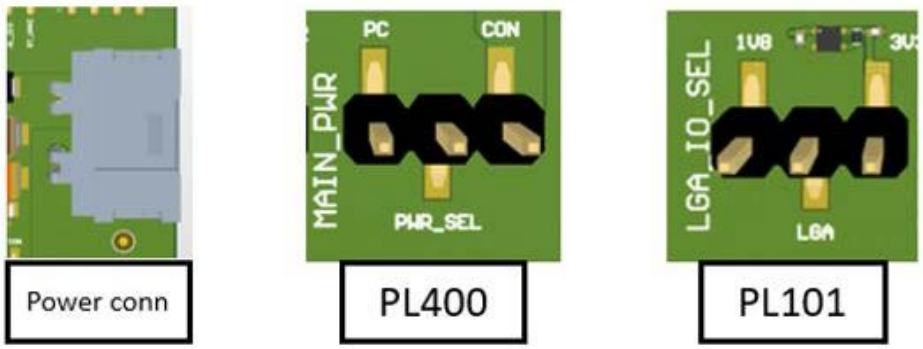


Figure 16: EVB Power Supply Configuration

There are two ways to supply power to the EVB: Through host PCIe socket or External power supply connector. To supply power from external DC power supply, connect the power cable included with the EVB into the connector SO401 and place jumper on PL400 2-3.

Figure 17: Power cable

PL400 1-2: 3.3V main power is supplied through the PCIe socket (Default jumper config).

PL400 2-3: 3.3V main power is supplied through external DC power supply.

PL101 1-2: 1.8V I/O level LGA module (Default jumper config).

PL101 2-3: 3.3V I/O level LGA module.

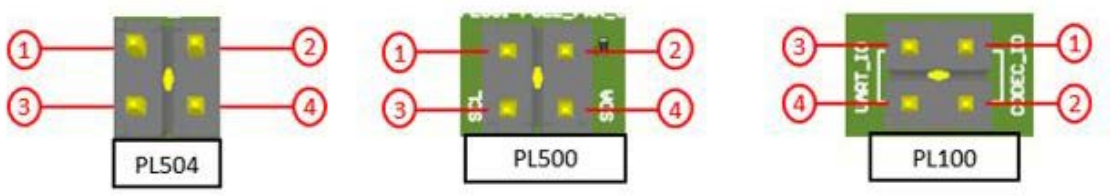


Figure 18: EVB Power Supply Configuration

PL504 1-2: 3.3V pull-up to BT_WAKE_HOST pin of LGA Module (Default jumper config).

PL504 3-4: I/O(1.8Vor3.3V) pull-up on BT_WAKE_HOST pin of LGA Module.

PL500 1-2: I/O(1.8Vor3.3V) pull-up on HOST WAKE BT&WL (LGA module), HOST WAKE BT&WL (M.2) pin (PL501).

PL500 3: Codec I2C_SCL

PL500 4: Codec I2C_SDA

PL100 1-2: 1.8V I/O power for codec (Default jumper config).

PL100 3-4: 1.8V I/O power for FTDI chip (Default jumper config).

5.10 TEST Header

Header for BT and Wi-Fi Disable.

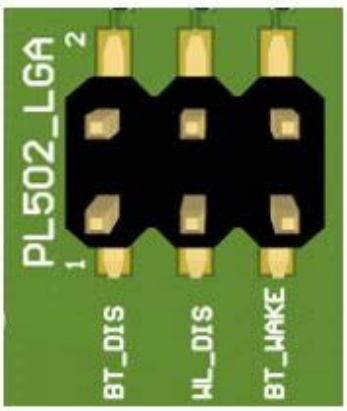


Figure 19: PL502 Test Header for LGA Module

PL502 1-2: LGA module BT_DIS pin for functional test.

PL502 3-4: LGA module WL_DIS pin for functional test.

PL502 5-6: LGA module BT_WAKE_HOST pin for functional test.

Note: Do not place the jumpers on this connector for normal operation.

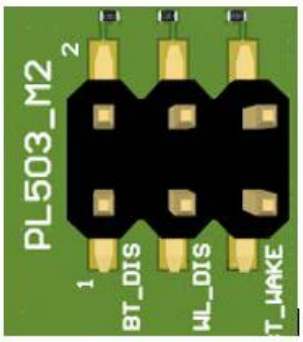


Figure 20: PL503 Test Header for M.2

PL503 1-2: M.2 BT_DIS pin for functional test.

PL503 3-4: M.2 WL_DIS pin for functional test.

PL503 5-6: M.2 BT_WAKE_HOST pin for functional test.

Note: Do not place the jumpers on this connector for normal operation.

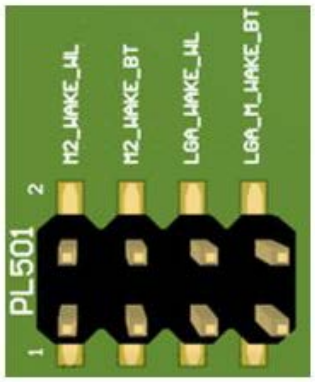


Figure 21: PL501 Test Header for LGA and M.2

PL501 1-2: M.2 HOST_WAKE_WL pin for functional test.

PL501 3-4: M.2 HOST_WAKE_BT pin for functional test.

PL501 5-6: LGA module HOST_WAKE_WL pin for functional test (Default jumper config).

PL501 7-8: LGA module HOST_WAKE_BT pin for functional test (Default jumper config).

Note: Either LGA module or M.2 card must be present on EVB. Test only one form factor.

6 WE310K6-P Basic Operations

6.1 General Information on Power Supply

The EVB can be powered in two ways.

1. 3.3V power can be supplied from the HOST PCIe slot.
2. 3.3V power can be supplied from external DC power supply.

Make sure to place jumper on PL400 2-3 if the EVB should be powered from external power supply.

7 Acronyms and Abbreviations

Table 4: Acronyms and Abbreviations

Acronym	Definition
PCIe	Peripheral Component Interconnect Express
CLK	Clock
HCI	Host Controller Interface
HS	High Speed
I/O	Input Output
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
BT	Bluetooth
UART	Universal Asynchronous Receiver Transmitter
WLAN	Wireless LAN
USB	Universal Serial Bus
I2C	Inter-integrated circuit

8 Related Documents

Refer to https://dz.telit.com/ for current documentation and downloads.

Table 5: Related Documents

S.no	Book Code	Document Title
1	1VV0301856	WE310K6-P Module Hardware User Guide

9 Document History

Table 6: Document History

Revision	Date	Changes
0	2023-08-09	First Issue

From Mod.0818 Rev.11

Technical Documentation