TMPM440 Group

The TMPM440 Group is a high-performance 32-bit RISC microprocessor product group based on the ARM Cortex® -M4F core containing FPU.

The TMPM440 Group incorporates three arithmetic circuits including the CPU, FPU and PSC. It has developed as a succeeding version of TMP19A44FE/F10XBG Toshiba original microcontroller. The target applications are digital equipment such as a single-lens reflex camara and amusement machines.

These three arithmetic circuits operate in parallel, so that decentralized data processing enables process performance to improve.

Thanks to the built-in "100MHz non-wait access Flash ROM", a greatly reduced consumption current achieves without impairment of the high-performance.

The TMPM440 Group has 228 pins and various peripheral functions, thus they are suitable for use as platforms of a surveillance camera and amusement devices.

Application	Peripheral functions suitable for each application
 Surveillance camera	Built-in three types of arithmetic circuits. They can operate in parallel. High-resolution PPG output (TMRD)
 Amusement device	Various timers and serial interfaces.

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Please contact your Toshiba sales representative for updated information before designing your products.

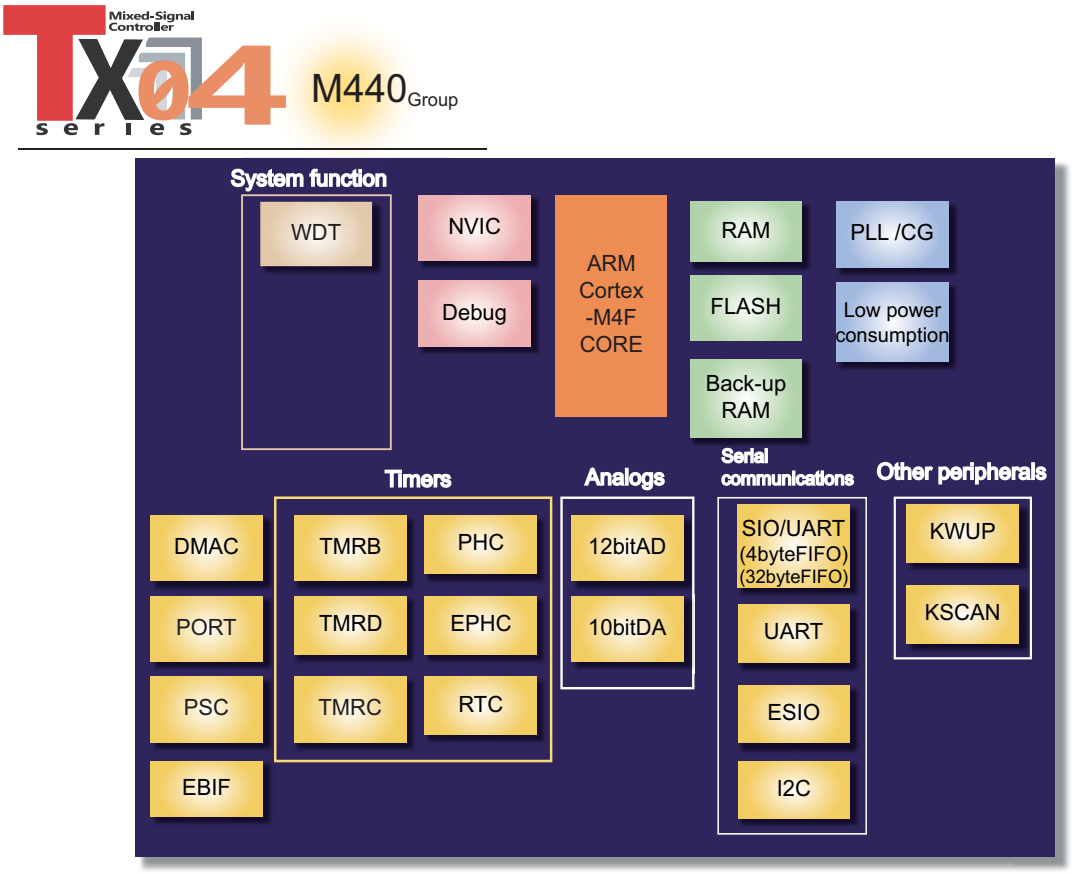


Figure 1-1 Block diagram of TMPM440 Group

1.1 Product Lineup of TMPM440 Group

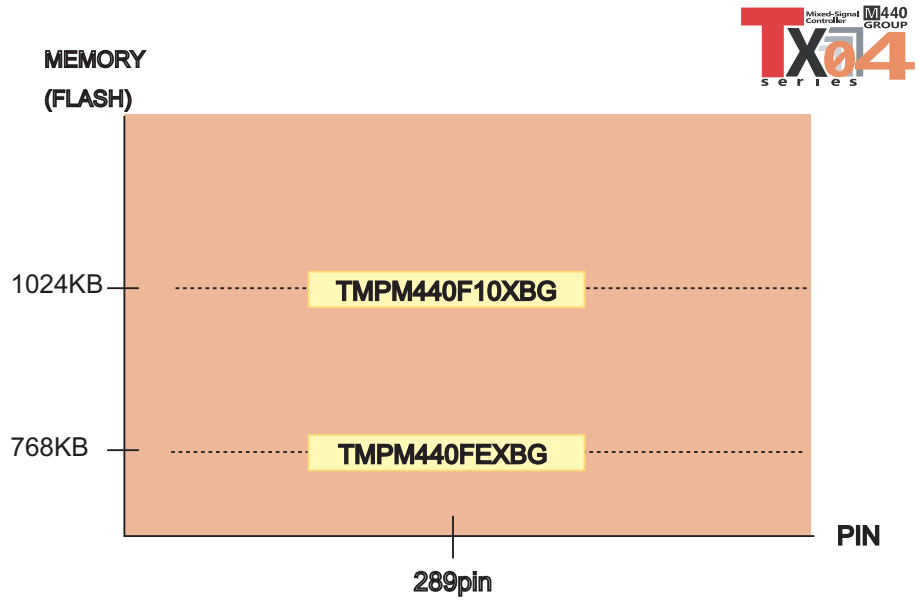


Table 1-1 A product list described in functional order

Peripheral functions		Product name	
		TMPM440FEXBG	TMPM440F10XBG
Memory	Flash	768 KBytes	1024 KBytes
	RAM	56 KBytes, back-up RAM 8 KBytes, PSC RAM (data area/code area) 8 KB/8 KB	
External bus interface	EBIF	Expandable up to 32 MB, 2 channels of $\overline{CSx}$	
External interrupt	INT	External interrupt pin: 24	
	NMI	0	0
DMA	DMA	3 units (2 channels, 16 factors per unit)	3 units 2 channels, 16 factors per unit)
PSC	PSC	1 unit	1 unit
Input/output port	Input/output	207	207
	Input	20	20
	Output	1	1
	5V-tolerant	14	14
Timer function	TMRB	20 channels	20 channels
	TMRD	1 block	1 block
	TMRC	1 unit	1 unit
	PHC	2 channels	2 channels
	EPHC	1 channel	1 channel
	RTC	1 channel	1 channel
Serial communication function	SIO/UART	6 channels	6 channels
	UART	2 channels	2 channels
	ESIO	3 channels	3 channels
	I2C	1 channel	1 channel
Analog function	ADC	3 units (8 channels + 8 channels + 4 channels)	3 units (8 channels + 8 channels + 4 channels)
	DAC	2 channels	2 channels
Other peripheral functions	KWUP	2 units (40 channels)	2 units (40 channels)
	KSCAN	8 inputs × 8 outputs	8 inputs × 8 outputs
System function	WDT	1 channel	1 channel
Debug interface	Debug	JTAG, SWD	
Package		VFBGA289 (11mm x 11mm, 0.5mm pitch)	

1.2 Functional Description

1. ARM Cortex-M4F core and FPU are incorporated.

   Mass data processing and calculation can be executed at high speed.

2. Flash memory and RAM

   Flash memory: Large capacity Flash memories of 768 KBytes and 1024 KBytes are available.

   RAM: Large capacity RAM of 56 KBytes and backup RAM of 8 KBytes to store the contents used in the low power consumption mode are housed. Furthermore, data area of 8 KBytes and code area of 8 KBytes for the PSC are incorporated.

3. External bus interface (EBIF)

   Built-in external bus interface is incorporated if further large capacity Flash memory and RAM are needed.

   Expandable up to 32 MBytes (shared with program and data)

4. Clock control (CG)

   The built-in PLL can use an inexpensive oscillator even when the MCU operates at high speed.

   Also, the clock gear function can reduce a power consumption by slowing the core's operation speed while peripheral functions operate at high speed.

5. Low power consumption function

   The following low power consumption modes are available in the TMPM440 Group.

   - IDLE mode: Stops the CPU and specified peripheral functions.
   - STOP1 mode: Stops all peripheral functions including an oscillator, except some peripheral functions. A greater reduction in power consumption can be achieved compared to the IDLE mode.
   - STOP2 mode: Stops product-specified peripheral functions and stops a power supply to other peripheral functions. Therefore, the STOP2 mode can achieve a greater reduction in power supply than the STOP1 mode.

6. External interrupt function

   The MCU has external interrupt pins that can specify a 7-level of interrupt priority.

   These external interrupt pins are also used for releasing the low-power consumption mode.

7. Bus matrix

The bus matrix is optimized to operate built-in multiple bus masters efficiently.

The TMPM440 Group incorporates the following bus masters:

- DMA controller

  Three units of DMA controllers that have 2 channels with 16 startup factors per unit are incorporated.

  In addition to the memory-memory transfer, data is transferred from/to the registers of built-in peripheral functions at high speed.

8. Programmable servo/sequence controller (PSC)

The PSC deals some processes, so that the performance of whole process improves and the CPU arithmetic tasks are distributed. This reduces the power consumption.

9. Input/output ports

Normal input/output ports, input ports, an output port and 5V-tolerant ports are incorporated.

10. Timer functions

The following timer functions are available in the TMPM440 Group.

- 16-bit timer/event counter (TMRB)
- 32-bit timer (TMRC)
- High-resolution 16-bit timer (TMRD)
- 2-phase pulse input counter (PHC)
- Enhanced 2-phase pulse input counter (EPHC)
- Real-time clock (RTC)

11. Serial communication functions

The following serial communication functions are available in the TMPM440 Group.

- Serial channels (SIO/UART)
- Asynchronous serial communication interface using flow control mechanism (UART)
- Enhanced serial I/O interface (ESIO)
- Serial bus interface (I2C)

12. Analog functions

The following analog functions are available in the TMPM440 Group.

- 12-bit analog-digital converter (ADC)
- 10-bit digital-analog converter (DAC)

13. Other peripheral functions

The following other peripheral functions are available in the TMPM440 Group.

- Key-on wake-up (KWUP) function
- Key-matrix scan (KSCAN) function

14. System functions

The following system-related function is available in the TMPM440 Group.

- Watchdog timer (WDT)

15. Endian

- Supports big-endian and little-endian.

16. Debug interface

- Supports JTAG/SWD.
- Supports SWV and TRACE Data as ETM.

17. JTAG interface

- Supports the boundary scan.

1.3 Operating Conditions

1. Maximum operating frequency
   - 100MHz

2. Operating voltage range
   - 2.7 to 3.6V

3. Operating temperature range
   - –40°C to 85°C (except when Flash W/E and debugging)
   - 0°C to 60°C (Flash W/E)

1.4 Package

The following package is available for the TMPM440 Group.

- VFBGA289 (11mm x 11mm, 0.5mm pitch)

1.5 Functional Description

This section describes peripheral functions built-in the TMPM440 Group.

1.5.1 Flash Memory

The capacities and configurations of Flash memory for the TMPM440 Group are as follows:

Writing is performed in the unit of pages.

One word means 32 bits.

Table 1-2 Capacities and configurations of Flash memory

Products	Capacity (Bytes)	Block configuration (pcs)					Number of words per page	Write time (s)		Erase time (s)	
		128K (Bytes)	64K (Bytes)	32K (Bytes)	16K (Bytes)	8K (Bytes)		1 page	1 Chip	1 block	1 Chip
TMPM440F10XBG	1024K	0	12	4	4	8	64	0.00125	5.12	0.1	1.6
TMPM440FEXBG	768K	0	8	4	4	8		0.00125	3.84		

Note: This table shows each register initial value after reset. A data transfer time is not included. An write time per chip differs depending on users' reprogramming method.

1.5.2 RAM

The RAM capacities for the TMPM440 Group are as follows:

The contents of RAM except backup RAM are not maintained when the MCU enters in the STOP2 mode.

Necessary data in the STOP2 mode should be stored in the backup RAM.

Table 1-3 RAM capacity and configuration

Products	RAM capacity (Bytes)	Backup RAM capacity (Bytes)	PSC RAM (Bytes) (Data area/code area)
TMPM440FEXBG TMPM440F10XBG	56 K	8 K	16 K (8 K/8 K)

1.5.3 External Bus Interface (EBIF)

The outline of the external bus interface of the TMPM440 Group is as follows:

Table 1-4 Outline of external bus interface

Functions	Features
Supported memory	NOR Flash memory, SRAM, peripheral I/O Selectable from separate bus or multiplex bus mode
Data bus width	Either an 8- or 16-bit width is settable for each channel.
Chip select signals	2 channels ($\overline{CS0}$, $\overline{CS1}$)
Endian	Supports little-endian and big-endian
Clock output function	Enables to output a clock synchronizing with the bus cycle.
Accessible area	Supports up to 32MB accessible areas. 0x6000_0000 to 0x61FF_FFFF (settable up to 16MB in each CS.)
Internal wait function	Up to 15 cycles can be inserted per channel.
ALE assert time	An assert time is selectable from 1, 2,3 or 5 cycles in each channel.
Setup cycle insert function	$\overline{RD}$ and $\overline{WR}$ setup cycles can be inserted. (t_{AC} cycle duration can extend.)
Recovery (Hold) cycle insert function	When external bus cycles successively continue, up to 8 dummy cycles can be inserted. (Settable in each channel.) $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ address/data hold cycles can be inserted. (t_{CAR} and t_{RAE} cycles can extend.)
Bus extension function	Values of the internal wait, ALE assert time, setup cycle and recovery cycle can be doubled or quadrupled. (Common in all channels.)
Control pins	Separate bus mode: D[15:0], A[23:0], $\overline{RD}$, $\overline{WR}$, $\overline{BELL}$, $\overline{BELH}$, $\overline{CS0}$, $\overline{CS1}$, ENDIAN Multiplex bus mode: AD[15:0], A[23:16], $\overline{RD}$, $\overline{WR}$, $\overline{BELL}$, $\overline{BELH}$, $\overline{CS0}$, $\overline{CS1}$, ALE, ENDIAN

1.5.4 Clock Control (CG)

The outline of clock control circuit of the TMPM440 Group is as follows:

1. Internal high-speed oscillation circuit:10MHz ± 10%
2. The external high-speed oscillation circuit or external clock input are selectable.
3. PLL (multiplier): Two PLL units are incorporated. The number of multiplications is selectable per unit according to oscillation frequencies of high-speed oscillation circuit shown below.

PLL	Number of multiplications	Peripheral function
PLL0	A factor of 5, 6, 8 and 10	fc, PSC, TMRD
PLL1	A factor of 8 and 10	ADC

4. Clock gear: Any high-speed clock (clock gear) is selectable from 1/1, 1/2, 1/4, 1/8 or 1/16 as the system clock (fsys).

1.5.5 DMA Controller (DMAC)

The MCU incorporates three DMA controllers containing 2 channels with 16 startup factors per unit.

1.5.5.1 Outline

The outline of DMA controllers is as follows:

Table 1-5 Outline of DMA (per unit)

Parameter	Function		Note
Number of channels	2 channels		-
Number of DMA requests	16 factors		-
DMA startup trigger	Started by hardware		Startup by a DMA request from peripheral functions
	Started by software		Set by registers
Bus master	32bit × 1 (AHB)		-
Priority	Higher: ch0 Lower: ch1		Fixed
FIFO	4word × 2ch		-
Transfer data size	8-/16-/32-bit		Transfer data size can be set for transfer source and destination respectively.
Burst size	1/4/8/16/32/64/128/256		-
Number of transfers	1 to 4095		-
Address	Transfer source address	Increment Not increment	Settings of source and destination addresses can be chosen either from "increment" or "not increment." (Address wrapping is not supported.)
	Transfer destination address	Increment Not increment	
Endian	Little-endian/big-endian		-
Transfer type	Peripheral to Memory Memory to Peripheral Memory to Memory Peripheral to Peripheral Note) TMPM440 Group does not support "Peripheral to Peripheral" as a transfer type.		If "Memory to Memory" is selected as a transfer type, a hardware startup by DMA is not supported. Allocations of peripheral functions as source and destination are limited.
Interrupt function	Transfer completion interrupt (INTDMACxTC) Error interrupt (INTDMACxERR)		-
Special Function	Scatter/gather function		-

1.5.5.2 A List of DMA Startup Factors

The following tables list startup factors in each unit.

Table 1-6 A list of DMA startup factors

Startup factor No.	Unit A (ch0,1)		Unit B (ch0,1)		Unit C (ch0,1)	
	Burst	Single	Burst	Single	Burst	Single
0	ESIO reception (channel 0)	–	ESIO reception (channel 1)	–	ESIO reception (channel 2)	–
1	ESIO transmission (channel 0)	–	ESIO transmission (channel 1)	–	ESIO transmission (channel 2)	–
2	Normal AD conversion completion (Unit A)	–	Normal AD conversion completion (Unit B)	–	Normal AD conversion completion (Unit C)	–
3	SIO/UART reception (channel 3)	–	SIO/UART reception (channel 4)	–	SIO/UART reception (channel 5)	–
4	SIO/UART transmission (channel 3)	–	SIO/UART transmission (channel 4)	–	SIO/UART transmission (channel 5)	–
5	SIO/UART reception (channel 0)	–	SIO/UART reception (channel 1)	–	SIO/UART reception (channel 2)	–
6	SIO/UART transmission (channel 0)	–	SIO/UART transmission (channel 1)	–	SIO/UART transmission (channel 2)	–
7	TMRB00 Comparator 1 (CP1) match detection	–	UART reception (channel 0)	UART reception (channel 0)	UART reception (channel 1)	UART reception (channel 1)
8	TMRB04 Comparator 1 (CP1) match detection	–	UART transmission (channel 0)	UART transmis-sion (channel 0)	UART transmission (channel 1)	UART transmis-sion (channel 1)
9	TMRB10 Comparator 1 (CP1) match detection	–	TMRB08 Input capture 0 interrupt	–	TMRB19 Input capture 0 interrupt	–
10	TMRB14 Comparator 1 (CP1) match detection	–	TMRC input capture 0 interrupt	–	TMRC input capture 2 interrupt	–
11	TMRC compare 0 match	–	TMRC input capture 1 interrupt	–	TMRC input capture 3 interrupt	–
12	TMRC compare 1 match	–	Highest priority AD con-version completion (Unit B)	–	Highest priority AD con-version completion (Unit C)	–
13	Highest priority AD con-version completion (Unit A)	–	PHCNT compare 0 match (channel 1)	–	EPHC Cycle 0 interrupt (channel 0)	–
14	PHCNT compare 0 match (channel 0)	–	TMRD00 compare match	–	TMRD10 compare match	–
15	$\overline{\text{DREQA}}$ pin	–	$\overline{\text{DREQB}}$ pin	–	$\overline{\text{DREQC}}$ pin	–

1.5.6 Timer Function

1.5.6.1 16-bit timer/event counter (TMRB)

(1) Outline

The TMRB is a peripheral function that incorporates the 16-bit counter and can be used as a timer or event counter.

It captures the value of the 16-bit counter at a specified timing.

Multiple channels can be started simultaneously and can be started synchronously with external triggers.

(2) Operation mode

The TMRB has the following operation modes. These operation modes can be switched in each channel.

(a) Interval timer mode

The mode is one that counts up a 16-bit counter at a specified clock count of the source clock.

When the counter matches a preset value, an interrupt request occurs.

The counter value can also be captured by the capture register at a specified timing (at a change of software capture, capture trigger and input capture input pin).

(b) Event counter mode

The mode is one that counts up a 16-bit counter using an external clock instead of the source clock in the interval timer mode.

The interrupt and capture function can be used in the same way as the interval timer mode (the pin used by an external clock input cannot be used as a capture input).

(c) Programmable rectangular wave output (PPG) mode

The mode is one that outputs a rectangular waveform at a specific frequency and duty ratio to the output pins.

Either "active-low" or "active-high" logic can be selected for the output pins.

(d) Programmable rectangular wave output (PPG) external trigger mode

The mode is one that starts a 16-bit up-counter at a specified timing. It outputs a rectangular waveform at a specified frequency and duty ratio to the output pins.

Functions other than the above-mentioned are the same as the programmable rectangular waveform output (PPG) mode.

(3) Interrupt request

The TMRB has the following interrupt requests:

(a) Compare match interrupt

When the 16-bit up-counter matches a preset value, a compare match interrupt request occurs. As the compare match interrupt request is a shared interrupt with an overflow interrupt, the interrupt handler detects the factor by reading the status flag.

(b) Overflow interrupt

When the 16-bit up-counter has overflowed, an overflow interrupt request occurs. As the overflow interrupt request is a shared interrupt with a compare match interrupt, the interrupt handler detects the factor by reading the status flag.

(c) Input capture interrupt

When the capture register captures the value of the 16-bit up-counter, an input capture interrupt request occurs.

1.5.6.2 High-resolution 16-bit timer (TMRD)

(1) Outline

The TMRD is a peripheral function that incorporates two units of the timer unit and clock setting circuit (prescaler). It can be used as a timer or rectangular output.

A rectangular output can be used in the 1-bit modulation and can be adjusted on a duty ratio that is pseudo-higher resolution than fc.

These two timer units can operate independently or in an interlocked fashion.

(2) Operation mode

The TMRB has the following operation modes. These operation modes can be switched in each channel.

(a) 16-bit interval timer

1. Timer mode

   Two timer units operate independently.

   The mode is one that counts up a 16-bit counter at a specified clock count of the source clock.

   Two types of the counter operation are available. According to the setting, different operations can be specified in each timer unit.

   Regardless of the counter operation, if the value of the counter matches a specified value, an interrupt request occurs.

2. Interlock timer (synchronous start) mode

   The mode is one that the both counters in each timer unit can start simultaneously. A timer cycle is settable respectively.

(b) 16-bit programmable rectangular waveform output (PPG)

The mode is one that outputs a rectangular waveform at a specific frequency and duty ratio to the output pins.

Either "active-low" or "active-high" logic can be selected for the output pins.

1. PPG mode

   Two timer units operate independently. In this mode, the TMRD can output programmable rectangular waveforms in frequency and duty ratios respectively.

   These two units output two channels of rectangular waveforms with the same frequency respectively.

2. Interlock PPG mode

   The mode is one in which two timer units operate in an interlocked fashion via the comparator containing the phase shift function.

(3) Interrupt request

The TMRD has the following interrupt requests:

(a) Compare match interrupt

When the 16-bit up-counter matches a preset value, a compare match interrupt request occurs. As the compare match interrupt request is a shared interrupt with an overflow interrupt, the interrupt handler detects the factor by reading the status flag.

(b) Overflow interrupt

When the 16-bit up-counter has overflowed, an overflow interrupt request occurs. As the overflow interrupt request is a shared interrupt with a compare match interrupt, the interrupt handler detects the factor by reading the status flag.

1.5.6.3 32-bit timer (TMRC)

(1) Outline

TMRC is a peripheral function that incorporates a 32-bit time-base timer, 32-bit input capture register and 32-bit compare register and can be used as a timer or event counter.

It also has a noise canceller that removes a noise from an external clock of the 32-bit time-base timer and from inputs of the 32-bit input capture. Noise cancellation is implemented without external circuits.

(2) Operation mode

The TMRC has the following operation modes. These operation modes can be switched in each channel.

(a) 32-bit interval timer mode

The mode is one that counts up a 32-bit counter at a specified clock count of the source clock.

When the counter matches a preset value, an interrupt request occurs.

The counter value can also be captured by the capture register at a specified timing (at a change of software capture, capture trigger and input capture input pin).

(b) 32-bit event counter mode

The mode is one that counts up a 32-bit counter using an external clock instead of the source clock in the interval timer mode.

The interrupt and capture function can be used in the same way as the interval timer mode. (The pin used by an external clock input cannot be used as a capture input.)

(c) Compare output

The mode is one that outputs a rectangular waveform at a specific frequency and duty ratio to the output pins.

Either "active-low" or "active-high" logic can be selected for the output pins.

(3) Interrupt request

TMRC has the following interrupt requests:

(a) Compare match interrupt

When the 32-bit up-counter matches a preset value, a compare match interrupt request occurs.

(b) Overflow interrupt

When the 32-bit up-counter has overflowed, an overflow interrupt request occurs.

(c) Input capture interrupt

When the capture register captures the value of the 32-bit up-counter, an input capture interrupt request occurs.

1.5.6.4 2-phase pulse input counter (PHC)

(1) Outline

The PHC is a peripheral circuit that incorporates the 16-bit counter counting a 2-phase pulse which has a 90 degree phase difference. It counts outputs from a rotary encoder.

The 16-bit counter has three selectable operation modes.

(2) Operation mode

The PHC has the following counter operation modes. A combination of asynchronous 2-phase pulse inputs determines whether the 16-bit counter counts up or counts down.

(a) Normal mode

The mode is one in which the 16-bit counter counts up/down every time a combination of the 2-phase pulse inputs changes four times.

(b) 4-fold multiplication mode

The mode is one in which the 16-bit counter counts up/down every time a combination of the 2-phase pulse inputs.

(c) Twofold multiplication mode

The mode is one in which the 16-bit counts up/down every time either of 2-phase pulse inputs changes.

(3) Interrupt request

The PHC has the following interrupt requests:

(a) Compare 0 match interrupt

When the 16-bit up-counter matches a preset value, an interrupt request occurs.

(b) Compare 1 match interrupt

When the 16-bit up-counter matches a preset value, an interrupt request occurs.

(c) Interrupts when the counter counts up or counts down

An interrupt occurs every time the counter counts up or counts down.

1.5.6.5 Enhanced 2-phase pulse input counter (EPHC)

(1) Outline

The EPHC is a peripheral circuit that incorporates the 16-bit counter counting a 2-phase pulse that has a 90-degree phase difference. It counts outputs from a rotary encoder.

The 16-bit counter has three selectable operation modes.

(2) Operation mode

The EPHC has selectable operation modes in each function as follows:

(a) 2-phase pulse input counter function

The 2-phase pulse input counter function is a peripheral function that increments/decrements the up/down-counter depending on the transition of the combination of 2-phase input pulse or transition of 1-phase input pulse.

1. 1-pulse counter mode

   This mode increments/decrements the 16-bit up/down-counter depending on the transition of two inputs states.

2. 2-phase pulse counter mode

   This mode increments/decrements the 16-bit up/down-counter depending on the transition of two input pulse.

   A combination order of the two pulses can be reversed with the setting.

(b) Cycle phase difference measurement function

The cycle phase measurement captures a value of the 24-bit free-running counter on rising/falling edge of 2-phase input pulse. Based on this value, it measures a cycle of 2-phase input and phases between edges.

1. Cycle measurement

   This function measures a cycle of two input pulses.

   A measurement period is selectable from a rising edge to rising edge; falling edge to falling edge.

2. Phase difference measurement

   This function measures a phase difference between two input pulses.

   A positive phase and negative phase can be selected.

(3) Interrupt request

The EPHC has interrupt requests in each function.

(a) 2-phase pulse input counter function

1. Compare match interrupt

   When the 16-bit up-counter matches a preset value, a compare match interrupt request occurs. As the compare match interrupt request is a shared interrupt with an overflow/underflow interrupt, the interrupt handler detects the factor by reading the status flag.

2. Overflow/underflow interrupts of the up-down counter

   When the 16-bit up-counter has overflowed/underflowed, an overflow/underflow interrupt request occurs. As the overflow/underflow interrupt request is a shared interrupt with a compare match interrupt, the interrupt handler detects the factor by reading the status flag.

(b) Cycle phase difference measurement function

1. Cyclic interrupt

   A cyclic interupt occurs when data is stored in the cycle counter register.

2. Phase error interrupt

   A phase error interrupt occurs whenever an opposite pulse signal against the preset phase is input.

3. Overflow interrupt

   An overflow interrupt occurs when the 24-bit free-running counter overflows.

1.5.6.6 Real-time clock (RTC)

(1) Outline

The RTC is a peripheral function that has a second counter, clock function, leap-year calender function.

It also has the alarm function that generates an interrupt on a specified time and date.

Because the RTC operates on a low-speed external oscillation clock, it can operate in the low power consumption mode such as STOP1 and STOP2 modes. In addition, the MCU can be returned from the low power consumption mode by an interrupt request of RTC.

(2) Operation mode

The RTC has the following operation modes:

(a) Clock function

The clock can select either 24-hour or 12-hour clock.

(b) Alarm function

Combined with the clock and calender function, an interrupt request can be generated on a preset time and day.

(3) Interrupt request

The RTC has the following interrupt requests:

(a) 1Hz interrupt, 2Hz interrupt, 4Hz interrupt, 8Hz interrupt, 16Hz interrupt

These interrupt requests are generated at a certain cycle.

(b) Alarm interrupt

This interrupt request is generated on a preset time and date that are scheduled in the clock and calender.

1.5.7 Serial Interface Function

1.5.7.1 Serial channel (SIO/UART)

(1) Outline

The serial function is a peripheral function that switches the operation modes between the synchronous communication mode (I/O interface mode) and asynchronous communication mode (UART mode).

It has the 4-stage and 32-stage FIFO and baud-rate generator that enable communications at various transfer rates.

(2) Operation mode

The SIO/UART has the following operation modes:

(a) I/O interface mode

The I/O interface mode is the mode where data is transferred using the half-duplex or full-duplex communication system in synchronization with clock signals.

In the I/O interface mode, a switch between a master and slave, designation of LSB and MSB of transfer data, and designation of a transfer clock edge of the slave mode are possible.

In addition, the hold time of the last bit and level of the data output pin after the last bit is output can be specified.

(b) UART mode

The UART mode is one in which data is transferred at a preset transfer rate.

The flow control is implemented using CTS.

The data bit length is selectable from 7-bit, 8-bit or 9-bit. When a 7-bit or 8-bit data length is selected, a parity bit can be added.

(3) Interrupt request

The SIO/UART has the following interrupt requests:

(a) I/O interface mode

1. Transmit interrupt

   When the transmit double buffer is disabled, if data transmission is complete, a transmit interrupt request occurs.

   When the transmit double buffer or transmit FIFO is enabled, if transmit data has been transferred from the transmit double buffer of transmit FIFO to the shift register, a transmit interrupt request occurs.

2. Receive interrupt

   When data reception is complete, a receive interrupt request occurs. When the receive FIFO is enabled, if the data has reached to the preset fill-level of FIFO, a reception interrupt request occurs.

(b) UART mode

1. Transmit interrupt

   When the transmit double buffer is disabled, a transmit interrupt occurs immediately before the STOP bit is output.

   When the transmit double buffer or transmit FIFO is enabled, if transmit data has been transferred from the transmit double buffer or transmit FIFO to the shift register, a transmit interrupt request occurs.

2. Receive interrupt

   A receive interrupt request occurs around the center of the 1st STOP bit.

1.5.7.2 Asynchronous serial communication interface with flow control (UART)

(1) Outline

The UART is a peripheral function that supports asynchronous serial communications with flow control including IrDA.

It has the 32-stage FIFO.

(2) Operation mode

The UART has the following operation modes:

(a) UART mode

The mode is one in which flow control is implemented using CTS and RTS. A control pin status of MODEM can also be read by the status registers. A control pin status of MODEM can be controlled by the control registers.

A data bit length is selectable from 5-bit, 6-bit, 7-bit or 8-bit. In addition, a parity bit can be added.

(b) IrDA mode

This mode is in conformity with IrDA 1.0.

The low power consumption mode in which consumption current is reduced in communications is available.

(3) Interrupt request

The UART has the following interrupt requests:

(a) UART interrupt request

When data has reached to a preset level of the FIFO, an UART interrupt request occurs. If a transfer error occurs, an UART interrupt request also occurs.

As the UART interrupt request is a shared interrupt with multiple factors, the interrupt handler detects the factor by reading the status flag.

1.5.7.3 Enhanced serial interface (ESIO)

(1) Outline

The Enhanced Serial I/O (ESIO) is a serial interface that enables synchronous communications at high speed.

There are two types of selectable communication modes such as SPI mode and SIO mode. In the SPI mode, a CS (Chip Select) signal is used at communications; in the SIO mode, a CS signal is not used at communications.

The ESIO incorporates a baud-rate generator that can communicate at various transfer speeds. It also has the error detection function that can detects an error between frames using a parity bit.

The ESIO enables high-speed communications and can determine the number of data lines for transmission/reception in a range from 1 to 4.

(2) Operation mode

The ESIO employs the following communication methods:

(a) SPI communication

SPI communication method can connect with two slave devices using two chip select (CS) signals; however only one slave device can communicate with the master at a time.

(b) SIO communication

This communication method does not use chip select (CS) signals. Only one slave device can be connected.

(3) Interrupt request

The ESIO has the following interrupt requests:

(a) Transmit interrupt

Transmit interrupts can occur in the half-duplex (transmission) or full-duplex mode in the transmit mode.

One transmit interrupt signal is provided for a transmit completion interrupt and transmit FIFO interrupt. Each interrupt can be set to enable or disable respectively.

A transmit interrupt is determined by reading a status flag when an interrupt occurs.

1. Transmit completion interrupt

   A transmit completion interrupt occurs when one frame has been transferred in the single transfer mode; in the burst transfer mode, it occurs at a CS signal negated timing after the specified number of burst transfers has been done.

2. Transmit FIFO interrupt

   While the value of the current fill level is greater +1 than the specified transmit interrupt generation condition (fill level), if a data transfer occurs from the transmit FIFO to the transmit shift register, and a fill level of the transmit FIFO is -1. As a result, the value of current fill level and the transmit interrupt generation condition (fill level) become the same value, so that a transmit interrupt occurs once.

(b) Receive interrupt

A receive interrupt occurs in the half-duplex (reception) or full-duplex communications.

One receive interrupt signal is provided for a receive completion interrupt and receive FIFO interrupt. Each interrupt can be set to enable or disable respectively.

A receive interrupt is determined by reading a status flag when an interrupt occurs.

1. Receive completion interrupt

   A receive completion interrupt occurs when one frame has been transferred in the single transfer mode; in the burst mode, it occurs at a CS signal negated timing after the specified number of burst transfers has been done.

2. Receive/transmit FIFO interrupt

   While the value of the current fill level is smaller than the specified receive interrupt generation condition (fill level), if a data transfer occurs from the receive shift register to the receive FIFO, a fill level of the transmit FIFO is +1. As a result, the value of the current fill level and the receive interrupt condition (fill level) become the same value, so that a receive/transmit FIFO interrupt occurs once.

(c) Error interrupt

One error interrupt signal is provided for a vertical parity receive error interrupt and horizontal parity receive error interrupt. Each interrupt can be set to enable or disable respectively.

An error interrupt is determined by reading a status flag when an interrupt occurs.

1.5.7.4 I2C bus interface (I2C)

(1) Outline

This peripheral function supports the I2C bus standard mode and fast mode.

(2) Maximum transfer rate

- Standard mode

  100 kHz (Master mode, slave mode)
- Fast mode

  400 kHz (Master mode, slave mode)

(3) Interrupt request

The I2C has the following interrupt request.

(a) I2C interrupt request

An I2C interrupt request occurs when transmission or reception is complete.

1.5.8 Analog Function

1.5.8.1 12-bit analog digital converter (ADC)

(1) Outline

This 12-bit analog digital converter converts data at high speed.

Startup by software, trigger inputs and trigger inputs from the peripheral functions are available.

In addition, an interrupt, which occurs when a preset value is detected, is available.

(2) Operation mode

The ADC has the following operating modes:

(a) Fixed single conversion mode

A preset analog input is converted to a digital value.

(b) Scan single conversion mode

Analog inputs in a preset range are converted to digital values.

(c) Fixed repeat conversion mode

Preset analog inputs are repeatedly converted to digital values for a specified number of iterations

(d) Scan repeat conversion mode

Analog inputs in a preset range are repeatedly converted to digital values.

(3) Minimum conversion time

1.0ms@ ADC conversion clock 40MHz

(4) Interrupt request

The ADC has the following interrupt requests.

(a) Normal AD conversion completion interrupt request

A normal AD conversion completion interrupt request occurs when the normal AD conversion is complete.

(b) Highest priority AD conversion completion interrupt request

A highest priority AD conversion completion interrupt request occurs when the highest priority AD conversion is complete.

(c) AD monitor function interrupt

An AD monitor function interrupt occurs when the AD converter detects a preset conversion value.

1.5.8.2 10-bit Digital-Analog Converter (DAC)

(1) Outline

This 10-bit digital analog converter outputs a preset voltage.

Reference voltage pins for resistors and DA converter can switch between connection and disconnection.

(2) Maximum settling time

Immediately previous setting value	Maximum settling time
More than ± 64LSB	1000 μs
Within ± 64LSB	200 μs

1.5.9 Other Peripheral Functions

1.5.9.1 Key-on wake-up (KWUP)

(1) Outline

The key-on wake-up is a return function from the STOP1 and STOP2 mode that uses a key input interrupt.

1.5.9.2 Key matrix scan (KSCAN)

(1) Outline

The key matrix scan (KSCAN) is a peripheral function that controls a key matrix up to 64 (8 inputs × 8 outputs).

It provides the chattering elimination and key determination function.

By using the KSCAN and key-on wake-up functions in combination, an operation mode can easily be released from the STOP1 and STOP2 modes.

(2) Interrupt request

KSCAN has the following interrupt request:

(a) KSCAN interrupt request

If a key scan input is modified, a KSCAN interrupt occurs.

1.5.10 System Function

1.5.10.1 Watchdog timer (WDT)

(1) Outline

The WDT is a peripheral function that detects overflow of the binary counter and generates an interrupt request or resets the MCU. This is caused when a binary counter cannot be cleared within the preset detection time.

When WDT is programmed to clear the binary counter within the preset detection time beforehand, WDT can detect an MCU malfunction.

When the binary counter overflows, the watchdog timer out pin outputs "Low". This informs a MCU malfunction to the external ports on the circuit breadboard.

(2) Interrupt request

The WDT has the following interrupt requests:

(a) Watchdog timer interrupt request

When WDT detects that the binary counter overflows, it generates a watchdog timer interrupt request. The watchdog timer interrupt is a non-maskable interrupt.

1.6 Pin Layout

A pin layout of the TMPM440 Group is shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	BSC	PAC1	PAE6	PAE3	PAD7	PAD3	PAD0	PJ0	PJ1	PJ2	PJ3	PK0	PK5	PK4	PK6	PL0	PL1	PL2	PL3	PG0
B	PAC2	PAC0	PAC3	PAE4	PAE1	PAD6	PAD2	PJ4	PJ5	PJ6	PJ7	PK1	PV2	PW0	PW4	PL4	PL5	PL6	PL7	PM6
C	ADCVDD3	ADCVSS	PAA0	PAE7	PAE5	PAE2	PAD5	PAD1	PV4	PW1	PW5	PK2	PV7	PW6	PM2	PM1	PM0	PG1	PM7	PM4
D	ADCVREFH	ADCVREFL	PAA1															PG2	PG3	PM5
E	ADAVDD3	ADAVSS	PAA2															PG4	PG6	PH4
F	ADAVREFH	ADAVREFL	PAA4			PAA3	PAE0	PV1	PV5	PW3	PW7	PV0	PW2	PK7	PG5			PG7	PH1	PH5
G	ADBVDD3	ADBVSS	PAA5			PAA6	PAD4	PV3	DVSS	DVSS	DVSS	PV6	PK3	PM3	PH0			PH3	PH7	PH6
H	ADBVREFH	ADBVREFL	PAB2			PAB0	PAA7	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	PH2	PR3			PR0	PR2	PR1
J	DAVREFL	DAVSS	PAB7			PAB3	PAB1	DVSS	DVSS				DVSS	PY3	PY1			PR5	PR4	ENDIAN
K	DAVDD3	DAVREFH	DAAOUT			PAB5	PAB4	DVSS					DVSS	PT3	PY6			PY0	PR7	PR6
L	PU4	PU1	PU2			DABOUT	PAB6	DVDD3					DVDD3	PE0	PT5			PY5	PY4	PY2
M	PU6	PU5	PAF2			PU3	PN5	DVDD3					DVDD3	PE5	PE2			PT1	PT0	PY7
N	PU7	PAF5	PAF0			PU0	PN2	DVDD3	DVDD3	DVDD3	DVDD3	DVDD3	DVDD3	PF0	PD1			PT6	PT4	PT2
P	PAF1	PAF4	PAF3			PAH1	PAH7	PN6	DVDD3	DVDD3	DVDD3	DVDD3	PB2	PB7	PF4			PE4	PE1	PT7
R	RVDD3	BVDD3	PAF6			PAJ1	PAH4	PN1	PN3	PN7	PP7	PC2	PC6	PB3	PF3			PD0	PE6	PE3
T	DCSW	PAF7	PAG7															PD4	PD2	PE7
U	RVSS	BVSS	PAG4															PA3	PD5	PD3
V	DCV15IN	PAG5	PAG0	PAJ0	PAJ3	PAJ5	PAH0	PAH3	PN0	PP2	PP3	PC0	PC4	PB0	PB5	PF2	PF7	PA2	PD7	PD6
W	PAG3	PAG1	PAG2	PAG6	PAJ2	PAJ4	PAJ7	PAH5	PP1	PP0	PP4	PC1	PC5	PB1	PB6	PF5	PA0	PA7	PA4	PA6
Y	MODE	XT2	XT1	$\overline{\text{RESET}}$	X1	X2	PAJ6	PAH2	PAH6	PN4	PP5	PP6	PC3	PC7	PB4	PF1	PF6	PA1	PA5	FTEST3

Figure 1-2 Pin layout (TMPM440FE/F10XBG, VFBGA289 TOP VIEW)

1.7 Pin Names and Functions

1.7.1 Functional Pin Names and Functions

1.7.1.1 Pin Name of Peripheral Functions

Table 1-7 Peripheral functions, pin names and functions

Peripheral function	Pin name	Input or Output	Function
Clock/mode control	SCOUT	Output	Output pin for system clock
External bus interface	An	Input	Address bus output pin
	Dn	I/O	Data bus input/output pin
	ADn	I/O	Address/data bus input/output pin
	$\overline{RD}$	Output	Read strobe output pin
	$\overline{WR}$	Output	Write strobe output pin
	ALE	Output	Address latch enable output pin
	$\overline{BELL}$	Output	Byte enable output pin
	$\overline{BELH}$	Output	Byte enable output pin
	$\overline{CSn}$	Output	Chip select output pin
External interrupt	INTx	Input	External interrupt input pin External interrupt pin has a noise filter (filter width: 30ns typ.).
DMA	$\overline{DREQx}$	Input	DMA request input pin
PSC	PSCPTIO0 to 7	I/O	Input/output pin for PSC
PORT	PXn	I/O	Port pin
16-bit timer/event counter	TBxIN0	Input	Input capture input pin 0
	TBxIN1	Input	Input capture input pin 1
	TBxOUT	Output	Output pin
High-resolution 16-bit timer	TDxOUT0	Output	Timer output pin
	TDxOUT1	Output	Timer mode output pin
32-bit timer	TCTBTIN	Input	Clock input pin
	TCIN0 to 3	Input	Capture input pin
	TCOUT0 to 7	Output	Timer F/Foutput pin
2-phase pulse input counter	PHCxIN0	Input	2-phase pulse counter input pin
	PHCxIN1	Input	2-phase pulse counter input pin
Enhanced 2-phase pulse input counter	EPHCxIN0	Input	Enhanced 2-phase pulse counter input pin
	EPHCxIN1	Input	Enhanced 2-phase pulse counter input pin
Real-time clock	$\overline{ALARM}$	Output	Alarm output pin
SIO/UART	TXDx	Output	Data output pin
	RXDx	Input	Data input pin
	SCLKx	I/O	Clock input/output pin
	$\overline{CTSx}$	Input	Handshake input pin

Table 1-7 Peripheral functions, pin names and functions

Peripheral function	Pin name	Input or Output	Function
UART	TXD6 to 7	Output	Data output pin
	RXD6 to 7	Input	Data input pin
	$\overline{\text{CTS6}}$ to $\overline{\text{CTS7}}$	Input	Transmit enable input pin
	$\overline{\text{RTS6}}$ to $\overline{\text{RTS7}}$	Output	Transmit request output pin
Enhanced serial I/O	ESIOxTXD0 to 3	Output	ESIO data output pin
	ESIOxRXD0 to 3	Input	ESIO data input pin
	ESIOxSCK	I/O	ESIO clock input/output pin
	ESIOxCS0 to 1	Input	Handshake input pin
I2C	SDAx	I/O	Data input/output pin
	SCLx	I/O	Clock input/output pin
Analog-digital converter	AINAx	Input	Analog input pin
	AINBx	Input	Analog input pin
	AINCx	Input	Analog input pin
	$\overline{\text{ADTRGx}}$	Input	External trigger input pin
	$\overline{\text{ADTRGSNC}}$	Input	AD converter Unit A/Unit Bsynchronous startup request pin
Digital-analog converter	DAOUTx	Output	Analog output pin
Key-on wake-up	KWUPAx	Input	Key-on wake-up pin
	KWUPBx	Input	Key-on wake-up pin
Key scan matrix	KSIN0 to 7n	Input	Key scan input pin
	KSOUTx	Output	Key scan output pin

1.7.1.2 Debug Pins

Table 1-8 Debug pin name and function

Debug pin name	Input or Output	Functions
BSC	Input	JTAG debug mode/boundary scan mode switch input pin (TMPM462F15/F10XBG only)
TMS	Input	JTAG test mode selection input pin
TCK	Input	JTAG serial clock input pin
TDO	Output	JTAG serial data output pin
TDI	Input	JTAG serial data input pin
$\overline{\text{TRST}}$	Input	JTAG test reset input pin
SWDIO	I/O	Serial-wire data input/output pin
SWCLK	Input	Serial-wire clock input pin
SWV	Output	Serial-wire viewer output pin
TRACECLK	Output	Trace clock output pin
TRACEDATA0	Output	Trace data output pin 0
TRACEDATA1	Output	Trace data output pin 1
TRACEDATA2	Output	Trace data output pin 2
TRACEDATA3	Output	Trace data output pin 3

1.7.1.3 Control Pins

Table 1-9 Control pin names and functions

Control pin name	Input or Output	Functions
X1	Input	High-speed oscillation connection pin
X2	Output	High-speed oscillation connection pin
XT1	Input	Low-speed oscillation connection pin
XT2	Output	Low-speed oscillation connection pin
EHCLKIN	Input	External clock input pin
MODE	Input	Mode pin Must be fixed to "Low" level.
FTEST3	Input	Test pin Must be opened.
$\overline{\text{RESET}}$	Input	Reset signal input pin
ENDIAN	Input	Endian selection pin
$\overline{\text{BOOT}}$	Input	BOOT mode control pin BOOT mode control pin is sampled at rising edge of a reset signal input. If BOOT mode control pin is "Low", MCU becomes the single boot mod; if it is "High", MCU becomes the single chip mode. For details, refer to Chapter "Flash Memory."

1.7.1.4 Power Supply Pins

Table 1-10 Power supply pin names and functions

Power supply pin names	Function
RVDD3	Power supply pin for regulators
RVSS	GND pin for regulators
DVDD3	Power supply pin for digital DVDD3 supplies power to the following pins: PA to PH, PJ to PN,PP,PR,PT to PW,PY,PAD to PAH,PAJ, X1, X2, XT1, XT2, MODE, FTEST3, $\overline{\text{RESET}}$, $\overline{\text{BOOT}}$, BSC, ENDIAN
DVSS	GND pin for digital
BVDD3	Power supply pin for regulators used in always-ON area
BVSS	Power supply pin for regulators used in always-ON area
ADAVDD3 ADBVDD3 ADCVDD3	Power supply pin for ADC Unit x ADxVDD3 supplies power to the following pins: Unit A:PAA, Unit B:PAB, Unit C:PAC
ADAVSS ADBVSS ADCVSS	GND pin for ADC Unit x
ADAVREFH ADBVREFH ADCVREFH	Analog reference voltage for ADC Unit x (H)
ADAVREFL ADBVREFL ADCVREFL	Analog reference voltage for ADC Unit x (L)
DAVDD3	Power supply pin for DAC DAVDD3 supplies power supply to the following pins: DAOUT0, DAOUT1
DAVSS	GND pin for DAC
DAVREFH	Analog reference voltage for DAC (H)
DAVREFL	Analog reference voltage for DAC (L)
DCSW	SW pin for regulators
DCV15IN	1.5V input pin for input regulators

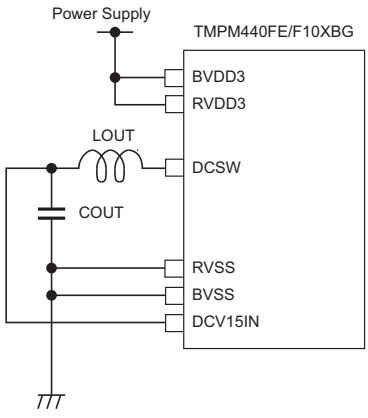


Figure 1-3 Capacitors connection diagram for regulators

1.7.2 A List of Pin Numbers and Functional Pin Names

1.7.2.1 Conventions Used in the Table

Various conventional symbols are used in the following tables:

1. Function A

   Dual functions in which the pins are assigned to ports without the function register settings are described.

2. Function B

   Dual functions in which the pins are assigned to ports by the register settings are described. Numbers described in the "Function B" Column correspond to the numbers of function registers.

3. Pin specifications

   The following symbols mean as follows:

- SMT/CMOS: Input gate

  SMT: Schmitt trigger input

  CMOS: CMOS input

- 5V_T: 5V tolerant

  Yes: Support

  N/A: Not available

- OD: Programmable open-drain output

  Yes: Support

  N/A: Not available

- PU/PD: Programmable pull-up/pull-down

  PU: Programmable pull-up is selectable.

  PD: Programmable pull-down is selectable.

1.7.2.2 Port/Shared Pins

Table 1-11 Pin numbers and pin names <PORT order> (1/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
PORT A											
W17	PA0		D0/AD0		PSCPTIO0			PU	N/A	N/A	CMOS
Y18	PA1		D1/AD1		PSCPTIO1			PU	N/A	N/A	CMOS
V18	PA2		D2/AD2		PSCPTIO2			PU	N/A	N/A	CMOS
U18	PA3		D3/AD3		PSCPTIO3			PU	N/A	N/A	CMOS
W19	PA4		D4/AD4		PSCPTIO4			PU	N/A	N/A	CMOS
Y19	PA5		D5/AD5		PSCPTIO5			PU	N/A	N/A	CMOS
W20	PA6		D6/AD6		PSCPTIO6			PU	N/A	N/A	CMOS
W18	PA7		D7/AD7		PSCPTIO7			PU	N/A	N/A	CMOS
PORT B											
V14	PB0		D8/AD8		TB12IN0			PU	N/A	N/A	CMOS
W14	PB1		D9/AD9		TB12IN1			PU	N/A	N/A	CMOS
P13	PB2		D10/AD10		TB13IN0			PU	N/A	N/A	CMOS
R14	PB3		D11/AD11		TB13IN1			PU	N/A	N/A	CMOS
Y15	PB4		D12/AD12		TB14IN0			PU	N/A	N/A	CMOS
V15	PB5		D13/AD13		TB14IN1			PU	N/A	N/A	CMOS
W15	PB6		D14/AD14		TB15IN0			PU	N/A	N/A	CMOS
P14	PB7		D15/AD15		TB15IN1			PU	N/A	N/A	CMOS
PORT C											
V12	PC0		A0	A16	INT5			PU	N/A	N/A	SMT
W12	PC1		A1	A17	INT6			PU	N/A	N/A	SMT
R12	PC2		A2	A18	INT7			PU	N/A	N/A	SMT
Y13	PC3		A3	A19	INT8			PU	N/A	N/A	SMT
V13	PC4		A4	A20	INT9			PU	N/A	N/A	SMT
W13	PC5		A5	A21	INTA			PU	N/A	N/A	SMT
R13	PC6		A6	A22	INTB			PU	N/A	N/A	SMT
Y14	PC7		A7	A23	INTC			PU	N/A	N/A	SMT
PORT D											
R18	PD0		A8	TB16IN0				PU	N/A	N/A	SMT
N15	PD1		A9	TB16IN1				PU	N/A	N/A	SMT
T19	PD2		A10	TB17IN0				PU	N/A	N/A	SMT

Table 1-11 Pin numbers and pin names <PORT order> (2/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
U20	PD3		A11	TB17IN1				PU	N/A	N/A	SMT
T18	PD4		A12	TB18IN0				PU	N/A	N/A	SMT
U19	PD5		A13	TB18IN1				PU	N/A	N/A	SMT
V20	PD6		A14	TB19IN0				PU	N/A	N/A	SMT
V19	PD7		A15	TB19IN1				PU	N/A	N/A	SMT
PORT E											
L14	PE0		A16	TXD2				PU	Yes	N/A	SMT
P19	PE1		A17	RXD2				PU	Yes	N/A	SMT
M15	PE2		A18	SCLK2	$\overline{\text{CTS2}}$			PU	Yes	N/A	SMT
R20	PE3	INT16	A19	$\overline{\text{DREQB}}$				PU	N/A	N/A	SMT
P18	PE4		A20	TXD5				PU	Yes	N/A	SMT
M14	PE5		A21	RXD5				PU	Yes	N/A	SMT
R19	PE6		A22	SCLK5	$\overline{\text{CTS5}}$			PU	Yes	N/A	SMT
T20	PE7	INT17	A23	$\overline{\text{DREQC}}$				PU	N/A	N/A	SMT
PORT F											
N14	PF0		$\overline{\text{RD}}$					PU	N/A	N/A	SMT
Y16	PF1		$\overline{\text{WR}}$					PU	N/A	N/A	SMT
V16	PF2		$\overline{\text{BELL}}$					PU	N/A	N/A	SMT
R15	PF3		$\overline{\text{BELH}}$					PU	N/A	N/A	SMT
P15	PF4		ALE					PU	N/A	N/A	SMT
W16	PF5		$\overline{\text{CS0}}$					PU	N/A	N/A	SMT
Y17	PF6		$\overline{\text{CS1}}$	$\overline{\text{DREQA}}$	INTD			PU	N/A	N/A	SMT
V17	PF7	$\overline{\text{BOOT}}$						PU	N/A	N/A	SMT
PORT G											
A20	PG0		TDO/SWV					PU	N/A	N/A	SMT
C18	PG1		TMS/ SWDIO					PU	N/A	N/A	SMT
D18	PG2		TCK/ SWCLK					PD	N/A	N/A	SMT
D19	PG3		TDI					PU	N/A	N/A	SMT
E18	PG4		$\overline{\text{TRST}}$					PU	N/A	N/A	SMT
F15	PG5		TRACE CLK					PU	N/A	N/A	SMT
E19	PG6		TRACE DATA0					PU	N/A	N/A	SMT
F18	PG7		TRACE DATA1					PU	N/A	N/A	SMT

Table 1-11 Pin numbers and pin names <PORT order> (3/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
PORT H											
G15	PH0		TRACE DATA2					PU	N/A	N/A	SMT
F19	PH1		TRACE DATA3					PU	N/A	N/A	SMT
H14	PH2		$\overline{\text{ADTRGA}}$					PU	N/A	N/A	SMT
G18	PH3		$\overline{\text{ADTRGB}}$	$\overline{\text{ADTRGSNC}}$				PU	N/A	Yes	SMT
E20	PH4		TXD0					PU	Yes	N/A	SMT
F20	PH5		RXD0					PU	Yes	N/A	SMT
G20	PH6		SCLK0	$\overline{\text{CTS0}}$				PU	Yes	N/A	SMT
G19	PH7		$\overline{\text{ADTRGC}}$					PU	N/A	Yes	SMT
PORT J											
A8	PJ0		ESIO0 TXD0					PU	N/A	N/A	SMT
A9	PJ1		ESIO0 TXD1					PU	N/A	N/A	SMT
A10	PJ2		ESIO0 TXD2					PU	N/A	N/A	SMT
A11	PJ3		ESIO0 TXD3					PU	N/A	N/A	SMT
B8	PJ4		ESIO0 RXD0					PU	N/A	N/A	CMOS
B9	PJ5		ESIO0 RXD1					PU	N/A	N/A	CMOS
B10	PJ6		ESIO0 RXD2					PU	N/A	N/A	CMOS
B11	PJ7		ESIO0 RXD3					PU	N/A	N/A	CMOS
PORT K											
A12	PK0		ESIO0SCK					PU	N/A	N/A	SMT
B12	PK1		ESIO0CS0					PU	N/A	N/A	SMT
C12	PK2		ESIO0CS1	TB07IN0				PU	N/A	N/A	SMT
G13	PK3			TB07IN1	INTE			PU	N/A	N/A	SMT
A14	PK4		TXD1					PU	Yes	Yes	SMT
A13	PK5		RXD1					PU	Yes	Yes	SMT
A15	PK6		SCLK1	TB08IN0	$\overline{\text{CTS1}}$			PU	Yes	Yes	SMT
F14	PK7			TB08IN1	INTF			PU	Yes	Yes	SMT
PORTL											

Table 1-11 Pin numbers and pin names <PORT order> (4/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
A16	PL0		ESIO1 TXD0					PU	N/A	N/A	SMT
A17	PL1		ESIO1 TXD1					PU	N/A	N/A	SMT
A18	PL2		ESIO1 TXD2					PU	N/A	N/A	SMT
A19	PL3		ESIO1 TXD3					PU	N/A	N/A	SMT
B16	PL4		ESIO1 RXD0					PU	N/A	N/A	CMOS
B17	PL5		ESIO1 RXD1					PU	N/A	N/A	CMOS
B18	PL6		ESIO1 RXD2					PU	N/A	N/A	CMOS
B19	PL7		ESIO1 RXD3					PU	N/A	N/A	CMOS
PORT M											
C17	PM0		ESIO1SCK					PU	N/A	N/A	SMT
C16	PM1		ESIO1CS0					PU	N/A	N/A	SMT
C15	PM2		ESIO1CS1	TB09IN0				PU	N/A	N/A	SMT
G14	PM3		SCOUT	TB09IN1	INT10			PU	N/A	N/A	SMT
C20	PM4		TXD3					PU	Yes	Yes	SMT
D20	PM5		RXD3					PU	Yes	Yes	SMT
B20	PM6		SCLK3	TB10IN0	$\overline{\text{CTS3}}$			PU	Yes	Yes	SMT
C19	PM7			TB10IN1	INT11			PU	Yes	Yes	SMT
PORT N											
V9	PN0		ESIO2 TXD0					PU	N/A	N/A	SMT
R8	PN1		ESIO2 TXD1					PU	N/A	N/A	SMT
N7	PN2		ESIO2 TXD2		INT12			PU	N/A	N/A	SMT
R9	PN3		ESIO2 TXD3		INT13			PU	N/A	N/A	SMT
Y10	PN4		ESIO2 RXD0					PU	N/A	N/A	CMOS
M7	PN5		ESIO2 RXD1					PU	N/A	N/A	CMOS
P8	PN6		ESIO2 RXD2					PU	N/A	N/A	CMOS
R10	PN7		ESIO2 RXD3					PU	N/A	N/A	CMOS

Table 1-11 Pin numbers and pin names <PORT order> (5/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
PORT P											
W10	PP0		ESIO2SCK					PU	N/A	N/A	SMT
W9	PP1		ESIO2CS0					PU	N/A	N/A	SMT
V10	PP2		ESIO2CS1	TXD7	INT14			PU	N/A	N/A	SMT
V11	PP3			RXD7	INT15			PU	N/A	N/A	SMT
W11	PP4		TXD4					PU	N/A	N/A	SMT
Y11	PP5		RXD4					PU	N/A	N/A	SMT
Y12	PP6		SCLK4	$\overline{\text{CTS7}}$	$\overline{\text{CTS4}}$			PU	N/A	N/A	SMT
R11	PP7			$\overline{\text{RTS7}}$	INT0			PU	N/A	N/A	SMT
PORT R											
H18	PR0		TXD6					PU	Yes	Yes	SMT
H20	PR1		RXD6					PU	Yes	Yes	SMT
H19	PR2		$\overline{\text{CTS6}}$	TB11IN0	INT1			PU	Yes	Yes	SMT
H15	PR3		$\overline{\text{RTS6}}$	TB11IN1	INT2			PU	Yes	Yes	SMT
J19	PR4		SCL0					PU	Yes	N/A	SMT
J18	PR5		SDA0					PU	Yes	N/A	SMT
K20	PR6	EPHC0IN0			INT3			PU	N/A	N/A	SMT
K19	PR7	EPHC0IN1			INT4			PU	N/A	N/A	SMT
PORT T											
M19	PT0		TCOUT0					PU	N/A	N/A	SMT
M18	PT1		TCOUT1					PU	N/A	N/A	SMT
N20	PT2		TCOUT2					PU	N/A	N/A	SMT
K14	PT3		TCOUT3					PU	N/A	N/A	SMT
N19	PT4		TCOUT4					PU	N/A	N/A	SMT
L15	PT5		TCOUT5					PU	N/A	N/A	SMT
N18	PT6		TCOUT6					PU	N/A	N/A	SMT
P20	PT7		TCOUT7					PU	N/A	N/A	SMT
PORT U											
N6	PU0		TCIN0					PU	N/A	N/A	SMT
L2	PU1		TCIN1					PU	N/A	N/A	SMT
L3	PU2		TCIN2					PU	N/A	N/A	SMT
M6	PU3		TCIN3					PU	N/A	N/A	SMT
L1	PU4		PHC0IN0					PU	N/A	N/A	SMT
M2	PU5		PHC0IN1					PU	N/A	N/A	SMT

Table 1-11 Pin numbers and pin names <PORT order> (6/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
M1	PU6		PHC1IN0					PU	N/A	N/A	SMT
N1	PU7		PHC1IN1					PU	N/A	N/A	SMT
PORT V											
F12	PV0		TB00OUT					PU	N/A	N/A	SMT
F8	PV1		TB01OUT					PU	N/A	N/A	SMT
B13	PV2		TB02OUT					PU	N/A	N/A	SMT
G8	PV3		TB03OUT					PU	N/A	N/A	SMT
C9	PV4		TB04OUT					PU	N/A	N/A	SMT
F9	PV5		TB05OUT					PU	N/A	N/A	SMT
G12	PV6		TB06OUT					PU	N/A	N/A	SMT
C13	PV7		TB07OUT					PU	N/A	N/A	SMT
PORT W											
B14	PW0		TB08OUT					PU	Yes	N/A	SMT
C10	PW1		TB09OUT					PU	Yes	N/A	SMT
F13	PW2		TB10OUT					PU	Yes	N/A	SMT
F10	PW3		TB11OUT					PU	Yes	N/A	SMT
B15	PW4		TB12OUT					PU	Yes	N/A	SMT
C11	PW5		TB13OUT					PU	Yes	N/A	SMT
C14	PW6		TB14OUT					PU	Yes	N/A	SMT
F11	PW7		TB15OUT					PU	Yes	N/A	SMT
PORT Y											
K18	PY0		TB16OUT					PU	N/A	N/A	SMT
J15	PY1		TB17OUT					PU	N/A	N/A	SMT
L20	PY2		TB18OUT					PU	N/A	N/A	SMT
J14	PY3		TB19OUT					PU	N/A	N/A	SMT
L19	PY4		TD0OUT0					PU	N/A	N/A	SMT
L18	PY5		TD0OUT1					PU	N/A	N/A	SMT
K15	PY6		TD1OUT0					PU	N/A	N/A	SMT
M20	PY7		TD1OUT1					PU	N/A	N/A	SMT
PORT AA											
C3	PAA0	AINA0						PU	N/A	N/A	SMT
D3	PAA1	AINA1						PU	N/A	N/A	SMT
E3	PAA2	AINA2						PU	N/A	N/A	SMT
F6	PAA3	AINA3						PU	N/A	N/A	SMT

Table 1-11 Pin numbers and pin names <PORT order> (7/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
F3	PAA4	AINA4						PU	N/A	N/A	SMT
G3	PAA5	AINA5						PU	N/A	N/A	SMT
G6	PAA6	AINA6						PU	N/A	N/A	SMT
H7	PAA7	AINA7						PU	N/A	N/A	SMT
PORT AB											
H6	PAB0	AINB0						PU	N/A	N/A	SMT
J7	PAB1	AINB1						PU	N/A	N/A	SMT
H3	PAB2	AINB2						PU	N/A	N/A	SMT
J6	PAB3	AINB3						PU	N/A	N/A	SMT
K7	PAB4	AINB4						PU	N/A	N/A	SMT
K6	PAB5	AINB5						PU	N/A	N/A	SMT
L7	PAB6	AINB6						PU	N/A	N/A	SMT
J3	PAB7	AINB7						PU	N/A	N/A	SMT
PORT AC											
B2	PAC0	AINC0						PU	N/A	N/A	SMT
A2	PAC1	AINC1						PU	N/A	N/A	SMT
B1	PAC2	AINC2						PU	N/A	N/A	SMT
B3	PAC3	AINC3						PU	N/A	N/A	SMT
PORT AD											
A7	PAD0		KWUPA00					PU	N/A	N/A	SMT
C8	PAD1		KWUPA01					PU	N/A	N/A	SMT
B7	PAD2		KWUPA02					PU	N/A	N/A	SMT
A6	PAD3		KWUPA03					PU	N/A	N/A	SMT
G7	PAD4		KWUPA04					PU	N/A	N/A	SMT
C7	PAD5		KWUPA05					PU	N/A	N/A	SMT
B6	PAD6		KWUPA06					PU	N/A	N/A	SMT
A5	PAD7		KWUPA07					PU	N/A	N/A	SMT
PORT AE											
F7	PAE0		KWUPA08					PU	N/A	N/A	SMT
B5	PAE1		KWUPA09					PU	N/A	N/A	SMT
C6	PAE2		KWUPA10					PU	N/A	N/A	SMT
A4	PAE3		KWUPA11					PU	N/A	N/A	SMT
B4	PAE4		KWUPA12					PU	N/A	N/A	SMT
C5	PAE5		KWUPA13					PU	N/A	N/A	SMT

Table 1-11 Pin numbers and pin names <PORT order> (8/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
A3	PAE6		KWUPA14					PU	N/A	N/A	SMT
C4	PAE7		KWUPA15					PU	N/A	N/A	SMT
PORT AF											
N3	PAF0		KWUPA16					PU	N/A	N/A	SMT
P1	PAF1		KWUPA17					PU	N/A	N/A	SMT
M3	PAF2		KWUPA18					PU	N/A	N/A	SMT
P3	PAF3		KWUPA19					PU	N/A	N/A	SMT
P2	PAF4		KWUPA20					PU	N/A	N/A	SMT
N2	PAF5		KWUPA21					PU	N/A	N/A	SMT
R3	PAF6		KWUPA22					PU	N/A	N/A	SMT
T2	PAF7		KWUPA23					PU	N/A	N/A	SMT
PORT AG											
V3	PAG0		KWUPA24					PU	N/A	N/A	SMT
W2	PAG1		KWUPA25					PU	N/A	N/A	SMT
W3	PAG2		KWUPA26					PU	N/A	N/A	SMT
W1	PAG3		KWUPA27					PU	N/A	N/A	SMT
U3	PAG4		KWUPA28					PU	N/A	N/A	SMT
V2	PAG5		KWUPA29					PU	N/A	N/A	SMT
W4	PAG6		KWUPA30					PU	N/A	N/A	SMT
T3	PAG7		KWUPA31	TCTBTIN				PU	N/A	N/A	SMT
PORT AH											
V7	PAH0	KSIN0 KWUPB0						PU	N/A	N/A	SMT
P6	PAH1	KSIN1 KWUPB1						PU	N/A	N/A	SMT
Y8	PAH2	KSIN2 KWUPB2						PU	N/A	N/A	SMT
V8	PAH3	KSIN3 KWUPB3						PU	N/A	N/A	SMT
R7	PAH4	KSIN4 KWUPB4						PU	N/A	N/A	SMT
W8	PAH5	KSIN5 KWUPB5						PU	N/A	N/A	SMT
Y9	PAH6	KSIN6 KWUPB6						PU	N/A	N/A	SMT
P7	PAH7	KSIN7 KWUPB7						PU	N/A	N/A	SMT
PORT AJ											

Table 1-11 Pin numbers and pin names <PORT order> (9/9)

Pin No.	PORT	Function A	Function B					Port specification			
VFBGA 289			1	2	3	4	5	PU/ PD	OD	5V_T	SMT/ CMOS
V4	PAJ0		KSOUT0					PU	Yes	N/A	SMT
R6	PAJ1		KSOUT1					PU	Yes	N/A	SMT
W5	PAJ2		KSOUT2					PU	Yes	N/A	SMT
V5	PAJ3		KSOUT3					PU	Yes	N/A	SMT
W6	PAJ4		KSOUT4					PU	Yes	N/A	SMT
V6	PAJ5		KSOUT5					PU	Yes	N/A	SMT
Y7	PAJ6		KSOUT6					PU	Yes	N/A	SMT
W7	PAJ7		KSOUT7					PU	Yes	N/A	SMT

1.7.2.3 Dedicated Pins

(1) Analog Pins

Table 1-12 Pin numbers and Pin names

Pin No. VFBG289	Analog Pin names
K3	DAOUT0
L6	DAOUT1

(2) Debug Pin

Table 1-13 Pin numbers and Pin names

Pin No. VFBGA289	Debug Pin nams
A1	BSC

(3) Control Pins

Table 1-14 Pin numbers and Pin names

Pin No. VFBGA289	Control Pin names
Y1	MODE
Y4	$\overline{\text{RESET}}$
J20	ENDIAN

(4) Clock Pins

Table 1-15 Pin numbers and Pin names

Pin No. VFBGA289	Clock Pin names
Y5	X1/EHCLKIN
Y6	X2
Y3	XT1
Y2	XT2

(5) Test Pin

Table 1-16 Pin numbers and Pin names

Pin No. VFBGA289	Test Pin names
Y20	FTEST3

1.7.2.4 Power Supply Pins

Table 1-17 Pin numbers and pin names

Pin No. VFBGA 289	Power supply pin names
R1	RVDD3
U1	RVSS
L8, M8, N8, N9, P9, N10, P10, N11, P11, N12, P12, N13, M13, L13	DVDD3
H8, J8, K8, G9, H9, J9, G10, H10, G11, H11, H12, H13, J13, K13	DVSS
R2	BVDD3
U2	BVSS
E1	ADAVDD3
G1	ADBVDD3
C1	ADCVDD3
E2	ADAVSS
G2	ADBVSS
C2	ADCVSS
F1	ADAVREFH
H1	ADBVREFH
D1	ADCVREFH
F2	ADAVREFL
H2	ADBVREFL
D2	ADCVREFL
K1	DAVDD3
J2	DAVSS
K2	DAVREFH
J1	DAVREFL
T1	DCSW
V1	DCV15IN

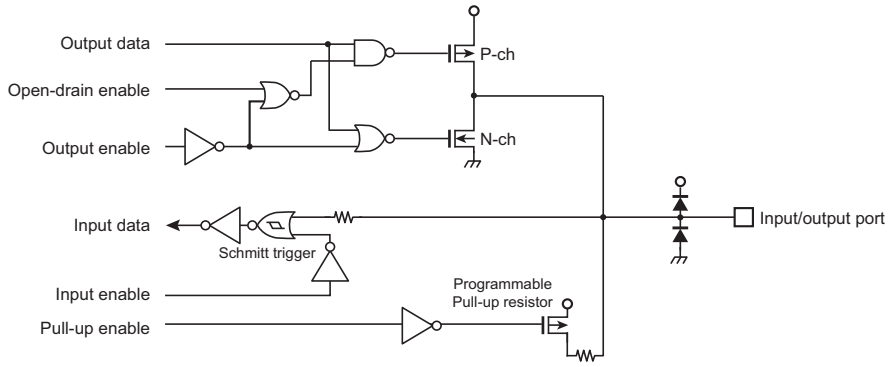
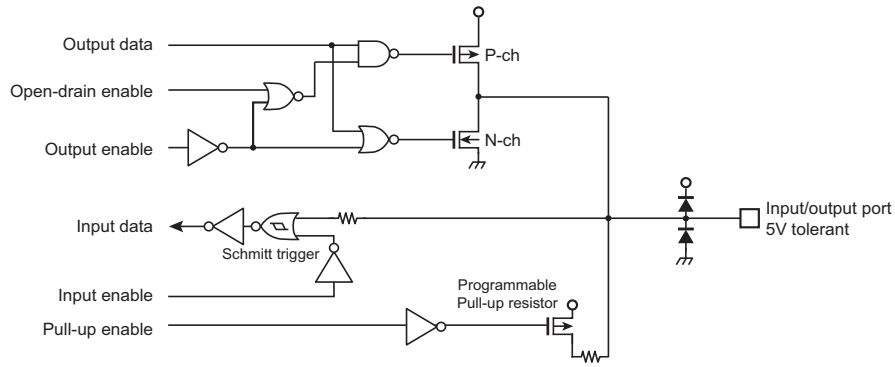
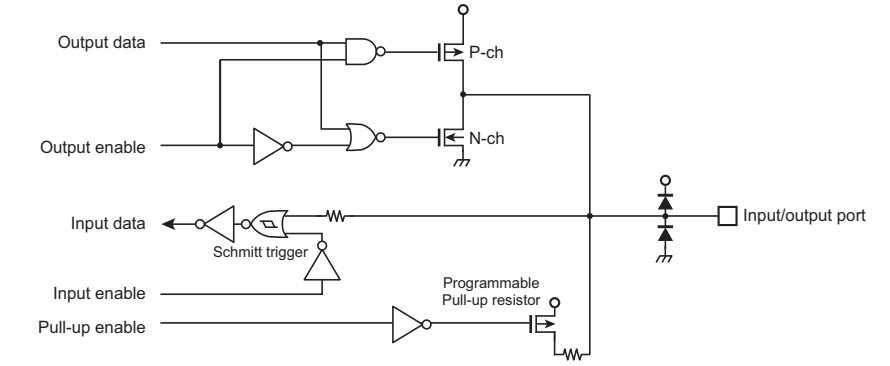
1.8 Port Equivalent Circuit Schematic

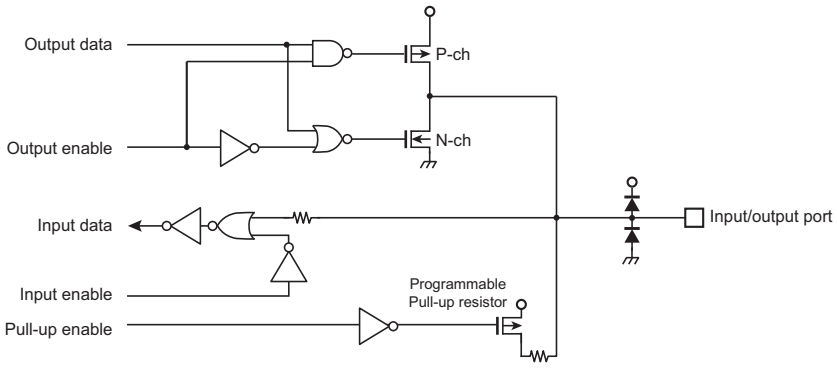
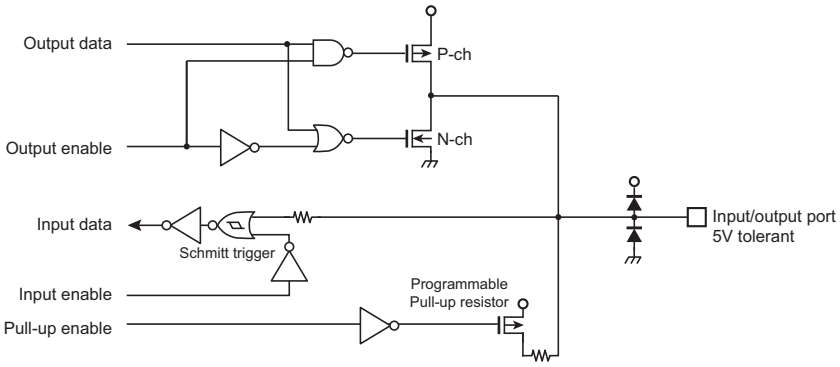
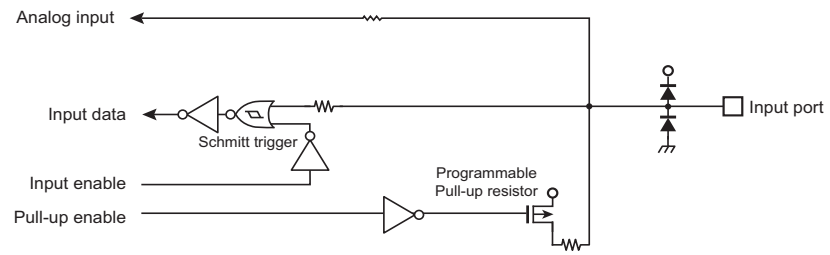
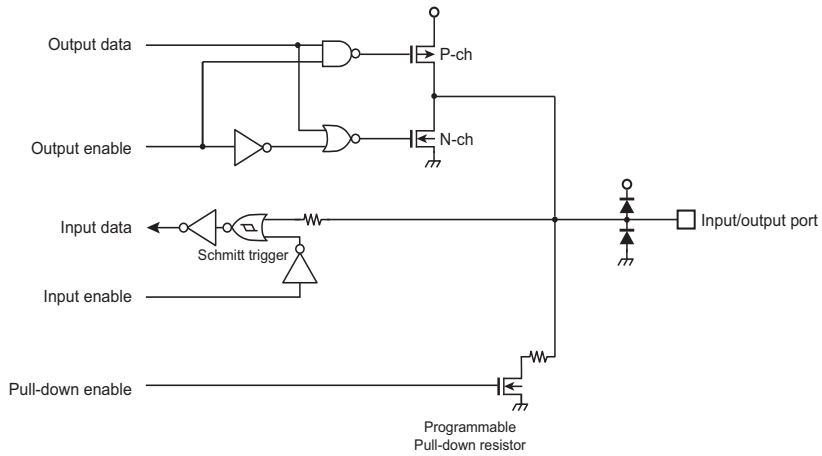
The port equivalent circuit schematic is basically drawn by using the same gate symbols as those of Standard CMOS logic 74HCxx series.

The input protection resistance ranges from several tens of Ω to several hundreds Ω. The X2 and XT2 damping resistance values shown in the following figures are typical values.

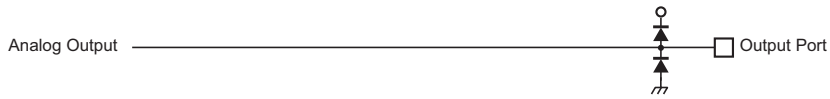
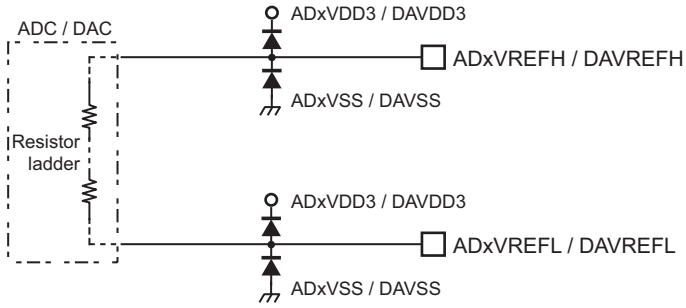
Note: Resistors without values in the following figures indicate input protection resistors.

1.8.1 Ports

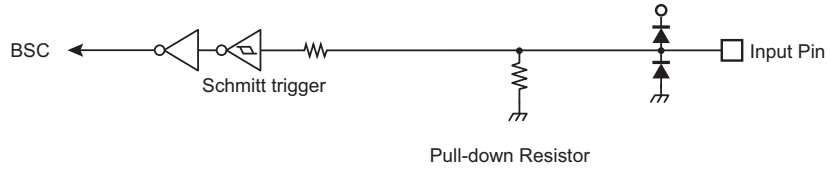
PE0 to 2, PE4 to 6, PH4 to 6, PR4 to 5, PW0 to 7, PAJ0 to 7	
PK4 to 7, PM4 to 7, PR0 to 3	
PC0 to 7, PD0 to 7, PE3, PE7, PF0 to 7, PG0 to 1 PG3 to 7, PH0 to 2 PJ0 to 3, PK0 to 3, PL0 to 3, PM0 to 3, PN0 to 3, PP0 to 7, PR6 to 7,PT0 to 7, PU0 to 7, PV0 to 7, PY0 to 7, PAD0 to 7, PAE0 to 7, PAF0 to 7, PAG0 to 7, PAH0 to 7	

PA0 to 7, PB0 to 7, PJ4 to 7, PL4 to 7, PN4 to 7	
PH3, PH7	
PAA0 to 7, PAB0 to 7, PAC0 to 3	
PG2	

1.8.2 Analog Power Supply Pins

DAOUT0 DAOUT1	
ADAVREFH, ADAVREFL ADBVREFH, ADBVREFL ADCVREFH, ADCVREFL DAVREFH, DAVREFL	

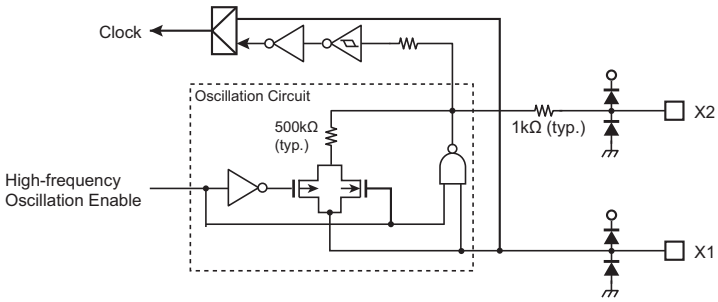
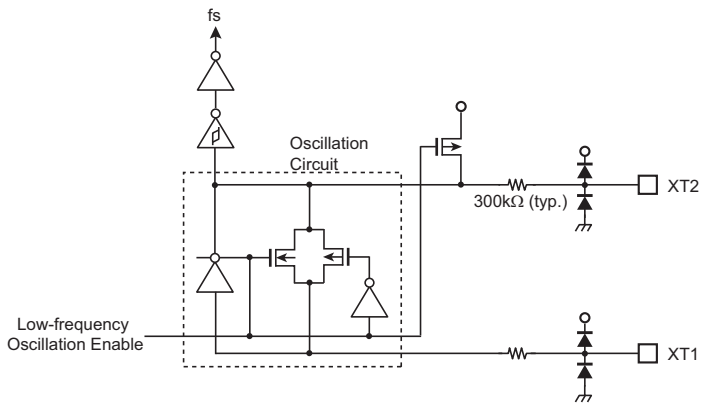
1.8.3 Debug Pins

BSC	

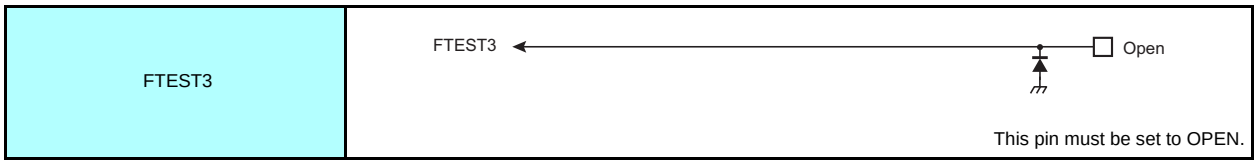
1.8.4 Control Pins

MODE	 This pin must be connected to GND.
ENDIAN	
$\overline{\text{RESET}}$	

1.8.5 Clock Pins

X1, X2	
XT1, XT2	

1.8.6 Test Pin



1.9 Revision History

Revision	Date	Comment
rev1.0	2014/1/21	First Release
rev1.1	2014/1/23	Contents Revised

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