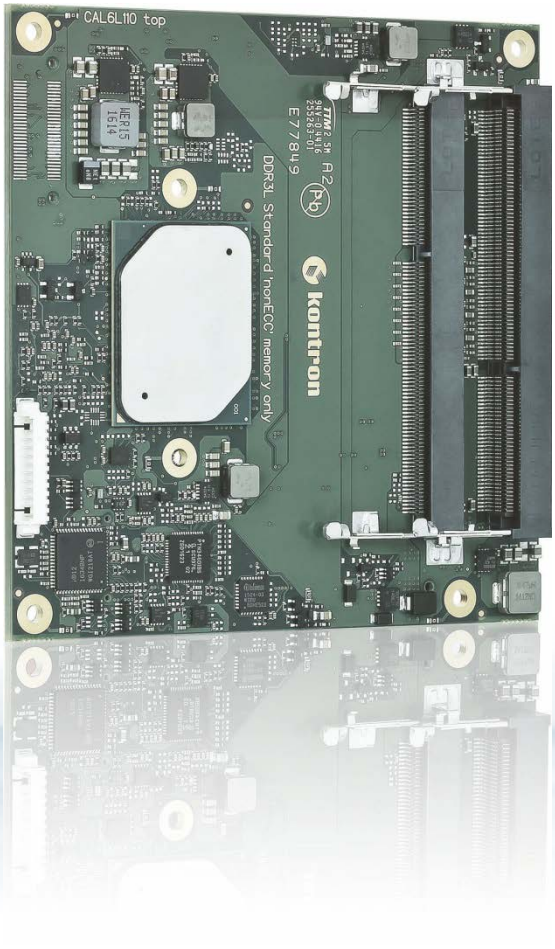
USER GUIDE



COMe-cAL6

Doc. User Guide Rev.1.9

Doc. ID: 1061-1953

POSSIBILITIES START HERE kontron S&T Group

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COME-CAL6 - USER GUIDE

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NOTICE

You find the most recent version of the “General Safety Instructions“ online in the download area of this product.

NOTICE

This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Kontron Support.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author/ Editor
1.0	Initial version	2017-Oct-17	CW
1.1	Included metal heat slug dimensions and information in Ch.2.5.1 and 2.8.3	2018-May-24	CW
1.2	Updates pSLC information in Chapters 2.3.13 and 3.1	2019-Apr-01	CW
1.3	Included the MTBF graphs	2020-Jan-08	CW
1.4	Extended Specification of COMe-cAL6 Processor Variants Table 8	2020-May-14	CW
1.5	Updated Accessories List	2020-Jul-23	CW
1.6	Ethernet controller i211AT replaced by i210AT	2022-Apr-22	CW
1.7	GPIO Updates	2022-Jul-29	CW
1.8	Figure 7, D1 and A1 pinning changed	2022-Aug-12	CW
1.9	Changed to Chapter 5 and Figure 7	2022-Aug-18	CW

Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit http://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Find Kontron contacts by visiting Kontron Support: https://www.kontron.com/en/support-and-services.

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/en/support-and-services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron Support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

⚠CAUTION

Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Follow the "General Safety Instructions for IT Equipment" supplied with the system.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See, Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

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1/ Introduction

1.1. Product Description

The COMe-cAL6 is a compact form factor, COM Express® type 6 Computer-on-Module based on Intel® Apollo Lake® series of processors Atom™, Pentium® and Celeron®, with an integrated chipset. The COMe-cAL6 combines increased efficiency and performance with TDP as low as 6 W, and no more than 12 W with Intel's® extensive HD Graphics capabilities.

The main COMe-cAL6 features are:

- Intel® Apollo Lake® series of processors with integrated chipset
- Up to 8 GByte DDR3L 1600/1866 (non-ECC) with 2x SO-DIMM sockets
- High-speed connectivity includes: up to 5x PCIe x1, 4x USB 3.0 (including USB 2.0) + 4x USB 2.0, and 2x SATA Gen 3 (6 Gb/s)
- Support for both commercial and Industrial temperature grade environments

1.2. Product Naming Clarification

COM Express® defines a Computer-on-Module, or COM, with all the components necessary for a bootable host computer, packaged as a super component. The product names for Kontron COM Express® Computer-on-Modules consist of:

- Short form of the industry standard
  - COMe-
- Module form factor
  - b=basic (125mm x 95mm)
  - c=compact (95mm x 95mm)
  - m=mini (84mm x 55mm)
- Intel's processor code name
  - AL = Apollo Lake
- Pinout type
  - Type 6
  - Type 7
  - Type10
- Available temperature variants
  - Commercial
  - Extended (E1)
  - Industrial (E2)
  - Screened industrial (E2S) and Rapid shutdown screened industrial (R E2S)
- Processor Identifier
  - Chipset identifier (if chipset assembled)
- Memory size
  - Memory down + DIMM memory (#GB) / eMMC pSLC memory (#S)

1.3. COM Express® Documentation

The COM Express® Specification defines the COM Express® module form factor, pinout and signals. The COM Express document is available at the PICMG® website.

1.4. Com Express® Functionality

All Kontron COM Express® basic and compact modules contain two 220-pin connectors; each of it has two rows called Row A & B on primary connector and Row C & D on secondary connector. COM Express® Computer-on-Modules feature the following maximum amount of interfaces according to the PICMG module pinout type.

Table 1: Type 6 and COMe-cAL6 Functionality

Feature	Type 6 Pinout	COMe-cAL6 Pinout
HD Audio	1x	1x
Gbit Ethernet	1x	1x
Serial ATA	4x	2x
PCI Express x 1	8x	5x
PCI Express x16 (PEG)	1x	Not supported
USB Client	1x	1x (USB Port 0 is dual role Client/Host)
USB	4x USB 3.0 (Including USB 2.0) 4x USB 2.0	4x USB 3.0 (Including USB 2.0) 4x USB 2.0
VGA	1x	Not supported
LVDS	Dual Channel	Dual Channel LVDS with optional embedded display port (eDP) overlay
DP++ (eDP/DP/HDMI/DVI/VGA)	3x	2x
LPC	1x	1x
External SMB	1x	1x
External I2C	1x	1x
GPIO	8x	8x (4x GPI, 4x GPO)
SDIO shared w/GPIO	1x optional	Not supported
UART (2-wire COM)	2x	2x
FAN PWM out	1x	1x
Express Card	2x	2x

1.5. COM Express® Benefits

COM Express® defines a Computer-on-Module, or COM, with all the components necessary for a bootable host computer, packaged as highly integrated computer. All Kontron COM Express® modules are very compact and feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM is based on the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application, on a baseboard optimally designed to fit a system's packaging.

A single baseboard design can use a range of COM Express® modules with different sizes and pinouts. This flexibility differentiates products at various price and performance points and provides a built-in upgrade path when designing future-proof systems. The modularity of a COM Express® solution also ensures against obsolescence when computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

2/ Product Specification

2.1. Module Variants

The COMe-cAL6 is available in different processor and chipset variants to cover demands in performance, price and power.

2.1.1. Commercial Temperature Grade Modules 0°C to +60°C

Table 2: Product Number for Commercial Grade Modules (0°C to +60°C operating)

Product Number	Product Name	Description
36023-0000-11-4	COMe-cAL6 N4200	COM Express® compact pin-out type 6 Computer-on-Module with Intel® Pentium® N4200, commercial grade
36023-0000-11-2	COMe-cAL6 N3350	COM Express® compact pin-out type 6 Computer-on-Module with Intel® Celeron® N3350,commercial grade

2.1.2. Industrial Temperature Grade Modules E2-40°C to +85°C

Table 3: Product number for Industrial Grade Modules E2 (-40°C to +85°C operating)

Product Number	Product Name	Description
36024-0032-16-7	COMe-cAL6 E2 E3950 32S PCIe	COM Express® compact pin-out type 6 Computer-on-Module with Intel® Atom™ x7 E3950, 32 GB pSLC eMMC, PCIe Hub, industrial temperature
36024-0000-16-7	COMe-cAL6 E2 E3950	COM Express® compact pin-out type 6 Computer-on-Module with Intel® Atom™ x7 E3950, industrial temperature
36024-0000-16-5	COMe-cAL6 E2 E3940	COM Express® compact pin-out type 6 Computer-on-Module with Intel® Atom™ x5 E3940, industrial temperature
36024-0000-13-5	COMe-cAL6 E2 E3930	COM Express® compact pin-out type 6 Computer-on-Module with Intel® Atom™ x5 E3930, industrial temperature

2.2. Accessories

Accessories are either COMe-cAL6 product specific, COMe type 6 specific, or general accessories including memory modules. For more information, contact your local Kontron sales representative or Kontron Inside Sales.

Table 4: Product Specific Accessories

Part Number	Heatspreader (validated ref. types)	Description
36024-0000-99-0	HSP COMe-cAL6 E2 thread	Heatspreader for COMe-cAL6 E2, threaded mounting holes
36024-0000-99-1	HSP COMe-cAL6 E2 through	Heatspreader for COMe-cAL6 E2, through holes

Table 5: COMe Type 6 Accessories

Part Number	COMe Carrier	Project Code	Description
38115-0000-00-x	COM Express® Ref. Carrier-i Type 6	ADTI	Thin-mITX carrier with 5 mm COMe connector
38116-0000-00-5	COM Express® Eval. Carrier2 Type 6	ADT6	ATX carrier with 5 mm COMe connector
Part Number	**COMe Adapter / Card**	**Project Code**	**Description**
96007-0000-00-3	ADA-PCIe-DP	APDP	PCIe x16 to DP Adapter for Evaluation carrier
96007-0000-00-7	ADA-Type6-DP3	DVO6	(Sandwich) Adapter Card for 3x Display Port
96006-0000-00-2	COMe POST T6	NFCB	POST Code / Debug Card
38019-0000-00-0	ADA-COMe-Height-dual	EERC	Height Adapter

Table 6: General COMe Accessories

Part Number	Cooling Solutions	Description
36099-0000-99-0	COMe Active Uni cooler	For CPUs up to 20 W TDP, to be mounted on HSP
36099-0000-99-1	COMe Passive Uni Cooler	For CPUs up to 10 W TDP, to be mounted on HSP
Part Number	**Mounting**	**Description**
38017-0000-00-5	COMe Mount KIT 5 mm 1 set	Mounting Kit for 1 module including screws for 5 mm connectors
38017-0100-00-5	COMe Mount KIT 5 mm 100 sets	Mounting Kit for 100 modules including screws for 5 mm connectors
38017-0000-00-0	COMe Mount KIT 8 mm 1 set	Mounting Kit for 1 module including screws for 8 mm connectors
38017-0100-00-0	COMe Mount KIT 8 mm 100 sets	Mounting Kit for 100 modules including screws for 8 mm connectors
Part Number	**Display Adapters**	**Description**
96006-0000-00-8	ADA-DP-LVDS	DP to LVDS adapter
96082-0000-00-0	KAB-ADAPT-DP-DVI	DP to DVI adapter cable
96083-0000-00-0	KAB-ADAPT-DP-VGA	DP to VGA adapter cable
96084-0000-00-0	KAB-ADAPT-DP-HDMI	DP to HDMI adapter cable
Part Number	**Cables**	**Description**
96079-0000-00-0	KAB-HSP 200 mm	Cable adapter FAN to module (COMe basic/compact)
96079-0000-00-2	KAB-HSP 40 mm	Cable adapter FAN to module (COMe basic/compact)

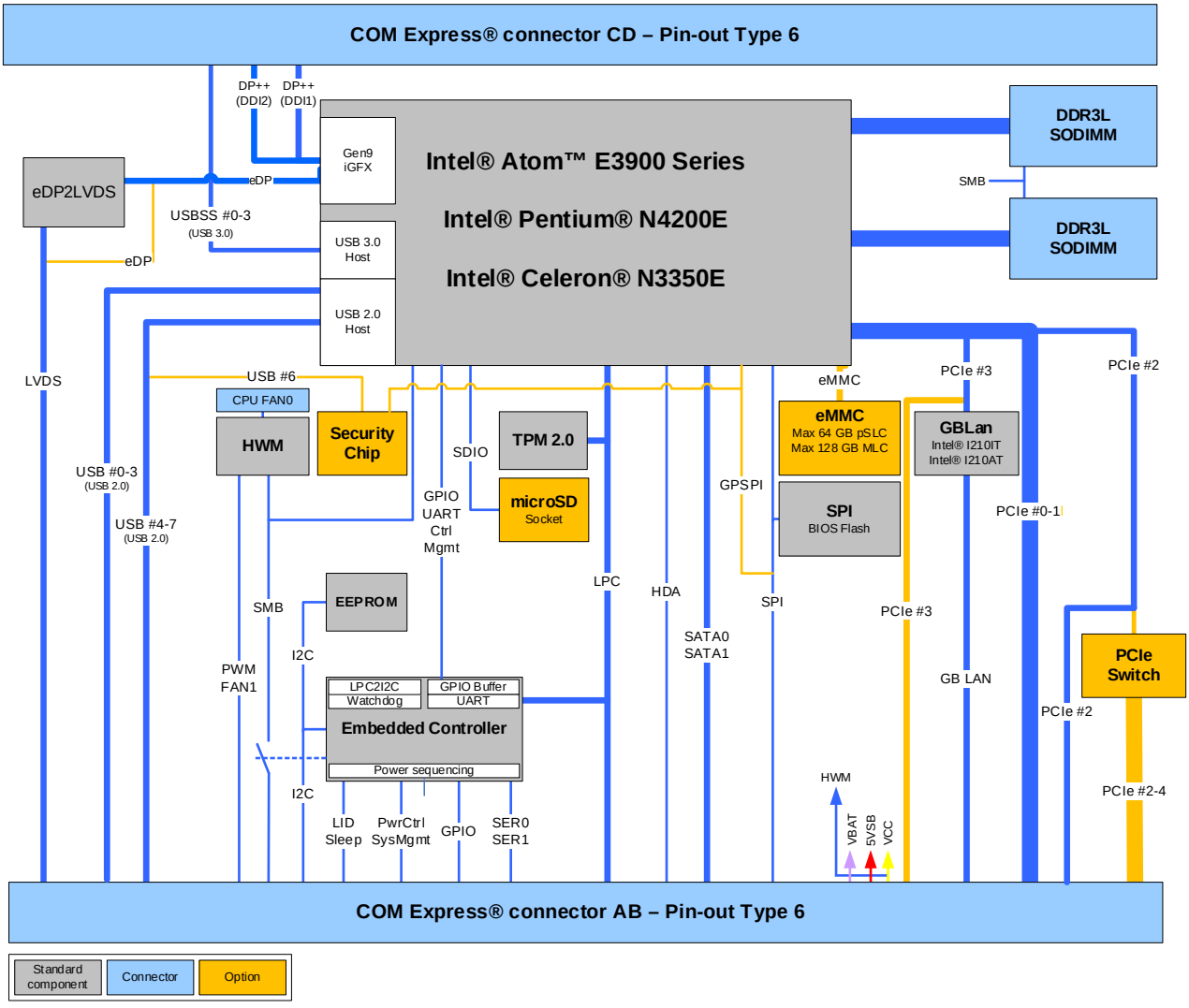
Table 7: Memory Modules

Part Number	Memory (validated reference types)	Description
97015-2048-19-0	DDR3L-1866 SODIMM 2GB_COM	DDR3L SDRAM, 204-pin, Speed = 933 MHz / DDR3L-1866 / 1.35 V
97015-2048-19-2	DDR3L-1866 SODIMM 2GB E2_COM	DDR3L SDRAM, 204-pin, Speed = 933 MHz / DDR3L-1866 / 1.35 V, industrial temperature -40°C to +85°C
97015-4096-19-0	DDR3L-1866 SODIMM 4GB_COM	DDR3L SDRAM, 204-pin, Speed = 933 MHz / DDR3L-1866 / 1.35 V
97015-4096-19-2	DDR3L-1866 SODIMM 4GB E2_COM	DDR3L SDRAM, 204-pin, Speed = 933 MHz / DDR3L-1866 / 1.35 V, industrial temperature -40°C to +85°C
97015-8192-19-0	DDR3L-1866 SODIMM 8GB_COM	DDR3L SDRAM, 204-pin, Speed = 933 MHz / DDR3L-1866 / 1.35 V
97015-8192-19-2	DDR3L-1866 SODIMM 8GB E2_COM	DDR3L SDRAM, 204-pin, Speed = 933 MHz / DDR3L-1866 / 1.35 V, industrial temperature -40°C to +85°C

2.3. Functional Specification

2.3.1. Block Diagram COMe-cAL6

Figure 1: Block Diagram COMe-cAL6



2.3.2. Processor

The Intel® Apollo Lake® series of processors use the 14 nm processor technology with 24 mm x 31 mm package size and FCBGA 1296.

In general, the Intel® Apollo Lake series of processors support the following technologies:

- Intel® 64 Architecture
- Idle States
- Intel® Virtualization Technology (VT-x)
- Intel® Virtualization Technology for Directed I/O (VT-d)
- Secure Boot
- Enhanced Intel Speedstep® Technology
- Thermal Monitoring Technologies
- Intel® HD Audio Technology
- Intel® Identity Protection Technology
- Intel® AES New Instructions
- Secure Key

The following table lists the general Intel® Apollo Lake® processor specifications.

Not all the items specified below are compatible with the COMe-cAL6's functional specification. For items marked with (*), see the relevant subheading in Chapter 2.3 Functional Specification for COMe-cAL6 specific compatibility information.

Table 8: Specification of the COMe-cAL6 Processor Variants

Specifications	Atom™	Atom™	Atom™	Pentium®	Celeron®
	x7 E3950	x5 E3940	x5 E3930	N4200	N3350
# of Cores	4	4	2	4	2
# of Threads	4	4	2	4	2
Processor Base Frequency	1.6 GHz	1.6 GHz	1.3 GHz	1.1 GHz	1.1 GHz
Burst Frequency	2 GHz	1.8 GHz	1.8 GHz	2.5 GHz	2.4 GHz
Thermal Design Power (TDP)	12 W	9.5 W	6.5 W	6 W	6W
Cache	2 MB L2	2 MB L2	2 MB l2	2 MB L2	2 MB LB
Memory Types (*)	DDR3L- up to 1866 LPDDR4 up to 2400	DDR3L- up to 1866 LPDDR4 up to 2133	DDR3L- up to 1866 LPDDR4 up to 2133	DDR3L/LPDDR3- up to 1866	DDR3L/LPDDR3- up to 1866
Max. Memory Channels (*)	4	4	4	2	2
Max. Memory Size	8 GB	8 GB	8 GB	8 GB	8 GB
Max. Memory Bandwidth (*)	38.4 GB/s	34.1 GB/s	34.1 GB/s	29.86 GB/s	29.86 GB/s
ECC Memory (*)	Supported	Supported	Supported	Not supported	Not supported

Specifications	Atom™	Atom™	Atom™	Pentium®	Celeron®
	x7 E3950	x5 E3940	x5 E3930	N4200	N3350
HD Graphics	HD Graphics 505	HD Graphics 500	HD Graphics 500	HD Graphics 505	HD Graphics 500
PCIe Express Configurations (*)	x4, x2, x1	x4, x2, x1	x4, x2, x1	4x1 or 1x4+1x2 or 2x1+1x2+1x2	4x1 or 1x4+1x2 or 2x1+1x2+1x2
Max. # PCIe Lanes (*)	6	6	6	6	6
Use Condition	Embedded Broad Marketing Extended Temp. Industrial Extended Temp.[1]			PC/Client	

[1] The default configuration for the Atom® processor E3900 series is for use condition "Embedded Broad Market Extended Temp".

Contact Kontron support if you want to use the Atom® processor E3900 series in use condition "Industrial Extended Temp" for 24/7 usage.

Detailed information about the various use condition definitions for the Atom® processor E3900 series is available from Intel under NDA

2.3.3. Platform Controller Hub

The Intel® Apollo Lake® product family is a System on a Chip (SoC) solution with integrated chipset.

The following table lists specific Platform Controller Hub (PCH) features.

USB	4x USB 3.0 (including USB 2.0) 4x USB 2.0
VT-d	Supported
SATA RAID	Not supported

2.3.4. System Memory

The system memory supports two memory channels with up to 1866 DDR3L, SO-DIMM sockets for a maximum of up to eight GBytes of non-ECC memory.

The following table lists specific system memory features.

Socket	2x SO-DIMM DDR3L
Memory Type	Channel 1: DDR3L-up to 1866 SO-DIMM, up to 8 GB non-ECC Channel 2: DDR3L-up to 1866 SO-DIMM, up to 8 GB non-ECC
Memory Module Size	2 GByte, 4 GByte and 8 Gbyte
Peak Bandwidth	29.86 GB/s at 1866 MT/s 25.60 GB/s at 1600 MT/s

For a list of Kontron memory modules, see Chapter 2.2 Accessories.

In general, memory modules have a much lower longevity than embedded motherboards, and therefore the EOL of the memory modules may occur several times during the lifetime of the module. Kontron guarantees to maintain memory modules by replacing EOL memory modules with another similar type of qualified module.

As a minimum, it is recommend to use Kontron memory modules for prototype system(s) in order to prove the stability of the system and as a reference.

For volume production, if required, test and qualify other types of RAM. In order to qualify RAM it is recommend to configure three systems running a RAM Stress Test program in a heat chamber at 60°C, for a minimum of 24 hours.

2.3.5. Graphics

2.3.5.1. Digital Display Interfaces

Up to three independent Digital Display Interfaces (DDIs) can be used simultaneously and in combination, to implement an independent or cloned display configuration.

Standard DDIs are:

- 2x DP 1.2 (++) on DDI1/DDI2
- 1x eDP 1.4/LVDS

For the DP++ interface, it is recommended to use DP-to-HDMI and DP-to-DVI dongles that are compliant to the VESA DisplayPort Dual-Mode Standard only.

Otherwise, there might be display detection issues, if dongles are used with FET level shifter for DDC translation.

2.3.5.2. Display Resolution

The following table lists the maximum display resolutions at a set frequency and bit per pixel (bpp) for the supported display interfaces.

Display Interfaces	Maximum Resolution
eDP	3840 x 2160 (60 Hz, 30 bpp)
DP 1.2 (++)	4096 x 2160 (60 Hz, 30 bpp)
HDMI 1.4	3840 x 2160 (30 Hz, 24 bpp)
DVI-D	3840 x 2160 (30 Hz, 24 bpp)

2.3.6. LVDS

A dual channel LVDS interface with two pixels per clock allows for up to 48-bit color. LVDS channel A and control signals are shared with eDP signals. The eDP to LVDS bridge is only necessary for LVDS support and can be removed if LVDS signals are optionally overlaid with eDP signals.

The following table lists basic LVDS features.

LVD Channels	1x or 2x
LVDS Bits / Pixel	Up to 48-bit
LVDS Maximum Resolution	Up to 1920 x 1280 (depending on available panels)
PWM Backlight Control	Configurable LVDS with I2C/PWM backlight support
Supported Panel Data	JILI / EDID / VESA DisplayID

2.3.7. AUDIO

The display controllers DDIs support audio on DP and HDMI. The Intel HDA link allows for the connection of a maximum of one codec that can be connected to an external third party peripheral audio device via the Intel® HDA interface.

Audio controller features are:

- HD-Audio and LPE Audio for DDI0/DDI1
- One external CODEC for external audio devices

2.3.8. PCI Express (PCIE) Lanes [0-4]

The COMe connector supports up to five general-purpose PCIe Gen 1 (2.5 GT/s) or PCIe Gen 2 (5 GT/s) lanes. The number of PCIe lanes varies depending on whether an optional PCIe hub switch and/or LAN is implemented

Four separate external PCIe devices are available on SoC PCIE ports [0-3]. If LAN is implemented, LAN uses SoC PCIE port 3 and only three external PCI devices can be implemented. Up to five external PCIe devices are available if a PCIe hub switch is implemented on SoC PCIE port 2.

The following table shows the supported PCIe port options for COMe lanes [0-4].

Number of PCI Ports	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Comments
3x PCIe Ports (with LAN)	SoC PCIE0	SoC PCIE1	SOC PCIE2	NC	NC	SoC port 3 connected to LAN
4x PCIe Ports (no LAN and no PCIe Switch)	SoC PCIE0	SoC PCIE1	SoC PCIE2	SoC PCIe3	NC	No LAN connection
5x PCIe Ports (with LAN and with PCIe Switch)	SoC PCIE0	SoC PCIE1	PCIe_SW 3	PCIe_SW1	PCIe_SW 2	SoC PCIe port 2 connected to PCIe hub switch and SoC PCIe port 3 connected to LAN

The default PCIe configuration is 3x PCIE ports with LAN. Other PCIe configurations are available for the 4x PCIE port and 5x PCIE port options. For more configuration information, contact Kontron Support.

The following table shows the PCIe link configurations.

COMe Lane	PCIe I/O Port	3x PCIe Ports	4 x PCIe Port			5x PCIe Ports
		Configuration (3x 1) Default	Configuration (4x 1)	Configuration (2x 2)	Configuration (1x 4)	Configuration (5x 1)
0	0	x 1	x 1	x 2	x 4	x 1
1	1	x 1	x 1			x 1
2	2	x 1	x 1	x 2		x 1
3	3	NC	x 1			x 1
4	4	NC	NC	NC	NC	x 1

2.3.9. USB

Both USB 3.0 ports and USB 2.0 ports are available, where USB 3.0 ports are backwards compatible with the USB 2.0 specification. This allows for either a maximum of four USB 3.0 ports and four USB 2.0 ports, or alternatively eight USB 2.0 ports. If the optional Kontron security chip is assembled, the number of available USB 2.0 ports is reduced as USB 2.0 port 6 is no longer available. For more information, see Chapter 3.11 Kontron Security Solution.

The following table lists supported USB features.

USB Ports	4x USB 3.0 ports (Including USB 2.0) 4x USB 2.0 ports
USB Over Current Signals	4x
USB Client Port	1x (USB Port 0 is dual role Client/Host)

The following table lists the COMe connector port and the SoC port USB 3.0 or USB 2.0 combinations.

COMe Port	SoC High-speed I/O Port	SoC Function		Comment
		USB 2.0	USB 3.0	
USB_0	USB#_0	✓	✓	USB 2.0/3.0 dual role, device mode can be enabled with standard BIOS (additional driver support necessary)
USB_1	USB#_1	✓	✓	USB 3.0/USB 2.0
USB_2	USB#_2	✓	✓	
USB_3	USB#_3	✓	✓	
USB_4	USB#_4	✓		USB 2.0
USB_5	USB#_5	✓		
USB_6	USB#_6	✓		USB 2.0 or optional assembly of Kontron's security chip connected to SoC USB2 Port 6 and COMe Port 6. If the security chip is connected, SoC USB2 port 6 is not available.
USB_7	USB#_7	✓		USB 2.0 or on customer request USB 2.0 dual role

2.3.10. SATA

The SATA high-speed storage interface supports two SATA Gen.3 ports with transfer rates of up to 6 Gb/s. The following SATA ports are available at the specified COMe connector ports.

The following table lists the COMe connector port and SoC port SATA combinations.

COMe Port	SoC High-speed I/O Port	SoC Function	Comment
SATA_0	SATA #0	SATA #0	SATA Gen.3, 6 Gb/s
SATA_1	SATA #1	SATA #1	SATA Gen.3, 6 Gb/s

2.3.11. Ethernet

One Gigabit Ethernet port is implemented on GBE0 and supports 10/ 100/ or 1000 Mbit/sec modes .If LAN is implemented, then PCIe port 3 is connected to the Ethernet controller.

The following table lists the supported Ethernet features.

Ethernet	10/100/1000 Mbit
Ethernet Controller	Intel ® i210AT Ethernet controller (commercial temperature) Intel® i210IT Ethernet controller (industrial temp)

Ethernet features are:

- Physical layer ports supporting Ethernet Media Dependent Interfaces MDI[10-3]
- Energy Efficient Ethernet (IEEE 802.3az)
- Jumbo frames (up to 9 kB)
- Interrupt moderation, VLAN support, IP checksum
- RSS and MSI-X to lower CPU utilization in multi-core systems
- Advanced cable diagnostics, auto MDI-X
- Error correcting memory (ECC)
- IEEE1588/802.1AS precision time synchronization for Time Sensitive Networking (TSN) applications

2.3.12. COMe High-speed Interfaces

High-speed serial interfaces, available on the COMe connector include PCI Express Gen. 2, USB 3.0, SATA Gen. 3 and up to 1 Gb Ethernet.

The following table shows the relationship between the COMe connector ports and the SoC high-speed I/O ports.

COMe Port	SoC High-speed I/O Port	SoC I/O Function				Comments
		USB 3.0	PCIe	SATA	LAN	
PCIE_0	PCIe #0		PCIe #0			PCI Express Gen. 2
PCIE_1	PCIe #1		PCIe #1			PCI Express Gen. 2
PCIE_2	PCIe #2		PCIe #2			PCI Express Gen. 2
PCIE_3/ GBE0_MDI	PCIe #3		PCIe #3		GBE0_MDI	Shared lane 1 Gbit LAN or PCIe Express Gen 2
PCIE_4	PCIe #4		PCIe #4			Available for PCIe switch variants only
SATA_0	SATA #0			SATA #0		SATA Gen. 3
SATA_1	SATA #1			SATA #1		
USB_SS0	USB3_0	USB3_0				USB 3.0
USB_SS1	USB3_1	USB3_1				USB 3.0
USB_SS2	USB3_2	USB3_2				USB 3.0
USB_SS3	USB3_3	USB3_3				USB 3.0

2.3.13. Storage Features

The following table lists supported optional on-board storage features.

eMMC	eMMC 5.0 NAND Flash Up to 64 GB pSLC (or up to 128 GB MLC)
SD Card Support	micro SD card slot for SD memory card support compliant to SD memory card specification version 3.01

Pseudo SLC (pSLC) is reconfigured MLC. pSLC memory capacity is half of the MLC capacity.

2.3.14. BIOS/Software Features

The following table lists supported BIOS and software features.

Supported BIOS EFI	AMI Aptio V UEFI
Software	KEAPI 3.0 for all supported OS Linux PLD driver BIOS/EFI Flash utility for EFI shell, Windows, Linux BIOS/EFI Utility for customers to implement Boot Logo
OS Support	Windows 10, (64-bit) Linux 64 bit + LiveCD VxWorks 7.X (64-bit)

2.3.15. COM Features

The following table lists supported COMe specification features. For more information, refer to COM Express® Spec.

SPI	Boot from an external SPI
LPC	Supported
UART	2x UART (RX/TX)
LID Signal	Supported
Sleep Signal	Supported
Audio	1x external HDA codec
SMBus	Supported

2.3.16. Kontron Features

The following table lists supported Kontron specific product features.

External I2C Bus	Fast I2C, 0 KHz - 400 kHz, MultiMaster capable
Embedded API	KEAPI3
Custom BIOS Settings / Flash Backup	Supported
Watchdog Support	Dual staged
External SIO	Supported on the baseboard
GPIO	8x GPIO (4x GPI and 4X GPO)

2.4. Electrical Specification

2.4.1. Power Supply Voltage Specification

The COMe-cAL6 supports operation in both ATX and single power supply modes.

The following table lists the power supply voltages.

Supply Voltage (VCC)	12 V
Standby Voltage	5 V ±5%
Supply Voltage Range (VCC)	8.5 V to 20 V (across the whole temperature range)
RTC Voltage Range	2.8 V to 3.47 V

5 V Standby voltage is not mandatory for operation.

2.4.1.1. Power Supply Rise Time

The input voltage rise time is 0.1 ms to 20 ms from input voltage ≤10% to nominal VCC (12 V). To comply with the ATX specification there must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of the DC input voltage final set point.

2.4.1.2. Power Supply Voltage ripple

The maximum power supply voltage ripple is 100 mV peak-to-peak at 0 MHz to 20 MHz.

2.4.2. Power Management

Power management options are available within the BIOS setup.

ACPI Settings	ACPI 5.0
Miscellaneous Power Management	Supported in BIOS setup menu

Within the BIOS setup, If VCC power is removed, 5 V ±5% can be applied to the V_5V_STBY pins to support the following suspend-states:

- Suspend to RAM (S3)
- Suspend-to-disk / Hibernate (S4)
- Soft-off state (S5)

The Wake-Up event (S0) requires VCC power, as the board is running.

2.4.3. Power Supply Control Settings

The power supply control settings are set in the BIOS and enable the module to shut down, rest and wake from standby properly.

The following table lists the implemented powersupply control settings.

Power Button (PWRBTN#)	Pin B12	To start the module using the power button, the PWRBTN# signal must be at least 50 ms (50 ms ≤ t < 4 s, typical 400 ms) at low level (Power Button Event). Pressing the power button for at least four seconds turns off power to the module (Power Button Override).
Power Good (PWR_OK)	Pin B24	PWR_OK is internally pulled up to 3.3 V and must be at the high level to power on the module. This can be driven low to hold the module from powering up as long as needed. The carrier needs to release the signal when ready. Low level prevents the module from entering the S0 state. A falling edge during S0 causes a direct switch to S5 (Power Failure). After a power failure (PWR_OK going HIGH again) the module will not start up automatically.
Reset Button (SYS_RESET#)	Pin B49	When the SYS_RESET# pin is detected active (falling edge triggered), it allows the processor to perform a "graceful" reset, by waiting up to 25 ms for the SMBus to go idle before forcing a reset, even though activity is still occurring. Once the reset is asserted, it remains asserted for 5 ms to 6 ms regardless of whether the SYS_RESET# input remains asserted or not.
SM-Bus Alert (SMB_ALERT#)	Pin B15	With an external battery manager present and SMB_ALERT #connected, the module always powers on even if the BIOS switch "After Power Fail" is set to "Stay Off".

The COMe-cAL6 includes an additional cold reset during the first cold boot after a complete power loss (including battery voltage). This additional reset will not happen on any subsequent warm or cold reboots.

2.4.4. Power Supply Modes

Setting the power supply controls enables the module to operating in either ATX power mode or in single power supply mode.

2.4.4.1. ATX Power Mode

To start the module in ATX mode and power VCC, follow the step below.

1. Connect the ATX PSU with VCC and 5 VSB to set PWR_OK to low and VCC to 0 V.
2. Pressing the power button then sets the PWR_OK to high and powers VCC.

The PS_ON# signal, generated by SUS_S3# (A15), indicates that the system is in Suspend to RAM state. An inverted copy of SUS_S3# on the carrier board may be used to enable non-standby power on a typical ATX supply. The input voltage must always be higher than 5 V standby (VCC > 5 VSB) for Computer-on-Modules supporting a wide input voltage range down to 8.5 V.

The following table lists the ATX power mode settings.

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0 V	x	0 V
S5	High	Low	5 V	High	0 V
S5 → S0	PWRBTN event	Low → High	5 V	High → Low	0 V→ VCC
S0	High	High	5 V	Low	VCC

(x) – Defines there is no difference if connected or open.

2.4.4.2. Single Supply Power Mode

In single supply mode, without 5 V standby, the module starts automatically if VCC power is connected and the Power Good input is open or at the high level (internal PU to 3.3 V).

PS_ON# is not used in single supply mode and the input voltage VCC range can be 8.5 V to 20 V.

To power on the module from S5 state, press the power button or reconnect VCC. Suspend/Standby states are not supported in single supply mode.

The following table lists the single supply power mode settings.

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	0 V / x	0 V / x	0 V / x	0 V / x
G3 → S0	High	Open / High	Open	connecting VCC
S5	High	Open / High	Open	VCC
S5 → S0	PWRBTN event	Open / High	Open	reconnecting VCC

(x) – Defines there is no difference if connected or open.

All ground pins must be connected to the carrier board's ground plane.

2.5. Thermal Management

2.5.1. Heatspreader Plate (HSP) Assembly and Metal Heat Slug

A heatspreader plate assembly is available for the COMe-cAL6, see Table 4: Product Specific Accessories. The heatspreader plate assembly is NOT a heat sink. The heatspreader works as a COM Express® standard thermal interface to be use with a heat sink or external cooling devices. External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any part of the heatspreader's surface according to the module specifications:

- 60°C for commercial grade modules
- 85°C for industrial temperature grade modules (E2S)

Commercial temperature grade variants have no preconfigured Intel heatspreader and the supplied metal heat slug (packed separately in the delivery box for the heatspreader) must be installed.

Industrial temperature grade variants have a preconfigured Intel heatspreader and do not require the metal heat slug to be installed.

For industrial temperature grade variants the CPU comes with a preconfigured heatspreader and the supplied metal heat slug is not required.

2.5.2. Active or Passive Cooling Solutions

Both active and passive thermal management approaches can be used with heatspreader plates. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Active or passive cooling solutions provided from Kontron for the COMe-cAL6 are usually designed to cover the power and thermal dissipation for a commercial temperature range used in housing with proper airflow. For more information concerning possible cooling solutions, see Table 6: General COMe Accessories.

2.5.3. Operating with Kontron Heatspreader Plate (HSP) Assembly

The operating temperature defines two requirements:

- Maximum ambient temperature with ambient being the air surrounding the module
- Maximum measurable temperature on any part of the heatspreader's surface

The heatspreader is tested for the following temperature specifications.

Table 9: Heatspreader Test Temperature Specifications

Temperature Specification	Validation Requirements
Commercial Grade	At 60°C HSP temperature the CPU @ 100% load needs to run at nominal frequency
Industrial Grade by screening (E2S)	At 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection

2.5.4. Operating without Kontron Heatspreader Plate (HSP) Assembly

The operating temperature is the maximum measurable temperature on **any** part of the module's surface.

2.5.5. On-board Fan Connector

The module's fan connector powers, controls and monitors a fan for chassis ventilation.

Table 10: 3-Pin Fan Connector Pin Assignment

Pin	Signal	Description	Type
1	Fan_Tach_IN#	Input voltage	I
2	V_FAN	Limited to a maximum of 12 V (±10%) across the whole input range	PWR
3	GND	Power GND	PWR

To connect a standard 3-pin connector fan to the module, use one of the following adaptor cables:

- KAB-HSP 200 mm (Part number- 96079-0000-00-0)
- KAB-HSP 40 mm (Part number - 96079-0000-00-2)

NOTICE

Always check the fan specification according to the limitations of the supply current and supply voltage.

If the input voltage is below 12 V or equal to 12 V, then the maximum supply current to the on-board fan connector is 350 mA and the fan output voltage is equal to the module input voltage. The maximum supply current is limited to 150 mA if the input voltage is more than 12 V but less than the maximum voltage input of 20 V. For an overview of the electrical characteristics, see Table 11: Electrical Characteristics of the Fan Connector.

Table 11: Electrical Characteristics of the Fan Connector

Module Input Voltage <= 12 V	
FAN Output Voltage	Equal to module's input voltage
FAN Output Current	Up to 350 mA
Module Input Voltage >12 V to <=20 V	
FAN Output Voltage	12 V (±10%)
FAN Output Current	Limited to 150 mA

2.6. Environmental Specification

2.6.1. Temperature

Kontron defines the following operating and non-operating temperature grades for Computer-on-Modules. For more information on the available temperature grades for the COMe-cAL6, see Chapter 2.1, Module Variants.

Table 12: Temperature Grade Specifications

Temperature Grades	Operating	Non-operating (Storage Temperature)
Commercial Grade	0°C to +60°C	-30°C to +85°C
Industrial Temperature Grade E2S (by screening)	-40°C to +85°C	-40°C to +85°C

2.6.2. Humidity

Table 13: Humidity Specification

Humidity	
Relative Humidity	93%, at +40°C, non-condensing (according to IEC 60068-2-78)

2.7. Standards and Certifications

The COMe-cAL6 complies with the following standards and certifications. For more information, contact Kontron Support.

Emission (EMC)	IEC / EN 61000-6-3 Electromagnetic compatibility (EMC)- Part 6-3:Generic standards – Emission standard for residential, commercial and light industrial environments Including the following tests: EN55032 Class B – Electromagnetic compatibility of multimedia equipment- Emission requirements CISPR 32 (modified) IEC / EN 61000-3-2 - Harmonic current emissions IEC / EN 61000-3-3 - Voltage changes, voltage fluctuations and flicker
Immunity (EMI)	IEC / EN 61000-6-2 Electromagnetic (EMC) – Part 6-2: Generic standards immunity for industrial environments Including the following tests: IEC / EN 61000-4-2 - Electrostatic discharge (ESD) immunity IEC / EN 61000-4-3 – Radiated, radio-frequency, electromagnetic field immunity IEC / EN 61000-4-4 - Electrical fast transient/burst immunity IEC / EN 61000-4-5 - Surge immunity test IEC / EN 61000-4-6 - Immunity to conducted disturbances, induced by radio-frequency fields IEC / EN 61000-4-8 - Power frequency magnetic field immunity IEC / EN 61000-4-11 - Voltage dips, short interruptions, and voltage variations immunity
Safety	EN 62368-1 Safety for audio/video and information technology equipment UL 60950-1 / CSA 60950-1 Information Technology Equipment Including Electrical Business Equipment NWGQ2.E304278 NWGQ8.E304278
Shock	IEC / EN 60068-2-27 Non-operating shock test – (half-sinusoidal, 11 ms, 15 g)
Vibration	IEC / EN 60068-2-6 Non-operating vibration – (sinusoidal, 10 Hz – 4000 Hz, +/- 0.15 mm, 2 g)
(RoHS II)	2011/65/EU Compliant with the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment

2.7.1. MTBF

The MTBF (Mean Time Before Failure) values were calculated using a combination of the manufacturer's test data, (if available) and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The Telcordia calculation used is "Method 1 Case 3" in a ground benign, controlled environment. This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned-in. Other environmental stresses (such as extreme altitude, vibration, salt-water exposure) lower MTBF values.

Table 14: MTBF Estimated Values

MTBF
System MTBF(hour) = 829207 @ 40°C for the COMe-cAL6 N4200 Reliability report article number: 36023-0000-11-4
System MTBF(hour) = 684743 @ 40°C for the COMe-cAL6 E2 E3950 32S Reliability report article number: 36024-0032-16-7

Fans usually shipped with Kontron's modules have a 50,000 hour typical operating life. The MTBF estimated values above assumes no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the module is connected to an external power source, the only battery drain is from leakage paths.

Figure 2 and Figure 3 show the MTBF de-rating values for module used in the E1 (-25°C to +75°C) temperature range in an office or telecommunications environment. Other environmental stresses (extreme altitude, vibration, salt-water exposure, etc.) lower MTBF values.

Figure 2: MTBF De-rating Values @ 40°C for the COMe- cAL6 N4200 (MTBF: 829207 hours)

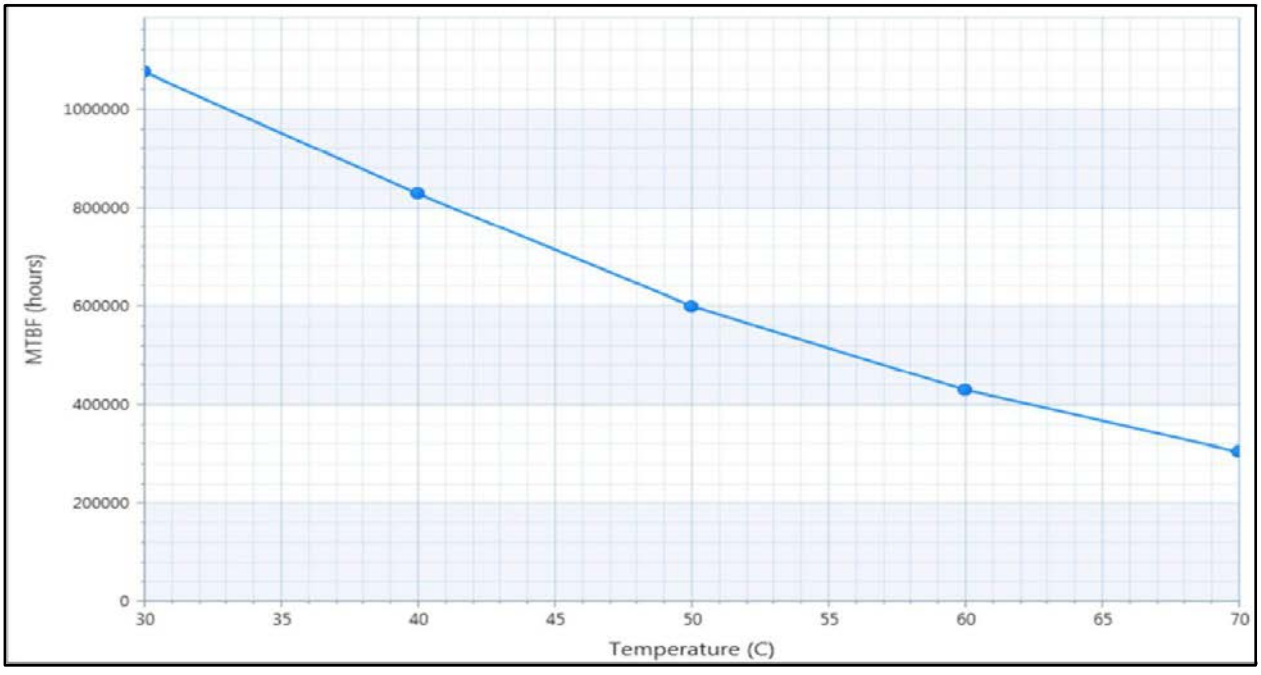
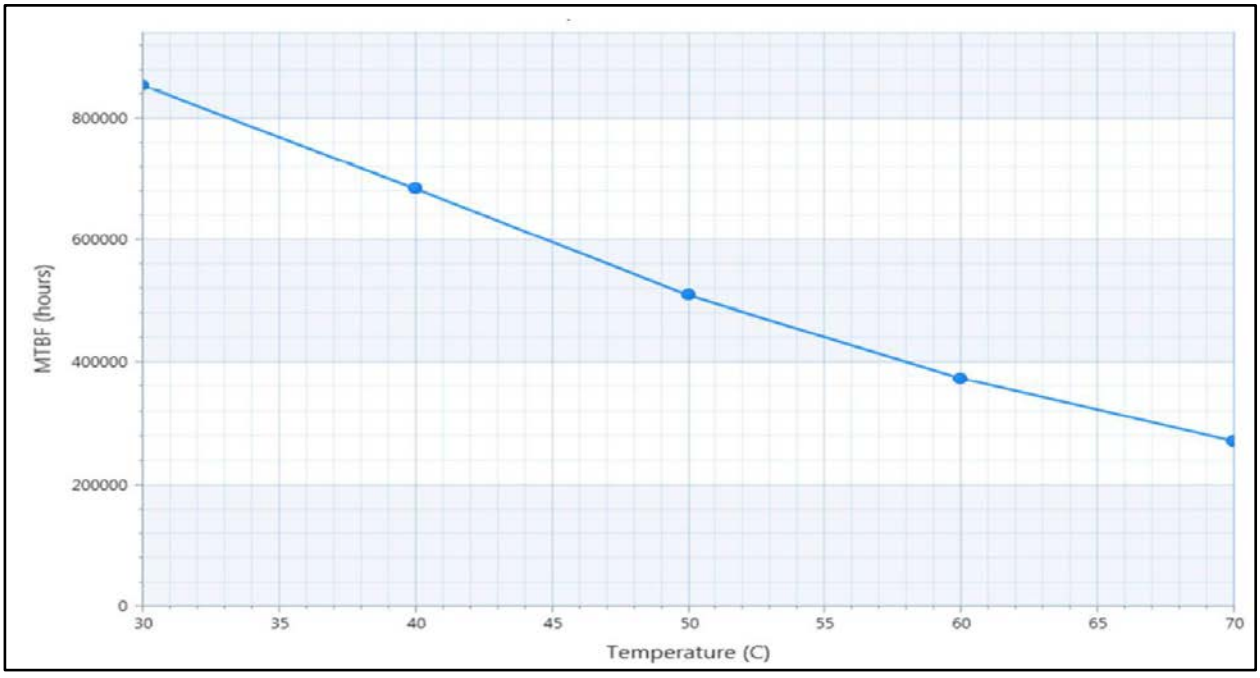


Figure 3: MTBF De-rating Values @ 40°C for the COMe- cAL6 E2 E3950 32S (MTBF: 684743 hours)



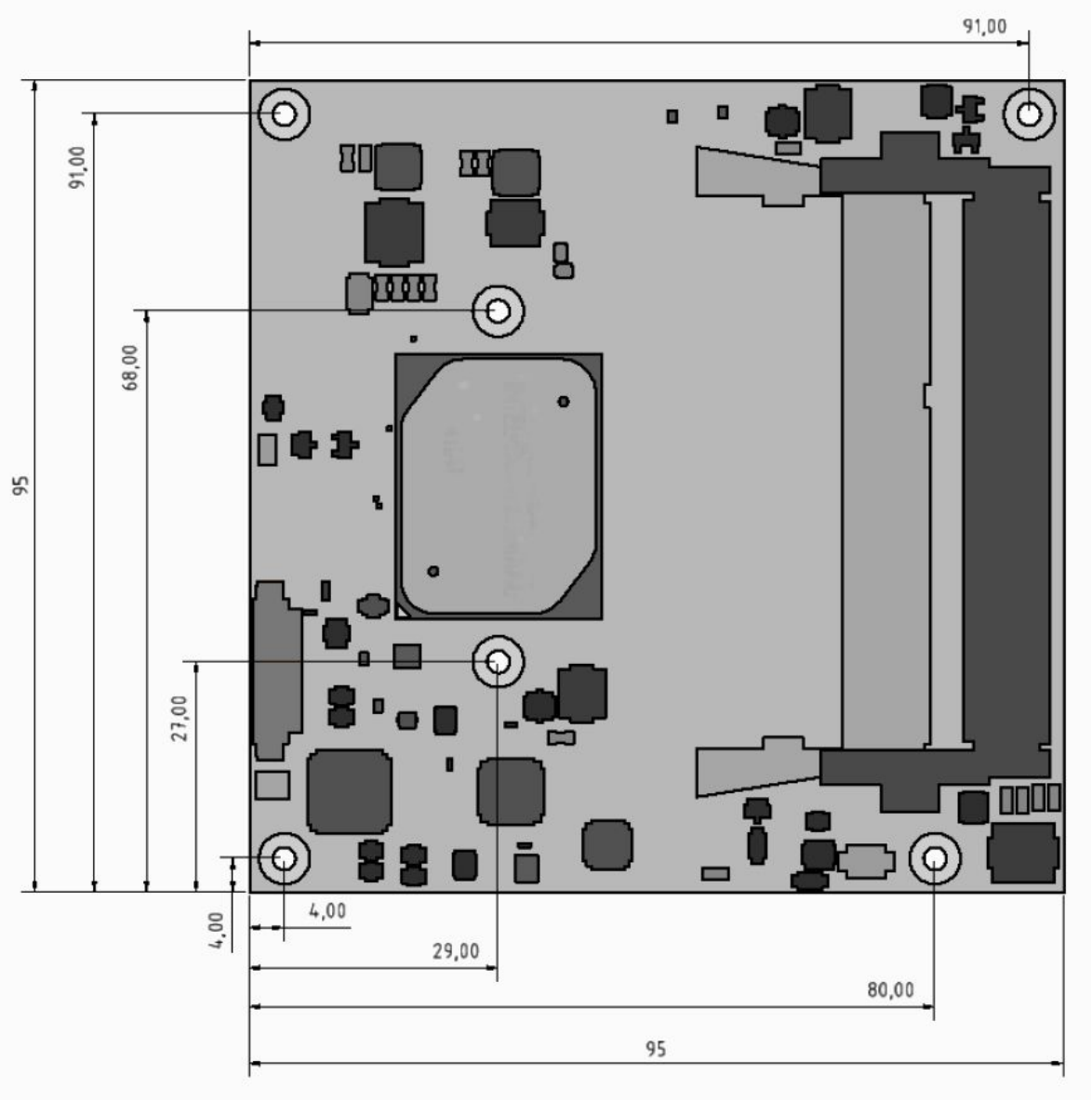
2.8. Mechanical Specification

The COMe-cAL6 is compliant to the mechanical specification of the COM Express® PICMG COM.0 Rev. 2.1.

2.8.1. Module Dimensions

The dimensions of the compact module are 95.0 mm x 95.0 mm (3.75 " x 3.75 “)

Figure 4: Module Dimensions



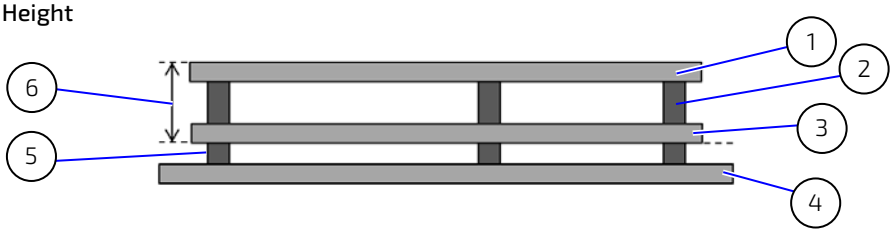
*All dimensions in mm.

2.8.2. Module Height

The overall height of the module depends on the height of the implemented cooling solution. The COM Express® Specification does not specify the height of the cooling solution.

The COM Express® specification defines a module height of approximately 13 mm from the bottom of the module's PCB board to the top of the heatspreader, as shown in Figure 5: Module Height.

Figure 5: Module Height



1	Heatspreader	4	Carrier Board PCB
2	Heatspreaader standoff(s)	5	Connector standoff(s) 5 or 8 mm
3	Module PCB board	6	13 mm +/- 0.65 mm

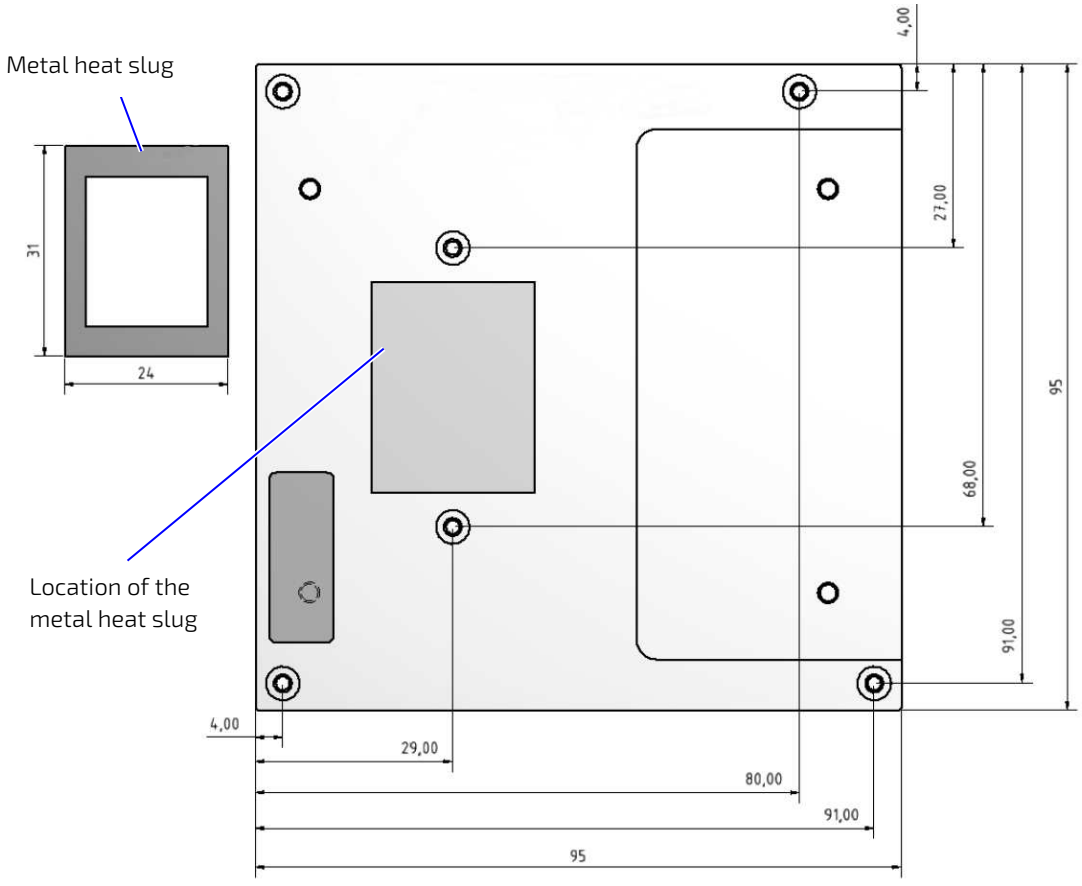
2.8.3. Heatspreader Dimensions

The COMe-cAL6 is available in commercial and industrial temperature grade variants, where:

- Industrial temperature grade CPUs have a preconfigured Intel heatspreader
- Commercial temperature grade CPUs have no preconfigured Intel heatspreader and the supplied metal heat slug (packed separately in the delivery box for the heatspreader) must be installed

For industrial temperature grade variants the CPU comes with a preconfigured heatspreader and the supplied metal heat slug is not required.

Figure 6: Heatspreader and Metal Heat Slug Dimensions



*All dimensions shown in mm.

3/ Features and Interfaces

3.1. eMMC Flash Memory

An optional embedded Multimedia Flash Card (eMMC) complying with the eMMC 5.0 specification can be permanently attached to the module, allowing for a capacity of up to 64 GByte NAND Flash. During the COMe-cAL6's manufacturing process, Multi Level Cell (MLC) eMMC is reconfigured to act as a pseudo Single Level Cell (pSLC) eMMC to provide improved reliability, endurance and performance.

Specific eMMC Flash memory features are:

- Up to 64 GByte pSLC (or128 GB MLC)
- eMMC 5.0 specification
- Class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
- HS200/HS400 modes
- DDR modes up to 52 MHz clock speed
- ECC and block management
- Boot operation (High-speed boot)
- Sleep mode
- Permanent and power-on write protection
- Replay-protected memory block (RPMB)
- Secure erase and secure trim

3.2. Micro SD Card

An ultra-low micro SD card socket is available as an optional feature on the SD Interface. The micro SD card socket supports a micro SD Flash memory card that complies with the micro SD 3.01 memory card specification and supports:

- Card detection
- Date rates up to 104 MB/s

3.3. LPC

The Low Pin Count (LPC) interface signals are connected to the LPC bus bridge located in the CPU or CPU's chipset. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O controller that typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. The COM Express® Design Guide maintained by PICMG provides implementation information or refer to the official PICMG documentation for more information.

The LPC bus does not support DMA (Direct Memory Access). When more than one device is used on LPC, a zero delay clock buffer is required. This leads to limitations for the ISA bus and SIO (standard I/O(s) like floppy or LPT interfaces) implementations.

All Kontron COM Express® Computer-on-Modules imply BIOS support for the following external baseboard LPC Super I/O controller features for the Winbond/Nuvoton 3.3V 83627DHG-P.

Table 15: Supported BIOS Features

3.3V 83627DHG-P	AMI EFI APTIO V
PS/2 , LPT, HWM, Floppy, GPIO	Not supported
COM1/COM2	Supported

Features marked as not supported do not exclude OS support., except for, HWM that is controlled by the BIOS setup within the Advanced setup menu and has no OS software support. The HWM is accessible via the System Management (SM) Bus, for more information, see Chapter 4.6 System Management (SM) Bus. If any other LPC Super I/O additional BIOS implementations are necessary, contact Kontron Support.

3.4. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface Bus (SPI bus) is a synchronous serial data link standard. Devices communicate in master/slave mode, where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. SPI is sometimes called a four-wire serial bus, contrasting with three, two and one-wire serial buses.

The SPI interface can only be used with a SPI flash device to boot from the external BIOS on the baseboard. No alternative usage is possible.

3.4.1. SPI Boot

It is not possible to flash to a SPI chip that is not the boot SPI flash chip. The only two possible options to flash the SPI chip are:

1. Boot from **internal** SPI Flash chip and flash the **internal** SPI Flash chip
2. Boot from **external** SPI Flash chip and flash the **external** SPI Flash chip

It is NOT POSSIBLE to flash the SPI chip by booting from an external SPI Flash chip and flash the internal SPI Flash chip.

The COMe-cAL6 supports boot from an external 16 MB, 3 V serial SPI Flash supports boot from an external SPI Flash, where pin A34 (BIOS_DIS0#) and pin B88 (BIOS_DIS1#) configure the SPI Flash as shown in Table 16: SPI Boot Pin Configuration.

Table 16: SPI Boot Pin Configuration

Configuration	BIOS_DIS0#	BIOS_DIS1#	Function
1	Open	Open	Boot on module SPI
2	GND	Open	Not supported
3	Open	GND	Boot on carrier SPI
4	GND	GND	Not supported

BIOS does not support being split between two chips. Booting takes place either from the module SPI or from the baseboard SPI.

Table 17: Supported SPI Boot Flash Types for 8-SOIC Package

Size	Manufacturer	Part Number	Device ID
16MB	Maxim	MX25L12835F	0x20
16MB	Winbond	W25Q128FV	0x40
16MB	Micron	N25Q128A	0xBA

3.4.2. Booting from an External SPI Flash

Initially, boot on the EFI Shell with an USB key containing the binary used to flash the SPI, plugged in on the system. Depending on which SPI you would like to flash, you will need to use the (BIOS_DIS1) selection jumper located on the COM Express® carrier, to determine BIOS boot device.

To flash the carrier or module Flash chip:

1. Connect a SPI flash with the correct size (similar to BIOS binary (*.BIN) file size) to the carrier SPI interface.
2. Open pin A34 (BIOS_DIS0#) and connect pin B88 (BIOS_DIS1#) to ground, to enable the external SPI flash to boot on carrier SPI.
3. Turn on the system and make sure that USB is connected then start the uEFI BIOS setup. (See Chapter 6.1 Starting the uEFI BIOS.)
4. Disable the BIOS lock:

   Chipset > South Cluster Configuration> Miscellaneous Configuration> BIOS Lock > Disabled
5. Save and exit the setup.
6. Reboot system into EFI shell.
7. From the EFI shell, enter the name of the partition of the USB Key in this example; select FS0: then press <enter>.
8. Enter the following:

```
FPT –F <biosname.BIN>
```

9. Wait until the program ends properly and then power cycle the whole system.
10. The system is now updated.

Depending on the state of the external SPI flash, the program may display up to two warning messages printed in red. Do not stop the process at this point! After a few seconds of timeout, flashing proceeds. For more information, refer to the Kontron's Customer Section.

3.4.3. External SPI Flash on Modules with Intel® ME

If booting from the external (baseboard mounted) SPI flash then exchanging the COM Express® module for another module of the same type will cause the Intel® Management Engine (ME) to fail during the next start. This is due to the design of the ME that bounds itself to every module, to which the ME was previously flashed. In the case of an external SPI flash, this is the module present at flash time.

To avoid this issue, conduct a complete flash of the external SPI flash device after changing the COM Express® module for another module. If disconnecting and reconnecting the same module again, this step is not necessary.

3.5. Fast I2C

Fast I2C supports transfer between components on the same board. The COMe-cAL6 features an onboard I2C controller connected to the LPC Bus.

The I2C controller supports:

- Multimaster transfers
- Clock stretching
- Collision detection
- Interruption on completion of an operation

3.6. UART

The UART implements an interface for serial communications and supports up to two serial RX/TX ports defined in the COM Express® specification on pins A98 (SERO_TX) /A99 (SERO_RX) for UART0 and pins A101 (SER1_TX)/A102 (SER1_RX) for UART1. The UART controller is fully 16550A compatible.

Features of the UART are:

- On-Chip bit rate (baud rate) generator
- No handshake lines
- Interrupt function to the host
- FIFO buffer for incoming and outgoing data

3.7. Dual Staged Watchdog Timer (WDT)

A watchdog timer or computer operating properly (COP) timer is a computer hardware or software timer. If there is a fault condition in the main program, the watchdog triggers a system reset or other corrective actions. The intention is to bring the system back from the non-responsive state to normal operation.

Possible fault conditions are a hang, neglect to service the watchdog regularly (writing a “service pulse” to it, also referred to as “kicking the dog”, “petting the dog”, “feeding the watchdog” or “triggering the watchdog”).

The COMe-cAL6 offers a watchdog that works with two stages that can be programmed independently and used stage-by-stage.

Table 18: Dual Stage Watchdog Timer- Time-out Events

0000b	**No action**	The stage is off and will be skipped.
0001b	**Reset**	A reset restarts the module and starts a new POST and operating system.
0101b	**Delay -> No action***	Might be necessary when an operating system must be started and the time for the first trigger pulse must be extended. Only available in the first stage.
1000b	**WDT Only**	This triggers the WDT Pin on the baseboard connector (COM Express® pin B27) only.

1001b	Reset + WDT	
1101b	DELAY + WDT -> No action*	

3.7.1. WDT Signal

Watchdog time-out event (pin B27) on COM Express® connector offers a signal that can be asserted when a watchdog timer has not been triggered with a set time. The WDT signal is configurable to any of the two stages. After reset, the signal is automatically deasserted. If deassertion is necessary during runtime, contact Kontron Support for further help.

3.8. GPIO

The eight GPIO pins support four inputs pins (A54 for GPI0, A63 for GPI1, A67 for GPI2 and A85 for GPI3) and four output pins (A93 for GPO0, B54 for GPO1, B57 for GPO2 and B63 for GPO3) by default. The four GPI [0-3] pins are pulled high with a pull-up resistor (e.g. 100 K ohms) and the four GPO [0-3] pins are pulled low with a pull-down resistor (e.g. 100 K ohms) on the module.

To change the default GPIO signal-state users are required to make BIOS and/or OS-driver changes, and additional hardware changes by adding external termination resistors on the carrier board to override the weak on-module pull-up resistors with a lower resistance pull-down (e.g. 10 K ohms), or pull-down resistors with a lower resistance pull-up (e.g. 10 K ohms).

3.9. Real Time Clock (RTC)

The RTC keeps track of the current time accurately. The RTC's low power consumption means that it can be powered from an alternate source of power enabling the RTC to continue to keep time while the primary source of power is “off” or “unavailable”.

The RTC battery voltage range is 2.8 V to 3.47 V. A typical RTC voltage is 3 V with a current of >10 µA. If the module is powered by the mains supply, the on-module regulators generate the RTC voltage to reduce RTC current draw.

3.10. Trusted Platform Module (TPM 2.0)

The COMe-cAL6 is compliant to Trusted Platform Module TPM 2.0. A TPM stores RSA encryption keys specific to the host system for hardware authentication. The term TPM refers to the set of specifications applicable to TPM chips. The LPC bus connects the TPM Chip to the CPU.

Each TPM chip contains an RSA key pair called the Endorsement Key (EK). The pair is maintained inside the chip and cannot be accessed by software. The Storage Root Key (SRK) is created when a user or administrator takes ownership of the system. This key pair is generated by the TPM based on the Endorsement Key and an owner-specified password.

A second key, called an Attestation Identity Key (AIK) protects the device against unauthorized firmware and software modification by hashing critical sections of firmware and software before they are executed. When the system attempts to connect to the network, the hashes are sent to a server that verifies that they match the expected values. If any of the hashed components have been modified since last started, the match fails, and the system cannot gain entry to the network.

3.11. Kontron Security Solution

Kontron Security Solution is a combined hardware and software solution that includes an embedded hardware security module and a software framework to protect applications. The COMe-cAL6 allows for the optional assembly of an integrated security module connected to SoC USB2 port 6. If the security chip is connected, SoC USB2 port 6 is not available for use as a USB 2.0 port.

Features of the integrated security solution are:

- Copy protection
- IP protection
- License model enforcement

If required, customers can customize the security solution to meet specific needs. For more information, contact Kontron Support.

3.12. SpeedStep® Technology

SpeedStep® technology enables the adaption of high performance computing to applications by switching automatically between maximum performance mode and battery-optimized mode, depending on the needs of the application. When battery powered or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, thus conserving battery life while maintaining a high level of performance. The frequency is automatically set back to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep® technology the operating system must support SpeedStep® technology.

By deactivating the SpeedStep® feature in the BIOS, manual control or modification of the CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use third party software to control the CPU Performance States.

4/ System Resources

4.1. Interrupt Request (IRQ) Lines

The following table specifies the device connected to each Interrupt line or if the line is available for new devices.

Table 19: Interrupt Requests

IRQ	General Usage	Project Usage
0	Timer	Timer
1	Keyboard	Keyboard (Super I/O)
2	Redirected secondary PIC	Redirected secondary PIC
3	COM2	COM2
4	COM1	COM1
5	LPT2/PCI devices	One of COM3+4
6	FDD	One of COM3+4 or not used
7	LPT1	LPT1 or one of COM3+4
8	RTC	RTC
9	SCI / PCI devices	Free for PCI devices
10	PCI devices	Free for PCI devices
11	PCI devices	Free for PCI devices
12	PS/2 mouse	Free for PCI devices
13	FPU	FPU
14	IDE0	Not used
15	IDE1	Not used

4.2. Memory Area

The following table specifies the usage of the address ranges within the memory area.

Table 20: Designated Memory Locations

Address Range (hex)	Size	Project Usage
00000000-0009FBFF	639 KB	Real mode memory
0009FC00-0009FFFF	1 KB	Extended BDA
000A0000-000BFFFF	128 KB	Display memory (legacy)
000C0000-000CBFFF	48 KB	VGA BIOS (legacy)
000CC000-000DFFFF	80 KB	Option ROM or XMS (legacy)
000E0000-000EFFFF	64 KB	System BIOS extended space (legacy)
000F0000-000FFFFF	64 KB	System BIOS base segment (legacy)
00100000-7FFFFFFF	128 MB	System memory (Low DRAM)
80000000-FFF00000	2 GB – 1 MB	PCI memory, other extensions (Low MMIO)
FEC00000-FEC00FFF	4 KB	IOxAPIC
FED00000-FED003FF	1 KB	HPET (Timer)
FED40000-FED40FFF	4KB	Always reserved for LPC TPM usage
FEE00000-FEEFFFFF	1MB	Local APIC region
FFFC0000-FFFFFFFF	256 KB	Mapping space for BIOS ROM/Boot vector
100000000-17FFFFFFF	2 GB	System memory (High DRAM)
180000000-F00000000	58 GB	High MMIO

4.3. I/O Address Map

The I/O port addresses are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0100h with additional hardware, for compatibility reasons, even if the I/O address is available.

Table 21: Designated I/O Port Address

I/O Address Range	General Usage	Project Usage
000-00F	DMA-Controller (Master) (8237)	DMA-Controller (Master) (8237)
020-021 024-025 028-029 02C-02D 030-031 034-035 038-039 03C-03D	Interrupt-Controller (Master) (8259)	Interrupt-Controller (Master) (8259)
02E-02F	SuperIO (Winbond)	External SuperIO (Winbond)
040-043 050-053	Programmable Interrupt Timer (8253)	Programmable Interrupt Timer (8253)
04E-04F	2nd SuperIO, TPM etc.	TPM
060, 064	KBD Interface-Controller (8042)	KBD Interface-Controller (8042)
061, 063 065, 067	NMI Controller	NMI Controller
062, 066	Embedded Microcontroller	Not used
070-071	RTC CMOS / NMI mask	RTC CMOS / NMI mask
072-073	RTC Extended CMOS	RTC Extended CMOS
080-083	Debug port	Debug port
0A0-0A1 0A4-0A5 0A8-0A9 0AC-0AD 0B0-0B1 0B4-0B5 0B8-0B9 0BC-0BD	Interrupt-Controller (Slave) (8259)	Interrupt-Controller (Slave) (8259)
0B2-0B3	APM control	APM control
0C0-0DF	DMA-Controller (Slave) (8237)(N/A)	Not used
0F0-0FF	FPU (N/A)	Not used
170-177	HDD-Controller IDE1 Master	Not used
1F0-1F7	HDD-Controller IDE0 Master	Not used
200-207	Gameport	Not used
220-22F	Soundblaster®	Not used
279	ISA PnP	ISA PnP
278-27F	Parallel port LPT2	Not used
295-296	Hardware monitor (Winbond default)	Reserved (If SuperIO present)
2B0-2BF	EGA	Not used
2D0-2DF	EGA	Not used
2E8-2EF	Serial port COM 4	Serial port COM4 (optional)
2F8-2FF	Serial port COM 2	Serial port COM2 from CPLD

I/O Address Range	General Usage	Project Usage
300-301	MIDI	Not used
300-31F	System specific peripherals	Not used
370-377	Floppy disk controller	Not used
376-377	HDD-Controller IDE1 Slave	Not used
378-37F	Parallel port LPT 1	LPT1 (If SuperIO present)
3BC-3BF	Parallel port LPT3	Not used
3C0-3CF	VGA/EGA	VGA/EGA
3D0-3DF	CGA	Not used
3E0-3E1	PCMCIA ExCA interface	Not used
3E8-3EF	Serial port COM3	Serial port COM3 (optional)
3F0-3F7	Floppy Disk Controller	Not used
3F6-3F7	HDD controller IDE0 Slave	Not used
3F8-3FF	Serial Port COM1	Serial port COM1
4D0-4D1	Interrupt-Controller (Slave)	Interrupt-Controller (Slave)
A80-A81	Kontron CPLD	Kontron CPLD control port
CF8	PCI configuration address	PCI configuration address
CF9	Reset control	Reset control
CFC-CFF	PCI configuration data	PCI configuration data

Other PCI device I/O addresses are allocated dynamically and not listed here. For more information on how to determine I/O address usage, refer to the OS documentation.

4.4. Peripheral Component Interconnect (PCI) Devices

All devices follow the PCI 2.3 and PCIe Base 1.0a specification. The BIOS and Operating System (OS) control the memory and I/O resources. For more information, refer to the PCI 2.3 specification.

4.5. I2C Bus

The following table specifies the devices connected the I2C bus including the I2C address.

Table 22: I2C Bus Port Address

I2C Address	Used For	Available	Comment
A0h	JIDA-EEPROM	No	Module EEPROM
AEh	FRU-EEPROM	No	Recommended for Baseboard EEPROM

4.6. System Management (SM) Bus

The 8-bit SMBus address uses the LSB (Bit 0) for the direction of the device.

- Bit0 = 0 defines the write address
- Bit0 = 1 defines the read address

The 8-bit address listed below shows the write address for all devices. The7-bit SMBus address shows the device address without bit0.

Table 23: SMBus Address

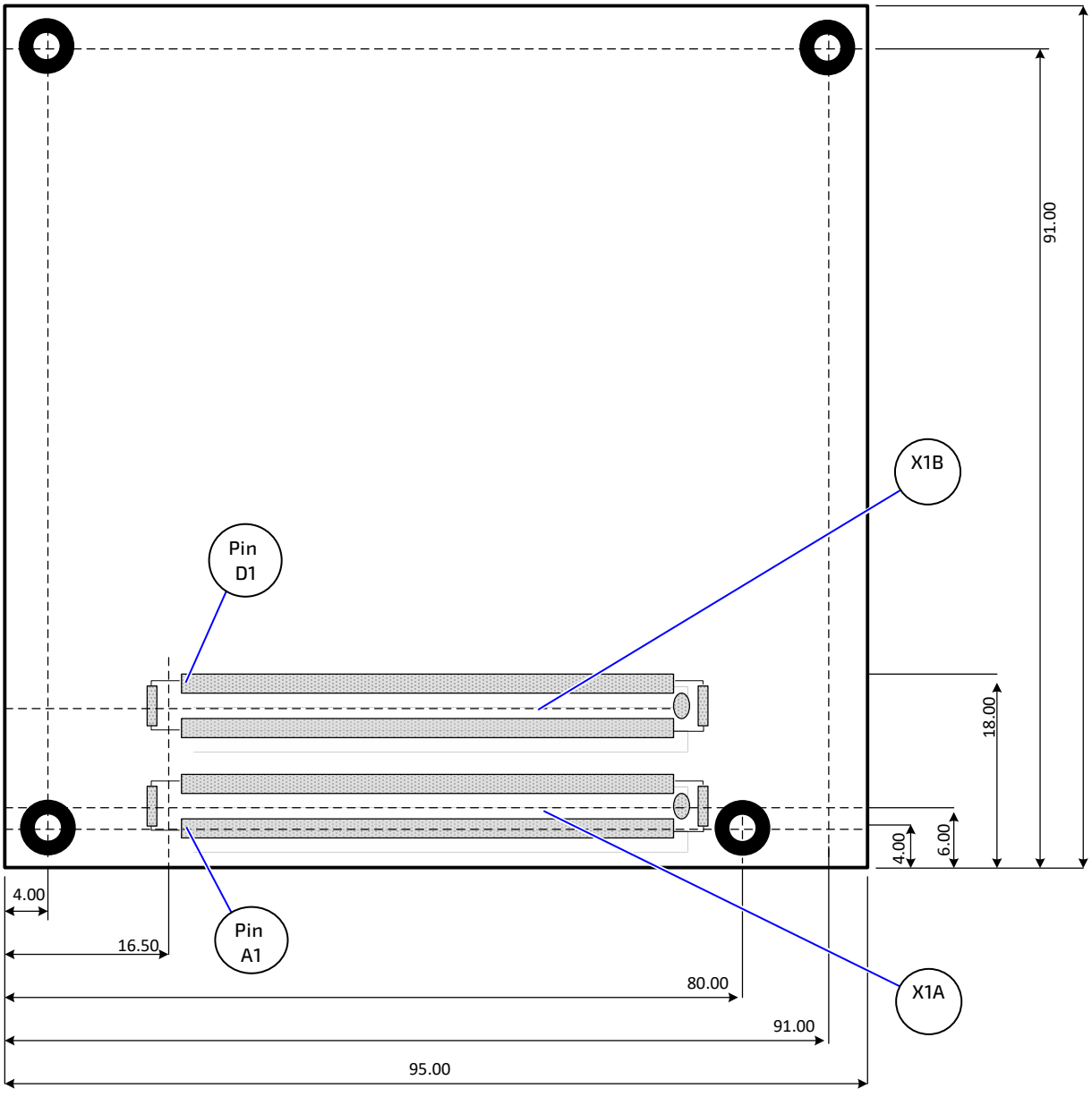
8-bit Address	7-bit Address	Device	Comment	SMBus
5Ch	2Eh	HWM NCT7802Y	Do not use under any circumstances	SMB
ACh	56h	Intenally Reserved	Do not use under any circumstances	SMB
A0h	50h	SPD DDR Channel 1 (SO-DIMM)		SMB
A2h	51h	SPD DDR Channel 2 (SO-DIMM)		SMB
30h	18h	SO-DIMM Thermal Sensor	If available on the used memory-module	SMB
32h	19h	SO-DIMM Thermal Sensor channel 2	If available on the used memory-module	SMB

5/ COMe Interface Connectors

The COMe-cAL6 is a COM Express® compact module containing two 220-pin connectors; each with two rows called row A & B on primary connector and row C & D on secondary connector.

The two interface connectors X1A and X1B are mounted on the rear side of the module, see Figure 7, a view from the top side of the module through to the rear side, showing the position of the connectors X1A and X1B on the rear side.

Figure 7: X1A and X1B COMe Interface Connectors



*All dimensions in mm.

5.1. X1A and X1B Signals

For a description of the terms used in the X1A and X1B pin assignment tables, see Table 24: General Signal Description or see Table 38: List of Acronyms. If a more detailed pin assignment description is required, refer to the PICMG specification COMe Rev 2.1 Type 6 standard.

The information provided under type, module terminations and comments is complimentary to the COM.0 Rev 2.1 Type 6 standard. For more information, contact Kontron Support.

Table 24: General Signal Description

Type	Description	Type	Description
NC	Not Connected (on this product)	O-1,8	1.8 V Output
I/O-3,3	Bi-directional 3.3 V I/O-Signal	O-3,3	3.3 V Output
I/O-5T	Bi-dir. 3.3 V I/O (5 V tolerance)	O-5	5 V Output
I/O-5	Bi-directional 5V I/O-Signal	DP-I/O	Differential Pair Input/Output
I-3,3	3.3 V Input	DP-I	Differential Pair Input
I/OD	Bi-directional Input/Output Open Drain	DP-O	Differential Pair Output
I-5T	3.3 V Input (5 V tolerance)	PU	Pull-Up Resistor
OA	Output Analog	PWR	Power Connection
OD	Output Open Drain	+ and -	Differential Pair Differentiator

NOTICE

To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current.

The enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN60950.

5.2. X1A and X1B Pin Assignment

For more information regarding the pin assignment of connector X1A (Row A and Row B) and connector X1B (Row C and Row D), see the pin assignment tables listed below:

- Table 25: Connector X1A Row A Pin Assignment (A1-A110)
- Table 26: Connector X1A Row B Pin Assignment (B1 -B110)
- Table 27: Connector X1B Row C Pin Assignment (C1 -C110)
- Table 28: Connector X1B Row D Pin Assignment (D1 -D110)

5.2.1. Connector X1A Row A1 – A110

Table 25: Connector X1A Row A Pin Assignment (A1-A110)

Pin	COMe Signal	Description	Type	Termination	Comment
A1	GND	Power ground	PWR GND		
A2	GBE0_MDI3-	Ethernet media dependent interface 3	DP-I/O		
A3	GBE0_MDI3+				
A4	GBE0_LINK100#	Ethernet controller speed indicator	OD		
A5	GBE0_LINK1000#				
A6	GBE0_MDI2-	Ethernet media dependent Interface 2	DP-I/O		
A7	GBE0_MDI2+				
A8	GBE0_LINK#	Ethernet controller link indicator	OD		
A9	GBE0_MDI1-	Ethernet media dependent interface 1	DP-I/O		
A10	GBE0_MDI1+				
A11	GND	Power ground	PWR GND		
A12	GBE0_MDI0-	Ethernet media dependent interface 0	DP-I/O		
A13	GBE0_MDI0+				
A14	GBE0_CTREF	Reference voltage for Carrier Board Ethernet magnetics center tab. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V.	O		100 nF capacitor to GND
A15	SUS_S3#	Indicates system is in Suspend to RAM (or deeper) state. An inverted copy of SUS_S3# on Carrier Board may be used to enable non-standby power on a typical ATX supply.	O-3.3	PD 10 KΩ	
A16	SATA0_TX+	Serial ATA transmit data pair 0	DP-O		
A17	SATA0_TX-				
A18	SUS_S4#	Indicates system is in Suspend to Disk state.	O-3.3	PD 10 KΩ	
A19	SATA0_RX+	Serial ATA receive data pair 0	DP-I		
A20	SATA0_RX-				
A21	GND	Power ground	PWR GND		
A22	SATA2_TX+	NC	NC		
A23	SATA2_TX-	NC	NC		
A24	SUS_S5#	Indicates system is in Soft Off state.	O-3.3		
A25	SATA2_RX+	NC	NC		
A26	SATA2_RX-	NC	NC		
A27	BATLOW#	Provides a battery-low signal to the module to indicate external battery is low	I-3.3	PU 10 KΩ, 3.3 V (S5)	Assertion prevents wake from S3-S5 state
A28	ATA_ACT#	Serial ATA activity LED indicator	OD-3.3	PU 10 KΩ, 3.3 V (S0)	Can sink 15 mA
A29	HDA_SYNC	HD audio sync	O-3.3		
A30	HDA_RST#	HD audio reset	O-3.3		
A31	GND	Power ground	PWR GND		
A32	HDA_CLK	HD audio bit clock output	O-3.3		
A33	HDA_SDOUT	HD audio serial data out	O-3.3		
A34	BIOS_DIS0#	BIOS selection strap 0 to determine the BIOS boot device	I-3.3	PU 10 KΩ, 3.3 V (S5)	
A35	THRMTRIP#	Thermal trip Indicates CPU has entered thermal shutdown	O-3.3	PU 10 KΩ, 3.3 V (S0)	Thermal trip event transition to S5 indicator
A36	USB6-	USB 2.0 data differential pair port 6	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5 kΩ ±5% on upsteam facing port
A37	USB6+				
A38	USB_6_7_OC#	USB overcurrent indicator port 6/7	I-3.3	PU 10 KΩ, 3.3 V (S5)	

Pin	COMe Signal	Description	Type	Termination	Comment
A39	USB4-	USB 2.0 data differential pair port 4	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5 kΩ ±5% on upsteam facing port
A40	USB4+				
A41	GND	Power ground	PWR GND		
A42	USB2-	USB 2.0 data differential pair port 2	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5 kΩ ±5% on upsteam facing port
A43	USB2+				
A44	USB_2_3_OC#	USB overcurrent indicator port 2/3	I-3.3	PU 10 KΩ 3.3V (S5)	
A45	USB0-	USB data differential pairs port 0	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5KΩ ±5% on upsteam facing port
A46	USB0+				
A47	VCC_RTC	Real Time Clock (RTC) circuit power input	PWR 3V		Voltage range 2.8 V to 3.47 V
A48	EXCD0_PERST#	PCI ExpressCard reset port 0	O-3.3	PD 10 KΩ	
A49	EXCD0_CPPE#	PCI ExpressCard capable card request port 0	I-3.3	PU 10 KΩ 3.3 V (S0)	
A50	LPC_SERIRQ	Serial interrupt request	I/OD-3.3	PU 8.2 KΩ, 3.3 V (S0)	
A51	GND	Power ground	PWR GND		
A52	RSVD	Reserved for future use	NC		
A53	RSVD	Reserved for future use	NC		
A54	GPI0	General purpose input 0	I-3.3	PU 20 KΩ, 3.3 V (S0)	
A55	PCIE_TX4+	PCI Express lane 4 transmit	DP-O		
A56	PCIE_TX4-				
A57	GND	Power ground	PWR GND		
A58	PCIE_TX3+	PCI Express lane 3 transmit	DP-O		
A59	PCIE_TX3-				
A60	GND	Power Ground	PWR GND		
A61	PCIE_TX2+	PCI Express lane 2 transmit	DP-O		
A62	PCIE_TX2-				
A63	GPI1	General purpose input 1	I-3.3	PU 20 KΩ, 3.3V (S0)	
A64	PCIE_TX1+	PCI Express lane 1 transmit	DP-O		
A65	PCIE_TX1-				
A66	GND	Power ground	PWR GND		
A67	GPI2	General purpose input 2	I-3.3	PU 20 KΩ, 3.3V (S0)	
A68	PCIE_TX0+	PCI Express lane 0 transmit	DP-O		
A69	PCIE_TX0-				
A70	GND	Power ground	PWR GND		
A71	LVDS_A0+	LVDS channel A DAT0 or EDP Lane 2 transmit	DP-O		
A72	LVDS_A0-				
A73	LVDS_A1+	LVDS channel A DAT1 or EDP Lane 1 transmit	DP-O		
A74	LVDS_A1-				
A75	LVDS_A2+	LVDS channel A DAT2 or EDP Lane 0 transmit	DP-O		
A76	LVDS_A2-				
A77	LVDS_VDD_EN	LVDS or EDP panel power control	O-3.3	PD 100 KΩ	
A78	LVDS_A3+	LVDS channel A DAT3	DP-O		
A79	LVDS_A3-				
A80	GND	Power ground	PWR GND		

Pin	COMe Signal	Description	Type	Termination	Comment
A81	LVDS_A_CK+	LVDS Channel A clock or EDP lane 3 transmit	DP-O		Clock 20 MHz to 80 MHz
A82	LVDS_A_CK-				
A83	LVDS_I2C_CK	I2C Clock for LVDS display (DDC) or eDP AUX +	I/O-3.3	PU 2.2 KΩ, 3.3V (S0)	
A84	LVDS_I2C_DAT	I2C Data line for LVDS display (DDC) or eDP AUX -	I/O-3.3	PU 2.2 KΩ, 3.3V (S0)	
A85	GPI3	General purpose input 3	I-3.3	PU 20 KΩ 3.3V (S0)	
A86	RSVD	Reserved for future use	NC		
A87	eDP_HPD	Detection of Hot Plug / unplug	I-3.3	100 KΩ EDP	
A88	PCIE_CK_REF+	Reference PCI Express clock for all PCI Express and PCI Express graphics lanes	DP-O		100 MHz
A89	PCIE_CK_REF-				
A90	GND	Power ground	PWR GND		
A91	SPI_POWER	3.3 V power output for external SPI Flash	O-3.3		100 mA maximum
A92	SPI_MISO	Data in to module from carrier SPI (SPI Master IN Slave Out)	I-3.3		.
A93	GPO0	General purpose output 0	O-3.3	PD 20k	
A94	SPI_CLK	Clock from module to carrier SPI	O-3.3		
A95	SPI_MOSI	Data out from module to carrier SPI	O-3.3		
A96	TPM_PP	TPM physical presence	I-3.3	PD 10KΩ	TMP does not use this functionality.
A97	TYPE10#	NC	NC		
A98	SER0_TX	Serial port 0 TXD	O-3.3		20 V protection circuit implemented on-module, PD on carrier board needed for proper operation.
A99	SER0_RX	Serial port 0 RXD	I-5T	PU 47 KΩ, 3.3V (S0)	20 V protection circuit implemented on-module.
A100	GND	Power ground	PWR GND		
A101	SER1_TX	Serial port 1 TXD	O-3.3		20 V protection circuit implemented on-module, PD on carrier board needed for proper operation.
A102	SER1_RX	Serial port 1 RXD	I-5T	PU 47 KΩ, 3.3 V (S0)	20 V protection circuit implemented on-module.
A103	LID#	LID switch input	I-3.3	PU 47 KΩ, 3.3 V (S5)	
A104	VCC_12V	Main input voltage (8.5 V - 20V)	PWR 8.5 V to 20 V		
A105	VCC_12V				
A106	VCC_12V				
A107	VCC_12V				
A108	VCC_12V				
A109	VCC_12V				
A110	GND	Power ground	PWR GND		

+ and - Differential pair differentiator

5.2.2. Connector X1A Row B 1 - B 110

Table 26: Connector X1A Row B Pin Assignment (B1 -B110)

Pin	COMe Signal	Description	Type	Termination	Comment
B1	GND	Power ground	PWR GND		
B2	GBE0_ACT#	Gigabit Ethernet Controller activity LED indicator	OD		
B3	LPC_FRAME#	Indicates the start of an LPC cycle	O-3.3		
B4	LPC_AD0	LPC multiplexed command, address and data	I/O-3.3		
B5	LPC_AD1				
B6	LPC_AD2				
B7	LPC_AD3				
B8	LPC_DRQ0#	NC	NC		Not supported on Apollo Lake SoC
B9	LPC_DRQ1#	NC	NC		
B10	LPC_CLK	LPC 24 MHz clock output	O-3.3	PD 20 KΩ in Soc	25 MHz
B11	GND	Power ground	PWR GND		
B12	PWRBTN#	Power Button - a falling edge creates a power button event	I-3.3	PU 10 KΩ, 3.3 V (S5eco)	
B13	SMB_CLK	SMBus clock line	O-3.3	PU 2.56 KΩ, 3.3 V (S5)	
B14	SMB_DAT	SMBus bidirectional data line	I/O-3.3	PU 2.56 KΩ, 3.3 V (S5)	
B15	SMB_ALERT#	SMBus alert can be used to generate a SMI# or to wake the system	I/O-3.3	PU 2.2 KΩ, 3.3 V (S5)	
B16	SATA1_TX+	Serial ATA transmit data pair	DP-O		
B17	SATA1_TX-				
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices.	O-3.3		
B19	SATA1_RX+	Serial ATA receive data pair 1	DP-I		
B20	SATA1_RX-				
B21	GND	Power ground	PWR GND		
B22	SATA3_TX+	NC	NC		
B23	SATA3_TX-	NC	NC		
B24	PWR_OK	Power OK from main power supply.	I-5T	PU 61 KΩ, 3.3 V	20 V protection circuit implemented on module
B25	SATA3_RX+	NC	NC		
B26	SATA3_RX-	NC	NC		
B27	WDT	Watchdog time-out event has occurred	O-3.3	PD 10 KΩ	
B28	HDA_SDIN2	NC	NC		Not supported on Apollo Lake SoC
B29	HDA_SDIN1	NC	NC		
B30	HDA_SDIN0	Audio Codec Serial data input 0	I-3.3		
B31	GND	Power ground	PWR GND		
B32	SPKR	Speaker output provides the PC beep signal and is mainly intended for debugging purposes	O-3.3		
B33	I2C_CK	General purpose I2C port clock output	O-3.3	PU 2.21 KΩ, 3.3 V (S5)	
B34	I2C_DAT	General purpose I2C port data I/O line	I/O-3.3	PU 2.21 KΩ, 3.3 V (S5)	
B35	THRM#	Input from off-Module temp sensor indicating an over-temp situation	I-3.3	PU 10 KΩ to 3.3 V (S0)	No function implemented
B36	USB7-	USB 2.0 differential data pairs port 7	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5KΩ ±5% on upsteam facing port
B37	USB7+				

Pin	COMe Signal	Description	Type	Termination	Comment
B38	USB_4_5_OC#	USB overcurrent indicator port 4/5	I-3.3	PU 10 KΩ, 3.3 V (S5)	
B39	USB5-	USB 2.0 differential data pairs port 5	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5KΩ ±5% on upsteam facing port
B40	USB5+				
B41	GND	Power ground	PWR GND		
B42	USB3-	USB 2.0 differential data pairs port 3	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5KΩ ±5% on upsteam facing port
B43	USB3+				
B44	USB_0_1_OC#	USB overcurrent indicator port 0/1	I-3.3	PU 10 KΩ, 3.3 V (S5)	
B45	USB1-	USB 2.0 differential data pairs port	DP-I/O	PD/PU in SoC	PD 15 kΩ ±5% on downstream facing port; PU 1.5KΩ ±5% on upsteam facing port
B46	USB1+				
B47	EXCD1_PERST#	PCI ExpressCard expansion, reset port 1	O-3.3	PD 10 KΩ	
B48	EXCD1_CPPE#	PCI ExpressCard expansion, capable card request port 1	I-3.3	PU 10KΩ, 3.3 V (S0)	
B49	SYS_RESET#	Reset button input	I-3.3	PU 3.48 KΩ, 3.3 V (S5)	
B50	CB_RESET#	Reset output from module to carrier board	O-3.3		
B51	GND	Power ground	PWR GND		
B52	PCIE_RX5+	Reserved for future use	NC		
B53	PCIE_RX5-	Reserved for future use	NC		
B54	GPO1	General Purpose Output 1	O-3.3	PD 20 KΩ	
B55	PCIE_RX4+	PCI Express receive lane 4	DP-I		
B56	PCIE_RX4-				
B57	GPO2	General Purpose Output 2	O-3.3	PD 20 KΩ	
B58	PCIE_RX3+	PCI Express receive lane 3	DP-I		
B59	PCIE_RX3-				
B60	GND	Power ground	PWR GND		
B61	PCIE_RX2+	PCI Express receive lane 2	DP-I		
B62	PCIE_RX2-				
B63	GPO3	General Purpose Output 3	O-3.3	PD 20 KΩ	
B64	PCIE_RX1+	PCI Express receive lane 1	DP-I		
B65	PCIE_RX1-				
B66	WAKE0#	PCI Express Wake Event wake up signal	I-3.3	PU 10 KΩ, 3.3 V (S5)	
B67	WAKE1#	General purpose Wake Event wake up signal, to implement wake-up on PS2 keyboard or mouse	I-3.3	PU 10 KΩ, 3.3 V (S5)	
B68	PCIE_RX0+	PCI Express receive lane 0	DP-I		
B69	PCIE_RX0-				
B70	GND	Power ground	PWR GND		
B71	LVDS_B0+	LVDS Channel B data pair 0	DP-O		
B72	LVDS_B0-				
B73	LVDS_B1+	LVDS Channel B data pair 1	DP-O		
B74	LVDS_B1-				
B75	LVDS_B2+	LVDS Channel B data pair 2	DP-O		
B76	LVDS_B2-				
B77	LVDS_B3+	LVDS Channel B data pair 3	DP-O		
B78	LVDS_B3-				
B79	LVDS/BKLT_EN	LVDS or EDP panel backlight enable (ON)	O-3.3	PD 100 KΩ	
B80	GND	Power ground	PWR GND		

Pin	COMe Signal	Description	Type	Termination	Comment
B81	LVDS_B_CK+	LVDS Channel B Clock	DP-O		20 MHz -80 MHz
B82	LVDS_B_CK-				
B83	LVDS_BKLT_CTRL	LVDS or EDP panel backlight brightness control	O-3.3		
B84	VCC_5V_SBY	5 V Standby	PWR 5 V (S5)		Optional, not necessary in single supply mode
B85	VCC_5V_SBY				
B86	VCC_5V_SBY				
B87	VCC_5V_SBY				
B88	BIOS_DIS1#	BIOS selection strap 1 to determine BIOS boot device	I-3.3	PU 10 KΩ, 3.3 V (S5)	
B89	VGA_RED	NC	NC		Not supported on Apollo Lake SoC
B90	GND	Power ground	PWR GND		
B91	VGA_GREEN	NC	NC		Not supported on Apollo Lake SoC
B92	VGA_BLUE	NC	NC		
B93	VGA_HSYNC	NC	NC		
B94	VGA_VSYNC	NC	NC		Optional connection to USB2_OTG_ID
B95	VGA_DDC_CLK	NC	NC		Not supported on Apollo Lake SoC
B96	VGA_DCC_DATA	NC	NC	PD 10KΩ (optional)	Optional connection to USB2_VBUS_SNS
B97	SPI_CS#	Chip select for carrier board SPI	O 3.3		
B98	RSVD	Reserved for future use	NC		
B99	RSVD				
B100	GND	Power ground	PWR GND		
B101	FAN_PWMOUT	Fan speed control by PWM Output	O-3.3		20 V protection circuit implemented on module, PD on carrier board needed for proper operation Default frequency of PWM signal is 25kHz.
B102	FAN_TACHIN	Fan tachometer input for fan with a two-pulse output	I-3.3	PU 47 KΩ, 3.3 V (S0)	20 V protection circuit implemented on module
B103	SLEEP#	Sleep button signal used by ACPI operating system to bring system to sleep state or wake system up again	I-3.3	PU 47 KΩ, 3.3 V (S5)	
B104	VCC_12V	Main input voltage (8.5 V - 20 V)	PWR 8.5 V- 20 V		
B105	VCC_12V				
B106	VCC_12V				
B107	VCC_12V				
B108	VCC_12V				
B109	VCC_12V				
B110	GND	Power ground	PWR GND		

+ and - Differential pair differentiator

5.2.3. Connector X1B Row C 1 - C 110

Table 27: Connector X1B Row C Pin Assignment (C1 -C110)

Pin	COMe Signal	Description	Type	Termination	Comment
C1	GND	Power ground	PWR GND		
C2	GND				
C3	USB_SSRX0-	USB SuperSpeed receive data pair 0	DP-I		
C4	USB_SSRX0+				
C5	GND	Power ground	PWR GND		
C6	USB_SSRX1-	USB SuperSpeed receive data pair 1	DP-I		
C7	USB_SSRX1+				
C8	GND	Power ground	PWR GND		
C9	USB_SSRX2-	USB SuperSpeed receive data pair 2	DP-I		
C10	USB_SSRX2+				
C11	GND	Power ground	PWR GND		
C12	USB_SSRX3-	USB SuperSpeed receive data pair 3	DP-I		
C13	USB_SSRX3+				
C14	GND	Power ground	PWR GND		
C15	DDI1_PAIR6+	NC	NC		
C16	DDI1_PAIR6-	NC	NC		
C17	RSVD	Reserved for future use	NC		
C18	RSVD				
C19	PCIE_RX6+	NC	NC		
C20	PCIE_RX6-	NC	NC		
C21	GND	Power ground	PWR GND		
C22	PCIE_RX7+	NC	NC		
C23	PCIE_RX7-	NC	NC		
C24	DDI1_HPD	DDI1 Hotplug Detect	I-3.3	PD 100 KΩ	
C25	DDI1_PAIR4+	NC	NC		
C26	DDI1_PAIR4-	NC	NC		
C27	RSVD	Reserved for future use	NC		
C28	RSVD				
C29	DDI1_PAIR5+	NC	NC		
C30	DDI1_PAIR5-	NC	NC		
C31	GND	Power ground	PWR GND		
C32	DDI2_CTRLCLK_AUX+	DDI2 clock/Auxilary	I/O-3.3	PD 100 KΩ	
C33	DDI2_CTRLDATA_AUX-	DDI2 date/Auxilary	I/O-3.3	PD 100 KΩ, 3.3 V (S0)	
C34	DDI2_DDC_AUX_SEL	DDI2 /Auxilary select	I-3.3	PD 1 MΩ	
C35	RSVD	Reserved for future use	NC		
C36	DDI3_CTRLCLK_AUX+	NC	NC		
C37	DDI3_CTRLDATA_AUX-	NC	NC		
C38	DDI3_DDC_AUX_SEL	NC	NC		
C39	DDI3_PAIR0+	NC	NC		
C40	DDI3_PAIR0-	NC	NC		
C41	GND	Power ground	PWR GND		
C42	DDI3_PAIR1+	NC	NC		
C43	DDI3_PAIR1-	NC	NC		
C44	DDI3_HPD	NC	NC		
C45	RSVD	Reserved for future use	NC		
C46	DDI3_PAIR2+	NC	NC		
C47	DDI3_PAIR2-	NC	NC		

Pin	COMe Signal	Description	Type	Termination	Comment
C48	RSVD	Reserved for future use	NC		
C49	DDI3_PAIR3+	NC	NC		
C50	DDI3_PAIR3-	NC	NC		
C51	GND	Power Ground	PWR GND		
C52	PEG_RX0+	NC	NC		Optional connection to MCSI_DP0_+ (MCSI data lane 0 D_PHY1.1
C53	PEG_RX0-	NC	NC		Optional connection to MCSI_DP0_- (MCSI data lane 0 D_PHY1.1
C54	TYPE0#	Indicates the Carrier Board the pinout Type. Not connected for Type 6.	NC		NC for Type 6 module
C55	PEG_RX1+	NC	NC		Optional connection to MCSI_DP1_+ (MCSI data lane 1 D_PHY1.1
C56	PEG_RX1-	NC	NC		Optional connection to MCSI_DP1_- (MCSI data lane 1 D_PHY1.1
C57	TYPE1#	Indicates the Carrier Board the pinout Type. Not connected for Type 6.	NC		NC for Type 6 module
C58	PEG_RX2+	NC	NC		Optional connection to MCSI_DP2_+ (MCSI data lane 2 D_PHY1.1
C59	PEG_RX2-	NC	NC		Optional connection to MCSI_DP2_- (MCSI data lane 2 D_PHY1.1
C60	GND	Power ground	PWR GND		
C61	PEG_RX3+	NC	NC		Optional connection to MCSI_DP3_+ (MCSI data lane 3 D_PHY1.1
C62	PEG_RX3-	NC	NC		Optional connection to MCSI_DP3_- (MCSI data lane 3 D_PHY1.1
C63	RSVD	Reserved for future use	NC		
C64	RSVD				
C65	PEG_RX4+	NC	NC		Optional connection to MCSI_RX_DATA0_+ (MCSI data lane 0 D_PHY1.2
C66	PEG_RX4-	NC	NC		Optional connection to MCSI_RX_DATA0_- (MCSI data lane 0 D_PHY1.2
C67	RSVD	Reserved for future use	NC		
C68	PEG_RX5+	NC	NC		Optional connection to MCSI_RX_DATA1_+ (MCSI data lane 1 D_PHY1.2
C69	PEG_RX5-	NC	NC		Optional connection to MCSI_RX_DATA1_- (MCSI data lane 1 D_PHY1.2
C70	GND	Power ground	PWR GND		
C71	PEG_RX6+	NC	NC		Optional connection to MCSI_RX_DATA2_+ (MCSI data lane 2 D_PHY1.2
C72	PEG_RX6-	NC	NC		Optional connection to MCSI_RX_DATA2_- (MCSI data lane 2 D_PHY1.2
C73	GND	Power ground	PWR GND		
C74	PEG_RX7+	NC	NC		Optional connection to MCSI_RX_DATA3_+ (MCSI data lane 3 D_PHY1.2

Pin	COMe Signal	Description	Type	Termination	Comment
C75	PEG_RX7-	NC	NC		Optional connection to MCSI_RX_DATA3_- (MCSI data lane 3 D_PHY1.2
C76	GND	Power ground	PWR GND		
C77	RSVD	Reserved for future use	NC		
C78	PEG_RX8+	NC	NC		
C79	PEG_RX8-	NC	NC		-
C80	GND	Power ground	PWR GND		
C81	PEG_RX9+	NC	NC		
C82	PEG_RX9-	NC	NC		
C83	RSVD	Reserved for future use	NC		
C84	GND	Power ground	PWR GND		
C85	PEG_RX10+	NC	NC		
C86	PEG_RX10-	NC	NC		
C87	GND	Power ground	PWR GND		
C88	PEG_RX11+	NC	NC		
C89	PEG_RX11-	NC	NC		
C90	GND	Power ground	PWR GND		
C91	PEG_RX12+	NC	NC		Optional connection to: CSI2_I2C1_SDA
C92	PEG_RX12-	NC	NC		Optional connect to: CSI2__I2C1_SCL
C93	GND	Power ground	PWR GND		
C94	PEG_RX13+	NC	NC		Optional connection to: GP_CAMERASB8 (MIPI camera sideband signal)
C95	PEG_RX13-	NC	NC		Optional connection to: GP_CAMERASB9 (MIPI camera sideband signal)
C96	GND	Power ground	PWR GND		
C97	RSVD	Reserved for future use	NC		
C98	PEG_RX14+	NC	NC		Optional connection to: GP_CAMERASB10 (MIPI camera sideband signal
C99	PEG_RX14-	NC	NC		Optional connection to: GP_CAMERASB11 (MIPI camera sideband signal
C100	GND	Power ground	PWR GND		
C101	PEG_RX15+	NC	NC		Optional connection to: CSI2_I2C2_SDA
C102	PEG_RX15-	NC	NC		Optional connect to: CSI2__I2C2_SCL
C103	GND	Power ground	PWR GND		
C104	VCC_12V	Main input voltage (8.5 V - 20 V)	PWR 8.5 V-to 20 V		
C105	VCC_12V				
C106	VCC_12V				
C107	VCC_12V				
C108	VCC_12V				
C109	VCC_12V				
C110	GND	Power ground	PWR GND		

+ and - Differential pair differentiator

5.2.4. Connector X1B Row D 1 - D 110

Table 28: Connector X1B Row D Pin Assignment (D1 -D110)

Pin	COMe Signal	Description	Type	Termination	Comment
D1	GND	Power ground	PWR GND		
D2	GND				
D3	USB_SSTX0-	USB SuperSpeed transmit data path 0	DP-O		
D4	USB_SSTX0+				
D5	GND	Power ground	PWR GND		
D6	USB_SSTX1-	USB SuperSpeed transmit data path 1	DP-O		
D7	USB_SSTX1+				
D8	GND	Power ground	PWR GND		
D9	USB_SSTX2-	USB SuperSpeed transmit data path 2	DP-O		
D10	USB_SSTX2+				
D11	GND	Power Ground	PWR GND		
D12	USB_SSTX3-	USB SuperSpeed transmit data path 3	DP-O		
D13	USB_SSTX3+				
D14	GND	Power Ground	PWR GND		
D15	DDI1_CTRLCLK_AUX+	DDI1 clock / Auxilary	I/O-3.3	PD 100 KΩ	
D16	DDI1_CTRLDATA_AUX-	DDI1 date / Auxilary	I/O-3.3	PU 100 KΩ, 3.3 V (S0)	
D17	RSVD	Reserved for future use	NC		
D18	RSVD				
D19	PCIE_TX6+	NC	NC		
D20	PCIE_TX6-	NC	NC		
D21	GND	Power Ground	PWR GND		
D22	PCIE_TX7+	NC	NC		
D23	PCIE_TX7-	NC	NC		
D24	RSVD	Reserved for future use	NC		
D25	RSVD				
D26	DDI1_PAIR0+	DDI1 pair 0	DP-O		
D27	DDI1_PAIR0-				
D28	RSVD	Reserved for future use	NC		
D29	DDI1_PAIR1+	DDI1 pair 1	DP-O		
D30	DDI1_PAIR1-				
D31	GND	Power ground	PWR GND		
D32	DDI1_PAIR2+	DDI1 pair 2	DP-O		
D33	DDI1_PAIR2-				
D34	DDI1_DDC_AUX_SEL	DDI1 DCC / Auxilary select	I-3.3	PD 1 MΩ	
D35	RSVD	Reserved for future use	NC		
D36	DDI1_PAIR3+	DDI1 pair 3	DP-O		
D37	DDI1_PAIR3-				
D38	RSVD	Reserved for future use	NC		
D39	DDI2_PAIR0+	DDI2 pair 0	DP-O		
D40	DDI2_PAIR0-				
D41	GND	Power ground	PWR GND		
D42	DDI2_PAIR1+	DDI2 pair 1	DP-O		
D43	DDI2_PAIR1-				
D44	DDI2_HPD	DDI2 Hotplug Detect	I-3.3	PD 100 KΩ	
D45	RSVD	Reserved for future use	NC		
D46	DDI2_PAIR2+	DDI2 pair 2	DP-O		
D47	DDI2_PAIR2-				

Pin	COMe Signal	Description	Type	Termination	Comment
D48	RSVD	Reserved for future use	NC		
D49	DDI2_PAIR3+	DDI2 pair 3	DP-0		
D50	DDI2_PAIR3-				
D51	GND	Power ground	PWR GND		
D52	PEG_TX0+	NC	NC		Optional connection to MCSI_CLK0+(MCSI clock 0 D_PHY1.1)
D53	PEG_TX0-	NC	NC		Optional connection to MCSI_CLK0-(MCSI clock 0 D_PHY1.1)
D54	PEG_LANE_RV#	PCI Express Graphics (PEG) Lane Reversal	NC		
D55	PEG_TX1+	NC	NC		Optional connection to MCSI_CLK0
D56	PEG_TX1-	NC	NC		
D57	TYPE2#	Ground for Type 6 modules	GND		GND for Type 6 module
D58	PEG_TX2+	NC	NC		Optional connection to MCSI_CLK1
D59	PEG_TX2-	NC	NC		
D60	GND	Power ground	PWR GND		
D61	PEG_TX3+	NC	NC		
D62	PEG_TX3-				-
D63	RSVD	Reserved for future use	NC		
D64	RSVD				
D65	PEG_TX4+	NC	NC		Optional connection to MCSI_CLK2+(MCSI clock 2 D_PHY1.1)
D66	PEG_TX4-	NC	NC		Optional connection to MCSI_CLK2-(MCSI clock 2 D_PHY1.1)
D67	GND	Power ground	PWR GND		
D68	PEG_TX5+	NC	NC		
D69	PEG_TX5-	NC	NC		
D70	GND	Power ground	PWR GND		
D71	PEG_TX6+	NC	NC		
D72	PEG_TX6-	NC	NC		
D73	GND	Power ground	PWR GND		
D74	PEG_TX7+	NC	NC		Optional connection to CSI2_I2C3_SDA
D75	PEG_TX7-	NC	NC		Optional connection to CSI2_I2C3_SCL
D76	GND	Power ground	PWR GND		
D77	RSVD	Reserved for future use	NC		
D78	PEG_TX8+	NC	NC		Optional connection to MCSI_RX_CLK0+(MCSI clock 0 D_PHY1.2)
D79	PEG_TX8-	NC	NC		Optional connection to MCSI_RX_CLK0-(MCSI clock 0 D_PHY1.2)
D80	GND	Power ground	PWR GND		
D81	PEG_TX9+	NC	NC		Optional connection to: GP_CAMERASB0 (MIPI camera sideband signal)
D82	PEG_TX9-	NC	NC		Optional connection to: GP_CAMERASB1 (MIPI camera sideband signal)
D83	RSVD	Reserved for future use	NC		

Pin	COMe Signal	Description	Type	Termination	Comment
D84	GND	Power ground	PWR GND		
D85	PEG_TX10+	NC	NC		Optional connection to: GP_CAMERASB2 (MIPI camera sideband signal)
D86	PEG_TX10-	NC	NC		Optional connection to: GP_CAMERASB3 (MIPI camera sideband signal)
D87	GND	Power ground	PWR GND		
D88	PEG_TX11+	NC	NC		Optional connection to MCSI_RX_CLK1_+ (MCSI clock 1 D_PHY1.2)
D89	PEG_TX11-	NC	NC		Optional connection to MCSI_RX_CLK1_- (MCSI clock 1 D_PHY1.2)
D90	GND	Power ground	PWR GND		
D91	PEG_TX12+	NC	NC		Optional connection to: CSI2_I2C0_SDA
D92	PEG_TX12-	NC	NC		Optional connection to: CSI2_I2C0_SCL
D93	GND	Power ground	PWR GND		
D94	PEG_TX13+	NC	NC		Optional connection to: GP_CAMERASB4 (MIPI camera sideband signal)
D95	PEG_TX13-	NC	NC		Optional connection to: GP_CAMERASB5 (MIPI camera sideband signal)
D96	GND	Power ground	PWR GND		
D97	RSVD	Reserved for future use	NC		
D98	PEG_TX14+	NC	NC		Optional connection to: GP_CAMERASB6 (MIPI camera sideband signal)
D99	PEG_TX14-	NC	NC		Optional connection to: GP_CAMERASB7 (MIPI camera sideband signal)
D100	GND	Power Ground	PWR GND		
D101	PEG_TX15+	NC	NC		
D102	PEG_TX15-	NC	NC		
D103	GND	Power ground	PWR GND		
D104	VCC_12V	Main input voltage (8.5 V - 20 V)	PWR 8.5 V-20V		
D105	VCC_12V				
D106	VCC_12V				
D107	VCC_12V				
D108	VCC_12V				
D109	VCC_12V				
D110	GND	Power ground	PWR GND		

+ and - Differential pair differentiator

6/ uEFI BIOS

6.1. Starting the uEFI BIOS

The COMe-cAL6 uses a Kontron-customized, pre-installed and configured version of Aptio® V uEFI BIOS based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the COMe-cAL6.

The BIOS version covered in this document might not be the latest version. The latest version might have certain differences to the BIOS options and features described in this chapter.

Register for the Kontron Customer Section to get access to BIOS downloads and PCN service.

The uEFI BIOS comes with a Setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows for access to various menus that provide functions or access to sub-menus with further specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Chapter 6.2.4: Security Setup Menu), press <RETURN>, and proceed with step 5.
5. A Setup menu appears.

The COMe-cAL6 uEFI BIOS Setup program uses a hot key navigation system. The hot key legend bar is located at the bottom of the Setup screens. The following table provides a list of navigation hot keys available in the legend bar.

Table 29: Navigation Hot Keys Available in the Legend Bar

Sub-screen	Description
<F1>	<F1> key invokes the General Help window
<->	<Minus> key selects the next lower value within a field
<+>	<Plus> key selects the next higher value within a field
<F2>	<F2> key loads previous values
<F3>	<F3> key loads optimized defaults
<F4>	<F4> key Saves and Exits
<→> or <←>	<Left/Right> arrows selects major Setup menus on menu bar, for example, Main or Advanced
<↑> or <↓>	<Up/Down> arrows select fields in the current menu, for example, Setup function or sub-screen
<ESC>	<ESC> key exits a major Setup menu and enters the Exit Setup menu Pressing the <ESC> key in a sub-menu displays the next higher menu level
<RETURN>	<RETURN> key executes a command or selects a submenu

6.2. Setup Menus

The Setup utility features menus listed in the selection bar at the top of the screen The setup menus listed are:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

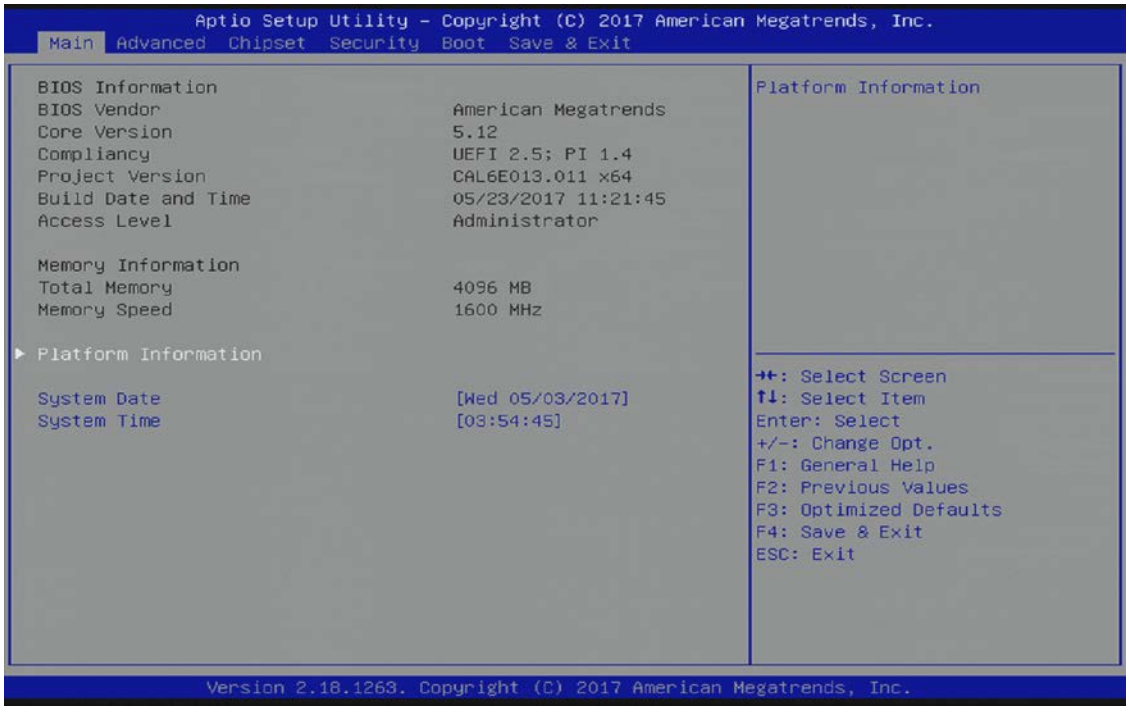
The currently active menu is highlighted in white. To change the Setup menu use the left and right arrow keys to select the required Setup menu.

Each Setup menu provides two main frames. The left frame displays all available functions. With configurable functions displayed in blue and functions displayed in grey that provide information about the status or the operational configuration. The right frame displays a Help window explaining about the respective function.

6.2.1. Main Setup Menu

On entering the uEFI BIOS, the setup program displays the Main Setup menu. This screen lists the Main Setup menu sub-screens and provides basic system information as well as functions for setting the system language, time and date.

Figure 8: Main Setup Menu Initial Screen



The following table shows the Main menu sub-screens and functions and describes the content.

Table 30: Main Setup Menu Sub-screens and Functions

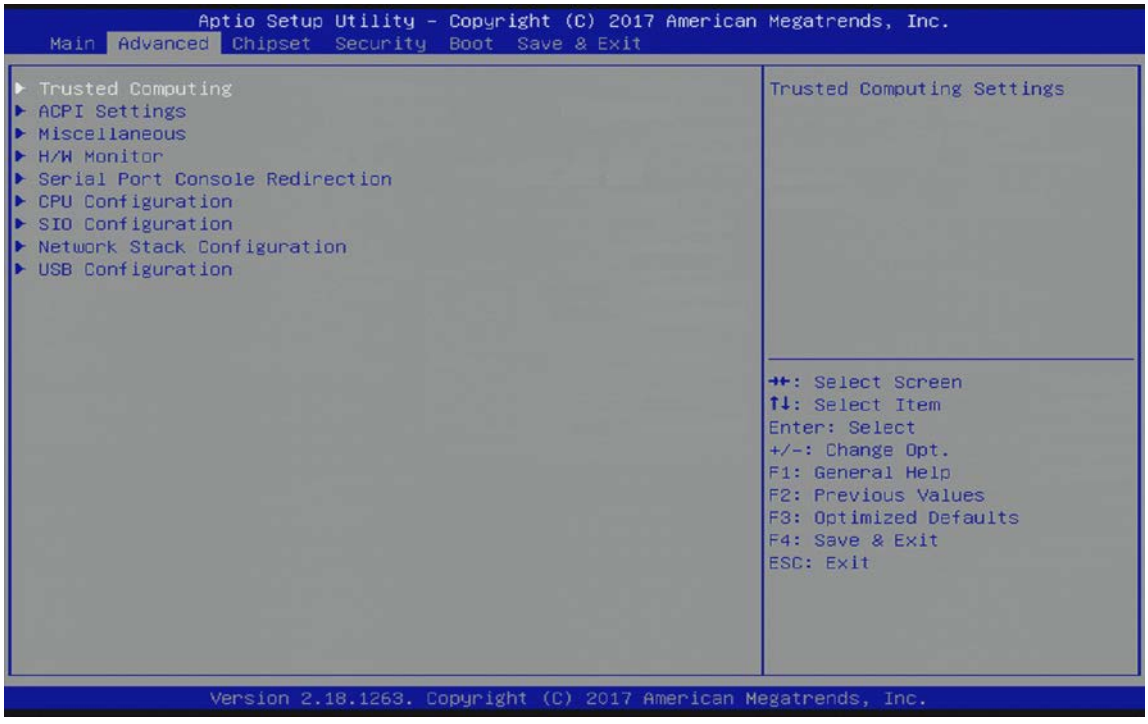
Sub-Screen	Description
BIOS Information>	Read only field BIOS vendor, Core version, Compliancy, Project version, Build date and time, and Access level
Memory Information>	Read only field Total memory and Memory speed
Platform Information>	Read only field Module Information Product name, Revision, Serial # ,MAC address, Boot counter, and CPLD rev
	Additional information for MAC Address The MAC address entry is the value used by the Ethernet controller and may contain the entry 'Inactive' - Ethernet chip is inactive. To activate the Ethernet chip set the following: Advanced > Network Stack Configuration > Network Stack > Enable 88:88:88:88:87:88 is a special pattern that will be filled in by the Ethernet firmware if there is no valid entry in the firmware block of the BIOS SPI (i.e. the MAC address has been overwritten during the last attempt to flash the system).
System Date>	Displays the system date [Week day mm/dd/yyyy]
System Time>	Displays the system time [hh:mm:ss]

6.2.2. Advanced Setup Menu

The Advanced Setup menu screen displays sub-screens and second level sub-screens with functions, for advanced configurations.

NOTICE Setting items, on this screen, to incorrect values may cause system malfunctions.

Figure 9: Advanced Setup Menu Initial Screen



The following table shows the Advanced sub-screens and functions and describes the content. Default settings are **bold**. Some functions include additional information.

Table 31: Advanced Setup menu Sub-screens and Functions

Sub-Screen	Function	Second level Sub-Screen / Description
Trusted Computing>	Read only Information TPM20 device, Vendor and Firmware version	
	Security Device Support>	Enables or disables BIOS support for security device Operating System will not show security device, and TCG EFI protocol and INT1A interface are not available. [**Enabled**, Disabled]
	Active PCR Banks>	Read only field Displays active PCR Banks
	Available PCR Banks>	Read only field Displays available PCR Banks
	SHA-1 PCR Bank>	SHA-1 PCR Bank [**Enabled**, Disabled]
	SHA256 PCR Bank>	SHA256 PCR Bank [**Enabled**, Disabled]

Sub-Screen	Function	Second level Sub-Screen / Description	
Trusted Computing> (continued)	Pending Operation>	Schedules an operation for security device Note: Computer reboots on restart to change the state of the security device. [**None**, TPM Clear]	
	Platform Hierarchy>	Platform Hierarchy [**Enabled**, Disabled]	
	Storage Hierarchy>	Storage Hierarchy [**Enabled**, Disabled]	
	Endorsement Hierarchy>	Endorsement Hierarchy [**Enabled**, Disabled]	
	TPM2.0 UEFI Spec. Version>	Selects TCG2 Spec Version support: TCG_1_2: Compatible mode for Win8/Win10 TCG_2: Supports TCG2 protocol and event format Win 10 or later. [TCG_1_2, **TCG_2**]	
	Physical Presence Spec Version>	Select to inform OS to support either PPI Spec 1.2 or 1.3 Note: Some HCK tests might not support 1.3. [1.2, **1.3**]	
	TPM 20 Interface Type>	Read only field	
	Device Select>	Selects BIOS support for security devices. Auto: Supports TPM 1.2 and TPM 2.0 with default set to TPM2.0 TPM 1.2: Restricts support to TPM 1.2 devices TPM 2.0: Restricts support to TPM 2.0 devices [TPM 1.2, TPM 2.0, **Auto**]	
ACPI Settings>	Enable ACPI Auto Configuration>	BIOS ACPI auto configuration. If enabled, the system uses generic ACPI settings that may not fit the system best. [Enabled, **Disabled**]	
	Enable Hibernation>	Enables or disables systems ability to hibernate (OS/S4 Sleep State) This option may not be effective with some operating systems. [**Enabled**, Disabled]	
	ACPI Sleep State>	Selects highest ACPI sleep state the system enters when SUSPEND button is pressed [Suspend Disabled, **S3 Suspend to Ram**]	
	Lock Legacy Resources>	Lock of legacy resources [Enabled, **Disabled**]	
Miscellaneous>	Watchdog>	Auto Reload>	Enables automatic reload of watchdog timers on timeout [Enabled, **Disabled**]
		Global Lock>	Sets all Watchdog registers (except for WD_KICK) to read only, until the module is reset. [Enabled, **Disabled**]
		Stage 1 Mode>	Selects action for Watchdog stage 1 [**Disable**, Reset, Delay, WDT Signal only]
	Additional Information two-staged watchdog Programmable stages to trigger different actions - If one stage is disabled, then the next stage is also disabled. Common actions for a watchdog trigger events are 'Delay', 'Reset' and 'Watchdog signal only'. Timeouts can be set to eight different fixed values between 1 second and 30 minutes.		

Sub-Screen	Function	Second level Sub-Screen / Description
Miscellaneous> (continued)	Reset Button Behavior>	Selects reset button behavior [**Chipset Reset**, Power Cycle]
	I2C Speed>	Selects internal I2C bus speed between (1 kHz and 400 kHz) For a default system 200 kHz is an appropriate value.
	On-board I2C Mode>	Keep 'Multimaster' setting unless otherwise noted [**MultiMaster**, BusClear]
	Manufacturing Mode>	Read only field Function is **disabled**
	LID Switch Mode>	Shows or hides Lid Switch Inside ACPI OS. [Enabled, **Disabled**]
	Sleep Button Mode>	Shows or hides Sleep Button inside ACPI OS. [Enabled, **Disabled**]
	MBus device ACPI Output>	Hides the SMBus device from OS if set to hidden. Otherwise, the device is visible in OS. [**Hidden**, Normal]
	CPLD device ACPI Mode>	Hides the CPLD device from OS if set to hidden. Otherwise the device is visible in OS. [**Hidden**, Normal]
H/W Monitor>	CPU Temperature>	Read only field CPU temperature (°C) and Module temperature (°C)
	Module Temperature>	Read only field Module temperature (°C)
	CPU Fan – Fan Control>	Sets CPU Fan Control mode Disable - Stops fan. Manual – Manually sets the fan Auto – Hardware monitor controls cooling, similar to ACPI based 'Active Cooling', without producing a software load to the system. [Disabled, Manual, **Auto**]
	CPU Fan – Fan Pulse>	Displays number of pulses the fan produces during one revolution. (Range: 1-4)
	CPU Fan – Fan Trip Point>	Displays temperature at which the fan accelerates. (Range: 20°C – 80°)
	CPU Fan – Trip Point Speed>	Displays Fan speed at trip point in %. Minimum value is 30%. Fan always runs at 100% at (TJmax.-10°C).
	CPU Fan – Ref. Temperature>	Determines temperature source used for automatic fan control [**Module Temperature**, CPU Temperature]
	Additional Information CPU Temperature The CPU temperature value is taken from a thermal resistor (NTC) that is placed very close to the CPU. The NTC resistor is not capable of measuring very fast rises and falls in temperature and measurements show a certain non-linearity. The NTC thermal resistor gives a general indication of the temperature close to the CPU. If the NTC thermal resistor value is compared to internal CPU values (i.e. DTS based values) certain differences are expected. These differences are due to the design and are not a bug. The thermal resistor method was chosen because the CPU does not support PECI based temperature measurement, and does not supply an internal diode on the CPU's die that can be used instead of PECI. Reading the DTS based values would harm the system's real-time behavior and is therefore not used.	

Sub-Screen	Function	Second level Sub-Screen / Description	
H/W Monitor> (continue)	External Fan-Fan Control>	Sets Fan Control mode for external fan Disable - Stops the fan Manual – Manually set the fan Auto - Hardware monitor controls cooling, similar to ACPI based 'Active Cooling', without producing a software load to the system. [Disable, Manual, **Auto**]	
	External Fan–Fan Pulse>	Displays number of pulse the fan produces during one revolution (Range: 1-4)	
	External Fan-Fan Trip point>	Displays temperature at which fan accelerates. (Range: 20°C to 80°C)	
	External Fan-Trip Point Speed>	Displays fan speed at trip point in %. Minimum value is 30% Fan always runs at 100% at (TJmax.-10°C)	
	External Fan Reference Temperature>	Determines temperature source used for automatic fan control [**Module Temperature**, CPU Temperature]	
	Additional Information External Fan An external fan can be connected to baseboard. The external fan's control lines are routed via the COMe connector.		
	5.0V Standby>	Read only field Displays standby voltage	
	Batt. Volt. at COMe pin>	Read only field Displays battery voltage at COMe pin	
	Wide range VCC>	Read only field Displays wide range VCC	
Serial Port Console Redirection>	COM0 Console Redirection>	Console redirection via COMe module's COM1. [Enabled, **Disabled**]	
	COM1 Console Redirection>	Console redirection via COMe module's COM2. [Enabled, **Disabled**]	
	COM2 Console Redirection>	Console redirection via COMe module's COM3. [Enabled, **Disabled**]	
	COM3 Console Redirection>	Console redirection via COMe module's COM4 [Enabled, **Disabled**]	
	Additional Information COM # Console If redirection is enabled then the port settings such as Terminal type, Bits per second, Data bits, Parity etc. can be adjusted here. On-module COM ports do not support flow control. If the Port is disabled, the COM# port is displayed as a read only field.		
	Legacy Console Redirection settings>	Legacy Serial Redirection Port>	Selects a COM port to display redirection of legacy OS and legacy OPROM messages [**COM0**, COM1, COM2, COM3]
	Serial Port for Out-of-Band Management / Windows EMS Console Redirection>	Console redirection [Enabled, **Disabled**]	

Sub-Screen	Function	Second level Sub-Screen / Description	
CPU Configuration>	Socket 0 CPU Information>	Read only field Processor Type, CPU signature, Microcode patch, Max. CPU Speed, Min. CPU speed, Processor Cores, Intel HT technology, Intel VT-x technology, L1 Data Cache, L1 Code Cache, L2 Cache and L3 Cache.	
	Read only field Speed and 64 bit		
	CPU Power Management Configuration>	EIST>	Intel Speedstep® [**Enabled**, Disabled]
		Turbo Mode>	Turbo mode Note: EMTTM must also be enabled. Auto means enabled unless the max. turbo ratio is bigger than 16-SKL A0 W/A. [**Enabled**, Disabled]
		Boot Performance Mode>	Selects the performance state the BIOS sets before OS handoff [**Max. Performance**, Max. Battery]
		C-States>	Enables or disables CPU power management to allow CPU to enter C-State [**Enabled**, Disabled]
		Enhanced C-States>	Enables or disables C1E. If enabled CPU switches to minimum speed when all cores enter C-state. [**Enabled,** Disabled]
		Max. Package C-States>	Controls maximum package C-state that the processor supports [**PC2**, PC1, C0]
		Max. Core C-State>	Controls max. core C-state that cores support. [Fused value, Core C10, Core C9, Core C8 ,Core C7, **Core C6**, Core C1, Unlimited]
		C-State Auto Demotion>	Configures C-state auto demotion [Disabled, **C1**]
		C-State Un-demotion>	Configures C-state un-demotion [Disabled, **C1**]
	Active Processor Cores>	Number of cores to enable in each processor package [Enabled, **Disabled**]	
	Intel (VME) Virtual Technology>	Enables VMM to utilize additional hardware capabilities provided by Vanderpool Technology [**Enabled**, Disabled]	
	VT-D>	CPU VT-d [Enabled, **Disabled**]	
	PROCHOT>	Enables external agents can drive PROCHOT# to throttle the processor [**Enabled,** Disabled]	
	Monitor MWait>	Monitor Mwait [Enabled, Disabled, **Auto**]	
	P-State Coordinator>	Changes P-State coordination type [**HW_ALL**, SW_ALL, SW_ANY]	
	DTS>	Digital Thermal Sensor (DTS) [Enabled, **Disabled]**	

Sub-Screen	Function	Second level Sub-Screen / Description	
SIO Configuration>	Read only field AMI SIO driver version		
	Serial Port 0>	Use This Device>	Enables or disables the use of this logical device [**Enabled**, Disabled]
		Logical Device Settings: Current>	Read only field IO=3F8h; IRQ=4
		Logical Device Settings: Possible>	Allows the user to change the device's resource settings. New settings are reflected on the setup page after system restarts. [**Use Automatic Settings**, IO=3F8h; IRQ=4, IO=3F8h; IRQ=3,4,5,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,7,9,10,11,12, IO=3E8h; IRQ=3,4,5,7,9,10,11,12, IO=2E8h; IRQ=3,4,5,7,9,10,11,12]
	Serial Port 1>	Use This Device>	Enables or disables the use of this logical device [**Enabled**, Disabled]
		Logical Device Settings: Current>	Read only field IO=2F8h; IRQ=3
		Logical Device Setting: Possible>	Allows the user to change the device's resource settings. New settings are reflected on the setup page after system restart. [**Use Automatic Settings**, IO=2F8h; IRQ=3, IO=3F8h; IRQ=3,4,5,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,7,9,10,11,12, IO=3E8h; IRQ=3,4,5,7,9,10,11,12, IO=2E8h; IRQ=3,4,5,7,9,10,11,12]
	Additional Information SIO: Warning: Logical Devices state on the left side of the control reflects the current logical device state. Changes made during the setup session are shown after restarting the system. Disabling SIO logical devices may have unwanted effects. The SIO Configuration menu enables all available serial interfaces to be configured. The module-based serial interfaces always appear as COM1 and COM2. COM 1 and COM 2 can be treated as 16550-compatible legacy COM interfaces at the standard I/O addresses and are based in the on-module CPLD. Note: Hardware flow control is not supported. Optionally, If the baseboard contains an activated SuperIO of the type Winbond 83627, then its serial interfaces are added to the system as COM3 and COM4. COM3 and COM4 IRQ and I/O addresses are configurable in this menu, too. Although the chipset internal COMs are not supported due to technical constraints their driver must be installed. Installing the driver does not mean that these serial interfaces are useable.		
Network Stack Configuration>	Network Stack>	UEFI network stack [Enabled, **Disabled**]	
USB Configuration>	Read only fields USB Configuration, UBS module version, USB controllers, and USB devices		
	XHCI Hand-off>	XHCI ownership change claimed by XHCI driver Note: This is a work around for OS(s) without XHCI hand-off support. [**Enabled,** Disabled]	

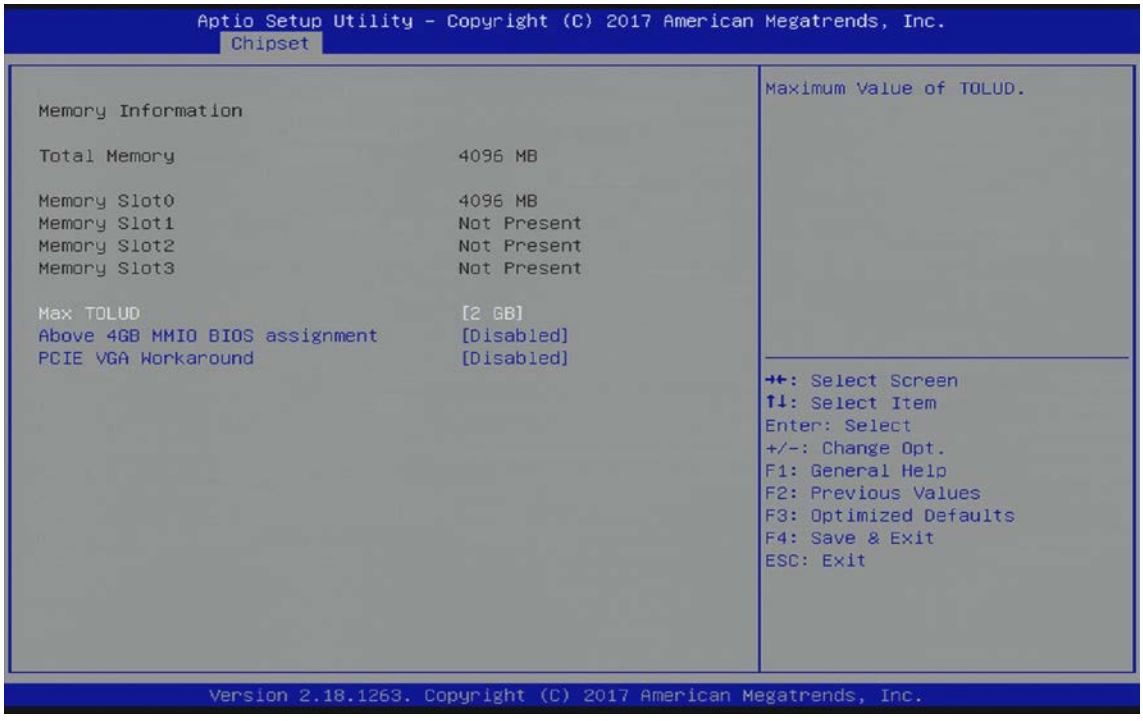
Sub-Screen	Function	Second level Sub-Screen / Description
USB Configuration> (continued)	USB Mass Storage Driver Support>	USB mass storage driver support [**Enabled,** Disabled]
	USB Transfer Time-out>	Displays timeout value for control, bulk and interrupt transfers [1 sec, 5 sec, 10 sec, **20 sec**]
	Device Reset Time-out>	Displays USB mass storage device start unit command time-out [10 sec, **20 sec**, 30 sec, 40 sec]
	Device Power-up Delay>	Displays maximum time device takes to report to the host properly. Auto uses the default values of 100 ms for a root port and for a hub port the delay is taken from hub port descriptor. [**Auto**, Manual]

6.2.3. Chipset Setup Menu

The Chipset Setup menu screen lists four sub-screen options North Bridge, South Bridge, Uncore Configuration and South Cluster Configuration..

6.2.3.1. Chipset>North Bridge

Figure 10: Chipset > North Bridge Menu Initial Screen



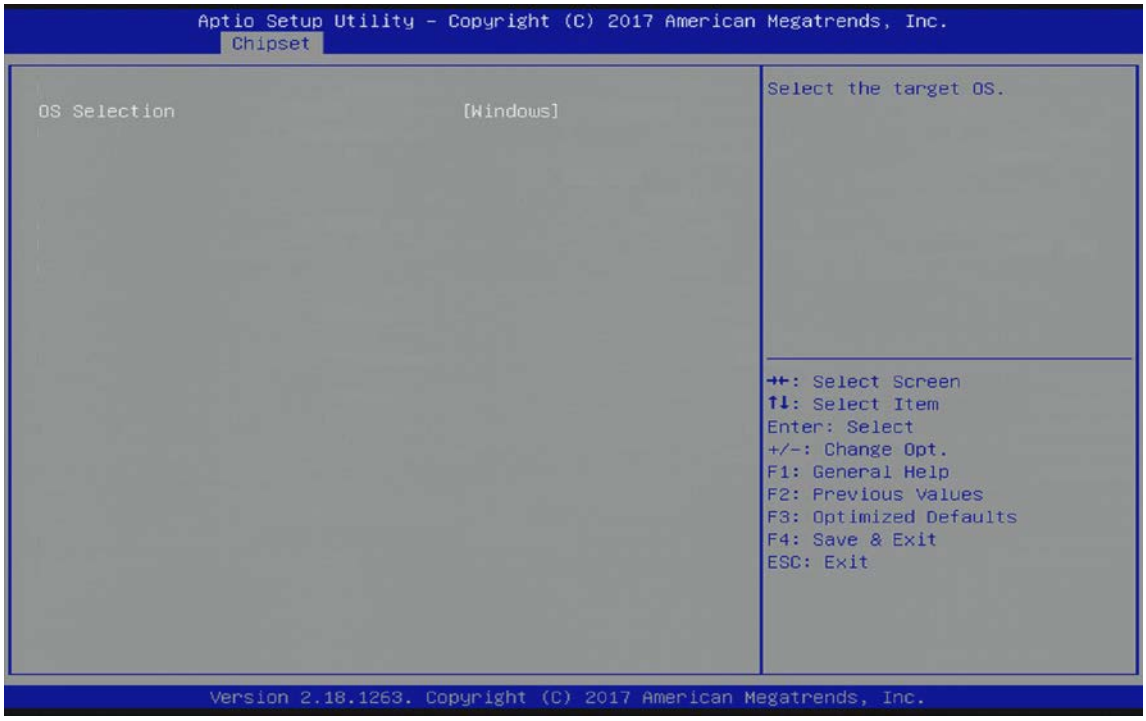
The following table shows the North bridge sub-screens and functions, and describes the content. Default settings are **bold**.

Table 32: Chipset> North Bridge Sub-screens and Function

Function	Second level Sub-Screen / Description	
Memory Configuration>	Read only field Total memory, Memory slot 0, Memory slot 1.	
	Max TOLUD>	Sets the maximum TOLUD value Dynamic assignment adjusts TOLUD automatically, based on largest MMIO length of the installed graphic controller [**2 GB**, 2.25 GB, 2.5 GB, 2,75 GB, 3 GB]
	Above 4GB MMIO BIOS Assignment>	Enables or disables above 4 GB memory mapped IO BIOS assignment. This is disabled automatically when aperture size is set to 2048 MB. [Enabled, **Disabled**]
	PCIE VGA Workaround>	Enable If PCIe card cannot boot in DOS. For test purposes only. [Enabled, **Disabled**]

6.2.3.2. Chipset> South Bridge

Figure 11: Chipset > South Bridge Menu Initial Screen



The following table shows the South bridge sub-screens and functions, and describes the content. Default settings are **bold.**

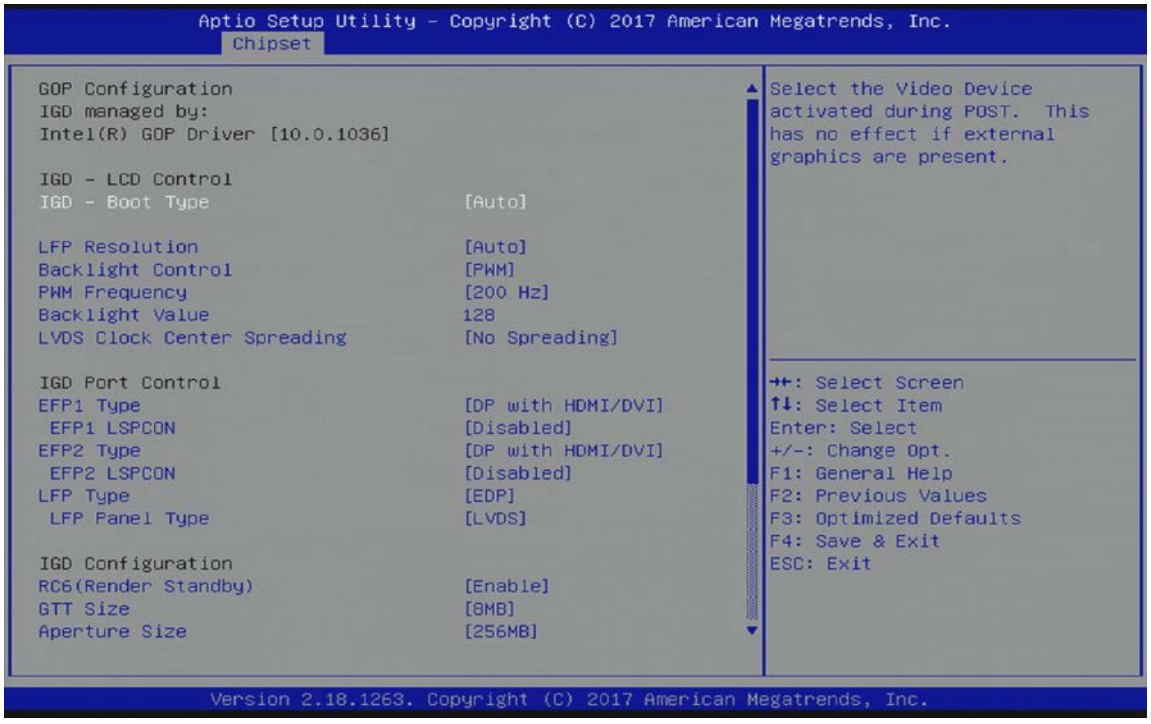
Table 33: Chipset> South Bridge Sub-screens and Functions

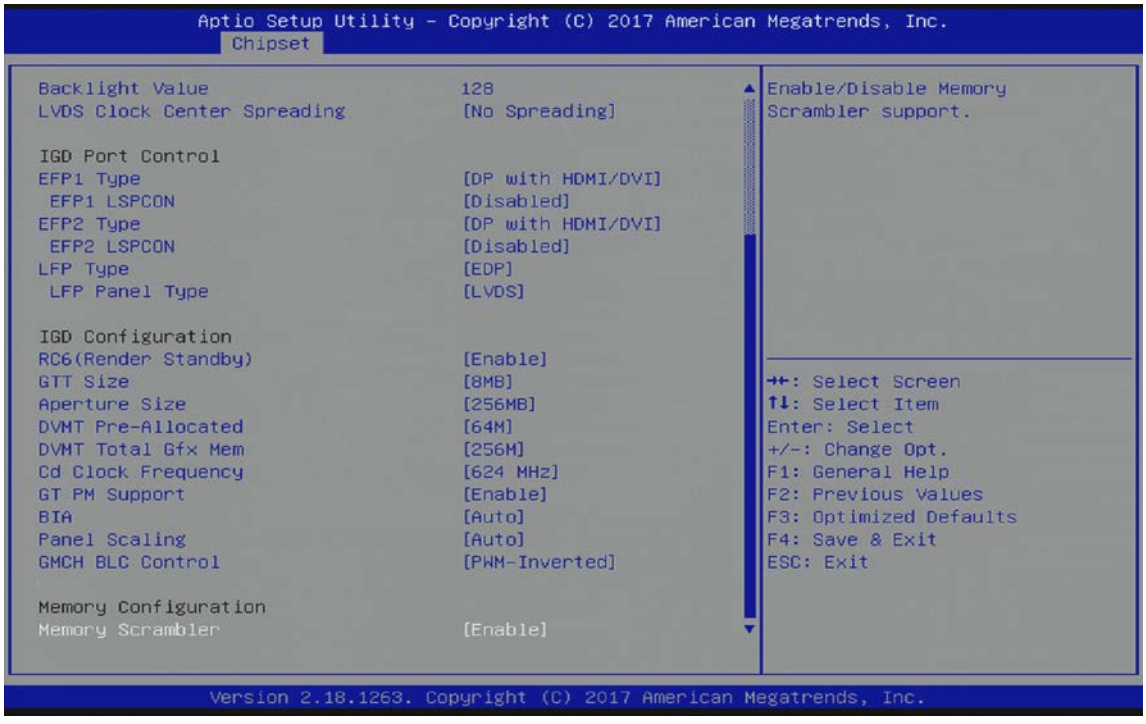
Function	Second level Sub-Screen / Description
OS Selection>	Selects target OS. [**Windows**, Android, Intel Linux]

The OS Selection function must but be selected in the setup to reflect the Operating System (OS) in use. Otherwise, the correct functionality might not be possible.

6.2.3.3. Chipset>Uncore Configuration

Figure 12: Chipset>Uncore Configuration Menu Initial Screens





The following table shows the Uncore Configuration sub-screens and functions, and describes the content. Default settings are **bold.**

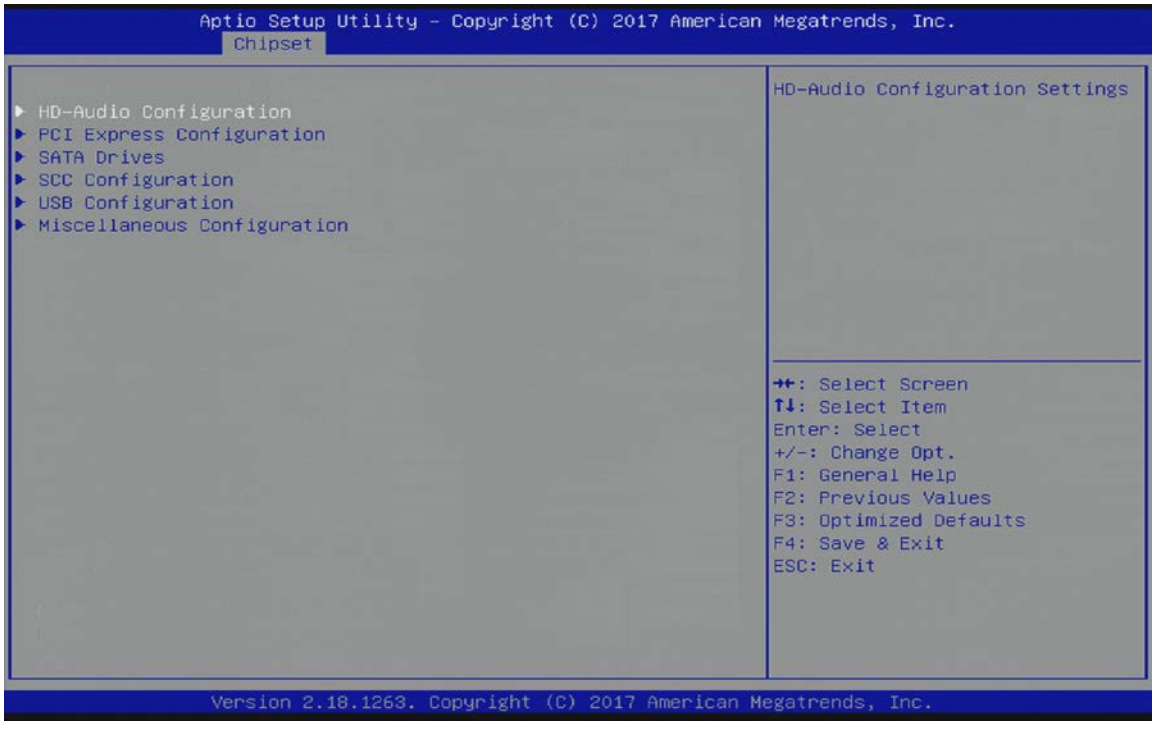
Table 34: Chipset> Uncore Configuration Sub-screens and Functions

Function	Second level Sub-Screen / Description
Read only field GOP Configuration data and IGD managed by Intel® GOP driver Information	
IGD–Boot Type>	Selects the internal video device activated during POST This has no effect if external graphics are present. [**Auto**, LFP, EFP1, EFP2]
IGD-Secondary Boot Type	Selects the second internal video device activated during post. [**Disabled**, EFP1, EFP2]
LFP Resolution>	Selects LFP used by Internal Graphics device by selecting the appropriate setup item Default is [**Auto**]
Backlight Control>	Backlight control setting [None/External, **PWM**, PWM Inverted, I2C, I2C Inverted]
PWM Frequency>	Sets LCD backlight PWM frequency [**200 Hz**, 400 Hz, 1 kHz, 2 kHz, 4 kHz, 8 kHz, 20 kHz, 40 kHz]
Backlight Value>	Sets LCD backlight brightness Range: (0-255)
LVDS Clock Center Spreading>	Selects LVDS clock frequency center spreading depth [**No Spreading**, 0.5%, 1.0%, 1.5%, 2.0%, 2.5%]
EFP1 Type>	Integrated HDMI/Display Port configuration with external connectors [No Device, DisplayPort Only, **DP with HDMI/DVI**, DP with DVI, HDMI/DVI, DVI Only]
EFP1 LSPCON>	HDMI 2.0 feature Level shifter/Protocol converter [Enabled, **Disabled**]
EFP2 Type>	Integrated HDMI/Display Port configuration with external connectors [No Device, DisplayPort Only, **DP with HDMI/DVI,** HDMI/DVI,]
EFP2 LSPCON>	HDMI 2.0 feature Level shifter/Protocol converter [Enabled, **Disabled**]
LFP Type>	LFP Configuration [No Device, **EDP**]
LFP Panel Type>	Selects panel type connected to eDP port as native eDP or LVDS via bridge device. This switch depends on the modules H/W option. [**LVDS**, eDP]
RC6 (render Standby)>	Check to enable render standby support. IF SOix is enabled, RC6 should be enabled. This function is read only if SOix is enabled. [**Enabled**, Disabled]
GTT Size>	Selects the GTT size [2 MB, 4 MB, **8 MB**]
Aperture Size>	Selects the aperture size [128 MB, **256 MB**, 512 MB]

Function	Second level Sub-Screen / Description
DVMT Pre-Allocated>	Selects DVMT 5.0 pre-allocated (fixed) graphics memory size used by Internal graphics [**64 M**, 96 M, 128 M, 160 M, 192 M, 224 M, 256 M, 288 M, 320 M, 352 M 384 M, 416 M, 448 M, 480M, 512 M]
DVMT Total Gfx Mem>	Selects DVMT 5.0 total graphics memory size used by internal graphics device [128 M, **256 M**, MAX]
Cd Clock Frequency>	Selects the highest Cd clock frequency supported by the platform [144 MHz, 288 MHz, 384 MHz, 576 MHz, **624 MHz**]
GT PM Support>	GT PM Support [**Enabled**, Disabled]
BIA>	Auto: GMCH uses VBIOS default Level n: is enabled with selected aggressiveness level [**Auto**, Disabled, Level 1, Level 2, Level 3, Level 4, Level5]
Panel Scaling>	Sets Panel scaling [**Auto**, Centering, Stretching]
GMCH BLC Control>	Backlight control settings [**PWM-Inverted**, GMBus-Inverted, PWM-Normal, GMBus-Normal]
Memory Scrambler>	Memory scrambler support [**Enabled**, Disabled]

6.2.3.4. Chipset>South Cluster Configuration

Figure 13: Chipset>South Cluster Configuration Menu Initial Screen



The following table shows the South Cluster Configuration sub-screens and functions, and describes the content. Default settings are **bold.**

Table 35: Chipset>South Cluster Configuration Menu Sub-screens and Functions

Function	Second level Sub-Screen / Description	
HD Audio Configuration>	HD-Audio Support>	HD-Audio support [**Enabled**, Disabled]
	HD-Audio CSME memory Transfers>	Sets HD-Audio CSME memory transfers to VC0/VC2 [**VC0**, VC2]
	HD-Audio CSME Memory Transfers>	Sets HD-Audio CSME memory transfers to VC0/VC2 [**VC0**, VC2]
	HD-Audio Host Memory Transfers>	Sets HD-Audio Host memory transfers to VC0/VC2 [**VC0**, VC2]
	HD-Audio I/O Buffer Ownership Select>	Sets HD-Audio I/O buffer ownership [HD-Audio link owns all the I/O buffers, **I2S port owns all the I/O buffers**]
	HD-Audio Clock Gating>	HD-Audio Clock gating [**Enabled**, Disabled]
	HD-Audio Power Gating>	HD-Audio Power gating [**Enabled**, Disabled]

Function	Second level Sub-Screen / Description		
HD Audio Configuration> (continued)	HD-Audio PME>	HD-Audio PME [**Enabled**, Disabled]	
	HD-Audio Link Frequency>	Selects HD-Audio link frequency Applicable only if HDA codec supports selected frequency. [6 MHz, 12 MHz, **24 MHz**]	
	iDisplay Link Frequency>	Selects iDisplay Link frequency Applicable only if iDisp codec supports selected frequency. [48 MHz, **96 MHz**]	
PCI Express Configuration>	PCI Express Clock Gating>	PCI Express clock gating for each root port [Enabled, **Disabled**]	
	Port8xh Decode>	PCI express port 8xh decode [Enabled, **Disabled**]	
	Peer Memory Write Enable>	Peer memory write [Enabled, **Disabled**]	
	Compliance Mode>	Enable when using compliance load board [Enabled, **Disabled**]	
	PCI Root Port 3 (COMe PCIe#1)> or PCI Root Port 4 (COMe PCIe#2)> or PCI Root Port 5 (COMe PCIe#3)> or PCI Root Port 6 (GbE)>	PCI Express Root Port[#]>	Controls the PCI Express port [**Enabled**, Disabled]
		ASPM>	PCI Express Active State Power Management (ASPM) level settings [**Disabled**, L0s, L1, L0sL1, Auto]
		L1 Substates>	PCI Express L1 substrates settings [Disabled, L1.1, L1.2, **L1.1 & L1.2**]
		ACS>	Access Control Service Extended Capability [**Enabled**, Disabled]
		URR>	PCI Express unsupported request reporting [Enabled, **Disabled**]
		FER>	PCI Express device fatal error reporting [Enabled, **Disabled**]
		NFER>	PCI Express device non-fatal error reporting [Enabled, **Disabled**]
		CER>	PCI Express device correctable error reporting [Enabled, **Disabled**]
		CT0>	PCI Express completion timer (T0) [**Default Setting**, 16 ms55 ms, 65ms210 ms, 260 ms900 ms, 1 s-3.5 s, Disabled]
		SEFE>	Root PCI Express System Error on Fatal Error [Enabled, **Disabled**]
		SENFE>	Root PCI Express System Error on non-Fatal Error [Enabled, **Disabled**]
		SECE>	Root PCI Express System Error on correctable error [Enabled, **Disabled**]

Function	Second level Sub-Screen / Description		
PCI Express Configuration> (continued)	PCI Root Port 3 (COMe PCIe#1)> or PCI Root Port 4 (COMe PCIe#2)> or PCI Root Port 5 (COMe PCIe#3)> or PCI Root Port 6 (GbE)> (continued)	PME SCI>	PCI Express PME SCI [**Enabled**, Disabled]
		PCIe Speed>	Configures PCIe speed [**Auto**, Gen 1, Gen2]
		Transmitter Half Swing>	Transmitter half swing [Enabled, **Disabled**]
		Extra Bus Reserved>	Extra bus reserved for bridges behind this root bridge. (0-7)
		Reserved Memory>	Reserved memory and prefetchable memory for this root bridge Range: (1 MB-20 MB)
		Reserved I/O>	Reserved I/O for this root bridge Range: (4 k, 8 k, 16 k, 20 k)
		PCH PCIE1 LTR>	PCH PCIE latency reporting [**Enabled**, Disabled]
		Snoop Latency Override>	Snoop latency override or Non Snoop override for PCH PCIE. Disabled: disables override Manual: manually enters override values Auto: maintains default BIOS flow. [Disabled, Manual, **Auto**]
		Non Snoop Latency Override>	
		PCIE1 LTR Lock>	PCIE LTR configuration lock [Enabled, **Disabled**]
		PCIE Selectable De-emphasis>	Selects level of de-emphasis for an upstream component, if the Link operates at 5.0 GT/s speed. (1b – 3.5 dB, 0b – 6 dB) [**Enabled,** Disabled]
SATA Drivers>	Chipset SATA>	Enables or disables the Chipset SATA controller. Chipset SATA controller supports two black internal SATA ports (up to 3 Gb/s per port.) [**Enabled**, Disabled]	
	SATA Test Mode>	Test mode [Enabled, **Disabled**]	
	Aggressive LPM>	Enable PCH to aggressively enter link power state [Enabled, **Disabled**]	
	SATA Port 0> or SATA Port 1>	SATA Port #>	Read only field SATA port installed/Not Installed and software preserve
		Port #>	SATA port # [**Enabled**, Disabled]
		SATA Port # Hot Plug Capability>	Reports SATA port as Hot Plug capable [Enabled, **Disabled]**
		Configured as eSATA>	Read only field

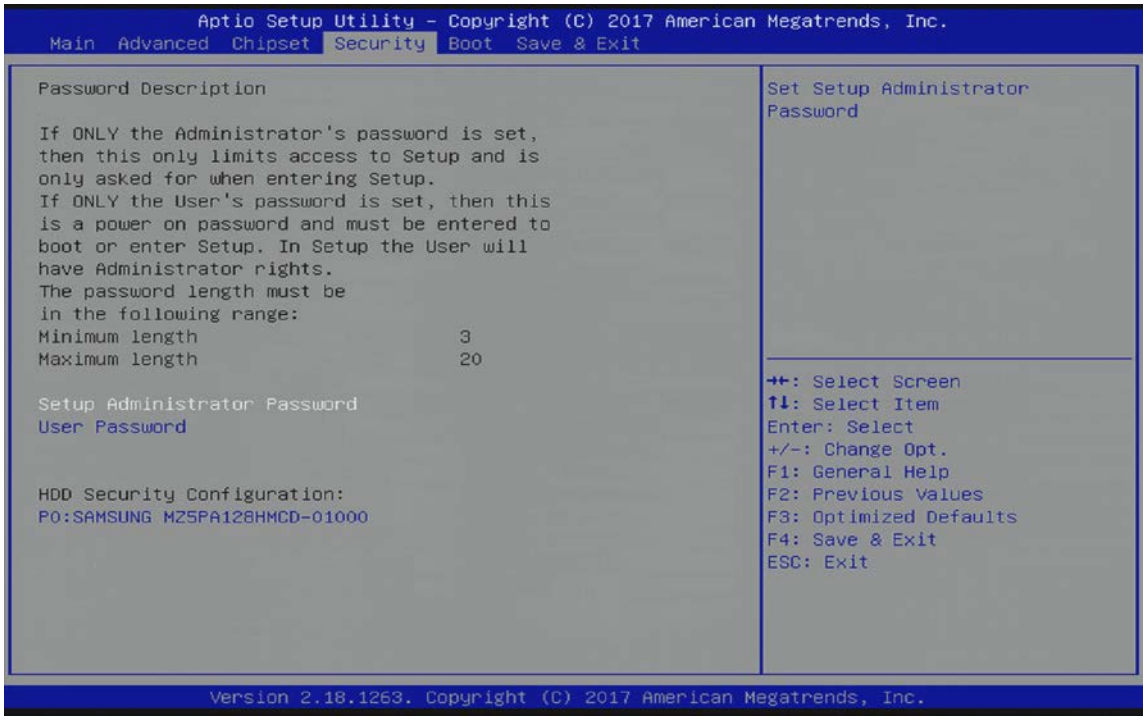
Function	Second level Sub-Screen / Description		
SATA Drivers> (continued)	SATA Port 0> or SATA Port 1> (continued)	Mechanical Presence Switch>	Controls reporting if port has a mechanical presence switch Note: Requires hardware support. [Enabled, **Disabled**]
		Spin Up Device>	If enabled for any port, staggered spin-up is performed and only drives with this option enabled will spin up at boot. Note: Otherwise, all drives spin up at boot. [Enabled, **Disabled**]
		SATA Device Type>	Identifies if SATA port is connected to a solid-state drive or hard disk drive. [**Hard Disk Drive**, Solid State Drive]
		SATA Port# DevSlp>	SATA Port # DevSlp Note: Board rework needed for LP before enabling. [Enabled, **Disabled**]
		DITO Configuration>	DITO configuration [Enabled, **Disabled**]
		DITO Value>	Read only field
		DM Value>	Read only field
SCC Configuration>	SCC SD Card Support (D27:F0)>	SCC card support [**Enabled**, Disabled]	
	SCC eMMC Support (D28:F0)>	SCC eMMC Support [**Enabled**, Disabled]	
	eMMC Max Speed>	Selects the eMMC max. speed allowed [**HS400**, HS200, DDR50]	
USB Configuration>	XHCI Pre-Boot Driver>	XHCI pre-boot driver support [Enabled, **Disabled**]	
	xHCI Mode>	Disable- disables XHCI controller function and USB devices are NOT detectable or usable during boot and in OS. Note: Do not disable unless required for debugging purposes. [**Enabled**, Disabled]	
	USB VBUS>	VBus should be 'ON' in host mode and 'OFF' in OTG device mode [Off, **ON**]	
	USB Port Disable Override>	Selectively enables or disables the corresponding USB port from reporting a device connection to the controller. [Enabled, **Disabled**]	
	xDCI Support>	XDCI [**Disable**, PCI Mode]	
	USB HW Mode AFE Comparators>	USB HW mode AFE comparators [Enabled, **Disabled**]	
Miscellaneous Configuration>	8254 Clock Gating>	8254 Clock gating [Enabled, **Disabled**]	

Function	Second level Sub-Screen / Description	
Miscellaneous Configuration> (continued)	State After G3>	Specifies which state to go to if power is reapplied after power failure (G3 state) S0 state: System boots directly as soon as power is applied. S5 state: System remains in power-off states until the power button is pressed. [**S0 State**, S5 State]
	Board Clock Spread Spectrum>	Clock chip's spread spectrum feature [Enabled, **Disabled**]
	Wake On LAN>	Wake on LAN [**Enabled**, Disabled]
	BIOS Lock>	SC BIOS Lock features NOTE: Required to be enabled to ensure SMM protection of flash. [**Enabled**, Disabled]
	DCI Enable (HDCIEN)>	If enabled, the user is considered to have consented to enable DCI and allows debug over the USB 3 interface. If disabled, the host controller does not enable the DCI feature. [Enabled, **Disabled**]
	DCI Auto Detect Enable>	If set, DCI Auto detects if DCI is connected during BIOS post time and enables DCI. If not set, DCI is disabled. [**Enabled**, Disabled]

6.2.4. Security Setup Menu

The Security Setup menu provides information about passwords and functions for specifying the security settings.

Figure 14: Security Setup Menu Initial Screen



The following table shows the Security set up sub-screens and functions, and describes the content.

Table 36: Security Setup Menu Sub-screens and Functions

Function	Description	
Setup Administrator Password>	Sets administrator password	
User Password>	Sets user password	
HDD Security Configuration>	Read Only Information Allows access to set, modify and clear Hard Disk user and master passwords. User Passwords need to be installed for Enabling Security. Master Password can be modified only when successfully unlocked with the Master Password in Post. If the 'Set HDD Password' is grayed out, then perform a power cycle to enable the option again. HDD Password Configuration Security Supported : Yes Security Enabled : No Security Locked : No Security Frozen : No HDD User Pwd Status : Not Installed HDD Master Pwd Status : Installed	
	Set User Password>	Sets HDD password.

Function	Description	
HDD Security Configuration> (continued)	Set User Password> (continued)	Note: It is advisable to power cycle the system after setting Hard Disk passwords. The 'Discard or Save Changes' setup option does not have an impact on HDD when the password is set or removed. Note: If the 'Set HDD User Password' option is grayed out, perform a power cycle to enable the option again.

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering the setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum length 20 and minimum length 3.

6.2.4.1. Remember the Password

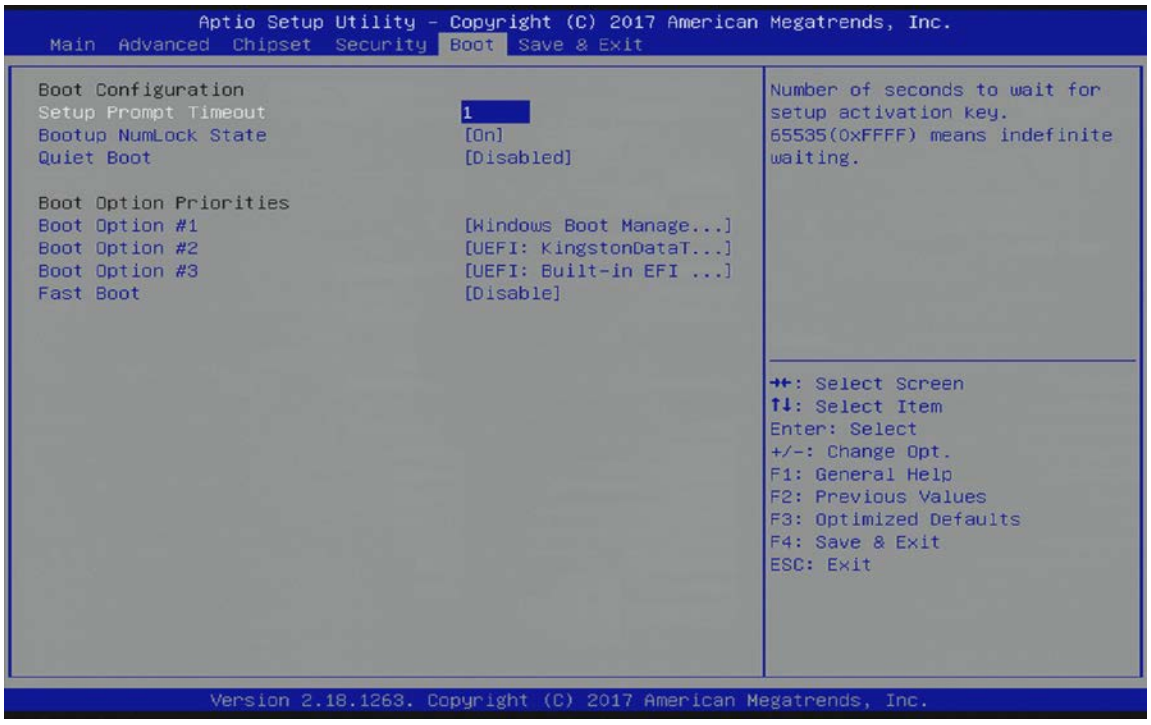
It is recommended to keep a record of all passwords in a safe place. Forgotten passwords results in the user being locked out of the system. If the system cannot be booted because the User Password or the Supervisor Password are not known, clear the uEFI BIOS settings, or contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

6.2.5. Boot Setup Menu

The Boot Setup menu lists the dynamically generated boot device priority order.

Figure 15: Boot Setup Menu Initial Screen



The following table shows the Boot Setup sub-screens and functions and describes the content. Default settings are **bold**.

Table 37: Boot Setup Menu Sub-screens and Functions

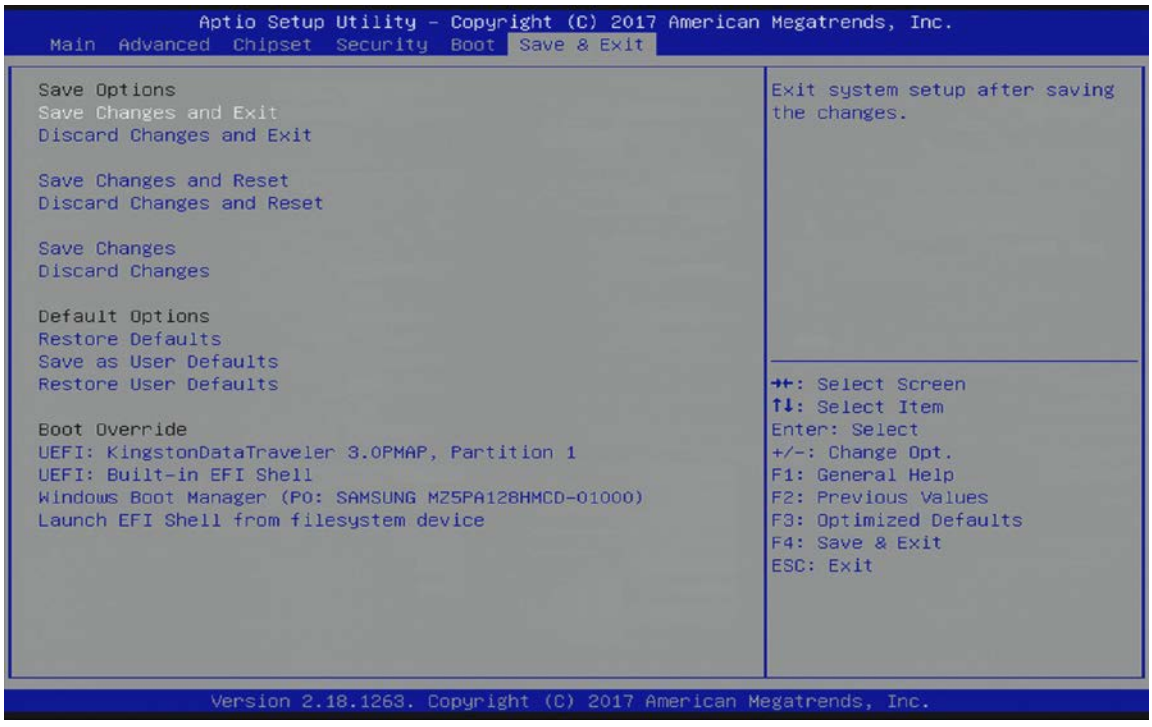
Function	Description
Setup Prompt Timeout>	Displays number of seconds the firmware waits for setup activation key The value 65535(0xFFFF) means an indefinite wait.
Bootup NumLock State>	Selects keyboard NumLock state [**ON**, OFF]
Quiet Boot>	Quiet Boot [Enabled, **Disabled**]
Boot Option #1>	Sets the system boot order [UEFI: KingstonDataTraveler 3.0PMAP, partition 1 UEFI: Built in EFI Shell **Windows Boot Manager (PO: Samsung MZ5PA128HMCD-01000)** Disabled]
Boot Option #2>	Sets the system boot order [**UEFI: KingstonDataTraveler 3.0PMAP, partition 1** UEFI: Built in EFI Shell Windows Boot Manager (PO: Samsung MZ5PA128HMCD-01000) Disabled]

Function	Description
Boot Option #3>	Sets the system boot order [UEFI: KingstonDataTraveler 3.0PMAP, partition 1 **UEFI: Built in EFI Shell** Windows Boot Manager (PO: Samsung MZ5PA128HMCD-01000) Disabled]
Fast Boot>	Enables or disables FastBoot features Note: Most probes are skipped to reduce time and cost during boot. [Enabled, **Disabled**]

6.2.6. Save and Exit Setup Menu

The Save and Exit Setup menu provides functions for handling changes made to the settings and exiting the program.

Figure 16: Save and Exit Setup Menu Initial Screen



The following table shows the Save and Exit Setup sub-screens and functions.

Table 38: Save and Exit Setup Menu Sub-screens and Functions

Function	Description
Save Changes and Exit >	Exits system after saving changes
Discard Changes and Exit>	Exits system setup without saving changes
Save Changes and Reset>	Resets system after saving changes
Discard Changes and Reset>	Resets system setup without saving changes
Save Changes>	Saves changes made so far for any setup options
Discard Changes>	Discards changes made so far for any setup options
Restore Defaults>	Restores/loads standard default values for all setup options
Save as User Defaults>	Saves changes made so far as user defaults
Restore User Defaults>	Restores user defaults to all setup options
Boot override UEFI: KingstonDataTraveler 3.0PMAP, Partition 1>	Attempts to launch the boot option #2
Boot override UEFI: Built in EFI Shell>	Attempts to launch the boot option #3

Function	Description
Boot override Windows Boot Manager (PO: Samsung MZ5PA128HMCD-01000)>	Attempts to launch the boot option #1
Boot override Launch EFI Shell from File System Device>	Attempts to launch EFI Shell application (Shell.efi) from one of the available file system devices

6.3. The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

AMI APTIO update utilities for DOS, EFI Shell and Windows are available at AMI.com: http://www.ami.com/support/downloads/amiflash.zip.

Kontron uEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual.

6.3.1. Basic Operation of the uEFI Shell

The uEFI Shell forms an entry into the uEFI boot order and is the first boot option by default.

6.3.1.1. Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power the board.
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices.
3. Choose 'UEFI: Built-in EFI shell'.

```
EFI Shell version 2.40 [5.11]
Current running mode 1.1.2
Device mapping table
Fs0      :HardDisk - Alias hd33b0b0b fs0
   Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
```

4. Press the <ESC> key within 5 seconds to skip startup.nsh, and any other key to continue.
5. The output produced by the device mapping table can vary depending on the board's configuration.
6. If the <ESC> key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell>
```

6.3.1.2. Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Use the **exit** uEFI Shell command to select the boot device, in the Boot menu, that the OS boots from.
2. Reset the board using the **reset** uEFI Shell command.

6.4. uEFI Shell Scripting

6.4.1. Startup Scripting

If the <ESC> key is not pressed and the timeout has run out then the uEFI Shell automatically tries to execute some startup scripts. It searches for scripts and executes them in the following order:

1. Initially searches for Kontron flash-stored startup script.
2. If there is no Kontron flash-stored startup script present, then the uEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued.

6.4.2. Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor edit or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system. To copy the startup script to the flash, use the **kBootScript** uEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the **kRamdisk** uEFI Shell command.

6.4.3. Example of Startup Scripts

6.4.3.1. Execute Shell Script on other Hard Drive

This example (**startup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disc drive (**fs0**).

```
fs0:
bootme.nsh
```

6.5. Firmware Update

Firmware updates are typically delivered as a ZIP archive containing only the firmware images. The content of the archive with the directory structure must be copied onto a data storage device with FAT partition.

6.5.1. Updating Procedure

BIOS can be updated with the Intel tool fpt.efi using the procedure below:

1. Copy the following files to an USB stick:

- flash.nsh (if available)
- fpt.efi
- fparts.txt
- cAL6r<xxx>.bin (where xxx stands for the version #)

2. Start the system into uEFI BIOS setup. (see Chapter 6.1: Starting the uEFI BIOS).
3. Disable the BIOS lock.

   Chipset > South Cluster Configuration> Miscellaneous Configuration> BIOS Lock > Disabled

4. Save and Exit the BIOS setup.
5. On the next start, boot into shell. (see Chapter 6.3.1.1: Entering the uEFI Shell).

6. Change to the drive representing the USB stick:

```
fsx:   (x = 0,1,2,etc. represents the USB stick)
```

and then change to the directory where you copied the flash tool:

```
cd <your_directory>
```

7. Start flash.nsh (if available) or enter the following:

```
fpt  –F cal6r<xxx>.bin
```

8. Wait until flashing is successful and then power cycle the board.

Do not switch off the power during the flash process!
Doing so leaves your module unrecoverable.

Changes made after step 3 above are only effective during the first boot after applying the changes. If you fail to flash during the next boot, you might have to repeat the steps under 3.

Appendix A: List of Acronyms

Table 39: List of Acronyms

ACPI	Advanced Configuration Power Interface
BIOS	Basic Input Output System
BSP	Board Support Package
Carrier Board	Application specific circuit board that accepts a COM Express ® module
COM	Computer-on-Module
COMe-b	COM Express® b=basic 125 mm x 95 mm module form factor
COMe-c	COM Express® c=compact 95 mm x 95 mm module form factor
COMe-m	COM Express® m=mini 84 mm x 55 mm module form factor
COP	Computer Operating Properly
DDC	Display Data Control
DDI	Digital Display Interface
DDIO	Digital Display Input/Output
DIMM	Dual In-line Memory Module
DP	DisplayPort
DMA	Direct Memory Access
DMIC	Digital Microphone
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface
EAPI	Embedded Application Programming Interface
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
eDP	Embedded Display Port
EMC	Electromagnetic Compatibility (EMC)
eMMC	Embedded Multimedia Card
ESD	Electro Sensitive Device
FAT	File Allocation Table
Gb	Gigabit
GbE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPU	Graphics Processing Unit
HDA	High Definition Audio (HD Audio)
HD/HDD	Hard Disk / Hard Disk Drive
HDMI	High Definition Multimedia Interface
HPM	PICMG Hardware Platform Management specification family
HWM	Hardware Monitor
IC	Integrated Circuit
I2C	Inter integrated Circuit Communications
IOT	Internet of Things
ISA	Industry Standard Architecture
LAN	Local Area Network
LPC	Low Pin-Count Interface:
LPT	Line Print Terminal
LVDS	Low Voltage Differential Signaling –
M.A.R.S.	Mobile Application for Rechargeable Systems
MDI	Media Dependent Interface
MLC	Multi Level Cell
MTBF	Mean Time Before Failure
NA	Not Available
NC	Not Connected
NC-SI	Network Communications - Services Interface
PCI	Peripheral Component Interface
PCIe	PCI-Express
PEG	PCI Express Graphics
PICMG®	PCI Industrial Computer Manufacturers Group
PHY	Ethernet controller physical layer device
Pin-out Type	COM Express® definitions for signals on COM Express® Module connector pins.
pSLC	pseudo Single Level Cell
PSU	Power Supply Unit
RoHS	Restriction of the use of certain Hazardous Substances
RTC	Real Time Clock
SATA	Serial AT Attachment:
SLC	Single Level Cell
SMB	System Management Bus
SoC	System on a Chip
SO-DIMM	Small Outline Dual In-line Memory Module
SOL	Serial Over LAN
SPI	Serial Peripheral Inteface

TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver Transmitter
UEFI	Unified Extensible Firmware Interface
UHD	Ultra High Definition
USB	Universal Serial Bus
VGA	Video Graphics Adapter
VLP	Very Low Profile
WDT	Watch Dog Timer
WEEE	Waste Electrical and Electronic Equipement (directive)

About Kontron

Kontron is a global leader in embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall. For more information, please visit: **www.kontron.com**

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