Lenovo

DC Persistent Memory Module Population Manual

First Edition (June 2019)

Contents

Chapter 1. DC Persistent Memory Module (DCPMM) setup

Follow the instructions in this section to complete required setup before installing DCPMMs for the first time, determine the most suitable configuration, and install memory modules accordingly.

Complete the following steps to finish system setup to support DCPMMs, and install the memory modules according to the designated combination.

1. Update the system firmware to the latest version that supports DCPMMs (see “Update the firmware” on page 6).
2. Make sure to meet all the following requirements before installing DCPMMs.
   - All the DCPMMs that are installed must be of the same part number.
   - All the DRAM DIMMs that are installed must be of the same type, rank, and capacity with minimum capacity of 16 GB. It is recommended to use Lenovo DRAM DIMMs of the same part number.
3. Refer to *DCPMM and DIMM installation order* sections in each system to determine the most suitable combination and the following:
   - Number and capacity of the DCPMMs and DRAM DIMMs to install.
   - Check if the presently installed processors support the combination. If not, replace the processors with ones that support the combination.
4. Based on the determined DCPMM combination, acquire the DCPMMs, DRAM DIMMs and processors if necessary.
5. Replace the processors if necessary.
6. Remove all the memory modules that are installed.
7. Follow the slot combination in *DCPMM and DIMM installation order* sections in each system to install all the DCPMMs and DRAM DIMMs.
8. Disable security on all the installed DCPMMs (see “Configure DC Persistent Memory Module (DCPMM)” on page 1).
9. Make sure the DCPMM firmware is the latest version. If not, update it to the latest version (see https://sysmgt.lenovofiles.com/help/topic/com.lenovo.lxca.doc/update_fw.html).
10. Configure DCPMMs so that the capacity is available for use (see “Configure DC Persistent Memory Module (DCPMM)” on page 1).

Configure DC Persistent Memory Module (DCPMM)

Follow the instructions in this section to configure DCPMMs and DRAM DIMMs.

DCPMM capacity could act as accessible persistent memory for applications or volatile system memory. Based on the approximate percentage of DCPMM capacity invested in volatile system memory, the following three operating modes are available for choice:

- **App Direct Mode** (0% of DCPMM capacity acts as system memory):

  In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

  The total displayed volatile system memory in this mode is the sum of DRAM DIMM capacity.

  Notes:

  - In App Direct Mode, the DRAM DIMMs that are installed can be configured to mirror mode.
  - When only one DCPMM is installed for each processor, only not-interleaved App Direct Mode is supported.
- **Mixed Memory Mode** (1-99% of DCPMM capacity acts as system memory):

  In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

  The total displayed volatile system memory in this mode is the DCPMM capacity that is invested in volatile system memory.
- **Memory Mode** (100% of DCPMM capacity acts as system memory):

  In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache.

  The total displayed volatile system memory in this mode is the sum of DCPMM capacity.

DCPMM Management options

DCPMMs can be managed with the following tools:

- **Lenovo XClarity Provisioning Manager (LEPT)**

  To open LEPT, power on the system and press **F1** as soon as the logo screen appears. If a password has been set, enter the password to unlock LEPT.

  Go to **UEFI Setup → System Settings → Intel Optane DCPMMs** to configure and manage DCPMMs.

  For more details, see https://sysmgt.lenovofiles.com/help/topic/LXPM/using_LXPM.html.

  Note: If the text-based interface of Setup Utility opens instead of Lenovo XClarity Provisioning Manager, go to **System Settings → <F1> Start Control** and select **Tool Suite**. Then, reboot the system and press **F1** as soon as the logo screen appears to open Lenovo XClarity Provisioning Manager.
- **Setup Utility**

  To enter Setup Utility:

  1. Power on the system and press **F1** to open LEPT.
  2. Go to **UEFI Settings → System Settings**, click on the pull-down menu on the upper right corner of the screen, and select **Text Setup**.
  3. Reboot the system, and press **F1** as soon as the logo screen appears.

  Go to **System Configuration and Boot Management → System Settings → Intel Optane DCPMMs** to configure and manage DCPMMs.
- **Lenovo XClarity Essentials OneCLI**

  Some management options are available in commands that are executed in the path of Lenovo XClarity Essentials OneCLI in the operating system. See https://sysmgt.lenovofiles.com/help/topic/toolsctr_cli_lenovo/onecli_t_download_use_tcscli.html to learn how to download and use Lenovo XClarity Essentials OneCLI.

Following are the available management options:

- **Intel Optane DCPMM details**

  Select this option to view the following details concerning each of the the installed DCPMMs:

  - Firmware version
  - Configuration status
  - Raw capacity
  - Memory capacity
  - App Direct capacity

- Unconfigured capacity
- Inaccessible capacity
- Reserved capacity
- Percentage remaining
- Security state

Alternatively, view DCPMM details with the following command in OneCLI:

```
onecli.exe config show IntelOptaneDCPMM
--imm USERID:PASSW0RD@10.104.195.86
```

Notes:
- *USERID* stands for XCC user ID.
- *PASSW0RD* stands for XCC user password.
- *10.104.195.86* stands for IP address.

- **Goals**
  - **Memory Mode [%]**

    Select this option to define the percentage of DCPMM capacity that is invested in system memory, and hence decide the DCPMM mode:

    - **0%:** App Direct Mode
    - **1-99%:** Mixed Memory Mode
    - **100%:** Memory Mode

    Go to **Goals → Memory Mode [%]**, input the memory percentage, and reboot the system.

    Notes:

    - Before changing from one mode to another:
      1. Make sure the capacity of installed DCPMMs and DRAM DIMMs meets system requirements for the new mode.
      2. Back up all the data and delete all the created namespaces. Go to **Namespaces → View/Modify/Delete Namespaces** to delete the created namespaces.
      3. Perform secure erase on all the installed DCPMMs. Go to **Security → Press to Secure Erase** to perform secure erase.
    - After the system is rebooted and the input goal value is applied, the displayed value in **System Configuration and Boot Management → Intel Optane DCPMMs → Goals** will go back to the following default selectable options:
      - **Scope:** [Platform]
      - **Memory Mode [%]:** 0
      - **Persistent Memory Type:** [App Direct]

      These values are selectable options for DCPMM settings, and do not represent the current DCPMM status.

    In addition, you can take advantage of a memory configurator, which is available at the following site: http://1config.lenovo.com/#/memory_configuration

    Alternatively, set DCPMM Goals with the following commands in OneCLI:

    1. Set create goal status.

       ```
       onecli.exe config set IntelOptaneDCPMM.CreateGoal Yes
       --imm USERID:PASSW0RD@10.104.195.86
       ```

    2. Define the DCPMM capacity that is invested in system volatile memory.

       ```
       onecli.exe config set IntelOptaneDCPMM.MemoryModePercentage 20
       --imm USERID:PASSW0RD@10.104.195.86
       ```

Where *20* stands for the percentage of capacity that is invested in system volatile memory.

3. Set the DCPMM mode.

```
onecli.exe config set IntelOptaneDCPMM.PersistentMemoryType "App Direct"
--imm USERID:PASSWORD@10.104.195.86
```

Where *App Direct* stands for the DCPMM mode.

– **Persistent Memory Type**

In App Direct Mode and Mixed Memory Mode, the DCPMMs that are connected to the same processor are by default interleaved (displayed as **App Direct**), while memory banks are used in turns. To set them as not interleaved in the Setup Utility, go to **Intel Optane DCPMMs → Goals → Persistent Memory Type [(DCPMM mode)]**, select **App Direct Not Interleaved** and reboot the system.

Note: Setting DCPMM App Direct capacity to not interleaved will turn the displayed App Direct regions from one region per processor to one region per DCPMM.

- **Regions**

After the memory percentage is set and the system is rebooted, regions for the App Direct capacity will be generated automatically. Select this option to view the App Direct regions.

- **Namespaces**

App Direct capacity of DCPMMs requires the following steps before it is truly available for applications.

1. Namespaces must be created for region capacity allocation.
2. Filesystem must be created and formatted for the namespaces in the operating system.

Each App Direct region can be allocated into one namespace. Create namespaces in the following operating systems:

– Windows: Use *Pmem* command.

– Linux: Use *ndctl* command.

– VMware: Reboot the system, and VMware will create namespaces automatically.

After creating namespaces for App Direct capacity allocation, make sure to create and format filesystem in the operating system so that the App Direct capacity is accessible for applications.

- **Security**

– Enable Security

Attention: By default, DCPMM security is disabled. Before enabling security, make sure all the country or local legal requirements regarding data encryption and trade compliance are met. Violation could cause legal issues.

DCPMMs can be secured with passphrases. Two types of passphrase protection scope are available for DCPMM:

– **Platform:** Choose this option to run security operation on all the installed DCPMM units at once. A platform passphrase is stored and automatically applied to unlock DCPMMs before operating system starts running, but the passphrase still has to be disabled manually for secure erase.

Alternatively, enable/disable platform level security with the following commands in OneCLI:

- Enable security:

1. Enable security.

```
onecli.exe config set IntelOptaneDCPMM.SecurityOperation "Enable Security"
--imm USERID:PASSWORD@10.104.195.86
```

2. Set the security passphrase.

```
onecli.exe config set IntelOptaneDCPMM.SecurityPassphrase "123456"
--imm USERID:PASSWORD@10.104.195.86
```

Where *123456* stands for the passphrase.

3. Reboot the system.

- Disable security:
  1. Disable security.

     ```
     onecli.exe config set IntelOptaneDCPMM.SecurityOperation "Disable Security"
     --imm USERID:PASSWORD@10.104.195.86
     ```

  2. Enter passphrase.

     ```
     onecli.exe config set IntelOptaneDCPMM.SecurityPassphrase "123456"
     --imm USERID:PASSWORD@10.104.195.86
     ```

  3. Reboot the system.

– **Single DCPMM:** Choose this option to run security operation on one or more selected DCPMM units.

Notes:

- Single DCPMM passphrases are not stored in the system, and security of the locked units needs to be disabled before the units are available for access or secure erase.
- Always make sure to keep records of the slot number of locked DCPMMs and corresponding passphrases. In the case the passphrases are lost or forgotten, the stored data cannot be backed up or restored, but you can contact Lenovo service for administrative secure erase.
- After three failed unlocking attempts, the corresponding DCPMMs enter “exceeded” state with a system warning message, and the DCPMM unit can only be unlocked after the system is rebooted.

To enable passphrase, go to **Security → Press to Enable Security**.

– Secure Erase

Note: If the DCPMMs to be secure erased are protected with a passphrase, make sure to disable security and reboot the system before performing secure erase.

Secure erase cleanses all the data that is stored in the DCPMM unit, including encrypted data. This data deletion method is recommended before returning or disposing a malfunctioning unit, or changing DCPMM mode. To perform secure erase, go to **Security → Press to Secure Erase**.

Alternatively, perform platform level secure erase with the following command in OneCLI:

```
onecli.exe config set IntelOptaneDCPMM.SecurityOperation "Secure Erase Without Passphrase"
--imm USERID:PASSWORD@10.104.195.86
```

- **DCPMM Configuration**

DCPMM contains spared internal cells to stand in for the failed ones. When the spared cells are exhausted to 0%, there will be an error message, and it is advised to back up data, collect service log, and contact Lenovo support.

There will also be a warning message when the percentage reaches 1% and a selectable percentage (10% by default). When this message appears, it is advised to back up data and run DCPMM diagnostics (see https://sysmgt.lenovofiles.com/help/topic/LXPM/running_diagnostics.html). To adjust the selectable percentage that the warning message requires, go to **Intel Optane DCPMMs → DCPMM Configuration**, and input the percentage.

Alternatively, change the selectable percentage with the following command in OneCLI:

```
onecli.exe config set IntelOptaneDCPMM.PercentageRemainingThresholds 20
--imm USERID:PASSWORD@10.104.195.86
```

Where *20* is the selectable percentage.

Update the firmware

Several options are available to update the firmware for the server.

You can use the tools listed here to update the most current firmware for your server and the devices that are installed in the server.

Note: Lenovo typically releases firmware in bundles called UpdateXpress System Packs (UXSPs). To ensure that all of the firmware updates are compatible, you should update all firmware at the same time. If you are updating firmware for both the Lenovo XClarity Controller and UEFI, update the firmware for Lenovo XClarity Controller first.

Best practices related to updating firmware is available at the following location:

http://lenovopress.com/LP0656

Important terminology

- **In-band update**. The installation or update is performed using a tool or application within an operating system that is executing on the server's core CPU.
- **Out-of-band update**. The installation or update is performed by the Lenovo XClarity Controller collecting the update and then directing the update to the target subsystem or device. Out-of-band updates have no dependency on an operating system executing on the core CPU. However, most out-of-band operations do require the server to be in the S0 (Working) power state.
- **On-Target update.** The installation or update is initiated from an Operating System executing on the server's operating system.
- **Off-Target update.** The installation or update is initiated from a computing device interacting directly with the server's Lenovo XClarity Controller.
- **UpdateXpress System Packs (UXSPs)**. UXSPs are bundled updates designed and tested to provide the interdependent level of functionality, performance, and compatibility. UXSPs are server machine-type specific and are built (with firmware and device driver updates) to support specific Windows Server, Red Hat Enterprise Linux (RHEL) and SUSE Linux Enterprise Server (SLES) operating system distributions. Machine-type-specific firmware-only UXSPs are also available.

See the following table to determine the best Lenovo tool to use for installing and setting up the firmware:

Note: The server UEFI settings for option ROM must be set to **Auto** or **UEFI** to update firmware using Lenovo XClarity Administrator or Lenovo XClarity Essentials. For more information, see the following Tech Tip:

https://datacentersupport.lenovo.com/us/en/solutions/ht506118

Tool	In-band update	Out-of-band update	On-target update	Off-target update	Graphical user interface	Command-line interface	Supports UXSPs
Lenovo XClarity Provisioning Manager Limited to core system firmware only.	√			√	√		√
Lenovo XClarity Controller Supports core system firmware and most advanced I/O option firmware updates		√		√	√	√	
Lenovo XClarity Essentials OneCLI Supports all core system firmware, I/O firmware, and installed operating system driver updates	√	√				√	√
Lenovo XClarity Essentials UpdateXpress Supports all core system firmware, I/O firmware, and installed operating system driver updates	√	√			√		√
Lenovo XClarity Essentials Bootable Media Creator Supports core system firmware and I/O firmware updates. You can update the Microsoft Windows operating system, but device drivers are not included on the bootable image	√				√	√	√
Lenovo XClarity Administrator Supports core system firmware and I/O firmware updates	√	√		√	√		

- **Lenovo XClarity Provisioning Manager**

  From Lenovo XClarity Provisioning Manager, you can update the Lenovo XClarity Controller firmware, the UEFI firmware, and the Lenovo XClarity Provisioning Manager software.

  Note: By default, the Lenovo XClarity Provisioning Manager Graphical User Interface is displayed when you press F1. If you have changed that default to be the text-based system setup, you can bring up the Graphical User Interface from the text-based system setup interface.

Additional information about using Lenovo XClarity Provisioning Manager to update firmware is available at:

http://sysmgt.lenovofiles.com/help/topic/LXPM/platform_update.html

- **Lenovo XClarity Controller**

  If you need to install a specific update, you can use the Lenovo XClarity Controller interface for a specific server.

  Notes:

  – To perform an in-band update through Windows or Linux, the operating system driver must be installed and the Ethernet-over-USB (sometimes called LAN over USB) interface must be enabled.

    Additional information about configuring Ethernet over USB is available at:

    http://sysmgt.lenovofiles.com/help/topic/com.lenovo.systems.management.xcc.doc/NN1ia_c_configuringUSB.html

  – If you update firmware through the Lenovo XClarity Controller, make sure that you have downloaded and installed the latest device drivers for the operating system that is running on the server.

  Specific details about updating firmware using Lenovo XClarity Controller are available at:

  http://sysmgt.lenovofiles.com/help/topic/com.lenovo.systems.management.xcc.doc/NN1ia_c_manageserverfirmware.html

- **Lenovo XClarity Essentials OneCLI**

  Lenovo XClarity Essentials OneCLI is a collection of command line applications that can be used to manage Lenovo servers. Its update application can be used to update firmware and device drivers for your servers. The update can be performed within the host operating system of the server (in-band) or remotely through the BMC of the server (out-of-band).

  Specific details about updating firmware using Lenovo XClarity Essentials OneCLI is available at:

  http://sysmgt.lenovofiles.com/help/topic/toolsctr_cli_lenovo/onecli_c_update.html

- **Lenovo XClarity Essentials UpdateXpress**

  Lenovo XClarity Essentials UpdateXpress provides most of OneCLI update functions through a graphical user interface (GUI). It can be used to acquire and deploy UpdateXpress System Pack (UXSP) update packages and individual updates. UpdateXpress System Packs contain firmware and device driver updates for Microsoft Windows and for Linux.

  You can obtain Lenovo XClarity Essentials UpdateXpress from the following location:

  https://datacentersupport.lenovo.com/solutions/lnvo-xpress

- **Lenovo XClarity Essentials Bootable Media Creator**

  You can use Lenovo XClarity Essentials Bootable Media Creator to create bootable media that is suitable for applying firmware updates, running preboot diagnostics, and deploying Microsoft Windows operating systems.

  You can obtain Lenovo XClarity Essentials BoMC from the following location:

  https://datacentersupport.lenovo.com/solutions/lnvo-bomc

- **Lenovo XClarity Administrator**

  If you are managing multiple servers using the Lenovo XClarity Administrator, you can update firmware for all managed servers through that interface. Firmware management is simplified by assigning firmware-compliance policies to managed endpoints. When you create and assign a compliance policy to managed endpoints, Lenovo XClarity Administrator monitors changes to the inventory for those endpoints and flags any endpoints that are out of compliance.

  Specific details about updating firmware using Lenovo XClarity Administrator are available at:

  http://sysmgt.lenovofiles.com/help/topic/com.lenovo.lxca.doc/update_fw.html

Chapter 2. DCPMM installation order for ThinkSystem compute nodes

Follow the population table in this section to install the DCPMMs and DIMMs.

SN550 DCPMM and DIMM configuration

Memory performance depends on several variables, such as memory mode, memory speed, memory ranks, memory population and processor.

Information about optimizing memory performance and configuring memory is available at the Lenovo Press website:

https://lenovopress.com/servers/options/memory

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

Specific information about the required installation order of memory modules in your compute node based on the system configuration and memory mode that you are implementing is shown below.

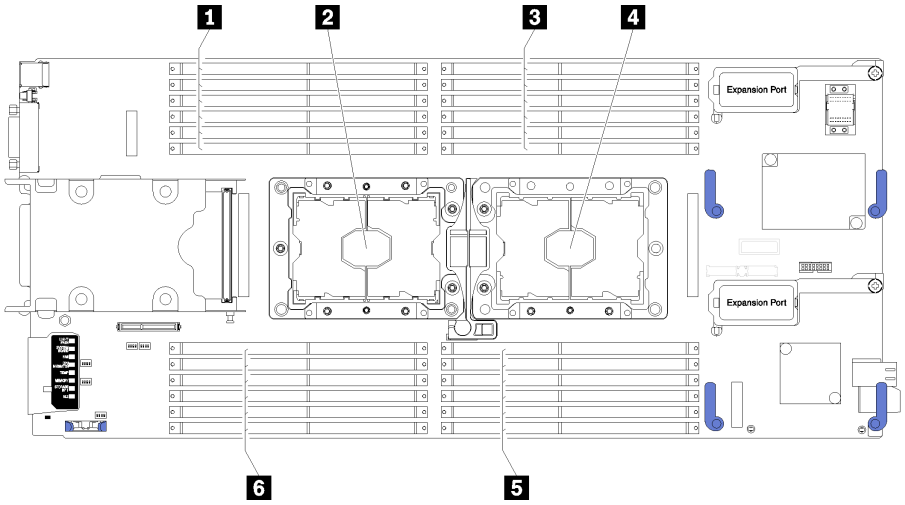

Figure 1. DIMM and processor location

Table 1. DIMM and processor location

1 DIMM connectors 13–18	4 Processor socket 1
2 Processor socket 2	5 DIMM connectors 7–12
3 DIMM connectors 1–6	6 DIMM connectors 19–24

Table 2. Channel and slot information of DIMMs around processor 1 and 2

The memory-channel configuration table is a three-column table that shows the relationship between the processors, memory controllers, memory channels, slot number and the DIMM connectors.

Table 2. Channel and slot information of DIMMs around processor 1 and 2 (continued)

Integrated Memory Controller (iMC)	Controller 0						Controller 1					
Channel	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slot	0	1	0	1	0	1	1	0	1	0	1	0
DIMM connector (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM connector (processor 2)	24	23	22	21	20	19	18	17	16	15	14	13

SN550 Memory Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your node. Below is the information of Memory Mode.

Note: Before installing DCPMM, refer to “SN550 DCPMM and DIMM configuration” on page 9 for the requirements.

Table 3. Three categories of DIMM

DIMM Category	DDR4 Type	Capacity
D1	RDIMM	All density of DDR4 more than 32 GB
D2	RDIMM	16 GB or 32 GB RDIMM

Following are all the combinations that are supported in this solution.

Memory Mode with one processor

Table 4. Memory Mode with one processor

D1–D2: Refer to Table 3 “Three categories of DIMM” on page 10.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
2 DCPMMs and 6 DIMMs	D2		D2		D2	**P**	**P**	D2		D2		D2
4 DCPMMs and 6 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
6 DCPMMs and 6 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1
2 DCPMMs and 4 DIMMs	**P**		D1		D1			D1		D1		**P**

Note: 2 DCPMMs and 4 DIMMs: one DIMM per processor channel configuration.

Table 5. Supported DCPMM capacity in Memory Mode with one processor

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
2	**6**	**L**		√	√
		M		√	√
		Other		√	
4	**6**	**L**		√	√

Table 5. Supported DCPMM capacity in Memory Mode with one processor (continued)

		M		√	
		Other			
6	**6**	**L**	√	√	√
		M	√	√	
		Other	√		
2	**4**	**L**		√	√
		M		√	√
		Other		√	

Memory Mode with two processors

Table 6. Memory Mode with two processors

D1–D2: Refer to Table 3 “Three categories of DIMM” on page 10.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1												Processor 2											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
4 DCPMMs and 12 DIMMs	D2		D2		D2	**P**	**P**	D2		D2		D2	D2		D2		D2	**P**	**P**	D2		D2		D2
8 DCPMMs and 12 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
12 DCPMMs and 12 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1
4 DCPMMs and 8 DIMMs	**P**		D1		D1			D1		D1		**P**	**P**		D1		D1			D1		D1		**P**

Note: 4 DCPMMs and 8 DIMMs: one DIMM per processor channel configuration.

Table 7. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
4	**12**	**L**		√	√
		M		√	√
		Other		√	
8	**12**	**L**		√	√
		M		√	
		Other			
12	**12**	**L**	√	√	√
		M	√	√	
		Other	√		
4	**8**	**L**		√	√

Table 7. Supported DCPMM capacity in Memory Mode with two processors (continued)

		M		√	√
		Other		√	

SN850 DCPMM and DIMM configuration

In Memory Mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache. Only DCPMM capacity is displayed as system memory in this mode.

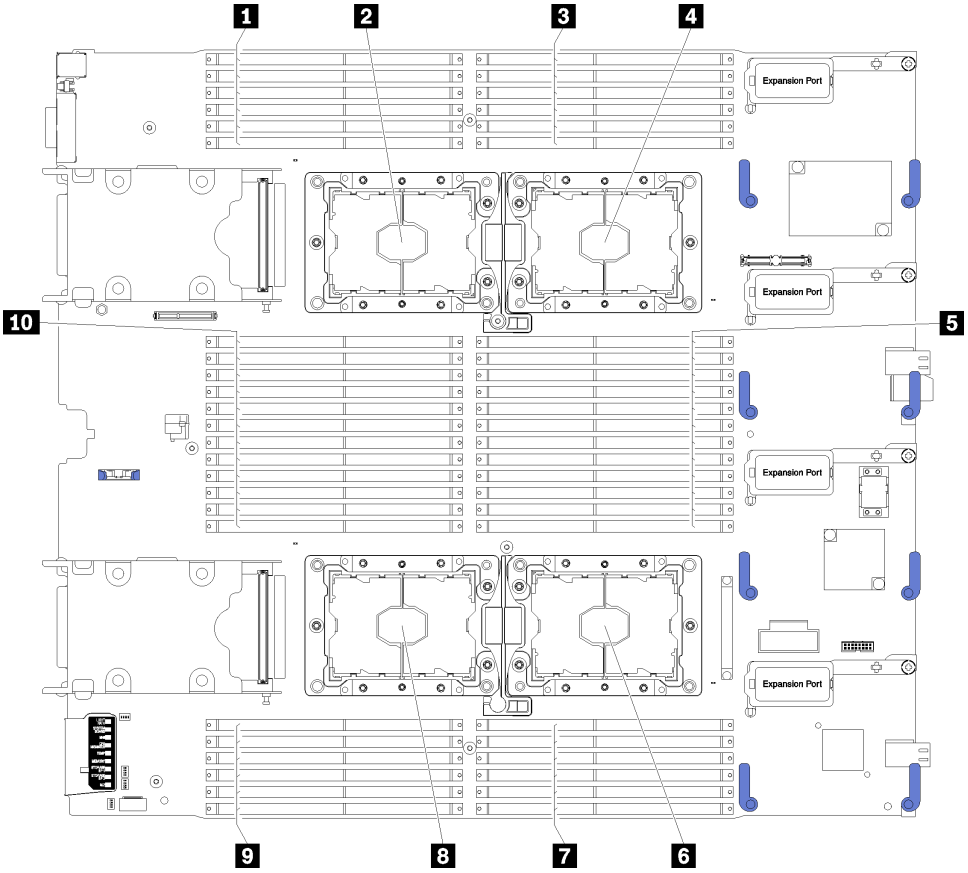

Figure 2. Processor and memory module layout

Table 8. Processor and memory module layout

1 DIMM 25 – 30	6 Processor socket 2
2 Processor socket 3	7 DIMM 19 – 24
3 DIMM 1 – 6	8 Processor socket 4
4 Processor socket 1	9 DIMM 43 – 48
5 DIMM 7 – 18	10 DIMM 31 – 42

Table 9. Channel and slot information of DIMMs around processor 1 and 2

Memory controllers	Controller 0						Controller 1					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM numbers (processor 2)	13	14	15	16	17	18	19	20	21	22	23	24

Table 10. Channel and slot information of DIMMs around processor 3 and 4

Memory controllers	Controller 1						Controller 0					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 3)	25	26	27	28	29	30	31	32	33	34	35	36
DIMM numbers (processor 4)	37	38	39	40	41	42	43	44	45	46	47	48

The memory mode DIMM population sequences for each supported processor configuration are:

- “SN850 Memory Mode with two processors” on page 14
- “SN850 Memory Mode with four processors” on page 16

SN850 Memory Mode with two processors

Memory module installation order for Memory Mode with two processors installed in the compute node.

Table 11. Three categories of DIMM

DIMM Category	DDR4 Type	Capacity
D1	RDIMM	All density of DDR4 more than 32 GB
D2	RDIMM	16 GB or 32 GB RDIMM

The following table shows the DIMM population sequence for Memory Mode when two processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 12. Memory Mode with two processors

D1–D2: Refer to Table 11 “Three categories of DIMM” on page 14.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1												Processor 2											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
4 DCPMMs and 12 DIMMs	D2		D2		D2	**P**	**P**	D2		D2		D2	D2		D2		D2	**P**	**P**	D2		D2		D2
8 DCPMMs and 12 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
12 DCPMMs and 12 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1
4 DCPMMs and 8 DIMMs	**P**		D1		D1			D1		D1		**P**	**P**		D1		D1			D1		D1		**P**

Note: 4 DCPMMs and 8 DIMMs: one DIMM per processor channel configuration.

Table 13. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
4	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
8	**12**	**L**	√	√	√
		M	√	√	
		Other	√		
12	**12**	**L**	√	√	√
		M	√	√	
		Other	√		

Table 13. Supported DCPMM capacity in Memory Mode with two processors (continued)

4	**8**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

SN850 Memory Mode with four processors

Memory module installation order for Memory Mode with four processors installed in the compute node.

Table 14. Three categories of DIMM

DIMM Category	DDR4 Type	Capacity
D1	RDIMM	All density of DDR4 more than 32GB
D2	RDIMM	16GB or 32GB RDIMM

The following tables show the DIMM population sequence for independent Memory Mode when four processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 15. Memory Mode with four processors (Processors 1 and 2)

D1–D2: Refer to Table 14 “Three categories of DIMM” on page 16.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1												Processor 2											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
8 DCPMMs and 24 DIMMs	D2		D2		D2	**P**	**P**	D2		D2		D2	D2		D2		D2	**P**	**P**	D2		D2		D2
16 DCPMMs and 24 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
24 DCPMMs and 24 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1
8 DCPMMs and 16 DIMMs	**P**		D1		D1			D1		D1		**P**	**P**		D1		D1			D1		D1		**P**

Note: 8 DCPMMs and 16 DIMMs: one DIMM per processor channel configuration.

Related DIMM population sequences for four processor systems:

To continue populating processor 3 and 4 DIMMs for system, see Table 16 “Memory Mode with four processors (Processors 3 and 4)” on page 17.

Table 16. Memory Mode with four processors (Processors 3 and 4)

D1–D2: Refer to Table 14 “Three categories of DIMM” on page 16.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 3												Processor 4											
	25	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**
8 DCPMMs and 24 DIMMs	D2		D2		D2	**P**	**P**	D2		D2		D2	D2		D2		D2	**P**	**P**	D2		D2		D2
16 DCPMMs and 24 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
24 DCPMMs and 24 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1
8 DCPMMs and 16 DIMMs	**P**		D1		D1			D1		D1		**P**	**P**		D1		D1			D1		D1		**P**

Note: 8 DCPMMs and 16 DIMMs: one DIMM per processor channel configuration.

Related DIMM population sequences for four processor systems:

To continue populating processor 1 and 2 DIMMs for system, see Table 15 “Memory Mode with four processors (Processors 1 and 2)” on page 16.

Table 17. Supported DCPMM capacity in Memory Mode with four processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
8	**24**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
16	**24**	**L**	√	√	√
		M	√	√	
		Other	√		
24	**24**	**L**	√	√	√
		M	√	√	
		Other	√		
8	**16**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

Chapter 3. DCPMM installation order for ThinkSystem high-density servers

Follow the population table in this section to install the DCPMMs and DIMMs.

SD530 DCPMM and DIMM configuration

This section contains information of how to install DCPMMs and DRAM DIMMs properly.

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Intel Xeon Platinum **82**80M*

  If the presently installed processors do not support DCPMMs, replace them with the processors that support DCPMMs.
- Supported memory capacity range varies with the following types of processors.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon 5215**L***)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8280**M***)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

The following illustration shows the location of the DIMM connectors on the system board.

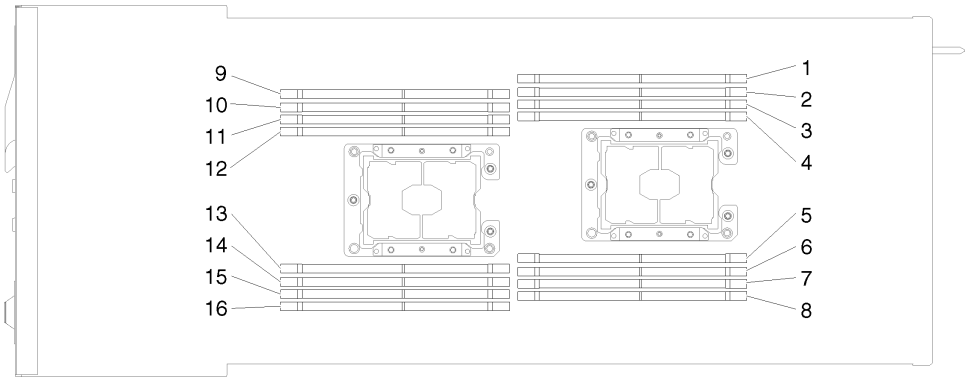

Figure 3. The location of the DIMM connectors on the system board

SD530 Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache.

Memory Mode - one processor

Table 18. Memory Mode with one processor

- **D**: DRAM DIMMs
- **P**: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
2 DCPMMs and 6 DIMMs	D	D	D	**P**	**P**	D	D	D

Table 19. Supported DCPMM capacity in Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
2	**6**	**L**		√	√
		M		√	√
		Other		√	

Memory Mode - two processors

Table 20. Memory Mode with two processors

- **D**: DRAM DIMMs
- **P**: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1								Processor 2							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**18**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
4 DCPMMs and 12 DIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 21. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	**12**	**L**		√	√
		M		√	
		Other			

SD530 App Direct Mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

App Direct Mode - one processor

Table 22. App Direct Mode with one processor

- **D**: DRAM DIMMs
- **P**: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1 DCPMM and 6 DIMMs	D	D	D		**P**	D	D	D
2 DCPMMs and 6 DIMMs	D	D	D	**P**	**P**	D	D	D

Table 23. Supported DCPMM capacity in App Direct Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**6**	**L**	√	√	
		M	√	√	
		Other	√	√	

App Direct Mode - two processors

Table 24. App Direct Mode with two processors

- **D**: DRAM DIMMs
- **P**: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1								Processor 2							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
1 DCPMM and 12 DIMMs	D	D	D		**P**	D	D	D	D	D	D			D	D	D
2 DCPMMs and 12 DIMMs	D	D	D		**P**	D	D	D	D	D	D		**P**	D	D	D
4 DCPMMs and 12 DIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 25. Supported DCPMM capacity in App Direct Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**12**	**L**	√	√	√
		M	√	√	√

Table 25. Supported DCPMM capacity in App Direct Mode with two processors (continued)

		Other	√	√	
4	**12**	**L**	√	√	√
		M	√	√	
		Other	√		

SD530 Mixed Memory Mode

In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

Mixed Memory Mode - one processor

Table 26. Mixed Memory Mode with one processor

- **D**: DRAM DIMMs
- **P**: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
2 DCPMMs and 6 DIMMs	D	D	D	**P**	**P**	D	D	D

Table 27. Supported DCPMM capacity in Mixed Memory Mode with one processor

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
2	**6**	**L**			√
		M			√
		Other			

Mixed Memory Mode - two processors

Table 28. Mixed Memory Mode with two processors

- **D**: DRAM DIMMs
- **P**: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1								Processor 2							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**18**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
4 DCPMMs and 12 DIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 29. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
4	**12**	**L**			√
		M			

Table 29. Supported DCPMM capacity in Mixed Memory Mode with two processors (continued)

		Other			

SD650 DCPMM and DIMM configuration

This section contains information of how to install DC Persistent Memory Module (DCPMM) and DRAM DIMMs.

For more information about the processors compatibility, see http://www.lenovo.com/us/en/serverproven/.

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processors with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***6*** or a larger number.
  - The second digit is ***2***.

  Example: *Intel Xeon **62**62V* and *Intel Xeon Platinum **82**60M*

  If the presently installed processors do not support DCPMMs, replace them with the processors that support DCPMMs.
- Supported memory capacity range varies with the following types of DCPMMs.
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8260**M***) support up to 2 TB of memory capacity per processor
  - **No suffix:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 6230*) support up to 1 TB of memory capacity per processor

  The following illustration shows the location of the DIMM connectors on the system board.

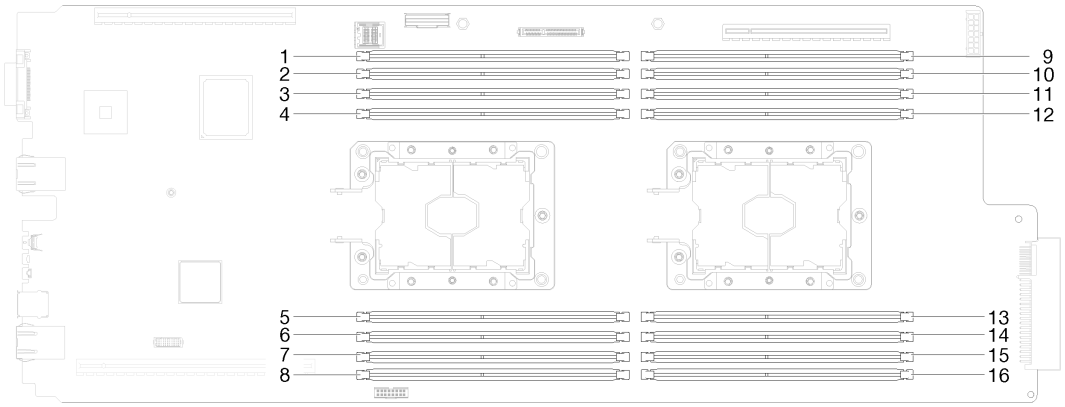

Figure 4. The location of the DIMM connectors on the system board

SD650 DCPMM installation order

This section contains information of how to install DC Persistent Memory Module (DCPMM) and DRAM DIMMs.

For more information about the processors compatibility, see http://www.lenovo.com/us/en/serverproven/.

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processors with description meeting *both* of the following requirements support DCPMMs.

– The first digit is ***6*** or a larger number.
– The second digit is ***2***.

Example: *Intel Xeon **62**62V* and *Intel Xeon Platinum **82**60M*

If the presently installed processors do not support DCPMMs, replace them with the processors that support DCPMMs.

- Supported memory capacity range varies with the following types of DCPMMs.
  – **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8260**M***) support up to 2 TB of memory capacity per processor
  – **No suffix:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 6230*) support up to 1 TB of memory capacity per processor

The following illustration shows the location of the DIMM connectors on the system board.

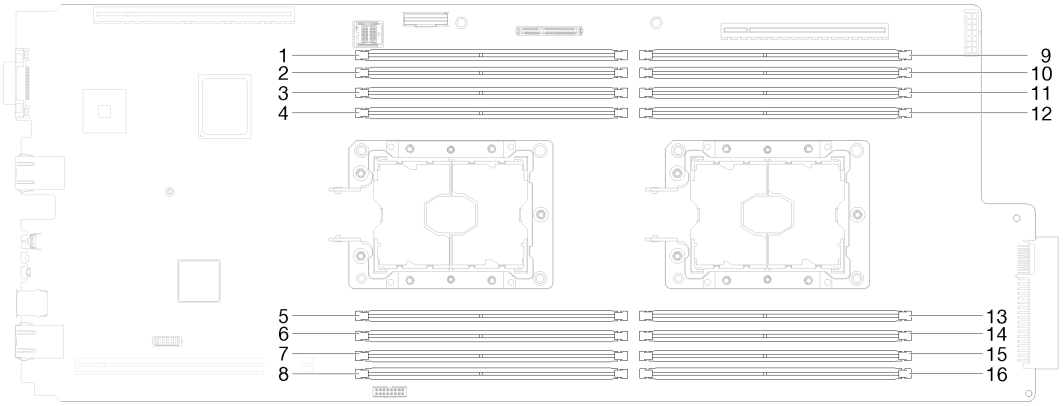

Figure 5. The location of the DIMM connectors on the system board

Table 30. Supported DCPMM capacity in DCPMM population configuration

App direct mode					
Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
1	**12**	**M**	√	√	√
		No suffix	√	√	√
2	**12**	**M**	√	√	√
		No suffix	√	√	√ Note 1
4	**12**	**M**	√	√	√
		No suffix	√	√ Note 2	
Notes: 1. 12x128 GB 3DS RDIMM + 2x512 GB DCPMM is not supported. 2. 12x128 GB 3DS RDIMM + 4x256 GB DCPMM is not supported.					
Memory mode					
Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**

Table 30. Supported DCPMM capacity in DCPMM population configuration (continued)

4	12	M	√	√	√
		No suffix	√	√	
Mixed memory mode					
Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
4	12	M	√	√	√
		No suffix	√	√	

To install DC Persistent Memory Module (DCPMM), refer to the following combinations:
- DCPMM population sequence - Memory mode
- DCPMM population sequence - App direct mode
- DCPMM population sequence - Mix memory mode

DCPMM installation order

DCPMMs shall only be installed on DIMM3, DIMM6, DIMM11 and DIMM14.

Table 31. DCPMM population sequence - Memory mode

DCPMM population sequence - Memory mode																	
Note: **D2: It represents RDIMMs (DIMM density =16GB or 32GB) can be installed on the corresponding DIMM slots.** **P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.**																	
Operation mode	**Con-figura-tion**	**Processor 1**								**Processor 2**							
		DIMM slot								**DIMM slot**							
		8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**
Memory mode	**4 AEPs and 12 DIMMs**	D2	D2	P	D2	D2	P	D2	D2	D2	D2	P	D2	D2	P	D2	D2

Table 32. DCPMM population sequence - App direct mode

DCPMM population sequence - App direct mode																	
Note: **D1: It represents RDIMMs (DIMM density ≥16GB) can be installed on the corresponding DIMM slots.** **P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.**																	
Operation mode	**Con-figura-tion**	**Processor 1**								**Processor 2**							
		DIMM slot								**DIMM slot**							
		8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**
App direct mode (not interleaved)	**1 AEP and 12 DIMMs**	D1	D1	P	D1	D1		D1	D1	D1	D1		D1	D1		D1	D1
App direct mode + Mirroring mode (not interleaved)	**1 AEP and 12 DIMMs**	D1	D1	P	D1	D1		D1	D1	D1	D1		D1	D1		D1	D1
App direct mode (not interleaved)	**2 AEPs and 12 DIMMs**	D1	D1	P	D1	D1		D1	D1	D1	D1	P	D1	D1		D1	D1
App direct mode + Mirroring mode (not interleaved)	**2 AEPs and 12 DIMMs**	D1	D1	P	D1	D1		D1	D1	D1	D1	P	D1	D1		D1	D1
App direct mode (interleaved or not interleaved)	**4 AEPs and 12 DIMMs**	D1	D1	P	D1	D1	P	D1	D1	D1	D1	P	D1	D1	P	D1	D1
App direct mode + Mirroring mode (interleaved or not interleaved)	**4 AEPs and 12 DIMMs**	D1	D1	P	D1	D1	P	D1	D1	D1	D1	P	D1	D1	P	D1	D1

Table 33. DCPMM population sequence - Mix memory mode

DCPMM population sequence - Mix memory mode																	
Note: **D3: It represents RDIMMs (DIMM density ≥16GB, no 3DS LRDIMM) can be installed on the corresponding DIMM slots.** **P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.**																	
Operation mode	**Con-figura-tion**	**Processor 1**								**Processor 2**							
		DIMM slot								**DIMM slot**							
		8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**
Mix memory mode (interleaved or not interleaved)	**4 AEPs and 12 DIMMs**	D3	D3	P	D3	D3	P	D3	D3	D3	D3	P	D3	D3	P	D3	D3

Chapter 4. DCPMM installation order for ThinkSystem rack servers

Follow the population table in this section to install the DCPMMs and DIMMs.

SR570 DCPMM and DIMM configuration

Memory modules must be installed in a specific order based on the memory configuration that you implement on your server.

Your server has 16 memory slots, and supports the following types of memory modules depending on the processors installed:

- For Intel Xeon Skylake processors:
  - TruDDR4 2666, single-rank or dual-rank, 8 GB/16 GB/32 GB RDIMMs
  - TruDDR4 2666, quad-rank, 64 GB LRDIMMs
- For Intel Xeon Cascade Lake processors:
  - TruDDR4 2666, single-rank or dual-rank, 16 GB/32 GB RDIMMs
  - DDR4 2933, single-rank or dual-rank, 8 GB/16 GB/32 GB/64 GB RDIMMs (available by June 2019)
  - 128 GB, 256 GB, or 512 GB DCPMMs

For a list of supported memory options, see: http://www.lenovo.com/us/en/serverproven/

The following illustration helps you to locate the memory slots on the system board.

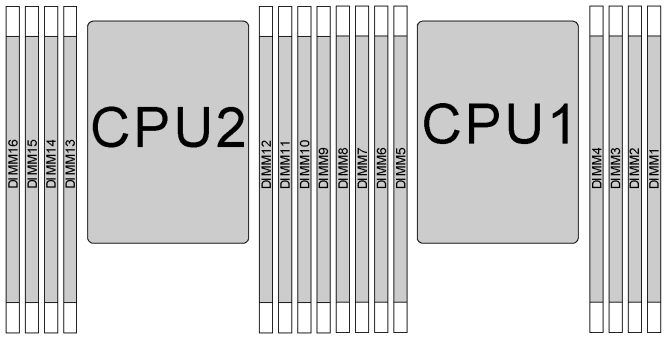

Figure 6. DIMM locations

The following table shows the relationship between the processors, memory controllers, memory channels, slots, and DIMM numbers. For each memory controller, channel 0 has two DIMM slots (slot 0, furthest from the processor, and slot 1, closest to the processor), and channel 1 and channel 2 have only one DIMM slot (slot 0).

Processor	CPU2		CPU1	
Integrated Memory Controller (iMC)	iMC1	iMC0	iMC1	iMC0

Channel (CH)	C-H2	C-H1	CH0		CH0		C-H1	C-H2	C-H2	C-H1	CH0		CH0		C-H1	C-H2
Slot	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0
DIMM number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only processors with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Intel Xeon Platinum **82**80M*

  If the presently installed processors do not support DCPMMs, replace them with the processors that support DCPMMs.
- Supported memory capacity range varies with the following types of processors:
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon 5215**L***)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8280**M***)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

SR570 Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache. Only DCPMM capacity is displayed as system memory in this mode.

Memory Mode with one processor

Table 34. Memory population order in Memory Mode with one processor

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)								
Configuration	**Processor 1**							
	8	7	6	5	4	3	2	1
2 DCPMMs and 6 RDIMMs	D	D	D	**P**	**P**	D	D	D

Table 35. Supported DCPMM capacity in Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM[1]	512 GB DCPMM[2]
2	**6**	**L**		√	√
		M		√	√

Table 35. Supported DCPMM capacity in Memory Mode with one processor (continued)

		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM.

Memory Mode with two processors

Table 36. Memory population order in Memory Mode with two processors

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported

P: DC Persistent Memory Module (DCPMM)

Configuration	**Processor 2**								**Processor 1**							
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
4 DCPMMs and 12 RDIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 37. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**[1]	**512 GB DCPMM**[2]
4	**12**	**L**		√	√
		M		√	√
		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM. To install four 512 GB DCPMMs, ensure that the processor TDP is lower than or equal to 125 watts.

SR570 App Direct Mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory. The total displayed system memory in this mode is the total capacity of DRAM DIMMs.

App Direct mode with one processor

Table 38. Memory population order in App Direct mode with one processor

D: DRAM DIMM; 16 GB, 32 GB, or 64 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)								
Configuration	**Processor 1**							
	8	7	6	5	4	3	2	1
1 DCPMM and 6 RDIMMs	D	D	D		**P**	D	D	D
2 DCPMMs and 6 RDIMMs	D	D	D	**P**	**P**	D	D	D

Table 39. Supported DCPMM capacity in App Direct mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

App Direct mode with two processors

Table 40. Memory population order in App Direct mode with two processors

D: DRAM DIMM; 16 GB, 32 GB, or 64 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)																
Configuration	**Processor 2**								**Processor 1**							
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1 DCPMM and 12 RDIMMs	D	D	D			D	D	D	D	D	D		**P**	D	D	D
2 DCPMMs and 12 RDIMMs	D	D	D		**P**	D	D	D	D	D	D		**P**	D	D	D
4 DCPMMs and 12 RDIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 41. Supported DCPMM capacity in App Direct mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
4	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

Note: To install four 512 GB DCPMMs, ensure that the processor TDP is lower than or equal to 125 watts.

SR570 Mixed Memory Mode

In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

Mixed Memory Mode with one processor

Table 42. Memory population order in Mixed Memory Mode with one processor

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)								
Configuration	**Processor 1**							
	8	7	6	5	4	3	2	1
2 DCPMMs and 6 RDIMMs	D	D	D	**P**	**P**	D	D	D

Table 43. Supported DCPMM capacity in Mixed Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM[1]	512 GB DCPMM[2]
2	**6**	**L**		√	√
		M		√	√
		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM.

Mixed Memory Mode with two processors

Table 44. Memory population order in Mixed Memory Mode with two processors

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)																
Configuration	**Processor 2**								**Processor 1**							
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
4 DCPMMs and 12 RDIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 45. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM[1]	512 GB DCPMM[2]
4	**12**	**L**		√	√
		M		√	√
		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM. To install four 512 GB DCPMMs, ensure that the processor TDP is lower than or equal to 125 watts.

SR590 DCPMM and DIMM configuration

Memory modules must be installed in a specific order based on the memory configuration that you implement on your server.

Your server has 16 memory slots, and supports the following types of memory modules depending on the processors installed:

- For Intel Xeon Skylake processors:
  - TruDDR4 2666, single-rank or dual-rank, 8 GB/16 GB/32 GB RDIMMs
  - TruDDR4 2666, quad-rank, 64 GB LRDIMMs
- For Intel Xeon Cascade Lake processors:
  - TruDDR4 2666, single-rank or dual-rank, 16 GB/32 GB RDIMMs
  - DDR4 2933, single-rank or dual-rank, 8 GB/16 GB/32 GB/64 GB RDIMMs (available by June 2019)
  - 128 GB, 256 GB, or 512 GB DCPMMs

For a list of supported memory options, see: http://www.lenovo.com/us/en/serverproven/

The following illustration helps you to locate the memory slots on the system board.

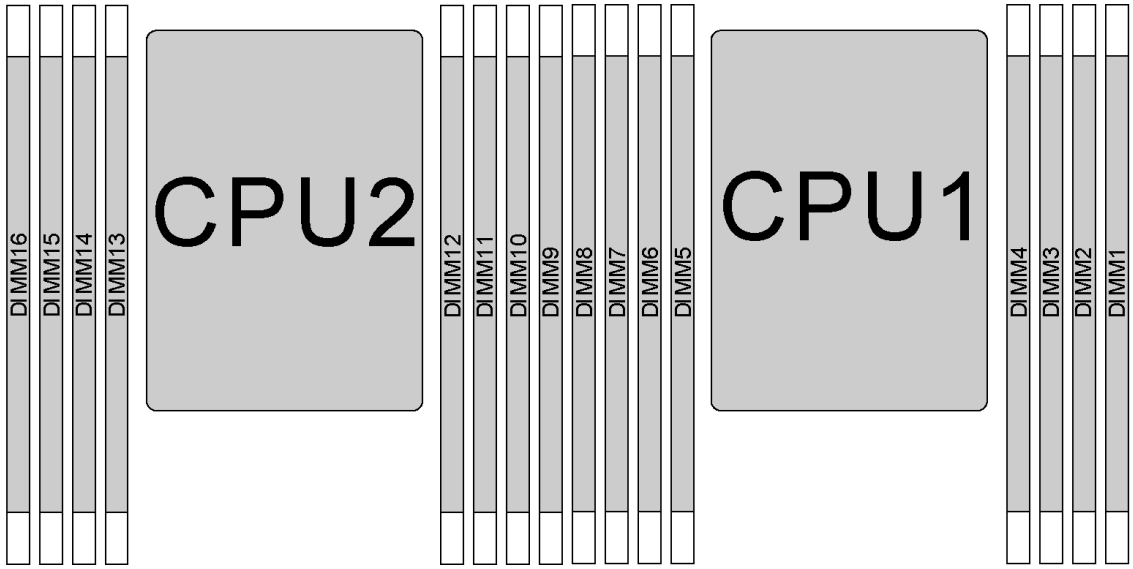

Figure 7. DIMM locations

The following table shows the relationship between the processors, memory controllers, memory channels, slots, and DIMM numbers. For each memory controller, channel 0 has two DIMM slots (slot 0, furthest from the processor, and slot 1, closest to the processor), and channel 1 and channel 2 have only one DIMM slot (slot 0).

Processor	CPU2						CPU1					
Integrated Memory Controller (iMC)	iMC1			iMC0			iMC1			iMC0		
Channel (CH)	C-H2	C-H1	CH0	CH0	C-H1	C-H2	C-H2	C-H1	CH0	CH0	C-H1	C-H2

Slot	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0
DIMM number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only processors with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Intel Xeon Platinum **82**80M*

  If the presently installed processors do not support DCPMMs, replace them with the processors that support DCPMMs.
- Supported memory capacity range varies with the following types of processors:
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon 5215**L***)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8280**M***)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

SR590 Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache. Only DCPMM capacity is displayed as system memory in this mode.

Memory Mode with one processor

Table 46. Memory population order in Memory Mode with one processor

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)								
Configuration	**Processor 1**							
	8	7	6	5	4	3	2	1
2 DCPMMs and 6 RDIMMs	D	D	D	**P**	**P**	D	D	D

Table 47. Supported DCPMM capacity in Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM[1]	512 GB DCPMM[2]
2	**6**	**L**		√	√
		M		√	√

Table 47. Supported DCPMM capacity in Memory Mode with one processor (continued)

		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM.

Memory Mode with two processors

Table 48. Memory population order in Memory Mode with two processors

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported

P: DC Persistent Memory Module (DCPMM)

Configuration	**Processor 2**								**Processor 1**							
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
4 DCPMMs and 12 RDIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 49. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**[1]	**512 GB DCPMM**[2]
4	**12**	**L**		√	√
		M		√	√
		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM. To install four 512 GB DCPMMs, ensure that the processor TDP is lower than or equal to 125 watts.

SR590 App Direct Mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory. The total displayed system memory in this mode is the total capacity of DRAM DIMMs.

App Direct mode with one processor

Table 50. Memory population order in App Direct mode with one processor

D: DRAM DIMM; 16 GB, 32 GB, or 64 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)								
Configuration	**Processor 1**							
	8	7	6	5	4	3	2	1
1 DCPMM and 6 RDIMMs	D	D	D		**P**	D	D	D
2 DCPMMs and 6 RDIMMs	D	D	D	**P**	**P**	D	D	D

Table 51. Supported DCPMM capacity in App Direct mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

App Direct mode with two processors

Table 52. Memory population order in App Direct mode with two processors

D: DRAM DIMM; 16 GB, 32 GB, or 64 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)																
Configuration	**Processor 2**								**Processor 1**							
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1 DCPMM and 12 RDIMMs	D	D	D			D	D	D	D	D	D		**P**	D	D	D
2 DCPMMs and 12 RDIMMs	D	D	D		**P**	D	D	D	D	D	D		**P**	D	D	D
4 DCPMMs and 12 RDIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 53. Supported DCPMM capacity in App Direct mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
4	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

Note: To install four 512 GB DCPMMs, ensure that the processor TDP is lower than or equal to 125 watts.

SR590 Mixed Memory Mode

In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

Mixed Memory Mode with one processor

Table 54. Memory population order in Mixed Memory Mode with one processor

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)								
Configuration	**Processor 1**							
	8	7	6	5	4	3	2	1
2 DCPMMs and 6 RDIMMs	D	D	D	**P**	**P**	D	D	D

Table 55. Supported DCPMM capacity in Mixed Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM[1]	512 GB DCPMM[2]
2	**6**	**L**		√	√
		M		√	√
		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM.

Mixed Memory Mode with two processors

Table 56. Memory population order in Mixed Memory Mode with two processors

D: DRAM DIMM; 16 GB or 32 GB RDIMM supported P: DC Persistent Memory Module (DCPMM)																
Configuration	**Processor 2**								**Processor 1**							
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
4 DCPMMs and 12 RDIMMs	D	D	D	**P**	**P**	D	D	D	D	D	D	**P**	**P**	D	D	D

Table 57. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM[1]	512 GB DCPMM[2]
4	**12**	**L**		√	√
		M		√	√
		Other		√	

Notes:
1. For 256 GB DCPMM, use 16 GB RDIMM.
2. For 512 GB DCPMM, use 16 GB or 32 GB RDIMM. To install four 512 GB DCPMMs, ensure that the processor TDP is lower than or equal to 125 watts.

SR630 DCPMM and DIMM configuration

Memory performance depends on several variables, such as memory mode, memory speed, memory ranks, memory population and processor.

More information about optimizing memory performance and configuring memory is available at the Lenovo Press website:

https://lenovopress.com/servers/options/memory

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

Table 58. Channel and slot information of DIMMs around processor 1 and 2

The memory-channel configuration table is a three-column table that shows the relationship between the processors, memory controllers, memory channels, slot number and the DIMM connectors.

Integrated Memory Controller (iMC)	Controller 0						Controller 1					
Channel	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slot	0	1	0	1	0	1	1	0	1	0	1	0
DIMM connector (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM connector (processor 2)	13	14	15	16	17	18	19	20	21	22	23	24

The following illustration helps you to locate the memory slots on the system board.

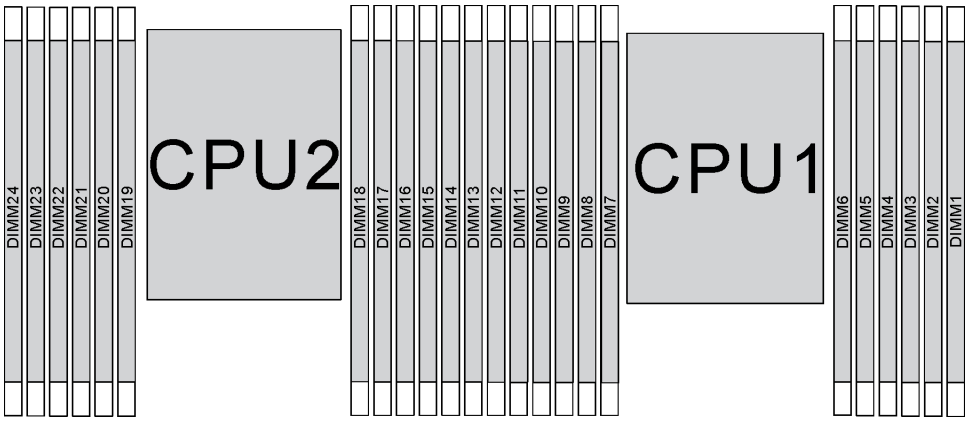

Figure 8. DIMM locations

SR630 Memory Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your node. Below is the information of memory mode.

Table 59. Four categories of DIMM

DIMM Category	DDR4 Type		Capacity
D1	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM
D2	RDIMM	3DS RDIMM	All density of DDR4 more than 32 GB
D3	RDIMM		16 GB or 32 GB RDIMM
D4	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM

Following are all the combinations that are supported in this solution.

Memory Mode with one processor

Table 60. Memory Mode with one processor

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1											
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
2 DCPMMs and 4 DIMMs	**P**		D2		D2			D2		D2		**P**
2 DCPMMs and 6 DIMMs	D3		D3		D3	**P**	**P**	D3		D3		D3
4 DCPMMs and 6 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
6 DCPMMs and 6 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 61. Supported DCPMM capacity in Memory Mode with one processor

Total DCPM-Ms	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
2	**4**	**L**		√[2]	√[4]
		M		√[2]	√[4]
		Other		√[2]	
2	**6**	**L**		√[1]	√[3]
		M		√[1]	√[3]
		Other		√[1]	
4	**6**	**L**		√[2]	√[4]
		M		√[2]	
		Other			
6	**6**	**L**	√[2]	√[4]	√[5]
		M	√[2]	√[4]	
		Other	√[2]		

Notes:

1. Supported DIMM capacity is 16 GB.
2. Supported DIMM capacity is 32 GB.
3. Supported DIMM capacity is up to 32 GB.
4. Supported DIMM capacity is 32 GB to 64 GB.
5. Supported DIMM capacity is 32 GB to 128 GB.

Memory Mode with two processors

Table 62. Memory Mode with two processors

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 2												Processor 1											
	24	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
4 DCPMMs and 8 DIMMs	**P**		D-2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
4 DCPMMs and 12 DIMMs	D3		D-3		D3	**P**	**P**	D3		D3		D3	D3		D3		D3	**P**	**P**	D3		D3		D3
8 DCPMMs and 12 DIMMs	D2		D-2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
12 DCPMMs and 12 DIMMs	D2	**P**	D-2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 63. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	**8**	**L**		√[2]	√[4]
		M		√[2]	√[4]
		Other		√[2]	
4	**12**	**L**		√[1]	√[3]
		M		√[1]	√[3]
		Other		√[1]	
8	**12**	**L**		√[2]	√[4]
		M		√[2]	
		Other			
12	**12**	**L**	√[2]	√[4]	√[5]
		M	√[2]	√[4]	
		Other	√[2]		

Notes:

1. Supported DIMM capacity is 16 GB.
2. Supported DIMM capacity is 32 GB.
3. Supported DIMM capacity is up to 32 GB.
4. Supported DIMM capacity is 32 GB to 64 GB.
5. Supported DIMM capacity is 32 GB to 128 GB.

SR630 App Direct Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your system. Follow the information of App Direct Mode as below.

Table 64. Four categories of DIMM

DIMM Category	DDR4 Type		Capacity
D1	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM
D2	RDIMM	3DS RDIMM	All density of DDR4 more than 32 GB
D3	RDIMM		16 GB or 32 GB RDIMM
D4	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM

Following are all the combinations that are supported in this solution.

App Direct Mode with one processor

Note: When adding one or more DCPMMs and DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 65. App Direct Mode with one processor

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1											
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
1 DCPMM and 6 DIMMs	D1		D1		D1	**P**		D1		D1		D1
2 DCPMMs and 4 DIMMs	**P**		D1		D1			D1		D1		**P**
2 DCPMMs and 6 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1
2 DCPMMs and 8 DIMMs	**P**		D1	D1	D1	D1	D1	D1	D1	D1		**P**
4 DCPMMs and 6 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
6 DCPMMs and 6 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1

Table 66. Supported DCPMM capacity in App Direct Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√[2]
2	**4**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
2	**6**	**L**	√	√	√
		M	√	√	√

Table 66. Supported DCPMM capacity in App Direct Mode with one processor (continued)

		Other	√	√[2]	
2	**8**	**L**	√	√	√
		M	√	√	√
		Other	√[2]	√[2]	
4	**6**	**L**	√	√	√
		M	√	√	
		Other	√[2]		
6	**6**	**L**	√	√	√
		M	√	√[2]	
		Other	√[1]		

Notes:

1. Supported DIMM capacity is up to 32 GB.
2. Supported DIMM capacity is up to 64 GB.

App Direct Mode with two processors

Note: When adding one or more DCPMMs and DIMMs during a memory upgrade, you might need to move other DCPMMs and DIMMs that are already installed to new locations.

Table 67. App Direct Mode with two processors

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 2												Processor 1											
	24	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
1 DCPMM and 12 DIMMs	D1		D1		D1			D1		D1		D1	D1		D1		D1		**P**	D1		D1		D1
2 DCPMMs and 12 DIMMs	D1		D1		D1		**P**	D1		D1		D1	D1		D1		D1		**P**	D1		D1		D1
4 DCPMMs and 8 DIMMs	**P**		D1		D1			D1		D1		**P**	**P**		D1		D1			D1		D1		**P**
4 DCPMMs and 12 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
4 DCPMMs and 16 DIMMs	**P**		D1	D1	D1	D1	D1	D1	D1	D1		**P**	**P**		D1	D1	D1	D-1	D1	D1	D-1	D1		**P**
8 DCPMMs and 12 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
12 DCPMMs and 12 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1

Table 68. Supported DCPMM capacity in App Direct Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	12	L	√	√	√
		M	√	√	√
		Other	√	√	√[2]
2	12	L	√	√	√
		M	√	√	√
		Other	√	√	√[2]
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√[2]	
4	16	L	√	√	√
		M	√	√	√
		Other	√[2]	√[2]	
8	12	L	√	√	√
		M	√	√	
		Other	√[2]		
12	12	L	√	√	√
		M	√	√[2]	
		Other	√[1]		

Notes:

1. Supported DIMM capacity is up to 32 GB.
2. Supported DIMM capacity is up to 64 GB.

SR630 Mixed Memory Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your node. Below is the information of mixed mode.

Table 69. Four categories of DIMM

DIMM Category	DDR4 Type		Capacity
D1	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM
D2	RDIMM	3DS RDIMM	All density of DDR4 more than 32 GB

Table 69. Four categories of DIMM (continued)

D3	RDIMM		16 GB or 32 GB RDIMM
D4	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM

Following are all the combinations that are supported in this solution.

Mixed Memory Mode with one processor

Note: When adding one or more DCPMMs and DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 70. Mixed Memory Mode with one processor

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1											
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
2 DCPMMs and 4 DIMMs	**P**		D4		D4			D4		D4		**P**
2 DCPMMs and 6 DIMMs	D4		D4		D4	**P**	**P**	D4		D4		D4
4 DCPMMs and 6 DIMMs	D4		D4	**P**	D4	**P**	**P**	D4	**P**	D4		D4
6 DCPMMs and 6 DIMMs	D4	**P**	D4	**P**	D4	**P**	**P**	D4	**P**	D4	**P**	D4

Table 71. Supported DCPMM capacity in Mixed Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
2	**4**	**L**		√[1]	√[2]
		M		√[1]	√[2]
		Other		√[1]	
2	**6**	**L**		√[1]	√[2]
		M		√[1]	√[2]
		Other		√[1]	
4	**6**	**L**	√[1]	√[2]	√[3]
		M	√[1]	√[2]	
		Other	√[1]		
6	**6**	**L**	√[1]	√[2]	√[3]
		M	√[1]	√[2]	
		Other	√[1]		

Notes:

1. Supported DIMM capacity is 16 GB.

2. Supported DIMM capacity is up to 32 GB.
3. Supported DIMM capacity is up to 64 GB.

Mixed Memory Mode with two processors

Table 72. Mixed Memory Mode with two processors

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 2												Processor 1											
	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
4 DCPMMs and 8 DIMMs	**P**		D-4		D4			D4		D4		**P**	**P**		D4		D4			D4		D4		**P**
4 DCPMMs and 12 DIMMs	D4		D-4		D4	**P**	**P**	D4		D4		D4	D4		D4		D4	**P**	**P**	D4		D4		D4
8 DCPMMs and 12 DIMMs	D4		D-4	**P**	D4	**P**	**P**	D4	**P**	D4		D4	D4		D4	**P**	D4	**P**	**P**	D4	**P**	D4		D4
12 DCPMMs and 12 DIMMs	D4	**P**	D-4	**P**	D4	**P**	**P**	D4	**P**	D4	**P**	D4	D4	**P**	D4	**P**	D4	**P**	**P**	D4	**P**	D4	**P**	D4

Table 73. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L		√[1]	√[2]
		M		√[1]	√[2]
		Other		√[1]	
4	12	L		√[1]	√[2]
		M		√[1]	√[2]
		Other		√[1]	
8	12	L	√[1]	√[2]	√[3]
		M	√[1]	√[2]	
		Other	√[1]		
12	12	L	√[1]	√[2]	√[3]
		M	√[1]	√[2]	
		Other	√[1]		

Notes:

1. Supported DIMM capacity is 16 GB.
2. Supported DIMM capacity is up to 32 GB.
3. Supported DIMM capacity is up to 64 GB.

SR650 DCPMM and DIMM configuration

For DCPMM, the following memory modes are available:

- “SR650 App Direct Mode” on page 51
- “SR650 Memory Mode” on page 49
- “SR650 Mixed Memory Mode” on page 54

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Intel Xeon Platinum **82**80M*

  Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
- DCPMMs are supported only by Intel Xeon Cascade Lake processors. For a list of supported processors and memory modules, see http://www.lenovo.com/us/en/serverproven/
- When you install two or more DCPMMs, all DCPMMs must have the same Lenovo part number.
- All DRAM memory modules installed must have the same Lenovo part number.
- 16 GB RDIMM has two different types: 16 GB 1Rx4 and 16 GB 2Rx8. The part number of the two types are different.
- Supported memory capacity range varies with the following types of DCPMMs.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon 5215 **L***)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8280 **M***)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

The following illustration helps you to locate the memory module slots on the system board.

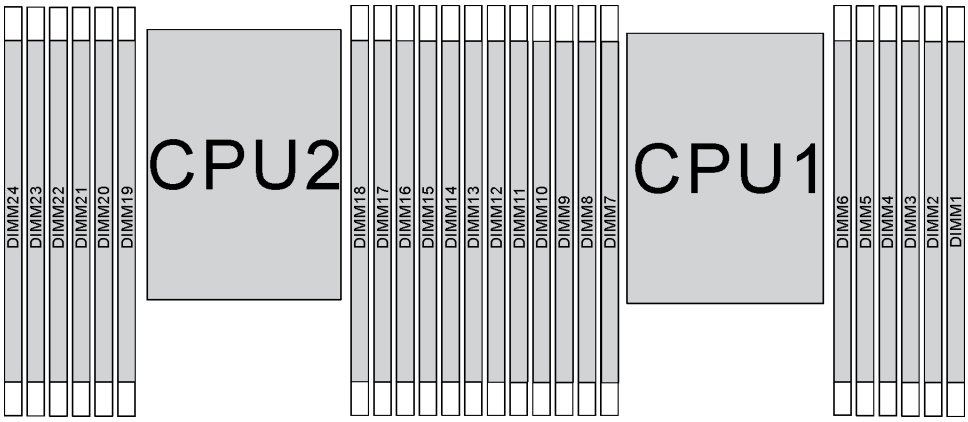

Figure 9. memory module slots on the system board

SR650 Memory Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your node. Below is the information of memory mode.

Table 74. Four categories of DIMM

DIMM Category	DDR4 Type		Capacity
D1	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM
D2	RDIMM	3DS RDIMM	All density of DDR4 more than 32 GB
D3	RDIMM		16 GB or 32 GB RDIMM
D4	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM

Following are all the combinations that are supported in this solution.

Memory Mode with one processor

Table 75. Memory Mode with one processor

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1											
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
2 DCPMMs and 4 DIMMs	**P**		D2		D2			D2		D2		**P**
2 DCPMMs and 6 DIMMs	D3		D3		D3	**P**	**P**	D3		D3		D3
4 DCPMMs and 6 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
6 DCPMMs and 6 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 76. Supported DCPMM capacity in Memory Mode with one processor

Total DCPM-Ms	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
2	**4**	**L**		√	√
		M		√	√
		Other		√	
2	**6**	**L**		√	√
		M		√	√
		Other		√	
4	**6**	**L**		√	√
		M		√	
		Other			
6	**6**	**L**	√	√	√
		M	√	√	
		Other	√		

Memory Mode with two processors

Table 77. Memory Mode with two processors

D1–D4: Refer to *Four categories of DIMM* table. **P**: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.																							
Configuration	Processor 2												Processor 1										
	24	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
4 DCPMMs and 8 DIMMs	**P**		D-2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
4 DCPMMs and 12 DIMMs	D3		D-3		D3	**P**	**P**	D3		D3		D3	D3		D3		D3	**P**	**P**	D3		D3		D3
8 DCPMMs and 12 DIMMs	D2		D-2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
12 DCPMMs and 12 DIMMs	D2	**P**	D-2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 78. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	Total RDIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L		√	√
		M		√	√
		Other		√	
4	12	L		√	√
		M		√	√
		Other		√	
8	12	L		√	√
		M		√	
		Other			
12	12	L	√	√	√
		M	√	√	
		Other	√		

SR650 App Direct Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your system. Follow the information of App Direct Mode as below.

Table 79. Four categories of DIMM

DIMM Category	DDR4 Type		Capacity
D1	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM
D2	RDIMM	3DS RDIMM	All density of DDR4 more than 32 GB

Table 79. Four categories of DIMM (continued)

D3	RDIMM		16 GB or 32 GB RDIMM
D4	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM

Following are all the combinations that are supported in this solution.

App Direct Mode with one processor

Note: When adding one or more DCPMMs and DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 80. App Direct Mode with one processor

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1											
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
1 DCPMM and 6 DIMMs	D1		D1		D1	**P**		D1		D1		D1
2 DCPMMs and 4 DIMMs	**P**		D1		D1			D1		D1		**P**
2 DCPMMs and 6 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1
2 DCPMMs and 8 DIMMs	**P**		D1	D1	D1	D1	D1	D1	D1	D1		**P**
4 DCPMMs and 6 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
6 DCPMMs and 6 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1

Table 81. Supported DCPMM capacity in App Direct Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**4**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
2	**6**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
2	**8**	**L**	√	√	√
		M	√	√	√

Table 81. Supported DCPMM capacity in App Direct Mode with one processor (continued)

		Other	√	√	
4	**6**	**L**	√	√	√
		M	√	√	
		Other	√		
6	**6**	**L**	√	√	√
		M	√	√	
		Other	√		

App Direct Mode with two processors

Note: When adding one or more DCPMMs and DIMMs during a memory upgrade, you might need to move other DCPMMs and DIMMs that are already installed to new locations.

Table 82. App Direct Mode with two processors

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 2												Processor 1											
	24	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
1 DCPMM and 12 DIMMs	D1		D1		D1			D1		D1		D1	D1		D1		D1		**P**	D1		D1		D1
2 DCPMMs and 12 DIMMs	D1		D1		D1		**P**	D1		D1		D1	D1		D1		D1		**P**	D1		D1		D1
4 DCPMMs and 8 DIMMs	**P**		D1		D1			D1		D1		**P**	**P**		D1		D1			D1		D1		**P**
4 DCPMMs and 12 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
4 DCPMMs and 16 DIMMs	**P**		D1	D1	D1	D1	D1	D1	D1	D1		**P**	**P**		D1	D1	D1	D-1	D1	D1	D-1	D1		**P**
8 DCPMMs and 12 DIMMs	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1	D1		D1	**P**	D1	**P**	**P**	D1	**P**	D1		D1
12 DCPMMs and 12 DIMMs	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1	D1	**P**	D1	**P**	D1	**P**	**P**	D1	**P**	D1	**P**	D1

Table 83. Supported DCPMM capacity in App Direct Mode with two processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
1	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**12**	**L**	√	√	√
		M	√	√	√

Table 83. Supported DCPMM capacity in App Direct Mode with two processors (continued)

		Other	√	√	√
4	**8**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
4	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
4	**16**	**L**	√	√	√
		M	√	√	√
		Other	√	√	
8	**12**	**L**	√	√	√
		M	√	√	
		Other	√		
12	**12**	**L**	√	√	√
		M	√	√	
		Other	√		

SR650 Mixed Memory Mode

Memory modules must be installed in a specific order based on the memory configuration that you implement on your node. Below is the information of mixed mode.

Table 84. Four categories of DIMM

DIMM Category	DDR4 Type		Capacity
D1	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM
D2	RDIMM	3DS RDIMM	All density of DDR4 more than 32 GB
D3	RDIMM		16 GB or 32 GB RDIMM
D4	RDIMM	3DS RDIMM	Any density of DDR4 except 8 GB 1Rx8 RDIMM

Following are all the combinations that are supported in this solution.

Mixed Memory Mode with one processor

Note: When adding one or more DCPMMs and DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 85. Mixed Memory Mode with one processor

D1–D4: Refer to *Four categories of DIMM* table. **P**: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.	
Configuration	Processor 1

Table 85. Mixed Memory Mode with one processor (continued)

	12	11	10	9	8	7	6	5	4	3	2	1
2 DCPMMs and 4 DIMMs	**P**		D4		D4			D4		D4		**P**
2 DCPMMs and 6 DIMMs	D4		D4		D4	**P**	**P**	D4		D4		D4
4 DCPMMs and 6 DIMMs	D4		D4	**P**	D4	**P**	**P**	D4	**P**	D4		D4
6 DCPMMs and 6 DIMMs	D4	**P**	D4	**P**	D4	**P**	**P**	D4	**P**	D4	**P**	D4

Table 86. Supported DCPMM capacity in Mixed Memory Mode with one processor

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
2	**4**	**L**		√	√
		M		√	√
		Other		√	
2	**6**	**L**		√	√
		M		√	√
		Other		√	
4	**6**	**L**	√	√	√
		M	√	√	
		Other	√		
6	**6**	**L**	√	√	√
		M	√	√	
		Other	√		

Mixed Memory Mode with two processors

Table 87. Mixed Memory Mode with two processors

D1–D4: Refer to *Four categories of DIMM* table.

P: Only Data Center Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 2												Processor 1											
	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
4 DCPMMs and 8 DIMMs	**P**		D-4		D4			D4		D4		**P**	**P**		D4		D4			D4		D4		**P**
4 DCPMMs and 12 DIMMs	D4		D-4		D4	**P**	**P**	D4		D4		D4	D4		D4		D4	**P**	**P**	D4		D4		D4
8 DCPMMs and 12 DIMMs	D4		D-4	**P**	D4	**P**	**P**	D4	**P**	D4		D4	D4		D4	**P**	D4	**P**	**P**	D4	**P**	D4		D4
12 DCPMMs and 12 DIMMs	D4	**P**	D-4	**P**	D4	**P**	**P**	D4	**P**	D4	**P**	D4	D4	**P**	D4	**P**	D4	**P**	**P**	D4	**P**	D4	**P**	D4

Table 88. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total DCPMMs	Total RDIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L		√	√
		M		√	√
		Other		√	
4	12	L		√	√
		M		√	√
		Other		√	
8	12	L	√	√	√
		M	√	√	
		Other	√		
12	12	L	√	√	√
		M	√	√	
		Other	√		

SR850 DCPMM and DIMM configuration

This section contains information of how to install DCPMMs and DRAM DIMMs properly.

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Xeon Platinum **82**80M*
- Supported memory capacity range varies with the following types of DCPMMs.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon **52**15L*)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Xeon Platinum **82**80M*)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

Processors and DIMM slots location

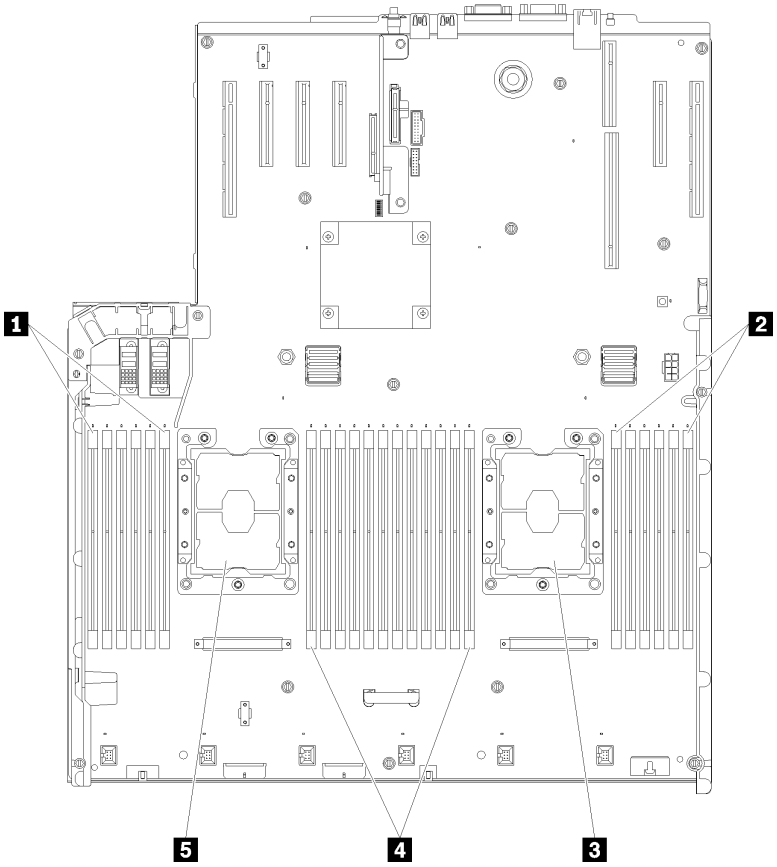

Figure 10. Processor and memory module layout: processor 1 and 2

Table 89. Processor and memory module layout: processor 1 and 2

1 DIMM slot 1-6	4 DIMM slot 7-18
2 DIMM slot 19-24	5 Processor 1
3 Processor 2	

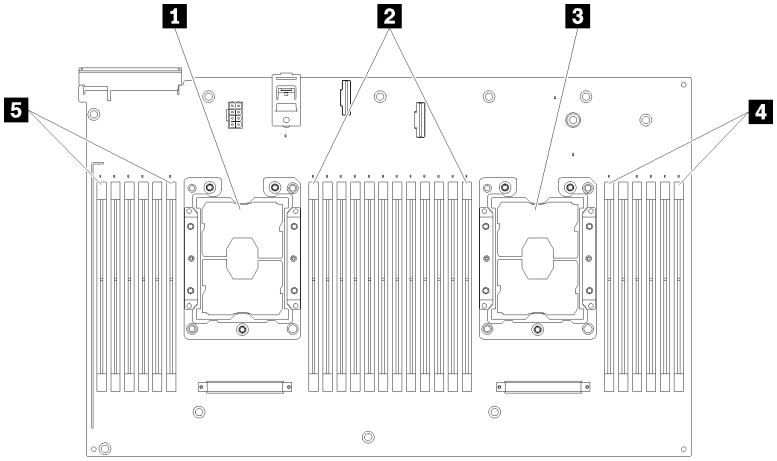

Figure 11. Processor and memory module layout: processor 3 and 4

Table 90. Processor and memory module layout: processor 3 and 4

1 Processor 3	4 DIMM slot 43-48
2 DIMM slot 31-42	5 DIMM slot 25-30
3 Processor 4	

Table 91. Channel and slot information of DIMMs around a processor

Slot	0	1	0	1	0	1		1	0	1	0	1	0
Channel	Channel 2		Channel 1		Channel 0			Channel 0		Channel 1		Channel 2	
DIMM number (Processor 1)	1	2	3	4	5	6		7	8	9	10	11	12
DIMM number (Processor 2)	13	14	15	16	17	18	Processor	19	20	21	22	23	24
DIMM number (Processor 3)	25	26	27	28	29	30		31	32	33	34	35	36
DIMM number (Processor 4)	37	38	39	40	41	42		43	44	45	46	47	48

SR850 Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache.

Installation order: Memory Mode with two processors

Memory module installation order for DCPMM Memory Mode with two installed processors.

Table 92. Memory population in Memory Mode with two processors

- **D1: DRAM DIMMs of 16 or 32 GB**
- **D2: DRAM DIMMs of 32 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 8 DIMMs	**P**		D2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
4 DCPMMs and 12 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
8 DCPMMs and 12 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
12 DCPMMs and 12 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 93. Supported DCPMM capacity in Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		√
12	12	L	√	√	√
		M	√	√	
		Other	√		√

Installation order: Memory Mode with four processors

Memory module installation order for DCPMM Memory Mode with four installed processors.

Table 94. Memory population in Memory Mode with four processors

- **D1: DRAM DIMMs of 16 or 32 GB**
- **D2: DRAM DIMMs of 32 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
8 DCPMMs and 24 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
16 DCPMMs and 24 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
24 DCPMMs and 24 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 95. Supported DCPMM capacity in Memory Mode with four processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		√
24	24	L	√	√	√
		M	√	√	
		Other	√		√

SR850 App Direct Mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

Installation order: App Direct Mode with two processors

Memory module installation order for DCPMM App Direct Mode with two installed processors.

Table 96. Memory population in App Direct Mode with two processors

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
4 DCPMMs and 16 DIMMs	**P**		D	D	D	D	D	D	D	D		**P**	**P**		D	D	D	D	D	D	D	D		**P**
4 DCPMMs and 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs and 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs and 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 97. Supported DCPMM capacity in App Direct Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	16	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		
12	12	L	√	√	√
		M	√	√	
		Other	√		

Table 98. Memory population in App Direct Mode with two processors (not interleaved only)

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1 DCPMM and 12 DIMMs	D		D		D		**P**	D		D		D	D		D		D			D		D		D
2 DCPMMs and 12 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D

Table 99. Supported DCPMM capacity in App Direct Mode with two processors (not interleaved only)

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	12	L	√	√	√
		M	√	√	√
		Other	√	√	√
2	12	L	√	√	√
		M	√	√	√
		Other	√	√	√

Installation order: App Direct Mode with four processors

Memory module installation order for DCPMM App Direct Mode with four installed processors.

Table 100. Memory population in App Direct Mode with four processors

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
8 DCPMMs and 32 DIMMs	**P**		D	D	D	D	D	D	D	D		**P**	**P**		D	D	D	D	D	D	D	D		**P**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 101. Supported DCPMM capacity in App Direct Mode with four processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	X
8	32	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		
24	24	L	√	√	√
		M	√	√	
		Other	√		

Table 102. Memory population in App Direct Mode with four processors (not interleaved only)

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D
Configuration	**Processor 3**												**Processor 4**											
	25	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**
1 DCPMM and 24 DIMMs	D		D		D			D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D

Table 103. Supported DIMM capacity in App Direct Mode with four processors (not interleaved only)

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	24	L	√	√	√
		M	√	√	√
		Other	√	√	√
4	24	L	√	√	√
		M	√	√	√
		Other	√	√	

SR850 Mixed Memory Mode

In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

Installation order: Mixed Memory Mode with two processors

Memory module installation order for DCPMM Mixed Memory mode with two installed processors.

Table 104. Memory population in Mixed Memory Mode with two processors

- **D: DRAM DIMMs of 16 GB or larger capacity**

  Note: 3DS LRDIMMs are not supported in this mode.
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs with 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
4 DCPMMs with 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs with 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs with 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 105. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		√
12	12	L	√	√	√
		M	√	√	
		Other	√		√

Installation order: Mixed Memory Mode with four processors

Memory module installation order for DCPMM Mixed Memory mode with four installed processors.

Table 106. Memory population in Mixed Memory Mode with four processors

- **D: DRAM DIMMs of 16 GB or larger capacity**

  Note: 3DS LRDIMMs are not supported in this mode.
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		P	**P**		D		D			D		D		**P**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 107. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		√
24	24	L	√	√	√
		M	√	√	
		Other	√		√

SR860 DCPMM and DIMM configuration

This section contains information of how to install DCPMMs and DRAM DIMMs properly.

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Xeon Platinum **82**80M*

  If the presently installed processors do not support DCPMMs, replace them with those that do. For more details, see:

  https://www.intel.com/content/www/us/en/products/docs/memory-storage/optane-persistent-memory/lenovo-partner-video.htm
- Supported memory capacity range varies with the following types of DCPMMs.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon **52**15L*)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Xeon Platinum **82**80M*)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

Processors and DIMM slots location

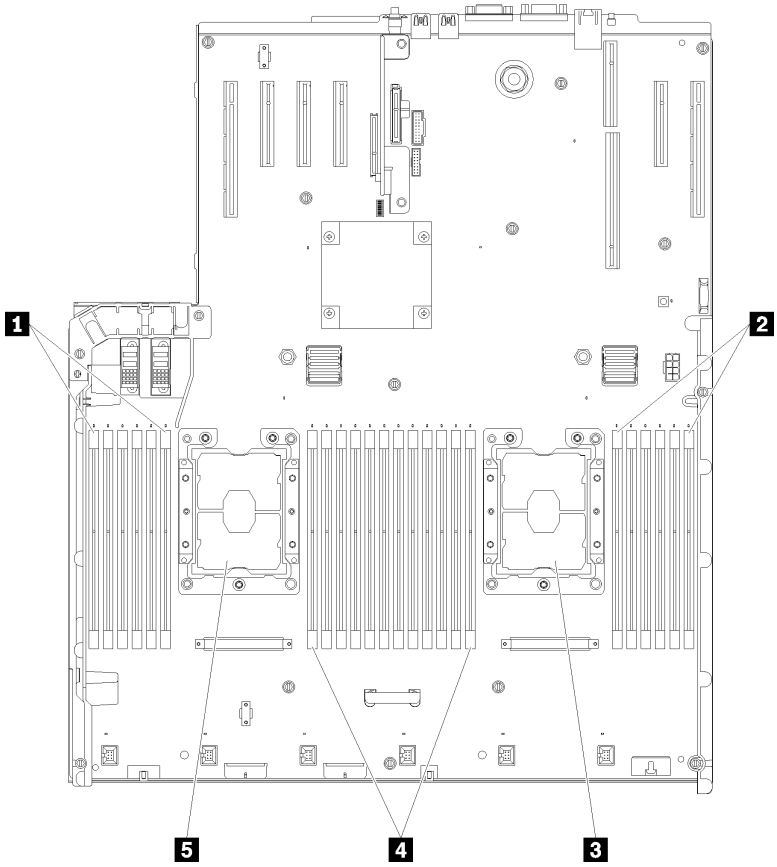

Figure 12. Processor and memory module layout: processor 1 and 2

Table 108. Processor and memory module layout: processor 1 and 2

1 DIMM slot 1-6	4 DIMM slot 7-18
2 DIMM slot 19-24	5 Processor 1
3 Processor 2	

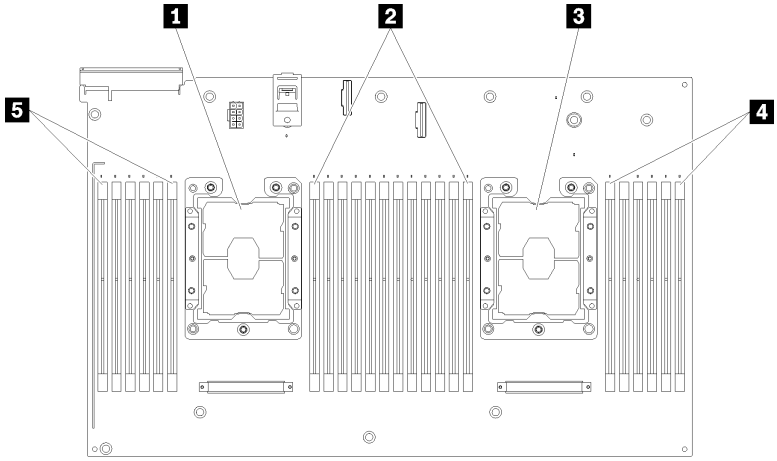

Figure 13. Processor and memory module layout: processor 3 and 4

Table 109. Processor and memory module layout: processor 3 and 4

1 Processor 3	4 DIMM slot 43-48
2 DIMM slot 31-42	5 DIMM slot 25-30
3 Processor 4	

Table 110. Channel and slot information of DIMMs around a processor

Slot	0	1	0	1	0	1		1	0	1	0	1	0
Channel	Channel 2		Channel 1		Channel 0			Channel 0		Channel 1		Channel 2	
DIMM number (Processor 1)	1	2	3	4	5	6		7	8	9	10	11	12
DIMM number (Processor 2)	13	14	15	16	17	18	Processor	19	20	21	22	23	24
DIMM number (Processor 3)	25	26	27	28	29	30		31	32	33	34	35	36
DIMM number (Processor 4)	37	38	39	40	41	42		43	44	45	46	47	48

SR860 Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache.

Installation order: Memory Mode with two processors

Memory module installation order for DCPMM Memory Mode with two installed processors.

Table 111. Memory population in Memory Mode with two processors

- **D1: DRAM DIMMs of 16 or 32 GB**
- **D2: DRAM DIMMs of 32 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 8 DIMMs	**P**		D2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
4 DCPMMs and 12 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
8 DCPMMs and 12 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
12 DCPMMs and 12 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 112. Supported DCPMM capacity in Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		√
12	12	L	√	√	√
		M	√	√	
		Other	√		√

Installation order: Memory Mode with four processors

Memory module installation order for DCPMM Memory Mode with four installed processors.

Table 113. Memory population in Memory Mode with four processors

- **D1: DRAM DIMMs of 16 or 32 GB**
- **D2: DRAM DIMMs of 32 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
8 DCPMMs and 24 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
16 DCPMMs and 24 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
24 DCPMMs and 24 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 114. Supported DCPMM capacity in Memory Mode with four processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		√
24	24	L	√	√	√
		M	√	√	
		Other	√		√

SR860 App Direct Mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

Installation order: App Direct Mode with two processors

Memory module installation order for DCPMM App Direct Mode with two installed processors.

Table 115. Memory population in App Direct Mode with two processors

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
4 DCPMMs and 16 DIMMs	**P**		D	D	D	D	D	D	D	D		**P**	**P**		D	D	D	D	D	D	D	D		**P**
4 DCPMMs and 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs and 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs and 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 116. Supported DCPMM capacity in App Direct Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	16	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		
12	12	L	√	√	√
		M	√	√	
		Other	√		

Table 117. Memory population in App Direct Mode with two processors (not interleaved only)

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1 DCPMM and 12 DIMMs	D		D		D		**P**	D		D		D	D		D		D			D		D		D
2 DCPMMs and 12 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D

Table 118. Supported DCPMM capacity in App Direct Mode with two processors (not interleaved only)

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	12	L	√	√	√
		M	√	√	√
		Other	√	√	√
2	12	L	√	√	√
		M	√	√	√
		Other	√	√	√

Installation order: App Direct Mode with four processors

Memory module installation order for DCPMM App Direct Mode with four installed processors.

Table 119. Memory population in App Direct Mode with four processors

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
8 DCPMMs and 32 DIMMs	**P**		D	D	D	D	D	D	D	D		**P**	**P**		D	D	D	D	D	D	D	D		**P**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 120. Supported DCPMM capacity in App Direct Mode with four processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	X
8	32	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		
24	24	L	√	√	√
		M	√	√	
		Other	√		

Table 121. Memory population in App Direct Mode with four processors (not interleaved only)

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D
Configuration	**Processor 3**												**Processor 4**											
	25	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**
1 DCPMM and 24 DIMMs	D		D		D			D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D

Table 122. Supported DIMM capacity in App Direct Mode with four processors (not interleaved only)

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	24	L	√	√	√
		M	√	√	√
		Other	√	√	√
4	24	L	√	√	√
		M	√	√	√
		Other	√	√	

SR860 Mixed Memory Mode

In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

Installation order: Mixed Memory Mode with two processors

Memory module installation order for DCPMM Mixed Memory mode with two installed processors.

Table 123. Memory population in Mixed Memory Mode with two processors

- **D: DRAM DIMMs of 16 GB or larger capacity**

  Note: 3DS LRDIMMs are not supported in this mode.
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs with 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
4 DCPMMs with 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs with 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs with 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 124. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		√
12	12	L	√	√	√
		M	√	√	
		Other	√		√

Installation order: Mixed Memory Mode with four processors

Memory module installation order for DCPMM Mixed Memory mode with four installed processors.

Table 125. Memory population in Mixed Memory Mode with four processors

- **D: DRAM DIMMs of 16 GB or larger capacity**

  Note: 3DS LRDIMMs are not supported in this mode.
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		P	**P**		D		D			D		D		**P**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 126. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		√
24	24	L	√	√	√
		M	√	√	
		Other	√		√

SR950 DCPMM and DIMM configuration

There are a number of criteria that must be followed when selecting and installing memory modules in your server.

The DIMM population sequences in this document show all memory population combinations that are supported by your server. Some of these combinations will perform better than others because they balance the distribution of memory across processors, memory controllers, and memory channels. Balanced memory configurations enable optimal interleaving across all populated memory channels of a processor to boost memory performance.

https://lenovopress.com/servers/options/memory

In addition, you can take advantage of a memory configurator tool, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

Memory module selection

The following memory modules (DIMMs) are supported for use in the server. See http://www.lenovo.com/us/en/serverproven/ for specific memory module part numbers and ordering information.

A label on each DIMM identifies the DIMM type. This information is in the format **xxxxx *n*Rxxx PC4-xxxxx-xx-xx-xxx**. Where ***n*** indicates if the DIMM is single-rank (n=1) or dual-rank (n=2).

Notes:

- When you replace a DIMM, the server provides automatic DIMM enablement capability without requiring you to use the Lenovo XClarity Provisioning Manager to enable the new DIMM manually.

Memory architecture

The relationship between memory controllers, channels, and connectors on each compute system board is shown in the following illustration and each memory channel has two DIMM slots (0, furthest from the processor, and 1, closest to the processor).

- Each processor in your server has two memory controllers: IMC1 and IMC2.
- Each memory controller has three memory channels:
  - Processor 1:
    - IMC1 has memory channels A, B, and C.
    - IMC2 has memory channels D, E, and F.

  - Processor 2:
    - IMC1 has memory channels G, H, and J.
    - IMC2 has memory channels K, L, and M.
- Each memory channel has two DIMM slots: slot 0 (furthest from the processor) and slot 1 (closest to the processor).

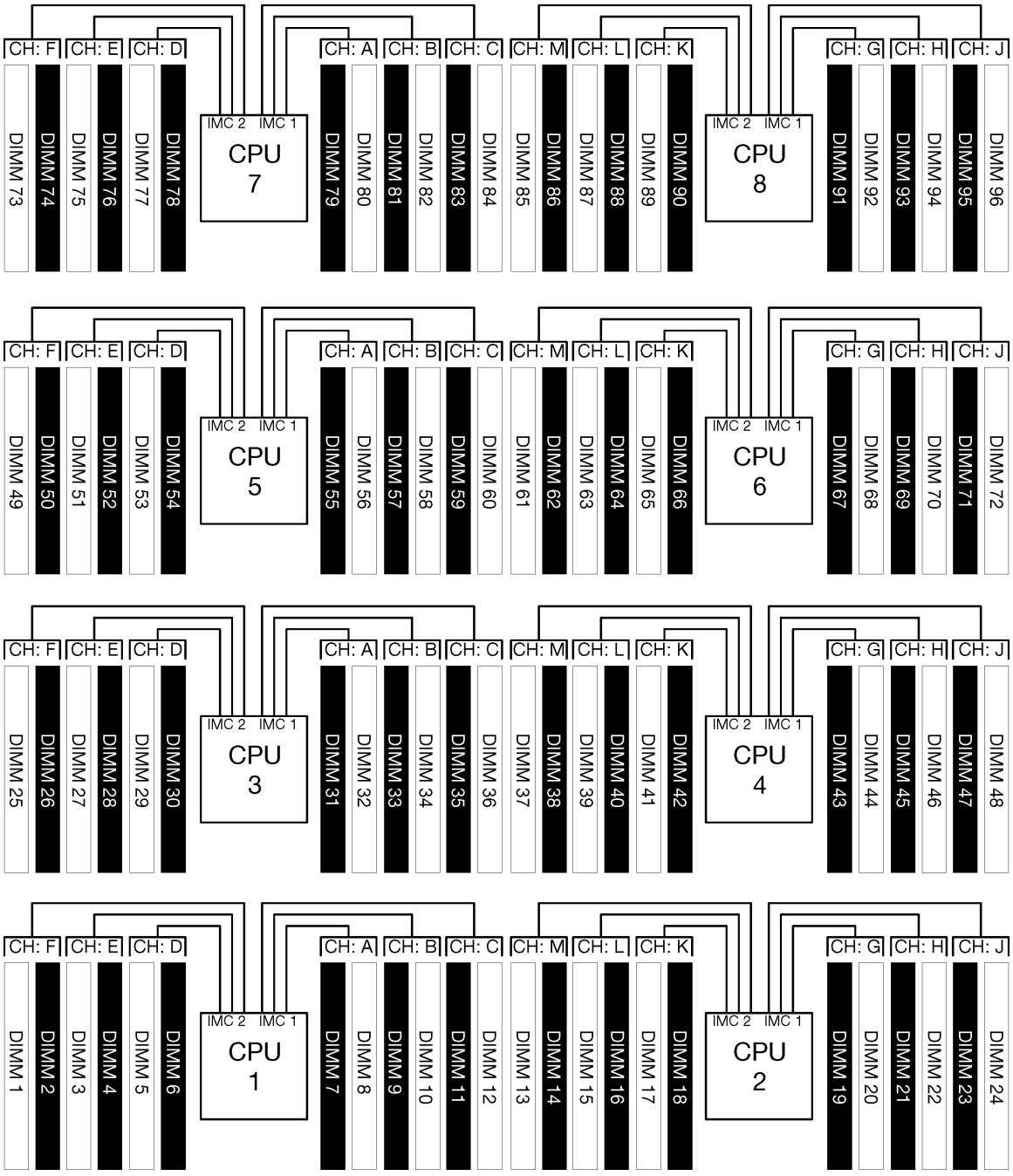

Figure 14. Memory architecture

Memory modules population requirements

Observe the following rules when populating memory modules for all memory modes.

Note: The following guidelines discuss the memory architecture related to compute system board processor 1. For compute system board processor 2, substitute memory channels G/H/J/K/L/M for processor 1 memory channels A/B/C/D/E/F in the discussion.

- Do not mix R-DIMMs, LR-DIMMs, and 3DS DIMMs in a server.
- At least one DIMM is required for each processor. Install at least six DIMMs per processor for good performance.
- An “M” SKU processor is required for processors with more than six 128GB DIMMs installed.
- Within a memory controller:
  - Populate channel A/D first. Channel B/E will be either empty or must be identically populated as channel A/D. Channel C/F will be either empty or must be identically populated as channel B/E.

    Note: Five DIMM configurations is a supported exception to these population rules. Five DIMMs are populated so channels 0 and 1 each have two DIMMs and channel 2 has one DIMM.
  - Populate the memory connector in each channel that is physically furthest from the processor (slot 0) first.
  - If a memory channel has two DIMMs installed and these DIMMs have different numbers of ranks, populate the DIMM with higher number of ranks in the memory connector that is physically furthest from the processor (slot 0).
  - If two DIMMs on a channel have identical ranks, populate the DIMM with higher capacity in the memory connector that is physically furthest from the processor (slot 0).

Populating memory modules for best system performance

To populate memory configurations for the best memory performance, observe the following general guidelines for all memory modes.

Note: The following guidelines discuss the memory architecture related to compute system board processor 1. For compute system board processor 2, substitute memory channels G/H/J/K/L/M for processor 1 memory channels A/B/C/D/E/F in the discussion.

- When multiple processors are installed, all processors within the server must have identical memory population.
- Populate all memory channels for optimal performance.
- If a processor has only three DIMMs that are identical (same Lenovo part number), populate all of them in memory controller 1 (IMC1).

Additional requirements for memory mirroring

The following rules apply for memory mirroring.

Note: The following guidelines discuss the memory architecture related to compute system board processor 1. For compute system board processor 2, substitute memory channels G/H/J/K/L/M for processor 1 memory channels A/B/C/D/E/F in the discussion.

- The server supports only two, three, four, or six DIMMs per memory controller (one or five DIMMs per memory controller is not supported).
- As with independent memory mode, equal DIMM sizes must be installed for the populated memory channels. DIMM slot population within a channel does not have to be identical; however, the same DIMM slot locations across channel A/B/C or channels D/E/F must be populated identically.

- If DIMMs are installed in only two memory channels, mirroring occurs across two DIMMs. Channels A/D and B/E hold the primary and secondary cache lines.
- If DIMMs are installed in all three memory channels, mirroring occurs across all three DIMM channels. Channels A/D and B/E, Channels B/E and C/F, and Channels C/F and A/D hold the primary and secondary cache lines.
- Do not mix 2–channel and 3–channel DDR mirroring in a memory controller.

Additional requirements for memory sparing

The following rules apply for memory sparing:

- As with independent memory mode, all memory channels must have at least two ranks.
- Every populated memory channel must have at least two ranks of DIMMs.
- If a memory channel has only single rank DIMMs, populate both single rank DIMMs on one channel.
- Single DIMM-per-channel systems do not support single-rank DIMMs in sparing mode.

Notes:

- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Intel Xeon Platinum **82**80M*

  If the presently installed processors do not support DCPMMs, replace them with the processors that support DCPMMs.
- Supported memory capacity range varies with the following types of processors.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon 5215**L***)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8280**M***)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

http://1config.lenovo.com/#/memory_configuration

SR950 Memory Mode

In Memory Mode, 100% of DCPMM capacity acts as system memory. The DRAM DIMMs act as cache.

When implementing Memory Mode, any supported DIMMs in any capacity can be installed.

DCPMM Installation order: Memory mode with two processors

When implementing Memory mode, any supported DIMMs in any capacity can be installed.

When two processors are installed in the server:

- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.

Several configurations are supported with implementing Memory mode with two processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 127. Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 128. Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 129. Memory mode with 2 DCPMMs and 8 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/ 6 DRAM DIMMs per processor

Table 130. Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Note: In this configuration, only RDIMMs are recommended for the DRAM DIMMs.

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 131. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P

DCPMM Installation order: Memory mode with four processors

When implementing Memory mode, any supported DIMMs in any capacity can be installed. However, you should consider using DIMMs that are greater than 32 GB.

When four processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.

Several configurations are supported with implementing Memory mode with four processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 132. Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 133. Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 134. Memory mode with 2 DCPMMs and 8 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM

Table 134. Memory mode with 2 DCPMMs and 8 DRAM DIMMs per processor (4 processors) (continued)

- D = DRAM DIMM

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/ 6 DRAM DIMMs per processor

Table 135. Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Note: In this configuration, only RDIMMs are recommended for the DRAM DIMMs.

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 136. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P

DCPMM Installation order: Memory mode with six processors

When implementing Memory mode, any supported DIMMs in any capacity can be installed. However, you should consider using DIMMs that are greater than 32 GB.

When six processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.
- Processors 5 and 6 are installed in the lower compute system board of the upper compute tray.

Several configurations are supported with implementing Memory mode with six processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 137. Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 138. Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 5												**Processor 6**											

Table 138. Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (6 processors) (continued)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 139. Memory mode with 2 DCPMMs and 8 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 5												Processor 6											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/ 6 DRAM DIMMs per processor

Table 140. Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Note: In this configuration, only RDIMMs are recommended for the DRAM DIMMs.

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 5												Processor 6											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 141. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM

Table 141. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (6 processors) (continued)

- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

DCPMM Installation order: Memory mode with eight processors

When implementing Memory mode, any supported DIMMs in any capacity can be installed. However, you should consider using DIMMs that are greater than 32 GB.

When eight processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.
- Processors 5 and 6 are installed in the lower compute system board of the upper compute tray.
- Processors 7 and 8 are installed in the upper compute system board of the upper compute tray.

Several configurations are supported with implementing Memory mode with eight processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 142. Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 143. Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

Table 143. Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (8 processors) (continued)

Processor 3												Processor 4											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 144. Memory mode with 2 DCPMMs and 8 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/ 6 DRAM DIMMs per processor

Table 145. Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Note: In this configuration, only RDIMMs are recommended for the DRAM DIMMs.

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

Table 145. Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (8 processors) (continued)

Processor 3												Processor 4											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 146. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

SR950 App Direct Mode

In App Direct Mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

When implementing App Direct Mode, any supported DIMMs in any capacity can be installed.

DCPMM Installation order: App Direct mode with two processors

When implementing App Direct Mode, any supported DIMMs in any capacity can be installed.

When two processors are installed in the server:

- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.

Several configurations are supported with implementing App Direct mode with eight processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/8 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor
- 1 DCPMM/6 DRAM DIMMs per processor
- 1 DCPMM in the system

6 DCPMMs/6 DRAM DIMMs per processor

Table 147. App Direct mode with 6 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/6 DRAM DIMMs per processor

Table 148. App Direct mode with 4 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 149. App Direct mode with 2 DCPMMs and 8 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/6 DRAM DIMMs per processor

Table 150. App Direct mode with 2 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/4 DRAM DIMMs per processor

Table 151. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

1 DCPMM/6 DRAM DIMMs per processor

Table 152. App Direct mode with 1 DCPMMs and 6 DRAM DIMMs

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D

1 DCPMM in the system

Table 153. App Direct mode with 1 DCPMM in the system

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D			D		D		D

DCPMM Installation order: App Direct mode with four processors

When implementing App Direct Mode, any supported DIMMs in any capacity can be installed.

When eight processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.

Several configurations are supported with implementing App Direct mode with eight processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/8 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor
- 1 DCPMM/6 DRAM DIMMs per processor
- 1 DCPMM in the system

6 DCPMMs/6 DRAM DIMMs per processor

Table 154. App Direct mode with 6 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/6 DRAM DIMMs per processor

Table 155. App Direct mode with 4 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 156. App Direct mode with 2 DCPMMs and 8 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/6 DRAM DIMMs per processor

Table 157. App Direct mode with 2 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/4 DRAM DIMMs per processor

Table 158. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

1 DCPMM/6 DRAM DIMMs per processor

Table 159. App Direct mode with 1 DCPMMs and 6 DRAM DIMMs

In the table below:

Table 159. App Direct mode with 1 DCPMMs and 6 DRAM DIMMs (continued)

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D

1 DCPMM in the system

Table 160. App Direct mode with 1 DCPMM in the system

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D			D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D			D		D		D	D		D		D			D		D		D

DCPMM Installation order: App Direct mode with six processors

When implementing App Direct Mode, any supported DIMMs in any capacity can be installed.

When eight processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.
- Processors 5 and 6 are installed in the lower compute system board of the upper compute tray.

Several configurations are supported with implementing App Direct mode with eight processors:

- 6 DCPMMs/ 6 DRAM DIMMs per processor
- 4 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/8 DRAM DIMMs per processor
- 2 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 4 DRAM DIMMs per processor
- 1 DCPMM/6 DRAM DIMMs per processor
- 1 DCPMM in the system

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 161. App Direct mode with 6 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 162. App Direct mode with 4 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											

Table 162. App Direct mode with 4 DCPMMs and 6 DRAM DIMMs per processor (6 processors) (continued)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 163. App Direct mode with 2 DCPMMs and 8 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												**Processor 2**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/ 6 DRAM DIMMs per processor

Table 164. App Direct mode with 2 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												**Processor 2**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 165. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (6 processors)

In the table below:

Table 165. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (6 processors) (continued)

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

1 DCPMM/6 DRAM DIMMs per processor

Table 166. App Direct mode with 1 DCPMMs and 6 DRAM DIMMs

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D

1 DCPMM in the system

Table 167. App Direct mode with 1 DCPMM in the system

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D			D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D			D		D		D	D		D		D			D		D		D

Table 167. App Direct mode with 1 DCPMM in the system (continued)

Processor 5												Processor 6											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D			D		D		D	D		D		D			D		D		D

DCPMM Installation order: App Direct mode with eight processors

When implementing App Direct Mode, any supported DIMMs in any capacity can be installed.

When eight processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.
- Processors 5 and 6 are installed in the lower compute system board of the upper compute tray.
- Processors 7 and 8 are installed in the upper compute system board of the upper compute tray.

Several configurations are supported with implementing App Direct mode with eight processors:

- 6 DCPMMs/6 DRAM DIMMs per processor
- 4 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/8 DRAM DIMMs per processor
- 2 DCPMMs/6 DRAM DIMMs per processor
- 2 DCPMMs/4 DRAM DIMMs per processor
- 1 DCPMM/6 DRAM DIMMs per processor
- 1 DCPMM in the system

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 168. App Direct mode with 6 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 169. App Direct mode with 4 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Table 169. App Direct mode with 4 DCPMMs and 6 DRAM DIMMs per processor (8 processors) (continued)

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 8 DRAM DIMMs per processor

Table 170. App Direct mode with 2 DCPMMs and 8 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P

2 DCPMMs/ 6 DRAM DIMMs per processor

Table 171. App Direct mode with 2 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**

Table 171. App Direct mode with 2 DCPMMs and 6 DRAM DIMMs per processor (8 processors) (continued)

D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 172. App Direct mode with 2 DCPMMs and 4 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												**Processor 2**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

1 DCPMM/6 DRAM DIMMs per processor

Table 173. App Direct mode with 1 DCPMMs and 6 DRAM DIMMs

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												**Processor 2**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D

Table 173. App Direct mode with 1 DCPMMs and 6 DRAM DIMMs (continued)

Processor 3												Processor 4											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D		P	D		D		D

1 DCPMM in the system

Table 174. App Direct mode with 1 DCPMM in the system

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D		P	D		D		D	D		D		D			D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D			D		D		D	D		D		D			D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D			D		D		D	D		D		D			D		D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D			D		D		D	D		D		D			D		D		D

SR950 Mixed Memory Mode

In Mixed Memory Mode, 1-99% of DCPMM capacity acts as system memory. In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

When implementing Mixed Memory Mode, any supported DIMMs in any capacity can be installed.

DCPMM Installation order: Mixed Memory mode with two processors

When implementing Mixed Memory mode, any supported DIMMs in any capacity can be installed.

When two processors are installed in the server:

- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.

Several configurations are supported with implementing Mixed Memory mode with six processors:

- 6 DCPMMs/ 6 DRAM DIMMs per processor
- 4 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 175. Mixed Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 176. Mixed Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 6 DRAM DIMMs per processor

Note: Only RDIMMs are recommended for this configuration

Table 177. Mixed Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 178. Mixed Memory mode with 2 DCPMMs and 4 DRAM DIMMs per processor (2 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

DCPMM Installation order: Mixed Memory mode with four processors

When implementing Mixed Memory mode, any supported DIMMs in any capacity can be installed.

When four processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.

Several configurations are supported with implementing Mixed Memory mode with six processors:

- 6 DCPMMs/ 6 DRAM DIMMs per processor
- 4 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 179. Mixed Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 180. Mixed Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 6 DRAM DIMMs per processor

Note: Only RDIMMs are recommended for this configuration

Table 181. Mixed Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (4 processors)

In the table below:

Table 181. Mixed Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (4 processors) (continued)

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 182. Mixed Memory mode with 2 DCPMMs and 4 DRAM DIMMs per processor (4 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

DCPMM Installation order: Mixed Memory mode with six processors

When implementing Mixed Memory mode, any supported DIMMs in any capacity can be installed.

When six processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.
- Processors 5 and 6 are installed in the lower compute system board of the upper compute tray.

Several configurations are supported with implementing Mixed Memory mode with six processors:

- 6 DCPMMs/ 6 DRAM DIMMs per processor
- 4 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 183. Mixed Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 184. Mixed Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 5												**Processor 6**											

Table 184. Mixed Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (6 processors) (continued)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 6 DRAM DIMMs per processor

Note: Only RDIMMs are recommended for this configuration

Table 185. Mixed Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 5												Processor 6											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 186. Mixed Memory mode with 2 DCPMMs and 4 DRAM DIMMs per processor (6 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												Processor 4											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P
Processor 5												Processor 6											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P

DCPMM Installation order: Mixed Memory mode with eight processors

When implementing Mixed Memory mode, any supported DIMMs in any capacity can be installed.

When eight processors are installed in the server:
- Processors 1 and 2 are installed in the lower compute system board of the lower compute tray.
- Processors 3 and 4 are installed in the upper compute system board of the lower compute tray.
- Processors 5 and 6 are installed in the lower compute system board of the upper compute tray.
- Processors 7 and 8 are installed in the upper compute system board of the upper compute tray.

Several configurations are supported with implementing Mixed Memory mode with eight processors:

- 6 DCPMMs/ 6 DRAM DIMMs per processor
- 4 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 6 DRAM DIMMs per processor
- 2 DCPMMs/ 4 DRAM DIMMs per processor

6 DCPMMs/ 6 DRAM DIMMs per processor

Table 187. Mixed Memory mode with 6 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

4 DCPMMs/ 6 DRAM DIMMs per processor

Table 188. Mixed Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												Processor 2											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 3												**Processor 4**											

Table 188. Mixed Memory mode with 4 DCPMMs and 6 DRAM DIMMs per processor (8 processors) (continued)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D

2 DCPMMs/ 6 DRAM DIMMs per processor

Note: Only RDIMMs are recommended for this configuration

Table 189. Mixed Memory mode with 2 DCPMMs and 6 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												**Processor 2**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 3												**Processor 4**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D

2 DCPMMs/ 4 DRAM DIMMs per processor

Table 190. Mixed Memory mode with 2 DCPMMs and 4 DRAM DIMMs per processor (8 processors)

In the table below:

- P = DCPMM
- D = DRAM DIMM

Processor 1												**Processor 2**											
1	**2**	**3**	**4**	**5**	**6**	**7**	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 3												**Processor 4**											

Table 190. Mixed Memory mode with 2 DCPMMs and 4 DRAM DIMMs per processor (8 processors) (continued)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
P		D		D			D		D		P	P		D		D			D		D		P
Processor 5												**Processor 6**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P
Processor 7												**Processor 8**											
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
P		D		D			D		D		P	P		D		D			D		D		P

Index

Lenovo