Smarc

User Manual

SM-C93

SMARC® Rel. 2.1.1 compliant module with the Intel® Atom™ x6000E Series and Intel® Pentium® and Celeron® N and J Series processors (formerly Elkhart Lake) for FuSa applications

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	19th April 2021	First official release	AR
1.1	23rd December 2021	Safety Policy included	SO

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SM-C93 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The SM-C93 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a SM-C93 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SM-C93 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the SM-C93 Module shall be:

- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the module never exceeds 100 W, even in worst-case fault);
- used inside an enclosure; the enclosure is not necessary if the temperature of the parts likely to be touched never exceeds 70 °C;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which includes a SM-C93 module in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition
- Prescribe temperature and humidity range for operating, transport and storage conditions;
- Prescribe to perform maintenance on the module only when it is off and has already cooled down;
- Prescribe that the connections from or to the Module have to be compliant to ES1 requirements;
- The module in its enclosure must be evaluated for temperature and airflow considerations.

1.8 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
AVC	Advanced Video Coding, a video compression standard, also known as H.264
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DP	Display Port, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HEVC	High Efficiency Video Coding, a video compression standard, also known as H.265
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
JPEG/MJPEG	Joint Photographic Experts Group, standard method for lossy compression of digital images. Motion JPEG is a video compression format
LAN	Local Area Network
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of

	the MMC. They are devices that incorporate the flash memories on a single BGA chip.
MPEG2	Standard for the generic coding of moving pictures and associated audio information
MVC	Multiview Video Coding, a stereoscopic video coding standard for video compression
N.A.	Not Applicable
N.C.	Not Connected
OpenCL	Open Computing Language, specifies programming languages for programming different devices and API
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OS	Operating System
PCI-e	Peripheral Component Interface Express
PHY	Abbreviation of Physical, it is the device implementing the Physical Layer of ISO/OSI-7 model for communication systems
PWM	Pulse Width Modulation
PWR	Power
RGMII (PHY)	Reduced Gigabit Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer
SATA	Serial Advance Technology Attachment, a differential full duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SGET	Standardization Group for Embedded Technologies
SMARC	Smart Mobility Architecture, a computer Module standard maintained by the SGET
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SOC	System-on-a-chip
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
UART	Universal Asynchronous Receiver-Transmitter, is an asynchronous serial interface where data format and transmission speed are configurable
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface

USB	Universal Serial Bus
VP8	Open video compression format, a traditional block-based transform coding format
VP9	Successor to VP8, customized for video greater than 1080p
WMV9	Series 9 of Windows Media Video, a video compression format inlcuding native support for interlaced video, non-square pixels, and frame interpolation

1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	https://uefi.org/specifications
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
FastEthernet	http://standards.ieee.org/about/get/802/802.3.html
Gigabit Ethernet	https://standards.ieee.org/standard/802_3-2018.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
Intel® Atom™ Elkhart Lake family	https://ark.intel.com/content/www/us/en/ark/products/codename/80644/Elkhart-lake.html#@Embedded
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SMARC Design Guide 2.0	https://sget.org/wp-content/uploads/2018/09/SMARC_DG_V2.pdf
SMARC Hardware Specification 2.1.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home

SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	https://usb.org.10-1-108-210.causewaynow.com/sites/default/files/usb_32_20191024.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram

2.1 Introduction

The SM-C93 is a SMARC Rel. 2.1.1 compliant module based on the Intel® Atom® x6000E Series and Intel® Pentium® and Celeron® N and J Series processors (formerly Elkhart Lake) for FuSa applications, a series of Dual / Quad SOCs with 64-bit instruction set.

These new family of processors offers different use conditions, such as PC Client, Embedded and Industrial targets and is optimized for usage in vertical applications for IOT including Industrial, Office Automation, Retail, Gaming, Healthcare, Transportation.

New features introduced by Elkhart Lake are, but not limited to the following: Time Sensitive Network (TSN) and Time Coordinate Computing (TCC) for real-time and responsive applications, Scalability and consolidation of temporally deterministic workloads, In band and OOB remote manageability (reboot/power-on/power-off), Platform Trust Technology (PTT), Dynamic Application Loader (DAL) and Secure Guard Extension (SGX), Intel Programmable Service Engine, Intel UHD Graphics, media, and display supporting, Fully Integrated Voltage Regulator (FIVR). Last but not least, this is the first Intel product designed with functional safety capabilities, made available by Intel® Safety Island (SI), a functional safety IP integrated into the Elkhart Lake Platform Control Hub (PCH), intended to raise the safety level of the platform with a single source for managing the safety faults of the SOC.

These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation, which is essential for boards with sizes so reduced as for SMARC ("Smart Mobility ARChitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

The Embedded Memory Controller allows the integration of up to 16GB of LPDDR4 Memory directly soldered onboard with In-Band Error Correction Code supported (Safety related feature) and speed up to 4267MT/s on single rank and 3733MT/s on dual rank.

All SOCs embed an Intel® Gen11 UHD Graphics controller with up to 32 Execution Units, which offer high graphical performances, with support for Microsoft® DirectX12.1, OpenGL 4.5, OpenCL™ 1.2, OpenGL ES 3.1, Vulkan 1.1 and HW acceleration for video encoding and decoding of HEVC (H.265), H.264, VP8, VP9, JPEG/MJPEG. It is also possible the HW video decoding only of MPEG2, VC-1.

This embedded GPU is able to drive three independent displays, by using the interfaces available on SMARC connector: one DP++ 1.4, one HMDI 1.4 or DP++ 1.4 and one eDP 1.3 or Dual Channel 18/24bit LVDS (factory alternatives).

Mass Storage capabilities of the board include one external S-ATA Gen3 channel, a standard 4-bit SD interface and one optional eMMC 5.1 Drive soldered on board (Safety related), with up to 128GB capabilities.

Other than the interfaces already discussed previously, on SMARC connector there are the signals necessary for the implementation of 2x GbE, up to 6 ports in USB2.0 only and up to 2 Super Speed (SS) ports (i.e. USB 3.1 Gen2 compliant), 4 x PCI-Express Gen3 lanes, HD and I^2S Audio interfaces, CAN, I^2C, SPI and SM buses, up to 14 GPIOs, HS-UART and UART interfaces.

Interfacing to the board comes through a single card edge connector, whose pinout is defined by SMARC specifications Rel.2.1.1. For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as integration of other peripherals/devices not already included in SM-C93 CPU module.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

2.2 Technical Specifications

Processors

Intel® Atom™ x6000E CPUs certified for FuSa, compliant to IEC 61508 and ISO 13849 requirements for Functional Safety and Safety Integrity Levels:

- Atom™ x6427FE Quad Core @1.9GHz (no Turbo) 12W TDP w/ IBECC, IHS and TCC, FuSa Certified - Ind. Temp. Range
- Atom™ x6200FE Dual Core @1.0GHz (no Turbo) 4.5W TDP no Graphics w/ IBECC, IHS and TCC, FuSa Certified- Ind. Temp. Range

Other Intel Atom™ x6000E, Pentium® and Celeron® N and J Series CPUs:

- Celeron® J6413 Quad Core @ 1.8GHz (3.0GHZ Turbo) 10W TDP - Comm. Temp. Range
- Celeron® N6211 Dual Core @1.2GHz (3.0GHZ Turbo) 6.5W TDP - Comm. Temp. Range
- Pentium® J6426 Quad Core @2.0GHz (3.0GHZ Turbo) 10W TDP - Comm. Temp. Range
- Pentium® N6415 Quad Core @1.2GHz (3.0GHZ Turbo) 6.5W TDP - Comm. Temp. Range
- Atom™ x6211E Dual Core @1.3GHz (3.0GHZ Turbo) 6W TDP w/ IBECC and IHS - Ind. Temp. Range
- Atom™ x6413E Quad Core @1.5GHz (3.0GHZ Turbo) 9W TDP w/ IBECC and IHS - Ind. Temp. Range
- Atom™ x6425E Quad Core @2.0GHz (3.0GHZ Turbo) 12W TDP w/ IBECC and IHS - Ind. Temp. Range
- Atom™ x6212RE Dual Core @1.2GHz (no Turbo) 6W TDP w/ IBECC, IHS and TCC - Ind. Temp. Range
- Atom™ x6414RE Quad Core @1.5GHz (no Turbo) 9W TDP w/ IBECC, IHS and TCC - Ind. Temp. Range
- Atom™ x6425RE Quad Core @1.9GHz (no Turbo) 12W TDP w/ IBECC, IHS and TCC - Ind. Temp. Range

(*) IHS: Integrated Heatspreader; TCC: Time Coordinated Computing

Memory

32-bit LPDDR4x Soldered Down Memory
Up to 16GB Quad Channel with In-Band Error Correction Code (IBECC, Safety Related feature) supported
4GB Dual Channel, 8GB or 16GB Quad Channel
Speed:4267MT/s single rank (1GB/2GB/4GB/8GB), 3733MT/s dual rank (16GB)

Graphics

Up to 3 independent displays
Integrated Gen11 UHD Graphics controller with up to 32 EU
4K HW decoding and encoding of HEVC (H.265), H.264, VP8/ VP9, WMV9/VC1 (decoding only)
DirectX 12.1, OpenGL ES 3.1, OpenGL 4.5, OpenCL™ 1.2, Vulkan 1.0

Video Interfaces

eDP 1.3 or Dual Channel 18/24bit LVDS interface (factory options)
2 x DP++ 1.4 or 1x DP++ 1.4 and 1x HDMI 1.4 interfaces

Video Resolution

Up to 4096 x 2160 @60Hz

Mass Storage

1 x external S-ATA Gen3 Channel
SDIO interface
Optional eMMC 5.1 drive soldered on-board (Safety Related)

PCI Express

Up to 4 x PCI-e Gen3 Lanes

Networking

2x Gigabit Ethernet PHY with precision clock synchronization and synchronous Ethernet clock output for IEEE 1588 (Safety Related – Black channel).
Optional SERDES (SGMII) Interface for additional third Gigabit Ethernet (factory option, alternative to fourth PCI-e lane)

USB

6 x USB 2.0 Host Ports
2 x USB 3.1 Gen2 Ports

Audio

HD Audio interface

Serial ports

2 x HS-UARTs (Safety Related)
2 x UARTs

CAN Bus

2 x CAN interfaces

Other Interfaces

Up to 14x GPIOs
SM Bus
Power Management Signals
I2C Bus
1x SPI interface for boot
1x General Purpose SPI or eSPI (Factory Alternatives)

Functional Safety Features

FuSa Interface signals for IEC 61508 and ISO 13849

Power supply voltage: +5V_{DC} and +3.3V_RTC

Operating System

Microsoft® Windows 10 Enterprise (64 bit)
Linux Yocto 64-bit

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version -40°C ÷ +85°C **.

Dimensions: 50 x82 mm (1.97” x 3.23”)

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*
Please also check paragraph 4.1

2.3 Electrical Specifications

According to SMARC specifications, the SM-C93 module needs to be supplied only with an external +5V_{DC} power supply.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout). All remaining voltages needed for board's working are generated internally from +5V_{DC} power rail.

2.3.1 Power Consumption

SM-C93 module, like all SMARC modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source. Anyway, it has been possible to measure power consumption directly on VDD_IN power rail (5V_{DC}) that supplies the board. Power consumption must be intended as average value (30 seconds acquisition).

Status	Configuration															
	Intel Atom™ x6425E 16GB LPDDR4 128GB eMMC 4 x PCI-e LVDS and 2x DP++ TPM 2.0 Comm Temp Range				Intel Pentium® J6425 8GB LPDDR4 128GB eMMC 4 x PCI-e LVDS and 2x DP++ TPM 2.0 Comm Temp Range				Intel Atom™ x6425RE 16GB LPDDR4 128GB eMMC 4 x PCI-e eDP and 2x DP++ TPM 2.0 Ind Temp Range				Intel Atom™ x6427FE 8GB LPDDR4 64GB eMMC 4 x PCI-e LVDS and 2x DP++ TPM 2.0 FuSa Ind Temp Range			
	Avg Value		Peak Value		Avg Value		Peak Value		Avg Value		Peak Value		Avg Value		Peak Value	
Idle – (Win10) – power saving configuration	3.5W	0.7A	6.22W	1.24A	2.46W	0.49A	6.79W	1.35A	6W	1.2A	6.3W	1.26A	6.97W	1.39A	9.71W	1.94A
OS Boot – (Win10)	5.68W	1.13A	12.63W	2.52A	6.28W	1.25A	9.41W	1.88A	7.85W	1.57A	13.6W	2.72A	6.83W	1.36A	12.61W	2.52A
Video reproduction @1080p	4.34W	0.54A	9.96W	2A	4.27W	0.85A	11W	2.2A	6.53W	1.31A	9.12W	1.82A	7.38W	1.47A	9.49W	1.9A
Video reproduction 4K	6.71W	1.34A	10.64W	2.12A	6W	1.2A	11.83W	2.36A	7.76W	1.55A	10.47W	2.09A	7.76W	1.55A	10.47A	2.09A
Intel PTU (package power limit and TURBO Enabled)	16.12W	3.22A	19.96W	3.98A	11.22W	2.24A	16.29W	3.25A	13.68W	2.73A	14.52W	2.9A	13.39W	2.68A	14.03W	2.8A
Intel PTU (without power limits and TURBO Enabled)	22.91W	4.58A	24.2W	4.83A	17.36W	3.47A	18.92W	3.98A	14.46W	2.89A	15.74W	3.15A	14.39W	2.87A	15.6W	3.12A

Independently by the SOC mounted onboard, the following power consumptions are common to all boards:

Battery Backup power consumption:	3.11µA
Soft-Off State power consumption:	174mA
Suspend State power consumption:	176mA

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. +5V voltage directly coming from the card edge connector, internally named as 5V_DSW.

VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card for supplying the RTC clock on the Elkhart Lake SOCs.

+3.3V_DSW: +3.3 Deep Sleep Well, derived internally from 5V_DSW

+3.3V_RUN: +3.3 Switched voltage, derived internally from +3.3V_DSW

+3.3V_ALW: +3.3 Always-on voltage, derived internally from +3.3V_DSW

+1.8V_ALW: +1.8 Always-on voltage, derived internally from 5V_DSW

+1.8V_RUN: +1.8 Switched voltage, derived internally from +1.8V_ALW

+1.8V_DSW: +1.8 Deep sleep well, derived internally from +3.3V_DSW

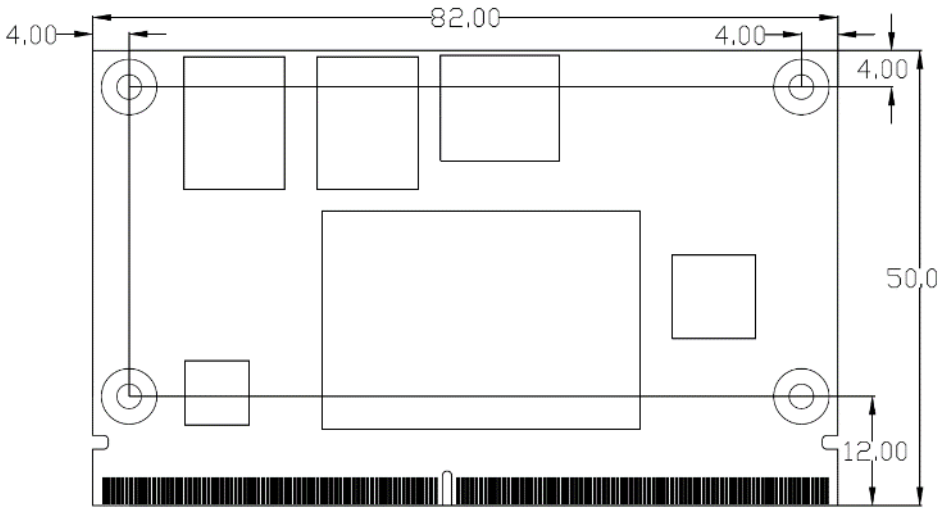
2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97” x 3.23”) including the pin numbering and edge finger pattern.

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of SM-C93 will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector’s height, if there is the need to place components on the carrier board in the zone below the SMARC module.



2.5 Supported Operating Systems

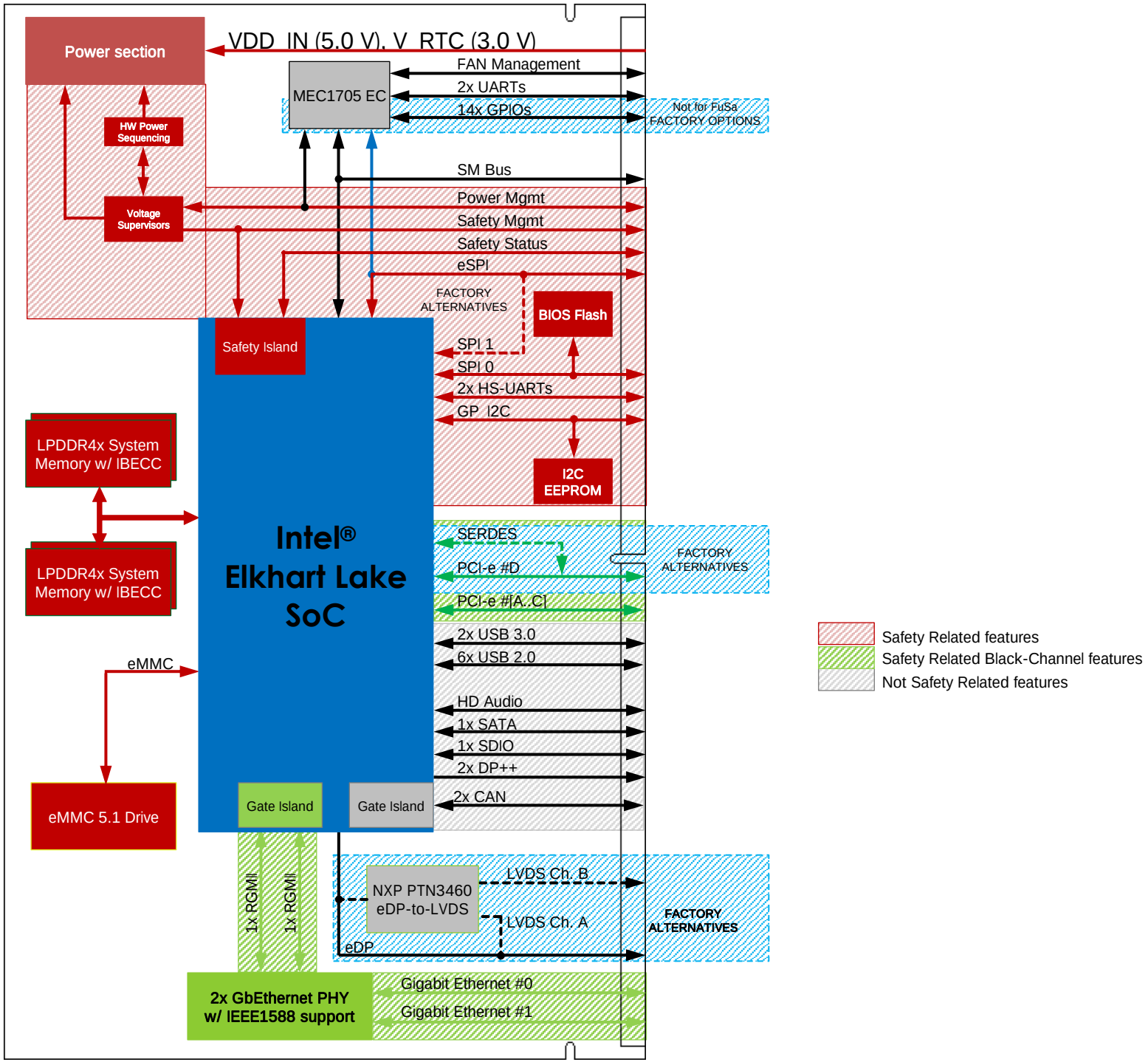
SM-C93 module supports the following operating systems:

- Microsoft® Windows 10 Enterprise (64 bit)
- Linux Yocto 64-bit

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the SMARC board and the Carrier Board, assuming that the Carrier Board is designed following SECO SMARC Design Guide, with the same IC’s.

For further details, please visit https://www.seco.com.

2.6 Block Diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors description

3.1 Introduction

According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

TOP SIDE

Card Edge golden finger, pin P1

Card Edge golden finger, pin P156

BOTTOM SIDE

Card Edge golden finger, pin S158

Card Edge golden finger, pin S1

3.2 Connectors description

3.2.1 SMARC Connector

According to SMARC Rel 2.1 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC Rel 2.1 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals reported on the card edge connector.

For accurate signals description, please consult the following paragraphs.

SMARC Golden Finger Connector – CN1

TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	PROCHOT	I/O	FUSA
MANAGEMENT	I	SMB_ALERT#	P1	S2	FUSA_PWRFAIL#	I/O	FUSA
		GND	P2	S3	GND		
		N.C.	P3	S4	CHXPMICEN	I	FUSA
		N.C	P4	S5	N.C.		
GBE	I/O	GBE1_SDP	P5	S6	N.C.		
GBE	I/O	GBE0_SDP	P6	S7	N.C.		
		N.C.	P7	S8	N.C.		
		N.C	P8	S9	N.C.		
		GND	P9	S10	GND		
		N.C.	P10	S11	N.C.		
		N.C	P11	S12	N.C.		
		GND	P12	S13	GND		
		N.C.	P13	S14	N.C.		
		N.C	P14	S15	N.C.		
		GND	P15	S16	GND		
		N.C.	P16	S17	GBE1_MDI0+	I/O	GBE

		N.C	P17	S18	GBE1_MDI0-	I/O	GBE
		GND	P18	S19	GBE1_LINK100#	O	
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+	I/O	GBE
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-	I/O	GBE
GBE	O	GBE0_LINK100#	P21	S22	GBE1_LINK1000#	O	
GBE	O	GBE0_LINK1000#	P22	S23	GBE1_MDI2+	I/O	GBE
GBE	I/O	GBE0_MDI2-	P23	S24	GBE1_MDI2-	I/O	GBE
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3-	I/O	GBE
GBE	I/O	GBE0_MDI1-	P26	S27	GBE1_MDI3+	I/O	GBE
GBE	I/O	GBE0_MDI1+	P27	S28	N.C.		
		N.C.	P28	S29	SERDES_0_TX+ / PCIE_D_TX+	O	SERDES / PCI-e
GBE	I/O	GBE0_MDI0-	P29	S30	SERDES_0_TX- / PCIE_D_TX-	O	SERDES / PCI-e
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	O	GBE
		N.C.	P31	S32	SERDES_0_RX+ / PCIE_D_RX+	I	SERDES / PCI-e
		GND	P32	S33	SERDES_0_RX- / PCIE_D_RX-	I	SERDES / PCI-e
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	AUDIO_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	ESPI_ALERT0#	I	ESPI INTERFACE
SPI 0 INTERFACE	O	SPI0_CS0#	P43	S44	ESPI_ALERT1#	I	ESPI INTERFACE

SPI 0 INTERFACE	O	SPI0_CK	P44	S45	MDIO_CLK	O	SERDES
SPI 0 INTERFACE	I	SPI0_DIN	P45	S46	MDIO_DAT	I/O	SERDES
SPI 0 INTERFACE	O	SPI0_DO	P46	S47	GND		
		GND	P47	S48	I2C_GP_CK	I/O	I2C
SATA	O	SATA_TX+	P48	S49	I2C_GP_DAT	I/O	I2C
SATA	O	SATA_TX-	P49	S50	HDA_SYNC	I/O	HD AUDIO
		GND	P50	S51	HDA_SDO	O	HD AUDIO
SATA	I	SATA_RX+	P51	S52	HDA_SDI	I	HD AUDIO
SATA	I	SATA_RX-	P52	S53	HDA_CK	O	HD AUDIO
		GND	P53	S54	SATA_ACT#	O	SATA
SPI 1 / eSPI INTERFACE	O	SPI1_CS0#/ESPI_CS0#	P54	S55	USB5_EN_OC#	I/O	USB
SPI 1 / eSPI INTERFACE		SPI1_CS1#/ESPI_CS1#	P55	S56	ESPI_IO_2	I/O	eSPI INTERFACE
SPI 1 / eSPI INTERFACE	O	SPI1_CK / ESPI_CK	P56	S57	ESPI_IO_3	I/O	eSPI INTERFACE
SPI 1 / eSPI INTERFACE	I/O	SPI1_DIN / ESPI_IO_1	P57	S58	ESPI_RESET#	O	eSPI INTERFACE
SPI 1 / eSPI INTERFACE	I/O	SPI1_DO / ESPI_IO_0	P58	S59	USB5+	I/O	USB
		GND	P59	S60	USB5-	I/O	USB
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	USB3_SSTX+	O	USB
USB	I/O	USB0_EN_OC#	P62	S63	USB3_SSTX-	O	USB
		N.C.	P63	S64	GND		
		N.C.	P64	S65	USB3_SSRX+	I	USB
USB	I/O	USB1+	P65	S66	USB3_SSRX-	I	USB
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		
USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SSTX-	O	USB
FUSA	I/O	SPIM_MOSI	P72	S73	GND		
FUSA	I/O	THERMTRIP	P73	S74	USB2_SSRX+	I	USB

USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCI_e	O	PCIE_A_RST#	P75	S76	PCIE_B_RST#	O	PCI-e
USB	I/O	USB4_EN_OC#	P76	S77	PCIE_C_RST#	O	PCI-e
PCI-e	I	PCIE_B_CLKREQ#	P77	S78	PCIE_C_RX+	I	PCI-e
PCI-e	I	PCIE_A_CLKREQ#	P78	S79	PCIE_C_RX-	I	PCI-e
		GND	P79	S80	GND		PCI-e
PCI-e	O	PCIE_C_REFCK+	P80	S81	PCIE_C_TX+	O	PCI-e
PCI-e	O	PCIE_C_REFCK-	P81	S82	PCIE_C_TX-	O	PCI-e
		GND	P82	S83	GND		
PCI-e	O	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCK+	O	PCI-e
PCI-e	O	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCK-	O	PCI-e
		GND	P85	S86	GND		
PCI-e	I	PCIE_A_RX+	P86	S87	PCIE_B_RX+	I	PCI-e
PCI-e	I	PCIE_A_RX-	P87	S88	PCIE_B_RX-	I	PCI-e
		GND	P88	S89	GND		
PCI-e	O	PCIE_A_TX+	P89	S90	PCIE_B_TX+	O	PCI-e
PCI-e	O	PCIE_A_TX-	P90	S91	PCIE_B_TX-	O	PCI-e
		GND	P91	S92	GND		
DP++ INTERFACE #1	O	DP1_LANE0+	P92	S93	DP0_LANE0+	O	DP++ INTERFACE #0
DP++ INTERFACE #1	O	DP1_LANE0-	P93	S94	DP0_LANE0-	O	DP++ INTERFACE #0
		GND	P94	S95	DP0_AUX_SEL	I	DP++ INTERFACE #0
DP++ INTERFACE #1	O	DP1_LANE1+	P95	S96	DP0_LANE1+	O	DP++ INTERFACE #0
DP++ INTERFACE #1	O	DP1_LANE1-	P96	S97	DP0_LANE1-	O	DP++ INTERFACE #0
		GND	P97	S98	DP0_HPD	I	DP++ INTERFACE #0
DP++ INTERFACE #1	O	DP1_LANE2+	P98	S99	DP0_LANE2+	O	DP++ INTERFACE #0
DP++ INTERFACE #1	O	DP1_LANE2-	P99	S100	DP0_LANE2-	O	DP++ INTERFACE #0
		GND	P100	S101	GND		
DP++ INTERFACE #1	O	DP1_LANE3+	P101	S102	DP0_LANE3+	O	DP++ INTERFACE #0
DP++ INTERFACE #1	O	DP1_LANE3-	P102	S103	DP0_LANE3-	O	DP++ INTERFACE #0
		GND	P103	S104	N.C.		

DP++ INTERFACE #1	I	DP1_HPD	P104	S105	DP0_AUX+	I/O	DP++ INTERFACE #0
DP++ INTERFACE #1	I/O	DP1_AUX+	P105	S106	DP0_AUX-	I/O	DP++ INTERFACE #0
DP++ INTERFACE #1	I/O	DP1_AUX-	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT
DP++ INTERFACE #1	I	DP1_AUX_SEL	P107	S108	LVDS1_CK+	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO0 / OKNOK0	P108	S109	LVDS1_CK-	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO1 / OKNOK1	P109	S110	GND		
GPIO / FUSA	I/O	GPIO2 / ALERT#	P110	S111	LVDS1_0+	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO3 / SPIS_CS#	P111	S112	LVDS1_0-	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO4 / SPIS_SCLK	P112	S113	N.C.		
GPIO / FUSA	I/O	GPIO5 / SPIS_MISO	P113	S114	LVDS1_1+	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO6 / SPIS_MOSI	P114	S115	LVDS1_1-	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO7 / CHXPMIC_EN	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO / FUSA	I/O	GPIO8 / CHX_RLYSWITCH	P116	S117	LVDS1_2+	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO9 / CHXOKNOX0	P117	S118	LVDS1_2-	O	PRIMARY_DISPLAY
GPIO / FUSA	I/O	GPIO10 / CHXOKNOK1	P118	S119	GND		
GPIO / FUSA	I/O	GPIO11 / SPIM_CS#	P119	S120	LVDS1_3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO13 / SPIM_MISO	I/O	GPIO / FUSA
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_0+ / eDP0_TX0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_0- / eDP0_TX0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_1+ / eDP0_TX1+	O	PRIMARY_DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_1- / eDP0_TX1+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_2+ / eDP0_TX2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_2- / eDP0_TX2-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK+ / eDP0_AUX+	O	PRIMARY_DISPLAY

ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK- / eDP0_AUX-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_3+ / eDP0_TX3+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_3- / eDP0_TX3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C_LCD_CK	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C_LCD_DAT	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12 / SPIM_SCLK	I/O	GPIO / FUSA
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	eDP0_HPD	I	PRIMARY_DISPLAY
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
		N.C.	P145	S146	PCIE_WAKE#	I	PCI_e
		N.C.	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT
				S158	GND		

3.2.1.1 LCD Display Support Signals

The Intel® family of SOCs formerly coded as Elkhart Lake offers signal for direct driving of a panel and its display's backlight: enabling signals for panel (LCD0_VDD_EN) and backlight (LCD0_BKLT_EN), Backlight Brightness Control signal (LCD0_BKLT_PWM). These signals have an electrical of +1.8V_RUN, so they will be adapted/level shifted by the carrier board for external use.

There are also the signals necessary for driving I2C Data and Clock lines of LCD EDID EEPROM.

The panel control signals are:

LCD0_VDD_EN: Panel #0 Panel enable signal. Active high signal, +1.8V_RUN electrical level Output.

LCD0_BKLT_EN: Panel #0 Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. Active high signal, +1.8V_RUN electrical level Output.

LCD0_BKLT_PWM: This signal can be used to adjust the Panel #0 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level with a 2.2kΩ pull-up resistor.

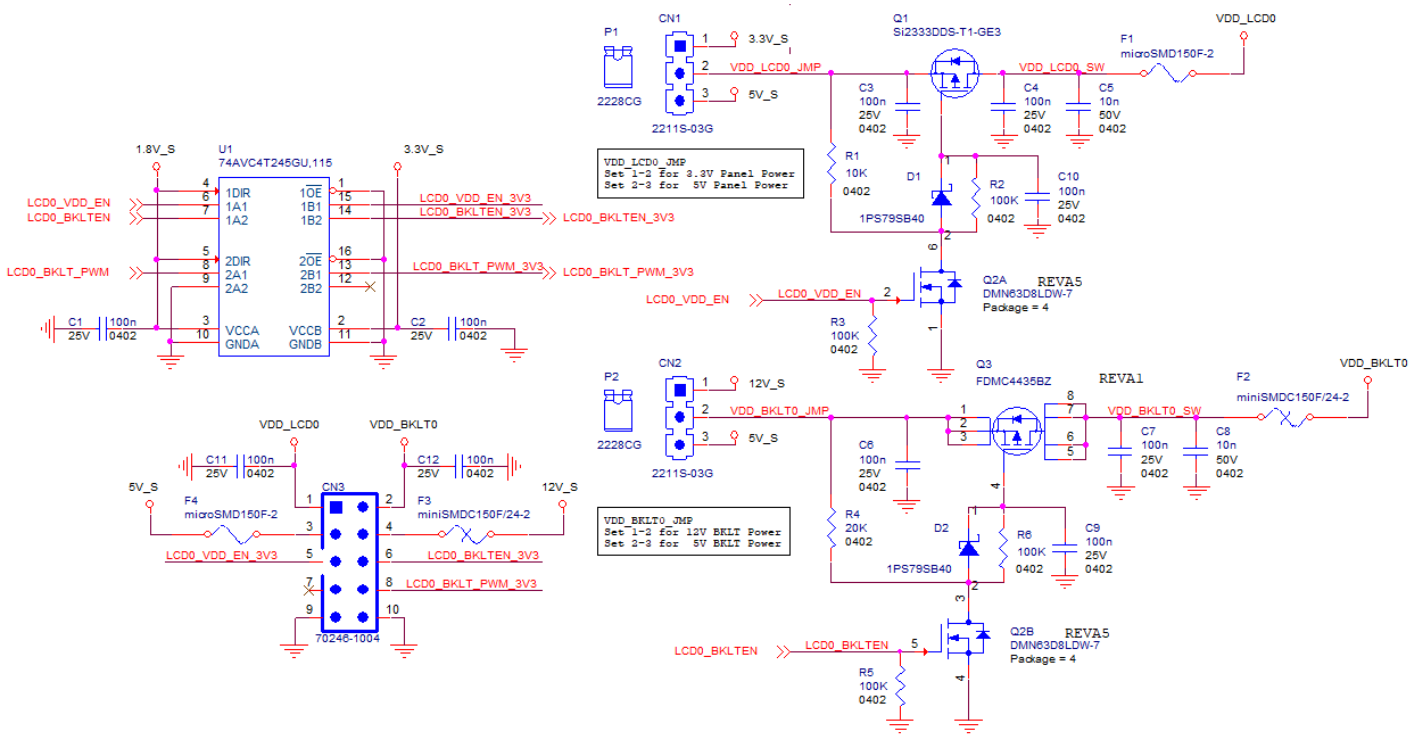
I2C_LCD_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level with a 2.2kΩ pull-up resistor.

Please refer to the following schematics as an example of implementation for LCD and backlight support signals driving connection + voltage level shifters on the carrier board.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design



3.2.1.2 eDP / Dual Channel LVDS (factory alternatives)

The Intel® family of SOCs formerly coded as Elkhart Lake offers a wide range of single and multi-purpose Digital Display Interfaces.

SM-C93 offers one embedded Display Port (eDP) interface or Dual Channel LVDS (factory alternatives), two multimode display ports (DP++) or one multimode display port (DP++) and one HDMI.

The LVDS interface, which is frequently used in many application fields, is not directly supported by the SOC. For this reason, considering that LVDS dual channel interfaces can be factory alternative on the same pins with eDP interface, on SM-C93 module can be implemented an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode). Such an interface is derived from the SOCs' dedicated eDP Interface.

> **!** Please remember that LVDS interface is not native for the Intel® family of SOCs formerly coded as Elkhart Lake, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is possible to have available LVDS or eDP interface. Please take care of specifying if it is necessary LVDS interface or eDP, before placing an order of SM-C93 module.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for Channel #0 are LVDS:

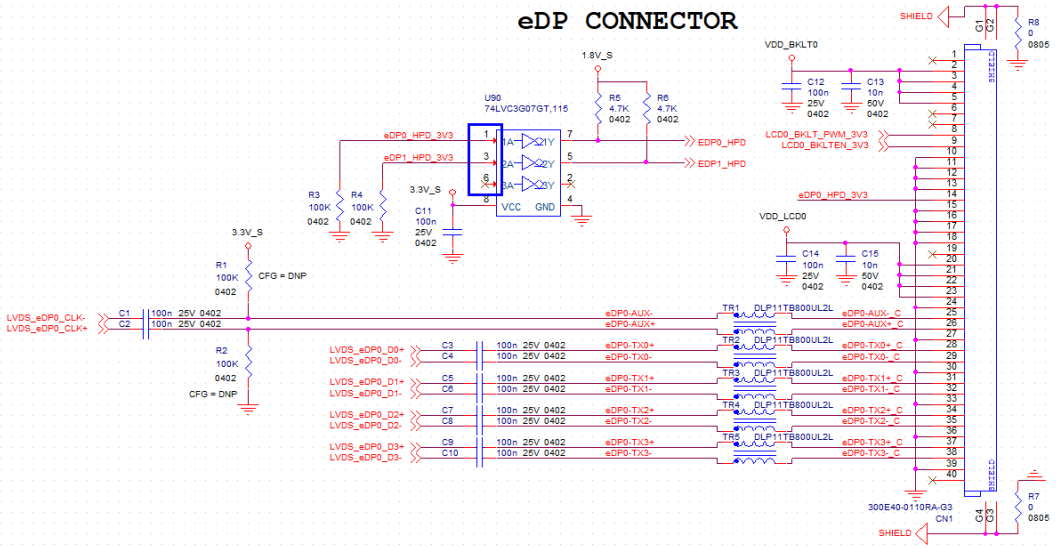
LVDS0_0+/LVDS0_0-: LVDS Channel #0 differential data pair #0.
LVDS0_1+/LVDS0_1-: LVDS Channel #0 differential data pair #1.
LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2.
LVDS0_3+/LVDS0_3-: LVDS Channel #0 differential data pair #3.
LVDS0_CK+/LVDS0_CK-: LVDS Channel #0 differential Clock.

OR the signals for Channel #0 are eDP:

eDP0_TX0+/ eDP0_TX0-: eDP Channel #0 differential data pair #0.
eDP0_TX1+/ eDP0_TX1-: eDP Channel #0 differential data pair #1.
eDP0_TX2+/ eDP0_TX2-: eDP Channel #0 differential data pair #2.
eDP0_TX3+/ eDP0_TX3-: eDP Channel #0 differential data pair #3.
eDP0_AUX+/ eDP0_AUX-: eDP Channel #0 differential Clock.

eDP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

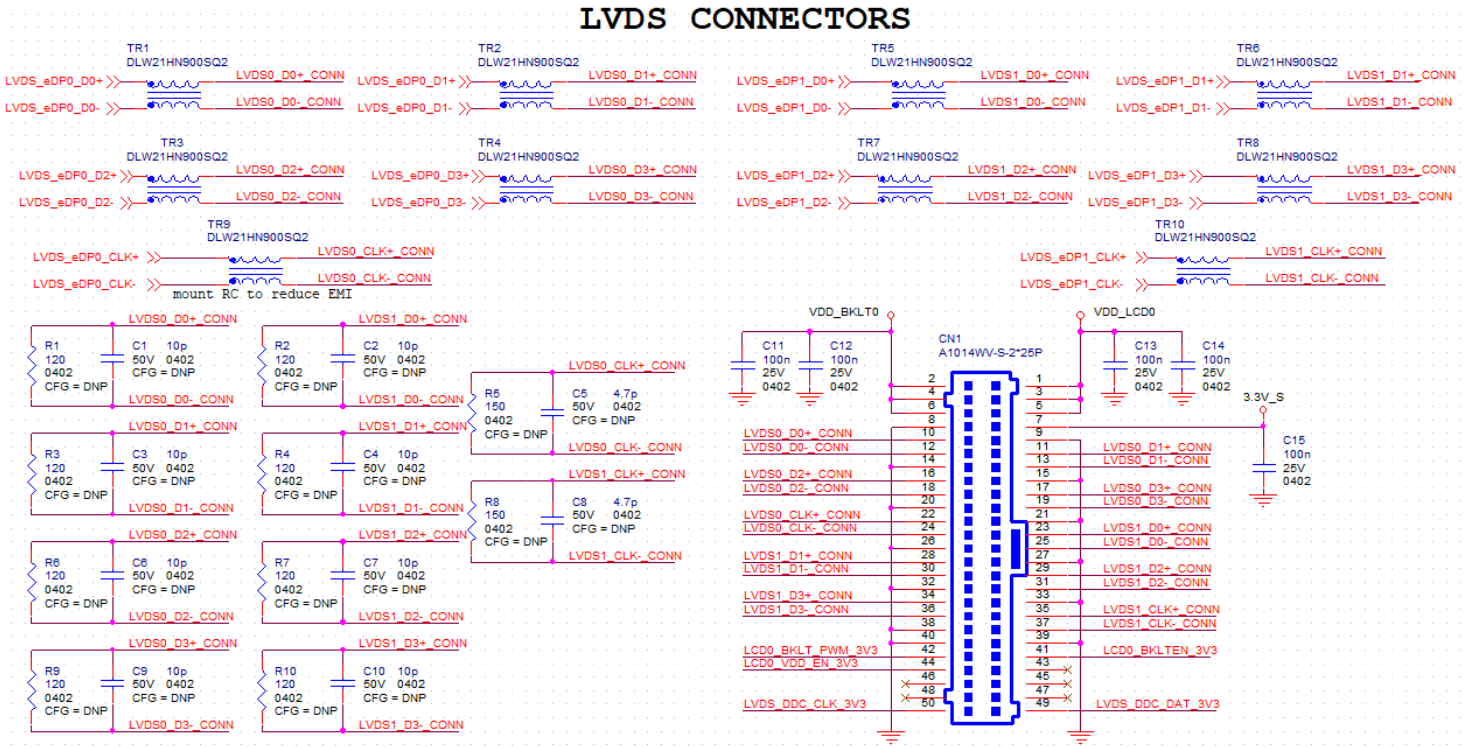
Please refer to the following schematics as an example of connection of eDP interface on the carrier board. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation.



The signals for Channel #1 are LVDS, when this interface is selected in factory board configuration, otherwise these pins will be not connected.

LVDS1_1+ / LVDS1_0- : LVDS Channel #1 differential data pair #0
LVDS1_1+/ LVDS1_1-: LVDS Channel #1 differential data pair #1
LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2
LVDS1_3+/ LVDS1_3-: LVDS Channel #1 differential data pair #3
LVDS1_CK+/ LVDS1_CK-: LVDS Channel #1 differential Clock

Please refer to the following schematics as an example of connection of dual channel LVDS interface on the carrier board, with EMI filtering section included.



3.2.1.3 HDMI / DP++ (factory alternatives) interface signals

As described in the previous paragraph, the Intel® family of SOCs formerly coded as Elkhart Lake offers, as secondary display interface, a native multimode Digital Display Interface, configurable as a factory alternative to work as a multimode Display Port (DP++) with a resolution up to 4096 x 2160 @60Hz or HDMI v1.4 with a resolution up to 3840 x 2160 @30Hz.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for the Channel are HDMI:

HDMI_D0+/HDMI_D0-: HDMI Output Differential Pair #0

HDMI_D1+/HDMI_D1-: HDMI Output Differential Pair #1

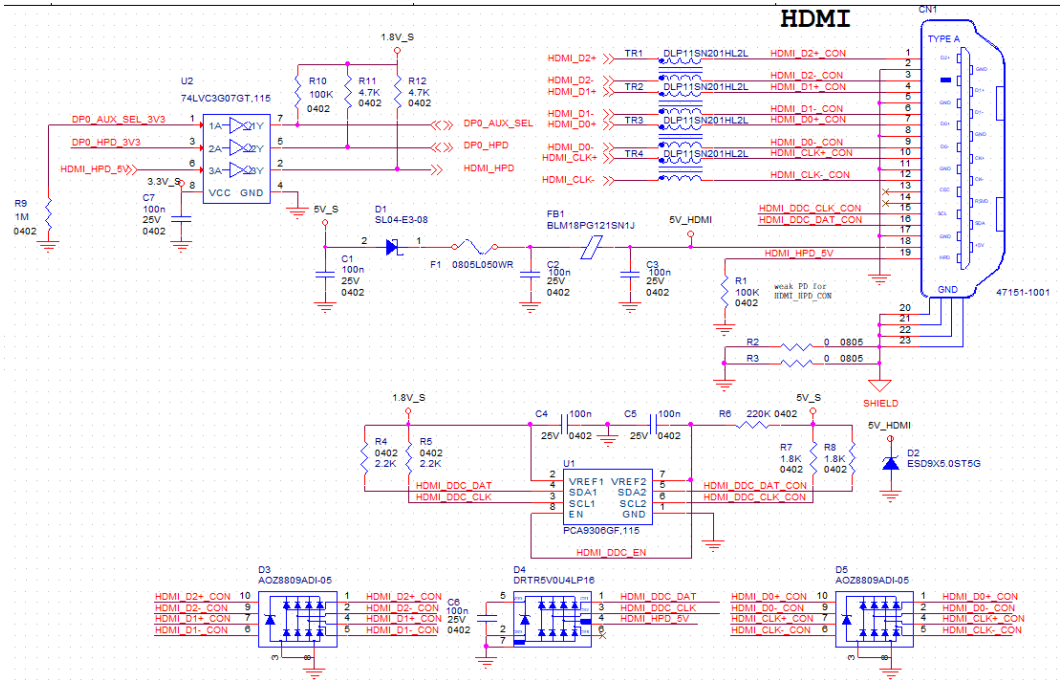
HDMI_D2+/HDMI_D2-: HDMI Output Differential Pair #2

HDMI_CK+/HDMI_CK-: HDMI Differential Clock

HDMI_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

HDMI_CTRL_CK: DDC Clock line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor



Please refer to the above schematics as an example of connection of HDMI interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression, as well as common mode choke inductors for EMI purpose. Voltage level shifters are necessary on Control data/Clock signals, as well as for Hot Plug Detect signal.

OR the signals for the Channel are DP++:

DP1_LANE0+/ DP1_LANE0-: DP Channel #1 Output Differential Pair #0

DP1_LANE1+/ DP1_LANE1-: DP Channel #1 Output Differential Pair #1

DP1_LANE2+/ DP1_LANE2-: DP Channel #1 Output Differential Pair #2

DP1_LANE3+/ DP1_LANE3-: DP Channel #1 Output Differential Pair #3

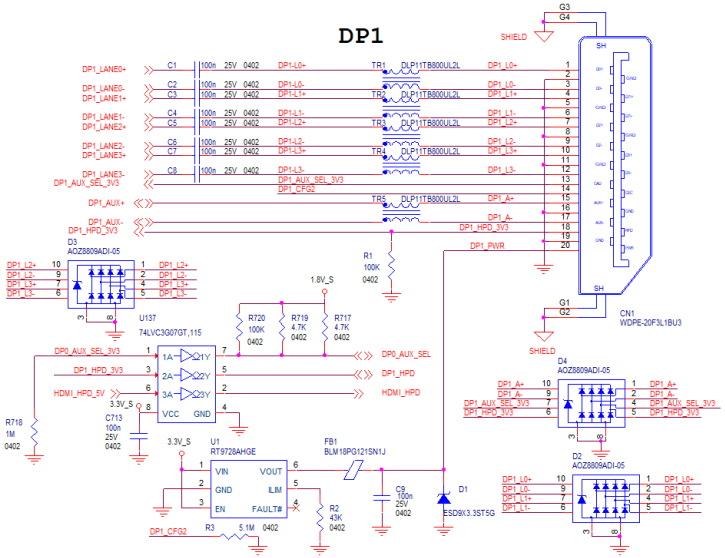
DP1_AUX+: DDC Clock line for DP Channel #1. Bidirectional signal, +3.3V_RUN electrical level with a 100kΩ pull-up resistor

DP1_AUX-: DDC Data line for DP Channel #1. Bidirectional signal, +3.3V_RUN electrical level with a 100kΩ pull-up resistor

DP1_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

DP1_AUX_SEL: Select input signal to switch between I2C Clock/Data for HDMI (high level) and Display Port Auxiliary Channel for DP/HDMI (low level). 1MΩ pull-down resistor is placed on module for this signal.

Please refer to the following schematics as an example of connection of DP interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation. Switch with settable current limit on power lines are recommended.



3.2.1.4 DP++ interface signals

As described in the previous paragraph, the Intel® family of SOCs formerly coded as Elkhart Lake offers a native multimode Display Port (DP) interface, with a resolution up to 4096 x 2160 @60Hz

The signals related to DP++ are as follows:

DP0_LANE0+/ DP0_LANE0-: DP Channel #0 differential data pair #0.

DP0_LANE1+/ DP0_LANE1-: DP Channel #0 differential data pair #1.

DP0_LANE2+/ DP0_LANE2-: DP Channel #0 differential data pair #2.

DP0_LANE3+/ DP0_LANE3-: DP Channel #0 differential data pair #3.

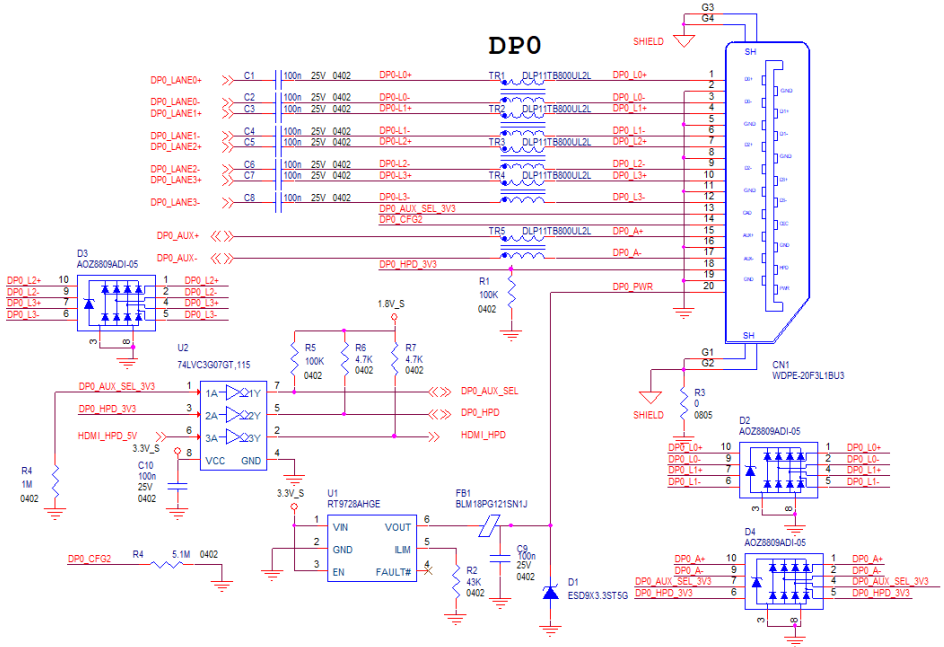
DP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

DP0_AUX+: DDC Clock line for DP Channel #0. Bidirectional signal, +3.3V_RUN electrical level with a 100kΩ pull-up resistor

DP0_AUX-: DDC Data line for DP Channel #0. Bidirectional signal, +3.3V_RUN electrical level with a 100kΩ pull-up resistor

DP0_AUX_SEL: Select input signal to switch between I2C Clock/Data for HDMI (high level) and Display Port Auxiliary Channel for DP/HDMI (low level). 1MΩ pull-down resistor is placed on module for this signal.

Please refer to the following schematics as an example of connection of DP interface on the carrier board, with Voltage clamping diodes highly recommended on all



signal lines for ESD suppression. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation. Switch with settable current limit on power lines are recommended.

3.2.1.5 SATA interface signals

The Intel® family of SOCs formerly coded as Elkhart Lake offers one S-ATA interface.

The interface is Gen3 compliant, with support of 1.5Gbps, 3.0 Gbps and 6.0 Gbps data rates

Here following the signals related to SATA interface:

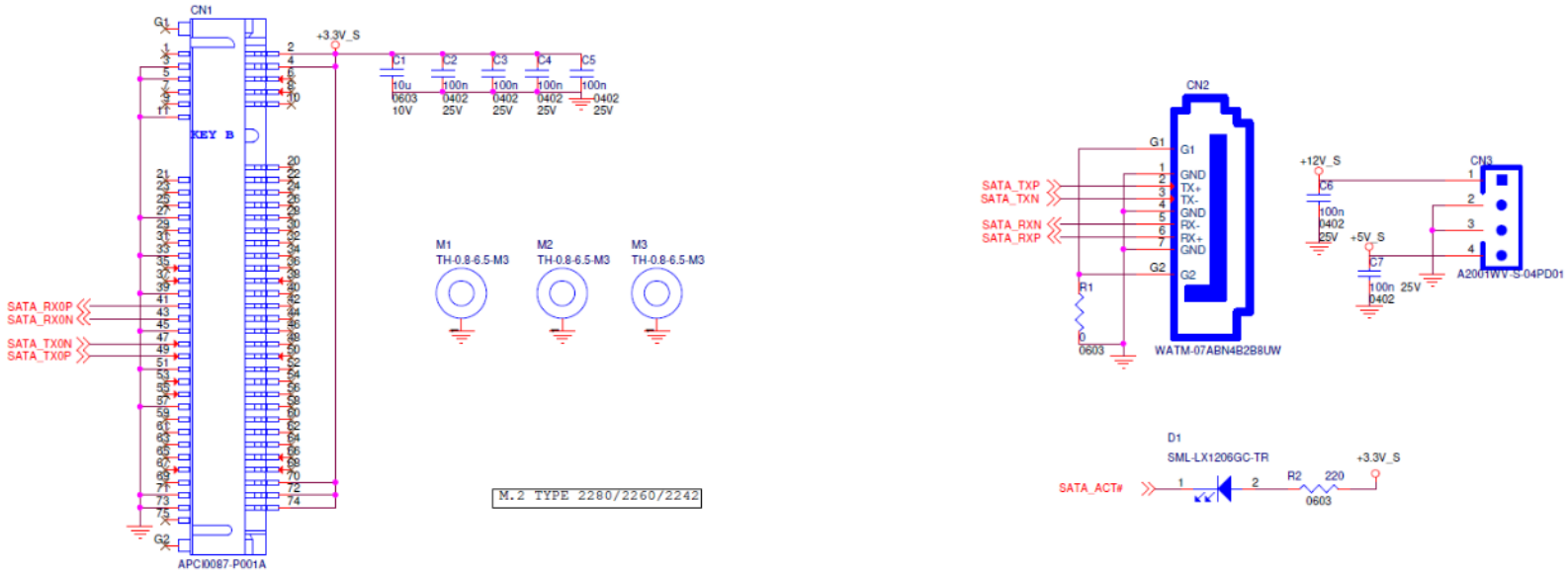
SATA_TX+/SATA_TX-: Serial ATA Channel #1 Transmit differential pair

SATA_RX+/SATA_RX-: Serial ATA Channel #1 Receive differential pair

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_RUN voltage

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to a SATA M 7p connector or switched for an M.2 SSD Slot, which allow plugging M.2 Socket 2 Key B Solid State Drives. Please refer to the following schematics as an example of connection of SATA interface on the carrier board to selected connector.



3.2.1.6 SDI/O interface signals

The Intel® family of SOCs formerly coded as Elkhart Lake offers one SD Card controller, able to support SD Card 3.0 interface.

Such an SD controller complies with SD Host Controller Standard Specification version 3.01 and only supports devices for data storage.

The SD port is externally accessible through the SD Card Slot connector, can work in 1-bit and 4-bit mode operation with data rate up to 104MB/s.

The signals related to SDIO are as follows:

SDIO_WP: Write Protect input, electrical level +3.3V_RUN with 10kΩ pull-up resistor. It is used to communicate the status of Write Protect switch of the external SD card. Since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal must be tied to GND, otherwise the OS will always consider the card as protected from writing.

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_RUN, used to send command from Host (Intel processor) to the connected card, and to send the response from the card to the Host.

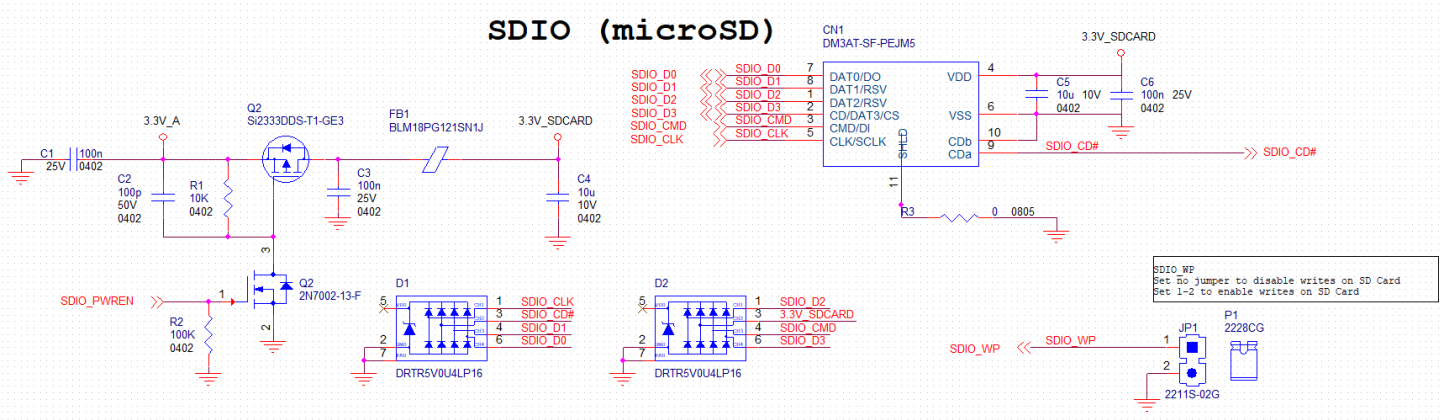
SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), 50 MHz maximum frequency for SD/SDIO High Speed Mode.

SDIO_PWR_EN: SDIO Power Enable output, active high signal, electrical level +3.3V_RUN. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SD Card data bus. SDIO_D0 signal is used for all communication modes. SDIO_[D1÷D3] signals are required for 4-bit communication mode.

Please refer to the following schematics as an example of connection of SDIO interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression.



3.2.1.7 SPI interface signals

The Intel® family of SOCs formerly coded as Elkhart Lake offers also one dedicated Serial Peripheral Interface (SPI0) for boot device purpose and one general purpose Serial Peripheral Interface (SPI1) or eSPI (factory alternatives).

The signals related to SPI0 are as follows:

SPI0_CS0#: SPI channel #0 primary Chip select, active low output signal. Electrical level +1.8V_ALW

On the same bus there is a second SPI slave device (BIOS flash boot device), mounted on the module, connected to a dedicated chip select signal

SPI0_CK: SPI channel #0 Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_ALW

SPI0_DIN: SPI channel #0 Master Data Input, electrical level +1.8V_ALW

SPI0_DO: SPI channel #0 Master Data Output, electrical level +1.8V_ALW

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for the SPI1 are general-purpose SPI bus:

SPI1_CS0#: SPI channel #1 primary Chip select, active low output signal. Electrical level +1.8V_ALW

SPI1_CS1#: SPI channel #1 secondary Chip select, active low output signal. Electrical level +1.8V_ALW

SPI1_CK: SPI channel #1 Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_ALW

SPI1_DIN: SPI0 channel #1 Master Data Input, electrical level +1.8V_ALW

SPI1_DO: SPI0 channel #1 Master Data Output, electrical level +1.8V_ALW

OR the signals for the SPI1 are Enhanced Serial Peripheral Interface (eSPI) bus:

ESPI_CK: ESPI Master Clock Output. Electrical level +1.8V_ALW. The reference timing signal for all the serial input and output operations

ESPI_CS0#: ESPI Master Chip Select Output #0. Electrical level +1.8V_ALW. Driven low by the processor to select the ESPI slave device on the carrier board.

ESPI_CS1#: ESPI Master Chip Select Output #1. Electrical level +1.8V_ALW. This signal must be used only in case there are two ESPI devices on the carrier board, and the first chip select signal (ESPI_CS0#) has already been used. It must not be used in case there is only one ESPI device

ESPI_IO_[0:3]: ESPI Master Data Bidirectional. Electrical level +1.8V_ALW. Data transfer between the master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).

ESPI_RESET#: ESPI Reset. Output. Electrical level +1.8V_ALW with 75kΩ pull-down resistor. Reset the ESPI interface for both master and slaves.

ESPI_ALERT0#: Alert signal driven by the slave ESPI slave device #0. Input. Electrical level +1.8V_ALW

ESPI_ALERT1#: Alert signal driven by the slave ESPI slave device #1. Input. Electrical level +1.8V_ALW

3.2.1.8 Audio interface signals

The Intel® family of SOCs formerly coded as Elkhart Lake supports I2S and HD audio format, thanks to native support offered by the processor to this audio codec standard.

Here are following the signals related to I2S Audio interface:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_LRCK: Left& Right audio interface #0 synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDOUT: Digital audio interface #0 Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDIN: Digital audio interface #0 Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_CK: Digital audio interface #0 clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

All these signals can be connected, on the Carrier Board, to an I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

Here are following the signals related to HD Audio interface:

HDA_SYNC: Synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

HDA_SDO: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

HDA_SDI: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

HDA_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

HDA_RST#: Digital Audio Reset. This signal is multiplexed with GPIO4. This pin has to be defined via BIOS so that GPIO4/HDA_RST# is in HDA_RST# modality.

All these signals have to be connected, on the Carrier Board, to an HD Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.1.9 I2C / SM bus Interface

The Intel® family of SOCs formerly coded as Elkhart Lake supports one general purpose I2C interface and one power management SM bus.

Here are following the signals related to general purpose I2C interface:

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with 2.2kΩ pull-up resistor

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with 2.2kΩ pull-up resistor

Here are following the signals related to power management SM bus:

I2C_PM_CK:SMB Power management clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor. This signal is managed by the Embedded controller MEC1705 from Microchip.

I2C_PM_DAT: SMB Power management data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor This signal is managed by the Embedded controller MEC1705 from Microchip.

3.2.1.10 Asynchronous Serial Ports (UART) interface signals

The Intel® family of SOCs formerly coded as Elkhart Lake offers in its Low Power Sub System (LPSS) two high speed UART, with a maximum speed of 115,200 kb/s or 3.6864Mb/s depending on Industry standards.

In addition, two additional UART are offered and managed by the Embedded controller MEC1705 from Microchip

SER0_TX: UART #0 Interface, Serial data Transmit (output) line, 1.8V_RUN electrical level. It is managed by Microchip MEC1705 controller.

SER0_RX: UART #0 Interface, Serial data Receive (input) line, 1.8V_RUN electrical level. It is managed by Microchip MEC1705 controller.

SER0_RTS#: UART #0 Interface, Handshake signal, Request to Send (output) line, 1.8V_ RUN electrical level

SER0_CTS#: UART #0 Interface, Handshake signal, Clear to Send (Input) line, 1.8V_ RUN electrical level

SER1_TX: HS-UART #0 Interface, Serial data Transmit (output) line, 1.8V_ RUN electrical level. It is directly managed by Intel processor.

SER1_RX: HS-UART #0 Interface, Serial data Receive (input) line, 1.8V_ RUN electrical level. It is directly managed by Intel processor.

SER2_TX: UART #1 Interface, Serial data Transmit (output) line, 1.8V_ RUN electrical level. It is managed by Microchip MEC1705 controller.

SER2_RX: UART #1 Interface, Serial data Receive (input) line, 1.8V_ RUN electrical level. It is managed by Microchip MEC1705 controller.

SER2_RTS#: UART #1 Interface, Handshake signal, Request to Send (output) line, 1.8V_ RUN electrical level.

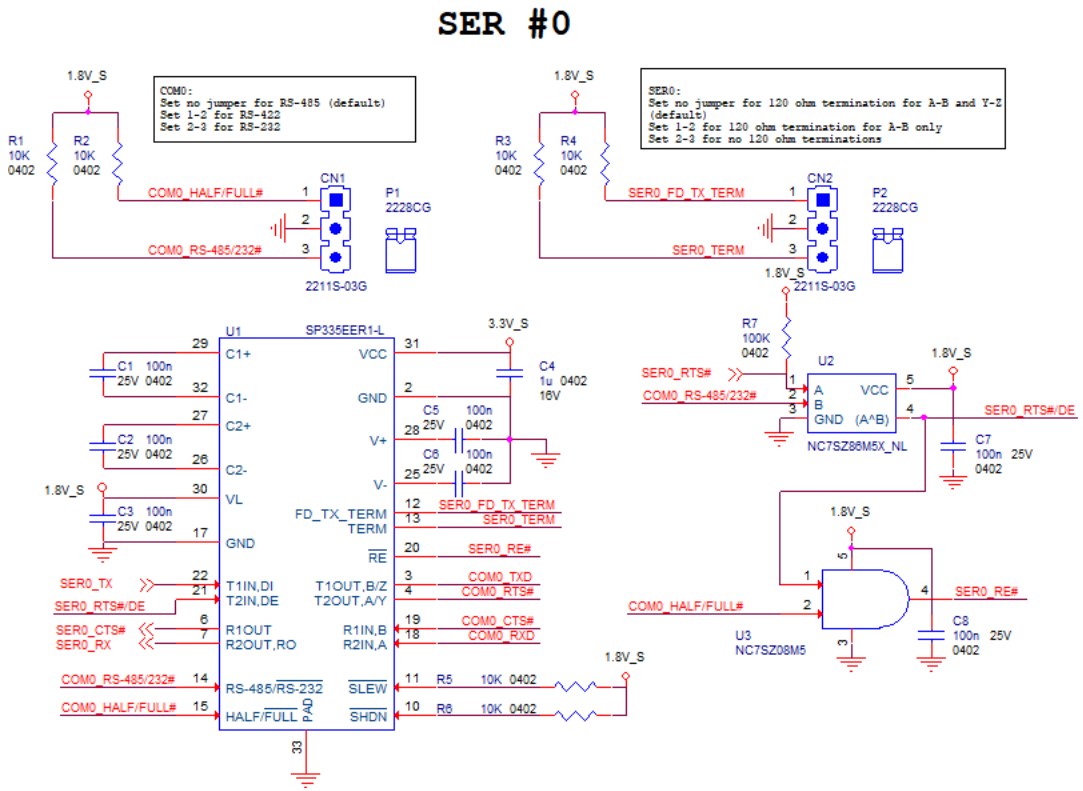
SER2_CTS#: UART #1 Interface, Handshake signal, Clear to Send (Input) line, 1.8V_ RUN electrical level.

SER3_RX: HS-UART #1 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level. It is directly managed by Intel processor.

SER3_TX: HS-UART #1 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level. It is directly managed by Intel processor.

Please consider that interface is at +1.8V_ RUN electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_ RUN level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

In the following schematic here is an example of UART interface on the carrier board, with a multiprotocol transceiver allowing to support RS485/RS-422/RS-232 serial interfaces.



3.2.1.11 USB interface signals

The Intel® family of SOCs formerly coded as Elkhart Lake offers an xHCI USB controller, which is able to manage up to 4 Superspeed ports (i.e. USB 3.1 compliant) and up to 10 ports in USB 2.0 mode only, one of them also capable of OTG.

In SM-C93, there are up to 6 ports in USB2.0 only and up to 2 Super Speed (SS) ports (i.e. USB 3.1 compliant).

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB0+/ USB0-: Universal Serial Bus 2.0 Port #0 differential pair (directly managed by Intel processor)

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for over current operation information.

USB1+/ USB1-: Universal Serial Bus Port 2.0 #1 differential pair.

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port 2.0 #2 differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB3+/USB3-: Universal Serial Bus Port 2.0 #3 differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB4+/USB4-: Universal Serial Bus Port 2.0 #4 differential pair.

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB5+/USB5-: Universal Serial Bus Port 2.0 #3 differential pair.

USB5_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

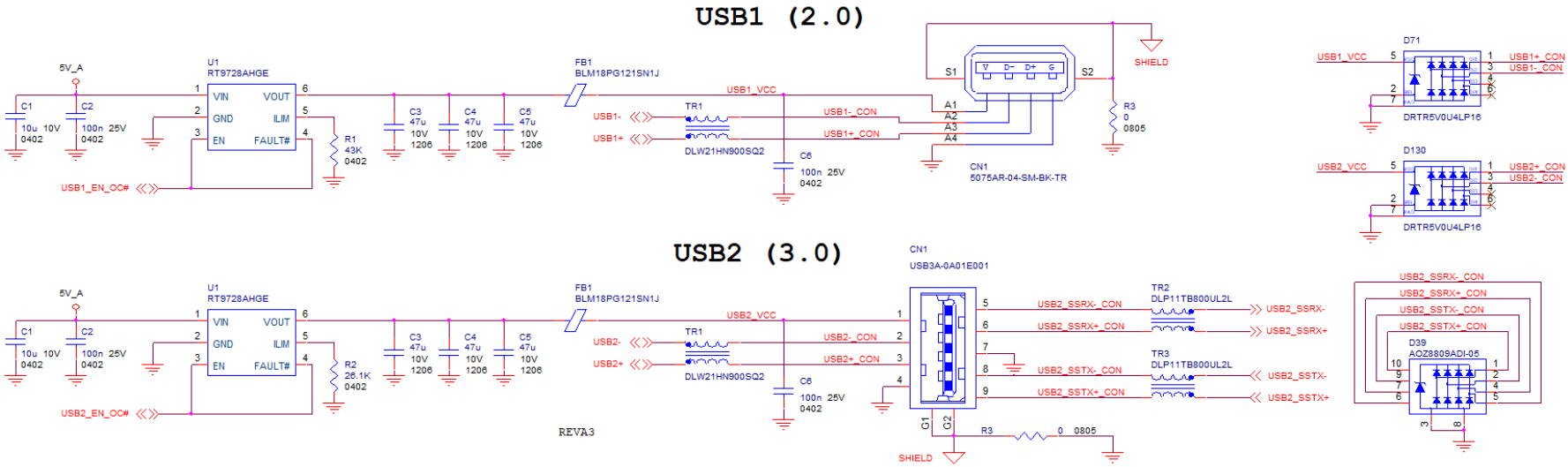
USB2_SSTX+/ USB2_SSTX-: USB 3.0 Port #1 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB 3.0 Port #1 Superspeed Receive differential pair.

USB3_SSTX+/ USB3_SSTX-: USB 3.0 Port #2 Superspeed Transmit differential pair.

USB3_SSRX+/ USB3_SSRX-: USB 3.0 Port #2 Superspeed Receive differential pair.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed. Switch with settable current limit on power lines are recommended.



3.2.1.12 PCI Express interface signals

The SM-C93 module can offer externally up to four PCI Express lane, which are directly managed by the Intel® family of SOCs formerly coded as Elkhart Lake.

PCI express Gen 3.0 (8GT/s) is supported.

Here following the signals involved in PCI express management

PCIE_A_RX+/ PCIE_A_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE_A_REFCK+/ PCIE_A_REFCK-: PCI Express Reference Clock for lane #0, Differential Pair

PCIE_A_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level with a 100kΩ pull-down resistor. It can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is recommended to provide for a buffer on the carrier board.

PCIE_A_CKREQ#: PCI Express Port A clock request signal, used from a PCI-e device to request the need for PCI Express Reference Clock. Bidirectional signal, +3.3V_RUN electrical level with a 10k pull-up resistor.

PCIE_B_RX+/ PCIE_B_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE_B_TX+/PCIE_B_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE_B_REFCK+/ PCIE_B_REFCK-: PCI Express Reference Clock for lane #1, Differential Pair

PCIE_B_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level with a 100kΩ pull-down resistor. It can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is recommended to provide for a buffer on the carrier board. This signal is shared

PCIE_B_CKREQ#: PCI Express Port B clock request signal, used from a PCI-e device to request the need for PCI Express Reference Clock. Bidirectional signal, +3.3V_RUN electrical level with a 10k pull-up resistor.

PCIE_C_RX+/ PCIE_C_RX-: PCI Express lane #2, Receiving Input Differential pair

PCIE_C_TX+/PCIE_C_TX-: PCI Express lane #2, Transmitting Output Differential pair

PCIE_C_REFCK+/ PCIE_C_REFCK-: PCI Express Reference Clock for lane #2, Differential Pair

PCIE_C_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level with a 100kΩ pull-down resistor. It can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is recommended to provide for a buffer on the carrier board.

PCIE_D_RX+/ PCIE_D_RX-: PCI Express lane #3, Receiving Input Differential pair

PCIE_D_TX+/PCIE_D_TX-: PCI Express lane #3, Transmitting Output Differential pair

PCIE_WAKE#: PCIe wake up interrupt to host input signal. Active low, +3.3V_ALW electrical level with a 10k pull-up resistor.

In the following table are shown the possible groupings allowed of the PCI-e lanes:

Allowed groupings	Lane #0	Lane #1	Lane #2	Lane #3
1 PCI-e x 4 port	√			
2 PCI- e x2	√		√	
1 PCI-e x 2 + 2 PCI-e x1	√		√	√
4 PCI-e x1	√	√	√	√

Please also be aware that this grouping cannot be changed dynamically, it is a fixed feature of the BIOS.

The customer in phase of order must select what grouping to have for PCI-e lanes.

3.2.1.13 SERDES interface signal

The SM-C93 module can offer one optional SERDES interface, alternative to fourth PCI-e lane. The most common use for this interface is the implementation of an additional LAN port on carrier board with SGMII interface.

Here following the signals involved in SERDES management:

SERDES_0_TX+/ SERDES_0_TX-: Differential SERDES 0 Transmit Data Pair

SERDES_0_RX+/ SERDES_0_RX-: Differential SERDES 0 Receive Data Pair

MDIO_CLK: MDIO Signals to Configure Possible PHYs. +1.8V_ RUN electrical level with 2k2Ω pull-up resistor.

MDIO_DAT: MDIO Signals to Configure Possible PHYs. +1.8V_ RUN electrical level with 2k2Ω pull-up resistor.

3.2.1.14 Gigabit Ethernet signals

Gigabit Ethernet interfaces are realized on SM-C93 module by using two TI Gigabit Ethernet PHY transceivers, which are interfaced to Intel processor through RGMII interface.

Here following the signals involved in Gigabit Ethernet #0 management:

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_SDP: Software defined pin, directly managed by TI Gigabit Ethernet PHY transceiver #0. Bidirectional signal, +3.3V_ALW electrical level.

Here following the signals involved in Gigabit Ethernet #1 management:

GBE1_MDI0+/GBE1_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE1_MDI1+/GBE1_MDI1-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_MDI2+/GBE1_MDI2-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_MDI3+/GBE1_MDI3-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

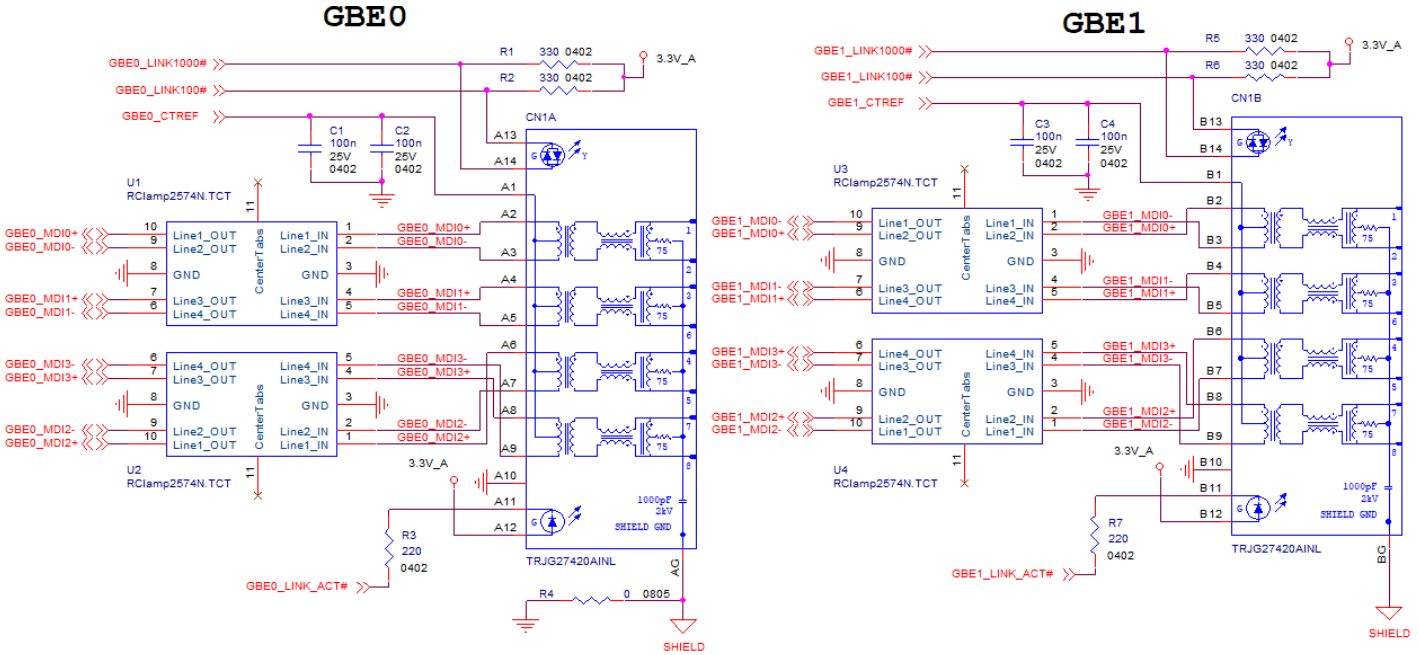
GBE1_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_SDP: Software defined pin, directly managed by Intel® Ethernet Controller I210 for Gigabit Ethernet #1

Please refer to the following schematics as an example of connection of Ethernet interface on the carrier board, with TVS diodes specifically designed to protect

sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. TI Gigabit Ethernet PHY transceiver, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on SMARC connector.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary, for both Gigabit Ethernet interfaces



3.2.1.15 CAN interface signals

Two CAN interfaces, directly managed by the Elkhart Lake processor, are available on SMARC card edge connector.

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal.

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal.

CAN1_TX: CAN Transmit Output for CAN Bus Channel 1. +1.8V_RUN electrical voltage level signal.

CAN1_RX: CAN Receive Input for CAN Bus Channel 1. +1.8V_RUN electrical voltage level signal.

Please consider that it is not possible to connect the SMARC CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.1.16 Watchdog

WDT_TIME_OUT#: Watchdog timer Output. +1.8V_DSW electrical level

3.2.1.17 GPIO signals

The Embedded controller MEC1705 GPIO interface provides general purpose input monitoring and output control, as well as many other features for the GPIO described on datasheet.

The signals involved in GPIO management are:

GPIO0: General Purpose I/O #0, +1.8V_DSW electrical level

GPIO1: General Purpose I/O #1, +1.8V_DSW electrical level

GPIO2: General Purpose I/O #2, +1.8V_DSW electrical level

GPIO3: General Purpose I/O #3, +1.8V_DSW electrical level

GPIO4: General Purpose I/O #4, +1.8V_DSW electrical level

GPIO5: General Purpose I/O #5, +1.8V_DSW electrical level

GPIO6: General Purpose I/O #6, +1.8V_DSW electrical level

GPIO7: General Purpose I/O #7, +1.8V_DSW electrical level

GPIO8: General Purpose I/O #8, +1.8V_DSW electrical level

GPIO9: General Purpose I/O #9, +1.8V_DSW electrical level

GPIO10: General Purpose I/O #10, +1.8V_DSW electrical level

GPIO11: General Purpose I/O #11, +1.8V_DSW electrical level

GPIO12: General Purpose I/O #12, +1.8V_DSW electrical level

GPIO13: General Purpose I/O #13, +1.8V_DSW electrical level

3.2.1.18 FuSa signals

As a factory alternative to GPIO signals, SM-C93 does provide functional safety functions through following signals:

OKNOK0: Output antivalent signal for error indication to the system. Intel® Safety Island has an error collection hub that receives errors from processor, classifies them into severity levels and reports them as an output state to the system through this signal. +1.8V_ALW electrical level. Combined with OKNOK1, the system will switch to safe state for any of following OKNOK0 / OKNOK1 states (“0” / “0” power off, “0” / “1” error state, “1” / “1” reset state), while is in normal operating state “OK” with “1” / “1” (no fault). “0” stands for low level (GND), while “1” stands for high level (+1.8V_ALW).

OKNOK1: Output antivalent signal for error indication to the system. Intel® Safety Island has an error collection hub that receives errors from processor, classifies them into severity levels and reports them as an output state to the system through this signal. +1.8V_ALW electrical level. Combined with OKNOK1, the system will switch to safe state for any of following OKNOK0 / OKNOK1 states (“0” / “0” power off, “0” / “1” error state, “1” / “1” reset state), while is in normal operating state “OK” with “1” / “1” (no fault). “0” stands for low level (GND), while “1” stands for high level (+1.8V_ALW).

ALERT#: Output signal indicating that a correctable error occurred. Active low signal, +3.3V_ALW electrical level with 4k7Ω pull up resistor

SPIS_CS#: SPI Slave chip select active low input, +1.8V_ALW electrical level

SPIS_SCLK: SPI Slave clock input, +1.8V_ALW electrical level

SPIS_MISO: SPI Slave Master In Slave Out, bi-directional data. +1.8V_ALW electrical level

SPIS_MOSI: SPI Slave Master Out Slave In, bi-directional data. +1.8V_ALW electrical level

CHXPMIC_EN: PMIC Enable override active high output signal, +1.8V_ALW electrical level

CHX_RLYSWITCH: Platform level relay switch override active high output signal, +1.8V_ALW electrical level

CHXOKNOX0: Output OK signal of other EHL channel, +1.8V_ALW electrical level

CHXOKNOK1: Output NOK signal of other EHL channel, +1.8V_ALW electrical level

SPIM_CS#: SPI Master chip select active low output, +1.8V_ALW electrical level

SPIM_SCLK: SPI Master clock output, +1.8V_ALW electrical level

SPIM_MISO: SPI Master Master In Slave Out, bi-directional data. +1.8V_ALW electrical level

In addition, SM-C93 does provide additional functional safety functions through following signals:

SPIM_MOSI: SPI Master Master Out Slave In, bi-directional data. +1.8V_ALW electrical level

THERMTRIP: Thermal Trip Output Signal, asserted by the processor to indicate a thermal trip event which may cause severe damage. Active high signal, +3.3V_ RUN electrical level with 10kΩ pull-up resistor

PROCHOT: Protection Output signal, asserted when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. Active high signal, +3.3V_ RUN electrical level with 10kΩ pull-up resistor

FUSA_PWRFAIL#: FuSa Power Fail indication output signal. Active low signal, +3.3V_ RUN electrical level with 10kΩ pull-up resistor

CHXPMICEN: FuSa power input disabling signal, once asserted will disable 5V_DSW input signal. Active high signal, with 100kΩ pull-down resistor

3.2.1.19 Management pins

A set of signals are used by SM-C93 to communicate with carrier board for power management and indication status. Please refer to SMARC hardware specifications ver. 2.1 for more detailed informations.

The signals involved are:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board, active low signal from a voltage detection circuit

CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output is set to +1.8V_ALW electrical level with a 10k pull-down resistor

CARRIER_STBY#: Stand By command to the Carrier Board. Output, active low signal, is set to +1.8V_ALW electrical level with a 10k pull-down resistor

RESET_OUT#: General Purpose Reset. Output, active low signal, +1.8V_ALW electrical level with a 10k pull-down resistor

RESET_IN#: General Purpose Reset. Input, active low signal, +1.8_ALW electrical level with a 10k pull-up resistor

POWER_BTN#: Power Button. Input, active low signal, +1.8_DSW electrical level with a 10k pull-up resistor

SLEEP#: Sleep indicator from Carrier board. Input, active low signal, +1.8_ALW electrical level with a 10k pull-up resistor

LID#: LID Switch. Input, active low signal, +1.8_ALW electrical level with a 10k pull-up resistor

BATLOW#: Battery Low indication signal from the Carrier Board. Input, active low signal, +1.8V_DSW electrical level with a 10k pull-up resistor

CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, active low signal, +1.8V_DSW electrical level with a 2k2 pull-up resistor

CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, active low signal, +1.8V_DSW electrical level with a 2k2 pull-up resistor

TEST#: Signals used to invoke from Carrier Board specific test function(s). Input, active low signal, +1.8V_DSW electrical level with a 10k pull-up resistor. At the moment, this function is not implemented and reserved for its use in the future.

SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, active low signal, +1.8V_DSW electrical level with a 2k2 pull-up resistor

3.2.1.20 Boot Select

The following signals are active low and driven by open/ground circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_ALW electrical level with a 10k pull-up resistor

BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_ALW electrical level with a 10k pull-up resistor

BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_ALW electrical level with a 10k pull-up resistor

FORCE_RECOV#: Force recovery Mode. Input, +1.8_ALW electrical level with a 10k pull-up resistor

Chapter 4.
Appendices

- Thermal Design

4.1 Thermal Design

Highly integrated modules like SM-C93 offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SM-C93 indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SM-C93 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
RC93-DISS-1-SKUS1-4-PK	SMARC HEAT SPREADER: SM-C93 Heat Spreader (PASSIVE), SKUS1-4 - Packaged
RC93-DISS-1-SKUS5-12-PK	SMARC HEAT SPREADER: SM-C93 Heat Spreader (PASSIVE), SKUS5-12 - Packaged
RC93-DISS-2-SKUS1-4-PK	SMARC HEAT SINK: SM-C93 Heat Sink (PASSIVE), SKUS1-4 – Packaged
RC93-DISS-2-SKUS5-12-PK	SMARC HEAT SINK: SM-C93 Heat Sink (PASSIVE), SKUS5-12 – Packaged

Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

SECO S.p.A. - Via A. Grandi, 20
52100 Arezzo - ITALY
Ph: +39 0575 26979 - Fax: +39 0575 350210
www.seco.com