1. CIRCUIT DESCRIPTION

1.1. GENERAL

A. BASE UNIT
   1). RECEIVER
   2). DIGITAL SIGNAL
   3). VOICE SIGNAL
   4). TRANSMITTER
   5). RINGER DETECTOR
   6). POWER SUPPLY CIRCUIT

B. REMOTE UNIT
   1). RECEIVER
   2). DIGITAL SIGNAL
   3). VOICE SIGNAL
   4). TRANSMITTER
   5). DIALING SIGNAL
   6). BATTERY SAVING OPERATION .

1.2. SYSTEM OPERATION

   1). INCOMING CALL
   2). OUTGOING CALL
   3). DIALING
   4). DIGITAL SECURITY CODING

REFERENCE TO THE BLOCK DIAGRAM WILL BE OF CONSIDERABLE HELP IN UNDERSTANDING THE OPERATION OF THE FF915 CIRCUITRY. PLEASE REFER TO THE SCHEMATIC DIAGRAM FOR SPECIFIC COMPONENT DETAILS.

1.1 GENERAL

A. BASE UNIT

1). RECEIVER

THE RF SIGNAL FROM THE ANTENNA IS FED THROUGH THE ANTENNA DUPLEXER DUP.1 TO THE RF AMPLIFIER Q1.

THE AMPLIFIED RF SIGNAL IS THEN HETERODYNED BY 1st MIXER Q2 WITH THE 1st LOCAL SIGNAL SUPPLIED FROM PLL (PHASE-LOCKED-LOOP) FREQUENCY SYNTHESIZER CONSISTING OF RX VCO AND PLL IC IC2, PRODUCING A FIRST IF SIGNAL (~~10.6875MHz~~ 10.900171MHz).

THE 1st IF SIGNAL IS THEN AMPLIFIED BY Q2 THROUGH CERAMIC FILTER ~~CF1~~ CF2 AND ~~CF2~~ CF3 WHICH SUPPRESSES THE 2nd IF IMAGE SIGNAL, AND FED TO 2nd MIXER WITHIN IC1, WHERE THE 1st IF SIGNAL HETERODYNED WITH 2nd LOCAL SIGNAL SUPPLIED FROM CPU CLOCK OSCILLATOR (8.0MHz), PRODUCING A ~~2.6875KHz~~ 2.7MHz 2nd IF.

THE 2nd IF SIGNAL IS FED TO THE IF LIMITTER AMPLIFIER WITHIN IC1. THE AMPLIFIED 2nd IF SIGNAL IS THEN DELIVERED TO THE DISCRIMINATOR WITHIN IC1 WHICH PRODUCES AN AUDIO OUTPUT IN RESPONSE TO A CORRESPONDING CHANGE IN THE FREQUENCY OF THE 2nd IF SIGNAL.

THE DISCRIMINATOR OUTPUT SIGNAL CONSISTS OF DIGITAL AND VOICE SIGNALS.

2). DIGITAL SIGNAL

THE DIGITAL SIGNAL WITH "TALK-ON", "TALK-OFF", DIAL DIGIT, FLASH, CHANNEL- CHANGE, AND SECURITY CODE IS SHAPED WAVEFORM BY DATA SHAPER WITHIN IC1, AND THEN FED TO THE CPU IC101. THE CPU DECODES THE DIGITAL SIGNAL TO REFORM REQUIRED OPERATION.

3). VOICE SIGNAL

THE VOICE SIGNAL IS FED TO THE EXPANDER WITHIN IC1 TO BE RETURNED ITS ORIGINAL DYNAMIC RANGE. THE VOICE SIGNAL IS THEN DELIVERED TO THE TELEPHONE LINE THROUGH THE AMPLIFIER WITHIN ~~Q102,~~ IC103-A HYBRID CIRCUIT ~~Q104,~~ Q104 AND THE ISOLATION TRANSFORMER T101.

4). TRANSMITTER

THE VOICE SIGNAL FROM THE TELEPHONE LINE THROUGH THE HYBRID CIRCUIT Q104 IS AMPLIFIED BY IC103-8 AND Q103, AND FED TO THE COMPRESSOR WITHIN IC1 TO COMPRESS ITS DYNAMIC RANGE. THE COMPRESSED VOICE SIGNAL IS APPLIED TO THE VARACTOR D2 FOR FREQUENCY MODULATION. A 903MHz CARRIER IS PRODUCED BY PLL CIRCUIT CONSISTING OF VCO AND PLL IC IC2. THE MODULATED CARRIER IS AMPLIFIED BY Q4 AND TRANSMITTED INTO THE ANTENNA THROUGH THE DUPLEXER DUP1.

5). RINGER DETECTOR

THE INCOMING RING SIGNAL IS DETECTED BY THE PHOTO COUPLER PC101 WHICH OUTPUT IS CONNECTED PIN 39 ~~10~~ OF CPU AND CHECKED ITS FREQUENCY BY CPU. THE "RING" CODE IS THEN GENERATED AND DELIVERED TO THE VARACTOR D2 FOR MODULATION.

6). POWER SUPPLY CIRCUIT

THE POWER SUPPLY CIRCUIT IS COMPOSED OF RIPPLE REJECTION CIRCUIT Q108 5V REGULATOR CIRCUIT IC102 AND REMOTE BATTERY CHARGE REGULATOR CIRCUIT Q109 & D107.

B. REMOTE UNIT

1). RECEIVER

THE RF SIGNAL FROM THE ANTENNA IS FED THROUGH THE ANTENNA DUPLEXER DUP401 TO THE RF AMPLIFIER Q401.

THE AMPLIFIED RF SIGNAL IS THEN HETERODYNED BY 1st MIXER Q403 WITH THE 1st LOCAL SIGNAL SUPPLIED FROM PLL FREQUENCY SYNTHESIZER CONSISTING OF RX VCO AND PLL IC IC402, PRODUCING A FIRST IF SIGNAL (~~10.6875~~10.7MHz).

THE 1st IF SIGNAL IS THEN AMPLIFIED BY Q405 THROUGH CERAMIC FILTER CF402 AND CF403 WHICH SUPPRESSES THE 2nd IF IMAGE SIGNAL, AND FED TO 2nd MIXER WITHIN IC401, WHERE THE 1st IF SIGNAL IS HETERODYNED WITH 2nd LOCAL SIGNAL (12.375MHz) SUPPLIED FROM THE TRIPLED CPU CLOCK OSCILLATOR (4.125MHz), PRODUCING A ~~1.6875~~1.675MHz 2nd IF.

THE 2nd IF SIGNAL IS FED TO THE IF LIMITTER AMPLIFIER WITHIN IC401.

THE AMPLIFIED 2nd IF SIGNAL THEN DELIVERED TO THE DISCRIMINATOR WITHIN IC401 AND PRODUCES AS AUDIO OUTPUT IN RESPONSE TO A CORRESPONDING CHANGE IN THE FREQUENCY OF THE 2nd IF SIGNAL.

THE DISCRIMINATOR OUTPUT SIGNAL CONSISTS OF DIGITAL AND VOICE SIGNALS.

2). DIGITAL SIGNAL

THE DIGITAL SIGNAL WITH INCOMING CALL, PAGING CALL, OR A SECURITY CODE IS SHAPED WAVEFORM BY DATA SHAPER WITHIN IC401 AND THEN FED TO THE CPU IC501.
THE CPU DECODES THE DIGITAL SIGNAL AND DRIVES THE BUZZER.

3). VOICE SIGNAL

THE VOICE SIGNAL IS FED TO THE EXPANDER WITHIN IC401 TO BE RETURNED ITS ORIGINAL DYNAMIC RANGE. THE VOICE SIGNAL IS THEN DELIVERED TO THE SPEAKER THROUGH THE DRIVE CIRCUIT Q407.

4). TRANSMITTER

THE VOICE SIGNAL ENTERED FROM THE MICROPHONE IS AMPLIFIED BY Q406 AND FED TO THE COMPRESSOR WITHIN IC401 TO BE COMPRESSED ITS DYNAMIC RANGE. THE COMPRESSED VOICE SIGNAL IS APPLIED TO THE VARACTOR D402 FOR FREQUENCY MODULATION. THE 926MHz CARRIER IS PRODUCED BY PLL CIRCUIT CONSISTING OF TX VCO AND PLL IC IC402. THE MODULATED CARRIER IS AMPLIFIED BY Q402 AND TRANSMITTED INTO THE ANTENNA THROUGH THE DUPLEXER DUP401.

5). DIALING SIGNAL

WHEN THE "TALK" KEY IS PRESSED, THE TRANSMITTER CIRCUIT IS ACTIVATED. THEN THE "TALK-ON" DIGITAL DATA WITH ID CODE IS DELIVERED TO THE VARACTOR D402 FOR MODULATION. AFTER THAT THE DIGIT KEY DATA IS SENT TO THE BASE UNIT.

6). BATTERY SAVING OPERATION

THE RECEIVER CIRCUIT UNDER STAND BY MODE WORKS PERIODICALLY TO EXTEND BATTERY LIFE. CPU CONTROLS THE PERIODICAL DC POWER TO THE RECEIVER.

1.2. SYSTEM OPERATION

1). INCOMING CALL

WHEN INCOMING RING SIGNAL IS DETECTED BY RINGER DETECTOR, THE TRANSMITTER IS ACTIVATED, AND "RING" CODE IS SENT TO THE REMOTE UNIT ALONG WITH ID CODE FROM PIN 2 OF BASE CPU UNTIL THE RING SIGNAL STOPS.

WHEN "RING" CODE IS DEMODULATED IN THE REMOTE UNIT, THE REMOTE CPU WILL DECODE IT AND GENERATE RING TONE TO THE BUZZER THROUGH THE DRIVE CIRCUIT Q506.

2). OUTGOING CALL

WHEN "TALK" KEY ON THE REMOTE UNIT IS PRESSED, PIN 20 OF REMOTE CPU GOES "LOW", CAUSING TX B+ SWITCH Q409 TO TURN ON.
THEN THE TRANSMITTER IS ACTIVATED AND "TALK-ON" CODE IS SENT TO THE BASE UNIT ALONG WITH ID CODE GENERATED FROM PIN 19 OF CPU.

WHEN THE BASE CPU DECODES "TALK-ON" CODE AND THE REMOTE ID CODE COINCIDE WITH THE BASE ID CODE, PIN 33 OF THE BASE CPU GOES "HIGH". AND THEN THE TEL. LINE LOOP RELAY RLY101 IS ACTIVATED.

3). DIALING

THE DIAL SIGNAL IS SENT TO THE BASE UNIT ACCORDING TO THE PRESSED KEY.

UPON RECEIPT OF DIAL SIGNAL, THE BASE UNIT GENERATES ~~EITHER PULSE DIAL SIGNAL OR~~ DTMF TONE SIGNAL ~~ACCORDING TO THE TEL. LINE MODE SELECT SWITCH SW101 POSITION.~~

~~UPON RECEIPT OF "*" SIGNAL AT PULSE MODE, THE BASE UNIT CHANGES DIAL MODE TO TONE MODE UNTIL THE LINE IS TERMINATED.~~

UPON RECEIPT OF "FLASH" SIGNAL, THE BASE UNIT OPENS THE TEL. LINE LOOP FOR A MOMENT.

UPON RECEIPT OF "REDIAL" SIGNAL, THE BASE UNIT OUTPUTS THE SAME DIAL DIGIT AS THE LAST DIAL, WHICH STORED IN BASE CPU MEMORY.

UPON RECEIPT OF "MEMORY" + "LOCATION NO." SIGNAL, THE BASE UNIT RECALL THE DIAL DIGITS WHICH STORED IN THE BASE CPU MEMORY AND OUTPUTS THEM TO THE TEL. LINE.

4). DIGITAL SECURITY CODING

THE 16-BIT ID CODE IS USED IN THIS SYSTEM TO SECURE THE RF LINK. BASE UNIT PROGRAMS THIS ID CODE RANDOMLY. WHENEVER THE REMOTE UNIT IS PLACED IN THE BASE CRADLE, ID CODE EXCHANGE IS DONE BETWEEN THE BOTH UNITS, AND THEN THE SAME ID CODE IS RETAINED IN THE BOTH UNITS' RAM.

DEFAULT ID CODE IS SET IN THE REMOTE RAM WHEN THE REMOTE UNIT IS POWERED-UP FROM BELOW THE DATA RETENTION VOLTAGE, APX. 2V. UNDER THIS CONDITION, THE BOTH UNITS DO NOT LINK.

RANDOM ID CODE IS GENERATED IN THE BASE UNIT WHEN THE BASE UNIT IS POWERED-UP WITH DEFAULT ID CODE OR WHEN THE REMOTE UNIT IS PLACED IN THE BASE CRADLE.

TABLE 1 CHANNEL FREQUENCY PLAN (Revised)

[MHz]

	BASE				REMOTE			
CH	TX Freq.	TX VCO	RX Freq.	RX VCO	TX Freq.	TX VCO	RX Freq.	RX VCO
1	902.2375	902.2375	925.3125	914.6123	925.3125	925.3125	902.2375	912.9375
2	902.3000	902.3000	925.3750	914.6748	925.3750	925.3750	902.3000	913.0000
3	902.3625	902.3625	925.4375	914.7373	925.4375	925.4375	902.3625	913.0625
4	902.4250	902.4250	925.5000	914.7998	925.5000	925.5000	902.4250	913.1250
5	902.4875	902.4875	925.5625	914.8623	925.5625	925.5625	902.4875	913.1875
6	902.5500	902.5500	925.6250	914.9248	925.6250	925.6250	902.5500	913.2500
7	902.6125	902.6125	925.6875	914.9873	925.6875	925.6875	902.6125	913.3125
8	902.6750	902.6750	925.7500	915.0498	925.7500	925.7500	902.6750	913.3750
9	902.7375	902.7375	925.8125	915.1123	925.8125	925.8125	902.7375	913.4375
10	902.8000	902.8000	925.8750	915.1748	925.8750	925.8750	902.8000	913.5000
11	902.8625	902.8625	925.9375	915.2373	925.9375	925.9375	902.8625	913.5625
12	902.9250	902.9250	926.0000	915.2998	926.0000	926.0000	902.9250	913.6250
13	902.9875	902.9875	926.0625	915.3623	926.0625	926.0625	902.9875	913.6875
14	903.0500	903.0500	926.1250	915.4248	926.1250	926.1250	903.0500	913.7500
15	903.1125	903.1125	926.1875	915.4873	926.1875	926.1875	903.1125	913.8125
16	903.1750	903.1750	926.2500	915.5498	926.2500	926.2500	903.1750	913.8750
17	903.2375	903.2375	926.3125	915.6123	926.3125	926.3125	903.2375	913.9375
18	903.3000	903.3000	926.3750	915.6748	926.3750	926.3750	903.3000	914.0000
19	903.3625	903.3625	926.4375	915.7373	926.4375	926.4375	903.3625	914.0625
20	903.4250	903.4250	926.5000	915.7998	926.5000	926.5000	903.4250	914.1250
21	903.4875	903.4875	926.5625	915.8623	926.5625	926.5625	903.4875	914.1875
22	903.5500	903.5500	926.6250	915.9248	926.6250	926.6250	903.5500	914.2500
23	903.6125	903.6125	926.6875	915.9873	926.6875	926.6875	903.6125	914.3125
24	903.6750	903.6750	926.7500	916.0498	926.7500	926.7500	903.6750	914.3750
25	903.7375	903.7375	926.8125	916.1123	926.8125	926.8125	903.7375	914.4375
26	903.8000	903.8000	926.8750	916.1748	926.8750	926.8750	903.8000	914.5000
27	903.8625	903.8625	926.9375	916.2373	926.9375	926.9375	903.8625	914.5625
28	903.9250	903.9250	927.0000	916.2998	927.0000	927.0000	903.9250	914.6250
29	903.9875	903.9875	927.0625	916.3623	927.0625	927.0625	903.9875	914.6875
30	904.0500	904.0500	927.1250	916.4248	927.1250	927.1250	904.0500	914.7500
31	904.1125	904.1125	927.1875	916.4873	927.1875	927.1875	904.1125	914.8125
32	904.1750	904.1750	927.2500	916.5498	927.2500	927.2500	904.1750	914.8750
33	904.2375	904.2375	927.3125	916.6123	927.3125	927.3125	904.2375	914.9375
34	904.3000	904.3000	927.3750	916.6748	927.3750	927.3750	904.3000	915.0000
35	904.3625	904.3625	927.4375	916.7373	927.4375	927.4375	904.3625	915.0625
36	904.4250	904.4250	927.5000	916.7998	927.5000	927.5000	904.4250	915.1250
37	904.4875	904.4875	927.5625	916.8623	927.5625	927.5625	904.4875	915.1875
38	904.5500	904.5500	927.6250	916.9248	927.6250	927.6250	904.5500	915.2500
39	904.6125	904.6125	927.6875	916.9873	927.6875	927.6875	904.6125	915.3125
40	904.6750	904.6750	927.7500	917.0498	927.7500	927.7500	904.6750	915.3750
CPU CLK	7.99989				4.125			
2ND LO.	7.99989				12.375			
1ST IF	10.700171				10.7			
2ND IF	2.700282				1.675			