intel®

AP-579

APPLICATION NOTE

Pentium® Processor Flexible Motherboard Design Guidelines

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FIGURES

TABLES

1.0. INTRODUCTION

This document provides guidelines for designing a Pentium® processor family flexible motherboard. The Pentium processor family flexible motherboard, as shown in Figure 1, is a single motherboard design that can support the various members of the Pentium processor family including Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium processors with MMX™ technology, Pentium OverDrive® processors, and future Pentium OverDrive processors with MMX technology.

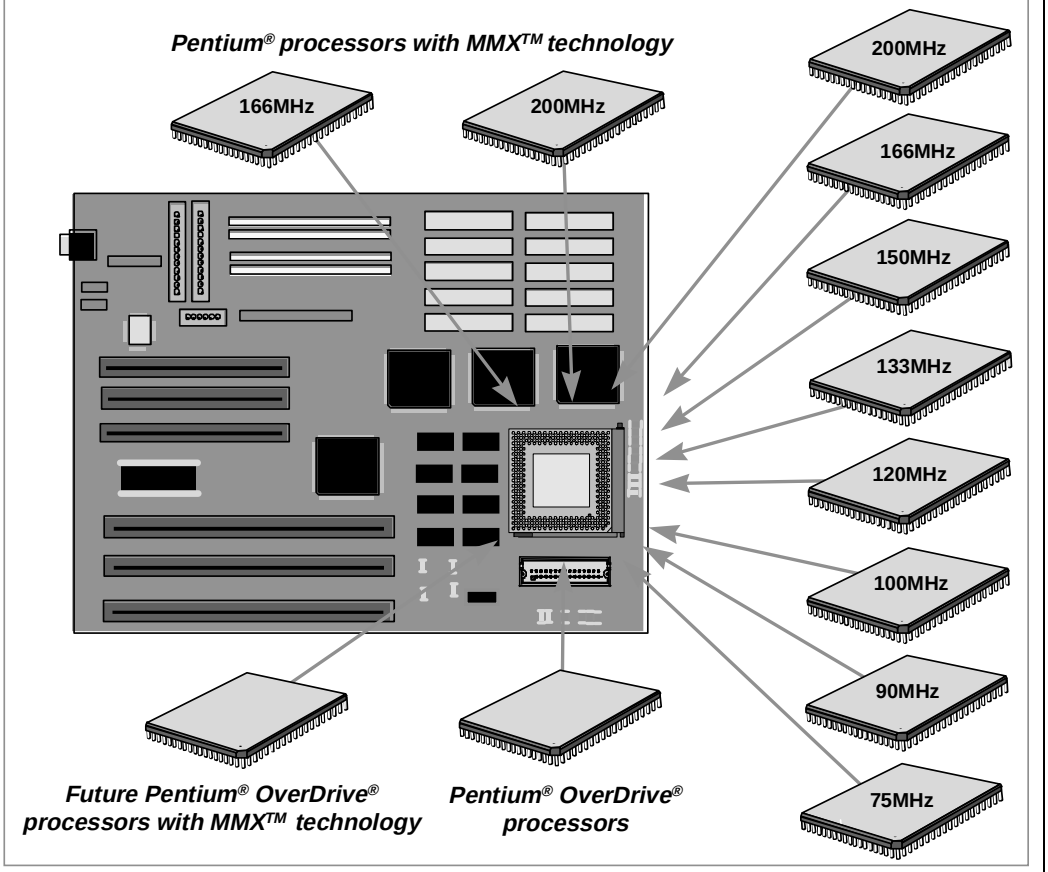


Figure 1. Pentium® Processor Flexible Motherboard

The Pentium processor family flexible motherboard should support the following features:

- Split Power Islands: The Pentium processor family flexible motherboard should accommodate split (separate) power islands to accept processors that have split core and I/O voltage planes. The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium OverDrive processor have a unified core and I/O power plane internal to the processor package. The Pentium processor with MMX technology and the future Pentium OverDrive processor with MMX technology have split power planes internal to the processor package. The two internal power planes of the Pentium processor with MMX technology receive two different voltages (i.e., 2.8V for the Core and 3.3V for the I/O).
- 3.3V Power Source: Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors and future Pentium OverDrive processor with MMX technology receive 3.3V (3.135 – 3.6V) from the processor socket for operation. The Pentium processor family flexible motherboard should provide 3.3V by using a system power supply unit or a voltage regulator.
- 2.8V Power Source: The Pentium processor with MMX technology receives 2.8V (±100 mV) for its core. The Pentium processor family flexible motherboard should provide support for a 2.8V power source through either an on-board 2.8V voltage regulator or a Voltage Regulator Module (see Appendix A).
- Socket 7: The Pentium processor family flexible motherboard should implement a Socket 7. Pin assignments vary according to processors, and Socket 7 is a processor socket designed to accept all processors in the Pentium processor family (i.e., Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium processors with MMX technology) regardless of their differences in pin assignments or power plane implementation. Socket 7 is a 321-pin ZIF socket and is a superset of the older 320-pin Socket 5. Socket 7 provides the option and capability to support both unified-plane processors and split-plane, dual-voltage supply processors and requires that CLK and PICCLK be driven at 3.3V levels. Socket 7 electrical specifications list the maximum current for the future Pentium processors with MMX technology upgradability as 5.0A at 3.3V; however, the Pentium processor with MMX technology has a core current draw of 5.7A at 2.8V.

  NOTE

  The current draw is processor dependent and any processor belonging to the Pentium processor family may be utilized in a Socket 7 provided the system design provides adequate current.

- Local Decoupling: Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology may cause rapid fluctuation of current during transitions between “low-power” states and “active” states. The Pentium processor family flexible motherboard provides accurate and adequate decoupling capacitors near the processor socket to prevent violation of the voltage supply range specification.
- Multiple Bus Frequencies: Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, and future Pentium OverDrive processors with MMX technology support external bus frequencies of 50 MHz, 60 MHz and 66 MHz. The Pentium processor with MMX technology supports external bus frequencies of 60 MHz and 66 MHz. The Pentium processor family flexible motherboard is implemented with system logic compatible with the AC timing parameters at these bus frequencies.
- Bus-to-Core Ratio: The Pentium processor family flexible motherboard should provide jumpers for bus fraction pin strapping options to allow for flexibility in configuring the external bus frequency to internal core frequency ratio. The bus-to-core ratios can be either 1/3, 2/5, 1/2 or 2/3. In order to support all Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium processors with MMX technology, selection jumpers should allow a high or low logic setting for both bus fraction pins (BF1 and BF0).

  NOTE

  Not all Pentium OverDrive processors and future Pentium OverDrive processors with MMX technology internally configure the bus fraction, and jumper changes are not

required when a Pentium OverDrive processor or a future Pentium OverDrive processor with MMX technology is installed in a Socket 7 system.

- Thermal and Mechanical Specifications: The Pentium processor family flexible motherboard should be designed to meet the thermal and mechanical specifications of the Socket 7 Specification, Rev. 3.0.
- BIOS Support: Each processor stepping is assigned a unique identification and feature signature. The execution of the CPUID instruction will retrieve these signatures for identification. The Pentium processor family flexible motherboard provides a system BIOS capable of supporting all Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium processors with MMX technology steppings. Through the use of the CPUID instruction, the BIOS can determine whether the processor supports certain features like APIC or MMX technology. (For more details, refer to application note AP-485, *Intel Processor Identification with the CPUID Instruction*. See Appendix E.)
- 3.3V Clock Drivers: Clock inputs on Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology can accept 3.3V clock drivers but not all are 5V tolerant. The Pentium processor family flexible motherboard provides a 3.3V clock driver (for CLK and PICCLK) to ensure compatibility with all Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology.

1.1. Benefits of a Flexible Motherboard

Producing a flexible motherboard design for the Pentium processor family offers several benefits:

- Offers various price/performance options: One flexible design, when populated by different members of the Pentium processor family, can provide a wide range of price/performance options. Flexibility can also be achieved through assembly time options for other components on the motherboard. For example, external caches may use asynchronous SRAM for cost effectiveness or pipelined burst SRAM for higher performance. Synchronous burst DRAM may replace extended data out (EDO) DRAM as main memory to maintain performance in cost-effective platforms with optional external cache memory.
- Reduces design and validation effort associated with multiple designs: The board does not have to be revised for every proliferation of the processor thus reducing design and validation efforts. Instead, one board is designed to accept various processors that can be populated at build-time.
- Reduces inventory and manufacturing costs: Only one motherboard design has to be manufactured and has to be maintained in inventory. This reduces the overall inventory management and manufacturing costs. For a varying product demand, the board can be populated with the appropriate processor to meet the current market demand.
- Reduces debug and technical support costs: Instead of several, only one motherboard has to be debugged. The field engineers and other support personnel need only to be trained on one base motherboard design thus reducing overall technical support efforts.

2.0. PROCESSOR DESIGN CONSIDERATIONS

This chapter describes the differences between the various processors that need to be considered when designing a Pentium processor family flexible motherboard.

2.1. Overview of the Pentium® Processor Family

Table 1 shows the members of the Pentium processor family that are supported on the flexible motherboard and highlights their respective electrical/thermal specifications. The following is a brief description of the Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology and future Pentium OverDrive processors with MMX technology processors that are supported on the flexible motherboard. Please refer to Appendix E in order to obtain specifications for each processor.

The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 is a 3.3V processor that operates at 75, 90, 100, 120, 133, 150, 166 and 200 MHz core speeds (50, 60, and 66 MHz external bus speeds). This is a unified plane processor that uses 3.3V [Standard (3.135V – 3.6V) or VRE (3.4V – 3.6V) voltage] for all V_{CC} pins.

The Pentium processor with MMX technology 166/200 is the newest addition to the Pentium processor family. Several architectural enhancements have been made: the internal data and code cache sizes have each been doubled from 8 Kbytes to 16 Kbytes, the branch prediction has been improved, and support for Intel MMX technology has been added. MMX technology is an extension to the Intel Architecture (IA) instruction set which adds 57 new opcodes and a new MMX register set. The Pentium processor with MMX technology operates at core frequencies of 166 and 200 MHz (60 and 66 MHz external bus speeds). The Pentium processor with MMX technology uses 2.8V for its internal core while its I/O operates at 3.3V (to provide full compatibility with existing chipset and SRAM). It is pin, package, and functionally compatible with the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and is operating system transparent. The Pentium processor with MMX technology's CLK and PICCLK buffers are not 5V tolerant and should only use 3.3V clock inputs.

The Pentium OverDrive processor 125/150/166 is the upgrade processor for the Pentium processor 75/90/100-based systems. It plugs into either Socket 5 or Socket 7 based designs. Pentium OverDrive processors are end-user, single-chip processor upgrade products for Pentium processor systems that speed up nearly all software applications and are binary compatible with the Pentium processor.

The future Pentium OverDrive processor with MMX technology 125/150/166/180/200 is the end-user, single chip, processor upgrade for the Pentium processor 75/90/100/120/133-based Socket 5 or Socket 7 designs. The future Pentium OverDrive processor with MMX technology 180/200 can also upgrade Pentium processor 150/166/180/200-based designs to MMX technology, but with a lower overall performance increase. The 200 MHz future Pentium OverDrive processor with MMX technology will only be supported by Socket 7-based designs.

2.2. Pinout Considerations

For the processors that are supported on the flexible motherboard, most of the signals are compatible to each other. The differences are noted below:

- V_{CC2} , V_{CC3} : On the Pentium processor with MMX technology, the internal bus logic is isolated from the core logic so that the core can run at a lower voltage (2.8V) in order to obtain faster core frequencies and reduce overall power consumption. The bus logic remains at 3.3V to remain compatible with existing chipsets and cache SRAM. The voltage for the core logic is supplied through the V_{CC2} pins and the voltage for the bus logic is supplied through the V_{CC3} pins. The motherboard design therefore splits the processor power plane into a separate 2.8V core voltage island and a 3.3V I/O voltage island.
- VCC2DET#: This is a new signal defined on the Pentium processor with MMX technology to indicate to the system that the processor installed in the processor socket uses an isolated 2.8V core supply on the V_{CC2} pins. This pin is internally connected to ground on the Pentium processor with MMX technology. On Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, and future Pentium OverDrive processors with MMX

technology, this pin is defined as INC (Internal No Connect). This signal is pulled high externally on the flexible motherboard or left as a no connect otherwise.

Table 1. Pentium® Processors and Pentium OverDrive® Processors and Their Key Differences

	Pentium® Processor	Pentium Processor with MMX™ Technology	Pentium OverDrive® Processor	Future Pentium OverDrive Processor with MMX Technology
Core Frequency	75, 90, 100, 120, 133, 150, 166, 200	166, 200	125, 150, 166	125, 150, 166, 180, 200 (7)
Bus Frequency	50, 60, 66	60, 66	50, 60, 66	50, 60, 66
Frequency Ratio	1/2, 2/3, 2/5,1/3	2/5,1/3	2/5 (4)	2/5, 1/3 (4)
Clock Level	3.3V or 5V	3.3V	3.3V or 5V	3.3V or 5V (7)
Core Supply	3.135V – 3.60V (STD); 3.40V – 3.60V (VRE)	2.7V – 2.9V	3.135 – 3.6V	
I/O Supply	3.135V – 3.60V (STD); 3.40V – 3.60V (VRE)	3.135V – 3.60V	3.135 – 3.6V	
I_{CC2} (1, 5)	Connected to I_{CC3}	5700mA (200 MHz) 4750mA (166 MHz)	Connected to I_{CC3}	Note (6)
I_{CC3} (2, 5)	4600mA (200 MHz) 2650mA (75 MHz)	650mA (200 MHz) 540mA (166 MHz)	4330mA	5000mA (200 MHz) (6) 4330mA(125–180 MHz)
I_{CC5} (3, 5)	Not Applicable	200mA	200mA	
Max. Power (5)	15.5W (200 MHz)	15.7 W (200 MHz)	15.0 W	17.0W (200 MHz) 15.0W (125–180 MHz)
No. of V_{CC2} Pins	None	25	None	28
No. of V_{CC3} Pins	53	28	60	32
No. of V_{CC5} Pins	None	2	2	
External Plane Type	Unified	Split	Unified	Unified or Split
Internal Plane Type	Unified	Split	Unified	Split
Package Type	296-pin PPGA or CPGA	296-pin PPGA or CPGA	320-pin CPGA	320-pin CPGA

NOTES:

1. I_{CC3} refers to V_{CC3} (I/O) supply current.
2. I_{CC2} refers to V_{CC2} (Core) supply current.
3. I_{CC5} refers to 5V supply current. This is used to power the fan/heatsink on the Pentium® OverDrive® processors.
4. Pentium OverDrive processors and future Pentium OverDrive processors with MMX™ technology do not require the bus frequency ratio to be changed when upgraded.
5. The number shown represents worst case or maximum current/power at highest available frequency.
6. When the future Pentium OverDrive processor with MMX technology is installed in split plane designs, 4600 mA at 3.3V is drawn through V_{CC2} pins and 400 mA from V_{CC3} pins.
7. The 200 MHz future Pentium OverDrive processor with MMX technology will only be supported in Socket 7 designs.

- **BF1-0: The bus fraction selection pins determine the bus to core frequency ratio. The BF pins are sampled by the processor at RESET, and will not be sampled by the processor again until another cold-boot (1ms) assertion of RESET. The signal on the BF pins is not an indication of the bus speed, only the ratio of the processor core with respect to the bus. The Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology do not require the BF pins to be changed when upgraded and will operate properly with the bus fraction ratio selected for the processor being replaced. Table 2 summarizes the operation of the BF pins on Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium processors with MMX technology.**

- **CLK, PICCLK: The clock inputs on the Pentium processor with MMX technology are not 5V tolerant. The clock inputs to the processor on the flexible motherboard are driven by an appropriate 3.3V clock driver. Driving the clock at 3.3 volts is also compatible with the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the Pentium OverDrive processor, and the future Pentium OverDrive processor with MMX technology.**

2.3. Processor Identification

The CPUID instruction is used to provide information to the BIOS and other software about the vendor, family, model, and stepping of the processor. An input value of 1 loaded into the EAX register prior to executing the CPUID instruction will return the identification signature in the EAX register. Figure 2 shows the EAX bit assignment for the CPUID instruction. (For more details, refer to application note AP-485, *Intel Processor Identification with the CPUID Instruction*. See Appendix E.)

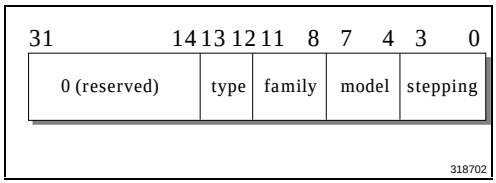


Figure 2. EAX Bit Assignments for CPUID

Table 3 provides the CPUID information for the different processors that are supported on the flexible motherboard.

Table 2. BF1-0 Core/Bus Ratio Selection Pins (1)

BF1 Value (5)	BF0 Value (5)	Pentium® Processor 75 / 90 / 100 / 120 / 133 / 150 / 166 200 Frequency Ratio	Pentium Processor with MMX™ Technology Frequency Ratio
0	0	2/5 (2)	2/5 (2)
0	1	1/3	1/3
1	0	1/2 (3)	1/2 (3) (Default)
1	1	2/3 (4) (Default)	Reserved

NOTES:

1. The Pentium processors with a maximum rated core frequency of less than 75 MHz have only one bus fraction ratio defined – (1:1).
2. The 2/5 ratio is defined on the Pentium® processor with MMX™ technology and Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200.
3. Defaults to 1/2 ratio if BF1 and BF0 are left unconnected on the Pentium processor with MMX technology. On the Pentium processor with MMX technology, the BF1 pin has an internal pull-up resistor, and the BF0 pin has an internal pull-down resistor.
4. Defaults to 2/3 ratio if BF1 and BF0 are left unconnected on Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200. On the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the BF1 and BF0 pins have internal pull-up resistors.
5. The value of external pull-down resistors used on the BF0/BF1 pins should be 500 ohms or less. The value of external pull-up resistors used on the BF0/BF1 pins should be 2.2 Kohms or less.

Table 3. CPUID Information

Type Bits(13:12)	Family Bits(11:8)	Model Bits(7:4)	Stepping Bits(3:0)	Description
00	0101	0010	xxxx	Pentium® processors (75, 90, 100, 120, 133, 150, 166, 200)
00	0101	0100	xxxx	Pentium processor with MMX™ technology (166, 200)
00 (1)	0101	0010	xxxx	Pentium OverDrive® processor for Pentium processor (75, 90, 100)
01	0101	0100	xxxx	Future Pentium OverDrive processor with MMX technology for Pentium processor (75, 90, 100, 120, 133, 150, 166, 200)

NOTES:

1. The definition of the type field for the OverDrive® processor is 01. An errata on the Pentium® OverDrive processor will always return 00 as the type.

3.0. FLEXIBLE MOTHERBOARD IMPLEMENTATION

This chapter describes the implementation of a split plane flexible motherboard using Socket 7.

3.1. Voltage Supply Implementation Overview

In order to support the various members of the Pentium processor family with different voltage requirements, the flexible motherboard should include provisions for both 2.8V and 3.3V supply voltages for the processor.

The power supply pins on the Pentium processor with MMX technology are split into separate V_{CC2} and V_{CC3} pins. Socket 7 definition splits the 60 V_{CC} pins on Socket 5 into 28 V_{CC2} pins and 32 V_{CC3} pins. These pins are connected appropriately to the processor core voltage island and processor I/O voltage island. The Pentium processor with MMX technology uses 5.7A at 2.8V (200 MHz) for its core from the supply voltage solution. The 3.3V I/O voltage for the Pentium processor with MMX technology is supplied by the system (either through the 3.3V power supply or through a 3.3V voltage regulator on the motherboard).

The voltage provided to the core of the future Pentium OverDrive processor with MMX technology is supplied by a voltage regulator, internal to the OverDrive processor package, powered by 3.3V on the V_{CC2} pins. The I/O is powered directly from the 3.3V V_{CC3} pins. The voltage supply solution on the flexible motherboard supplies a minimum of 0.4A at 3.3V on V_{CC3} and 4.6A at 3.3V on V_{CC2} to support the 200 MHz future Pentium OverDrive processor with MMX technology. It is not required that both power planes be supplied by the same source. In addition, the Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology also use a +5V supply to power the fan/heatsink.

In a typical single processor system, the 3.3V power supply uses approximately 7A to power all the 3.3V components (i.e. processor, cache and chipset). In the 200 MHz Pentium processor with MMX technology, the 2.8V regulator draws up to approximately 5.7A at 2.8V for the processor core while the 3.3V power supply should require approximately 2A at 3.3V for the cache and chipset. Additional 3.3V devices such as 3.3V DRAM may require additional power. Actual power requirements should be calculated for the specific design.

3.2. The Distinct Power Planes

A typical desktop flexible motherboard contains a maximum of four different power planes. Any Pentium processor will directly plug into two of these planes (V_{CC2}, V_{CC3}) and may be indirectly connected to the 3.3V power supply ($3V_{POWER\ SUPPLY}$) through the $V_{I/O}$ (V_{CC3}) power plane. See Figure 3. For the most economically flexible motherboard design, it is recommended that the $V_{I/O}$ plane simply be connected to the

motherboard's $3V_{POWER\ SUPPLY}$ by jumpers or 0Ω resistors. Therefore, excluding the main 5V power plane, the Pentium processor family flexible motherboard may have a minimum of two distinct motherboard power planes: V_{CORE} and $V_{I/O}$ + $3V_{POWER\ SUPPLY}$. However, some board designers may power the $V_{I/O}$ plane with VRE voltage instead and keep it isolated from the $3V_{POWER\ SUPPLY}$. This will then maintain the total possibility of four separate power planes.

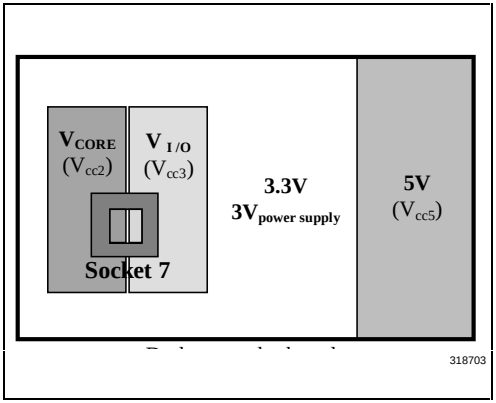


Figure 3. The Typical Power Planes in a Desktop Pentium® Processor Family Flexible Motherboard

The power plane distinctions are described below.

V_{CORE} — This power plane is connected to the V_{CC2} power pins on the Pentium processor family's Socket 7 connector (see Figure 3). When a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 is installed in the system, this plane will typically be connected to the $V_{I/O}$ plane through 0Ω resistors, jumpers, or the internal power plane of the Pentium processor. However, in the case of the Pentium processor with MMX technology, the V_{CC2} and V_{CC3} planes remain completely electrically separate. Also, the future Pentium OverDrive processor with MMX technology will not connect V_{CC2} and V_{CC3} through its internal power planes. Depending upon which processor is being supported, the V_{CC2} plane may require either a discrete 2.8V voltage regulator, or a configurable 2.8V/3.3V/VRE voltage regulator. The VCC2DET# signal can be used to select between 2.8V and 3.3V/VRE on the configurable V_{CORE} voltage regulator. The V_{CORE} power plane uses a voltage regulator that can supply at least 5.0A at 3.3V for a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and at least 5.7A at 2.8V for a Pentium processor with MMX technology.

$V_{I/O}$ — This power plane is connected to the V_{CC3} power pins on the Pentium processor family's Socket 7 connector. The $V_{I/O}$ plane may also be connected to the $3V_{POWER\ SUPPLY}$ plane (if the motherboard power supply is used instead of a 3.3V/VRE voltage regulator). Therefore, the $V_{I/O}$ plane may require either an electrical connection to the motherboard's $3V_{POWER\ SUPPLY}$, or its own discrete 3.3V/VRE voltage regulator. When isolated from the $3V_{POWER\ SUPPLY}$, the processor's V_{CC3} pins may only require as little as 0.65A (at 200 MHz) as is the case in the Pentium processor with MMX technology. However, in order to minimize the number of discrete 3.3V voltage regulators in a flexible motherboard, it is recommended that the $V_{I/O}$ plane connect the processor's V_{CC3} pins with the motherboard's L2 cache, chipset and any 3.3V DRAM. Since the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 (a unified-plane processor) has its V_{CORE} + $V_{I/O}$ plane supplied with VRE voltage, the V_{CORE} + $V_{I/O}$ plane may need to be isolated from the 3.3V components and $3V_{POWER\ SUPPLY}$. See Figure 5. An auto-configurable flexible motherboard should make provisions for connecting/disconnecting the $V_{I/O}$ and $3V_{POWER\ SUPPLY}$ in order to accommodate processors running on VRE voltage or 3.3V voltage (see next section).

$3V_{POWER\ SUPPLY}$ — This power plane is the motherboard's 3.3V power plane (not to be confused with the motherboard's 5V power plane). This typically powers the 3.3V cache, chipset and DRAM components on the Pentium processor family flexible motherboard. In cost effective motherboards, the $3V_{POWER\ SUPPLY}$ is typically connected to the $V_{I/O}$ power plane; however, if the processor is a unified-plane processor, this plane will then be connected to both the $V_{I/O}$ and V_{CORE} power planes as well (see next section). In a split plane, dual voltage processor, like the Pentium processor with MMX technology, the $3V_{POWER\ SUPPLY}$ plane will be separated from the V_{CORE} power plane.

NOTE

The future Pentium OverDrive aprocessor with MMX technology will not internally connect V_{CORE} to $V_{I/O}$.

$5V_{POWER\ SUPPLY}$— This is the motherboard's 5V power plane. This plane will power the 5V components such as DRAM, keyboard controller, mouse, FLASH BIOS memory, TTL Logic, and some I/O bus components and connectors.

3.3. Split Plane Processor/Unified Plane Processor Design Configurations

Currently, the Pentium processor family line may be divided into three power plane categories (*see Figure 4 and Table 4*):

The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium OverDrive processor have an internal unified power plane. This means that the V_{CC2} and V_{CC3} power pins are connected to a single power plane internal to the processor package. The processor may be operated by applying 3.3V/VRE to both the V_{CC2} power pins and V_{CC3} power pins simultaneously, or by applying 3.3V/VRE power to either the V_{CC2} pins or the V_{CC3} pins separately. Since the internal power plane is unified, the power from the V_{CC2} pins will flow to the V_{CC3} pins and vice-versa.

In designing flexible motherboard options, the V_{CORE} and $V_{I/O}$ power planes may be electrically isolated or they may be shorted together by jumpers or 0Ω resistors. In the case where the V_{CORE} and $V_{I/O}$ power planes are isolated (and there are no jumpers or 0Ω resistors to combine the two motherboard power planes), the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium OverDrive processor will serve as the means of conduction that shorts the two power planes together provided the current flow through the processor does not exceed 8A. See Figure 5. This scenario would never occur with a Pentium processor with MMX technology, nor with a future Pentium OverDrive processor with MMX technology, because of their internal split power plane design.

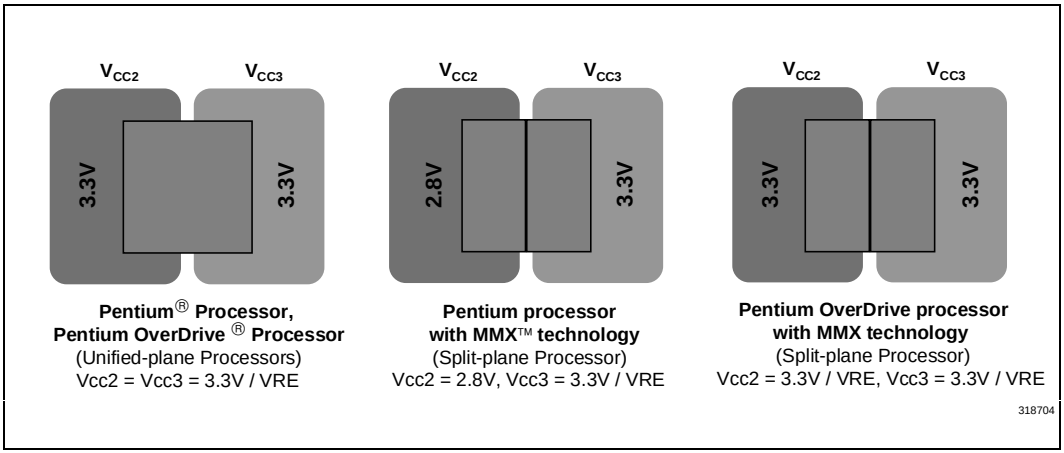


Figure 4. Pentium® Processor Family Power Plane Characteristics

Table 4. The Three Types of Pentium® Processor Power Planes

Category	Processor
Unified Plane processors with Single Voltage Input (V_{CC} = 3.3V/VRE)	Pentium® processors 75 / 90 / 100 / 120 / 133 / 150 / 166 200 MHz, Pentium OverDrive® processors 125/150/166 MHz
Split-Plane processors with Dual Voltage Input (V_{CC2} = 2.8V & V_{CC3} = 3.3V/VRE)	Pentium processors with MMX™ technology (166, 200 MHz)
Split-Plane processors with Single Voltage Input (V_{CC} =3.3V/VRE)	Future Pentium OverDrive processors with MMX technology 125/150/166/180/200 MHz

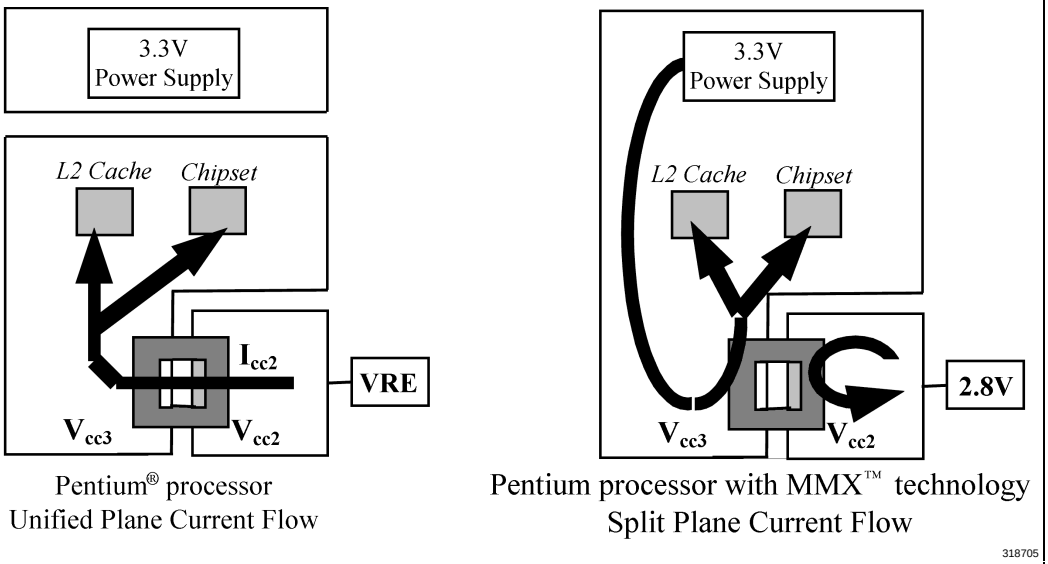


Figure 5. Unified Plane Current Flow vs. Split Plane Current Flow

The Pentium processor with MMX technology has an internal split power plane which means that the V_{CORE} and $V_{I/O}$ power planes, which are internal to the processor package, are electrically isolated. For proper processor operation, the V_{CC2} pins have to be supplied with 2.8V while the V_{CC3} pins have to be supplied simultaneously with 3.3V/VRE.

The future Pentium OverDrive processor with MMX technology also has an internal split power plane which means that the V_{CORE} and $V_{I/O}$ power planes, internal to the processor package, are also electrically isolated. In order to properly operate this OverDrive processor, the V_{CC2} pins and V_{CC3} pins must always be powered simultaneously with 3.3V/VRE.

NOTE

The two power planes do not have to be powered by the same voltage source.

3.4. Power Plane Connections and Voltage Regulator Shutdown

As a flexible motherboard option, the two V_{CORE} and $V_{I/O}$ power planes have the option of being connected via 0Ω resistors, jumpers, a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 or Pentium OverDrive processor, shorting blocks, or even MOSFETs (see Figure 6). MOSFETs are typically implemented in flexible motherboards with an auto-detect circuit and are an ideal solution for designing in an "automatic" power plane selection device using VCC2DET# as an input.

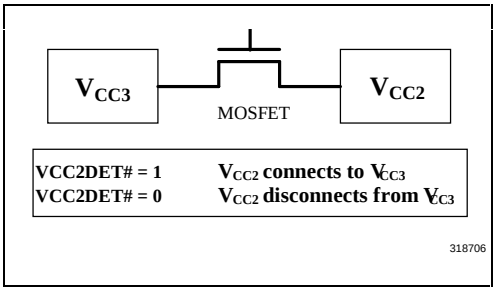


Figure 6. Use of MOSFETs to Connect/Disconnect Power Planes

If a unified-plane processor is plugged into a flexible motherboard with two voltage regulators, one of the voltage regulators may "shut down". The voltage regulator attached to the V_{CC2} power pins will always have a much higher current rating than the voltage regulator attached to the V_{CC3} power pins because the V_{CC2} plane directly powers the processor core. When a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 or Pentium OverDrive processor is plugged into the system, the current will flow from the V_{CC2} plane to the V_{CC3} power plane and shut down the weaker voltage regulator (the weaker voltage regulator will detect the increased current and shut itself down). This is acceptable provided the 8A maximum specification for current flow across a unified plane processor is maintained (see Figure 7). However, when a split plane processor, like the Pentium processor with MMX technology or the future Pentium OverDrive processor with MMX technology, is inserted in the socket, the two regulators are electrically isolated and each continues to function. Also, the designer may design the motherboard such that the two voltage regulators current share; however, this is an implementation specific option and up to the designer's discretion.

3.5. Voltage Supply Implementation Options

There are several voltage supply implementation options to support all the different Pentium family processors on the flexible motherboard. The following options will be discussed in this section:

1. **Using a 2.8V/3.3V auto-configurable voltage regulator.**
2. **Using an on-board 2.8V regulator as a build option.**
3. **Using the Voltage Regulator Module (VRM). Refer to Appendix A.**

3.5.1. 2.8V/3.3V AUTO-CONFIGURABLE REGULATOR

An auto-configurable regulator circuit is an option for supply voltage implementation on the flexible motherboard. This approach allows all Pentium processors 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processors, Pentium processors with MMX technology, and future Pentium OverDrive processors with MMX technology to be easily supported without the need for any jumper/resistor configuration. Figure 8 shows two regulators that work together to form an auto-configurable voltage solution.

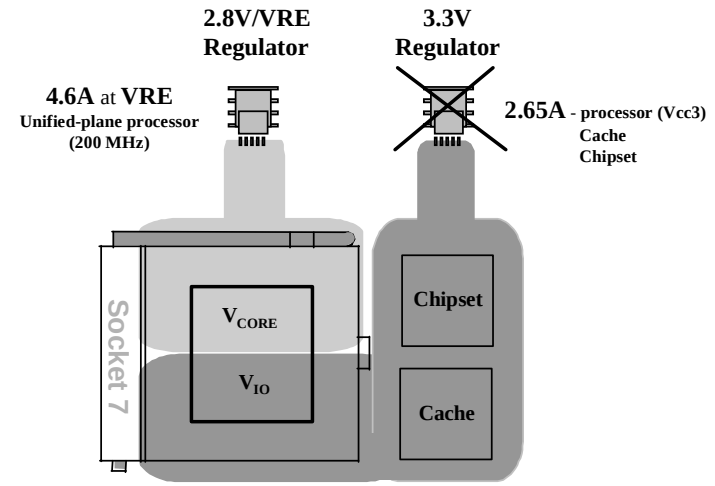


Figure 7. Regulator Shutdown Phenomenon

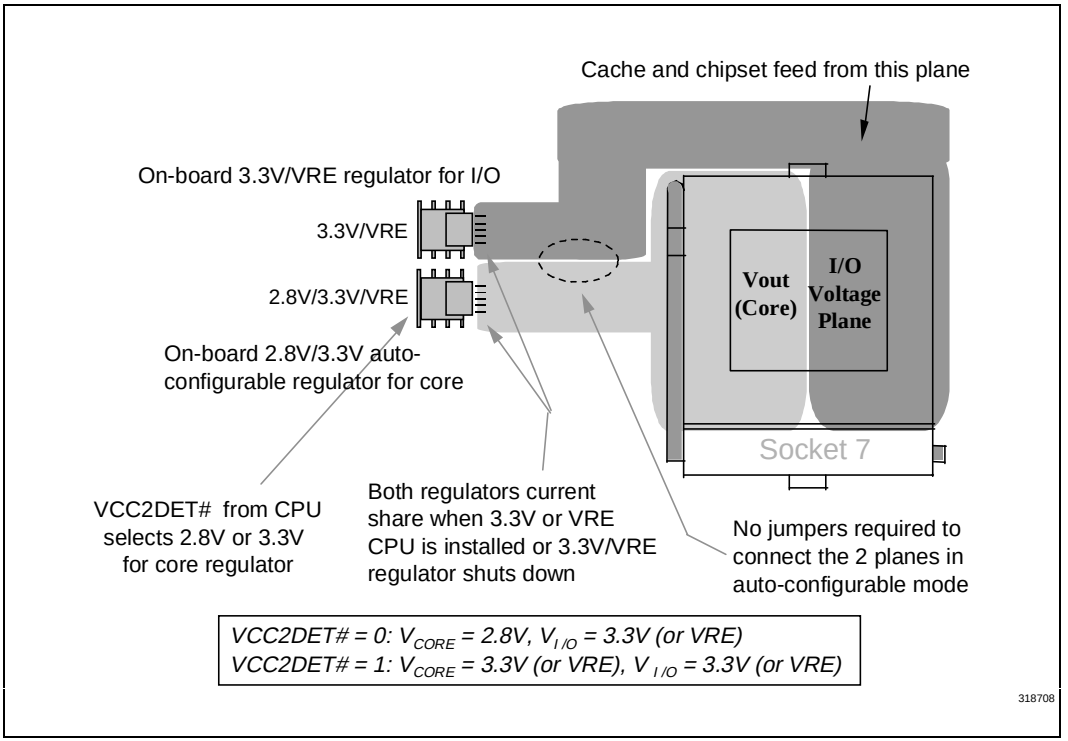


Figure 8. Auto-Configurable Voltage Regulator Solution

The VCC2DET# pin, defined on the Pentium processor with MMX technology and Socket 7, is used to steer the voltage regulator supplying the processor core to the correct voltage depending on which processor is in the socket. On the Pentium processor with MMX technology, the VCC2DET# pin is always driven low (or grounded). On the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology, this pin is an internal no connect; therefore, the VCC2DET# signal trace needs an external pull-up resistor so that the auto-configurable regulator circuit does not confuse a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 with a Pentium processor with MMX technology and apply the incorrect input voltages.

When a unified-plane processor (Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 or Pentium OverDrive processor) is plugged into a Socket 7 in the auto-configurable system, the following events take place:

1. **The VCC2DET# signal is not asserted and the 2.8V/3.3V/VRE voltage regulator toggles to either 3.3V or VRE voltage.**
2. **The V_{CORE} and $V_{I/O}$ power planes automatically become electrically shorted (V_{CORE} + $V_{I/O}$) because the processor unifies these two planes internal to the package. This is within processor specification provided that the total sum of electrical current flowing through the processor does not exceed 8A. The 2.8V/3.3V/VRE voltage regulator would have to be sized to accommodate the current draw of any other components attached to the V_{CORE} + $V_{I/O}$ plane. The 8A of current should be adequate to power the processor, cache and chipset.**
3. **The 3.3/VRE voltage regulator will then shut itself down as it detects the power flow of the much larger 2.8/3.3V/VRE voltage regulator.**

When a split-plane, dual voltage processor (Pentium processor with MMX technology) is plugged into a

Socket 7 in the auto-configurable system, the following events take place:

1. The VCC2DET# signal is asserted and the 2.8V/3.3V/VRE voltage regulator toggles to 2.8V voltage.
2. The V_{CORE} and $V_{I/O}$ power planes remain electrically isolated because the processor splits these two planes internal to the package.
3. The 3.3V/VRE voltage regulator continues to function and supply the $V_{I/O}$ power plane which may include both the processor's V_{CC3} pins and any cache and chipset on the $V_{I/O}$ plane.

When a split-plane, single voltage processor (future Pentium OverDrive processor with MMX technology) is plugged into a Socket 7 in the auto-configurable system, the following events take place:

1. The VCC2DET# signal is not asserted and the 2.8V/3.3V/VRE voltage regulator toggles to either 3.3V or VRE voltage.
2. The V_{CORE} and $V_{I/O}$ power planes remain electrically isolated because the processor splits these two planes internal to the package.
3. The 3.3V/VRE voltage regulator continues to function and supply the $V_{I/O}$ power plane which may include both the processor's V_{CC3} pins and any cache and chipset on the $V_{I/O}$ plane.

An auto-configurable voltage regulator solution may also be designed-in as a manufacturing stuffing option. In this case, both regulators are designed-in but only one regulator is populated on the board. This regulator needs to provide enough current capability to drive both the core and the I/O voltage planes. With only one regulator in the system, 4–6 0Ω resistors or external jumpers are also needed to connect both the core and I/O planes at manufacturing time (for split-plane, single voltage processors). When the second regulator and associated circuitry is populated on the board, these jumpers are removed or left out to provide the full auto-configurable capability.

3.5.2. 2.8V REGULATOR AS A BUILD OPTION

In this implementation option, the flexible motherboard is configured at manufacturing build or assembly time for either the Pentium processor, 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 (unified-plane, single-voltage processor) or the Pentium processor with MMX technology (split-plane, dual voltage processor).

NOTE

All Pentium OverDrive processors and future Pentium OverDrive processors with MMX technology are intended as a consumer upgrade product for unified-plane, single-voltage processors.

As shown in Figure 9, a 2.8V voltage regulator is designed-in and populated when the board is configured to support the Pentium processor with MMX technology.

When the 2.8V voltage regulator is not installed on the board, a Motherboard build option of 4–6 jumpers or 0Ω resistors (i.e. , #1206, 1/8 watt, surface mount resistors) is recommended to connect the core and I/O voltage planes (in split-plane, single voltage processors and, optionally, unified-plane, single voltage processors as well) for an approximate current carrying capability of approximately 5–8 amps (dependent upon the quantity of components). However, a unified-plane processor will conduct current between the core and I/O voltage planes without a need for jumpers/resistors. Conversely, when the 2.8V voltage regulator is assembled on the motherboard, the jumper/resistor build option should not be added in order to isolate the two voltage planes.

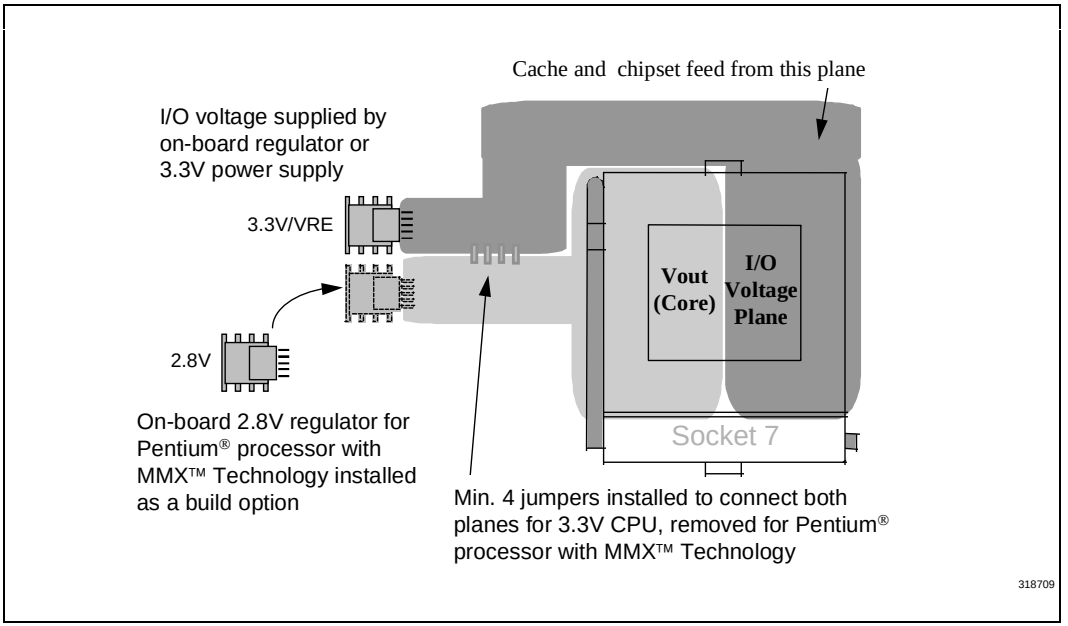


Figure 9. 2.8V Voltage Regulator Designed as a Build Option

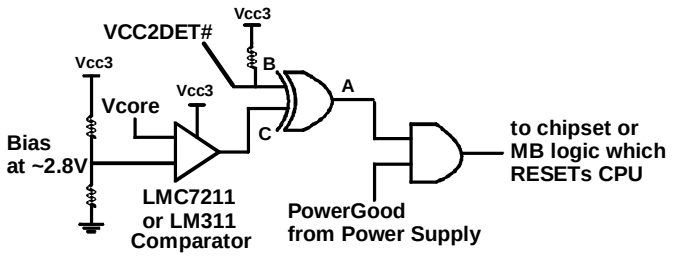
3.5.3. SAFEGUARDING THE PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY ON THE FLEXIBLE MOTHERBOARD

The Pentium processor with MMX technology core operates at 2.8V. A Socket 7 based flexible motherboard design that is not configured for 2.8V should implement some type of safeguarding mechanism to protect the Pentium processor with MMX technology from getting the wrong voltage. Operating the Pentium processor with MMX technology's core at 3.3V could potentially cause damage to the processor.

The VCC2DET# pin defined on the Pentium processor with MMX technology and Socket 7 may be used to implement some type of protection circuitry that can be used to either disable the voltage source or prevent the processor from booting if the wrong voltage is detected.

The example circuit shown in Figure 10 may be used to prevent RESET from being generated to the processor if the wrong core voltage is detected. This circuit uses a comparator to compare the core voltage to a reference voltage (~2.8V). If VCC2DET# is grounded (for the Pentium processor with MMX technology) and the core voltage is greater than the reference voltage, the output of the exclusive OR gate will be low which would signal the chipset to not assert RESET. Similarly if VCC2DET# is high (for 3.3V processor), and the core voltage is lower than the reference voltage, the chipset should not be allowed to assert RESET.

Another example of safeguard implementation is shown in Figure 11. The approach here is to reduce the output voltage of the core regulator (3.3V or VRE) if a low level on VCC2DET# pin is detected. This would be a simpler and cheaper implementation for designs that are using an adjustable voltage regulator, where the output voltage level can be adjusted using a resistor divider. As shown in Figure 9, the value of the resistor divider is altered appropriately (bottom resistor is shorted to ground) when VCC2DET# indicates a zero. This effectively can reduce the output voltage to an appropriate level for the Pentium processor with MMX technology.



Vcore (C)	Vcc2DET# (B)	(A)
2.8V (1)	(0) Pentium processor with MMX Technology	1
2.8V (1)	(1) Pentium processor	0
3.3V (0)	(0) Pentium processor with MMX Technology	0
3.3V (0)	(1) Pentium processor	1

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Figure 10. External Safeguard Circuit to Prevent Processor from Booting

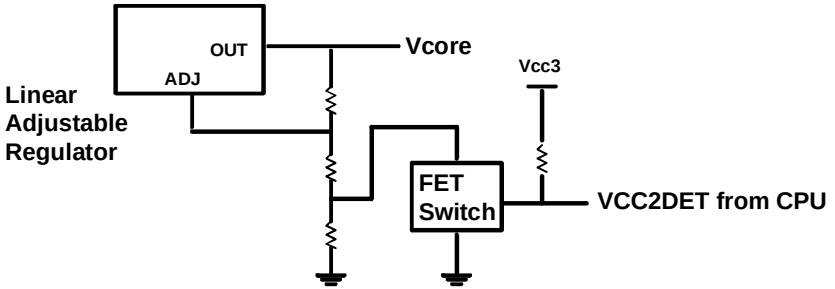

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Figure 11. External Safeguard by Reducing the Output Voltage

3.6. Split Power Plane Layout

Implementing a power island on an existing power layer instead of assigning a separate power layer for core V_{CC} can be a more economical solution. The separate voltage island can be isolated from the other section of the power plane using an air gap. The size of the air gap is determined by analysis of the noise effects and board manufacturing capabilities (typically 10–20 mils).

Figure 12 shows a typical layout of the separate voltage islands in the processor area. It shows the core V_{CC} pins (V_{CC2}) clustered on one side of the processor to allow easy layout of the core voltage island. The remaining V_{CC} pins for the periphery (V_{CC3}) are located on the other side and are part of the I/O voltage island (refer to Socket 7 pinout, see Appendix B).

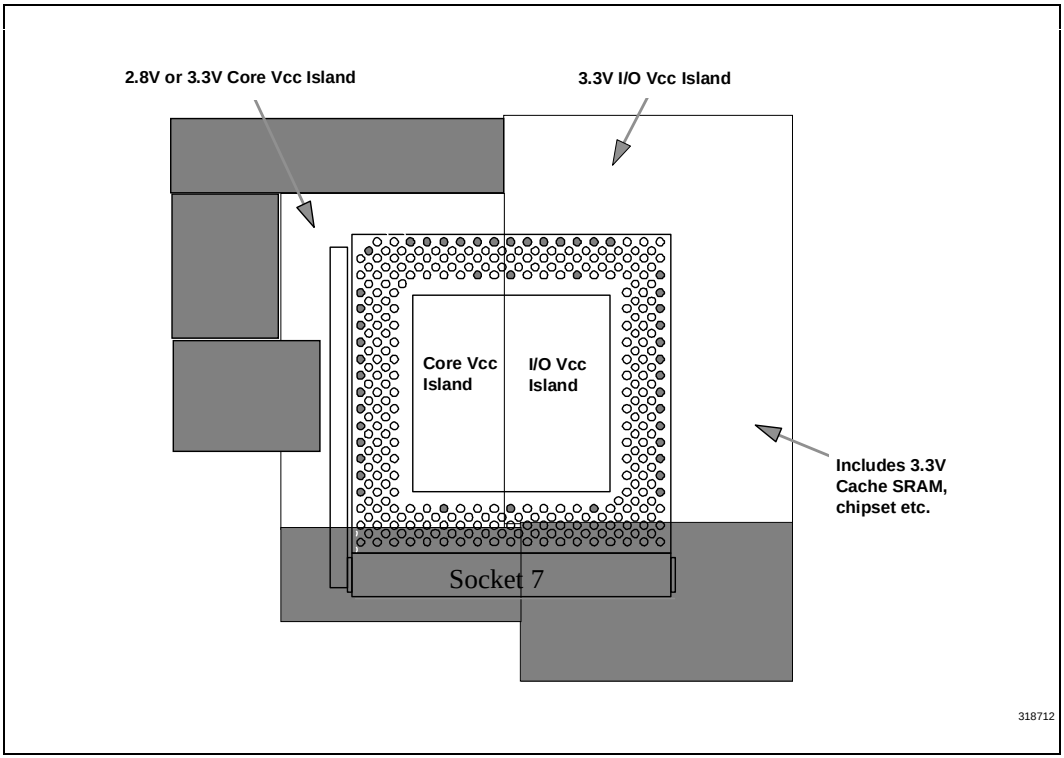


Figure 12. Processor Power Island Layout

The I/O V_{CC} island should also include other 3.3V components that interface with the processor. A typical configuration would include 3.3V cache SRAM, 3.3V chipset I/O, and processor I/O on the same 3.3V I/O voltage island. This ensures that signals interfacing between the processor and other 3.3V components operate at the same voltage levels. This is also to avoid split plane crossovers for these signals which is recommended for better signal quality and reduced EMI/RFI effects.

When using jumpers or 0Ω resistors to connect the two power planes (in the case of single voltage processors), the number of jumpers should be chosen so as to provide enough current carrying capability. Insufficient number of jumpers will result in excessive voltage drop and other reliability problems. For the flexible motherboard, a minimum of four (six recommended) zero-ohm, #1206, 1/8 watt, surface mount resistors should be used.

Routing of the power source to the voltage islands should also be carefully done to avoid significant voltage drop at the processor and an increase in thermal dissipation in the voltage islands. It is recommended that wide traces be used to prevent excessive voltage drop across the power plane. Also vias and through-holes cutting through the power plane at critical widths should be avoided.

3.7. Decoupling

The small size of the processor core voltage island, its isolation from the motherboard power plane, and support of varied voltage requirements make proper decoupling of the island power plane voltage and ground plane essential. Appropriate decoupling capacitors are implemented on the voltage island near the processor to ensure that the processor voltage stays within specified limits during normal and transient conditions. There are two types of decoupling that need to be considered: bulk decoupling and high frequency decoupling.

3.7.1. BULK DECOUPLING

For the processors supported on the flexible motherboard, the power consumption can transition from a low level to a much higher level (or vice versa) very rapidly. This can happen during normal program execution; however, a higher surge of current typically occurs when entering or exiting the Stop Grant state. Another example is when executing a HALT instruction which causes the processor to enter the Auto-HALT Power Down state, or transition from HALT back to the Normal state.

NOTE

The Auto-HALT Power Down feature is always enabled even when other power management features are not implemented.

All of these examples may cause abrupt changes in the power consumed by the processor.

As the voltage supply (regulator) cannot respond to a sudden load change instantaneously, bulk storage capacitors with low ESR (Effective Series Resistance) are used to maintain the regulated supply voltage during the interval that falls between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

3.7.2. HIGH FREQUENCY DECOUPLING

High frequency decoupling may be required to provide a short, low impedance path to high frequency components such as high current spikes in order to minimize noise. The processor driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

For high frequency decoupling, low inductance capacitors and interconnects are recommended for best high speed electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. Surface mount capacitors are preferable, as capacitors with long leads add inductance to the circuit. The capacitors should be of RF grade, with low ESR and low inductance to reduce spikes.

3.7.3. DECOUPLING RECOMMENDATIONS

Table 5 shows the processor decoupling recommendations for the flexible motherboard for both the processor core and I/O voltage islands. This is based on simulation and testing of the voltage transients from the processor and the effects of motherboard decoupling.

Spice modeling (modeling worst case current transients including the processor package inductance, capacitance, routing, decoupling, voltage regulator output inductance, etc.) should be used to estimate the amount of decoupling capacitance for the processor voltage island.

It is highly recommended that before committing to any change from the decoupling capacitor recommendation, the solution be simulated for the variety of variables in components, temperature and lifetime degradation.

Table 5. Decoupling Recommendations for Processor Core and I/O Voltage Islands

	Quantity	Value	ESR	ESL	Type
Processor Core Voltage Island	4	100 µF	25 mOhms (1)	0.45 nH (3)	Tantalum
	25	1 µF	0.6 mOhms (2)	0.084 nH (4)	X7R dielectric, ceramic
Processor I/O Voltage Island (5)	12	0.1 µF			603 Type

NOTES:

1. ESR per capacitor should be less than 100 mOhms.
2. ESR per capacitor should be less than 15 mOhms.
3. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.7 nH.
4. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.1 nH.
5. This does not include decoupling for components other than the processor in the 3.3V I/O voltage island.

For bulk decoupling, tantalum capacitors are recommended over electrolytic capacitors. In general, electrolytic capacitors degrade at a much faster rate, are not as accurate, and are not as stable over temperature as tantalum capacitors.

For high speed decoupling in the processor core voltage island, low inductance, 1µF capacitors of X7R dielectric are recommended. These capacitors not only decouple the processor core for high frequency noise but also control the voltage during very fast transients (less than 100 ns.) Figure 13 shows that ceramic capacitors of X7R (or X7S) dielectric exhibit relatively stable capacitor characteristics over temperature compared to capacitors of Z5U or Y5V type dielectric. For example, at a typical operating temperature of 45°C, the Y5V dielectric can lose 45% of the initial rated capacitance.

Measurement techniques to ensure that motherboard designs are within V_{CC} noise and transients specification are discussed in the following application notes (see Appendix E for order information).

- **Voltage Guidelines for Pentium® Processors with MMX™ Technology Processors**
- ***Implementation Guidelines for Pentium® Processors with VRE Specifications***

3.7.4. PLACEMENT OF DECOUPLING CAPACITORS

Figure 14 shows an example of how the recommended processor decoupling capacitors (Table 5) should be placed inside the respective voltage islands on the flexible motherboard. The bulk capacitors should be placed near the processor inside the voltage island to ensure that the supply voltage stays within specified limits during changes in the supply current during operation. The 1 µF, X7R capacitors should be evenly distributed inside the processor core voltage island inside and around the processor footprint. Figure 12 also shows the twelve 0.1 µF capacitors evenly placed around the processor, close to the processor V_{CC3} pins inside the processor I/O voltage island.

In this example, all the capacitors were placed on one side of the board. If components are assembled on both sides of the board then these capacitors can be distributed between the top and bottom sides. If done this way, vias connecting the capacitor pads to the power and ground layer can be shared between the capacitors on the top and bottom sides. This can help reduce the total overall capacitor inductance.

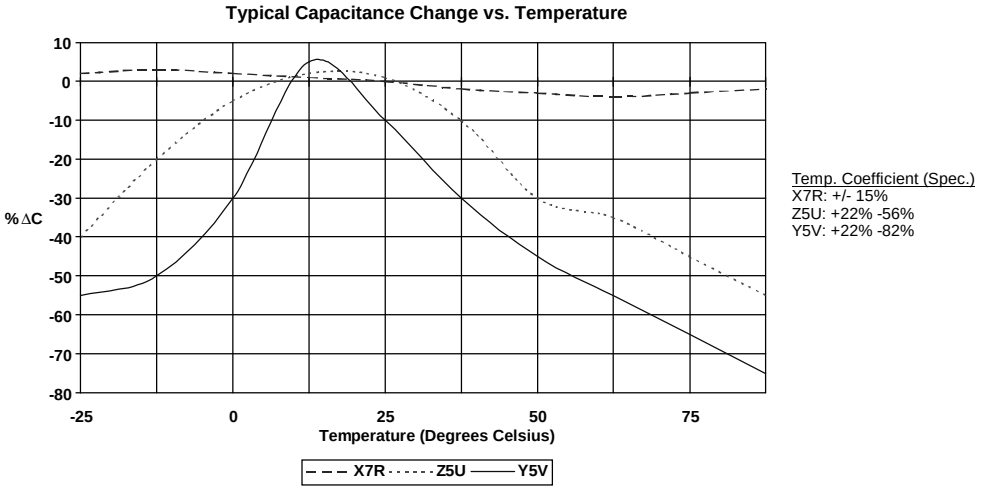


Figure 13. Typical Capacitor Characteristics

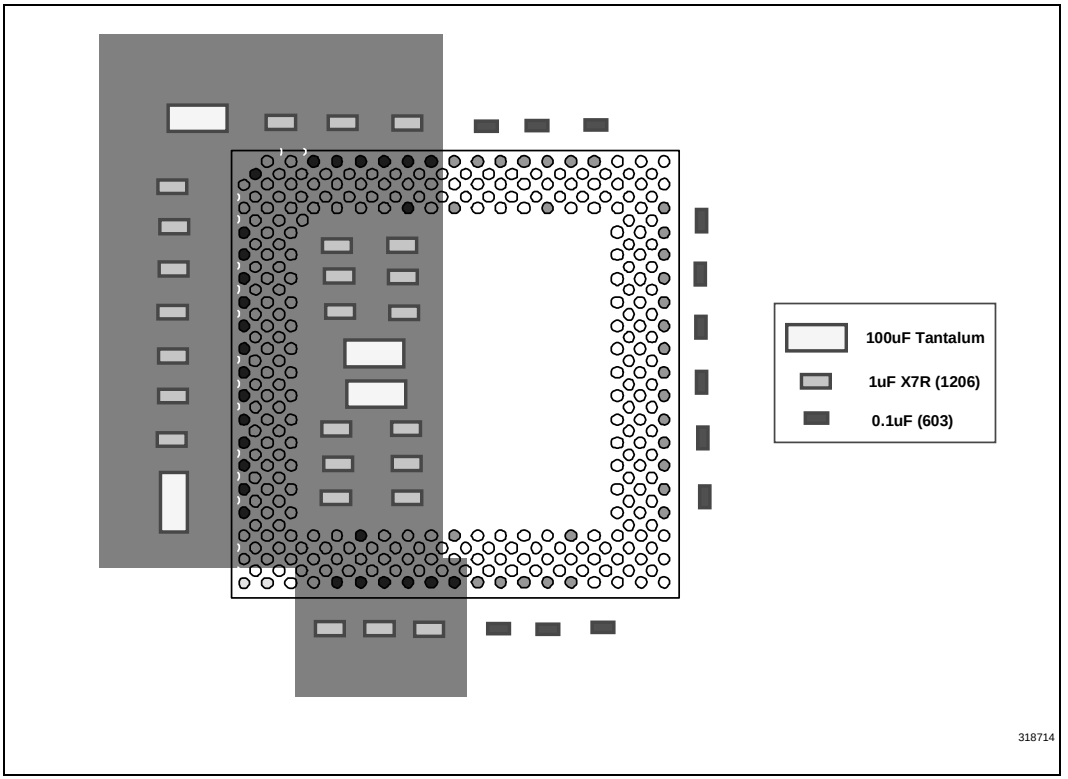


Figure 14. Example of Processor Decoupling Capacitor Placement

The traces connecting the vias to the capacitor pads should be kept as short as possible. In cases where it is difficult to reduce the length of the circuit board trace, the trace should be made wider so as to reduce the trace inductance.

3.8. Signal Routing Guidelines

As the power plane on the flexible motherboard is split into separate voltage islands, signal routing should be done in such a way so as to minimize crossovers between voltage islands for high speed signals. Signal routing between the voltage islands and the system power plane should be limited to only those signals that absolutely need to cross the gap between the island and the power plane. This is to avoid possible signal degradation from impedance discontinuity effects. Significant levels of EMI could be generated by electromagnetic radiation from high speed traces (such as clocks, strobes, data lines, and low address lines) when their return path is interrupted. On a multi-layer board this return path is on the power or ground plane that is adjacent to the signal layer directly under the signal trace. If this trace is routed over a break in the return path, the return current has to find another longer path in order to maintain current continuity. The increased area generated by the signal trace and the length of this extended return path can lead to increased radiation levels from this signal trace.

The following guidelines should be followed when routing high speed signals on the flexible motherboard:

Clocks and Strobes: These signals should not be routed over breaks in the reference plane return path. Use of vias to connect between signal planes should be minimized, and the signal planes should be within 8 mils of the reference plane. Clock

signals should be routed on the layer that is adjacent to the ground layer.

Data Bus and Low Address Lines: These signals can be routed on any signal layer. However, it is desired that the number of traces crossing over splits in the return path plane be minimized and ideally kept to zero. Among this group, signals that do need to cross the gap should be routed on the signal layer near the ground plane to minimize radiated emissions (using a via, a trace may be taken down to the layer that is referenced to the ground plane). On a four layer board, the signal layer with the least potential for signal crossovers should be placed adjacent to the power plane. Capacitive decoupling across the split planes can also be used near signal crossovers (for those which cannot be avoided) to help reduce the magnitude of EMI radiation. Within an inch of the signal crossover violation, a 0.1 μF ceramic capacitor should be placed across the power plane gap, using one capacitor for every three trace violations (provided they are all within the one inch limit).

3.9. Thermal and Physical Space Considerations

The thermal design of a system using the flexible motherboard should be based on the worst case power dissipation and related thermal requirements for the processors that are supported.

The Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 and Pentium processor with MMX technology use OEM specified heatsinks which are dependent upon the entire system cooling solution. The maximum case temperature for these processors should not exceed 70°C to ensure proper operation. Heatsinks also may need a certain airflow in order to maintain their specified temperature. For detailed information refer to the respective datasheet for these processors (see Appendix E). In addition, detailed discussion of thermal design issues for the Pentium processor is covered in *Pentium® Processor Thermal Design Guidelines* (see Appendix E).

The Pentium OverDrive processors and future Pentium OverDrive processors with MMX technology are shipped with integrated fan/heatsink cooling solutions. Although these fan/heatsinks remove the heat from the package, the system should be able to dissipate the added heat to the system. From Table 1, the future Pentium OverDrive processor with MMX technology dissipates the most power at 200 MHz. The system provides sufficient airflow to dissipate this power from the system and prevent the temperature of the air entering the fan/heatsink from exceeding 45°C. When the T_A (max) ≤ 45°C specification is met (T_A = ambient temperature), the Pentium OverDrive processor and future Pentium OverDrive processor with MMX technology fan/heatsink will keep T_C (case temperature) within the specified range, provided airflow through the fan/heatsink is unimpeded. The ambient temperature should be measured approximately 0.3" above the top of the fan/heatsink.

Figure 15 illustrates the thermal and physical space specifications for the Pentium OverDrive processor and the future Pentium OverDrive processor with MMX technology.

Physical space specifications for the future Pentium OverDrive processor with MMX technology are summarized as follows:

- 1.75" vertical clearance above the surface (opposite pin side) of Socket 7 when installed.
- 0.2" clearance around all four sides of the package.
- Space greater than specified above for end-user installation.

3.9.1. VOLTAGE REGULATOR THERMAL DESIGN CONSIDERATIONS

Voltage regulators are typically shipped with passive heatsinks for heat dissipation and may require adequate airflow. For a 45 to 50°C ambient temperature, voltage regulators typically call for an airflow of 200 LFM to ensure proper cooling. The airflow is parallel to the surface of the voltage regulator to ensure that the heatsink receives adequate airflow. Refer to your voltage regulator datasheet for actual specifications.

3.9.2. DESKTOP SYSTEM THERMAL DESIGN CONSIDERATIONS

To avoid localized heating at the processor, a clear air path and adequate venting is provided to prevent hot spots from occurring. A typical solution to this thermal problem is to add an auxiliary fan to the front vents of the chassis, directing airflow across the processor. While this solution would appear to be fairly simple, the addition of a second fan can actually cause the problem to intensify.

Unless the front vents are of sufficient size, and placement of the fan is carefully considered, the auxiliary fan can actually cause the air heated by the processor and other components to be re-circulated within the system rather than expelled out the back of the chassis. This heated air can easily raise the temperature around the processor beyond the temperature specifications for the components in the system.

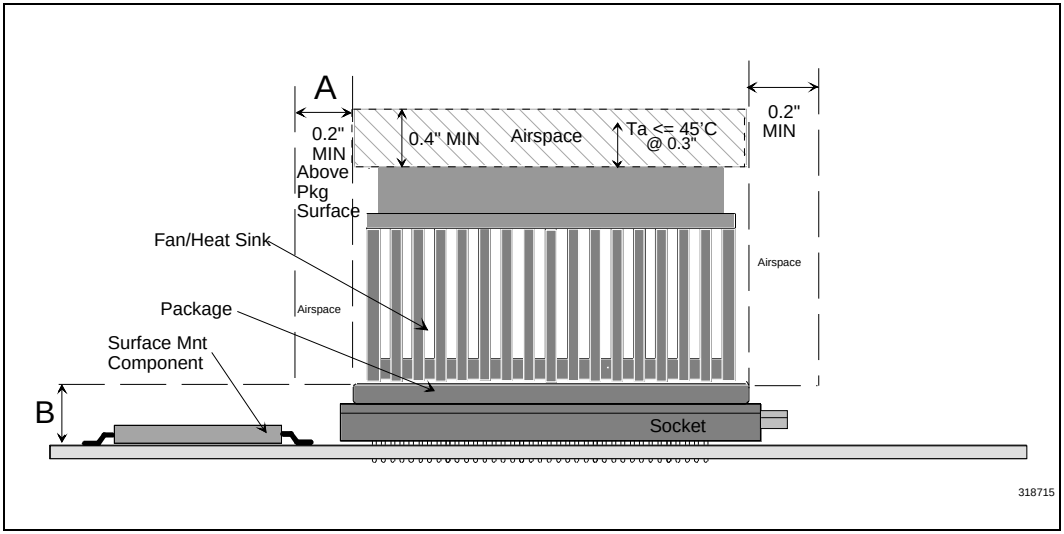


Figure 15. Thermal and Physical Space Requirements for the Pentium® OverDrive® Processor with MMX™ Technology

When adding an auxiliary fan to the system, the size of the chassis vents deserves special consideration. The fan is most effective when all of the air pushed through the fan blades comes from outside the chassis. If the vents are too small or inadequate for the fan velocity, gaps between the fan and chassis will cause air from inside the system to be drawn through the fan, causing re-circulation of heated air. The position of the fan is also critical. The highest air flow is from the blades and not from the center of the fan. Care should be taken not to block the blades with frame supports.

For details on Baby AT style chassis design suggestions, refer to the application note, *Pentium® Processor Chassis Design Suggestions* available on CD-ROM (See Appendix E).

3.10. BIOS/Software Considerations

As the flexible motherboard can accommodate a variety of processors, the BIOS is designed such that it can support all the different processors on the flexible motherboard. The BIOS code should use the CPUID instruction to identify the processor's CPUID signature (see Section 2.3.).

Other considerations for BIOS/software on the flexible motherboard include the following:

- **Processor test code should be independent of model specific registers (MSR). Various processors have different caches, test registers, and core architecture; e.g. the Pentium processor with MMX technology's cache size and associativity is different from the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200 resulting in differences in cache test registers.**
- **Since processors of various core frequencies are supported on the flexible motherboard, BIOS code should not contain any software timing loops and should be independent of the prefetch algorithm.**

3.11. Dual Processor Design Considerations

The Pentium processor family flexible motherboard may also be designed as one planar board to support uni-processor (UP) and dual-processor (DP) modes. This provides the flexibility of using the same motherboard populated with either one socket (for UP system) or two sockets (for DP system.) Figure 16 shows the layout for a split plane flexible motherboard designed with two sockets.

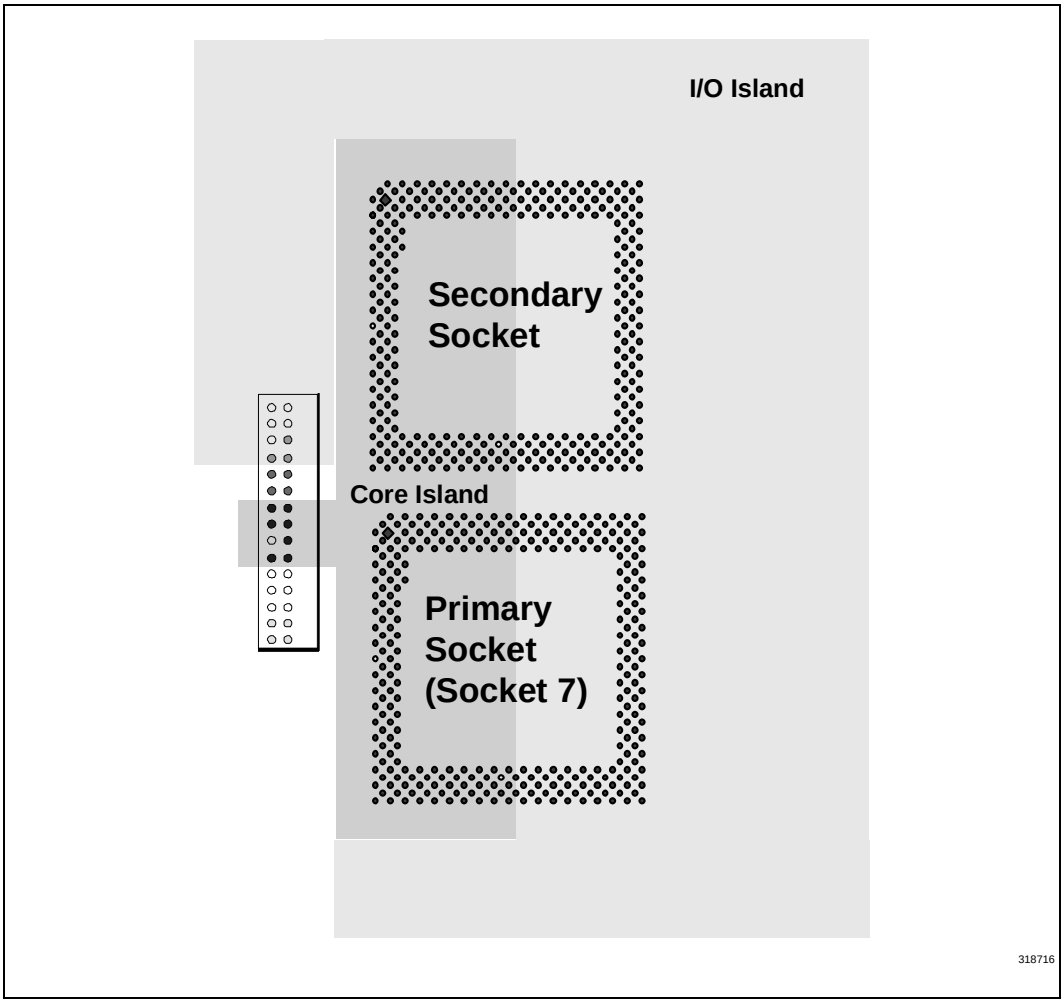


Figure 16. Layout of a DP Flexible Motherboard

The following needs to be considered when designing a split plane flexible motherboard with two sockets:

- **The power islands should be laid out such that the processor cores share one common island and the I/O share another island. This minimizes the number of islands resulting in better signal quality and reduced EMI effects.**
- **Socket 7 should only be used at the primary socket location. The secondary socket footprint should not be designed with the Socket 7 footprint.**

NOTE

Pentium OverDrive processors and future Pentium OverDrive processor with MMX technology do not support dual processor operation. The 296-pin LIF or ZIF socket should be used at the secondary socket location.

- **The primary socket location should always be populated. The nets should be balanced for**

worst case timing when the primary processor is driving the bus.

- **A single on-board voltage regulator (or VRM) should be used to support one or two processor cores. The on-board voltage regulator is located close to the processor such that the resistance and inductance is minimized.**
- **The recommended decoupling capacitors (Section 3.3.) should be used for each processor location to ensure that the voltage for each processor stays within specified limits during normal and transient conditions.**
- **The on-board voltage regulator (or VRM) needs to provide sufficient current in DP mode to support two processors unified on a single motherboard power plane and other 3.3V I/O current requirements in the I/O voltage island. For a 200 MHz, split-plane, dual-voltage input, DP Pentium processor with the MMX technology system, this amounts to approximately 11.4A at 2.8V and approximately 3–4A at 3.3V of typical current requirement. This assumes 5.7A at 2.8V for each of the processors, 1A for each of the dedicated 512K cache, and approximately 1.0A for the chipset. Actual current requirements will vary based on the devices used. In particular, current requirements should be carefully analyzed if implementing 3.3V DRAM powered from the I/O voltage island.**

APPENDIX A

A1.0. VOLTAGE REGULATOR MODULE

The Voltage Regulator Module (VRM) offers flexibility in that it allows processors with different voltage and current requirements to be easily supported on the flexible motherboard. The VRM is a voltage converter with a pinout capable of converting a system power supply voltage to the voltage necessary for the processor core. The only difference between the VRM and a voltage regulator on the motherboard is the pinout and ease in changing the processor supply voltage after assembly. By following a common pinout specification, a variety of VRMs may be developed by the OEM and third party vendors to support the Pentium processor family.

Figure 17 shows how the Voltage Regulator Module allows processors with different voltage and current requirements to be supported on the flexible motherboard using interchangeable VRMs.

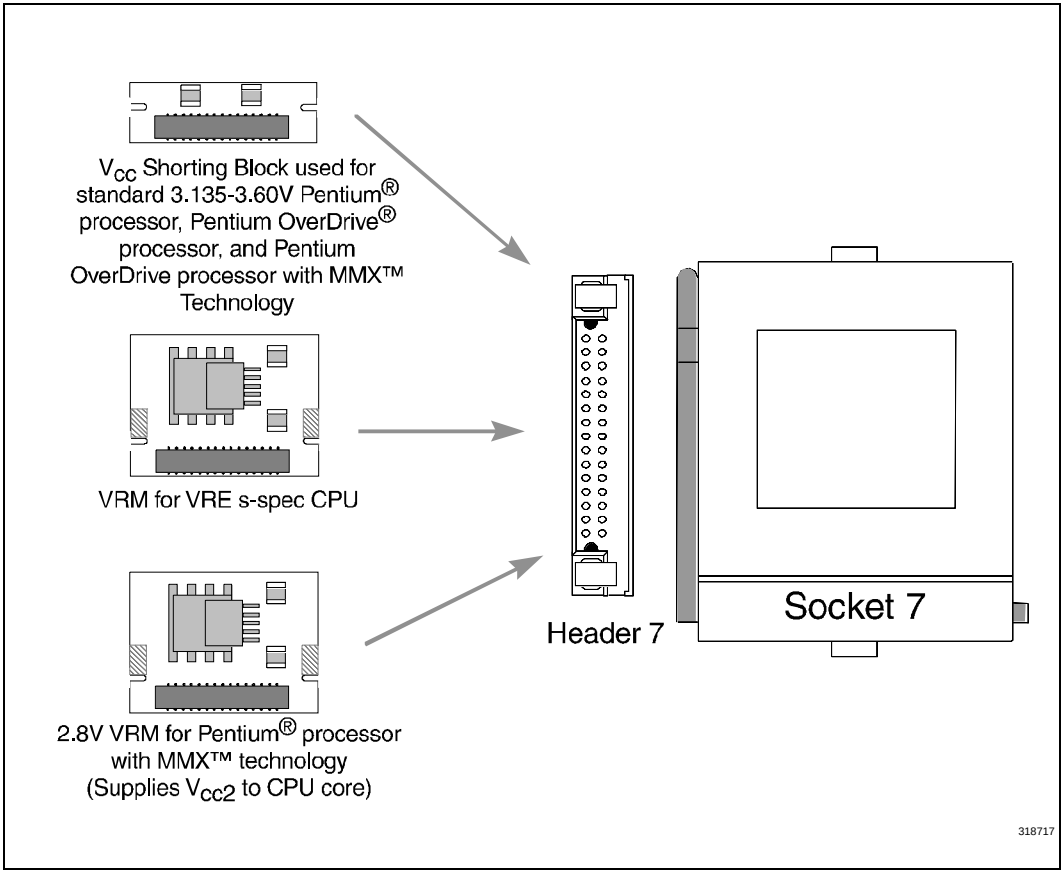


Figure 17. Voltage Regulator Modules

When the processor socket is populated with either the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the Pentium OverDrive processor, the Pentium processor with MMX technology or the future Pentium OverDrive processor with MMX technology, an OEM shorting block (pass-through module) can be installed in the VRM socket which allows 3.3V from the power supply (or on-board 3.3V regulator) to pass through to the processor core and I/O voltage islands.

When the processor socket is populated with a Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, a Pentium OverDrive processor, or a future Pentium OverDrive processor with MMX technology running on VRE voltage, a VRM designed for the specific operating voltage is used to supply the proper voltage to the core and I/O voltage islands.

NOTE

The VRM in this case needs to supply sufficient current to support higher frequency upgrade processors (Pentium OverDrive processor or future Pentium OverDrive processor with MMX technology) when installed.

When the processor socket is populated with the Pentium processor with MMX technology, a 2.8V VRM is installed in the VRM socket to supply 2.8V to the processor core's V_{CC2} pins. The 3.3V supplied to the processor I/O is not provided by the VRM in this case. The VRM only supplies 2.8V to the core V_{CC2} pins. The Pentium processor with MMX technology VRM, however, will have provisions to allow 3.3V from the power supply to pass through to the processor I/O voltage island.

Table 6 summarizes the *typical* processor voltage supply configuration with the VRM.

A1.1. Header 7

The VRM header (Header 7) is a 30-pin shrouded header with retaining clips. The retaining clips in the header hold the VRM in place when installed properly. The pins are set as 2 x 15 matrix. The power pins are capable of carrying up to 2A each.

The definition of Header 7 connections include: eight input voltage pins (four pins for +3.3V input, four pins for +5V input); ten output voltage pins (seven V_{CORE} pins that supply voltage to the processor core and three $V_{I/O}$ pins that connect to the voltage island supplying the processor V_{CC3} pins); three control signal pins (Disable input, Power Good output, Sense input); seven V_{SS} pins (Ground reference); one +12V pin (+12V or NC); and one RES pin (reserved for future use). Refer to the end of Appendix A for the VRM pinout and quick pin reference.

The 5V input pins on Header 7 are intended for regulation to 3.3V or 2.8V or any other voltage necessary for the processor. The 3.3V inputs can also be used for regulation (e.g. 2.8V) or as a source to connect to the processor 3.3V I/O plane through the $V_{I/O}$ pins. The +12V reference is used on some of the VRM's targeting VRE specifications. It is recommended to route +12V to this pin.

Table 6. Typical Processor Voltage Supply Configuration with VRM

	Core V_{CC}	I/O V_{CC}
Pentium® processor STD voltage (3.135V – 3.60V)	Shorting Block	Same as Core V_{CC} (1)
VRE (3.40V – 3.60V)	3.40V to 3.60V VRM (2)	Same as Core V_{CC}
Pentium processor with MMX™ technology	2.8V VRM	3.3V Power Supply or on-board 3.3V regulator
Pentium OverDrive® processor and future Pentium OverDrive processor with MMX technology	Shorting Block	Same as Core V_{CC}

NOTES:

1. Core and I/O voltages are supplied by the 3.3V power supply or an on-board 3.3V voltage regulator through the VRM header.
2. 3.40V to 3.60V VRM supplies voltage to the processor core, I/O and other 3.3V components on the motherboard that interface with the processor. The VRM is able to supply enough current (7A typical) to the processor, 3.3V cache and chipset in the processor I/O voltage island.

The primary output of the VRM is through the V_{CORE} pins. These pins supply the voltage necessary for the processor core. The $V_{I/O}$ output pins are connected to the processor power plane supplying the processor V_{CC3} pins. These $V_{I/O}$ pins are connected to the V_{CORE} pins on VRMs that need to power both the processor core and I/O from a single source (e.g. VRE VRMs.)

The control signals DISABLE and PWRGOOD on the VRM header are optional control signals provided for system use. It is up to the discretion of the OEM to decide whether to implement circuitry to use these features. The SENSE input, however, allows voltage regulators on the modules to adjust their output voltage to correct for a voltage drop through the connectors and power plane. SENSE should be routed to a point in the center of the processor core voltage island. The sense line can make contact to the power plane through a via supporting one of the decoupling capacitors.

If the flexible motherboard is designed with a VRM header, the +3.3V inputs on the VRM header are connected directly to the $V_{I/O}$ pins through the module (Pentium processor with MMX technology VRM) to supply the processor I/O voltage island. In the case where a VRE VRM is used, the module connects the V_{CORE} output pins to the $V_{I/O}$ pins to allow both islands to obtain the same voltage. The best solution for connecting the output of the 3.3V or VRE supply to both the voltage planes, when a unified plane processor is used, is through the VRM header. A shorting block in the VRM header to connect the 3.3V supply inputs on the VRM to the V_{CORE} and $V_{I/O}$ outputs will provide the best electrical performance.

A1.2. Shorting Block or Pass-Through Module

The shorting block or Pass-Through Module is nothing more than a connector which shorts the 3.3V input pins to the V_{CORE} and $V_{I/O}$ pins on the VRM header. This is used with the Pentium processor 75 / 90 / 100 / 120 / 133 / 150 / 166 / 200, the Pentium OverDrive processor, and the future Pentium OverDrive processor with MMX technology. The shorting block allows voltage from the 3.3V power supply or on-board 3.3V voltage regulator to pass through to the processor core and I/O voltage islands.

A1.3. VRM for Processors Running at VRE

The Voltage Regulator Module concept allows VRE (3.40V to 3.60V) processors to be easily supported on the flexible motherboard. A VRM designed for the VRE voltage range is used in Header 7 to supply the VRE processors. The VRM in this case supplies voltage to the processor core, I/O and other 3.3V components on the motherboard that interface with the processor. The VRM provides adequate current for all these components.

A1.4. VRM for Pentium® Processor with MMX™ Technology

The VRM for the Pentium processor with MMX technology supplies 5.7A at 2.8V (200 MHz) for the processor core. The VRM will regulate down to 2.8V from either 5V or 3.3V. The 3.3V supplied to the processor I/O will come from the 3.3V system power supply or on-board 3.3V regulator. The Pentium processor with MMX technology VRM will have the +3.3V inputs shunted to the $V_{I/O}$ outputs to allow 3.3V inputs to the VRM header to pass through to the 3.3V processor I/O voltage island.

NOTE

The Voltage Regulator Module for 2.8V processors will not generate the 3.3 volts for the processor I/O supply. This is necessary due to space constraints of the module and the potential power limitations for 3.3V components. The modules for 2.8V processors can connect the $V_{I/O}$ pins to the 3.3V input for ease of implementation. The system provides adequate current for the 3.3V components on the $V_{I/O}$ plane.

A1.5. VRM Header Placement

The VRM header should be located close to the processor socket. This is to prevent an excessive voltage drop across the power plane and allow the header to be easily located. It is recommended that the VRM header be located no further than 1 inch from the processor socket.

NOTE

The VRM specifications allow for a maximum of 7 mOhms resistance and a maximum of 3.4 nH inductance from VRM to processor V_{CC2} pins.

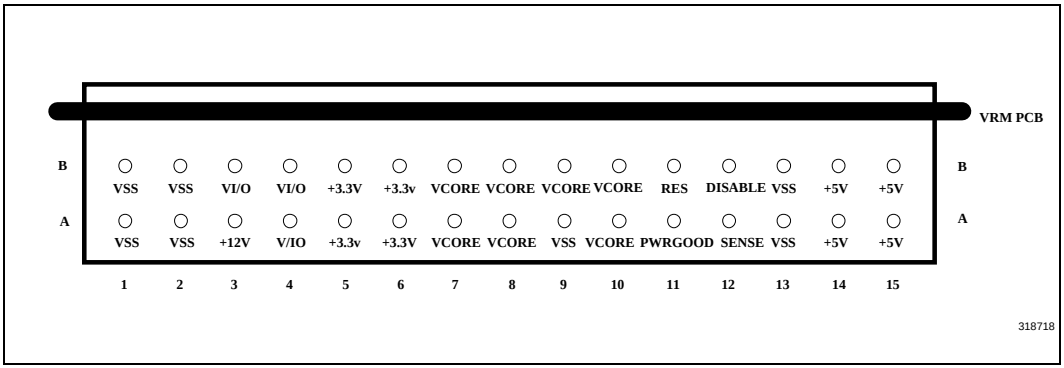
The VRM header should be placed such that it provides easy routing of the core and I/O voltage islands from processor to VRM. The header may be located on the handle side of Socket 7 or any of the

two sides that are closest to the handle side. Placing the header on the side that is opposite to the handle side is not recommended as it increases the distance from VRM to the processor, thereby increasing the voltage drop across the power plane. It also makes routing to the core island more difficult. If the VRM header is placed on the handle side of Socket 7, it should be located no closer than 0.5 inch to the ZIF handle. This clearance allows easy access to the socket handle.

Location of the VRM header with respect to the processor socket should also take into consideration the following:

- The distance from motherboard surface to VRM component overhang should be kept at a minimum vertical distance of 0.55".
- Ease of routing the 3.3V voltage island from the 3.3V power supply to the +3.3V inputs on the VRM header.
- The VRM does not impede the installation of full size add-in cards in the I/O slots.
- The VRM is located such that it receives adequate airflow to ensure proper cooling. The airflow is parallel to the surface of the VRM to ensure that the heatsink on the VRM receives adequate airflow.
- Use of logic analyzer probes — The VRM header is placed such that is does not impede the installation of probes into the processor socket.

A2.0. VOLTAGE REGULATOR MODULE HEADER PIN DIAGRAM



VRM Pinout Top Side View

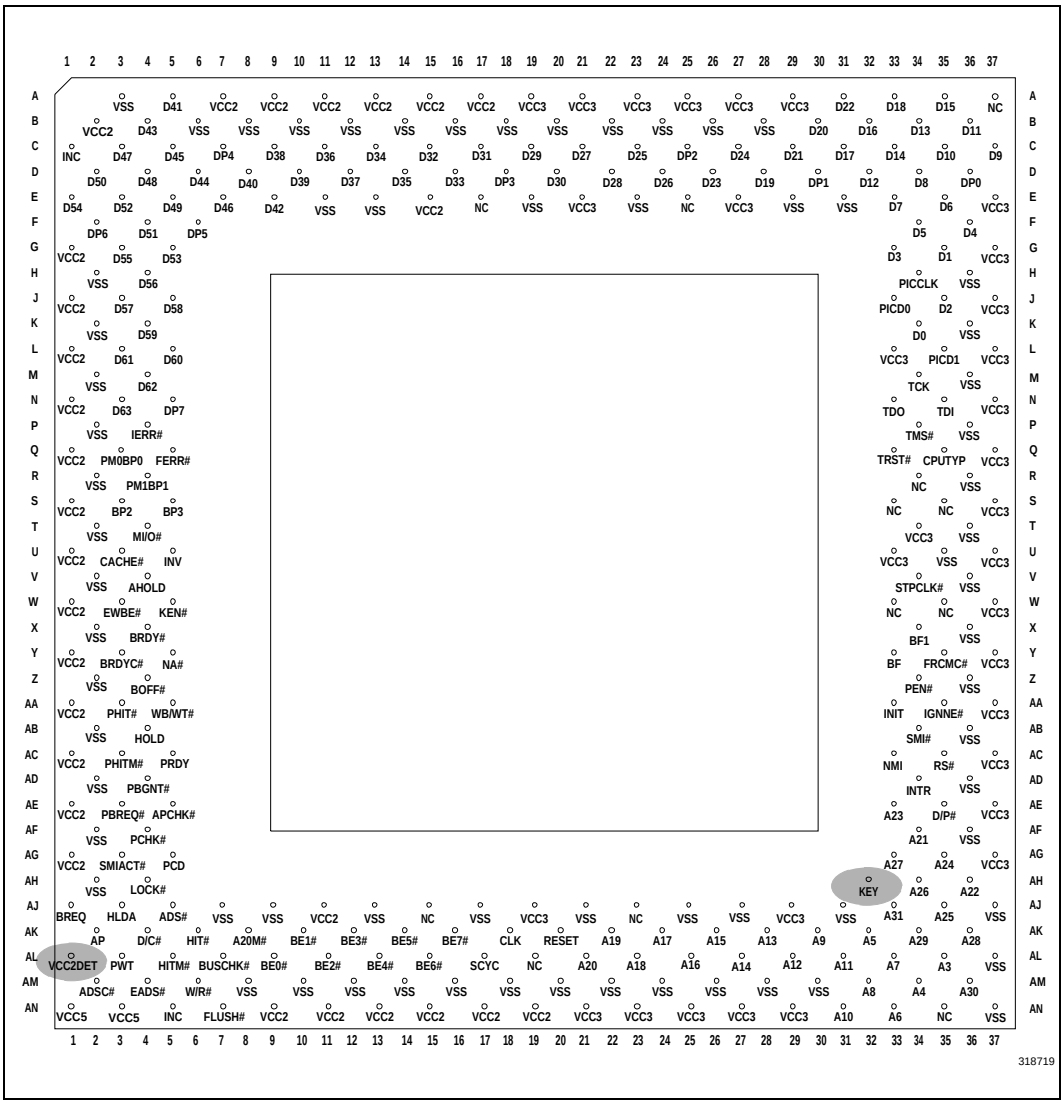
A3.0. VOLTAGE REGULATOR MODULE QUICK PIN REFERENCE

The pin definitions of the Voltage Regulator Module socket are as follows.

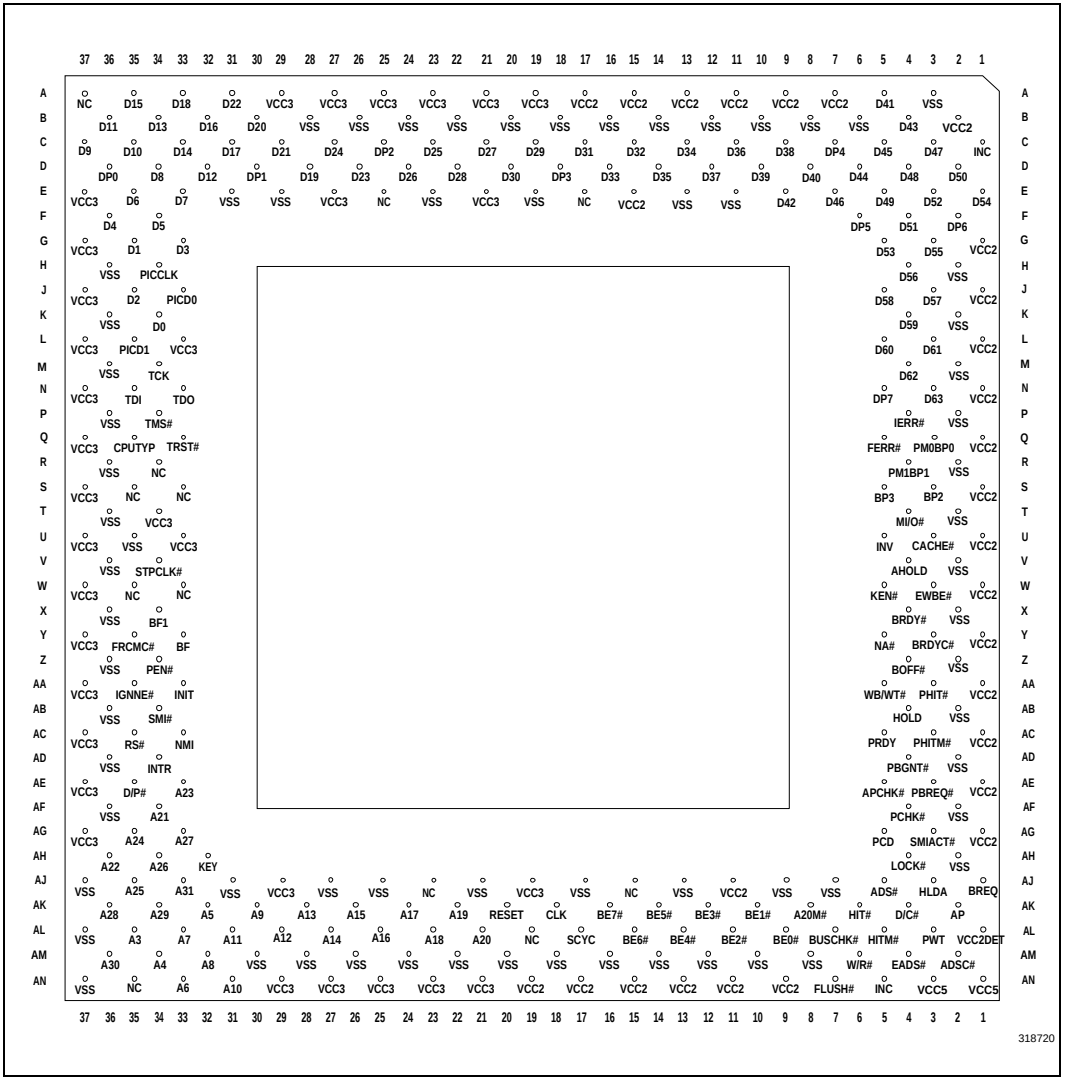
Pin Name	Type	Function
+3.3V	Input	+3.3V Supply, may be used for OEM processor regulation supply, a control signal pull-up or as a supply to the $V_{I/O}$ plane. The +3.3V input is connect to the $V_{I/O}$ output on the Pentium® OverDrive® processor with MMX™ technology module.
+5V	Input	+5V Supply may be used for Pentium processor family regulation to 3.3V/VRE
+12V	Input	+12V Reference Supply, may be necessary for some Voltage Regulator Modules targeting VRE specifications.
DISABLE	Input	When driven high, this input will disable the Voltage Regulator Module output and the output of the module will float.
PWRGOOD	Output	Power Good is an open collector output driven low when the VRM output is not within valid levels.
SENSE	Input	Sense is provided for the regulator to correct for voltage drops across the connector and motherboard power plane. This signal should be connected to the center of the V_{CORE} plane.
RES	N/A	RESERVED
V_{CORE}	Output	Voltage Regulator Module Output.
$V_{I/O}$	Output	Processor I/O power connection. Allows for VRM to specify I/O voltage.
V_{SS}	Input	Ground Reference.

APPENDIX B

B1.0. SOCKET 7 PIN DIAGRAM



Socket 7 Pinout—Top Side View



Socket 7 Pinout—Pin Side View

B2.0. SOCKET 7 QUICK PIN REFERENCE

Socket 7 has the same pin definition as Socket 5 with the exception of the following pins.

Symbol	Type	Name and Function
CLK, PICCLK	(I)	Unlike some Pentium® processors, the **Clock and Programmable Interrupt Controller Clock** inputs to Socket 7 are **not** 5V tolerant. These inputs are driven by an appropriate 3.3V clock driver.
KEY	NA	The KEY pin is strictly a mechanical keying device for future Pentium OverDrive® processors. The hole in the socket permits installation of the higher speed Pentium OverDrive processors. The corresponding pin on the Pentium OverDrive processors is an Internal No Connect and has no electrical purpose. This pin is not populated on 320-pin packages.
VCC2DET#	(O)	**V_{CC2} Detect** is defined for the Pentium processor with MMX™ technology which uses a supply of 2.8 volts on the V_{CC2} pins. The Pentium processor with MMX technology with a core voltage of 2.8 volts, will always drive V_{CC2DET} low. This pin may be used to select the proper core voltage from a voltage regulator or system supply. This pin is not driven high on 3.3 volt Pentium processors or Pentium OverDrive processors. The VCC2DET# system trace has a pull-up for proper use.
V_{CC2}	(I)	Socket 7 has 28 power supply pins defined for the core voltage on processors with separate power inputs. For processors with a single power supply requirement, these pins can be considered the same as V_{CC3} pins and should be driven with the same power source.
V_{CC3}	(I)	Socket 7 has 32 power supply pins defined for the I/O voltage on processors with separate power inputs. For processors with a single supply requirement, these pins are used in conjunction with the V_{CC2} pins to power the device.

APPENDIX C

C1.0. LINEAR AND SWITCHING REGULATOR SOLUTIONS

Appendix C contains a list of Linear/Switching Voltage Regulator solutions. These lists may not be all inclusive or accurate of all vendor solutions, but they are intended as a voltage regulator reference lists for known 2.8V/3.3V/VRE regulator solutions. Please contact your vendor for their latest product specifications.

2.8V/3.3V/VRE Linear Regulator Solutions

Vendor	Part Number	Electrical				Remote Sense	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Power (Max) (W)			Sample	Product
Cherry	CS5206	5	2.8	6	17	No	TO-220/ D^2Pak	Now	Now
		5	3.3/ VRE	6	20				
	CS5207A	5	2.8	7	20	Yes	TO-220	Q4'96	Q4'96
		5	3.3/ VRE	7	23				
Linear Tech	LT1575 (+ ext FET)	3.3	2.8	10	5	Yes	8-pin SOIC	Now	Now
		5	2.8	10	22				
		5	3.3/VRE	10	27				
	LT1577 (Dual)	5	2.8	10	22	Yes	16-pin SOIC	Now	Now
		5	3.3/VRE	10	27				
	LT1580	5	2.8	7	15.4	Yes	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	LT1584	5	2.8	7	15.4	No	TO-220/ TO-263	Now	Now
		5	3.3/VRE	7	11.9				
	LT1585A	5	3.3	5	8.5	No	TO-220/ TO-263	Now	Now
Linfinity	LX8384	5	3.3/VRE	5	8.5	No	TO-220/ TO-263	Now	Now
	LX8585	5	3.3/VRE	4.6	7.82	No	TO-220/ TO-263	Now	Now
	LX8586	5	2.8	6	13.2	No	TO-220/ TO-247	Now	Now
		5	3.3/VRE	6	10.2				

2.8V/3.3V/VRE Linear Regulator Solutions (Contd)

Vendor	Part Number	Electrical				Remote Sense	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Power (Max) (W)			Sample	Product
National	LM2951	5	2.8	7	15.4	No	SO-8	Now	Now
		5	3.3/VRE	7	11.9				
	LM3411	5	3.3/VRE	7	11.9	No	SO-8/ 5-pin SOT 23	Now	Now
Raytheon	RC5102 (Dual)	5	2.8	7	15.4	Yes	8-pin SOIC	Now	Now
		5	3.3/VRE	7	11.9				
Semtech	EZ1083/A	5	2.8	7.5	16.5	No	TO-220 or	Now	Now
		5	3.3/VRE	7.5	12.75		TO-247		
	EZ1082	5	2.8	10	22.0	No	TO-220 or	Now	Now
		5	3.3/VRE	10	17		TO-247		
	EZ1584A	5	2.8	7	15.4	No	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1900	5	2.8	7	15.4	No	8-pin SOIC	Now	Now
	(Dual)	5	3.3/VRE	7	11.9				
	EZ1580	5	2.8	7	15.4	Yes	5-pin TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1585D	5	2.8	6	13.2	No	TO-220	Now	Now
		5	3.3/VRE	6	10.2				
Unisem	US1080	5	2.8	8	17.6	No	TO-220/ TO-263	Q1'97	Q1'97
		5	3.3/VRE	8	13.6				

2.8V/3.3V/VRE Switching Regulator Solutions

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
Cherry	CS5120	5	2.8	5.7	92%	2	14-pin PDIP	Now	Now
		5	3.3/VRE	5.7	92%		14-pin SOIC		
Harris	HIP5010	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5011	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5010	5	2.8	6	89%	2	7-pin TO-220 or	Now	Now
		5	3.3/VRE	6	92%		7-pin D^2Pak		
	HIP5016	5	2.8	6	89%	2	7-pin TO-220 or	Now	Now
		5	3.3/VRE	6	92%		7-pin D^2Pak		
Linear Tech	LTC1266	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
	LTC1430	5	2.8	15	93%	2	16-pin SOIC or	Now	Now
		5	3.3	15	95%		8-pin SOIC		
	LTC1435	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
Linfinity	LX1660/1	5	2.8	12	85%	2	SO-16	Q4'96	Q4'96
		5	3.3/VRE	12	85%				
Maxim	MAX797	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				
	MAX798	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				

2.8V/3.3V/VRE Switching Regulator Solutions (Cond)

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
National	LM3578 & LM3411	5	3.3/VRE	10	88%	1	SO-8 or 5-pin SOT23	Now	Now
Raytheon	RC5036 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5031	5	2.8	10	87%	1	14-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5035 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
Siliconix	Si9140	5	2.8	6	90%	2	16-pin SOIC	Now	Now
		5	3.3	6	90.5%				
	Si9145	5	2.8	6	82%	1	16-pin SOIC or 16-pin TSSOP	Now	Now
		5	3.3/VRE	6	83%				
Unitrode	UC3886	5	2.8	10	85%	1	16-pin SOIC or 16-pin DIP	Now	Now
		5	3.3/VRE	10	85%				
	UCC3881	5	2.8	10	85%	1	16-pin SOIC or 16-pin DIP	Now	Q1‘97
		5	3.3/VRE	10	85%				
	UCC3880	5	2.8	10	85%	1	20-pin SOIC or 20-pin DIP	Now	Now
		5	3.3/VRE	10	85%				
	UC3874	5	2.8	10	90%	2	18-pin SOIC or 18-pin DIP	Now	Now
		5	3.3/VRE	10	90%				
Unisem	US2050	5	2.8	10	85%	1	7-pin TO-220 or TO-263	Q1’97	
		5	3.3/VRE	10	85%				

APPENDIX D

D1.0. REGULATOR VENDOR SOLUTIONS CONTACT LIST

On-board Regulators

Vendor	North America	Europe	Asia	Japan
Cherry	Dennis Gatano Tel: (401) 886-3305 Fax: (401) 885-5786			
Harris	Dean Henderson Tel: (919) 405-3603 Fax: (919) 405-3651	Robert Lahaye Tel: (33) 1 346 54046 Fax: (33) 1 394-64054	Jason Lin Tel: (886) 2 716 9310 Fax: (886) 2 715 3029	Masaru Agano Tel: (81) 3 3265 7571 Fax: (81) 3 3265 7575
Linear Tech	Bob Scott Tel: (408) 432-1900 Fax: (408) 434-0507	Fred Killinger Tel: (49) 89 9642550 Fax: (49) 89 963147	Dave Quarrels Tel: (65) 753 2692 Fax: (65) 754 4112	
Linfinity	Andrew Stewart Tel: (714) 898-8121 Fax: (714) 893-2570			
Maxim	David Timm Tel: (408) 737-7600 Fax: (408) 737-7194	David Watson Tel: (44) 17 3430 3388 Fax: (44) 17 3430 5511	Steve Huang Tel: (886) 2558 6801 Fax: (886) 2555 6348	Tadi Kodairo Tel: (81) 3 3232 6141 Fax: (81) 3 3232 6149
National	Venkatesh Shan Tel: (408) 721-3753 Fax: (408) 721-8763	Werner Obermaier Tel: (49) 81 4135 1331 Fax: (49) 81 4135 1220	Vincent Lin Tel: (852) 2737 1616 Fax: (852) 2736 9931	Mark Kachmerak Tel: (81) 43 299 2373
Raytheon	David McIntyre Tel: (415) 9667734 Fax: (415) 966-7742	David Frye Tel: (44) 17 0566 5555 Fax: (44) 17 0566 3355	Mike Wisnia Tel: (81) 3 3406 5998 Fax: (81) 3 3406 5998	
Semtech	Gene Krzwinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Siliconix	Erik Ogren Tel: 408-970-5543 Fax: 408-567-8910	Sean Montgomery Tel: (44) 344 485757 Fax: (44) 344 427371	Serge Jaunay Tel: (852) 2378 9715 Fax: (852) 2375 5733	Tony Grizelj Tel: (81) 3 5562 3321 Fax: (81) 3 5562 3316
Unitrode	John O'Connor Tel: (603) 429-8504 Fax: (603) 429-8963	David Wells Tel: (44) 181 318 1431 Fax: (44) 181 318 2549	Wilkie Wong Tel: 8522-722-1101 Fax: 8522-369-7596	
Unisem	Reza Amirani Tel: (714) 453-1008 Fax: (714) 453-8748			

Voltage Regulator Modules

Vendor	North America	Europe	APAC	Japan
Ambit	Leonard Kao Tel: (886) 35-7849575 Fax: (886) 35-782924			
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 1753-67-6800 Fax: (44) 1753-67-6801	Joe Navin Tel: (81) 44-813-8507 Fax: (81) 44-813-8500	
C-MAC	Dave Holmes Tel: (407) 881-2321 Fax: (407) 881-2342			
Corsair	John Beckley Tel: (408) 559-1777 Fax: (408) 559-4294			
Semtech	Gene Krzywinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Raytheon	David McIntyre Tel: (415) 966-7734 Fax: (415) 966-7742	David Frye Tel: 44 17 0566 5555 Fax: 44 17 0566 3355	Mike Wisnia Tel: 81 3 3406 5998 Fax: 81 3 3406 5998	
VXI	Joseph Chang Tel: (503) 652-7300 Fax: (503) 786-5011			

Socket 7

Vendor	North America	Europe	APAC	Japan
Amp	Bob Branden Tel: (910) 855-2247 Fax: (910) 855-2224	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Appros	Hiroshi Narita Tel: (81) 45-941-4080			
Augat	David M. Barnum Tel: (508) 699-9890 Fax: (508) 695-8111	Arif Shahab Tel: (44) 952-670-281 Fax: (44) 952-670-342	Atsushi Sasaki Tel: (81) 44-853-5400 Fax: (81) 44-853-1113	
Foxconn	Julia Jang Tel: (408) 749-1228 Fax: (408) 749-1266		Wesley Lin or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Yamaichi	Ann Sheperd Tel: (408) 456-0797 Fax: (408) 456-0779	Mr. Matsuda Tel: (49) 89-451021-43 Fax: (49) 89-451021-10	Alan Liu Tel: (886) 02-546-0507 Fax: (886) 02-546-0509	Mr. Shiwaku Tel: (81) 3-3778-6161 Fax: (81) 3-3778-6181
Berg/ McKenie	Fred Baldwin Tel: (510) 651-2700 Fax: (510) 651-1020			

Header 7

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Wesley Lin or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	

Decoupling Capacitors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1µF, X7S	Dennis Lienemann Tel: (803) 946-0616	Steve Chan (Singapore) Tel: (65) 258-2833 Fax: (65) 258-8221
	TPSD107K010R0100	100µF, Tantalum	Fax: (803) 946-6678	K.J. Kim (Korea) Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
Johanson Dielectrics	160R18W105K4	1µF, X7R	Dave Lopez Tel: (818) 364-9800 Fax: (818) 364-6100 NCTR (California only) Tel: (510) 624-8900 Fax: (510) 624-8905	Bill Yu (Taiwan) Nanco Electronics Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Sales Dept (Hong Kong) Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100µF, Tantalum	Richey-Cypress Elect. Tel: (408) 654-9100 Fax: (408) 566-0160	Warren Marshall Tel: (800) 421-7258 Fax: (714) 713-0129
Murata Electronics	GRM40X7R105J016	1µF, X7R	Sales Department Tel: (770) 436-1300 Fax: (770) 436-3030	Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721 Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (847) 803-6100 Fax: (847) 803-6296	Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090 Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108

Shorting Blocks

Vendor	North America	Europe	APAC	Japan
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	H. Itoh Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Foxconn	Julia Jang or Paul Fitting Tel: (408) 749-1228 Fax: (408) 749-1266		Wesley Lin or Ivan Liaw Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Molex	Micheal Gits Tel: (408) 946-4700 Fax: (408) 946-5386	(Molex) Tel: (49) 89-413092-0 Fax: (49) 89-401527	(Molex) Tel: (65) 268-6868 Fax: (65) 265-6044	(Molex) Tel: (81) 427-21-5539 Fax: (81) 427-21-5562

Resistors

Vendor	Size	Type	Accuracy/ Value	Contact
Thin Film Technology	1208	thin	0.1%, 100-250KΩ 0.5%, 10-250KΩ	(507) 625-8445 Region Sales Mgrs
	0805	thin	0.1%, 100-100KΩ 0.5%, 10-1MΩ	Patrick Lyons x14 W. of Mississippi (except TX & S. Cal)
	0803	thin	0.1%, 100-33KΩ 0.5%, 10-330KΩ	Mark Porisch x12 Southern US, E. of Mississippi (inc. TX)
	0402	thin	0.5%, 10-100KΩ	Tim Goertzen x13 Northern U.S., E. of Mississippi & Canada Mike Smith (310) 768-8923 Southern California
Dale Electronics	0603	thin	0.5%, 10-100KΩ	Gary Bruns (402) 371-0080
		thick	1%,2%, 10-1MΩ	
	805	thin	0.1%, 100-100KΩ	
Koa Spear	805	thin	0.1%, 100-100KΩ	T. Yogi (814) 362-5536
		thick	0.5-5%, 10-1MΩ	
Beckman Industrial	0805	thin	0.1%, 10K-100KΩ	Cathy Whittaker (214) 392-7616
		thick	1-5%, 10-1MW	
	0603	thick	1-5%, 10-1MW	

3.3V Clock Driver Suppliers

Supplier	Contact	Phone	Fax
ICS	Raju Shah	408-925-9493	408-925-9460
ICW	Angel Atondo	408-922-0202 ext 1131	408-922-0833
National Semiconductor	John Bergen	408-721-2990	408-732-6017
Cypress Semiconductor	John Wunner	206-821-9202 ext 325	206-820-8959
Texas Instruments	David Hoover	903-868-5694	903-868-5962
IDT	Mark Hermsen	408-492-8366	408-492-8362
AMCC	Mark Denzin	619-535-6526	619-450-9885
Motorola	Geraldine Stih	602-952-3046	602-952-3682
Triquint Semiconductor	George Sanders	503-644-3535	503-644-3198
IMI	Elie Ayache	408-263-6300	408-263-6571

APPENDIX E

E1.0. LIST OF RELATED TOOLS & COLLATERAL

E1.1. Public Documentation

These documents may be ordered from the Intel Literature Center by calling 800-548-4725 in the U.S. In other geographies please contact your local sales office.

Document Title	Order Number
Pentium® Processor Family Developer's Manual (3 Volume Set) - Volume 1: Pentium Processors (Databook) - Volume 2: 82496/82497/82498 Cache Controller and 82491/82492/82493 Cache SRAM (Databook - Volume 3: Architecture and Programming Manua	241563 241428 241429 241430
Pentium® Processor Datasheet (75 MHz, 90 MHz, 100 MHz, 120 MHz, 133 MHz, 150 MHz, 166 MHz and 200 MHz)	241997
Pentium® Processor Specification Update	242480
Pentium® Processor Family Product Briefs	241561
Pentium® Processor Performance Brief	241557
Pentium® Processor Technical Overview	241610
AP-479: Pentium® Processor Clock Design	241574
AP-480: Pentium® Processor Thermal Design Guidelines	241575
AP-485: Intel Processor Identification with the CPUID Instruction	241618
AP-577: An Introduction to PPGA Packaging	243103
AP-522: Implementation Guidelines for 3.3V Pentiun® Processors with VRE Specifications	242687
AP-578: Software and Hardware Considerations in Handling FPU Exceptions	242415
Pentium® Processor 3.3V Clock Driver Specifications	Contact your local Intel Sales Office or Distributor
Pentium® Processor 3.3V ASIC Interface Specification	Contact your local Intel Sales Office or Distributor
Pentium® Processor 3.3V Pipeline BSRAM Specification	Contact your local Intel Sales Office or Distributor

E1.2. Collateral Available Under Non-Disclosure Agreement

These documents may be obtained by contacting your local Intel sales office or distributor.

Product Information

Document Title	Notes ID/PDDC Document Number
Pentium® Processor Specification Update	FMKIHU
200 MHz P54CS-cC0 Stepping Information, Rev. 1.0	EW3Q1T
P55C BIOS Compatibility	CW1QGR
P55C External Design Specification (EDS), Rev. 3.1	SC-1294
P55C Platform Architecture Analysis, Rev. 3.0	SC-1263

System Design Documentation

Document Title	Notes ID/PDDC Document Number
Pentium® Processor Flexible Motherboard (FMB) Design Guidelines, Rev 2.0	RG4Y1L
P55C/FMB Design Review Checklist, Rev 3.0	MCLOOO
Socket 7 Specification, Rev. 3.0	FM-0632
Socket 7 Design Review Checklist, Rev. 2.0	PC89O9
Pentium® Processor Input Strapping Recommendations, Rev. 2.0	MCQ3OW
P55C Voltage Regulator Module Overview and Target Spec., Rev 4.0	FBKP54
Voltage Guidelines for Pentium® Processors with MMX™ Technology	KW1TFD

System Design Tools

Split-plane Platform Test Kit	Contact your local Intel Sales Office or Distributor

E2.0. REFERENCES

Clyde F. Coombs, Jr., *Printed Circuits Handbook*, McGraw Hill Publishing Co., New York, 1988

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