Never stop thinking

PROFET™+
PSpice Behavioral Model

Application Note

V1.0 2012-04-11

Automotive Power

Table of Contents

1 General Information

- These models are meant to be used with Cadence Capture CIS (Allegro Design Entry CIS ) as it will be explained in the following slides.
- The *.lib files are encrypted to protect the Infineon IP.
- The PROFET+ PSPICE Simulation models show the typical device behavior.
- It is not possible to use the PSPICE 9.1 student version or LTSPICE.
- The dynamic switching shutdown (Datasheet parameter P_6.6.8) is not implemented in the models BTSxxx.
- The models for 24V PROFET+ have the dynamic switching shutdown (Datasheet parameter P_6.6.8) implemented and provide additional pins to show the junction temperatures (TJx).
- For the thermal behavior (Zth/Rth-ja) the JEDEC 2s2p setup is considered.
- The Pin “TAMB” sets the ambient temperature for the device. Use a voltage source (VDC) to set it.
- To avoid convergence issues, use VPWL or VPULSE sources for INx and VS Pins.

2 How to use the PROFET+ Model

The following section gives a short guidance on how to include the PROFET+ models into the Cadence Environment.

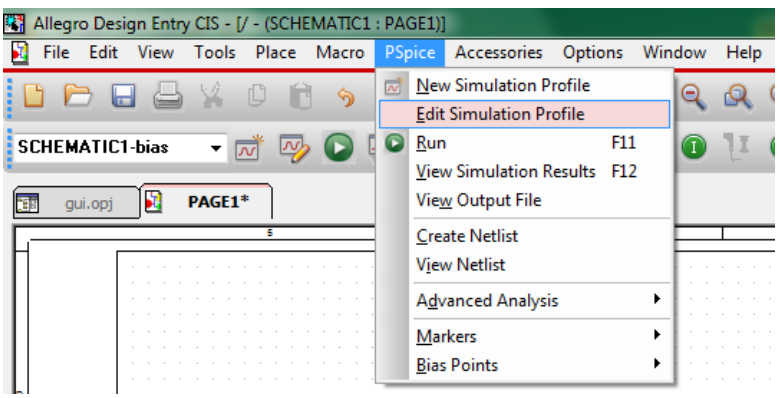
2.1 Files

- The delivery package (*.zip) contains important files that enable the use of the model in custom schematic test benches.
- *.lib: encrypted PSpice behavioral description
- *.olb: contains the symbol view for the graphical user interface “Capture” compatible with Allegro ver. 15 and newer
- *_16_2.olb: contains the symbol view for the graphical user interface “Capture” compatible with Allegro ver. 16.2 and newer
- *_16_3.olb: contains the symbol view compatible with Allegro ver. 16.3

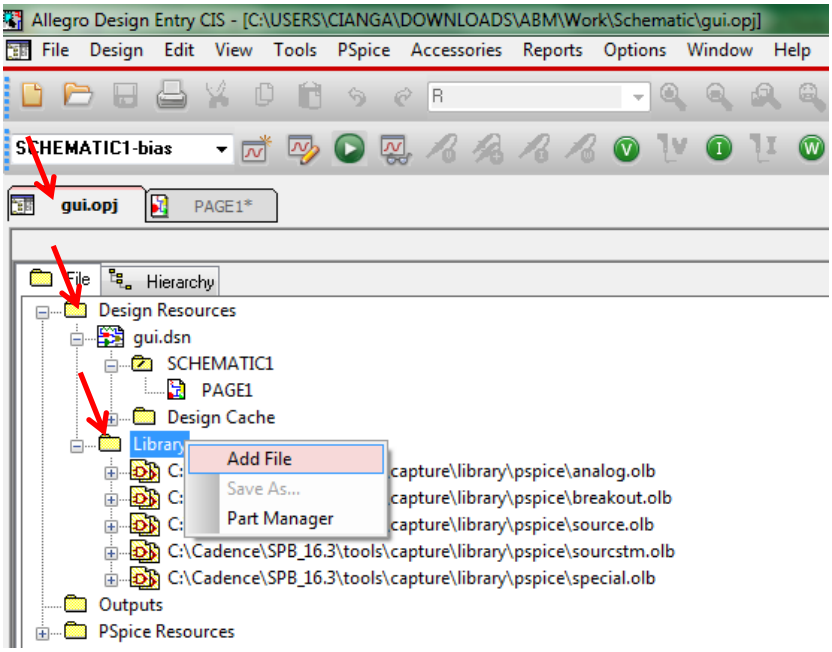
2.2 Graphical User Interface

Once you have opened Cadence OrCad Capture CIS and you have a custom test bench or wish to create one, in order to use the PSpice model the following steps are necessary:

1) from the *PSpice* menu choose *Edit simulation profile*:

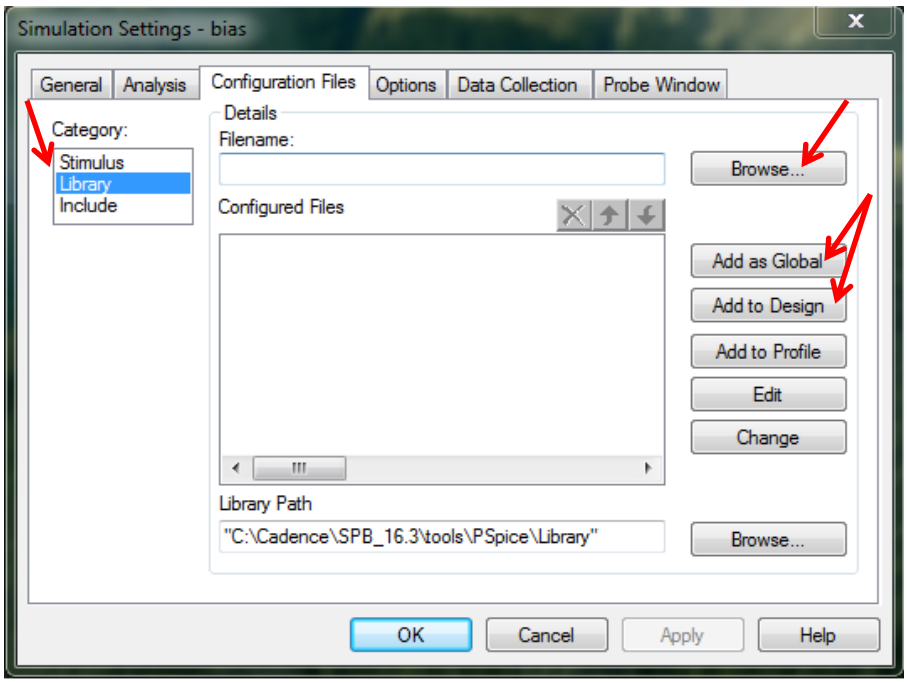


2) On the window menu that pops up go to the *Configuration files* tab and from the *Category* options choose *Library*. Under *Details*, at the *Filename* tag click *Browse* and select the model *.lib file (in this case ***.lib**) from the folder you have it stored.

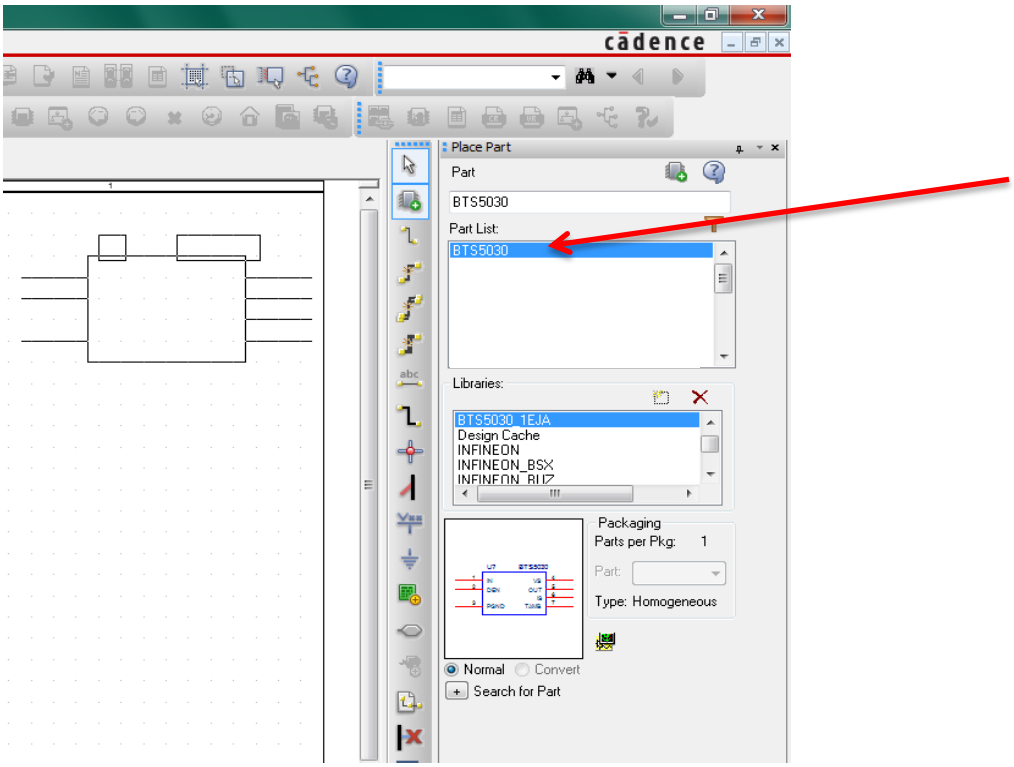


3) After validating the selection, you have to choose how you want the library to be available: as *Global* to all the designs or just for the current *Design*.

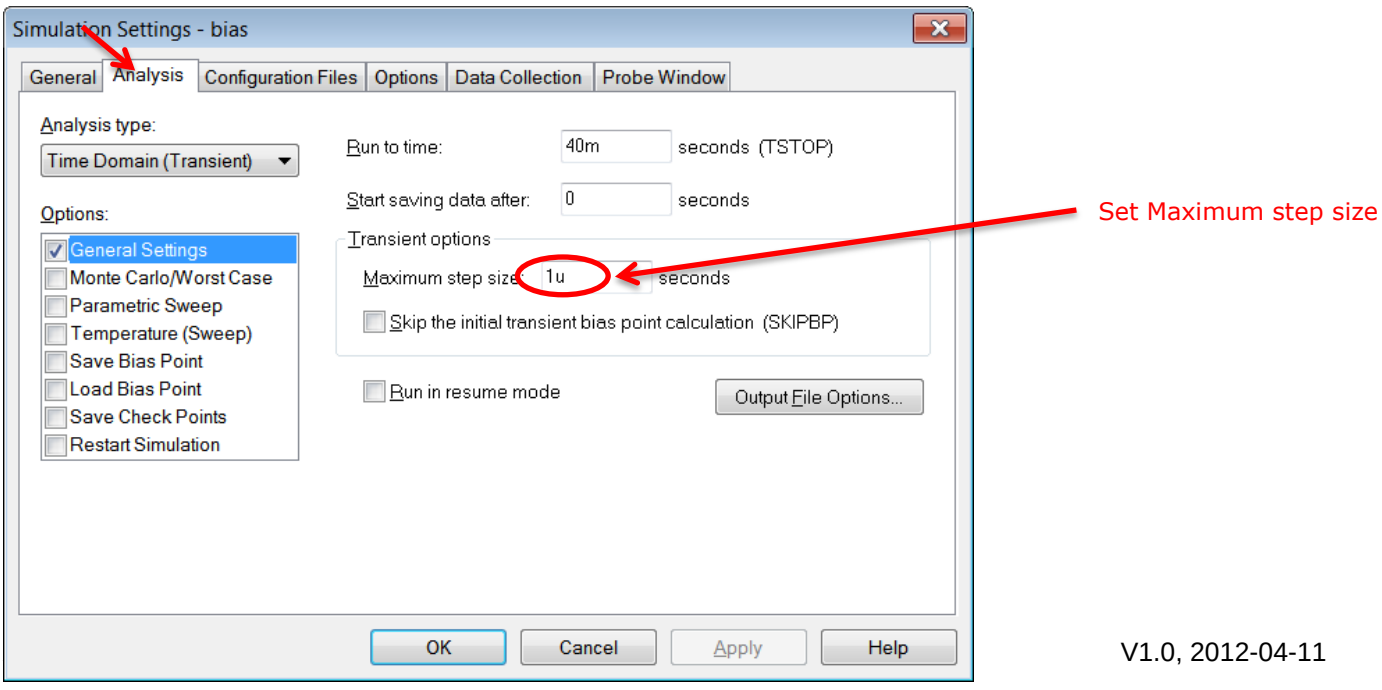
4) Add the Capture part *.olb symbol file: From the Project tab, under *Design Resour*ces, **right click** on *Library* and choose *Add File*.



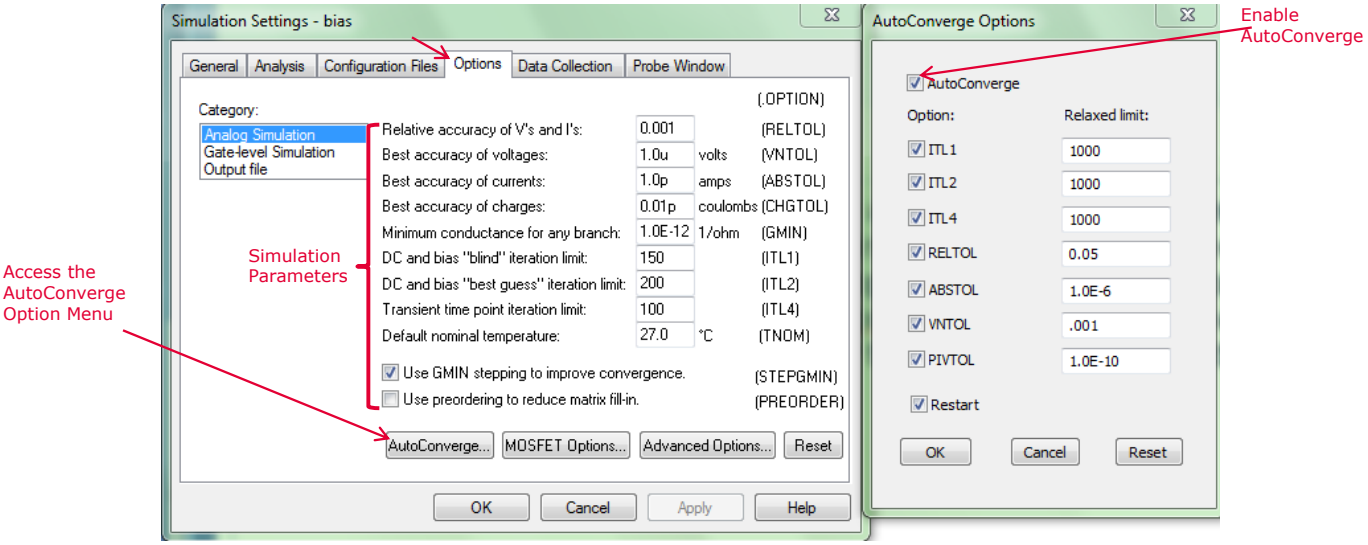
5) Adding that file to the design resources makes the model available for use: Searching for it in the Place Part sidebar, you can place the Model Symbol in a schematic of your choice.



6) To set the right parameters for simulation, click on Edit Simulation Profile.  It is recommended to set the Maximum step size to 1us to increase the accuracy. To increase the simulation speed you have to increase this value.



7) The PSpice Model is not guaranteed to work in every test situation with the default simulator settings. Therefore when the simulation does not converge it is recommended to change the simulation options and relax the parameters. Also, the simulator has a special option called AutoConverge, that helps overcoming convergence issues and it is found under the *PSpice\Edit Simulation Profile* menu



3 External Components

3.1 Voltage Sources

It is recommended to use VPWL or VPULSE voltage sources instead of VDC for the VS and INput pins to improve the model convergence.

3.2 Inductance

To account for cable in a real application, small inductances can be added. However the possibility to create oscillations is increased. In case of convergence problems, try to remove the line inductances.

4 Wiring

For the wirring of the models it is recommended to follow the setup of the application diagram in the datasheet. The detailed description for each can be found in Table 1:

PSpice Model Pin	Real Device Pin	Purpose	Recommended Wiring
VS	Exposed Pad, VS	Battery Supply, Main supply PROFET+ 12V: 5…28V PROFET+ 24V: 5…48V	Connect to a VPWL or VPULSE
INx	INx	Digital Input pins to switch the device channels (OUTx) ON / OFF	Connect to a 3.3V or 5V supply; eg: VPWL or VPULSE
DEN	DEN	Diagnosis Enable pin, Enables/Disables the diagnosis current at IS	Connect to a 3.3V or 5V supply; eg: VDC, VPWL or VPULSE
DSELx	DSELx	Diagnosis Select pin; Selects which channel is diagnosed via the IS pin	Connect to a 3.3V or 5V supply; eg: VDC, VPWL or VPULSE
IS	IS	The diagnosis pin that gives a current equivalent to the current through the output pin (OUTx). The ratio is given by the kilis value in the datasheet.	Can be left open (see Figure 5)
GND	GND	Ground connection of the device	Connect via a diode parallel to a 1k resistor to the ground.
TJx	Not available	Read out the junction temperature of the DMOS connected to OUTx. 1 Volt equals 1 Kelvin	Connect via a 1k resistor to the ground.
TCASE	Not available	Set the ambient temperature for the device	

Table 1 Pinout Description

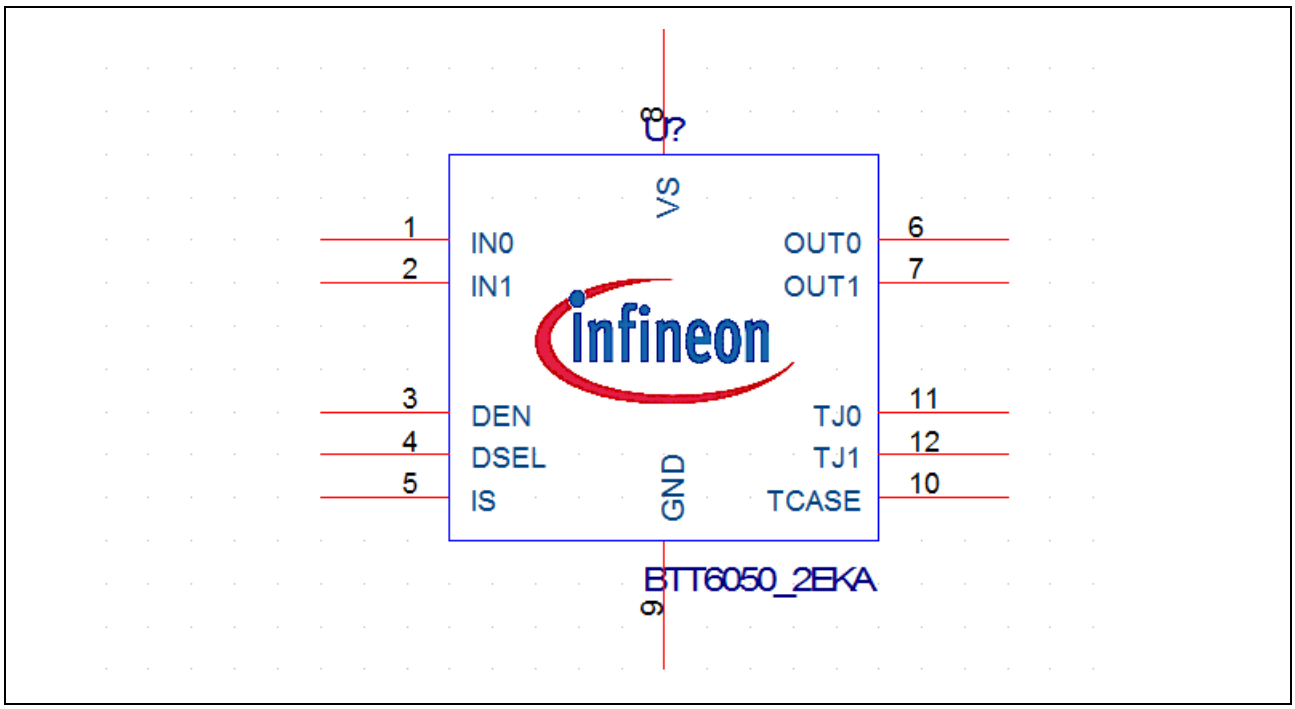


Figure 1 Pinout of BTT6050-2EKA Model

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5 Thermal Network

The PROFET+ PSpice models have a Cauer Network implemented to simulate the device heating.

5.1 General Cauer Network

The temperature behavior of a power semiconductor can be modeled by the thermal capacitance and thermal resistance. The junction temperature is determined by the summing up the ambient temperature and temperature increase.

$$T_j = \Delta T_{CH} + T_{amb} \quad (1)$$

Figure 2 shows the basic model for a Cauer Ladder.

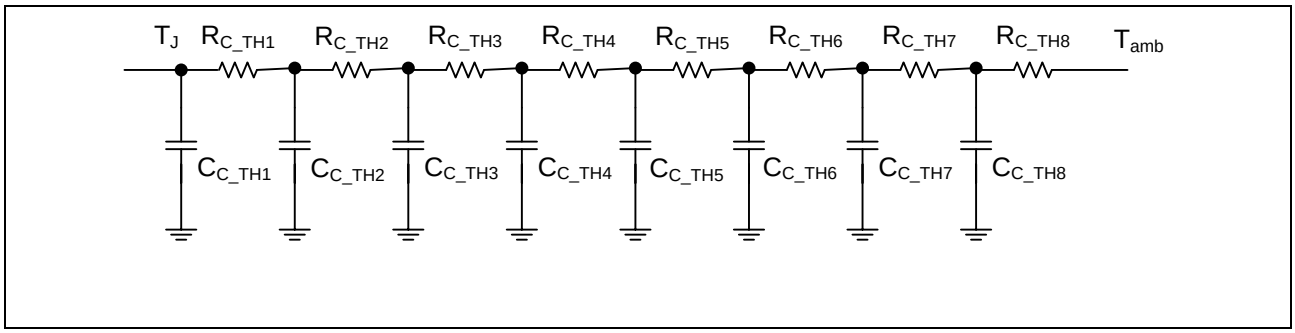

Figure 2 General Cauer Network

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Thermal parameter			Equivalent electrical parameter		
Symbol	Unit	Parameter	Symbol	Unit	Parameter
P	W	Power losses into the junction	I	A	Current
T	°C	Temperature of one layer	V	V	Potential
ΔT	K	Delta of temperature	U	V	Voltage
R_{th}	K/W	Thermal resistance	R	Ohm	Resistance
C_{th}	Ws/K	Thermal capacitance	C	F	Capacitance

Table 2 Thermal / Electrical model equivalence

5.2 PROFET+ PSpice Thermal Network

In the PROFET+ PSpice model for each channel an independent cauer ladder is implemented. In addition a connection to the thermal network of the adjacent channel exists to model the thermal interaction.

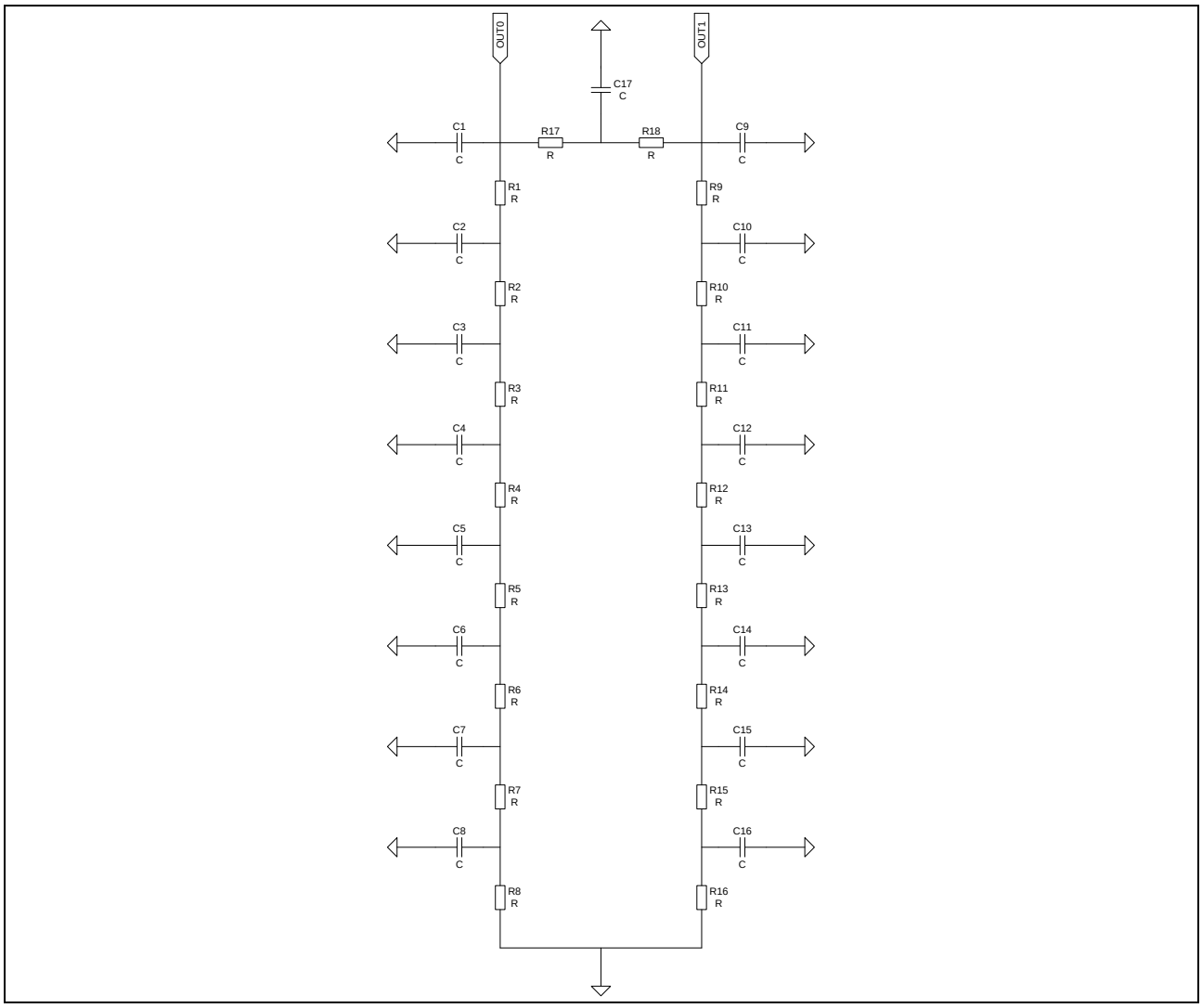

Figure 3 PROFET+ PSpice Cauer Network for a Dual Channel Device

6 Application Circuit

Figure 4 shows the basic schematics for the BTS5020-1EKA PSpice model.

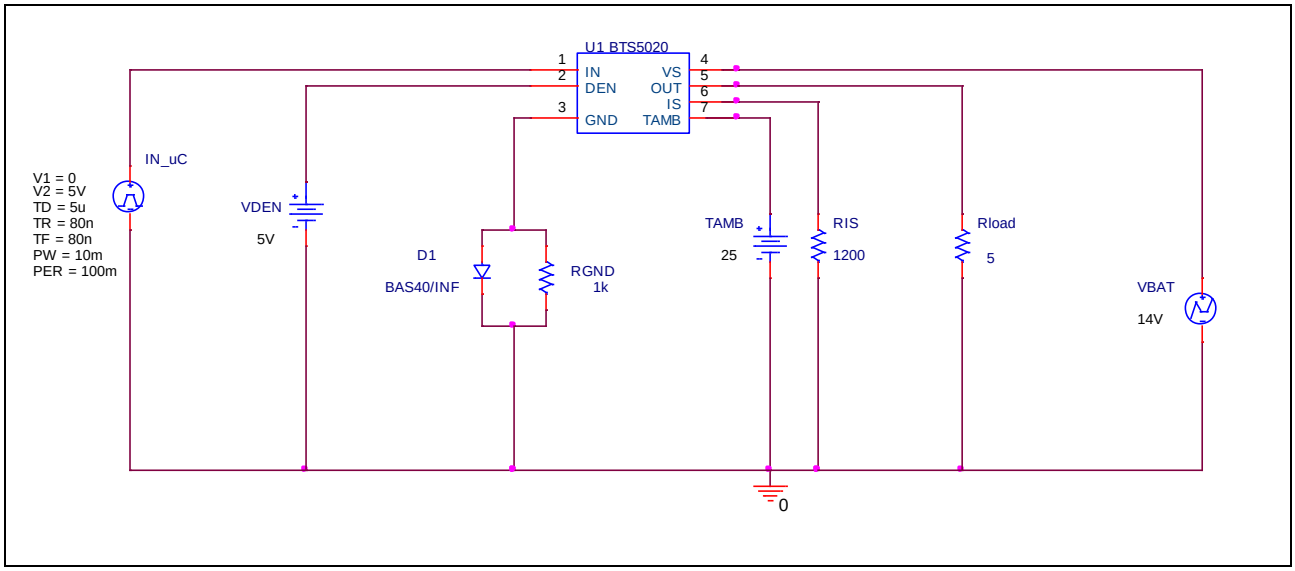

Figure 4 Basic Schematics of BTS5020-1EKA

Note: This is a simplified example of an application circuit.

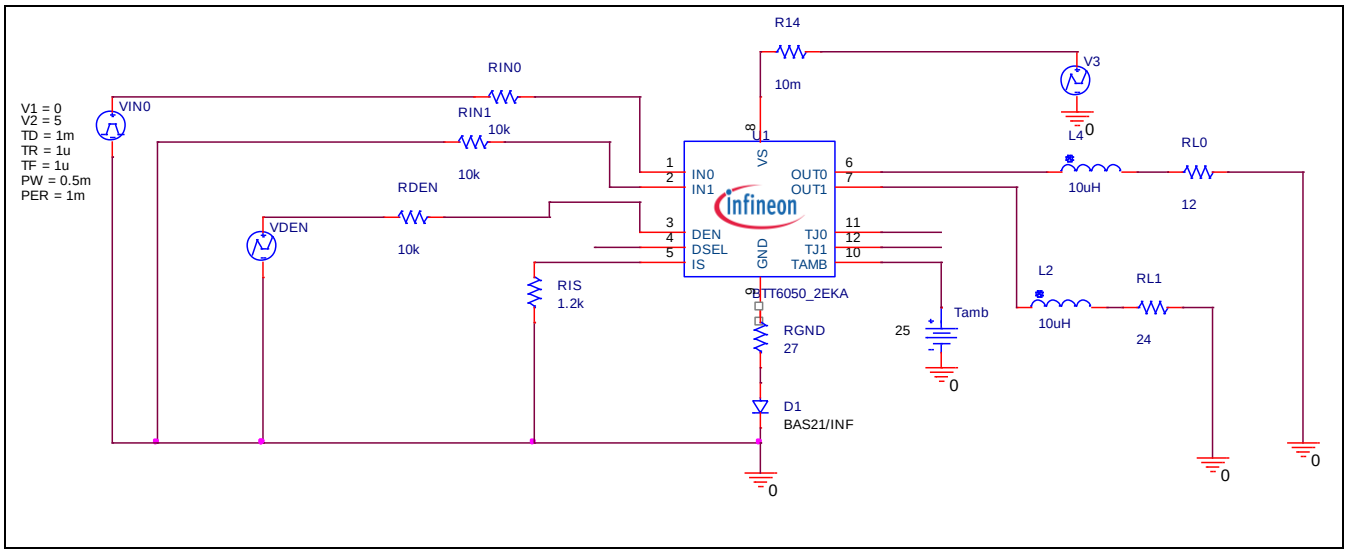

Figure 5 Basic Schematics of BTT6050-2EKA

Note: This is a simplified example of an application circuit.

7 Simulation Model Disclaimer

The Simulation Model is subject to change without notice. In addition, models can be a useful tool in evaluating device performance, they cannot reflect the accurate device performance under all conditions, nor are they intended to replace lab verifications. Infineon therefore does not assume any warranty or liability whatever arising from their use. Infineon does not assume any warranty or liability for the values and functions of the Simulation Model.

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Edition 2012-04-11

Published by
Infineon Technologies AG
81726 Munich, Germany

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Published by Infineon Technologies AG