DFI

DV970

COM Express Basic Module
User's Manual

A47900935

Copyright

Trademarks

COM Express Specification Reference

PICMG® COM Express Module™ Base Specification.

http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

1. The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
2. Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

Warranty

1. Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.

2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.

3. Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.

4. We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

1. To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.

2. Wear an antistatic wrist strap.

3. Do all preparation work on a static-free surface.

4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.

5. Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:

Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

To avoid damage to the system:

- Use the correct AC input voltage range.

To reduce the risk of electric shock:

- Unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One DV970 board
- One CPU Cooler (Height: 23.6mm for SKUs with normal temp. & 47.8mm for SKUs with wide temp.)

Optional Items

- COM333-I carrier board kit
- Heat spreader (Height: 11mm)

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

- Memory module
- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

Specifications

SYSTEM	Processor	Intel Atom® Processor C3000 Series, BGA1310 Intel Atom® C3958 Processor, 16 Cores, 16M Cache, 2.0GHz, 31W Intel Atom® C3808 Processor, 12 Cores, 12M Cache, 2.0GHz, 25W Intel Atom® C3758 Processor, 8 Cores, 16M Cache, 2.2GHz, 25W Intel Atom® C3708 Processor, 8 Cores, 16M Cache, 1.7GHz, 17W
	Memory	Two 260-pin ECC SODIMM up to 32GB Supports dual channel DDR4 1866/2133/2400MHz (Max. memory speed depends on CPU SKU)
	BIOS	Insyde SPI 128Mbit
EXPANSION	Interface	000G/200G/300G: B1: 2 x PCIe x2 or 2 x PCIe x1 (Gen 3) B2: 1 x PCIe x2 (Gen 3) + 1 x PCIe x1 (Gen 2) or 2 x PCIe x1 (Lane 8 Gen 3, Lane 12 Gen 2) B3: 1 x PCIe x8 or 2 x PCIe x4 or 4 x PCIe x2 or 4 x PCIe x1 (Gen 3) 100G: B1: 1 x PCIe x8 or 2 x PCIe x4 or 4 x PCIe x2 or 4 x PCIe x1 (Gen 3) B3: 2 x PCIe x2 or 2 x PCIe x1 (Gen 3) B4: 2 x PCIe x2 or 2 x PCIe x1 (Gen 3) 1 x LPC 1 x I²C 1 x SMBus 2 x UART (TX/RX)
ETHERNET	Controller	PHY for X557 or CS4227/CS4223 and Controller for Intel® I210AT/ Intel® I210IT 2 x Independent 10GbE Media Access Controller (dependent on SKU) Supports up to two 10GBASE-KR Interfaces and up to four 10GbE MAC ports Supports Intel® X557-AT/AT2/AT4 10GbE PHY Supports Inphi CS4227 (2 port)/CS4223 (4 port) (maximum bandwidth is 20Gb when 4 ports of 10G interface active at the same time) 1 x Intel® I210AT (10/100/1000Mbps) (normal temp.) or 1 x Intel® I210IT (10/100/1000Mbps) (wide temp.)

I/O	USB	2 x USB 3.0 4 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s)
	DIO	1 x 8-bit DIO (4 in, 4 out)
WATCHDOG TIMER	Output & Interval	System reset, programmable via software from 1 to 255 Seconds
SECURITY	TPM	Available upon request
POWER	Type	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
	Consumption	Boot up: 26.652W Idle: 24.226W Max. Load (Intel PTU): 40.206W S5 mode (WOL disabled): 7.4W/1.75W@5V standby power (with carrier board/without carrier board) S5 mode (WOL enabled): 8.55W/2.9W@5V standby power (with carrier board/without carrier board)
OS SUPPORT		Windows Server 2012 Windows Server 2016 Yocto Project v1.8/v2.0
ENVIRONMENT	Temperature	Intel Atom® C3758 & C3958 (normal temp.): support 0 to 60°C operating temperature Intel Atom® C3708 & C3808 (wide temp.): support -40 to 85°C operating temperature Storage Temperature: -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
	MTBF	Intel Atom®C3758 & C3958 (normal temp.): 2,055,292 hrs@25°C; 1,158,756 hrs@45°C; 747,377 hrs @60°C excluding accessories Intel Atom® C3708 & C3808 (wide temp.): 2,142,843 hrs@25°C; 1,186,002 hrs@45°C; 758,590 hrs @60°C excluding accessories Calculation Model: Telcordia Issue 2, Method Case 3 Environment: GB, GC – Ground Benign, Controlled
Mechanical	Dimensions	COM Express® Basic 95mm (3.74") x 125mm (4.9")
	Compliance	PICMG COM Express® R3.0, Type 7

Features

• Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

• DDR4

DDR4 delivers increased system bandwidth and improves performance. The advantages of DDR4 provide an extended battery life and improve the performance at a lower power than DDR3/DDR2.

• Serial ATA

Serial ATA is a storage interface that is compliant with SATA 1.0a specification. With speed of up to 6Gb/s (SATA 3.0), it improves hard drive performance faster than the standard parallel ATA whose data transfer rate is 100MB/s. However, the bandwidth of the SATA 3.0 will be limited by carrier board design.

• 10 Gigabit and Gigabit Ethernet

This system, based on the COM Express Type 7 revision 3.0 standard, supports up to two 10GbE KR interface lanes as well as NC-SI sideband signals. In addition, the Intel Atom® C3000 processor series comes with integrated Intel® Ethernet that supports up to four 10GbE adapters.

• USB

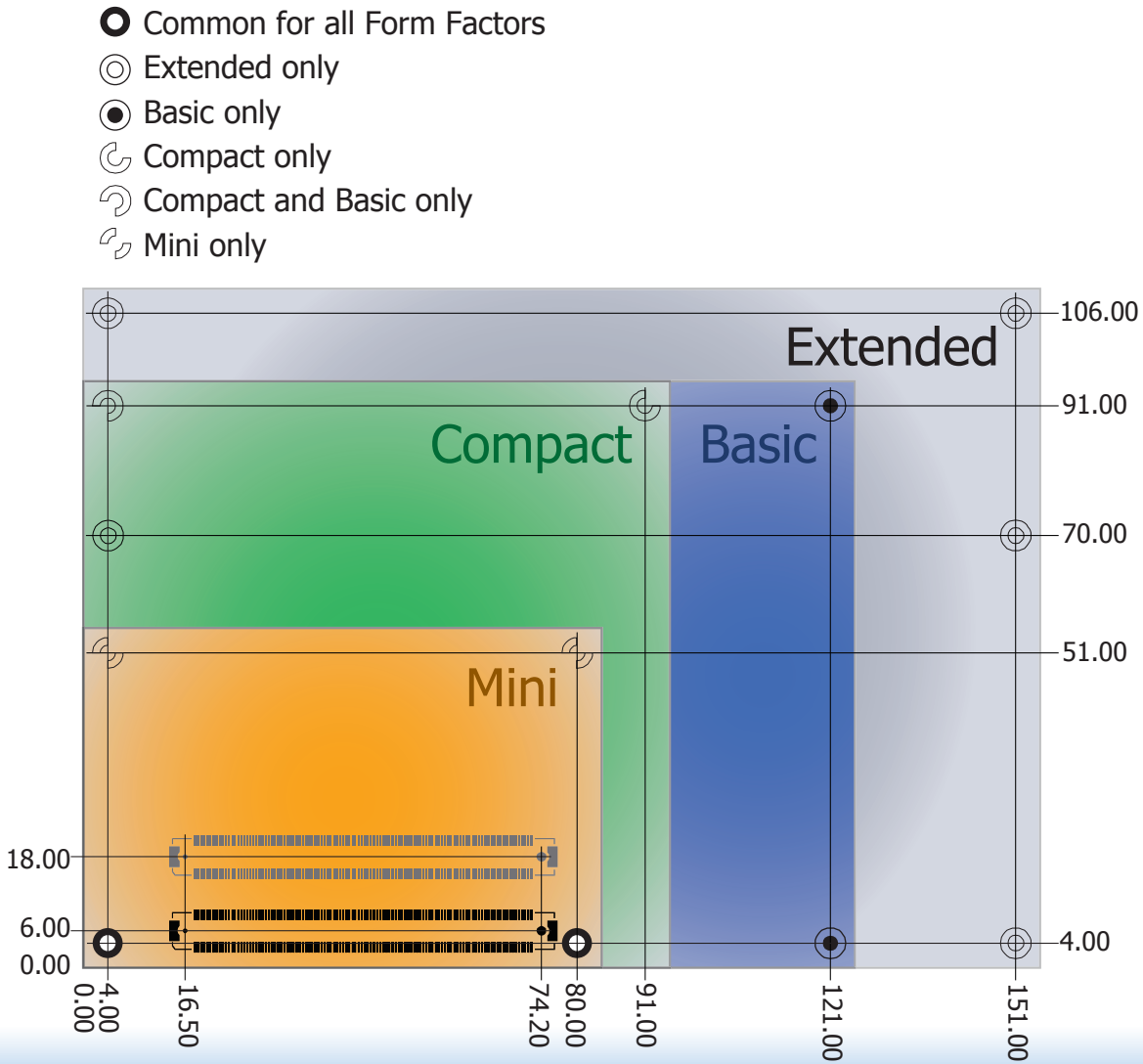
The system board supports the USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

Chapter 2 - Concept

COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.

DV970 is a COM Express Basic module. Its dimension is 95mm x 125mm (4.92" x 3.74").



Specification Comparison Table

The table below shows the COM Express standard specifications and the corresponding specifications supported on the DV970 module.

Type 7 Based on Type 6. Modules trades all audio and video interfaces, 2 SATA ports and four USB 2.0 for additional PCI Express lanes, four 10 Gb Ethernet ports and an NC-SI management interface for the GbE port.

Connector	Feature	COM Express Module Base Specification Type 7 Min / Max	DFI DV970 Type 7 (000G/200G/300G)	DFI DV970 Type 7 (100G)
	System I/O			
A-B	PCI Express Lanes 0 - 5	6 / 6	4	6
A-B , C-D	PCI Express Lanes 6 - 15	0 / 10	3	2
C-D	PCI Express Lanes 16 - 31	0 / 16	8	8
C-D	PCI Express Graphics (PEG)	NA	NA	NA
C-D	10G LAN Ports 0 - 3	0 / 4	4	4
A-B	NC-SI	0 / 1	1	0
A-B	1Gb LAN Port 0	1 / 1	1	0
A-B	DDI 0	NA	NA	NA
A-B	DDIs 1 - 3	NA	NA	NA
A-B	LVDS Channel A	NA	NA	NA
A-B	LVDS Channel B	NA	NA	NA
A-B	eDP on LVDS CH A pins	NA	NA	NA
A-B	VGA Port	NA	NA	NA
A-B	Serial Ports 1 - 2	0 / 2	2	2
A-B	CAN interface on SER1	0 / 1	0	0
A-B	SATA Ports	0 / 2	2	2
A-B	HDA Digital Interface	NA	NA	NA
A-B	USB 2.0 Ports	4 / 4	4	4
A-B	USB0 Client	0 / 1	0	0
A-B	USB7 Client	NA	NA	NA
C-D	USB 3.0 Ports	0 / 4	2	2
A-B	LPC Bus or eSPI	1 / 1	1 LPC	1 LPC
A-B	SPI (Devices)	1 / 2	1	1
C-D	Rapid Shutdown	0 / 1	0	0
	System Management			
A-B[2]	SDIO (muxed on GPIO)	0 / 1	0	0
A-B	General Purpose I/O	8 / 8	8	8
A-B	SMBus	1 / 1	1	1
A-B	I2C	1 / 1	1	1
A-B	Watchdog Timer	0 / 1	1	1
A-B	Speaker Out	1 / 1	1	1
A-B	Carrier Board BIOS Flash Support	0 / 1	1	1
A-B	Reset Functions	1 / 1	1	1
A-B	Trusted Platform Module	0 / 1	1	1
	Power Management			
A-B	Thermal Protection	0 / 1	1	1
A-B	Battery Low Alarm	0 / 1	1	1
A-B	Suspend/Wake Signals	0 / 3	2	2
A-B	Power Button Support	1 / 1	1	1
A-B	Power Good	1 / 1	1	1
A-B	VCC_5V_SBY Contacts	4 / 4	4	4
A-B[1]	Sleep Input	0 / 1	1	1
A-B[1]	Lid Input	0 / 1	1	1
A-B[1]	Carrier Board Fan Control	0 / 1	1	1
	Power			
A-B , C-D	VCC_12V Contacts	24 / 24	24	24

1. Indicates 12V-tolerant features on former VCC_12V signals.
2. Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

Features	C3958	C3808	C3758	C3708
Thermal Design Power (TDP) (Watts)	31	25	25	17
Number of 64-bit Intel Atom® Microarchitecture Goldmont Cores	16	12	8	8
Processor Base Frequency (GHz)	2.0	2.0	2.2	1.7
Total SoC L2 Cache (MB)	16	12	16	16
Max. Number of Memory Channels Available	2			
Max. DDR4 (1.2V) Memory Data Rate Supported (MT/s)	2400	2133		
Number of High-Speed I/O (HSIO) Lanes Shared between PCIe, SATA, and USB 3.0	20			
HSIO Lane Numbers (0 through 19) Available	Lanes 0-19			
Max. Number of PCI Express (8.0/5.0/2.5 GT/s) Lanes	16 via HSIO Lanes from Lanes 0-15			
Max. Number of SATA (6.0/3.0/1.5 Gbps) Lanes	16 via HSIO Lanes from Lanes 4-19			
Max. Number of Sets of USB 3.0 Signals (SSTX+/SSTX- SSRX+/SSRX-)	4 via HSIO Lanes from Lanes 16-19			
Number of Sets of USB 2.0 Signals (DATA+/DATA-)	4			
LAN Controller 0 (Gb/s)*	10/2.5/1			
LAN Controller 1 (Gb/s)*	10/2.5/1			

* Each LAN controller must run the same LEK.

Note: Different SKUs may require different BIOS.

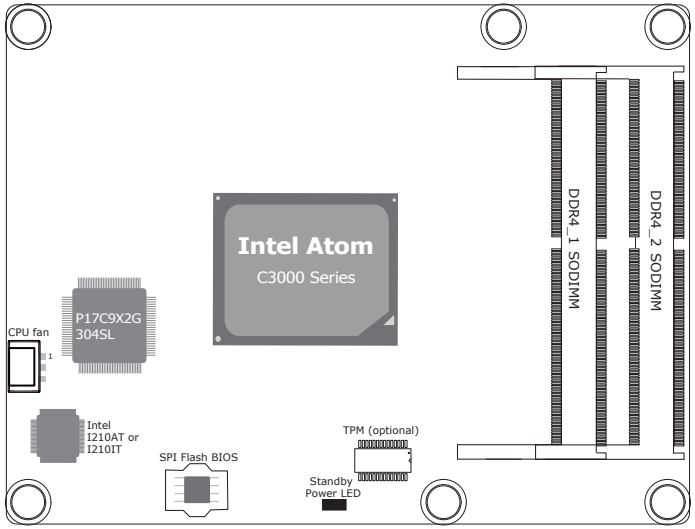
DV970 PCIe Lanes Routing Table

This table below summarizes the configuration of High-Speed I/O (HSIO) Lanes shared among PCIe, SATA, and USB 3.0 for different SKUs of DV970.

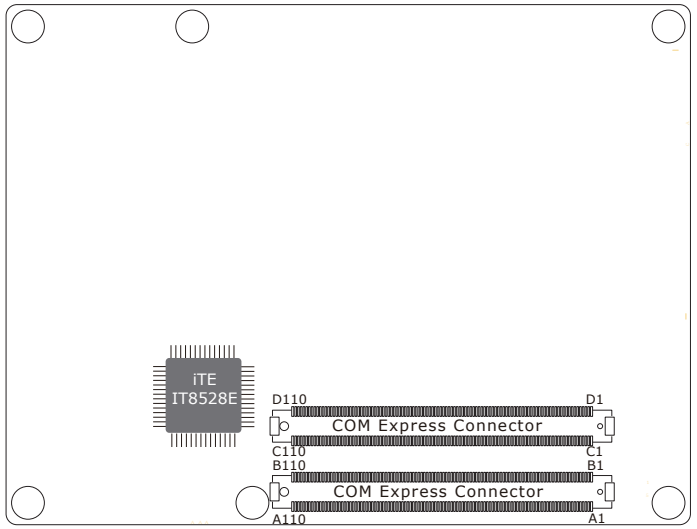
<table>
<tr><th colspan="2">PICMG COM.0 R3.0 Type-7
PCIe Lanes Mapping</th><th colspan="5">DV970
(000G/200G/300G)</th><th colspan="5">DV970
(100G)</th></tr>
<tr><th>Bucket</th><th>Lane NO.</th><th colspan="5">Link Width</th><th colspan="5">Link Width</th></tr>
<tr><td rowspan="8">B1</td><td>Lane 0</td><td rowspan="2">via HSIO
Lane 0-1</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td><td rowspan="8">via HSIO
Lane 0-7</td><td rowspan="8">x8
(default)</td><td rowspan="4">x4
(optional)</td><td>x2
(optional)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 1</td><td></td><td></td></tr>
<tr><td>Lane 2</td><td colspan="4" rowspan="2">N.C.</td><td>x2
(optional)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 3</td><td></td><td></td></tr>
<tr><td>Lane 4</td><td rowspan="2">via HSIO
Lanes 4-5</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td><td rowspan="4">x4
(optional)</td><td>x2
(optional)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 5</td><td></td><td></td><td></td></tr>
<tr><td>Lane 6</td><td colspan="4" rowspan="2">N.C.</td><td>x2
(optional)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 7</td><td></td><td></td></tr>
<tr><td rowspan="8">B2</td><td>Lane 8</td><td rowspan="2">via HSIO
Lanes 2-3</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td><td colspan="5" rowspan="8">N.C.</td></tr>
<tr><td>Lane 9</td><td></td><td></td></tr>
<tr><td>Lane 10</td><td colspan="4" rowspan="2">N.C.</td></tr>
<tr><td>Lane 11</td><td></td></tr>
<tr><td>Lane 12</td><td>via HSIO</td><td colspan="2">x1 (default for BMC)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 13</td><td colspan="4" rowspan="3">N.C.</td></tr>
<tr><td>Lane 14</td></tr>
<tr><td>Lane 15</td></tr>
<tr><td rowspan="8">B3</td><td>Lane 16</td><td rowspan="8">via HSIO
Lane 8-15</td><td rowspan="8">x8
(default)</td><td rowspan="4">x4
(optional)</td><td>x2
(optional)</td><td>x1 (optional)</td><td>via HSIO
Lane 8-9</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 17</td><td></td><td></td><td></td></tr>
<tr><td>Lane 18</td><td rowspan="2">x2
(optional)</td><td>x1 (optional)</td><td colspan="4" rowspan="2">N.C.</td></tr>
<tr><td>Lane 19</td><td></td></tr>
<tr><td>Lane 20</td><td rowspan="4">x4
(optional)</td><td>x2
(optional)</td><td>x1 (optional)</td><td>via HSIO
Lane 12-13</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 21</td><td></td><td></td><td></td></tr>
<tr><td>Lane 22</td><td rowspan="2">x2
(optional)</td><td>x1 (optional)</td><td colspan="4" rowspan="2">N.C.</td></tr>
<tr><td>Lane 23</td><td></td></tr>
<tr><td rowspan="8">B4</td><td>Lane 24</td><td colspan="8" rowspan="8">N.C.</td><td>via HSIO
Lane 10-11</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 25</td><td></td><td></td><td></td></tr>
<tr><td>Lane 26</td><td colspan="4" rowspan="2">N.C.</td></tr>
<tr><td>Lane 27</td></tr>
<tr><td>Lane 28</td><td>via HSIO
Lane 14-15</td><td colspan="2" rowspan="2">x2 (default)</td><td>x1 (optional)</td></tr>
<tr><td>Lane 29</td><td></td><td></td><td></td></tr>
<tr><td>Lane 30</td><td colspan="4" rowspan="2">N.C.</td></tr>
<tr><td>Lane 31</td></tr>
<tr><td rowspan="4">USB3</td><td>USB3_P0</td><td>via HSIO</td><td colspan="7">USB3_P0</td><td>via HSIO</td><td colspan="4">USB3_P0</td></tr>
<tr><td>USB3_P1</td><td>via HSIO</td><td colspan="7">USB3_P1</td><td>via HSIO</td><td colspan="4">USB3_P1</td></tr>
<tr><td>USB3_P2</td><td colspan="8" rowspan="2">N.C.</td><td colspan="5" rowspan="2">N.C.</td></tr>
<tr><td>USB3_P3</td></tr>
<tr><td rowspan="2">SATA3</td><td>SATA3_P0</td><td>via HSIO</td><td colspan="7">SATA3_P0</td><td>via HSIO</td><td colspan="4">SATA3_P0</td></tr>
<tr><td>SATA3_P1</td><td>via HSIO</td><td colspan="7">SATA3_P1</td><td>via HSIO</td><td colspan="4">SATA3_P1</td></tr>
</table>

Chapter 3 - Hardware Installation

Board Layout

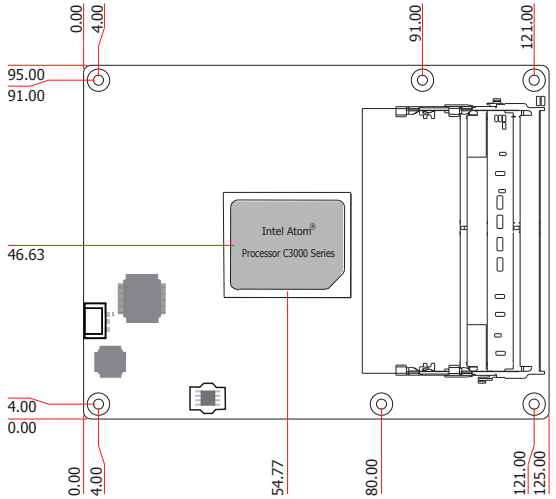


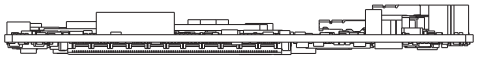
Top View

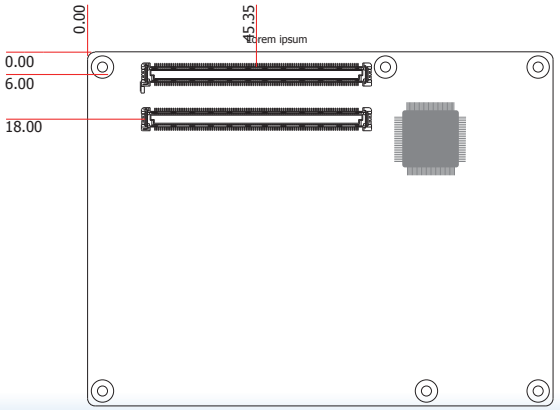


Bottom View

Mechanical Diagram



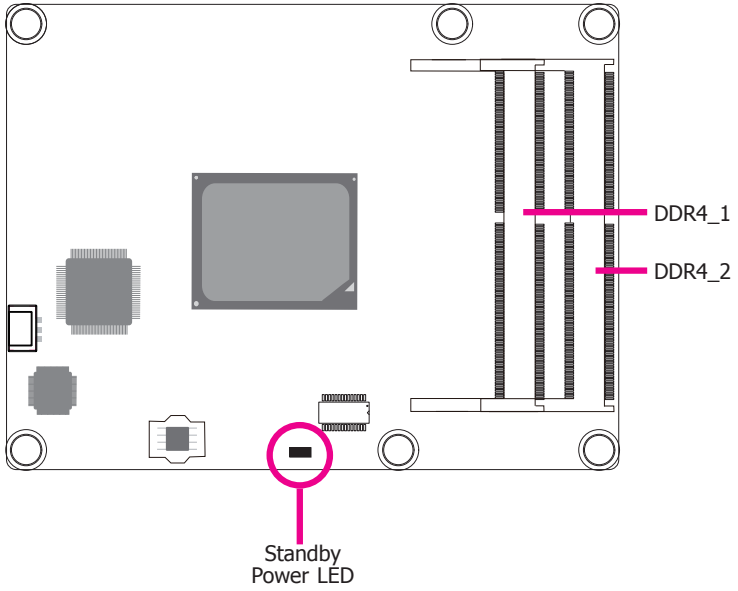




Important:
Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

System Memory

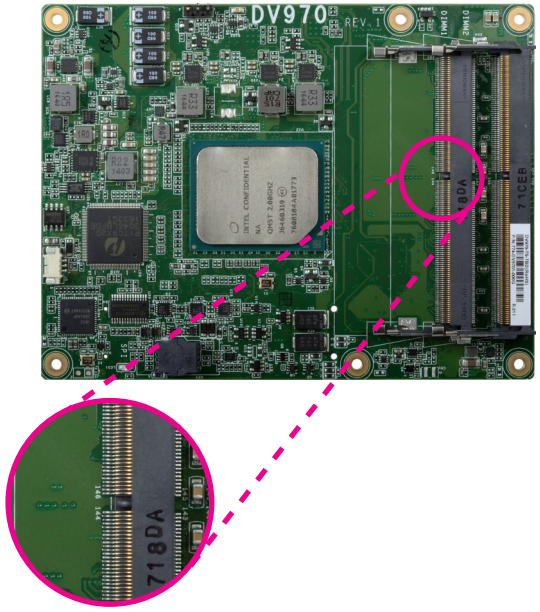
Important:
When the Standby Power LED is red, it indicates that there is power on the board. Power off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the board and components.



Installing a SODIMM Module

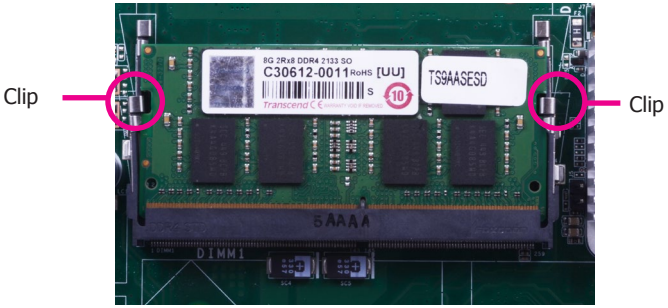
Note:
The system board used in the following illustrations may not resemble the actual one. These illustrations are for reference only.

1. Make sure the PC and all other peripheral devices connected to it has been powered down.
2. Disconnect all power cords and cables.
3. Locate the SODIMM socket on the system board.
4. Note the key on the socket. The key ensures that the module can be plugged into the socket in only one direction.



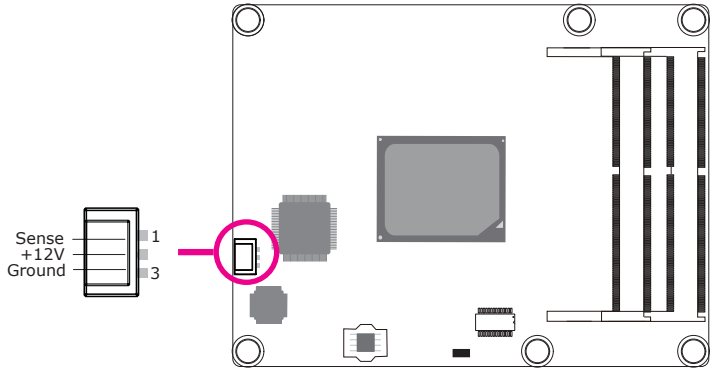
5. Grasping the module by its edges, align the module into the socket at an approximately 30 degrees angle. Apply firm even pressure to each end of the module until it slips down into the socket. The contact fingers on the edge of the module will almost completely disappear inside the socket.

6. Push down the module until the clips at each end of the socket lock into position. You will feel a distinctive "click", indicating the module is correctly locked into position.



Connectors

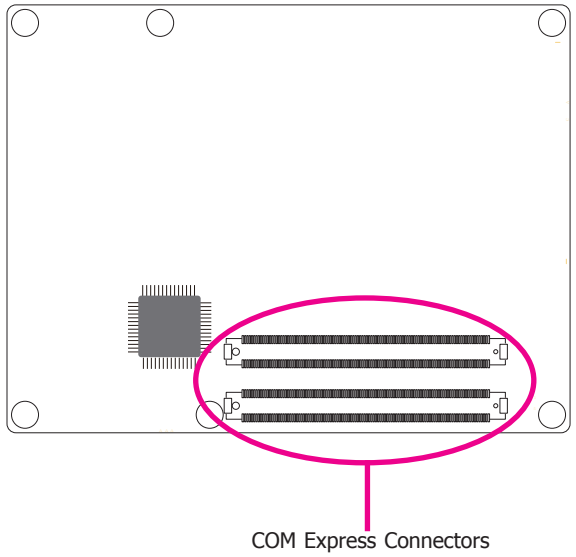
CPU Fan Connector



Connect the CPU fan's cable connector to the CPU fan connector on the board. The cooling fan will provide adequate airflow throughout the chassis to prevent overheating the CPU and board components.

COM Express Connectors

The COM Express connectors are used to interface the DV970 COM Express board to a carrier board. Connect the COM Express connectors (located on the solder side of the board) to the COM Express connectors on the carrier board.



Refer to the following pages for the pin functions of these connectors.

COM Express Connectors-Continued

Row A		Row B		Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	PCIE_TX8+	B71	PCIE_RX8+
A17	SATA0_TX-	B17	SATA1_TX-	A72	PCIE_TX8-	B72	PCIE_RX8-
A18	SUS_S4#	B18	SUS_STAT#	A73	GND	B73	GND
A19	SATA0_RX+	B19	SATA1_RX+	A74	PCIE_TX9+	B74	PCIE_RX9+
A20	SATA0_RX-	B20	SATA1_RX-	A75	PCIE_TX9-	B75	PCIE_RX9-
A21	GND (FIXED)	B21	GND (FIXED)	A76	GND	B76	GND
A22	N.C.	B22	N.C.	A77	N.C.	B77	N.C.
A23	N.C.	B23	N.C.	A78	N.C.	B78	N.C.
A24	SUS_S5#	B24	PWR_OK	A79	GND	B79	GND
A25	N.C.	B25	N.C.	A80	GND (FIXED)	B80	GND (FIXED)
A26	N.C.	B26	N.C.	A81	N.C.	B81	N.C.
A27	BATLOW#	B27	WDT	A82	N.C.	B82	N.C.
A28	(S)ATA_ACT#	B28	RSVD	A83	GND	B83	GND
A29	RSVD	B29	RSVD	A84	NCSI_TX_EN	B84	VCC_5V_SBY
A30	RSVD	B30	RSVD	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	RSVD	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	RSVD	B33	I2C_CK	A88	PCIE_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CK_REF-	B89	NCSI_RX_ER
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	N.C.	B36	N.C.	A91	SPI_POWER	B91	NCSI_CLK_IN
A37	N.C.	B37	N.C.	A92	SPI_MISO	B92	NCSI_RXD1
A38	GND	B38	GND	A93	GPO0	B93	NCSI_RXD0
A39	PCIE_TX12+	B39	PCIE_RX12+	A94	SPI_CLK	B94	NCSI_CRS_DV
A40	PCIE_TX12-	B40	PCIE_RX12-	A95	SPI_MOSI	B95	NCSI_TXD1
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	NCSI_TXD0
A42	USB2-	B42	USB3-	A97	N.C.	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	NCSI_ARB_IN
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	NCSI_ARB_OUT
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN#	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD	B48	N.C.	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

DV970 only supports LPC interface, no eSPI mode interface.

Row C		Row D		Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)	C56	PCIE_RX17-	D56	PCIE_TX17-
C2	GND	D2	GND	C57	N.C.	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PCIE_RX18+	D58	PCIE_TX18+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PCIE_RX18-	D59	PCIE_TX18-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PCIE_RX19+	D61	PCIE_TX19+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PCIE_RX19-	D62	PCIE_TX19-
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	N.C.	D9	N.C.	C64	RSVD	D64	RSVD
C10	N.C.	D10	N.C.	C65	PCIE_RX20+	D65	PCIE_TX20+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PCIE_RX20-	D66	PCIE_TX20-
C12	N.C.	D12	N.C.	C67	RAPID_SHUTDOWN	D67	GND
C13	N.C.	D13	N.C.	C68	PCIE_RX21+	D68	PCIE_TX21+
C14	GND	D14	GND	C69	PCIE_RX21-	D69	PCIE_TX21-
C15	10G_PHY_MDC_SCL3	D15	10G_PHY_MDIO_SDA3	C70	GND (FIXED)	D70	GND (FIXED)
C16	10G_PHY_MDC_SCL2	D16	10G_PHY_MDIO_SDA2	C71	PCIE_RX22+	D71	PCIE_TX22+
C17	10G_SDP2	D17	10G_SDP3	C72	PCIE_RX22-	D72	PCIE_TX22-
C18	GND	D18	GND	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PCIE_RX23+	D74	PCIE_TX23+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PCIE_RX23-	D75	PCIE_TX23-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD	D77	RSVD
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PCIE_RX24+	D78	PCIE_TX24+
C24	10G_INT2	D24	10G_INT3	C79	PCIE_RX24-	D79	PCIE_TX24-
C25	GND	D25	GND	C80	GND (FIXED)	D80	GND (FIXED)
C26	10G_KR_RX3+	D26	10G_KR_TX3+	C81	PCIE_RX25+	D81	PCIE_TX25+
C27	10G_KR_RX3-	D27	10G_KR_TX3-	C82	PCIE_RX25-	D82	PCIE_TX25-
C28	GND	D28	GND	C83	RSVD	D83	RSVD
C29	10G_KR_RX2+	D29	10G_KR_TX2+	C84	GND	D84	GND
C30	10G_KR_RX2-	D30	10G_KR_TX2-	C85	N.C.	D85	N.C.
C31	GND (FIXED)	D31	GND (FIXED)	C86	N.C.	D86	N.C.
C32	10G_SFP_SDA3	D32	10G_SFP_SCL3	C87	GND	D87	GND
C33	10G_SFP_SDA2	D33	10G_SFP_SCL2	C88	N.C.	D88	N.C.
C34	10G_PHY_RST_23	D34	10G_PHY_CAP_23	C89	N.C.	D89	N.C.
C35	10G_PHY_RST_01	D35	10G_PHY_CAP_01	C90	GND (FIXED)	D90	GND (FIXED)
C36	10G_LED_SDA	D36	RSVD	C91	PCIE_RX28+	D91	PCIE_TX28+
C37	10G_LED_SCL	D37	RSVD	C92	PCIE_RX28-	D92	PCIE_TX28-
C38	10G_SFP_SDA1	D38	10G_SFP_SCL1	C93	GND	D93	GND
C39	10G_SFP_SDA0	D39	10G_SFP_SCL0	C94	PCIE_RX29+	D94	PCIE_TX29+
C40	10G_SDP0	D40	10G_SDP1	C95	PCIE_RX29-	D95	PCIE_TX29-
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	10G_KR_RX1+	D42	10G_KR_TX1+	C97	RSVD	D97	RSVD
C43	10G_KR_RX1-	D43	10G_KR_TX1-	C98	N.C.	D98	N.C.
C44	GND	D44	GND	C99	N.C.	D99	N.C.
C45	10G_PHY_MDC_SCL1	D45	10G_PHY_MDIO_SDA1	C100	GND (FIXED)	D100	GND (FIXED)
C46	10G_PHY_MDC_SCL0	D46	10G_PHY_MDIO_SDA0	C101	N.C.	D101	N.C.
C47	10G_INT0	D47	10G_INT1	C102	N.C.	D102	N.C.
C48	GND	D48	GND	C103	GND	D103	GND
C49	10G_KR_RX0+	D49	10G_KR_TX0+	C104	VCC_12V	D104	VCC_12V
C50	10G_KR_RX0-	D50	10G_KR_TX0-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PCIE_RX16+	D52	PCIE_TX16+	C107	VCC_12V	D107	VCC_12V
C53	PCIE_RX16-	D53	PCIE_TX16-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	RSVD	C109	VCC_12V	D109	VCC_12V
C55	PCIE_RX17+	D55	PCIE_TX17+	C110	GND (FIXED)	D110	GND (FIXED)

COM Express Connectors Signals and Descriptions

Pin Types I Input to the Module O Output from the Module I/O Bi-directional input / output signal OD Open drain output RSVD pins are reserved for future use and should be no connect. Do not tie the RSVD pins together. Power Inputs used for power delivery to the Module electronics. KR 10GBASE-KR compatible signal.

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend			
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend			
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend			
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V			Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V			Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V			Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V			Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE0_CTREF	A14	REF	GND min, 3.3V max		N.C.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.
GBE0_SDP	A49	I/O	3.3V Suspend/3.3V		RSVD PU 10KΩ	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.

NC-SI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
NCSI_CLK_IN	B91	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Clock reference for receive, transmit, and control interface.
NCSI_RXD0	B93	O CMOS	3.3V Suspend/3.3V		PD 3KΩ to GND	NC-SI Receive Data (from NC to BMC).
NCSI_RXD1	B92	O CMOS	3.3V Suspend/3.3V		PD 3KΩ to GND	NC-SI Receive Data (from NC to BMC).
NCSI_TXD0	B96	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Transmit Data (from BMC to NC).
NCSI_TXD1	B95	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Transmit Data (from BMC to NC).
NCSI_CRS_DV	B94	O CMOS	3.3V Suspend/3.3V		PD 10KΩ to GND	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.
NCSI_TX_EN	A84	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Transmit enable.
NCSI_RX_ER	B89	O CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3.3V Suspend	NC-SI Receive error.
NCSI_ARB_IN	B98	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	RSVD PU 4.7KΩ to 3.3V Suspend (IPD 20KΩ)	NC-SI hardware arbitration input.
NCSI_ARB_OUT	B99	O CMOS	3.3V Suspend/3.3V			NC-SI hardware arbitration output.

10Gb Ethernet Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
10G_KR_TX0+	D49	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX0-	D50	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX1+	D42	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX1-	D43	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX2+	D29	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX2-	D30	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX3+	D26	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX3-	D27	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_RX0+	C49	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX0-	C50	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX1+	C42	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX1-	C43	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX2+	C29	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX2-	C30	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX3+	C26	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX3-	C27	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_PHY_MDIO_SDA0	D46	O CMOS I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	MDIO: PU 2.2KΩ to 3.3V Suspend	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. **I2C Mode:** I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.
10G_PHY_MDIO_SDA1	D45					
10G_PHY_MDIO_SDA2	D16					
10G_PHY_MDIO_SDA3	D15					
10G_PHY_MDC_SCL0	C46	O CMOS I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	MDC : PU 2.2KΩ to 3.3V Suspend	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. **I2C Mode:** I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.
10G_PHY_MDC_SCL1	C45					
10G_PHY_MDC_SCL2	C16					
10G_PHY_MDC_SCL3	C15					
10G_PHY_CAP_01	D35	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 100KΩ to 3.3V Suspend	Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I²C interface
10G_PHY_CAP_23	D34	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 100KΩ to 3.3V Suspend	Phy mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configurationcapability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I²C interface
10G_SFP_SDA0	C39	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	IPU 5KΩ, RSV PU 4.7KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SDA1	C38	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	IPU 5KΩ, RSV PU 4.7KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.

10G_SFP_SDA2	C33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 4.7KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SDA3	C32	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 4.7KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL0	D39	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	IPU 5KΩ, RSV PU 4.7KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL1	D38	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	IPU 5KΩ, RSV PU 4.7KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL2	D33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 4.7KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL3	D32	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 4.7KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_LED_SDA	C36	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 4.7KΩ to 3.3V Suspend	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs. Refer to the details in I2C Data Mapping to Carrier Board Based PCA9539 I/O Expander.
10G_LED_SCL	C37	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 4.7KΩ to 3.3V Suspend	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs.
10G_INT0	C47	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_INT1	D47	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_INT2	C24	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_INT3	D24	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_SDP0	C40	I/O CMOS	3.3V Suspend/3.3V			Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_SDP1	D40	I/O CMOS	3.3V Suspend/3.3V			Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_SDP2	C17	I/O CMOS	3.3V Suspend/3.3V			Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_SDP3	D17	I/O CMOS	3.3V Suspend/3.3V			Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_PHY_RST_01	C35	O CMOS	3.3V Suspend/3.3V		PU 10KΩ to 3.3V Suspend	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used).
10G_PHY_RST_23	C34	O CMOS	3.3V Suspend/3.3V		PU 10KΩ to 3.3V Suspend	Output signal that resets an Optical PHY on port 2 and port 3 (with Copper PHY this signal is not used).

SATA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
SATA0_TX+	A16	O SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module		AC Coupling capacitor	
SATA0_RX+	A19	I SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module		AC Coupling capacitor	
SATA1_TX+	B16	O SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module		AC Coupling capacitor	
SATA1_RX+	B19	I SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module		AC Coupling capacitor	

(S)ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V		AND Gate out, up to 3.3V	Serial ATA (activity indicator), active low.

General Purpose PCI Express Lanes Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
PCIE_TX0+	A68	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 0
PCIE_TX0-	A69				AC Coupling capacitor	
PCIE_RX0+	B68	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 1
PCIE_TX1-	A65				AC Coupling capacitor	
PCIE_RX1+	B64	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 1
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 2
PCIE_TX2-	A62				AC Coupling capacitor	
PCIE_RX2+	B61	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 2
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 3
PCIE_TX3-	A59				AC Coupling capacitor	
PCIE_RX3+	B58	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 3
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 4
PCIE_TX4-	A56				AC Coupling capacitor	
PCIE_RX4+	B55	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 4
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 5
PCIE_TX5-	A53				AC Coupling capacitor	
PCIE_RX5+	B52	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 5
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 6
PCIE_TX6-	D20				AC Coupling capacitor	
PCIE_RX6+	C19	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 6
PCIE_RX6-	C20					
PCIE_TX7+	D22	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 7
PCIE_TX7-	D23				AC Coupling capacitor	
PCIE_RX7+	C22	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 7
PCIE_RX7-	C23					
PCIE_TX8+	A71	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 8
PCIE_TX8-	A72				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX8+	B71	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 8
PCIE_RX8-	B72					Different connector layout for Type 7
PCIE_TX9+	A74	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 9
PCIE_TX9-	A75				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX9+	B74	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 9
PCIE_RX9-	B75					Different connector layout for Type 7
PCIE_TX10+	A77	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 10
PCIE_TX10-	A78				N.C.	Different connector layout for Type 7
PCIE_RX10+	B77	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 10
PCIE_RX10-	B78				N.C.	Different connector layout for Type 7

PCIE_TX11+	A81	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 11
PCIE_TX11-	A82				N.C.	Different connector layout for Type 7
PCIE_RX11+	B81	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 11
PCIE_RX11-	B82				N.C.	Different connector layout for Type 7
PCIE_TX12+	A39	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 12
PCIE_TX12-	A40				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX12+	B39	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 12
PCIE_RX12-	B40					Different connector layout for Type 7
PCIE_TX13+	A36	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 13
PCIE_TX13-	A37				N.C.	Different connector layout for Type 7
PCIE_RX13+	B36	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 13
PCIE_RX13-	B37				N.C.	Different connector layout for Type 7
PCIE_TX14+	A25	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 14
PCIE_TX14-	A26				N.C.	Different connector layout for Type 7
PCIE_RX14+	B25	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 14
PCIE_RX14-	B26				N.C.	Different connector layout for Type 7
PCIE_TX15+	A22	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 15
PCIE_TX15-	A23				N.C.	Different connector layout for Type 7
PCIE_RX15+	B22	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 15
PCIE_RX15-	B23				N.C.	Different connector layout for Type 7
PCIE_TX16+	D52	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 16
PCIE_TX16-	D53				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX0±
PCIE_RX16+	C52	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 16
PCIE_RX16-	C53					These are the same lines as Type 7 PEG_RX0±
PCIE_TX17+	D55	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 17
PCIE_TX17-	D56				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX1±
PCIE_RX17+	C55	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 17
PCIE_RX17-	C56					These are the same lines as Type 7 PEG_RX1±
PCIE_TX18+	D58	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 18
PCIE_TX18-	D59				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX2±
PCIE_RX18+	C58	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 18
PCIE_RX18-	C59					These are the same lines as Type 7 PEG_RX2±
PCIE_TX19+	D61	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 19
PCIE_TX19-	D62				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX3±
PCIE_RX19+	C61	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 19
PCIE_RX19-	C62					These are the same lines as Type 7 PEG_RX3±
PCIE_TX20+	D65	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 20
PCIE_TX20-	D66				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX4±
PCIE_RX20+	C65	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 20
PCIE_RX20-	C66					These are the same lines as Type 7 PEG_RX4±
PCIE_TX21+	D68	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 21
PCIE_TX21-	D69				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX5±
PCIE_RX21+	C68	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 21
PCIE_RX21-	C69					These are the same lines as Type 7 PEG_RX5±
PCIE_TX22+	D71	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 22
PCIE_TX22-	D72				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX6±
PCIE_RX22+	C71	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 22
PCIE_RX22-	C72					These are the same lines as Type 7 PEG_RX6±
PCIE_TX23+	D74	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 23
PCIE_TX23-	D75				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX7±

PCIE_RX23+	C74	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 23
PCIE_RX23-	C75					These are the same lines as Type 7 PEG_RX7±
PCIE_TX24+	D78	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 24
PCIE_TX24-	D79				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX8±
PCIE_RX24+	C78	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 24
PCIE_RX24-	C79					These are the same lines as Type 7 PEG_RX8±
PCIE_TX25+	D81	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 25
PCIE_TX25-	D82				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX9±
PCIE_RX25+	C81	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 25
PCIE_RX25-	C82					These are the same lines as Type 7 PEG_RX9±
PCIE_TX26+	D85	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 26
PCIE_TX26-	D86				N.C.	These are the same lines as Type 7 PEG_TX10±
PCIE_RX26+	C85	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 26
PCIE_RX26-	C86				N.C.	These are the same lines as Type 7 PEG_RX10±
PCIE_TX27+	D88	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 27
PCIE_TX27-	D89				N.C.	These are the same lines as Type 7 PEG_TX11±
PCIE_RX27+	C88	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 27
PCIE_RX27-	C89				N.C.	These are the same lines as Type 7 PEG_RX11±
PCIE_TX28+	D91	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 28
PCIE_TX28-	D92				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX12±
PCIE_RX28+	C91	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 28
PCIE_RX28-	C92					These are the same lines as Type 7 PEG_RX12±
PCIE_TX29+	D94	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 29
PCIE_TX29-	D95				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX13±
PCIE_RX29+	C94	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 29
PCIE_RX29-	C95					These are the same lines as Type 7 PEG_RX13±
PCIE_TX30+	D98	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 30
PCIE_TX30-	D99				N.C.	These are the same lines as Type 7 PEG_TX14±
PCIE_RX30+	C98	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 30
PCIE_RX30-	C99				N.C.	These are the same lines as Type 7 PEG_RX14±
PCIE_TX31+	D101	O PCIE	AC coupled on Module		N.C.	PCI Express Differential Transmit Pairs 31
PCIE_TX31-	D102				N.C.	These are the same lines as Type 7 PEG_TX15±
PCIE_RX31+	C101	I PCIE	AC coupled off Module		N.C.	PCI Express Differential Receive Pairs 31
PCIE_RX31-	C102				N.C.	These are the same lines as Type 7 PEG_RX15±
PCIE_CLK_REF+	A88	O PCIE	PCIE			Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE_CLK_REF-	A89					

USB Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
USB0+	A46	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channels 0. For type 7 only, USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 1.
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 2.
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 3.
USB3-	B42					

USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	IPU 20KΩ RSV PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	IPU 20KΩ RSV PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4	O PCIE	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	D3				AC Coupling capacitor	
USB_SSRX0+	C4	I PCIE	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	C3					
USB_SSTX1+	D7	O PCIE	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	D6				AC Coupling capacitor	
USB_SSRX1+	C7	I PCIE	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	C6					
USB_SSTX2+	D10	O PCIE	AC coupled on Module		N.C.	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2-	D9				N.C.	
USB_SSRX2+	C10	I PCIE	AC coupled off Module		N.C.	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9				N.C.	
USB_SSTX3+	D13	O PCIE	AC coupled on Module		N.C.	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3-	D12				N.C.	
USB_SSRX3+	C13	I PCIE	AC coupled off Module		N.C.	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12				N.C.	
USB0_HOST_PRSNT	B48	I COMS	3.3V Suspend/3.3V		N.C.	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.

LPC Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD (LPC mode)	Module Base Specification R3.0
LPC_AD0	B4	I/O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V			LPC multiplexed address, command and data bus.
LPC_AD1	B5					
LPC_AD2	B6					
LPC_AD3	B7					
LPC_FRAME#	B3	O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V			LPC frame indicates the start of an LPC cycle
LPC_DRQ0#	B8	I CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V		PU 10KΩ to 3.3V	LPC serial DMA request
LPC_DRQ1#	B9				PU 10KΩ to 3.3V	
LPC_SERIRQ	A50	I/O CMOS O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	LPC_SERIRQ : PU 8.2K to 3.3V	PU 10KΩ to 3.3V	LPC serial interrupt
LPC_CLK	B10	O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	series 22Ω resistor	series 22Ω resistor	LPC clock output - 33MHz nominal

SUS_STAT#	B18	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 1.8V		IPU 20KΩ to 3V3 Suspend.	SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.
BIOS_DIS0#	A34	I CMOS	NA	PU 10K to 3V3 Suspend.	PU 10KΩ to 3V3 Suspend.	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to 4.13 for strapping options of BIOS disable signals.
BIOS_DIS1#	B88			PU 10K to 3V3 Suspend.	PU 10KΩ to 3V3 Suspend.	

SPI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 (SPI_3VDU) PU/PD	Module Base Specification R3.0
SPI_CS#	B97	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V	Series resistor 33Ω	Series resistor 33Ω	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.

General Purpose Serial Interface Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
SER0_TX	A98	O CMOS-T	5V/12V			General purpose serial port 0 transmitter
SER0_RX	A99	I CMOS-T	5V/12V		PU 10KΩ to 3.3V & isolate by Diode	General purpose serial port 0 receiver
SER1_TX / CAN_TX	A101	O CMOS-T	5V/12V 3.3V/12V			General purpose serial port 1 transmitter CAN TX output for CAN Bus channel 0.
SER1_RX / CAN_RX	A102	I CMOS-T	5V/12V 3.3V/12V		PU 10KΩ to 3.3V & isolate by Diode	General purpose serial port 1 receiver RX input for CAN Bus channel 0.

I2C Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose I2C port data I/O line

Miscellaneous Signal Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
SPKR	B32	O CMOS	3.3V / 3.3V			Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V		PD 100KΩ to GND.	Output indicating that a watchdog time-out event has occurred.
FAN_PWMOUT	B101	O OD CMOS	3.3V / 12V		RSV PD 100KΩ to GND	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
FAN_TACHIN	B102	I OD CMOS	3.3V / 12V	PU 47KΩ to 3.3V	PU 47KΩ to 3.3V	Fan tachometer input for a fan with a two pulse output.
TPM_PP	A96	I CMOS	3.3V / 3.3V	PD to GND.	PD 100KΩ to GND.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.

Power and System Management Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU to 3.3V	PU to 3.3V	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend / 3.3V			Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend		General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes. In a type 7 system, BATLOW# can be used as a power fail indication.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	PU 47KΩ to 3.3V Suspend & isolate by Diode	LID switch. Low active signal used by the ACPI operating system for a LID switch.
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	PU 47KΩ to 3.3V Suspend & isolate by Diode	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.

Rapid Shutdown Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
RAPID_SHUTDOWN	C67	I CMOS	5.0V Suspend / 5.0V			Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.

Thermal Protection Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
THRM#	B35	I CMOS	3.3V / 3.3V		IPU 10KΩ to 3.3V	Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V			Active low output indicating that the CPU has entered thermal shutdown.

SMBUS Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional clock line.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V		PU 2.2KΩ to 3.3V Suspend	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

GPIO Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
GPO0	A93	O CMOS	3.3V / 3.3V			General purpose output pins. Upon a hardware reset, these outputs **should** be low.
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	3.3V / 3.3V		PU 47KΩ to 3.3V	General purpose input pins. Pulled high internally on the Module.
GPI1	A63				PU 47KΩ to 3.3V	
GPI2	A67				PU 47KΩ to 3.3V	
GPI3	A85				PU 47KΩ to 3.3V	

Power and GND Signal Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD	Module Base Specification R3.0
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.

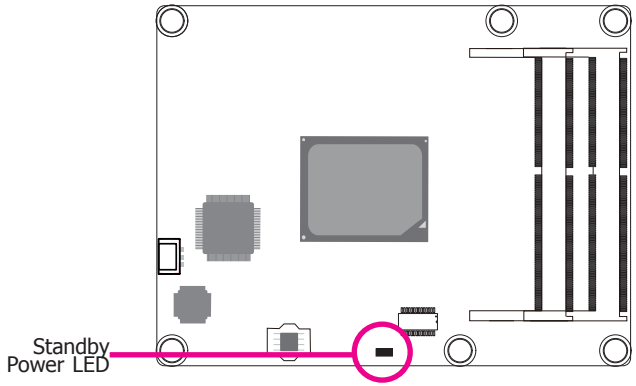
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A90, A100, A110, B1, B11, B21 ,B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110, C1, C2, C5, C8, C11, C14, C18, C21, C25, C28, C31, C41, C44, C48, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D18, D21, D25, D28, D31, D41, D44, D48, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103,	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.

Module type Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	DV970 PU/PD (T7)	Module Base Specification R3.0
TYPE0#	C54	PDS			PD 0Ω to GND	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X). TYPE2# TYPE1# TYPE0# X X X pin out Type 1 (deprecated) NC NC NC pin out Type 2 (deprecated) NC NC GND pin out Type 3 (no IDE) (deprecated) NC GND NC pin out Type 4 (no PCI) (deprecated) NC GND GND pin out Type 5 (no IDE、PCI) (deprecated) GND NC NC pin out Type 6 (no IDE, no PCI) GND NC GND pin out Type 7 * The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.
TYPE1#	C57	PDS			N.C.	
TYPE2#	D57	PDS			PD 0Ω to GND	

TYPE10#	A97	PDS			N.C.	Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0 or a Rev 2.0/3.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47K resistor 12V Pin-out R1.0 This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. In R3.0 this pin is defined as a no connect for types 6 and 7. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. R3.0 Module types 6 and 7 will no connect this pin. Type 10 Modules shall pull this pin to ground through a 47K resistor.

Standby Power LED



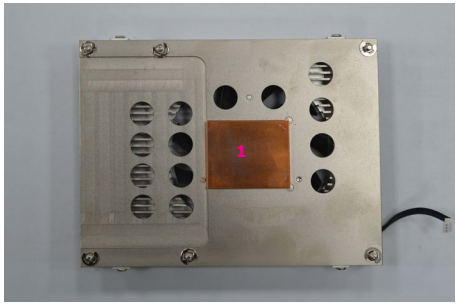
This LED will be red when module board has suspend power rail.

Cooling Option

Heat Sink with Fan

Note:
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

Top View of the Heat Sink



Bottom View of the Heat Sink

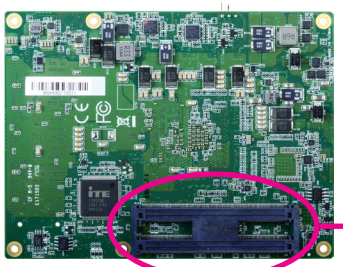
- "1" denotes the location of the thermal pad designed to contact the corresponding components on DV970.

Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto DV970.

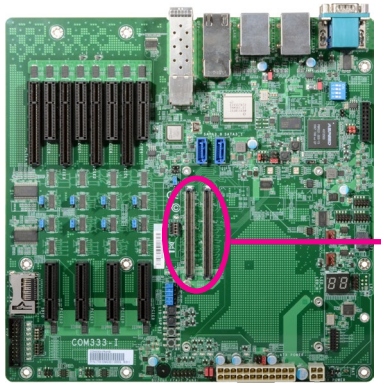
Installing DV970 onto a Carrier Board

Important:
The carrier board used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install DV970 onto the carrier board of your choice.

1. Grasp DV970 by its edges and position it on top of the carrier board with its mounting holes aligned with the standoffs on the carrier board. This helps align the COM Express connectors of the two boards to each other.

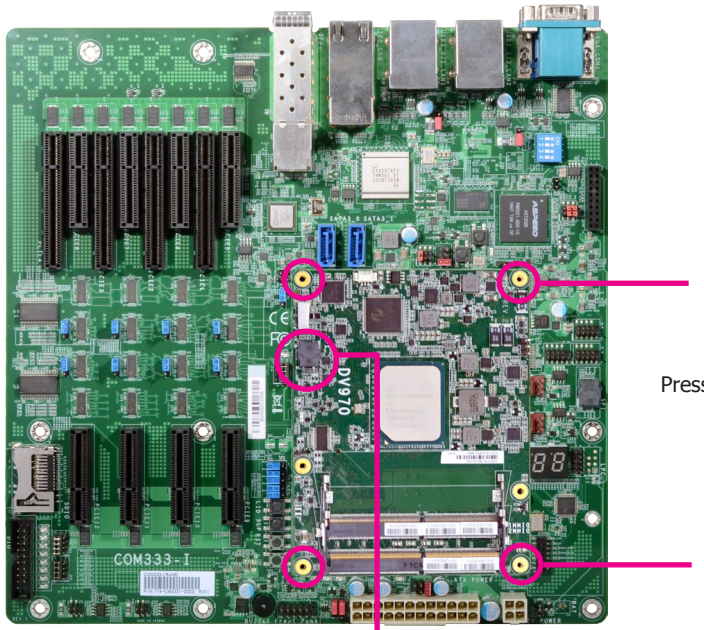


COM Express connectors on DV970



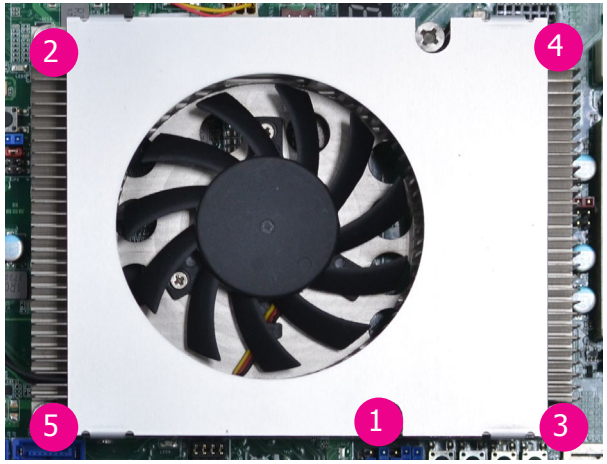
COM Express connectors on the carrier board

2. Apply firm even pressure to the side with the connectors first and push down the entire board. You will hear a "click", indicating the module is correctly seated in the COM Express connectors of the carrier board.



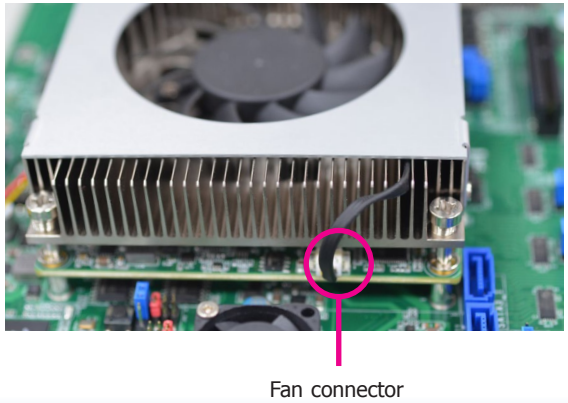
Note:
The illustrations above show the pressing points of the module onto the carrier board. Be careful when pressing the module, it may damage the socket.

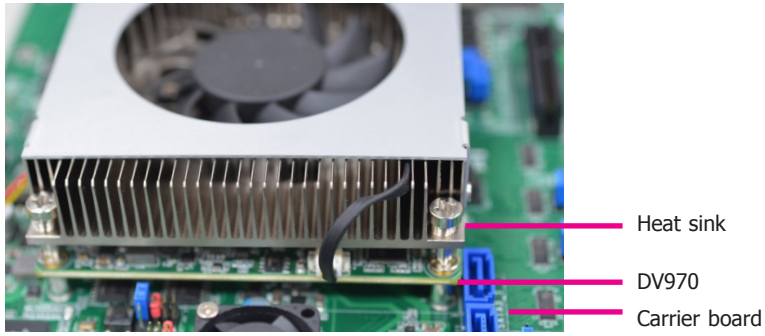
3. Install a heat sink onto the DV970 with the carrier board. First align the mounting holes of the heat sink with the mounting holes of the module.



Note:
Install the heat sink according to the sequence of the screws shown in the image above to avoid damage to the CPU.

4. Connect the heat sink and fan's cable to the fan connector on DV970.





Side View of the Heat sink, Module, and Carrier Board

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.
It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are key-board commands. The commands are available on the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
F1	Help
<Esc>	Exit
Up and Down Arrows	Select Item
Right and Left Arrows	Select Item
<F5>/<F6>	Change Values
<Enter>	Select ▶ Submenu
<F9>	Setup Defaults
<F10>	Save and Exit

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

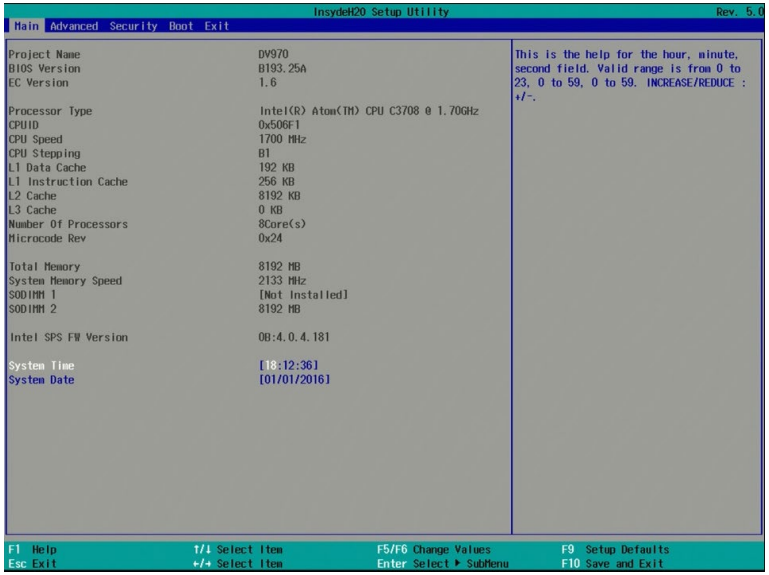
Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

Insyde BIOS Setup Utility

Main

The Main menu is the first screen that you will see when you enter the BIOS setup utility.



System Date

The date format is <month>, <date>, <year>. Day displays a day, from Sunday to Saturday. Month displays the month, from January to December. Date displays the date, from 1 to 31. Year displays the year, from 1980 to 2099.

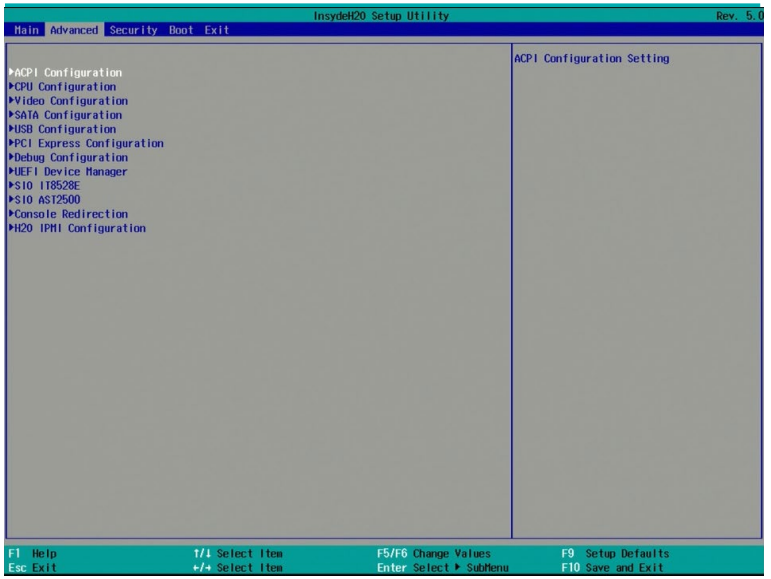
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

Advanced

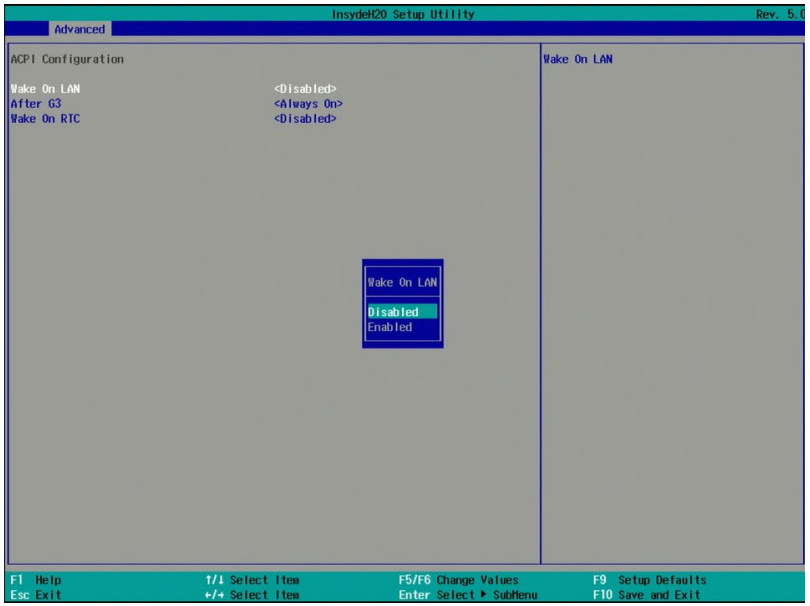
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



ACPI Settings

This section configures the system's ACPI settings.



Wake on LAN

Enable or disable the use of LAN signals to wake up the system.

After G3

Specify which state the system should be in when power is re-applied after a power failure (G3, the mechanical-off, state).

Always On The system is powered on.

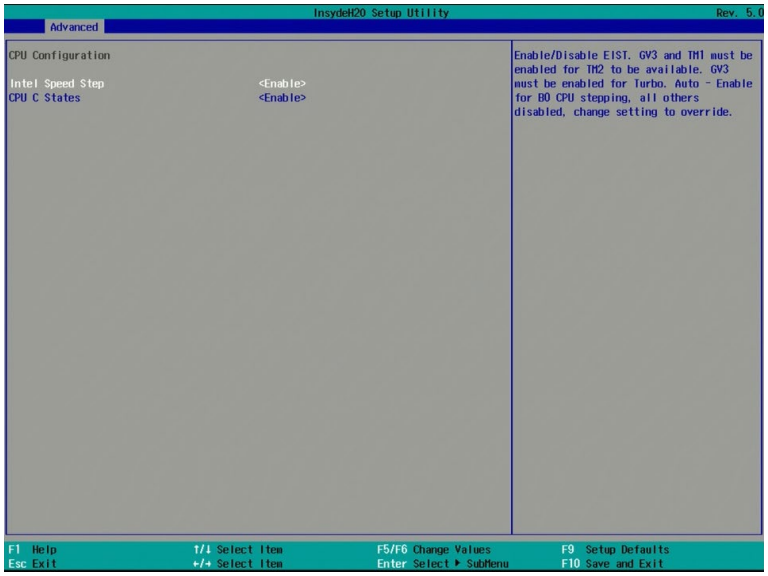
Always Off The system is powered off.

Wake on RTC

Automatically power the system on at a particular time every day from the real-time clock battery. Specify the wake up time of the day below: <hour>, <minute>, <second>.

CPU Configuration

This section configures the CPU.



Intel® SpeedStep™

Enable or disable the Enhanced Intel® SpeedStep™ Technology, which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, you can take advantage of its offering by setting power schemes from the operating system's power options.

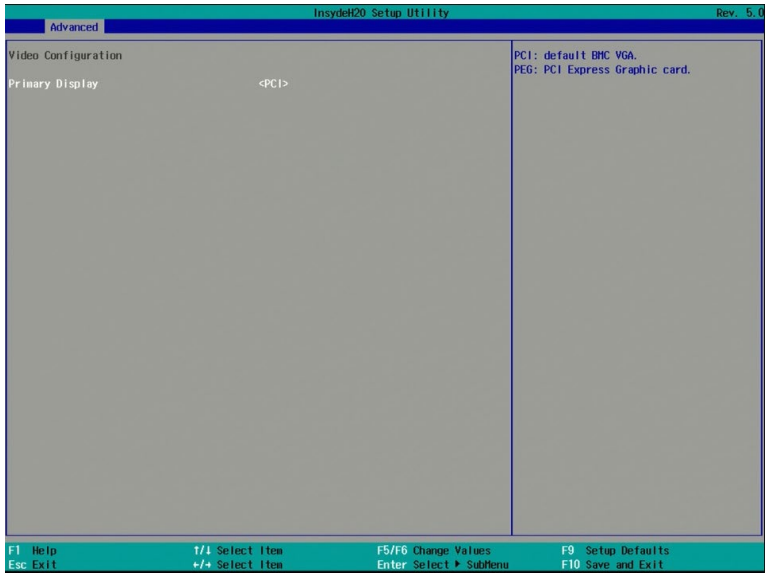
CPU C States

Enable or disable CPU power management. It allows the CPU to go to C states when it's not 100% utilized.

Note:
For some Linux-based operating systems such as Debian, CentOS, Ubuntu, you may need to set "CPU C States" to "disabled" before installation.

Video Configuration

This section configures video settings.



Primary Display

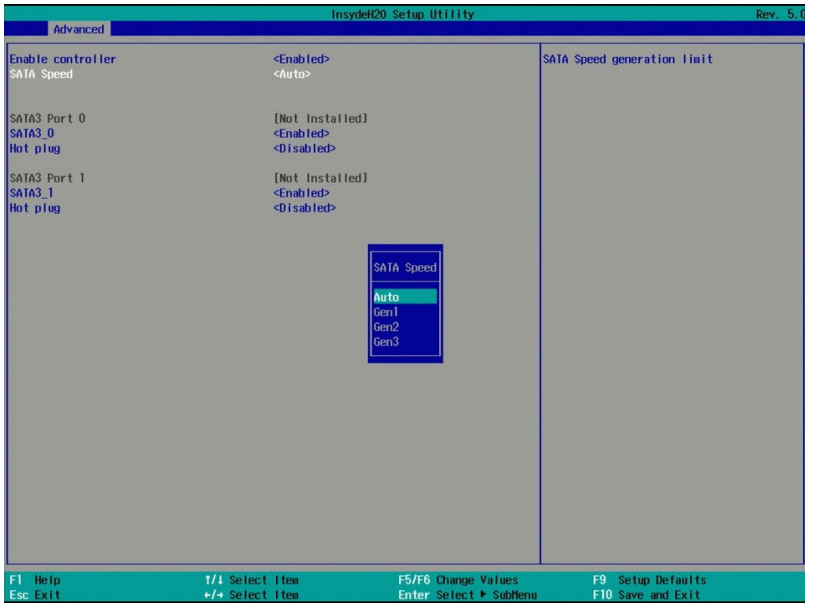
Select the primary display for the system. The options are PCI (the default BMC VGA) and PEG (PCIe graphics card). The order of video device initialization will be as follows:

PCI (default): PCI graphics device -> PCIe graphics device

PEG: PCIe graphics device -> PCI graphics device

SATA Configuration

This section configures SATA controllers.



SATA Controller(s)

Enable or disable Serial ATA devices.

SATA Speed

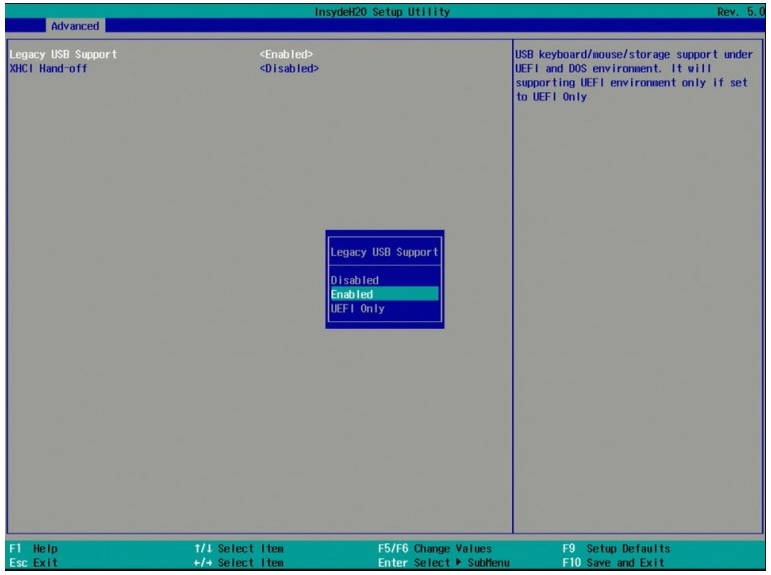
Select Serial ATA device speed: Gen1 (1.5 Gbit/s), Gen2 (3 Gbit/s), Gen 3 (6 Gbit/s) or auto.

SATA3_0, SATA3_1 and Hot Plug

Enable or disable each Serial ATA port and its hot plug function.

USB Configuration

This section configures the parameters of the USB devices.



Legacy USB Support

Disabled

Disable USB keyboard/mouse/storage support.

Enabled

Enable USB keyboard/mouse/storage support under UEFI and DOS environment.

UEFI Only

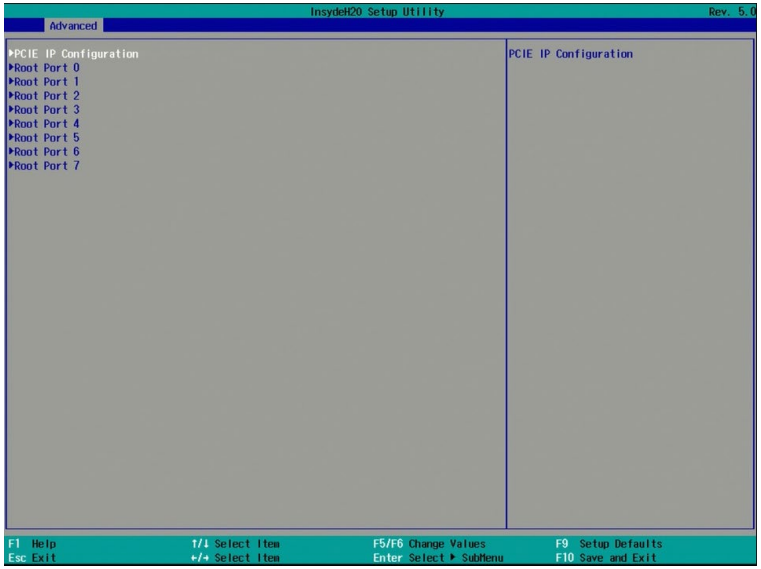
Enable USB keyboard/mouse/storage support only under UEFI environment.

XHCI Hand-off

Set this option to disabled if the operating system supports xHCI hand-off (i.e. more recent versions of Windows) and enabled if the operating system does not support xHCI hand-off (i.e. older versions of Windows).

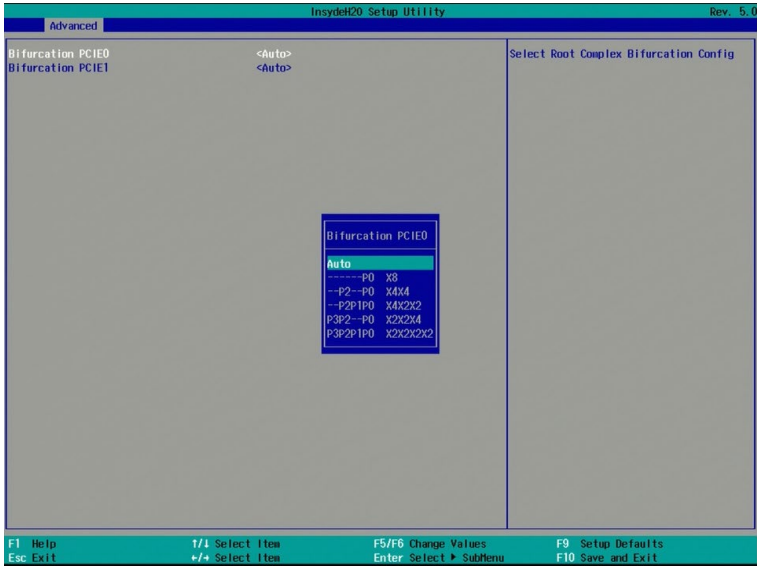
PCI Express Configuration

This section configures the settings of the PCIe root ports.



PCIE IP Configuration

This section configures PCIe lanes.



Bifurcation PCIE0/PCIE1

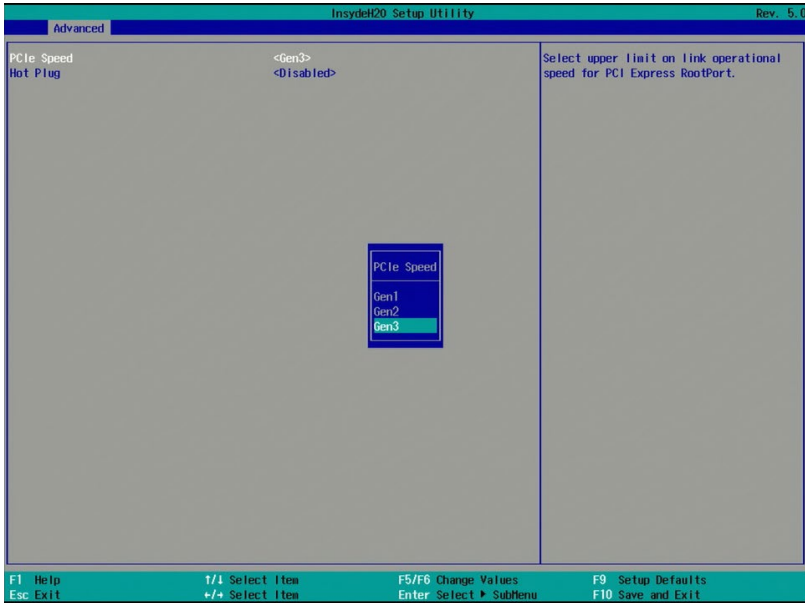
The PCIE bifurcation method allows you to split a PCIE lane into multiple lanes by dividing its bandwidth.

The options are as follows for PCIE0 and PCIE1:

Auto: P0.....x8 (the default setting for SKU 100G)
P2, P0.....x4, x4
P2, P1, P0.....x4, x2, x2
P3, P2, , P0.....x2, x2, x4
P3, P2, P1, P0.....x2, x2, x2, x2 (the default setting for SKUs 000G/200G/300G)

PCI Express Root Port Configuration

This section configures the PCI Express root ports.



PCIe Speed

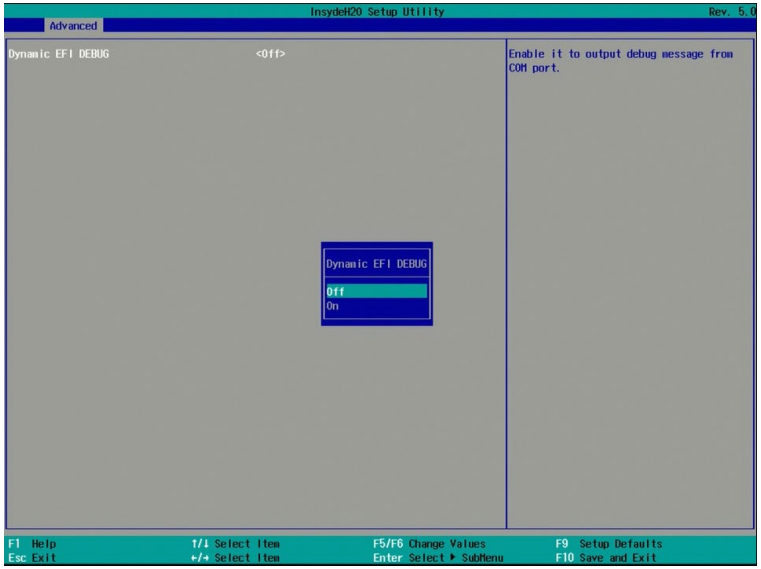
Select the speed of the PCI Express Root Port: Auto, Gen1 (2.5 GT/s), Gen2 (5.0 GT/s) or Gen3 (8.0 GT/s).

Hot Plug

Enable or disable the hot plug function of each PCI Express root port.

Debug Configuration

This section configures the debug function.

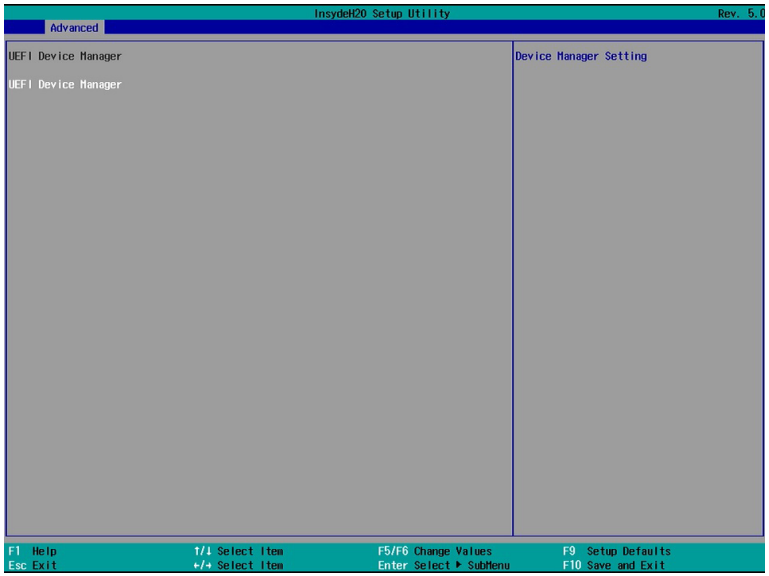


Dynamic EFI Debug

Enable or disable output of the debugging messages through a serial port. (On COM333-I carrier board, the designated serial port will be COM1 pin header.)

UEFI Device Manager

This Device Manager menu is used to configure UEFI network settings when the "Network Stack" is enabled in the "Dual" or "UEFI" boot mode. Refer to the "Boot" section in this chapter. After this function is selected, the screen will warn you that you are going to exit the BIOS setup utility.

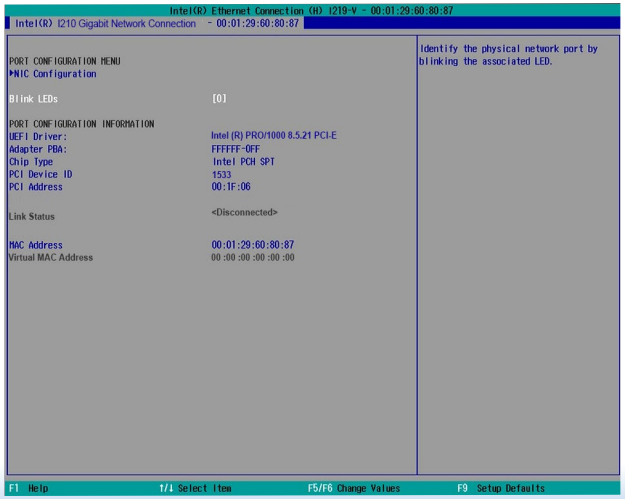


Network Device List

The "Device Manager" screen is displayed. And if the "Network Stack" option is enabled from the "Boot" menu, the "Network Device List" should be shown in the "Device list". Select "Network Device List" to view all of the detected network devices. For each network device, you can select to view and configure its settings. In addition, you can select either the IPv4 or IPv6 network settings for UEFI network configuration.

NIC Configuration Menu

This screen shows hardware information for the Ethernet controllers and configures their operation.



Blink LEDs

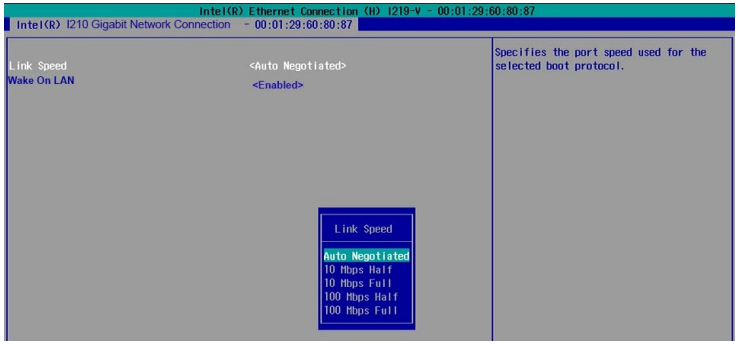
Enter the duration (seconds) to blink the Ethernet port's LED to indicate its presence.

NIC Configuration

This screen configures the Ethernet controller. Select the link speed from the following options: Auto Negotiated, 10Mbps Half, 10Mbps Full, 100Mbps Half, and 100Mbps Full.

Wake on LAN

Enable or disable the wake-on-LAN function for this network device.



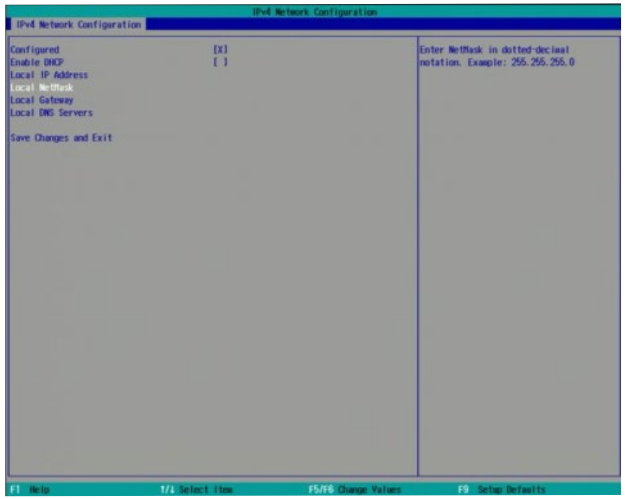
IPv4 Network Configuration

This screen configures the IP addressing method (DHCP or static IP). For static IP addressing, configure the following:

Local IP address and subnet mask: Enter the IP address in the IPv4 format: x . x . x . x (x must be a decimal value between 0 and 255).

Local Gateway: Enter the gateway address in the IPv4 format.

Local DNS (Domain Name System) Servers: Enter DNS (Domain Name System) server IP addresses in the IPv4 format.



IPv6 Network Configuration

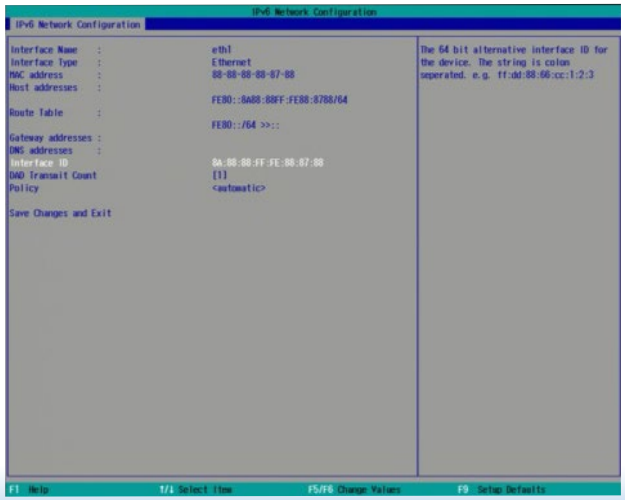
If you select to use IPv6 network settings, enter the Interface ID (64 bit).
Policy: Select either automatic or manual. And select "Advanced Configuration" to configure IPv6 network address manually if the manual option is selected.

New IPv6 address: Enter the IP address in the IPv6 format:

x : x : x : x : x : x : x : x (x can be any hexadecimal value between 0 and FFFF). Place a space to separate each IP address to enter more than one address.

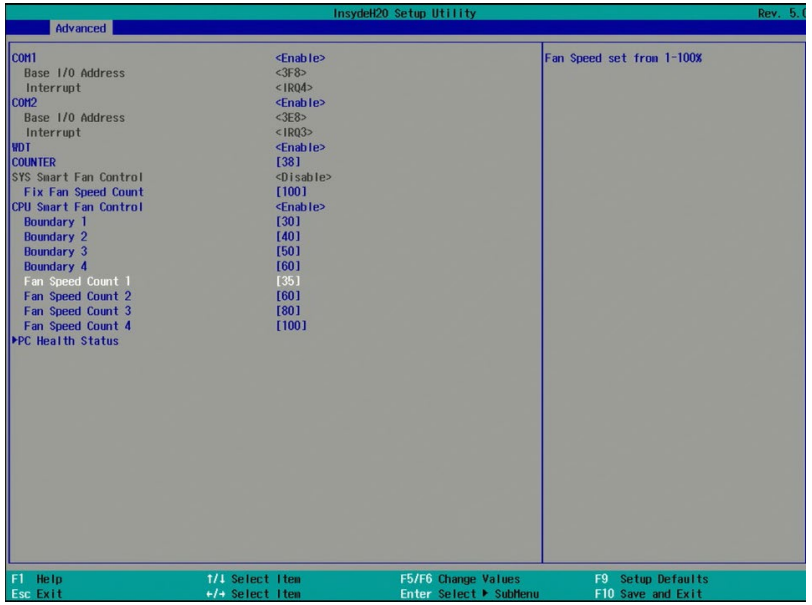
New Gateway addresses: Enter gateway addresses in the IPv6 format.

New DNS addresses: Enter DNS (Domain Name System) server IP addresses in the IPv6 format.



SIO IT8528E

This section configures the parameters of the system's super I/O chip IT8528E.



COM Port 1 and COM Port 2

Enable or disable each serial port. The screen also shows the base I/O address and IRQ assignment of each port.

WDT

Enable or disable the watchdog function. A counter will appear if you select to enable WDT. Input any value between 1 and 255.

SYS Fix Fan Speed Count

Set the fan speed. The range is from 1 (lowest speed)-100% (full speed).

CPU Smart Fan Control

Enable or disable the system or CPU smart fan.

Boundary 1 to Boundary 4

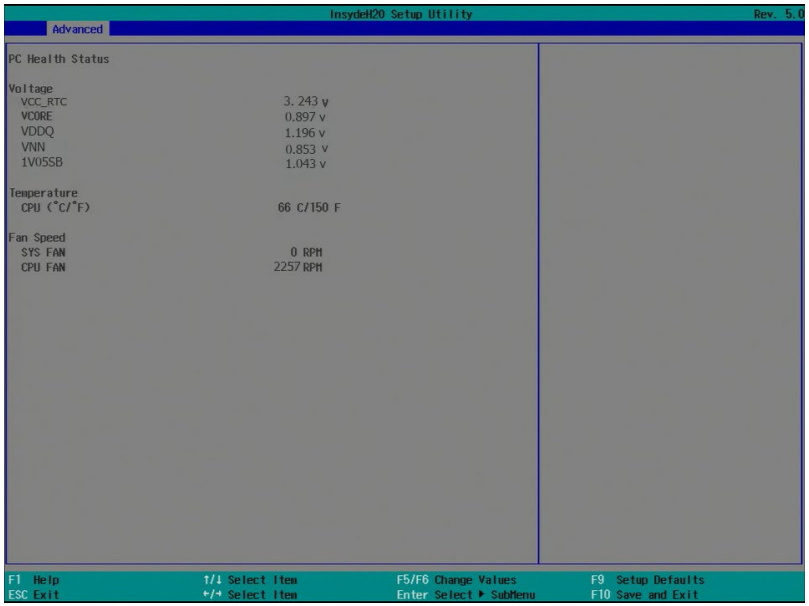
Set the boundary temperatures that determine the operation of the fan with different fan speeds accordingly. For example, when the system or the CPU temperature reaches boundary temperature 1, the system or CPU fan should be turned on and operate at the designated speed. The range of the temperature is from 0 to 127°C.

Fan Speed Count 1 to Fan Speed Count 4

Set the fan speed. The range is from 1 (lowest speed)-100% (full speed).

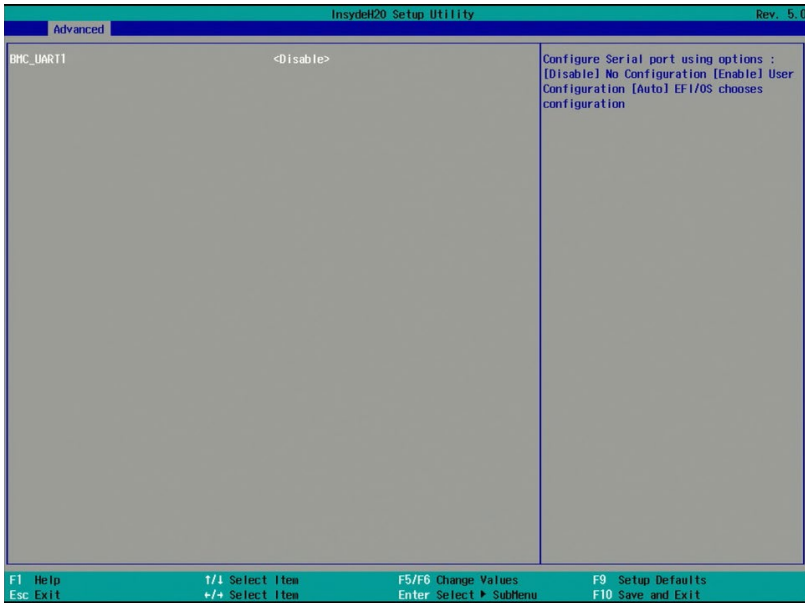
PC Health Status

This section displays PC health status.



SIO AST2500

This section configures the parameters of the system's super I/O chip AST2500.

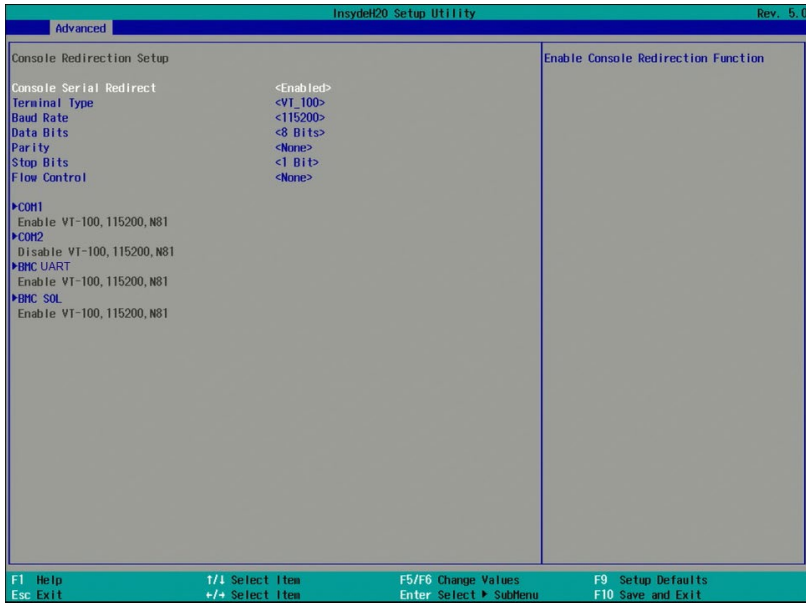


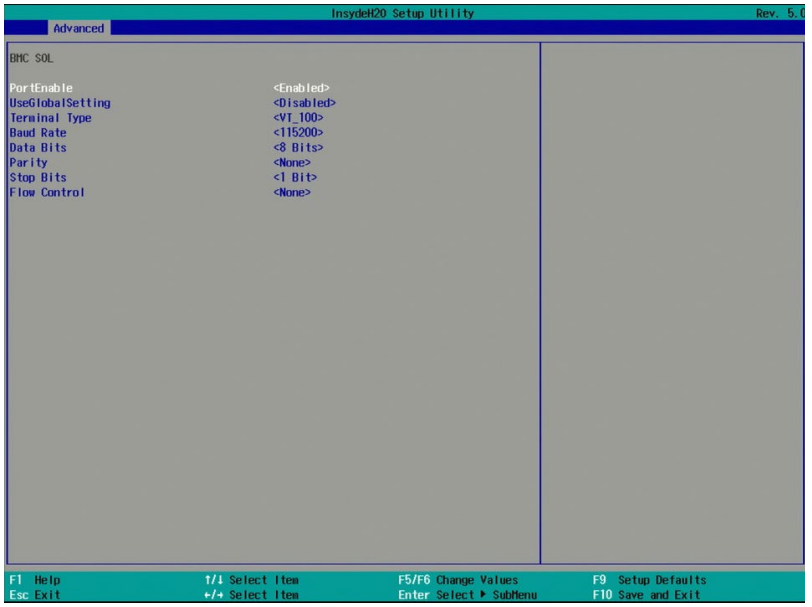
BMC_UART1

Enable or disable BMC UART1 port.

Console Redirection

Console redirection lets you monitor and control the system from a remote station by re-directing the host screen output through a serial port.





Console Serial Redirect

Enable or disable the console redirection function. (The default is disabled.) If you select to enable it, please configure the following parameters for serial communication between the system and a remote station:

Terminal type: VT_100, VT_100+, VT_UTF8, or PC_ANSI.

Baud rate: 115200, 57600, 38400, 19200, 9600, 4800, 2400 or 1200.

Data bits: 8 bits or 7 bits.

Parity: None, Even or Odd.

Stop bits: 1 bit or 2 bits.

Flow control: None, RTS/CTS or XON/XOFF

This above settings are global and can be used for all of the designated serial ports for console redirection.

COM 1/COM 2/BMC UART/BMC SOL

Enable or disable console redirection for COM 1, COM 2, BMC UART and BMC serial-over-LAN port. If you select to enable it, please choose to use the global setting or configure the following parameters for serial communication between the system and a remote station:

Terminal type: VT_100, VT_100+, VT_UTF8, or PC_ANSI.

Baud rate: 115200, 57600, 38400, 19200, 9600, 4800, 2400 or 1200.

Data bits: 8 bits or 7 bits.

Parity: None, Even or Odd.

Stop bits: 1 bit or 2 bits.

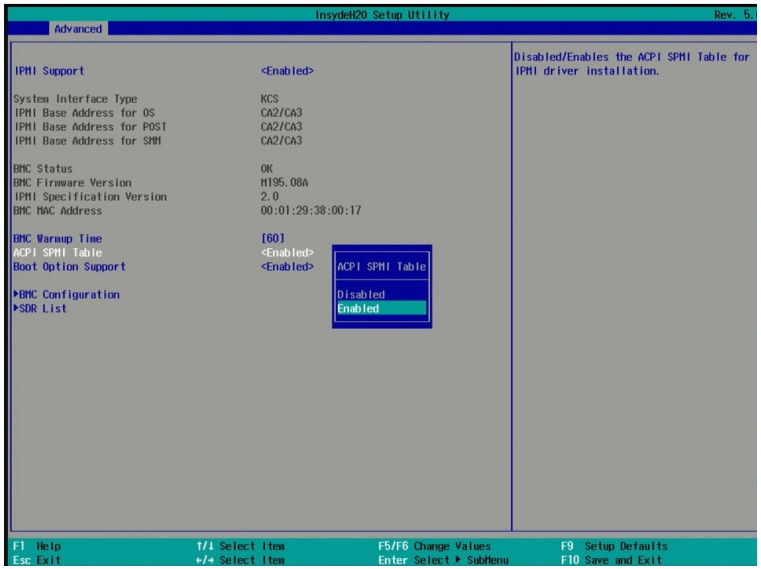
Flow control: None, RTS/CTS or XON/XOFF

UseGlobalSetting

Enable this option to use the global setting from previous menu without the need to configure each port individually for console redirection.

H2O IPMI Configuration

This section configures Intelligent Platform Management Interface (IPMI) settings.



IPMI Support

Enable or disable the support for IPMI. The default is disabled.

The screwn also lists BMC (Baseboard Management Controller) related information such as firmware version and status.

BMC Warmup Time

Select the time needed for the BMC to power on and start functioning. The valid range is from 0 to 240 seconds.

ACPI SPMI Table

Enable or disable the ACPI SPMI Table for installing IPMI drivers.

Boot Option Support

Enable or disable the display of IPMI options at startup.

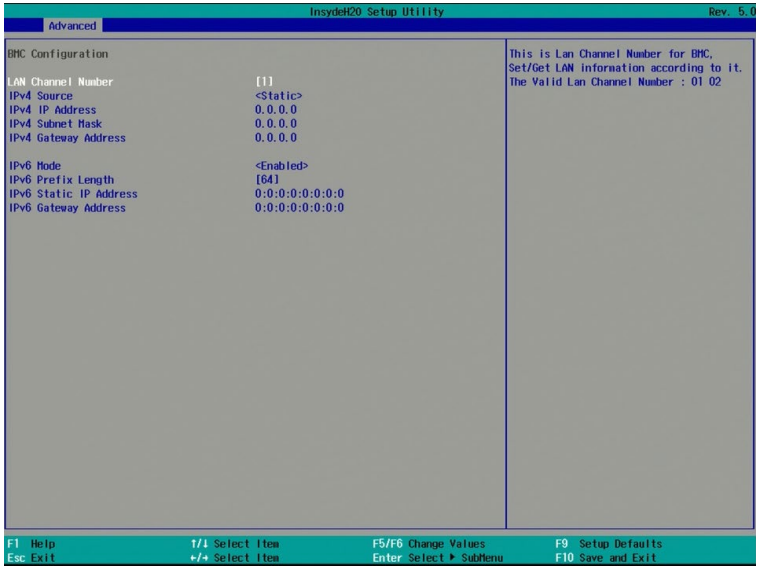
BMC Configuration

Configure the BMC functions.

SDR List

BMC Configuration

This section configures BMC (Baseboard Management Controller) settings.



LAN Channel Number

Select the channel number for the onboard BMC: 01 or 02. Channel 01 is designated as the LAN I210 Port (LAN 1 port on the COM 333-I carrier board) whereas Channel 02 is designated as the BMC management PORT (MGMT_PORT on COM333-I).

IPv4 Source

Select the IP address addressing method for communicating with the BMC. If DHCP is selected, a DHCP (Dynamic Host Configuration Protocol) server in your network will automatically assign an available IP address for the system. If Static is selected, you need to assign a valid IP address as well as the following information manually:

IPv4 address and subnet mask: Enter the IP address in the IPv4 format:
x . x . x . x (x must be a decimal value between 0 and 255).

IPv4 Gateway Address: Enter the gateway address in the IPv4 format.

IPv6 Mode

Enable or disalbe IPv6 addressing scheme.

If you select to use IPv6 network settings, enter the IPv6 prefix length (enter an integer between 1 and 128; the default is 64 bit).

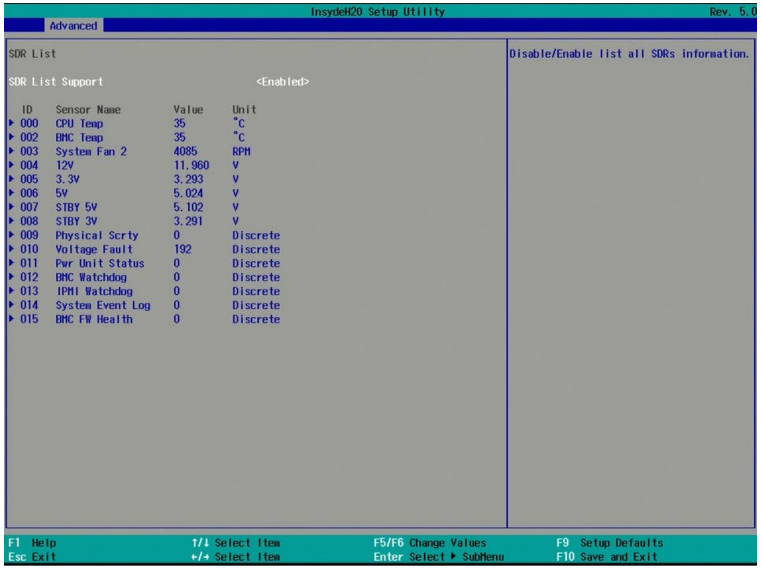
IPv6 Static address: Enter the IP address in the IPv6 format:

x : x : x : x : x : x : x : x (x can be any hexadecimal value between 0 and FFFF).

IPv6 Gateway addresses: Enter gateway addresses in the IPv6 format.

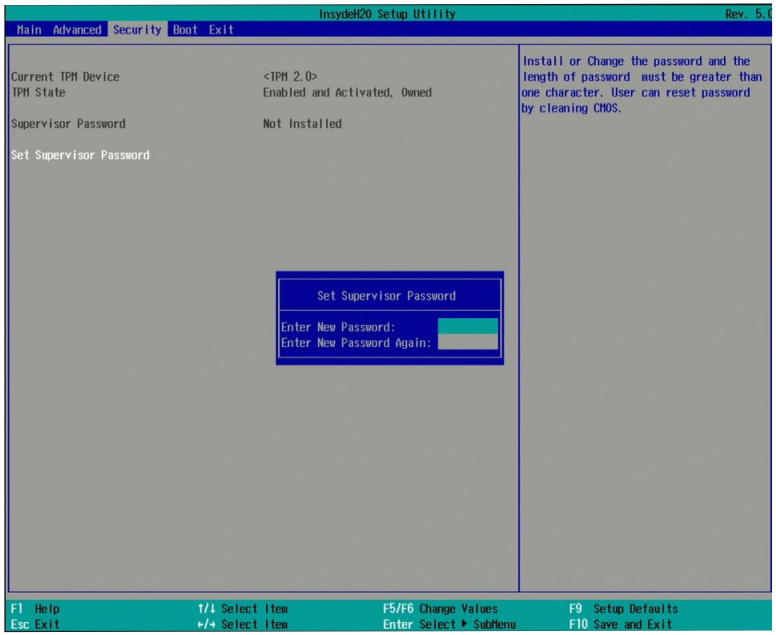
SDR List

This section lists SDR (Sensor Data Record) information.



Security

This section configures security-related settings.



TPM Availability (optional)

Show or hide TPM availability and its configurations.

TPM Operation

Select one of the supported operation: Enable, Disable, or No Operation.

No Operation: No changes to the current state.
Disable: Disable and deactivate TPM.
Enable: Enable and activate TPM.

Clear TPM

Remove all TPM ownership contents.

Set Supervisor Password

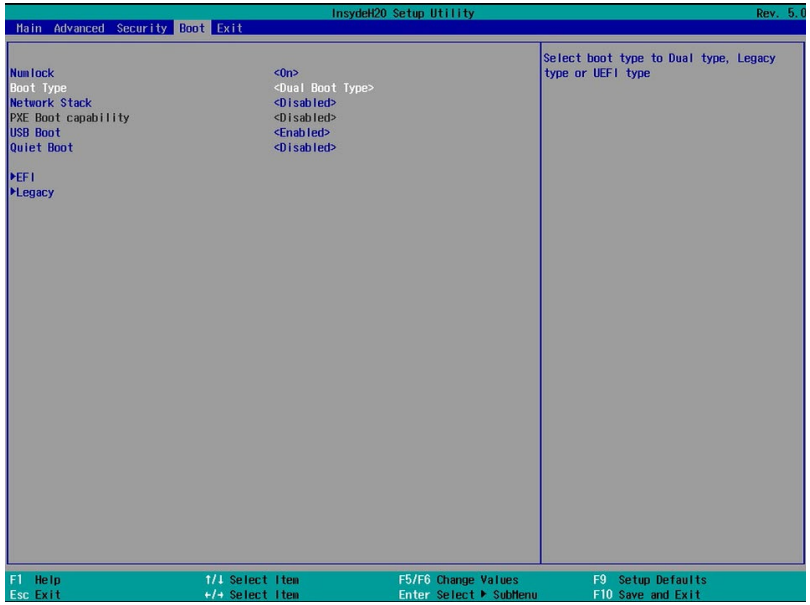
Set the administrative password for entering the BIOS setup utility or upon entering the power-on self-test (POST) process. The length of the password must be greater than 1 character and less than or equal to 10 characters.

Power-on Password

If you select to set the supervisor password, this option will be shown. Enable or disable prompt for password at system startup.

Boot

This section configures boot options.



NumLock

Select the power-on state for the Num Lock key: on or off (default).

Boot Type

Select the boot type. The options are Legacy Boot Type, UEFI Boot Type and Dual Boot Type (default).

Network Stack

This option is shown only when the boot type is set to Dual or UEFI.
Enable or disable UEFI network stack. It supports the operation of these functions or software: Windows 8 BitLocker Network Unlock, UEFI IPv4/IPv6 PXE and legacy PXE option ROM.
If this function is enabled, you can then go to "Advanced">"UEFI Device Manager" to configure network settings for network connection under the UEFI environment. The default is disabled.

PXE Boot Capability (UEFI mode) /PXE Boot to LAN (Legacy mode)

Enable or disable Preboot eXecution Environment (PXE) boot to LAN. In the UEFI or Dual boot mode, this function can only be enabled if the Network Stack support is enabled. The default is disabled.

USB Boot

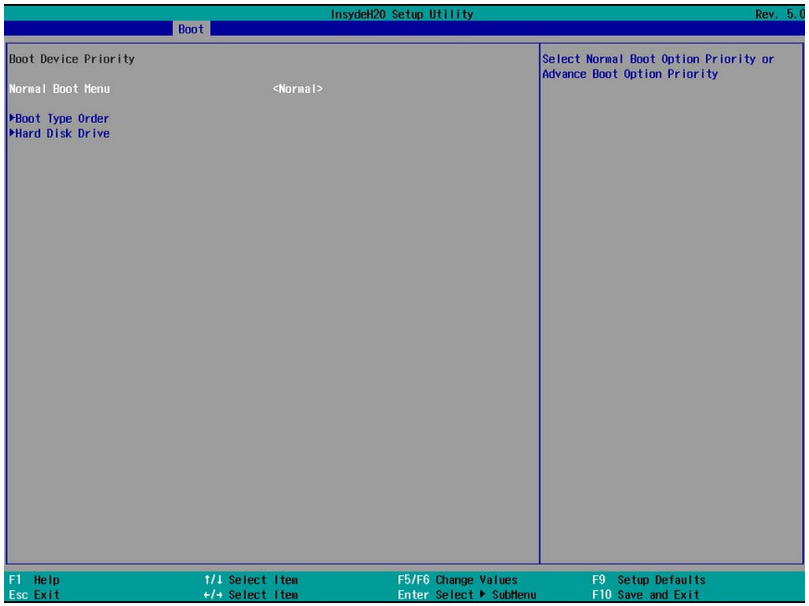
Enable this function to boot from a USB flash drive.

Quiet Boot

Enable or disable the quiet boot function to configure the screen's display between POST messages or the OEM logo at startup. Select "Disabled (default)" to display the POST messages and select Enabled to display the OEM logo.

Boot Device Priority

This section configures legacy or EFI boot order or both depending on the "Boot Type" selected.



EFI Boot Menu

Use + and - keys to rearrange the priority list for boot devices.

Legacy Boot Menu

Normal

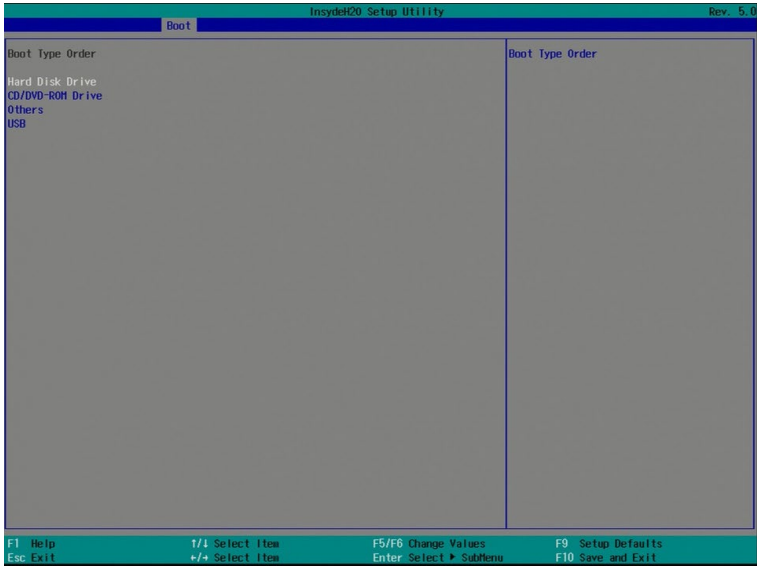
For this option, determine the boot order for the devices within each category. Use the + and - key to arrange the priority of the boot type devices in the list. The first device in the list has the highest boot priority.

Advance

For this option, determine the boot order for all bootable devices. Use + and - keys to arrange the priority of the detected boot devices in the list. The first device in the list has the highest boot priority.

Exit

This section configures options for exiting the BIOS setup utility.



Exit Saving Changes

Select this field and press <Enter> to exit BIOS setup and save your changes.

Load Optimal Defaults

Select this field and press <Enter> to load the optimal defaults.

Discard Changes

Select this field and press <Enter>to exit the BIOS setup without saving your changes.

Save Setting to file

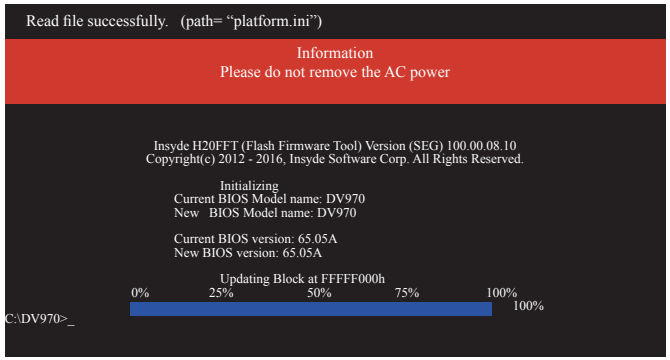
Select this option to save BIOS configuration settings to a USB drive. The operation will fail if there aren't any USB devices detected on the system. The saved configuration will have the DSF file extension and can be used for restoration.

Restore Setting from file

Select this option to restore BIOS configuration settings from a USB drive. Note that this option will not be available if there aren't any USB devices detected on the system.

Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the latest BIOS file and the firmware update utility. For instructions on how to update BIOS with the flash utility, please see https://www.dfi.com/Knowledge/Video/31 from the Knowledge Base of the DFI website.



Notice: BIOS SPI ROM

1. The Intel® Server Platform Services (SPS) has already been integrated into this system board. Due to safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.

2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.

3. If you do not follow the methods above, the Intel® Server Platform Services will not be updated and will cease to be effective.

Notes:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical personnel's instructions to confirm that the MAC address should be burned or not.

Chapter 5 - Supported Software

The system requires you to install drivers for some devices to operate properly. To download the latest driver, please go to the DFI Download Center:

https://www.dfi.com/downloadcenter

Once you are in the "Download Center" page, select your product or type the model name and click "Search" to find product-related resources such as documentation and drivers.

Drivers are available for the following devices in Windows Server 2012 & 2016:

- Intel® Chipset Device Software
- Graphics Driver (optional, ASPEED Graphics Windows WDDM Driver)
- Intel® LAN Driver

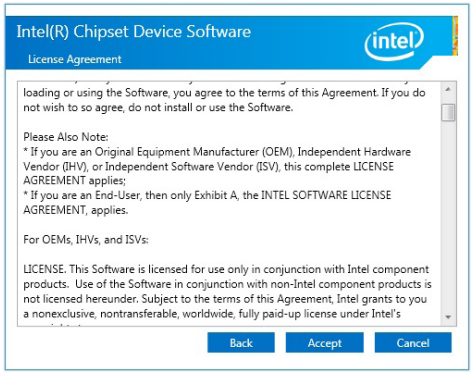
Intel Chipset Software Installation Utility

The Intel Chipset Software Installation Utility is used for updating Windows® INF files so that the Intel chipset can be recognized and configured properly in the system.

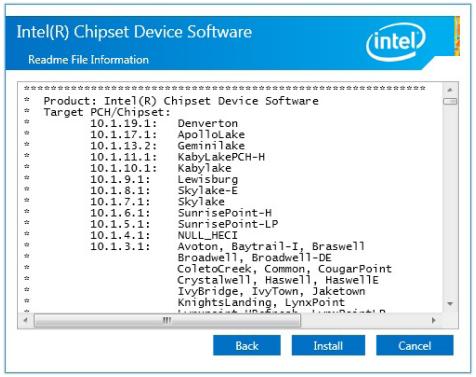
To install the utility, unzip the driver package and click the executable file in the package folder.

1. Setup is ready to install the utility. Click "Next" to continue.

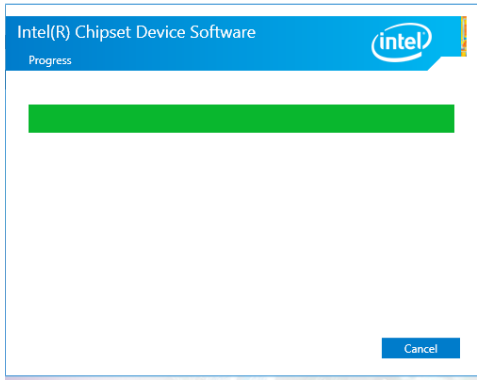
2. Read the license agreement, then click "Accept" if you accept the terms and conditions.



3. Go through the readme document for system requirements and installation tips, then click "Install".



4. Please wait while the installation is in progress.

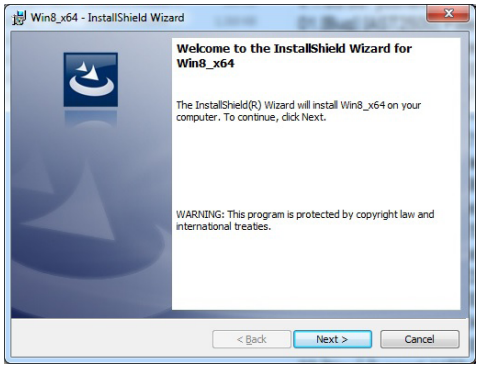


5. Click "Finish" to exit the installation utility.

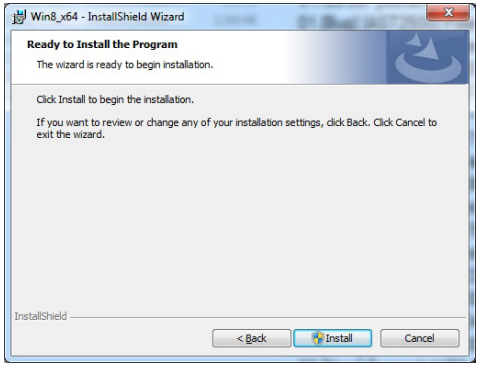
Graphics Drivers (optional)

To install the ASPEED Graphics Windows WDDM Driver, unzip the driver package and click the executable file in the package folder.

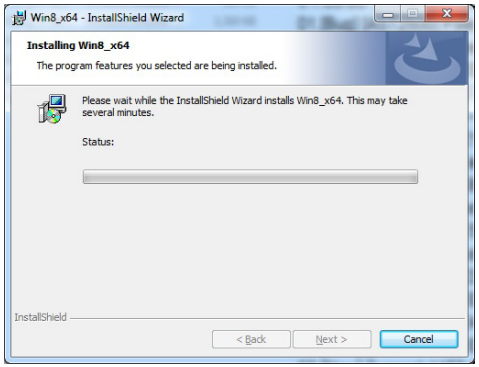
1. The welcome screen appears.



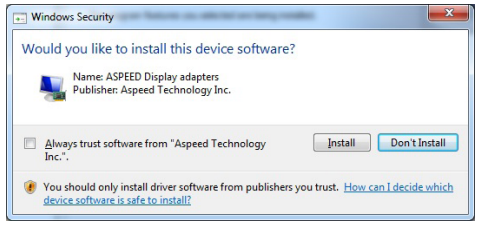
2. Setup is now ready to install the graphics driver. Click "Install" to begin the installation.



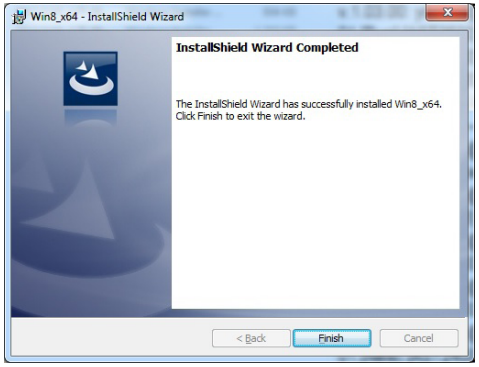
3. Please wait while the installation is in progress.



4. Click "Install" to confirm that you would like to install this device software.



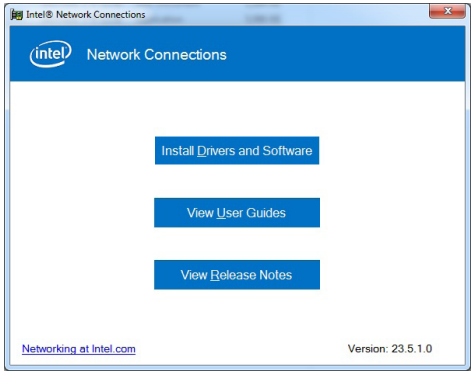
5. Click "Finish" to exit the installation utility.



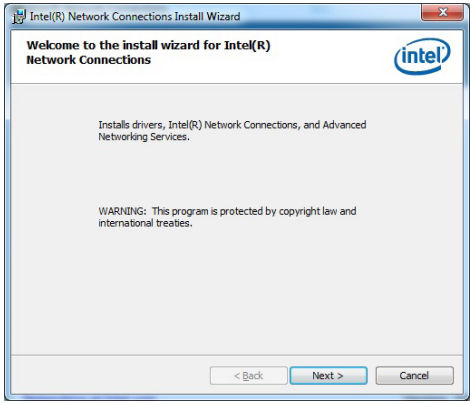
Intel LAN Drivers

To install the driver, unzip the driver package and click the executable file in the package folder.

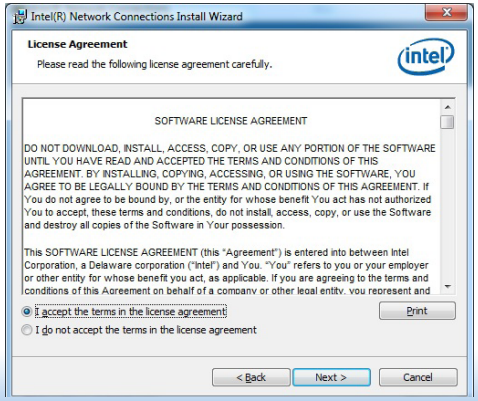
1. Setup is preparing to install the driver. Click "Install Drivers and Software" to continue.



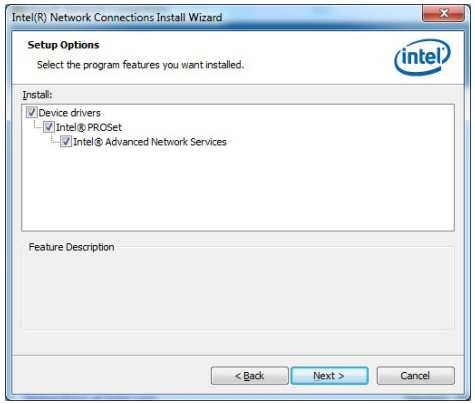
2. The welcome screen appears to inform you that Intel® network drivers and networking services will be installed.



3. Read the license agreement, then click "Next" if you accept the terms and conditions.



4. Choose the components to be installed and click "Next" to begin the installation.



5. After the installation is complete, click "Finish".