Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for IoT Applications

Datasheet, Volume 2 (Book 3 of 3)

Intel® Programmable Services Engine (Intel® PSE)

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Revision History

Revision Date	Revision Number	Description
March 2023	003	• Chapter 2, "Inter-Process Communication (IPC) Interface" — Section 2.1.22 - Updated Default & Access field for Bit Range 16 to 05h • Chapter 3, "TSN GbE Controller" — Section 3.3.2.28 - Updated Field Name and Description with 125 ps instances • Chapter 11, "Universal Asynchronous Receiver-Transmitter (UART) Interface" — Section 11.2.3 - Updated this section
September 2021	002	• Chapter 3, "TSN GbE Controller" — Section 3.2.52 - Updated field description on the register, MAC_GPIO_STATUS - Address 20Ch • Chapter 14, "Intel® PSE ARM Registers" — Section 14.20.1.51 - Updated field description on Bit19:16, MAC_GPIO_STATUS - Offset 5020020Ch — Section 14.20.3.51 - Updated field description on Bit19:16, MAC_GPIO_STATUS - Offset 5022020Ch
July 2021	001	Initial release.

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1 Introduction

The Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor is targeted towards various IoT segments, such as industrial, retail, and embedded. It features real time compute with technologies such as TSN, TCC, which are expected to drive the future of IoT.

Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor is an Intel Architecture (IA) Multi-Chip Processor (MCP) 2-Chip Package, built on a 10-nanometer Compute Die and a 14-nanometer Platform Controller Hub (PCH) into a single package. Both dies are connected via the On Package Interface (OPI).

1.1 About this Manual

This document is intended for Original Equipment Manufacturers (OEMs), Original Design Manufacturers (ODM) and BIOS vendors creating products based on the Elkhart Lake family Multi Chip Package (MCP).

Throughout this document, the name "Processor" is used as a general term and refers to all Elkhart Lake family SKUs, unless specifically noted otherwise. The compute die may be referred to simply as "Compute Die" and the Platform Controller Hub may be referred to simply as "PCH".

This manual assumes a working knowledge of the vocabulary and principles of interfaces and architectures such as PCI express* (PCIe*), Universal Serial Bus (USB), Advanced Host Controller Interface (AHCI), eXtensible Host Controller Interface (xHCI), and so forth.

This manual abbreviates PCI buses as Bn, devices as Dn and functions as Fn. For example, Device 31 Function 0 is abbreviated as D31:F0, and Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0. These numbers are shown as decimal unless otherwise indicated.

This is the core reference document for external design specifications. Information provided here takes precedence, if there are any discrepancies found in related documents.

1.2 References

Specification	Document #/Location
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for IoT Applications Datasheet Volume 1	636112
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications, Datasheet, Volume 2 (Book 1 of 3)	635255
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications, Datasheet, Volume 2 (Book 2 of 3)	636722

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2 Inter-Process Communication (IPC) Interface

2.1 IPC Configuration Registers Summary

These registers in Bus: 0, Device 29, Function 0.

Table 2-1. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4BB30000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h

Table 2-1. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

2.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4BB30000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BB3h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

2.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort

Bit Range	Default & Access	Field Name (ID): Description
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

2.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

2.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

2.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

2.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

2.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

2.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

2.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

2.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

2.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

2.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

2.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

2.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

2.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

2.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

2.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

2.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

2.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

2.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

2.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

2.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	05h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

2.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

2.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

2.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

2.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

2.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

2.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

2.2 IPC MMIO Registers Summary

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Peripheral Interrupt Status - LH2OSE (PISR_LH2OSE) - Offset 0h	00000000h
4h	4	Peripheral Interrupt Mask - LH2OSE (PIMR_LH2OSE) - Offset 4h	00000000h
8h	4	LH2OSE Peripheral Interrupt Mask (HOST_PIMR_LH2OSE) - Offset 8h	00000101h
Ch	4	LH2OSE Peripheral Interrupt Status (HOST_PISR_LH2OSE) - Offset Ch	00000000h
10h	4	LH2OSE Channel Interrupt Mask (CIM_LH2OSE) - Offset 10h	00000000h
14h	4	LH2OSE Channel Interrupt Status (CIS_LH2OSE) - Offset 14h	00000000h
34h	4	LH2OSE Firmware Status (ISH_HOST_FWSTS_LH2OSE) - Offset 34h	00000000h
38h	4	LH2OSE Communication (HOST_COMM_LH2OSE) - Offset 38h	00000000h
48h	4	Inbound DoorbellLH2OSE To ISH (HOST2ISH_DOORBELL_LH2OSE) - Offset 48h	00000000h
54h	4	Outbound DoorbellISH To LH2OSE (ISH2HOST_DOORBELL_LH2OSE) - Offset 54h	00000000h
60h	4	Outbound Inter Processor Message 1 From ISH To LH2OSE (ISH2HOST_MSG1_LH2OSE) - Offset 60h	00000000h
64h	4	Outbound Inter Processor Message 2 From ISH To LH2OSE (ISH2HOST_MSG2_LH2OSE) - Offset 64h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
68h	4	Outbound Inter Processor Message 3 From ISH To LH2OSE (ISH2HOST_MSG3_LH2OSE) - Offset 68h	00000000h
6Ch	4	Outbound Inter Processor Message 4 From ISH To LH2OSE (ISH2HOST_MSG4_LH2OSE) - Offset 6Ch	00000000h
70h	4	Outbound Inter Processor Message 5 From ISH To LH2OSE (ISH2HOST_MSG5_LH2OSE) - Offset 70h	00000000h
74h	4	Outbound Inter Processor Message 6 From ISH To LH2OSE (ISH2HOST_MSG6_LH2OSE) - Offset 74h	00000000h
78h	4	Outbound Inter Processor Message 7 From ISH To LH2OSE (ISH2HOST_MSG7_LH2OSE) - Offset 78h	00000000h
7Ch	4	Outbound Inter Processor Message 8 From ISH To LH2OSE (ISH2HOST_MSG8_LH2OSE) - Offset 7Ch	00000000h
80h	4	Outbound Inter Processor Message 9 From ISH To LH2OSE (ISH2HOST_MSG9_LH2OSE) - Offset 80h	00000000h
84h	4	Outbound Inter Processor Message 10 From ISH To LH2OSE (ISH2HOST_MSG10_LH2OSE) - Offset 84h	00000000h
88h	4	Outbound Inter Processor Message 11 From ISH To LH2OSE (ISH2HOST_MSG11_LH2OSE) - Offset 88h	00000000h
8Ch	4	Outbound Inter Processor Message 12 From ISH To LH2OSE (ISH2HOST_MSG12_LH2OSE) - Offset 8Ch	00000000h
90h	4	Outbound Inter Processor Message 13 From ISH To LH2OSE (ISH2HOST_MSG13_LH2OSE) - Offset 90h	00000000h
94h	4	Outbound Inter Processor Message 14 From ISH To LH2OSE (ISH2HOST_MSG14_LH2OSE) - Offset 94h	00000000h
98h	4	Outbound Inter Processor Message 15 From ISH To LH2OSE (ISH2HOST_MSG15_LH2OSE) - Offset 98h	00000000h
9Ch	4	Outbound Inter Processor Message 16 From ISH To LH2OSE (ISH2HOST_MSG16_LH2OSE) - Offset 9Ch	00000000h
A0h	4	Outbound Inter Processor Message 17 From ISH To LH2OSE (ISH2HOST_MSG17_LH2OSE) - Offset A0h	00000000h
A4h	4	Outbound Inter Processor Message 18 From ISH To LH2OSE (ISH2HOST_MSG18_LH2OSE) - Offset A4h	00000000h
A8h	4	Outbound Inter Processor Message 19 From ISH To LH2OSE (ISH2HOST_MSG19_LH2OSE) - Offset A8h	00000000h
ACh	4	Outbound Inter Processor Message 20 From ISH To LH2OSE (ISH2HOST_MSG20_LH2OSE) - Offset ACh	00000000h
B0h	4	Outbound Inter Processor Message 21 From ISH To LH2OSE (ISH2HOST_MSG21_LH2OSE) - Offset B0h	00000000h
B4h	4	Outbound Inter Processor Message 22 From ISH To LH2OSE (ISH2HOST_MSG22_LH2OSE) - Offset B4h	00000000h
B8h	4	Outbound Inter Processor Message 23 From ISH To LH2OSE (ISH2HOST_MSG23_LH2OSE) - Offset B8h	00000000h
BCh	4	Outbound Inter Processor Message 24 From ISH To LH2OSE (ISH2HOST_MSG24_LH2OSE) - Offset BCh	00000000h
C0h	4	Outbound Inter Processor Message 25 From ISH To LH2OSE (ISH2HOST_MSG25_LH2OSE) - Offset C0h	00000000h
C4h	4	Outbound Inter Processor Message 26 From ISH To LH2OSE (ISH2HOST_MSG26_LH2OSE) - Offset C4h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C8h	4	Outbound Inter Processor Message 27 From ISH To LH2OSE (ISH2HOST_MSG27_LH2OSE) - Offset C8h	00000000h
CCh	4	Outbound Inter Processor Message 28 From ISH To LH2OSE (ISH2HOST_MSG28_LH2OSE) - Offset CCh	00000000h
D0h	4	Outbound Inter Processor Message 29 From ISH To LH2OSE (ISH2HOST_MSG29_LH2OSE) - Offset D0h	00000000h
D4h	4	Outbound Inter Processor Message 30 From ISH To LH2OSE (ISH2HOST_MSG30_LH2OSE) - Offset D4h	00000000h
D8h	4	Outbound Inter Processor Message 31 From ISH To LH2OSE (ISH2HOST_MSG31_LH2OSE) - Offset D8h	00000000h
DCh	4	Outbound Inter Processor Message 32 From ISH To LH2OSE (ISH2HOST_MSG32_LH2OSE) - Offset DCh	00000000h
E0h	4	Inbound Inter Processor Message 1 From LH2OSE To ISH (HOST2ISH_MSG1_LH2OSE) - Offset E0h	00000000h
E4h	4	Inbound Inter Processor Message 2 From LH2OSE To ISH (HOST2ISH_MSG2_LH2OSE) - Offset E4h	00000000h
E8h	4	Inbound Inter Processor Message 3 From LH2OSE To ISH (HOST2ISH_MSG3_LH2OSE) - Offset E8h	00000000h
ECh	4	Inbound Inter Processor Message 4 From LH2OSE To ISH (HOST2ISH_MSG4_LH2OSE) - Offset ECh	00000000h
F0h	4	Inbound Inter Processor Message 5 From LH2OSE To ISH (HOST2ISH_MSG5_LH2OSE) - Offset F0h	00000000h
F4h	4	Inbound Inter Processor Message 6 From LH2OSE To ISH (HOST2ISH_MSG6_LH2OSE) - Offset F4h	00000000h
F8h	4	Inbound Inter Processor Message 7 From LH2OSE To ISH (HOST2ISH_MSG7_LH2OSE) - Offset F8h	00000000h
FCh	4	Inbound Inter Processor Message 8 From LH2OSE To ISH (HOST2ISH_MSG8_LH2OSE) - Offset FCh	00000000h
100h	4	Inbound Inter Processor Message 9 From LH2OSE To ISH (HOST2ISH_MSG9_LH2OSE) - Offset 100h	00000000h
104h	4	Inbound Inter Processor Message 10 From LH2OSE To ISH (HOST2ISH_MSG10_LH2OSE) - Offset 104h	00000000h
108h	4	Inbound Inter Processor Message 11 From LH2OSE To ISH (HOST2ISH_MSG11_LH2OSE) - Offset 108h	00000000h
10Ch	4	Inbound Inter Processor Message 12 From LH2OSE To ISH (HOST2ISH_MSG12_LH2OSE) - Offset 10Ch	00000000h
110h	4	Inbound Inter Processor Message 13 From LH2OSE To ISH (HOST2ISH_MSG13_LH2OSE) - Offset 110h	00000000h
114h	4	Inbound Inter Processor Message 14 From LH2OSE To ISH (HOST2ISH_MSG14_LH2OSE) - Offset 114h	00000000h
118h	4	Inbound Inter Processor Message 15 From LH2OSE To ISH (HOST2ISH_MSG15_LH2OSE) - Offset 118h	00000000h
11Ch	4	Inbound Inter Processor Message 16 From LH2OSE To ISH (HOST2ISH_MSG16_LH2OSE) - Offset 11Ch	00000000h
120h	4	Inbound Inter Processor Message 17 From LH2OSE To ISH (HOST2ISH_MSG17_LH2OSE) - Offset 120h	00000000h
124h	4	Inbound Inter Processor Message 18 From LH2OSE To ISH (HOST2ISH_MSG18_LH2OSE) - Offset 124h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
128h	4	Inbound Inter Processor Message 19 From LH2OSE To ISH (HOST2ISH_MSG19_LH2OSE) - Offset 128h	00000000h
12Ch	4	Inbound Inter Processor Message 20 From LH2OSE To ISH (HOST2ISH_MSG20_LH2OSE) - Offset 12Ch	00000000h
130h	4	Inbound Inter Processor Message 21 From LH2OSE To ISH (HOST2ISH_MSG21_LH2OSE) - Offset 130h	00000000h
134h	4	Inbound Inter Processor Message 22 From LH2OSE To ISH (HOST2ISH_MSG22_LH2OSE) - Offset 134h	00000000h
138h	4	Inbound Inter Processor Message 23 From LH2OSE To ISH (HOST2ISH_MSG23_LH2OSE) - Offset 138h	00000000h
13Ch	4	Inbound Inter Processor Message 24 From LH2OSE To ISH (HOST2ISH_MSG24_LH2OSE) - Offset 13Ch	00000000h
140h	4	Inbound Inter Processor Message 25 From LH2OSE To ISH (HOST2ISH_MSG25_LH2OSE) - Offset 140h	00000000h
144h	4	Inbound Inter Processor Message 26 From LH2OSE To ISH (HOST2ISH_MSG26_LH2OSE) - Offset 144h	00000000h
148h	4	Inbound Inter Processor Message 27 From LH2OSE To ISH (HOST2ISH_MSG27_LH2OSE) - Offset 148h	00000000h
14Ch	4	Inbound Inter Processor Message 28 From LH2OSE To ISH (HOST2ISH_MSG28_LH2OSE) - Offset 14Ch	00000000h
150h	4	Inbound Inter Processor Message 29 From LH2OSE To ISH (HOST2ISH_MSG29_LH2OSE) - Offset 150h	00000000h
154h	4	Inbound Inter Processor Message 30 From LH2OSE To ISH (HOST2ISH_MSG30_LH2OSE) - Offset 154h	00000000h
158h	4	Inbound Inter Processor Message 31 From LH2OSE To ISH (HOST2ISH_MSG31_LH2OSE) - Offset 158h	00000000h
15Ch	4	Inbound Inter Processor Message 32 From LH2OSE To ISH (HOST2ISH_MSG32_LH2OSE) - Offset 15Ch	00000000h
360h	4	Remap0 For LH2OSE (REMAP0_LH2OSE) - Offset 360h	00000000h
364h	4	Remap1 For LH2OSE (REMAP1_LH2OSE) - Offset 364h	00000000h
368h	4	Remap2 For LH2OSE (REMAP2_LH2OSE) - Offset 368h	00000000h
36Ch	4	Remap3 For LH2OSE (REMAP3_LH2OSE) - Offset 36Ch	00000000h
370h	4	Remap4 For LH2OSE (REMAP4_LH2OSE) - Offset 370h	00000000h
374h	4	Remap5 For LH2OSE (REMAP5_LH2OSE) - Offset 374h	00000000h
378h	4	ISH IPC Busy Clear For LH2OSE (ISH_IPC_BUSY_CLEAR_LH2OSE) - Offset 378h	00000000h
6D0h	4	D0i3 Control For LH2OSE (IPC_D0I3C_LH2OSE) - Offset 6D0h	00000008h
800h	4	Opcode Mask 0 For LH2OSE (OPCODE_MASK_REG_0_LH2OSE) - Offset 800h	00000000h
804h	4	Opcode Mask 1 For LH2OSE (OPCODE_MASK_REG_1_LH2OSE) - Offset 804h	00000000h
808h	4	Opcode Mask 2 For LH2OSE (OPCODE_MASK_REG_2_LH2OSE) - Offset 808h	00000000h
80Ch	4	Opcode Mask 3 For LH2OSE (OPCODE_MASK_REG_3_LH2OSE) - Offset 80Ch	00000000h
810h	4	Opcode Mask 4 For LH2OSE (OPCODE_MASK_REG_4_LH2OSE) - Offset 810h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
814h	4	Opcode Mask 5 For LH2OSE (OPCODE_MASK_REG_5_LH2OSE) - Offset 814h	00000000h
818h	4	Opcode Mask 6 For LH2OSE (OPCODE_MASK_REG_6_LH2OSE) - Offset 818h	00000000h
81Ch	4	Opcode Mask 7 For LH2OSE (OPCODE_MASK_REG_7_LH2OSE) - Offset 81Ch	00000000h
900h	4	Ownership Control 0 (OWNERSHIP_CTRL0_LH2OSE) - Offset 900h	00000000h
904h	4	Ownership Control 1 (OWNERSHIP_CTRL1_LH2OSE) - Offset 904h	00000000h
908h	4	Ownership Control 2 (OWNERSHIP_CTRL2_LH2OSE) - Offset 908h	00000000h
90Ch	4	Ownership Control 3 (OWNERSHIP_CTRL3_LH2OSE) - Offset 90Ch	00000000h
910h	4	Ownership Control 4 (OWNERSHIP_CTRL4_LH2OSE) - Offset 910h	00000000h
914h	4	Ownership Control 5 (OWNERSHIP_CTRL5_LH2OSE) - Offset 914h	00000000h
918h	4	Ownership Control 6 (OWNERSHIP_CTRL6_LH2OSE) - Offset 918h	00000000h
91Ch	4	Ownership Control 7 (OWNERSHIP_CTRL7_LH2OSE) - Offset 91Ch	00000000h
B00h	4	TGPIO Mux Sel 0 For LH2OSE (TGPIO_MUX_SEL_REG_0_LH2OSE) - Offset B00h	00000000h
B04h	4	TGPIO Mux Sel 1 For LH2OSE (TGPIO_MUX_SEL_REG_1_LH2OSE) - Offset B04h	00000000h
C00h	4	Feature Disable 0 For LH2OSE (FEATURE_DISABLE_REG_0_LH2OSE) - Offset C00h	00000000h
C04h	4	Feature Disable 1 For LH2OSE (FEATURE_DISABLE_REG_1_LH2OSE) - Offset C04h	00000000h
C50h	4	Fuse Disable 0 (FUSE_DISABLE_REG_0_LH2OSE) - Offset C50h	00000000h
C54h	4	LH2OSE ISH BIOS Selfshoot Reset (ISH_BIOS_SELFSHOOT_RST_LH2OSE) - Offset C54h	00000000h
4000h	4	Reg DASHBOARD_CP0 (DASHBOARD_CP0) - Offset 4000h	01200010h
4004h	4	Reg DASHBOARD_CP1 (DASHBOARD_CP1) - Offset 4004h	00000C00h
4008h	4	Reg DASHBOARD_LDR_WAP0 (DASHBOARD_LDR_WAP0) - Offset 4008h	05200010h
400Ch	4	Reg DASHBOARD_LDR_WAP1 (DASHBOARD_LDR_WAP1) - Offset 400Ch	00000C00h
4010h	4	Reg DASHBOARD_VRF_WAP0 (DASHBOARD_VRF_WAP0) - Offset 4010h	05200010h
4014h	4	Reg DASHBOARD_VRF_WAP1 (DASHBOARD_VRF_WAP1) - Offset 4014h	00000C00h
4018h	4	Reg IPINFO_REG1_0 (IPINFO_REG1_0) - Offset 4018h	00000000h
401Ch	4	Reg IPINFO_REG1_1 (IPINFO_REG1_1) - Offset 401Ch	00000000h
4020h	4	Reg IPINFO_REG2_0 (IPINFO_REG2_0) - Offset 4020h	00000000h
4024h	4	Reg IPINFO_REG2_1 (IPINFO_REG2_1) - Offset 4024h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4030h	4	Reg VERF_ERR_STS_REG (VERF_ERR_STS_REG) - Offset 4030h	00000000h
4040h	4	Reg VERF_ADDR_REG1_0 (VERF_ADDR_REG1_0) - Offset 4040h	00000000h
4044h	4	Reg VERF_ADDR_REG1_1 (VERF_ADDR_REG1_1) - Offset 4044h	00000000h
4048h	4	Reg VERF_SIZE_REG1_0 (VERF_SIZE_REG1_0) - Offset 4048h	00000000h
404Ch	4	Reg VERF_SIZE_REG1_1 (VERF_SIZE_REG1_1) - Offset 404Ch	00000000h
4050h	4	Reg VERF_ADDR_REG2_0 (VERF_ADDR_REG2_0) - Offset 4050h	00000000h
4054h	4	Reg VERF_ADDR_REG2_1 (VERF_ADDR_REG2_1) - Offset 4054h	00000000h
4058h	4	Reg VERF_SIZE_REG2_0 (VERF_SIZE_REG2_0) - Offset 4058h	00000000h
405Ch	4	Reg VERF_SIZE_REG2_1 (VERF_SIZE_REG2_1) - Offset 405Ch	00000000h
4060h	4	Reg VERF_ADDR_REG3_0 (VERF_ADDR_REG3_0) - Offset 4060h	00000000h
4064h	4	Reg VERF_ADDR_REG3_1 (VERF_ADDR_REG3_1) - Offset 4064h	00000000h
4068h	4	Reg VERF_SIZE_REG3_0 (VERF_SIZE_REG3_0) - Offset 4068h	00000000h
406Ch	4	Reg VERF_SIZE_REG3_1 (VERF_SIZE_REG3_1) - Offset 406Ch	00000000h
4070h	4	Reg VERF_ADDR_REG4_0 (VERF_ADDR_REG4_0) - Offset 4070h	00000000h
4074h	4	Reg VERF_ADDR_REG4_1 (VERF_ADDR_REG4_1) - Offset 4074h	00000000h
4078h	4	Reg VERF_SIZE_REG4_0 (VERF_SIZE_REG4_0) - Offset 4078h	00000000h
407Ch	4	Reg VERF_SIZE_REG4_1 (VERF_SIZE_REG4_1) - Offset 407Ch	00000000h
4080h	4	Reg IMR_INFO_ADDR_REG1_0 (IMR_INFO_ADDR_REG1_0) - Offset 4080h	00000000h
4084h	4	Reg IMR_INFO_ADDR_REG1_1 (IMR_INFO_ADDR_REG1_1) - Offset 4084h	00000000h
4088h	4	Reg IMR_INFO_SIZE_REG1_0 (IMR_INFO_SIZE_REG1_0) - Offset 4088h	00000006h
408Ch	4	Reg IMR_INFO_SIZE_REG1_1 (IMR_INFO_SIZE_REG1_1) - Offset 408Ch	00000000h
4090h	4	Reg IMR_INFO_ADDR_REG2_0 (IMR_INFO_ADDR_REG2_0) - Offset 4090h	00000000h
4094h	4	Reg IMR_INFO_ADDR_REG2_1 (IMR_INFO_ADDR_REG2_1) - Offset 4094h	00000000h
4098h	4	Reg IMR_INFO_SIZE_REG2_0 (IMR_INFO_SIZE_REG2_0) - Offset 4098h	00000006h
409Ch	4	Reg IMR_INFO_SIZE_REG2_1 (IMR_INFO_SIZE_REG2_1) - Offset 409Ch	00000000h
4100h	4	Reg VERF_MAT_ADDR_REG1_0 (VERF_MAT_ADDR_REG1_0) - Offset 4100h	00000000h
4104h	4	Reg VERF_MAT_ADDR_REG1_1 (VERF_MAT_ADDR_ REG1_1) - Offset 4104h	00000000h
4108h	4	Reg VERF_MAT_SIZE_REG1_0 (VERF_MAT_SIZE_REG1_0) - Offset 4108h	00000000h
410Ch	4	Reg VERF_MAT_SIZE_REG1_1 (VERF_MAT_SIZE_REG1_1) - Offset 410Ch	00000000h
4110h	4	Reg VERF_MAT_ADDR_REG2_0 (VERF_MAT_ADDR_REG2_0) - Offset 4110h	00000000h
4114h	4	Reg VERF_MAT_ADDR_REG2_1 (VERF_MAT_ADDR_REG2_1) - Offset 4114h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4118h	4	Reg VERF_MAT_SIZE_REG2_0 (VERF_MAT_SIZE_REG2_0) - Offset 4118h	00000000h
411Ch	4	Reg VERF_MAT_SIZE_REG2_1 (VERF_MAT_SIZE_REG2_1) - Offset 411Ch	00000000h
4120h	4	Reg VERF_MAT_ADDR_REG3_0 (VERF_MAT_ADDR_REG3_0) - Offset 4120h	00000000h
4124h	4	Reg VERF_MAT_ADDR_REG3_1 (VERF_MAT_ADDR_REG3_1) - Offset 4124h	00000000h
4128h	4	Reg VERF_MAT_SIZE_REG3_0 (VERF_MAT_SIZE_REG3_0) - Offset 4128h	00000000h
412Ch	4	Reg VERF_MAT_SIZE_REG3_1 (VERF_MAT_SIZE_REG3_1) - Offset 412Ch	00000000h
4130h	4	Reg VERF_MAT_ADDR_REG4_0 (VERF_MAT_ADDR_REG4_0) - Offset 4130h	00000000h
4134h	4	Reg VERF_MAT_ADDR_REG4_1 (VERF_MAT_ADDR_REG4_1) - Offset 4134h	00000000h
4138h	4	Reg VERF_MAT_SIZE_REG4_0 (VERF_MAT_SIZE_REG4_0) - Offset 4138h	00000000h
413Ch	4	Reg VERF_MAT_SIZE_REG4_1 (VERF_MAT_SIZE_REG4_1) - Offset 413Ch	00000000h
4140h	4	Reg IP_GP_REG3_0 (IP_GP_REG3_0) - Offset 4140h	00000000h
4144h	4	Reg IP_GP_REG3_1 (IP_GP_REG3_1) - Offset 4144h	00000000h
4148h	4	Reg IP_GP_REG3_2 (IP_GP_REG3_2) - Offset 4148h	00000000h
414Ch	4	Reg IP_GP_REG3_3 (IP_GP_REG3_3) - Offset 414Ch	00000000h
4150h	4	Reg IP_GP_REG3_4 (IP_GP_REG3_4) - Offset 4150h	00000000h
4154h	4	Reg IP_GP_REG3_5 (IP_GP_REG3_5) - Offset 4154h	00000000h
4158h	4	Reg IP_GP_REG3_6 (IP_GP_REG3_6) - Offset 4158h	00000000h
415Ch	4	Reg IP_GP_REG3_7 (IP_GP_REG3_7) - Offset 415Ch	00000000h
4160h	4	Reg IP_GP_REG4_0 (IP_GP_REG4_0) - Offset 4160h	00000000h
4164h	4	Reg IP_GP_REG4_1 (IP_GP_REG4_1) - Offset 4164h	00000000h
4168h	4	Reg IP_GP_REG4_2 (IP_GP_REG4_2) - Offset 4168h	00000000h
416Ch	4	Reg IP_GP_REG4_3 (IP_GP_REG4_3) - Offset 416Ch	00000000h
4170h	4	Reg IP_GP_REG4_4 (IP_GP_REG4_4) - Offset 4170h	00000000h
4174h	4	Reg IP_GP_REG4_5 (IP_GP_REG4_5) - Offset 4174h	00000000h
4178h	4	Reg IP_GP_REG4_6 (IP_GP_REG4_6) - Offset 4178h	00000000h
417Ch	4	Reg IP_GP_REG4_7 (IP_GP_REG4_7) - Offset 417Ch	00000000h
5030h	4	Reg LOAD_ERR_STS_REG (LOAD_ERR_STS_REG) - Offset 5030h	00000000h
5038h	4	Reg INT_MASK_REG (INT_MASK_REG) - Offset 5038h	00000000h
503Ch	4	Reg INT_STS_REG (INT_STS_REG) - Offset 503Ch	00000000h
5040h	4	Reg LOAD_ADDR_REG1_0 (LOAD_ADDR_REG1_0) - Offset 5040h	00000000h
5044h	4	Reg LOAD_ADDR_REG1_1 (LOAD_ADDR_REG1_1) - Offset 5044h	00000000h
5048h	4	Reg LOAD_SIZE_REG1_0 (LOAD_SIZE_REG1_0) - Offset 5048h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
504Ch	4	Reg LOAD_SIZE_REG1_1 (LOAD_SIZE_REG1_1) - Offset 504Ch	00000000h
5050h	4	Reg LOAD_ADDR_REG2_0 (LOAD_ADDR_REG2_0) - Offset 5050h	00000000h
5054h	4	Reg LOAD_ADDR_REG2_1 (LOAD_ADDR_REG2_1) - Offset 5054h	00000000h
5058h	4	Reg LOAD_SIZE_REG2_0 (LOAD_SIZE_REG2_0) - Offset 5058h	00000000h
505Ch	4	Reg LOAD_SIZE_REG2_1 (LOAD_SIZE_REG2_1) - Offset 505Ch	00000000h
5060h	4	Reg LOAD_ADDR_REG3_0 (LOAD_ADDR_REG3_0) - Offset 5060h	00000000h
5064h	4	Reg LOAD_ADDR_REG3_1 (LOAD_ADDR_REG3_1) - Offset 5064h	00000000h
5068h	4	Reg LOAD_SIZE_REG3_0 (LOAD_SIZE_REG3_0) - Offset 5068h	00000000h
506Ch	4	Reg LOAD_SIZE_REG3_1 (LOAD_SIZE_REG3_1) - Offset 506Ch	00000000h
5070h	4	Reg LOAD_ADDR_REG4_0 (LOAD_ADDR_REG4_0) - Offset 5070h	00000000h
5074h	4	Reg LOAD_ADDR_REG4_1 (LOAD_ADDR_REG4_1) - Offset 5074h	00000000h
5078h	4	Reg LOAD_SIZE_REG4_0 (LOAD_SIZE_REG4_0) - Offset 5078h	00000000h
507Ch	4	Reg LOAD_SIZE_REG4_1 (LOAD_SIZE_REG4_1) - Offset 507Ch	00000000h
50C0h	4	Reg IP_HASH_REG1_00 (IP_HASH_REG1_00) - Offset 50C0h	00000000h
50C4h	4	Reg IP_HASH_REG1_01 (IP_HASH_REG1_01) - Offset 50C4h	00000000h
50C8h	4	Reg IP_HASH_REG1_02 (IP_HASH_REG1_02) - Offset 50C8h	00000000h
50CCh	4	Reg IP_HASH_REG1_03 (IP_HASH_REG1_03) - Offset 50CCh	00000000h
50D0h	4	Reg IP_HASH_REG1_04 (IP_HASH_REG1_04) - Offset 50D0h	00000000h
50D4h	4	Reg IP_HASH_REG1_05 (IP_HASH_REG1_05) - Offset 50D4h	00000000h
50D8h	4	Reg IP_HASH_REG1_06 (IP_HASH_REG1_06) - Offset 50D8h	00000000h
50DCh	4	Reg IP_HASH_REG1_07 (IP_HASH_REG1_07) - Offset 50DCh	00000000h
50E0h	4	Reg IP_HASH_REG1_08 (IP_HASH_REG1_08) - Offset 50E0h	00000000h
50E4h	4	Reg IP_HASH_REG1_09 (IP_HASH_REG1_09) - Offset 50E4h	00000000h
50E8h	4	Reg IP_HASH_REG1_10 (IP_HASH_REG1_10) - Offset 50E8h	00000000h
50ECh	4	Reg IP_HASH_REG1_11 (IP_HASH_REG1_11) - Offset 50ECh	00000000h
50F0h	4	Reg IP_HASH_REG1_12 (IP_HASH_REG1_12) - Offset 50F0h	00000000h
50F4h	4	Reg IP_HASH_REG1_13 (IP_HASH_REG1_13) - Offset 50F4h	00000000h
50F8h	4	Reg IP_HASH_REG1_14 (IP_HASH_REG1_14) - Offset 50F8h	00000000h
50FCh	4	Reg IP_HASH_REG1_15 (IP_HASH_REG1_15) - Offset 50FCh	00000000h
5100h	4	Reg IP_HASH_REG2_00 (IP_HASH_REG2_00) - Offset 5100h	00000000h
5104h	4	Reg IP_HASH_REG2_01 (IP_HASH_REG2_01) - Offset 5104h	00000000h
5108h	4	Reg IP_HASH_REG2_02 (IP_HASH_REG2_02) - Offset 5108h	00000000h
510Ch	4	Reg IP_HASH_REG2_03 (IP_HASH_REG2_03) - Offset 510Ch	00000000h
5110h	4	Reg IP_HASH_REG2_04 (IP_HASH_REG2_04) - Offset 5110h	00000000h
5114h	4	Reg IP_HASH_REG2_05 (IP_HASH_REG2_05) - Offset 5114h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5118h	4	Reg IP_HASH_REG2_06 (IP_HASH_REG2_06) - Offset 5118h	00000000h
511Ch	4	Reg IP_HASH_REG2_07 (IP_HASH_REG2_07) - Offset 511Ch	00000000h
5120h	4	Reg IP_HASH_REG2_08 (IP_HASH_REG2_08) - Offset 5120h	00000000h
5124h	4	Reg IP_HASH_REG2_09 (IP_HASH_REG2_09) - Offset 5124h	00000000h
5128h	4	Reg IP_HASH_REG2_10 (IP_HASH_REG2_10) - Offset 5128h	00000000h
512Ch	4	Reg IP_HASH_REG2_11 (IP_HASH_REG2_11) - Offset 512Ch	00000000h
5130h	4	Reg IP_HASH_REG2_12 (IP_HASH_REG2_12) - Offset 5130h	00000000h
5134h	4	Reg IP_HASH_REG2_13 (IP_HASH_REG2_13) - Offset 5134h	00000000h
5138h	4	Reg IP_HASH_REG2_14 (IP_HASH_REG2_14) - Offset 5138h	00000000h
513Ch	4	Reg IP_HASH_REG2_15 (IP_HASH_REG2_15) - Offset 513Ch	00000000h
5140h	4	Reg IP_HASH_REG3_00 (IP_HASH_REG3_00) - Offset 5140h	00000000h
5144h	4	Reg IP_HASH_REG3_01 (IP_HASH_REG3_01) - Offset 5144h	00000000h
5148h	4	Reg IP_HASH_REG3_02 (IP_HASH_REG3_02) - Offset 5148h	00000000h
514Ch	4	Reg IP_HASH_REG3_03 (IP_HASH_REG3_03) - Offset 514Ch	00000000h
5150h	4	Reg IP_HASH_REG3_04 (IP_HASH_REG3_04) - Offset 5150h	00000000h
5154h	4	Reg IP_HASH_REG3_05 (IP_HASH_REG3_05) - Offset 5154h	00000000h
5158h	4	Reg IP_HASH_REG3_06 (IP_HASH_REG3_06) - Offset 5158h	00000000h
515Ch	4	Reg IP_HASH_REG3_07 (IP_HASH_REG3_07) - Offset 515Ch	00000000h
5160h	4	Reg IP_HASH_REG3_08 (IP_HASH_REG3_08) - Offset 5160h	00000000h
5164h	4	Reg IP_HASH_REG3_09 (IP_HASH_REG3_09) - Offset 5164h	00000000h
5168h	4	Reg IP_HASH_REG3_10 (IP_HASH_REG3_10) - Offset 5168h	00000000h
516Ch	4	Reg IP_HASH_REG3_11 (IP_HASH_REG3_11) - Offset 516Ch	00000000h
5170h	4	Reg IP_HASH_REG3_12 (IP_HASH_REG3_12) - Offset 5170h	00000000h
5174h	4	Reg IP_HASH_REG3_13 (IP_HASH_REG3_13) - Offset 5174h	00000000h
5178h	4	Reg IP_HASH_REG3_14 (IP_HASH_REG3_14) - Offset 5178h	00000000h
517Ch	4	Reg IP_HASH_REG3_15 (IP_HASH_REG3_15) - Offset 517Ch	00000000h
5180h	4	Reg IP_HASH_REG4_00 (IP_HASH_REG4_00) - Offset 5180h	00000000h
5184h	4	Reg IP_HASH_REG4_01 (IP_HASH_REG4_01) - Offset 5184h	00000000h
5188h	4	Reg IP_HASH_REG4_02 (IP_HASH_REG4_02) - Offset 5188h	00000000h
518Ch	4	Reg IP_HASH_REG4_03 (IP_HASH_REG4_03) - Offset 518Ch	00000000h
5190h	4	Reg IP_HASH_REG4_04 (IP_HASH_REG4_04) - Offset 5190h	00000000h
5194h	4	Reg IP_HASH_REG4_05 (IP_HASH_REG4_05) - Offset 5194h	00000000h
5198h	4	Reg IP_HASH_REG4_06 (IP_HASH_REG4_06) - Offset 5198h	00000000h
519Ch	4	Reg IP_HASH_REG4_07 (IP_HASH_REG4_07) - Offset 519Ch	00000000h
51A0h	4	Reg IP_HASH_REG4_08 (IP_HASH_REG4_08) - Offset 51A0h	00000000h
51A4h	4	Reg IP_HASH_REG4_09 (IP_HASH_REG4_09) - Offset 51A4h	00000000h
51A8h	4	Reg IP_HASH_REG4_10 (IP_HASH_REG4_10) - Offset 51A8h	00000000h
51ACh	4	Reg IP_HASH_REG4_11 (IP_HASH_REG4_11) - Offset 51ACh	00000000h
51B0h	4	Reg IP_HASH_REG4_12 (IP_HASH_REG4_12) - Offset 51B0h	00000000h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
51B4h	4	Reg IP_HASH_REG4_13 (IP_HASH_REG4_13) - Offset 51B4h	00000000h
51B8h	4	Reg IP_HASH_REG4_14 (IP_HASH_REG4_14) - Offset 51B8h	00000000h
51BCh	4	Reg IP_HASH_REG4_15 (IP_HASH_REG4_15) - Offset 51BCh	00000000h
5200h	4	Reg IP_GP_REG1_0 (IP_GP_REG1_0) - Offset 5200h	00000000h
5204h	4	Reg IP_GP_REG1_1 (IP_GP_REG1_1) - Offset 5204h	00000000h
5208h	4	Reg IP_GP_REG1_2 (IP_GP_REG1_2) - Offset 5208h	00000000h
520Ch	4	Reg IP_GP_REG1_3 (IP_GP_REG1_3) - Offset 520Ch	00000000h
5210h	4	Reg IP_GP_REG1_4 (IP_GP_REG1_4) - Offset 5210h	00000000h
5214h	4	Reg IP_GP_REG1_5 (IP_GP_REG1_5) - Offset 5214h	00000000h
5218h	4	Reg IP_GP_REG1_6 (IP_GP_REG1_6) - Offset 5218h	00000000h
521Ch	4	Reg IP_GP_REG1_7 (IP_GP_REG1_7) - Offset 521Ch	00000000h
5220h	4	Reg IP_GP_REG2_0 (IP_GP_REG2_0) - Offset 5220h	00000000h
5224h	4	Reg IP_GP_REG2_1 (IP_GP_REG2_1) - Offset 5224h	00000000h
5228h	4	Reg IP_GP_REG2_2 (IP_GP_REG2_2) - Offset 5228h	00000000h
522Ch	4	Reg IP_GP_REG2_3 (IP_GP_REG2_3) - Offset 522Ch	00000000h
5230h	4	Reg IP_GP_REG2_4 (IP_GP_REG2_4) - Offset 5230h	00000000h
5234h	4	Reg IP_GP_REG2_5 (IP_GP_REG2_5) - Offset 5234h	00000000h
5238h	4	Reg IP_GP_REG2_6 (IP_GP_REG2_6) - Offset 5238h	00000000h
523Ch	4	Reg IP_GP_REG2_7 (IP_GP_REG2_7) - Offset 523Ch	00000000h
5240h	4	Reg IP_ACCESS_LOG_REG (IP_ACCESS_LOG_REG) - Offset 5240h	00000000h
6000h	4	Control Policy Low (OSE_SEC_REG_LOW) - Offset 6000h	01200010h
6004h	4	Control Policy High (OSE_SEC_REG_HIGH) - Offset 6004h	00000C00h
6008h	4	OSE_OWNED_IP_RAC_LOW - Offset 6008h	05200010h
600Ch	4	OSE_OWNED_IP_RAC_HIGH - Offset 600Ch	00000C00h
6010h	4	OSE_OWNED_IP_WAC_LOW - Offset 6010h	05200010h
6014h	4	OSE_OWNED_IP_WAC_HIGH - Offset 6014h	00000C00h
6018h	4	OSE_LH_OWNED_IP_RAC_LOW - Offset 6018h	0120001Fh
601Ch	4	OSE_LH_OWNED_IP_RAC_HIGH - Offset 601Ch	00000E20h
6020h	4	OSE_LH_OWNED_IP_WAC_LOW - Offset 6020h	0120001Fh
6024h	4	OSE_LH_OWNED_IP_WAC_HIGH - Offset 6024h	00000E20h
6028h	4	NULL_OWNED_IP_RAC_LOW - Offset 6028h	01200010h
602Ch	4	NULL_OWNED_IP_RAC_HIGH - Offset 602Ch	00000C00h
6030h	4	NULL_OWNED_IP_WAC_LOW - Offset 6030h	01200010h
6034h	4	NULL_OWNED_IP_WAC_HIGH - Offset 6034h	00000C00h
6038h	4	LH2OSE_IPC_OS_REGION_RAC_LOW - Offset 6038h	0520001Fh
603Ch	4	LH2OSE_IPC_OS_REGION_RAC_HIGH - Offset 603Ch	00000E00h
6040h	4	LH2OSE_IPC_OS_REGION_WAC_LOW - Offset 6040h	0520001Fh
6044h	4	LH2OSE_IPC_OS_REGION_WAC_HIGH - Offset 6044h	00000E00h

Table 2-2. Summary of Bus: 0, Device: 29, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6048h	4	LH2OSE_IPC_BIOS_REGION_RAC_LOW - Offset 6048h	05200010h
604Ch	4	LH2OSE_IPC_BIOS_REGION_RAC_HIGH - Offset 604Ch	00000C00h
6050h	4	LH2OSE_IPC_BIOS_REGION_WAC_LOW - Offset 6050h	05200010h
6054h	4	LH2OSE_IPC_BIOS_REGION_WAC_HIGH - Offset 6054h	00000C00h
6058h	4	OSE_SRAM_LH2OSE_REG1_REGION_RAC_LOW - Offset 6058h	0520001Fh
605Ch	4	OSE_SRAM_LH2OSE_REG1_REGION_RAC_HIGH - Offset 605Ch	00000E00h
6060h	4	OSE_SRAM_LH2OSE_REG1_REGION_WAC_LOW - Offset 6060h	0520001Fh
6064h	4	OSE_SRAM_LH2OSE_REG1_REGION_WAC_HIGH - Offset 6064h	00000E00h
6068h	4	OSE_SRAM_LH2OSE_REG2_REGION_RAC_LOW - Offset 6068h	0520001Fh
606Ch	4	OSE_SRAM_LH2OSE_REG2_REGION_RAC_HIGH - Offset 606Ch	00000E00h
6070h	4	OSE_SRAM_LH2OSE_REG2_REGION_WAC_LOW - Offset 6070h	0520001Fh
6074h	4	OSE_SRAM_LH2OSE_REG2_REGION_WAC_HIGH - Offset 6074h	00000E00h
6078h	4	OSE_SRAM_LH2OSE_REG3_REGION_RAC_LOW - Offset 6078h	0520001Fh
607Ch	4	OSE_SRAM_LH2OSE_REG3_REGION_RAC_HIGH - Offset 607Ch	00000E00h
6080h	4	OSE_SRAM_LH2OSE_REG3_REGION_WAC_LOW - Offset 6080h	0520001Fh
6084h	4	OSE_SRAM_LH2OSE_REG3_REGION_WAC_HIGH - Offset 6084h	00000E00h
6088h	4	OSE_LH2OSE_SRAM_GBEPROXY_REGION_RAC_LOW - Offset 6088h	0520001Fh
608Ch	4	OSE_LH2OSE_SRAM_GBEPROXY_REGION_RAC_HIGH - Offset 608Ch	00000E00h
6090h	4	OSE_LH2OSE_SRAM_GBEPROXY_REGION_WAC_LOW - Offset 6090h	0520001Fh
6094h	4	OSE_LH2OSE_SRAM_GBEPROXY_REGION_WAC_HIGH - Offset 6094h	00000E00h
6098h	4	OSE_CSE_IPC_RAC_LOW - Offset 6098h	05210010h
609Ch	4	OSE_CSE_IPC_RAC_HIGH - Offset 609Ch	00000C00h
60A0h	4	OSE_CSE_IPC_WAC_LOW - Offset 60A0h	05210010h
60A4h	4	OSE_CSE_IPC_WAC_HIGH - Offset 60A4h	00000C00h
60A8h	4	OSE_PMC_IPC_RAC_LOW - Offset 60A8h	05200010h
60ACh	4	OSE_PMC_IPC_RAC_HIGH - Offset 60ACh	00000C00h
60B0h	4	OSE_PMC_IPC_WAC_LOW - Offset 60B0h	05200010h
60B4h	4	OSE_PMC_IPC_WAC_HIGH - Offset 60B4h	00000C00h
60B8h	4	OSE_AUDIO_IPC_RAC_LOW - Offset 60B8h	05200010h
60BCh	4	OSE_AUDIO_IPC_RAC_HIGH - Offset 60BCh	00020C00h
60C0h	4	OSE_AUDIO_IPC_WAC_LOW - Offset 60C0h	05200010h
60C4h	4	OSE_AUDIO_IPC_WAC_HIGH - Offset 60C4h	00020C00h
60C8h	4	OSE_SBEP_WAC_LOW - Offset 60C8h	07210010h
60CCh	4	OSE_SBEP_WAC_HIGH - Offset 60CCh	00020C00h
60D0h	4	OSE_SBEP_BOOTPREP_WAC_LOW - Offset 60D0h	05200000h
60D4h	4	OSE_SBEP_BOOTPREP_WAC_HIGH - Offset 60D4h	00000C00h

2.2.1 Peripheral Interrupt Status - LH2OSE (PISR_LH2OSE) - Offset 0h

This register contains the inbound interrupt status bits for the LH2OSE IPC channel. Interrupts are generated when PISR[x] & PIMR[x] are both set.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h NA	**PISR_H2IBCISC:** Host2ISH busy clear interrupt status clear interrupt: 1 -> Interrupt is active 0 -> Interrupt is inactive. Writing 1 to this bit clears it.
26:1	0h RO	**Reserved**
0	0h NA	**PISR_HOST2ISH:** Inbound IPC request from HOST to ISH status: 1 -> Interrupt is active 0 -> Interrupt is inactive.

2.2.2 Peripheral Interrupt Mask - LH2OSE (PIMR_LH2OSE) - Offset 4h

This register enables or disables inbound interrupts from LH2OSE to ISH. This register is not accessible by LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h NA	**H2IBCISC_IE:** Mask bit for H2IBCISC interrupt mask 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
26:12	0h RO	**Reserved**
11	0h NA	**PIMR_ISH2HOST_BUSY_CLEAR:** Mask bit for ISH2HOST busy clear interrupt 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
10:1	0h RO	**Reserved**
0	0h NA	**PIMR_HOST2ISH:** Reserved

2.2.3 LH2OSE Peripheral Interrupt Mask (HOST_PIMR_LH2OSE) - Offset 8h

This register is for enabling the interrupts generated by ISH towards LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000101h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	1h RW	**PIMR_HOST2ISH_BUSY_CLEAR:** Host2ISH busy clear interrupt mask bit 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
7:1	0h RO	**Reserved**
0	1h RW	**PIMR_ISH2HOST_IPC_REG:** Outbound IPC request from ISH to HOST Mask 1 -> Interrupt is unmasked 0 -> Interrupt is masked.

2.2.4 LH2OSE Peripheral Interrupt Status (HOST_PISR_LH2OSE) - Offset Ch

Interrupt Status Register for interrupts to LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW/1C	**PISR_HOST2ISH_BUSY_CLEAR:** Host2ISH busy clear interrupt status bit 1 -> Interrupt is active.
7:1	0h RO	**Reserved**
0	0h RO	**PISR_ISH2HOST_IPC_REG:** Outbound IPC request from ISH to HOST Status 1 -> Interrupt.

2.2.5 LH2OSE Channel Interrupt Mask (CIM_LH2OSE) - Offset 10h

This register is for masking the per channel interrupt, caused by any of the interrupt sources towards ARM M7 in the IPC Channel.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h NA	**CH_INTR_MASK:** Enable interrupts towards ARM M7 for the channel. 1 -> Interrupt is masked 0 -> Interrupt is enabled.

2.2.6 LH2OSE Channel Interrupt Status (CIS_LH2OSE) - Offset 14h

This register provides the per channel interrupt status, this is set if any of the interrupt sources towards ARM M7 are set in the IPC Channel.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h NA	**CH_INTR_STATUS:** Interrupt status for the interrupts to ARM M7 for the channel. This will be set if any of the interrupt sources are enabled and their status is high.

2.2.7 LH2OSE Firmware Status (ISH_HOST_FWSTS_LH2OSE) - Offset 34h

Write by ISH, RO by LH2OSE, this is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. As the firmware comes up after the reset or power cycle it sets bits of this register to 1b1 to indicate its status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**ISH_HOST_FWSTS:** ISH Host firmware status.

2.2.8 LH2OSE Communication (HOST_COMM_LH2OSE) - Offset 38h

Write by LH2OSE, RO by ISH, this is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. The Host sets bits of this register to 1b1 to communicate with the ISH.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HOST_COMM:** Host communication register.

2.2.9 Inbound DoorbellLH2OSE To ISH (HOST2ISH_DOORBELL_LH2OSE) - Offset 48h

Inbound doorbell register, from LH2OSE core to interrupt ISH. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. When software writes the message in to respective message register, it should set bit 31(BUSY Bit) of doorbell register to indicate that new data is written. The ISH will assert a level sensitive interrupt to the IOAPIC as long as the BUSY bit is set. When the ISH reads the message code from this register it should write back to this register and clear the BUSY bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the ISH CPU is Ready to accept a new message.
30:0	00000000h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

2.2.10 Outbound DoorbellISH To LH2OSE (ISH2HOST_DOORBELL_LH2OSE) - Offset 54h

Outbound doorbell register for the ISH to interrupt LH2OSE. Setting bit 31 of this register causes the Host to receive a IRQn interrupt. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. The ISH will set bit 31 of this reg to ring the doorbell after it has completed programming the message to Host. When the Host reads the message code from this register it should write back to this register and clear the BUSY bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the HOST CPU is Ready to accept a new message.
30:0	00000000h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

2.2.11 Outbound Inter Processor Message 1 From ISH To LH2OSE (ISH2HOST_MSG1_LH2OSE) - Offset 60h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.12 Outbound Inter Processor Message 2 From ISH To LH2OSE (ISH2HOST_MSG2_LH2OSE) - Offset 64h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.13 Outbound Inter Processor Message 3 From ISH To LH2OSE (ISH2HOST_MSG3_LH2OSE) - Offset 68h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.14 Outbound Inter Processor Message 4 From ISH To LH2OSE (ISH2HOST_MSG4_LH2OSE) - Offset 6Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.15 Outbound Inter Processor Message 5 From ISH To LH2OSE (ISH2HOST_MSG5_LH2OSE) - Offset 70h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.16 Outbound Inter Processor Message 6 From ISH To LH2OSE (ISH2HOST_MSG6_LH2OSE) - Offset 74h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.17 Outbound Inter Processor Message 7 From ISH To LH2OSE (ISH2HOST_MSG7_LH2OSE) - Offset 78h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.18 Outbound Inter Processor Message 8 From ISH To LH2OSE (ISH2HOST_MSG8_LH2OSE) - Offset 7Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.19 Outbound Inter Processor Message 9 From ISH To LH2OSE (ISH2HOST_MSG9_LH2OSE) - Offset 80h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.20 Outbound Inter Processor Message 10 From ISH To LH2OSE (ISH2HOST_MSG10_LH2OSE) - Offset 84h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.21 Outbound Inter Processor Message 11 From ISH To LH2OSE (ISH2HOST_MSG11_LH2OSE) - Offset 88h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.22 Outbound Inter Processor Message 12 From ISH To LH2OSE (ISH2HOST_MSG12_LH2OSE) - Offset 8Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.23 Outbound Inter Processor Message 13 From ISH To LH2OSE (ISH2HOST_MSG13_LH2OSE) - Offset 90h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.24 Outbound Inter Processor Message 14 From ISH To LH2OSE (ISH2HOST_MSG14_LH2OSE) - Offset 94h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.25 Outbound Inter Processor Message 15 From ISH To LH2OSE (ISH2HOST_MSG15_LH2OSE) - Offset 98h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.26 Outbound Inter Processor Message 16 From ISH To LH2OSE (ISH2HOST_MSG16_LH2OSE) - Offset 9Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.27 Outbound Inter Processor Message 17 From ISH To LH2OSE (ISH2HOST_MSG17_LH2OSE) - Offset A0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.28 Outbound Inter Processor Message 18 From ISH To LH2OSE (ISH2HOST_MSG18_LH2OSE) - Offset A4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.29 Outbound Inter Processor Message 19 From ISH To LH2OSE (ISH2HOST_MSG19_LH2OSE) - Offset A8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.30 Outbound Inter Processor Message 20 From ISH To LH2OSE (ISH2HOST_MSG20_LH2OSE) - Offset ACh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.31 Outbound Inter Processor Message 21 From ISH To LH2OSE (ISH2HOST_MSG21_LH2OSE) - Offset B0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.32 Outbound Inter Processor Message 22 From ISH To LH2OSE (ISH2HOST_MSG22_LH2OSE) - Offset B4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.33 Outbound Inter Processor Message 23 From ISH To LH2OSE (ISH2HOST_MSG23_LH2OSE) - Offset B8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.34 Outbound Inter Processor Message 24 From ISH To LH2OSE (ISH2HOST_MSG24_LH2OSE) - Offset BCh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.35 Outbound Inter Processor Message 25 From ISH To LH2OSE (ISH2HOST_MSG25_LH2OSE) - Offset C0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.36 Outbound Inter Processor Message 26 From ISH To LH2OSE (ISH2HOST_MSG26_LH2OSE) - Offset C4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.37 Outbound Inter Processor Message 27 From ISH To LH2OSE (ISH2HOST_MSG27_LH2OSE) - Offset C8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.38 Outbound Inter Processor Message 28 From ISH To LH2OSE (ISH2HOST_MSG28_LH2OSE) - Offset CCh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.39 Outbound Inter Processor Message 29 From ISH To LH2OSE (ISH2HOST_MSG29_LH2OSE) - Offset D0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.40 Outbound Inter Processor Message 30 From ISH To LH2OSE (ISH2HOST_MSG30_LH2OSE) - Offset D4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.41 Outbound Inter Processor Message 31 From ISH To LH2OSE (ISH2HOST_MSG31_LH2OSE) - Offset D8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.42 Outbound Inter Processor Message 32 From ISH To LH2OSE (ISH2HOST_MSG32_LH2OSE) - Offset DCh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

2.2.43 Inbound Inter Processor Message 1 From LH2OSE To ISH (HOST2ISH_MSG1_LH2OSE) - Offset E0h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.44 Inbound Inter Processor Message 2 From LH2OSE To ISH (HOST2ISH_MSG2_LH2OSE) - Offset E4h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.45 Inbound Inter Processor Message 3 From LH2OSE To ISH (HOST2ISH_MSG3_LH2OSE) - Offset E8h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.46 Inbound Inter Processor Message 4 From LH2OSE To ISH (HOST2ISH_MSG4_LH2OSE) - Offset ECh

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.47 Inbound Inter Processor Message 5 From LH2OSE To ISH (HOST2ISH_MSG5_LH2OSE) - Offset F0h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.48 Inbound Inter Processor Message 6 From LH2OSE To ISH (HOST2ISH_MSG6_LH2OSE) - Offset F4h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.49 Inbound Inter Processor Message 7 From LH2OSE To ISH (HOST2ISH_MSG7_LH2OSE) - Offset F8h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.50 Inbound Inter Processor Message 8 From LH2OSE To ISH (HOST2ISH_MSG8_LH2OSE) - Offset FCh

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.51 Inbound Inter Processor Message 9 From LH2OSE To ISH (HOST2ISH_MSG9_LH2OSE) - Offset 100h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.52 Inbound Inter Processor Message 10 From LH2OSE To ISH (HOST2ISH_MSG10_LH2OSE) - Offset 104h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.53 Inbound Inter Processor Message 11 From LH2OSE To ISH (HOST2ISH_MSG11_LH2OSE) - Offset 108h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.54 Inbound Inter Processor Message 12 From LH2OSE To ISH (HOST2ISH_MSG12_LH2OSE) - Offset 10Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.55 Inbound Inter Processor Message 13 From LH2OSE To ISH (HOST2ISH_MSG13_LH2OSE) - Offset 110h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.56 Inbound Inter Processor Message 14 From LH2OSE To ISH (HOST2ISH_MSG14_LH2OSE) - Offset 114h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.57 Inbound Inter Processor Message 15 From LH2OSE To ISH (HOST2ISH_MSG15_LH2OSE) - Offset 118h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.58 Inbound Inter Processor Message 16 From LH2OSE To ISH (HOST2ISH_MSG16_LH2OSE) - Offset 11Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.59 Inbound Inter Processor Message 17 From LH2OSE To ISH (HOST2ISH_MSG17_LH2OSE) - Offset 120h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.60 Inbound Inter Processor Message 18 From LH2OSE To ISH (HOST2ISH_MSG18_LH2OSE) - Offset 124h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.61 Inbound Inter Processor Message 19 From LH2OSE To ISH (HOST2ISH_MSG19_LH2OSE) - Offset 128h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.62 Inbound Inter Processor Message 20 From LH2OSE To ISH (HOST2ISH_MSG20_LH2OSE) - Offset 12Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.63 Inbound Inter Processor Message 21 From LH2OSE To ISH (HOST2ISH_MSG21_LH2OSE) - Offset 130h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.64 Inbound Inter Processor Message 22 From LH2OSE To ISH (HOST2ISH_MSG22_LH2OSE) - Offset 134h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.65 Inbound Inter Processor Message 23 From LH2OSE To ISH (HOST2ISH_MSG23_LH2OSE) - Offset 138h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.66 Inbound Inter Processor Message 24 From LH2OSE To ISH (HOST2ISH_MSG24_LH2OSE) - Offset 13Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.67 Inbound Inter Processor Message 25 From LH2OSE To ISH (HOST2ISH_MSG25_LH2OSE) - Offset 140h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.68 Inbound Inter Processor Message 26 From LH2OSE To ISH (HOST2ISH_MSG26_LH2OSE) - Offset 144h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.69 Inbound Inter Processor Message 27 From LH2OSE To ISH (HOST2ISH_MSG27_LH2OSE) - Offset 148h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.70 Inbound Inter Processor Message 28 From LH2OSE To ISH (HOST2ISH_MSG28_LH2OSE) - Offset 14Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.71 Inbound Inter Processor Message 29 From LH2OSE To ISH (HOST2ISH_MSG29_LH2OSE) - Offset 150h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.72 Inbound Inter Processor Message 30 From LH2OSE To ISH (HOST2ISH_MSG30_LH2OSE) - Offset 154h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.73 Inbound Inter Processor Message 31 From LH2OSE To ISH (HOST2ISH_MSG31_LH2OSE) - Offset 158h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.74 Inbound Inter Processor Message 32 From LH2OSE To ISH (HOST2ISH_MSG32_LH2OSE) - Offset 15Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 15Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

2.2.75 Remap0 For LH2OSE (REMAP0_LH2OSE) - Offset 360h

General Purpose Remap Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 360h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

2.2.76 Remap1 For LH2OSE (REMAP1_LH2OSE) - Offset 364h

General Purpose Remap Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 364h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

2.2.77 Remap2 For LH2OSE (REMAP2_LH2OSE) - Offset 368h

General Purpose Remap Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 368h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

2.2.78 Remap3 For LH2OSE (REMAP3_LH2OSE) - Offset 36Ch

General Purpose Remap Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 36Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

2.2.79 Remap4 For LH2OSE (REMAP4_LH2OSE) - Offset 370h

General Purpose Remap Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 370h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

2.2.80 Remap5 For LH2OSE (REMAP5_LH2OSE) - Offset 374h

General Purpose Remap Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 374h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

2.2.81 ISH IPC Busy Clear For LH2OSE (ISH_IPC_BUSY_CLEAR_LH2OSE) - Offset 378h

This register holds the status of the ISH IPC busy clear interrupts. ISH IPC busy clear interrupt is set when busy bit of respective outbound doorbell register gets cleared and interrupt is cleared when ISH writes 1 to respective bit in ISH IPC busy clear register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 378h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h NA	**ISH2HOST_BUSY_CLEAR:** Busy clear interrupt bit of ISH2HOST IPC 1 -> Interrupt active 0 -> Interrupt inactive.

2.2.82 D0i3 Control For LH2OSE (IPC_D0I3C_LH2OSE) - Offset 6D0h

This register will be used for D0i3 SW flow. The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6D0h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

2.2.83 Opcode Mask 0 For LH2OSE (OPCODE_MASK_REG_0_LH2OSE) - Offset 800h

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.84 Opcode Mask 1 For LH2OSE (OPCODE_MASK_REG_1_LH2OSE) - Offset 804h

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 804h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.85 Opcode Mask 2 For LH2OSE (OPCODE_MASK_REG_2_LH2OSE) - Offset 808h

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.86 Opcode Mask 3 For LH2OSE (OPCODE_MASK_REG_3_LH2OSE) - Offset 80Ch

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.87 Opcode Mask 4 For LH2OSE (OPCODE_MASK_REG_4_LH2OSE) - Offset 810h

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.88 Opcode Mask 5 For LH2OSE (OPCODE_MASK_REG_5_LH2OSE) - Offset 814h

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.89 Opcode Mask 6 For LH2OSE (OPCODE_MASK_REG_6_LH2OSE) - Offset 818h

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.90 Opcode Mask 7 For LH2OSE (OPCODE_MASK_REG_7_LH2OSE) - Offset 81Ch

Masking of opcodes for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OPCODE_MASK:** General Purpose Field.

2.2.91 Ownership Control 0 (OWNERSHIP_CTRL0_LH2OSE) - Offset 900h

Controls Ownership and Interrupt delivery for devices 7 to 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 900h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device7 (INTR_DELIVERY_DEV7):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device7 (OWNERSHIP_DEV7):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device6 (INTR_DELIVERY_DEV6):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device6 (OWNERSHIP_DEV6):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device5 (INTR_DELIVERY_DEV5):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
22:20	0h RW	**Ownership Device5 (OWNERSHIP_DEV5):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device4 (INTR_DELIVERY_DEV4):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device4 (OWNERSHIP_DEV4):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device3 (INTR_DELIVERY_DEV3):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
14:12	0h RW	**Ownership Device3 (OWNERSHIP_DEV3):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device2 (INTR_DELIVERY_DEV2):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device2 (OWNERSHIP_DEV2):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device1 (INTR_DELIVERY_DEV1):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
6:4	0h RW	**Ownership Device1 (OWNERSHIP_DEV1):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device0 (INTR_DELIVERY_DEV0):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device0 (OWNERSHIP_DEV0):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.92 Ownership Control 1 (OWNERSHIP_CTRL1_LH2OSE) - Offset 904h

Controls Ownership and Interrupt delivery for devices 15 to 8.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 904h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device15 (INTR_DELIVERY_DEV15):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device15 (OWNERSHIP_DEV15):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device14 (INTR_DELIVERY_DEV14):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device14 (OWNERSHIP_DEV14):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device13 (INTR_DELIVERY_DEV13):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
22:20	0h RW	**Ownership Device13 (OWNERSHIP_DEV13):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device12 (INTR_DELIVERY_DEV12):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device12 (OWNERSHIP_DEV12):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device11 (INTR_DELIVERY_DEV11):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
14:12	0h RW	**Ownership Device11 (OWNERSHIP_DEV11):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device10 (INTR_DELIVERY_DEV10):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device10 (OWNERSHIP_DEV10):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device9 (INTR_DELIVERY_DEV9):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Ownership Device9 (OWNERSHIP_DEV9):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device8 (INTR_DELIVERY_DEV8):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device8 (OWNERSHIP_DEV8):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.93 Ownership Control 2 (OWNERSHIP_CTRL2_LH2OSE) - Offset 908h

Controls Ownership and Interrupt delivery for devices 23 to 16.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 908h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device23 (INTR_DELIVERY_DEV23):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device23 (OWNERSHIP_DEV23):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device22 (INTR_DELIVERY_DEV22):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device22 (OWNERSHIP_DEV22):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device21 (INTR_DELIVERY_DEV21):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
22:20	0h RW	**Ownership Device21 (OWNERSHIP_DEV21):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device20 (INTR_DELIVERY_DEV20):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device20 (OWNERSHIP_DEV20):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device19 (INTR_DELIVERY_DEV19):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.

Bit Range	Default & Access	Field Name (ID): Description
14:12	0h RW	**Ownership Device19 (OWNERSHIP_DEV19):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device18 (INTR_DELIVERY_DEV18):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device18 (OWNERSHIP_DEV18):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device17 (INTR_DELIVERY_DEV17):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
6:4	0h RW	**Ownership Device17 (OWNERSHIP_DEV17):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device16 (INTR_DELIVERY_DEV16):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device16 (OWNERSHIP_DEV16):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.94 Ownership Control 3 (OWNERSHIP_CTRL3_LH2OSE) - Offset 90Ch

Controls Ownership and Interrupt delivery for devices 31 to 24.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device31 (INTR_DELIVERY_DEV31):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device31 (OWNERSHIP_DEV31):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device30 (INTR_DELIVERY_DEV30):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device30 (OWNERSHIP_DEV30):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device29 (INTR_DELIVERY_DEV29):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**Ownership Device29 (OWNERSHIP_DEV29):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device28 (INTR_DELIVERY_DEV28):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device28 (OWNERSHIP_DEV28):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device27 (INTR_DELIVERY_DEV27):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
14:12	0h RW	**Ownership Device27 (OWNERSHIP_DEV27):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device26 (INTR_DELIVERY_DEV26):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device26 (OWNERSHIP_DEV26):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device25 (INTR_DELIVERY_DEV25):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
6:4	0h RW	**Ownership Device25 (OWNERSHIP_DEV25):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device24 (INTR_DELIVERY_DEV24):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device24 (OWNERSHIP_DEV24):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.95 Ownership Control 4 (OWNERSHIP_CTRL4_LH2OSE) - Offset 910h

Controls Ownership and Interrupt delivery for devices 39 to 32.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 910h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device39 (INTR_DELIVERY_DEV39):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device39 (OWNERSHIP_DEV39):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device38 (INTR_DELIVERY_DEV38):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device38 (OWNERSHIP_DEV38):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device37 (INTR_DELIVERY_DEV37):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
22:20	0h RW	**Ownership Device37 (OWNERSHIP_DEV37):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device36 (INTR_DELIVERY_DEV36):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device36 (OWNERSHIP_DEV36):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device35 (INTR_DELIVERY_DEV35):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
14:12	0h RW	**Ownership Device35 (OWNERSHIP_DEV35):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device34 (INTR_DELIVERY_DEV34):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device34 (OWNERSHIP_DEV34):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device33 (INTR_DELIVERY_DEV33):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
6:4	0h RW	**Ownership Device33 (OWNERSHIP_DEV33):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device32 (INTR_DELIVERY_DEV32):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device32 (OWNERSHIP_DEV32):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.96 Ownership Control 5 (OWNERSHIP_CTRL5_LH2OSE) - Offset 914h

Controls Ownership and Interrupt delivery for devices 47 to 40.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 914h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device47 (INTR_DELIVERY_DEV47):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device47 (OWNERSHIP_DEV47):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device46 (INTR_DELIVERY_DEV46):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device46 (OWNERSHIP_DEV46):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device45 (INTR_DELIVERY_DEV45):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
22:20	0h RW	**Ownership Device45 (OWNERSHIP_DEV45):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device44 (INTR_DELIVERY_DEV44):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device44 (OWNERSHIP_DEV44):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device43 (INTR_DELIVERY_DEV43):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
14:12	0h RW	**Ownership Device43 (OWNERSHIP_DEV43):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device42 (INTR_DELIVERY_DEV42):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device42 (OWNERSHIP_DEV42):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device41 (INTR_DELIVERY_DEV41):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Ownership Device41 (OWNERSHIP_DEV41):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device40 (INTR_DELIVERY_DEV40):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device40 (OWNERSHIP_DEV40):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.97 Ownership Control 6 (OWNERSHIP_CTRL6_LH2OSE) - Offset 918h

Controls Ownership and Interrupt delivery for devices 55 to 48.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 918h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device55 (INTR_DELIVERY_DEV55):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device55 (OWNERSHIP_DEV55):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device54 (INTR_DELIVERY_DEV54):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device54 (OWNERSHIP_DEV54):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device53 (INTR_DELIVERY_DEV53):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
22:20	0h RW	**Ownership Device53 (OWNERSHIP_DEV53):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device52 (INTR_DELIVERY_DEV52):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device52 (OWNERSHIP_DEV52):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device51 (INTR_DELIVERY_DEV51):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.

Bit Range	Default & Access	Field Name (ID): Description
14:12	0h RW	**Ownership Device51 (OWNERSHIP_DEV51):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device50 (INTR_DELIVERY_DEV50):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device50 (OWNERSHIP_DEV50):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device49 (INTR_DELIVERY_DEV49):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
6:4	0h RW	**Ownership Device49 (OWNERSHIP_DEV49):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device48 (INTR_DELIVERY_DEV48):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device48 (OWNERSHIP_DEV48):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.98 Ownership Control 7 (OWNERSHIP_CTRL7_LH2OSE) - Offset 91Ch

Controls Ownership and Interrupt delivery for devices 63 to 56.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 91Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Delivery Device63 (INTR_DELIVERY_DEV63):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
30:28	0h RW	**Ownership Device63 (OWNERSHIP_DEV63):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
27	0h RW	**Interrupt Delivery Device62 (INTR_DELIVERY_DEV62):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
26:24	0h RW	**Ownership Device62 (OWNERSHIP_DEV62):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
23	0h RW	**Interrupt Delivery Device61 (INTR_DELIVERY_DEV61):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**Ownership Device61 (OWNERSHIP_DEV61):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
19	0h RW	**Interrupt Delivery Device60 (INTR_DELIVERY_DEV60):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
18:16	0h RW	**Ownership Device60 (OWNERSHIP_DEV60):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
15	0h RW	**Interrupt Delivery Device59 (INTR_DELIVERY_DEV59):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
14:12	0h RW	**Ownership Device59 (OWNERSHIP_DEV59):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
11	0h RW	**Interrupt Delivery Device58 (INTR_DELIVERY_DEV58):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
10:8	0h RW	**Ownership Device58 (OWNERSHIP_DEV58):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
7	0h RW	**Interrupt Delivery Device57 (INTR_DELIVERY_DEV57):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
6:4	0h RW	**Ownership Device57 (OWNERSHIP_DEV57):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).
3	0h RW	**Interrupt Delivery Device56 (INTR_DELIVERY_DEV56):** Interrupt Delivery: Valid only when device is owned by Host : 0 : MSI Messaging 1: IOSF SB assert/de-assert IRQ.
2:0	0h RW	**Ownership Device56 (OWNERSHIP_DEV56):** Ownership Value for device: 000 (ARM Owned) 001 (Host Owned) x1x (Null Owned or not a valid case).

2.2.99 TGPIO Mux Sel 0 For LH2OSE (TGPIO_MUX_SEL_REG_0_LH2OSE) - Offset B00h

Pin Mux Select Register for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Pin Mux Sel (TGPIO_MUX_SEL):** 2'b00 -Config 1 : All 30 pins are from GPIO i.e GPIO_OUT[29:0] = GPIO[29:0] 2'b01 -Config 2 : GPIO_OUT[29:0] = {TGPIO[19:0], GPIO[9:0]} 2'b10 -Config 3 : GPIO_OUT[29:0] = {GPIO[29:20], TGPIO[19:0]} 2'b11 -Config 4: GPIO_OUT[29:0] = {TGPIO[19:10], GPIO[19:10], TGPIO[9:0]}.

2.2.100 TGPIO Mux Sel 1 For LH2OSE (TGPIO_MUX_SEL_REG_1_LH2OSE) - Offset B04h

Pin Mux Select Register for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Pin Mux Sel (TGPIO_MUX_SEL):** 2'b00 -Config 1 : All 30 pins are from GPIO i.e GPIO_OUT[29:0] = GPIO[29:0] 2'b01 -Config 2 : GPIO_OUT[29:0] = {TGPIO[19:0], GPIO[9:0]} 2'b10 -Config 3 : GPIO_OUT[29:0] = {GPIO[29:20], TGPIO[19:0]} 2'b11 -Config 4: GPIO_OUT[29:0] = {TGPIO[19:10], GPIO[19:10], TGPIO[9:0]}.

2.2.101 Feature Disable 0 For LH2OSE (FEATURE_DISABLE_REG_0_LH2OSE) - Offset C00h

Feature Disable Register for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Feature Disable (FEATURE_DISBLE):** OSE will implement a BIOS writable register called FEATURE_DISABLEn in BIOS. Below are the bit fields of that register. Each bit corresponds to a particular Sub-IP in OSE. When the FEATURE_DISABLE for that SubIP is set, OSE HW will clock gate the SubIP. If FW tries to access the clock-gated SubIP, then the access would result in a fabric timeout error/interrupt. FW has to then follow the error recovery process.

2.2.102 Feature Disable 1 For LH2OSE (FEATURE_DISABLE_REG_1_LH2OSE) - Offset C04h

Feature Disable Register for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Feature Disable (FEATURE_DISBLE):** OSE will implement a BIOS writable register called FEATURE_DISABLEn in BIOS. Below are the bit fields of that register. Each bit corresponds to a particular Sub-IP in OSE. When the FEATURE_DISABLE for that SubIP is set, OSE HW will clock gate the SubIP. If FW tries to access the clock-gated SubIP, then the access would result in a fabric timeout error/interrupt. FW has to then follow the error recovery process.

2.2.103 Fuse Disable 0 (FUSE_DISABLE_REG_0_LH2OSE) - Offset C50h

Fuse Disable Info Register for LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Ownership Device7 (TGPIO_FUSE_DISABLE):** TGPIO Fuse Disable.When these fuses are set to disable the corresponding IPs - it is expected that BIOS will disable the corresponding PCI configuration space of the IP and program the ownership to NULL.
2	0h RO	**Reserved**
1	0h RO	**Ownership Device6 (QEP_FUSE_DISABLE):** QEP Fuse Disable.When these fuses are set to disable the corresponding IPs - it is expected that BIOS will disable the corresponding PCI configuration space of the IP and program the ownership to NULL.
0	0h RO	**Interrupt Delivery Device5 (PWM_FUSE_DISABLE):** PWM Fuse Disable.When these fuses are set to disable the corresponding IPs - it is expected that BIOS will disable the corresponding PCI configuration space of the IP and program the ownership to NULL.

2.2.104 LH2OSE ISH BIOS Selfshoot Reset (ISH_BIOS_SELFSHOOT_RST_LH2OSE) - Offset C54h

Though writeable by LH2OSE, this register is reserved for LH2OSE, LH2OSE should not write to this register. The reset register is a 32 bit register that can be written by BIOS. Setting bit 1 will cause ARM M7 to reset.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**BIOS_RESET_BIT:** ISH BIOS Self shoot Reset Register 1 -> Reset active 0 -> Reset inactive.

2.2.105 Reg DASHBOARD_CP0 (DASHBOARD_CP0) - Offset 4000h

Control Policy for Dashboard.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4000h	01200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	01200010h RW	**DASH_BOARD_CP_0:** SAI bits that can change this register, the Loader and verifier WAC registers and all other registers in the dashboard. Reads accesses are not restricted.

2.2.106 Reg DASHBOARD_CP1 (DASHBOARD_CP1) - Offset 4004h

Control Policy for Dashboard.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4004h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**DASH_BOARD_CP_1:** SAI bits that can change this register, the Loader and verifier WAC registers and all other registers in the dashboard. Reads accesses are not restricted.

2.2.107 Reg DASHBOARD_LDR_WAP0 (DASHBOARD_LDR_WAP0) - Offset 4008h

WAC for the Loader Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4008h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**DASH_BOARD_LDR_WAP_0:** SAI bits that can write the dashboard registers related to the Loader. Reads accesses are not restricted. The writes to this register should only be allowed to SAI s listed in the Control Policy Register.These WAC policies protect the below registers. 1. Loader Address and status_1 to 4 2. Loader Error Status 3. IP General Purpose Registers 1 and 2

2.2.108 Reg DASHBOARD_LDR_WAP1 (DASHBOARD_LDR_WAP1) - Offset 400Ch

WAC for the Loader Registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 400Ch	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**DASH_BOARD_LDR_WAP_1:** SAI bits that can write the dashboard registers related to the Loader. Reads accesses are not restricted. The writes to this register should only be allowed to SAI s listed in the Control Policy Register.These WAC policies protect the below registers. 1. Loader Address and status_1 to 4 2. Loader Error Status 3. IP General Purpose Registers 1 and 2

2.2.109 Reg DASHBOARD_VRF_WAP0 (DASHBOARD_VRF_WAP0) - Offset 4010h

Dashboard_Verifier_WAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4010h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**DASH_BOARD_VRF_WAP_0:** SAI bits that can write the dashboard registers related to the verifier. Reads accesses are not restricted. The writes to this register should only be allowed to SAI s listed in the Control Policy Register.These WAC policies protect the below registers. 1. Verifier Address and status_1 to 4 2. Verifier Error Status 3. Verifier Key Material registers 4. IMR Info Registers 5. General Purpose Registers 3 and 4

2.2.110 Reg DASHBOARD_VRF_WAP1 (DASHBOARD_VRF_WAP1) - Offset 4014h

Dashboard_Verifier_WAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4014h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**DASH_BOARD_VRF_WAP_1:** SAI bits that can write the dashboard registers related to the verifier. Reads accesses are not restricted. The writes to this register should only be allowed to SAI s listed in the Control Policy Register.These WAC policies protect the below registers. 1. Verifier Address and status_1 to 4 2. Verifier Error Status 3. Verifier Key Material registers 4. IMR Info Registers 5. General Purpose Registers 3 and 4

2.2.111 Reg IPINFO_REG1_0 (IPINFO_REG1_0) - Offset 4018h

Register describing the IPs capabilities when it comes to loading and verifying images.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4018h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**LOAD_CAP_SOC:** Loader Capabilities expected in another Processor IP (Example Security IP).
27:24	0h RO	**VERF_CAP_TEE:** Verifier Capability expected in IA SW/TEE.
23:20	0h RO	**LOAD_CAP_TEE:** Loader Capabilities expected in IA SW/TEE.
19:16	0h RO	**VERF_CAP_BIOS:** Verifier Capability expected in BIOS.
15:12	0h RO	**LOAD_CAP_BIOS:** Loader Capabilities expected in BIOS.
11:8	0h RO	**VERF_CAP_BUILTIN:** Verifier Capability is built within IP itself.
7:4	0h RO	**LOAD_CAP_BUILTIN:** Loader Capabilities is built within IP itself.
3	0h RO	**INLINE_HASH:** Inline HASHing supported by IP.
2:0	0h RO	**Reserved**

2.2.112 Reg IPINFO_REG1_1 (IPINFO_REG1_1) - Offset 401Ch

Verifier Capability register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 401Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO	**VERF_CAP_SOC:** Verifier capability expected in another Processor IP (Example Security IP).

2.2.113 Reg IPINFO_REG2_0 (IPINFO_REG2_0) - Offset 4020h

IP_Loader_and_Verifier_CAP1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DEBUG_POLICY:** Debug Policy/Mode enabled. This field should be used by the IP to reflect any non-production related states that the IP would like to inform the Loaders and verifiers. 1. Processor Policy that their Security plugin has detected. 2. SW defined encodings for any SW debug modes.
27:24	0h RO	**FLF_SPEC_VER:** SIIP FLF Spec version.
23:16	00h RO	**REVISION_ID:** This should be used by IP s to reflect the below information.
15:0	0000h RO	**IP_DEVICE_ID:** IP Device ID. This field should reflect the PCI Device ID of the IP. It along with the Revision ID will provide a unique ID that loader and verifier agents check to ensure correct firmware is being loaded and verified.

2.2.114 Reg IPINFO_REG2_1 (IPINFO_REG2_1) - Offset 4024h

IP_Loader_and_Verifier_CAP1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

2.2.115 Reg VERF_ERR_STS_REG (VERF_ERR_STS_REG) - Offset 4030h

VERF_ERR_STS_REG.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:12	0h RW	**FW_PUSH_BITS:** Firmware push completed: Optional bits one for each of the four FW instances. These bits should be set by the IP or the verifier when the FW load process is complete. These bits should be connected to an Interrupt to either the IP, or the verifier based on the IP's FW load model. If the IP supports a push model, this bit should interrupt the IP indicating push is complete. If the IP supports a pull model, these bits could interrupt the verifier indicating pull is complete.
11:8	0h RO	**Reserved**
7:4	0h RW	**VERF_ERR_CODE:** Verifying error code: 4 bits that could be used to exchange generic error codes. This error must correspond to the failure bit set in bits 3:0.
3:0	0h RW	**VERF_FAIL_BITS:** Verifying failed: Verifier is expected to set this bit on any failure. There are 4 bits allocated for each of the 4 images that could be loaded. IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.116 Reg VERF_ADDR_REG1_0 (VERF_ADDR_REG1_0) - Offset 4040h

VERF_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_1_0:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM s or to execute from. This register is updated by the verifier once it has finished verifying the IP s firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.117 Reg VERF_ADDR_REG1_1 (VERF_ADDR_REG1_1) - Offset 4044h

VERF_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4044h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_1_1:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM s or to execute from.This register is updated by the verifier once it has finished verifying the IP s firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.118 Reg VERF_SIZE_REG1_0 (VERF_SIZE_REG1_0) - Offset 4048h

VERF_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW/O	**DONE_PUSH_PULL_V1:** Firmware push or pull completed: Optional bits one for each of the four FW instances. These bits should be set by the IP or the verifier when the FW load process is complete. These bits should be connected to an Interrupt to either the IP, or the verifier based on the IP's FW load model. If the IP supports a push model, this bit should interrupt the IP indicating push is complete. If the IP supports a pull model, these bits could interrupt the verifier indicating pull is complete.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_V1:** Optional field indicating the IOSF Root Space to be used by IP to accessing the verifier address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**INTR_V1:** Verification Done: When this bit is set, Verifier will inform the IP (or equivalent HW logic or FW component) that the firmware corresponding to this dashboard register has successfully verified and resides at the physical memory address in bits 63:3. This bit along with the bits in the verifying error status register provide the status of the loading if verifying was triggered but not completed. IP's could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP's controller.

2.2.119 Reg VERF_SIZE_REG1_1 (VERF_SIZE_REG1_1) - Offset 404Ch

VERF_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 404Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_SIZE_REG_1_0:** Size of the image verified by the verifier in KB s. Note that this could only be the first block being verified. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.120 Reg VERF_ADDR_REG2_0 (VERF_ADDR_REG2_0) - Offset 4050h

VERF_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_2_0:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM's or to execute from. This register is updated by the verifier once it has finished verifying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.121 Reg VERF_ADDR_REG2_1 (VERF_ADDR_REG2_1) - Offset 4054h

VERF_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_2_1:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM's or to execute from. This register is updated by the verifier once it has finished verifying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.122 Reg VERF_SIZE_REG2_0 (VERF_SIZE_REG2_0) - Offset 4058h

VERF_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW/O	**DONE_PUSH_PULL_V2:** Firmware push or pull completed: Optional bits one for each of the four FW instances. These bits should be set by the IP or the verifier when the FW load process is complete. These bits should be connected to an Interrupt to either the IP, or the verifier based on the IP's FW load model. If the IP supports a push model, this bit should interrupt the IP indicating push is complete. If the IP supports a pull model, these bits could interrupt the verifier indicating pull is complete.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_V2:** Optional field indicating the IOSF Root Space to be used by IP to accessing the verifier address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**INTR_V2:** Verification Done: When this bit is set, Verifier will inform the IP (or equivalent HW logic or FW component) that the firmware corresponding to this dashboard register has successfully verified and resides at the physical memory address in bits 63:3. This bit along with the bits in the verifying error status register provide the status of the loading if verifying was triggered but not completed.IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.123 Reg VERF_SIZE_REG2_1 (VERF_SIZE_REG2_1) - Offset 405Ch

VERF_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 405Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_SIZE_REG_2_0:** Size of the image verified by the verifier in KB's. Note that this could only be the first block being verified. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.124 Reg VERF_ADDR_REG3_0 (VERF_ADDR_REG3_0) - Offset 4060h

VERF_ADDR_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4060h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_3_0:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM's or to execute form. This register is updated by the verifier once it has finished verifying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.125 Reg VERF_ADDR_REG3_1 (VERF_ADDR_REG3_1) - Offset 4064h

VERF_ADDR_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4064h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_3_1:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM's or to execute from. This register is updated by the verifier once it has finished verifying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.126 Reg VERF_SIZE_REG3_0 (VERF_SIZE_REG3_0) - Offset 4068h

VERF_SIZE_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4068h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW/O	**DONE_PUSH_PULL_V3:** Firmware push or pull completed: Optional bits one for each of the four FW instances. These bits should be set by the IP or the verifier when the FW load process is complete. These bits should be connected to an Interrupt to either the IP, or the verifier based on the IP's FW load model. If the IP supports a push model, this bit should interrupt the IP indicating push is complete. If the IP supports a pull model, these bits could interrupt the verifier indicating pull is complete.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_V3:** Optional field indicating the IOSF Root Space to be used by IP to accessing the verifier address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**INTR_V3:** Verification Done: When this bit is set, Verifier will inform the IP (or equivalent HW logic or FW component) that the firmware corresponding to this dashboard register has successfully verified and resides at the physical memory address in bits 63:3. This bit along with the bits in the verifying error status register provide the status of the loading if verifying was triggered but not completed.IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.127 Reg VERF_SIZE_REG3_1 (VERF_SIZE_REG3_1) - Offset 406Ch

VERF_SIZE_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 406Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_SIZE_REG_3_0:** Size of the image verified by the verifier in KB's. Note that this could only be the first block being verified. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.128 Reg VERF_ADDR_REG4_0 (VERF_ADDR_REG4_0) - Offset 4070h

VERF_ADDR_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4070h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_4_0:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM's or to execute from. This register is updated by the verifier once it has finished verifying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.129 Reg VERF_ADDR_REG4_1 (VERF_ADDR_REG4_1) - Offset 4074h

VERF_ADDR_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4074h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_ADDR_REG_4_1:** Physical address of the image after the verifier has integrity verified the image. This region should point to an integrity protected region only accessible to the verifier and the IP. This address is expected to be used by the IP to fetch the verified image into its local RAM's or to execute from. This register is updated by the verifier once it has finished verifying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the verifying done bit is set. The address is aligned to a single dword.

2.2.130 Reg VERF_SIZE_REG4_0 (VERF_SIZE_REG4_0) - Offset 4078h

VERF_SIZE_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4078h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW/O	**DONE_PUSH_PULL_V4:** Firmware push or pull completed: Optional bits one for each of the four FW instances. These bits should be set by the IP or the verifier when the FW load process is complete. These bits should be connected to an Interrupt to either the IP, or the verifier based on the IP's FW load model. If the IP supports a push model, this bit should interrupt the IP indicating push is complete. If the IP supports a pull model, these bits could interrupt the verifier indicating pull is complete.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_V4:** Optional field indicating the IOSF Root Space to be used by IP to accessing the verifier address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**INTR_V4:** Verification Done: When this bit is set, Verifier will inform the IP (or equivalent HW logic or FW component) that the firmware corresponding to this dashboard register has successfully verified and resides at the physical memory address in bits 63:3. This bit along with the bits in the verifying error status register provide the status of the loading if verifying was triggered but not completed. IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.131 Reg VERF_SIZE_REG4_1 (VERF_SIZE_REG4_1) - Offset 407Ch

VERF_SIZE_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 407Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**VERF_SIZE_REG_4_0:** Size of the image verified by the verifier in KB's. Note that this could only be the first block being verified. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.132 Reg IMR_INFO_ADDR_REG1_0 (IMR_INFO_ADDR_REG1_0) - Offset 4080h

IMR_INFO_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR_INFO_ADDR_REG_1_0:** Physical base address of the IMR memory region allocated by the verifier to the IP.

2.2.133 Reg IMR_INFO_ADDR_REG1_1 (IMR_INFO_ADDR_REG1_1) - Offset 4084h

IMR_INFO_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR_INFO_ADDR_REG_1_1:** Physical base address of the IMR memory region allocated by the verifier to the IP.

2.2.134 Reg IMR_INFO_SIZE_REG1_0 (IMR_INFO_SIZE_REG1_0) - Offset 4088h

IMR_INFO_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4088h	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**REG1_IMR_SIZE1:** Size of the IMR range in KB if the IMR is used and indicated by the address register.
3:1	3h RW	**REG1_ROOT_SPACE:** Optional bits indicating the Root Space to be used by the IP for accessing this address range. This is expected to be used in future if a Processor does not use RS3 to access IMR regions.
0	0h RW	**REG1_ALLOC_STS:** IMR Used: Bits used to indicate that an IMR is allocated by the Processor and the IP should use the values in this register and the size register for its address and size.

2.2.135 Reg IMR_INFO_SIZE_REG1_1 (IMR_INFO_SIZE_REG1_1) - Offset 408Ch

IMR_INFO_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 408Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG1_IMR_SIZE0:** Size of the IMR range in KB if the IMR is used and indicated by the address register.

2.2.136 Reg IMR_INFO_ADDR_REG2_0 (IMR_INFO_ADDR_REG2_0) - Offset 4090h

IMR_INFO_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4090h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR_INFO_ADDR_REG_2_0:** Physical base address of the IMR memory region allocated by the verifier to the IP.

2.2.137 Reg IMR_INFO_ADDR_REG2_1 (IMR_INFO_ADDR_REG2_1) - Offset 4094h

IMR_INFO_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4094h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IMR_INFO_ADDR_REG_2_1:** Physical base address of the IMR memory region allocated by the verifier to the IP.

2.2.138 Reg IMR_INFO_SIZE_REG2_0 (IMR_INFO_SIZE_REG2_0) - Offset 4098h

IMR_INFO_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4098h	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**REG2_IMR_SIZE1:** Size of the IMR range in KB if the IMR is used and indicated by the address register.
3:1	3h RW	**REG2_ROOT_SPACE:** Optional bits indicating the Root Space to be used by the IP for accessing this address range. This is expected to be used in future if a Processor does not use RS3 to access IMR regions.
0	0h RW	**REG2_ALLOC_STS:** IMR Used: Bits used to indicate that an IMR is allocated by the Processor and the IP should use the values in this register and the size register for its address and size.

2.2.139 Reg IMR_INFO_SIZE_REG2_1 (IMR_INFO_SIZE_REG2_1) - Offset 409Ch

IMR_INFO_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 409Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG2_IMR_SIZE0:** Size of the IMR range in KB if the IMR is used and indicated by the address register.

2.2.140 Reg VERF_MAT_ADDR_REG1_0 (VERF_MAT_ADDR_REG1_0) - Offset 4100h

VERF_MATERIAL_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**REG1_PHY_ADDR0:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.
2:1	0h RW	**REG1_ADDR_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.141 Reg VERF_MAT_ADDR_REG1_1 (VERF_MAT_ADDR_REG1_1) - Offset 4104h

VERF_MATERIAL_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG1_PHY_ADDR1:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.

2.2.142 Reg VERF_MAT_SIZE_REG1_0 (VERF_MAT_SIZE_REG1_0) - Offset 4108h

VERF_MATERIAL_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:1	0h RW	**REG1_SIZE_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.143 Reg VERF_MAT_SIZE_REG1_1 (VERF_MAT_SIZE_REG1_1) - Offset 410Ch

VERF_MATERIAL_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 410Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG1_VERF_MAT_SIZE:** Size in KB of the data structure that holds the verification material. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.144 Reg VERF_MAT_ADDR_REG2_0 (VERF_MAT_ADDR_REG2_0) - Offset 4110h

VERF_MATERIAL_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**REG2_PHY_ADDR0:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.
2:1	0h RW	**REG2_ADDR_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.145 Reg VERF_MAT_ADDR_REG2_1 (VERF_MAT_ADDR_REG2_1) - Offset 4114h

VERF_MATERIAL_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG2_PHY_ADDR1:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.

2.2.146 Reg VERF_MAT_SIZE_REG2_0 (VERF_MAT_SIZE_REG2_0) - Offset 4118h

VERF_MATERIAL_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:1	0h RW	**REG2_SIZE_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.147 Reg VERF_MAT_SIZE_REG2_1 (VERF_MAT_SIZE_REG2_1) - Offset 411Ch

VERF_MATERIAL_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 411Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG2_VERF_MAT_SIZE:** Size in KB of the data structure that holds the verification material. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.148 Reg VERF_MAT_ADDR_REG3_0 (VERF_MAT_ADDR_REG3_0) - Offset 4120h

VERF_MATERIAL_ADDR_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**REG3_PHY_ADDR0:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.
2:1	0h RW	**REG3_ADDR_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.149 Reg VERF_MAT_ADDR_REG3_1 (VERF_MAT_ADDR_REG3_1) - Offset 4124h

VERF_MATERIAL_ADDR_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG3_PHY_ADDR1:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.

2.2.150 Reg VERF_MAT_SIZE_REG3_0 (VERF_MAT_SIZE_REG3_0) - Offset 4128h

VERF_MATERIAL_SIZE_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:1	0h RW	**REG3_SIZE_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.151 Reg VERF_MAT_SIZE_REG3_1 (VERF_MAT_SIZE_REG3_1) - Offset 412Ch

VERF_MATERIAL_SIZE_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 412Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG3_VERF_MAT_SIZE:** Size in KB of the data structure that holds the verification material. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.152 Reg VERF_MAT_ADDR_REG4_0 (VERF_MAT_ADDR_REG4_0) - Offset 4130h

VERF_MATERIAL_ADDR_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**REG4_PHY_ADDR0:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.
2:1	0h RW	**REG4_ADDR_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.153 Reg VERF_MAT_ADDR_REG4_1 (VERF_MAT_ADDR_REG4_1) - Offset 4134h

VERF_MATERIAL_ADDR_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG4_PHY_ADDR1:** Physical address of the memory region hosting the verification related material. Verifier SW and trusted agents writing to this region need to agree on the structure of the data at this address.

2.2.154 Reg VERF_MAT_SIZE_REG4_0 (VERF_MAT_SIZE_REG4_0) - Offset 4138h

VERF_MATERIAL_SIZE_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:1	0h RW	**REG4_SIZE_ROOT_SPACE:** Root Space to be used for accessing this address range.
0	0h RO	**Reserved**

2.2.155 Reg VERF_MAT_SIZE_REG4_1 (VERF_MAT_SIZE_REG4_1) - Offset 413Ch

VERF_MATERIAL_SIZE_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 413Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REG4_VERF_MAT_SIZE:** Size in KB of the data structure that holds the verification material. The IP could chose to use this first block of 4KB to pass on additional information on the firmware like if its not in contiguous memory, the address for the next block and the RS information to access it.

2.2.156 Reg IP_GP_REG3_0 (IP_GP_REG3_0) - Offset 4140h

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_0:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.157 Reg IP_GP_REG3_1 (IP_GP_REG3_1) - Offset 4144h

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_1:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.158 Reg IP_GP_REG3_2 (IP_GP_REG3_2) - Offset 4148h

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_2:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.159 Reg IP_GP_REG3_3 (IP_GP_REG3_3) - Offset 414Ch

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 414Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_3:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.160 Reg IP_GP_REG3_4 (IP_GP_REG3_4) - Offset 4150h

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_4:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.161 Reg IP_GP_REG3_5 (IP_GP_REG3_5) - Offset 4154h

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_5:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.162 Reg IP_GP_REG3_6 (IP_GP_REG3_6) - Offset 4158h

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_6:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.163 Reg IP_GP_REG3_7 (IP_GP_REG3_7) - Offset 415Ch

IP_GPREG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 415Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_3_7:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.164 Reg IP_GP_REG4_0 (IP_GP_REG4_0) - Offset 4160h

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_0:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.165 Reg IP_GP_REG4_1 (IP_GP_REG4_1) - Offset 4164h

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_1:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.166 Reg IP_GP_REG4_2 (IP_GP_REG4_2) - Offset 4168h

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_2:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.167 Reg IP_GP_REG4_3 (IP_GP_REG4_3) - Offset 416Ch

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 416Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_3:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.168 Reg IP_GP_REG4_4 (IP_GP_REG4_4) - Offset 4170h

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4170h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_4:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.169 Reg IP_GP_REG4_5 (IP_GP_REG4_5) - Offset 4174h

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4174h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_5:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.170 Reg IP_GP_REG4_6 (IP_GP_REG4_6) - Offset 4178h

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4178h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_6:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.171 Reg IP_GP_REG4_7 (IP_GP_REG4_7) - Offset 417Ch

IP_GPREG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 417Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_4_7:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.172 Reg LOAD_ERR_STS_REG (LOAD_ERR_STS_REG) - Offset 5030h

LOAD_ERR_STS_REG.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	0h RW	**LOAD_ERROR_CODE:** Loading error code: 4 bits that could be used to exchange generic error codes. This error has to correspond to the failure bit set in bits 3:0.
3:0	0h RW	**LOAD_FAIL_BITS:** Loading failed: Loader is expected to set this bit on any failure. There are 4 bits allocated for each of the 4 images that could be loaded. IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.173 Reg INT_MASK_REG (INT_MASK_REG) - Offset 5038h

INT_MASK_REG.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5038h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW	**IP_ACC_DENIED_MASK:** Access Denied mask reg.
19:16	0h RW	**IE_PUSH_PULL_DONE:** Interrupt enable bit for IP push or pull complete. One bit is allocated for each FW instance. By default all interrupts are masked at reset.
15:12	0h RW	**IE_VERF_DONE:** Interrupt enable bit for Verification done. One bit is allocated for each FW instance. By default all interrupts are masked at reset.
11:8	0h RW	**IE_VERIFIER_LOAD_DONE:** Interrupt enable bit for Verifier load complete bit. One bit is allocated for each FW instance. By default all interrupts are masked at reset.
7:4	0h RW	**IE_FW_LOAD_DONE:** Interrupt enable bit for FW loading done. One bit is allocated for each FW instance. By default all interrupts are masked at reset.
3:0	0h RW	**IE_IP_READY:** Interrupt enable bit for IP ready for FW load. One bit is allocated for each FW instance. By default all interrupts are masked at reset.

2.2.174 Reg INT_STS_REG (INT_STS_REG) - Offset 503Ch

INT_STS_REG.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 503Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/1C	**IP_ACC_DENIED_INTR:** Access denied intr reg.
19:16	0h RW/1C	**IE_PUSH_PULL_DONE_INTR:** Interrupt status bit for IP push or pull complete. One bit is allocated for each FW instance. This bit is expected to clear the interrupt to de-assert the interrupt line.
15:12	0h RW/1C	**IE_VERF_DONE_INTR:** Interrupt status bit for Verification done. One bit is allocated for each FW instance. This bit is expected to clear the interrupt to de-assert the interrupt line.
11:8	0h RW/1C	**IE_VERIFIER_LOAD_DONE_INTR:** Interrupt status bit for Verifier load complete bit. One bit is allocated for each FW instance. This bit is expected to clear the interrupt to de-assert the interrupt line.
7:4	0h RW/1C	**IE_FW_LOAD_DONE_INTR:** Interrupt status bit for FW loading done. One bit is allocated for each FW instance. This bit is expected to clear the interrupt to de-assert the interrupt line.
3:0	0h RW/1C	**IE_IP_READY_INTR:** Interrupt status bit for IP ready for FW load. One bit is allocated for each FW instance. This bit is expected to clear the interrupt to de-assert the interrupt line.

2.2.175 Reg LOAD_ADDR_REG1_0 (LOAD_ADDR_REG1_0) - Offset 5040h

LOAD_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_1_0:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP s firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set. The address is aligned to a single dword.

2.2.176 Reg LOAD_ADDR_REG1_1 (LOAD_ADDR_REG1_1) - Offset 5044h

LOAD_ADDR_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5044h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_1_1:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP s firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.177 Reg LOAD_SIZE_REG1_0 (LOAD_SIZE_REG1_0) - Offset 5048h

LOAD_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/O	**VERFIER_COPY_DONE_LD1:** Verifier copy done: This is an optional bit set by the verifier after it has consumed the FW image form he loader and should be used if it needs to communicate to the loader that the buffer indicated by this pair of address and size register can now be reclaimed by the Loader. Note that usage of this bit will imply that the verifier should also be in the WAC of the loader registers.
16	0h RW/O	**IP_READY_LD1:** IP ready for FW download: Optional bits one for each of the four FW instances. These bits should be set by the IP HW or IP ROM when the IP is out of reset and wants to inform outside controllers of that state so that they could begin the enumeration process for FW load. These bits should be connected to an Interrupt to the verifier either via MSI or via SB message to the agent designated as the loader according to the IP Capabilities register.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_LD1:** Optional field indicating the IOSF Root Space to be used by IP to accessing the loader address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**LOAD_DONE_LD1:** Loading Done: When this bit is set, it will inform the verifier that the firmware has successfully loaded into the physical memory address in bits 63:3. This bit along with the bits in the Loading error status register provide the status of the loading if loading was triggered but not completed.IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.178 Reg LOAD_SIZE_REG1_1 (LOAD_SIZE_REG1_1) - Offset 504Ch

LOAD_SIZE_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 504Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_SIZE_REG_1_1:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.179 Reg LOAD_ADDR_REG2_0 (LOAD_ADDR_REG2_0) - Offset 5050h

LOAD_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_2_0:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.180 Reg LOAD_ADDR_REG2_1 (LOAD_ADDR_REG2_1) - Offset 5054h

LOAD_ADDR_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_2_1:** Size of the image for the verifier to verify in KB's. Loader agents need to update this register before updating the loading done bit.

2.2.181 Reg LOAD_SIZE_REG2_0 (LOAD_SIZE_REG2_0) - Offset 5058h

LOAD_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/O	**VERFIER_COPY_DONE_LD2:** Verifier copy done: This is an optional bit set by the verifier after it has consumed the FW image form he loader and should be used if it needs to communicate to the loader that the buffer indicated by this pair of address and size register can now be reclaimed by the Loader. Note that usage of this bit will imply that the verifier should also be in the WAC of the loader registers.
16	0h RW/O	**IP_READY_LD2:** IP ready for FW download: Optional bits one for each of the four FW instances in their respective registers. These bits should be set by the IP HW or first stage FW when the IP is out of reset and wants to inform outside controllers of that state so that they could begin the enumeration process for FW load of this respective stage of FW. These bits should be connected to an Interrupt to the verifier either via MSI or via SB message to the agent designated as the loader according to the IP Capabilities register.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_LD2:** Optional field indicating the IOSF Root Space to be used by IP to accessing the loader address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**LOAD_DONE_LD2:** Loading Done: When this bit is set, it will inform the verifier that the firmware has successfully loaded into the physical memory address in bits 63:3. This bit along with the bits in the Loading error status register provide the status of the loading if loading was triggered but not completed.IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.182 Reg LOAD_SIZE_REG2_1 (LOAD_SIZE_REG2_1) - Offset 505Ch

LOAD_SIZE_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 505Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_SIZE_REG_2_1:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.183 Reg LOAD_ADDR_REG3_0 (LOAD_ADDR_REG3_0) - Offset 5060h

LOAD_ADDR_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5060h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_3_0:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.184 Reg LOAD_ADDR_REG3_1 (LOAD_ADDR_REG3_1) - Offset 5064h

LOAD_ADDR_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5064h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_3_1:** Size of the image for the verifier to verify in KB's. Loader agents need to update this register before updating the loading done bit.

2.2.185 Reg LOAD_SIZE_REG3_0 (LOAD_SIZE_REG3_0) - Offset 5068h

LOAD_SIZE_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5068h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/O	**VERFIER_COPY_DONE_LD3:** Verifier copy done: This is an optional bit set by the verifier after it has consumed the FW image form he loader and should be used if it needs to communicate to the loader that the buffer indicated by this pair of address and size register can now be reclaimed by the Loader. Note that usage of this bit will imply that the verifier should also be in the WAC of the loader registers.
16	0h RW/O	**IP_READY_LD3:** IP ready for FW download: Optional bits one for each of the four FW instances in their respective registers. These bits should be set by the IP HW or first stage FW when the IP is out of reset and wants to inform outside controllers of that state so that they could begin the enumeration process for FW load of this respective stage of FW. These bits should be connected to an Interrupt to the verifier either via MSI or via SB message to the agent designated as the loader according to the IP Capabilities register.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_LD3:** Optional field indicating the IOSF Root Space to be used by IP to accessing the loader address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**LOAD_DONE_LD3:** Loading Done: When this bit is set, it will inform the verifier that the firmware has successfully loaded into the physical memory address in bits 63:3. This bit along with the bits in the Loading error status register provide the status of the loading if loading was triggered but not completed.IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.186 Reg LOAD_SIZE_REG3_1 (LOAD_SIZE_REG3_1) - Offset 506Ch

LOAD_SIZE_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 506Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_SIZE_REG_3_1:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.187 Reg LOAD_ADDR_REG4_0 (LOAD_ADDR_REG4_0) - Offset 5070h

LOAD_ADDR_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5070h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_4_0:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.188 Reg LOAD_ADDR_REG4_1 (LOAD_ADDR_REG4_1) - Offset 5074h

LOAD_ADDR_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5074h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_ADDR_REG_4_1:** Size of the image for the verifier to verify in KB's. Loader agents need to update this register before updating the loading done bit.

2.2.189 Reg LOAD_SIZE_REG4_0 (LOAD_SIZE_REG4_0) - Offset 5078h

LOAD_SIZE_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5078h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/O	**VERFIER_COPY_DONE_LD4:** Verifier copy done: This is an optional bit set by the verifier after it has consumed the FW image form he loader and should be used if it needs to communicate to the loader that the buffer indicated by this pair of address and size register can now be reclaimed by the Loader. Note that usage of this bit will imply that the verifier should also be in the WAC of the loader registers.
16	0h RW/O	**IP_READY_LD4:** IP ready for FW download: Optional bits one for each of the four FW instances in their respective registers. These bits should be set by the IP HW or first stage FW when the IP is out of reset and wants to inform outside controllers of that state so that they could begin the enumeration process for FW load of this respective stage of FW. These bits should be connected to an Interrupt to the verifier either via MSI or via SB message to the agent designated as the loader according to the IP Capabilities register.
15:4	0h RO	**Reserved**
3:1	0h RW/O	**IOSF_ROOT_SPACE_LD4:** Optional field indicating the IOSF Root Space to be used by IP to accessing the loader address range. This is optional information that could be provided by low level firmware components like BIOS or other Processor agents to inform the IP if the physical address being loaded is not in System memory or an IMR region of system memory that is stolen from the OS. IP s should default to use RS0 and use this field only in special cases when they expect to not use OS addressable memory or a memory region accessible by a peer to peer path in the fabrics.
0	0h RW/O	**LOAD_DONE_LD4:** Loading Done: When this bit is set, it will inform the verifier that the firmware has successfully loaded into the physical memory address in bits 63:3. This bit along with the bits in the Loading error status register provide the status of the loading if loading was triggered but not completed.IP s could further optimize the usage of this bit by connecting it to an interrupt towards the host or the IP s controller.

2.2.190 Reg LOAD_SIZE_REG4_1 (LOAD_SIZE_REG4_1) - Offset 507Ch

LOAD_SIZE_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 507Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/O	**LOAD_SIZE_REG_4_1:** Physical address of the image for the verifier to verify. This register is updated by the loader once it has finished copying the IP's firmware image blobs into a physical address in the Processor memory map. These bits should be set before the Loading done bit is set.The address is aligned to a single dword.

2.2.191 Reg IP_HASH_REG1_00 (IP_HASH_REG1_00) - Offset 50C0h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_00:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.192 Reg IP_HASH_REG1_01 (IP_HASH_REG1_01) - Offset 50C4h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_01:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.193 Reg IP_HASH_REG1_02 (IP_HASH_REG1_02) - Offset 50C8h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_02:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.194 Reg IP_HASH_REG1_03 (IP_HASH_REG1_03) - Offset 50CCh

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_03:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.195 Reg IP_HASH_REG1_04 (IP_HASH_REG1_04) - Offset 50D0h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_04:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.196 Reg IP_HASH_REG1_05 (IP_HASH_REG1_05) - Offset 50D4h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_05:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.197 Reg IP_HASH_REG1_06 (IP_HASH_REG1_06) - Offset 50D8h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_06:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.198 Reg IP_HASH_REG1_07 (IP_HASH_REG1_07) - Offset 50DCh

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_07:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.199 Reg IP_HASH_REG1_08 (IP_HASH_REG1_08) - Offset 50E0h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_08:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.200 Reg IP_HASH_REG1_09 (IP_HASH_REG1_09) - Offset 50E4h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_09:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.201 Reg IP_HASH_REG1_10 (IP_HASH_REG1_10) - Offset 50E8h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_10:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.202 Reg IP_HASH_REG1_11 (IP_HASH_REG1_11) - Offset 50ECh

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_11:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.203 Reg IP_HASH_REG1_12 (IP_HASH_REG1_12) - Offset 50F0h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_12:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.204 Reg IP_HASH_REG1_13 (IP_HASH_REG1_13) - Offset 50F4h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_13:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.205 Reg IP_HASH_REG1_14 (IP_HASH_REG1_14) - Offset 50F8h

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_14:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.206 Reg IP_HASH_REG1_15 (IP_HASH_REG1_15) - Offset 50FCh

IP_HASH_REG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_1_15:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.207 Reg IP_HASH_REG2_00 (IP_HASH_REG2_00) - Offset 5100h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_00:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.208 Reg IP_HASH_REG2_01 (IP_HASH_REG2_01) - Offset 5104h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_01:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.209 Reg IP_HASH_REG2_02 (IP_HASH_REG2_02) - Offset 5108h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_02:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.210 Reg IP_HASH_REG2_03 (IP_HASH_REG2_03) - Offset 510Ch

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 510Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_03:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.211 Reg IP_HASH_REG2_04 (IP_HASH_REG2_04) - Offset 5110h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_04:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.212 Reg IP_HASH_REG2_05 (IP_HASH_REG2_05) - Offset 5114h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_05:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.213 Reg IP_HASH_REG2_06 (IP_HASH_REG2_06) - Offset 5118h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_06:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.214 Reg IP_HASH_REG2_07 (IP_HASH_REG2_07) - Offset 511Ch

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 511Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_07:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.215 Reg IP_HASH_REG2_08 (IP_HASH_REG2_08) - Offset 5120h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_08:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.216 Reg IP_HASH_REG2_09 (IP_HASH_REG2_09) - Offset 5124h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_09:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.217 Reg IP_HASH_REG2_10 (IP_HASH_REG2_10) - Offset 5128h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_10:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.218 Reg IP_HASH_REG2_11 (IP_HASH_REG2_11) - Offset 512Ch

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 512Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_11:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.219 Reg IP_HASH_REG2_12 (IP_HASH_REG2_12) - Offset 5130h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_12:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.220 Reg IP_HASH_REG2_13 (IP_HASH_REG2_13) - Offset 5134h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_13:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.221 Reg IP_HASH_REG2_14 (IP_HASH_REG2_14) - Offset 5138h

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_14:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.222 Reg IP_HASH_REG2_15 (IP_HASH_REG2_15) - Offset 513Ch

IP_HASH_REG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 513Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_2_15:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.223 Reg IP_HASH_REG3_00 (IP_HASH_REG3_00) - Offset 5140h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_00:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.224 Reg IP_HASH_REG3_01 (IP_HASH_REG3_01) - Offset 5144h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_01:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.225 Reg IP_HASH_REG3_02 (IP_HASH_REG3_02) - Offset 5148h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_02:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.226 Reg IP_HASH_REG3_03 (IP_HASH_REG3_03) - Offset 514Ch

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 514Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_03:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.227 Reg IP_HASH_REG3_04 (IP_HASH_REG3_04) - Offset 5150h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_04:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.228 Reg IP_HASH_REG3_05 (IP_HASH_REG3_05) - Offset 5154h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_05:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.229 Reg IP_HASH_REG3_06 (IP_HASH_REG3_06) - Offset 5158h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_06:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.230 Reg IP_HASH_REG3_07 (IP_HASH_REG3_07) - Offset 515Ch

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 515Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_07:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.231 Reg IP_HASH_REG3_08 (IP_HASH_REG3_08) - Offset 5160h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_08:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.232 Reg IP_HASH_REG3_09 (IP_HASH_REG3_09) - Offset 5164h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_09:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.233 Reg IP_HASH_REG3_10 (IP_HASH_REG3_10) - Offset 5168h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_10:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.234 Reg IP_HASH_REG3_11 (IP_HASH_REG3_11) - Offset 516Ch

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 516Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_11:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.235 Reg IP_HASH_REG3_12 (IP_HASH_REG3_12) - Offset 5170h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5170h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_12:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.236 Reg IP_HASH_REG3_13 (IP_HASH_REG3_13) - Offset 5174h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5174h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_13:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.237 Reg IP_HASH_REG3_14 (IP_HASH_REG3_14) - Offset 5178h

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5178h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_14:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.238 Reg IP_HASH_REG3_15 (IP_HASH_REG3_15) - Offset 517Ch

IP_HASH_REG3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 517Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_3_15:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.239 Reg IP_HASH_REG4_00 (IP_HASH_REG4_00) - Offset 5180h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_00:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.240 Reg IP_HASH_REG4_01 (IP_HASH_REG4_01) - Offset 5184h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_01:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.241 Reg IP_HASH_REG4_02 (IP_HASH_REG4_02) - Offset 5188h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_02:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.242 Reg IP_HASH_REG4_03 (IP_HASH_REG4_03) - Offset 518Ch

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 518Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_03:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.243 Reg IP_HASH_REG4_04 (IP_HASH_REG4_04) - Offset 5190h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_04:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.244 Reg IP_HASH_REG4_05 (IP_HASH_REG4_05) - Offset 5194h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5194h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_05:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.245 Reg IP_HASH_REG4_06 (IP_HASH_REG4_06) - Offset 5198h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_06:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.246 Reg IP_HASH_REG4_07 (IP_HASH_REG4_07) - Offset 519Ch

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 519Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_07:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.247 Reg IP_HASH_REG4_08 (IP_HASH_REG4_08) - Offset 51A0h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_08:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.248 Reg IP_HASH_REG4_09 (IP_HASH_REG4_09) - Offset 51A4h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_09:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.249 Reg IP_HASH_REG4_10 (IP_HASH_REG4_10) - Offset 51A8h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_10:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.250 Reg IP_HASH_REG4_11 (IP_HASH_REG4_11) - Offset 51ACh

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_11:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.251 Reg IP_HASH_REG4_12 (IP_HASH_REG4_12) - Offset 51B0h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_12:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.252 Reg IP_HASH_REG4_13 (IP_HASH_REG4_13) - Offset 51B4h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_13:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.253 Reg IP_HASH_REG4_14 (IP_HASH_REG4_14) - Offset 51B8h

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_14:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.254 Reg IP_HASH_REG4_15 (IP_HASH_REG4_15) - Offset 51BCh

IP_HASH_REG4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_HASH_4_15:** HASH of the image being verified. This register should be used to pass on the HASH of the image from the loader to the verifier in case they are not one and the same or in the case the IP itself is doing the loader role while the verifier is some external IP.This register needs to be enabled in IP's that have direct access to storage and can DMA or copy data to an external verifier. The IP should also support HASH algorithms in either SW or HW to make use of this register.

2.2.255 Reg IP_GP_REG1_0 (IP_GP_REG1_0) - Offset 5200h

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_0:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.256 Reg IP_GP_REG1_1 (IP_GP_REG1_1) - Offset 5204h

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_1:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.257 Reg IP_GP_REG1_2 (IP_GP_REG1_2) - Offset 5208h

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_2:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.258 Reg IP_GP_REG1_3 (IP_GP_REG1_3) - Offset 520Ch

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 520Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_3:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.259 Reg IP_GP_REG1_4 (IP_GP_REG1_4) - Offset 5210h

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_4:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.260 Reg IP_GP_REG1_5 (IP_GP_REG1_5) - Offset 5214h

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_5:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.261 Reg IP_GP_REG1_6 (IP_GP_REG1_6) - Offset 5218h

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_6:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.262 Reg IP_GP_REG1_7 (IP_GP_REG1_7) - Offset 521Ch

IP_GPREG1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 521Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_1_7:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.263 Reg IP_GP_REG2_0 (IP_GP_REG2_0) - Offset 5220h

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_0:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.264 Reg IP_GP_REG2_1 (IP_GP_REG2_1) - Offset 5224h

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5224h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_1:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.265 Reg IP_GP_REG2_2 (IP_GP_REG2_2) - Offset 5228h

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_2:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.266 Reg IP_GP_REG2_3 (IP_GP_REG2_3) - Offset 522Ch

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 522Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_3:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.267 Reg IP_GP_REG2_4 (IP_GP_REG2_4) - Offset 5230h

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_4:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.268 Reg IP_GP_REG2_5 (IP_GP_REG2_5) - Offset 5234h

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_5:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.269 Reg IP_GP_REG2_6 (IP_GP_REG2_6) - Offset 5238h

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_6:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.270 Reg IP_GP_REG2_7 (IP_GP_REG2_7) - Offset 523Ch

IP_GPREG2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 523Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**IP_GPR_2_7:** Optional general purpose registers for any customized information that needs to be exchanged with IP.

2.2.271 Reg IP_ACCESS_LOG_REG (IP_ACCESS_LOG_REG) - Offset 5240h

IP_ACCESS_LOG.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**IP_ACC_ADDR_LOG:** Access log reg.
0	0h RO	**IP_ACC_RW_LOG:** Access log reg.

2.2.272 Control Policy Low (OSE_SEC_REG_LOW) - Offset 6000h

LSB 32 bit Register for configuring Control Policy.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6000h	01200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	01200010h RW	**Control Policy (LOW):** Bits 31:0.

2.2.273 Control Policy High (OSE_SEC_REG_HIGH) - Offset 6004h

MSB 32 bit Register for configuring Control Policy.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6004h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**Control Policy (HIGH):** Bits 63:32.

2.2.274 OSE_OWNED_IP_RAC_LOW - Offset 6008h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6008h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.275 OSE_OWNED_IP_RAC_HIGH - Offset 600Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 600Ch	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.276 OSE_OWNED_IP_WAC_LOW - Offset 6010h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6010h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.277 OSE_OWNED_IP_WAC_HIGH - Offset 6014h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6014h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.278 OSE_LH_OWNED_IP_RAC_LOW - Offset 6018h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6018h	0120001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0120001Fh RW	**LOW:** Bits 31:0.

2.2.279 OSE_LH_OWNED_IP_RAC_HIGH - Offset 601Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 601Ch	00000E20h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E20h RW	**HIGH:** Bits 63:32.

2.2.280 OSE_LH_OWNED_IP_WAC_LOW - Offset 6020h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6020h	0120001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0120001Fh RW	**LOW:** Bits 31:0.

2.2.281 OSE_LH_OWNED_IP_WAC_HIGH - Offset 6024h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6024h	00000E20h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E20h RW	**HIGH:** Bits 63:32.

2.2.282 NULL_OWNED_IP_RAC_LOW - Offset 6028h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6028h	01200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	01200010h RW	**LOW:** Bits 31:0.

2.2.283 NULL_OWNED_IP_RAC_HIGH - Offset 602Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 602Ch	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.284 NULL_OWNED_IP_WAC_LOW - Offset 6030h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6030h	01200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	01200010h RW	**LOW:** Bits 31:0.

2.2.285 NULL_OWNED_IP_WAC_HIGH - Offset 6034h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6034h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.286 LH2OSE_IPC_OS_REGION_RAC_LOW - Offset 6038h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6038h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.287 LH2OSE_IPC_OS_REGION_RAC_HIGH - Offset 603Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 603Ch	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.288 LH2OSE_IPC_OS_REGION_WAC_LOW - Offset 6040h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6040h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.289 LH2OSE_IPC_OS_REGION_WAC_HIGH - Offset 6044h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6044h	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.290 LH2OSE_IPC_BIOS_REGION_RAC_LOW - Offset 6048h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6048h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.291 LH2OSE_IPC_BIOS_REGION_RAC_HIGH - Offset 604Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 604Ch	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.292 LH2OSE_IPC_BIOS_REGION_WAC_LOW - Offset 6050h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6050h	01200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	01200010h RW	**LOW:** Bits 31:0.

2.2.293 LH2OSE_IPC_BIOS_REGION_WAC_HIGH - Offset 6054h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6054h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.294 OSE_SRAM_LH2OSE_REG1_REGION_RAC_LOW - Offset 6058h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6058h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.295 OSE_SRAM_LH2OSE_REG1_REGION_RAC_HIGH - Offset 605Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 605Ch	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.296 OSE_SRAM_LH2OSE_REG1_REGION_WAC_LOW - Offset 6060h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6060h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.297 OSE_SRAM_LH2OSE_REG1_REGION_WAC_HIGH - Offset 6064h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6064h	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.298 OSE_SRAM_LH2OSE_REG2_REGION_RAC_LOW - Offset 6068h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6068h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.299 OSE_SRAM_LH2OSE_REG2_REGION_RAC_HIGH - Offset 606Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 606Ch	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.300 OSE_SRAM_LH2OSE_REG2_REGION_WAC_LOW - Offset 6070h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6070h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.301 OSE_SRAM_LH2OSE_REG2_REGION_WAC_HIGH - Offset 6074h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6074h	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.302 OSE_SRAM_LH2OSE_REG3_REGION_RAC_LOW - Offset 6078h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6078h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.303 OSE_SRAM_LH2OSE_REG3_REGION_RAC_HIGH - Offset 607Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 607Ch	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.304 OSE_SRAM_LH2OSE_REG3_REGION_WAC_LOW - Offset 6080h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6080h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.305 OSE_SRAM_LH2OSE_REG3_REGION_WAC_HIGH - Offset 6084h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6084h	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.306 OSE_LH2OSE_SRAM_GBEPROXY_REGION_RAC_LOW - Offset 6088h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6088h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.307 OSE_LH2OSE_SRAM_GBEPROXY_REGION_RAC_HIGH - Offset 608Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 608Ch	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.308 OSE_LH2OSE_SRAM_GBEPROXY_REGION_WAC_LOW - Offset 6090h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6090h	0520001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0520001Fh RW	**LOW:** Bits 31:0.

2.2.309 OSE_LH2OSE_SRAM_GBEPROXY_REGION_WAC_HIGH - Offset 6094h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6094h	00000E00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000E00h RW	**HIGH:** Bits 63:32.

2.2.310 OSE_CSE_IPC_RAC_LOW - Offset 6098h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6098h	05210010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05210010h RW	**LOW:** Bits 31:0.

2.2.311 OSE_CSE_IPC_RAC_HIGH - Offset 609Ch

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 609Ch	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.312 OSE_CSE_IPC_WAC_LOW - Offset 60A0h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60A0h	05210010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05210010h RW	**LOW:** Bits 31:0.

2.2.313 OSE_CSE_IPC_WAC_HIGH - Offset 60A4h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60A4h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.314 OSE_PMC_IPC_RAC_LOW - Offset 60A8h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60A8h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.315 OSE_PMC_IPC_RAC_HIGH - Offset 60ACh

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60ACh	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.316 OSE_PMC_IPC_WAC_LOW - Offset 60B0h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60B0h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.317 OSE_PMC_IPC_WAC_HIGH - Offset 60B4h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60B4h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

2.2.318 OSE_AUDIO_IPC_RAC_LOW - Offset 60B8h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60B8h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.319 OSE_AUDIO_IPC_RAC_HIGH - Offset 60BCh

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60BCh	00020C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00020C00h RW	**HIGH:** Bits 63:32.

2.2.320 OSE_AUDIO_IPC_WAC_LOW - Offset 60C0h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60C0h	05200010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200010h RW	**LOW:** Bits 31:0.

2.2.321 OSE_AUDIO_IPC_WAC_HIGH - Offset 60C4h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60C4h	00020C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00020C00h RW	**HIGH:** Bits 63:32.

2.2.322 OSE_SBEP_WAC_LOW - Offset 60C8h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60C8h	07210010h

Bit Range	Default & Access	Field Name (ID): Description
31:0	07210010h RW	**LOW:** Bits 31:0.

2.2.323 OSE_SBEP_WAC_HIGH - Offset 60CCh

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60CCh	00020C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00020C00h RW	**HIGH:** Bits 63:32.

2.2.324 OSE_SBEP_BOOTPREP_WAC_LOW - Offset 60D0h

LSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60D0h	05200000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	05200000h RW	**LOW:** Bits 31:0.

2.2.325 OSE_SBEP_BOOTPREP_WAC_HIGH - Offset 60D4h

MSB 32 bit Register for configuring Policy/Range.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60D4h	00000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000C00h RW	**HIGH:** Bits 63:32.

3 TSN GbE Controller

3.1 TSN GbE Configuration Registers Summary

This registers of the Intel® PSE devices. This contains multiple Intel® PSE TSN GbE Controller devices:

- Intel® PSE TSN GbE Controller #0 - Bus: 0, Device: 29, Function: 1
- Intel® PSE TSN GbE Controller #1 - Bus: 0, Device: 29, Function: 2

DID Values:

- Intel® PSE TSN GbE Controller #0 - D29: F1
  - 4BA0h (RGMII: 1Gb Mode)
  - 4BA1h (SGMII: 1Gb Mode)
  - 4BA2h (SGMII: 2.5Gb Mode)
- Intel® PSE TSN GbE Controller #1 - D29: F2
  - 4BB0h (RGMII: 1Gb Mode)
  - 4BB1h (SGMII: 1Gb Mode)
  - 4BB2h (SGMII: 2.5Gb Mode)

The Function is discovered by software as a Root Complex integrated Endpoint (RCiEP). The PCI Bus Number, Device Number, and Function Number are assigned by the PCH design and not enumerated. Because it is an RCiEP, some of the register fields are designed to be altered by BIOS for a particular system implementation.

Note: BIOS has the capability to disable software access to the PCI Configuration Space of this Function. When disabled, the Function returns Unsupported Request (UR) to requests to access its configuration registers.

Table 3-1. Summary of Bus: 0, Devices: 29, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID Register (DEVVENDID)	4BAx0000h
4h	4	Status and Command (STATUSCOMMAND)	00100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	00000000h
Ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	00000000h
10h	4	Base Address Register (BAR)	00000000h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000100h
40h	4	PCIe Capabilities Register (PCIECAPREG)	00920010h
44h	4	PCIe Device Capability Register (DEVCAPREG)	10008FC0h
48h	4	PCIe Device Control Status Register (DEVCTRLSTAT)	00000000h
64h	4	PCIe Device Capability2 Register (DEVCAPREG2)	00000000h
68h	4	PCIe Device Control2 Status Register (DEVCTRLSTAT2)	00000000h
80h	4	Power Management Capability ID (POWERCAPID)	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1)	00000000h
B4h	4	General Purpose Read Write Register2 (GEN_PCI_REGRW2)	00000000h
B8h	4	General Purpose Read Write Register3 (GEN_PCI_REGRW3)	00000000h
BCh	4	General Purpose Read Write Register4 (GEN_PCI_REGRW4)	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG)	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW)	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH)	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA)	00000000h
E0h	4	MSI Mask Register (MSI_MASK)	00000000h
E4h	4	MSI Pending Register (MSI_PENDING)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

3.1.1 Device ID and Vendor ID Register (DEVVENDID) — Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BAxh RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device - 4BA0h (RGMII: 1Gb Mode) - 4BA1h (SGMII: 1Gb Mode) - 4BA2h (SGMII: 2.5Gb Mode)
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

3.1.2 Status and Command (STATUSCOMMAND) — Offset 4h

Command Register and Status Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** If '1', SB Interrupt generation is disabled If '0', SB Interrupt generation is enabled
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

3.1.3 Revision ID and Class Code (REVCLASSCODE) — Offset 8h

Revision ID register and Class Code Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision Id Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

3.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST) — Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MultifunctionDevice Field (MULFNDEV):** Multi-Function Device: This bit is set only if the device has multiple functions. For VF, this bit is set to 0
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size: Does not apply to PCI Express. PCI Express spec requires this to be implemented as an R/W register but has no functional impact on the AMBA Device connected. This field is RO and tied to 0 for VFs.

3.1.5 Base Address Register (BAR) — Offset 10h

Base Address Register low [31:2] type[2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

3.1.6 Base Address Register High (BAR_HIGH) — Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

3.1.7 Base Address Register1 (BAR1) — Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

3.1.8 Base Address Register1 High (BAR1_HIGH) — Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH Register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

3.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) — Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

3.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) — Offset 30h

Expansion ROM Base Address Register is a RO indicates support for Expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

3.1.11 Capabilities Pointer (CAPABILITYPTR) — Offset 34h

Capabilities Pointer Register indicates what the next capability is.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

3.1.12 Interrupt Register (INTERRUPTREG) — Offset 3Ch

Interrupt Line Register isn't used in Bridge directly Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT Register indicating the requirement of latency timers and MAX_LAT Register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

3.1.13 PCIe Capabilities Register (PCIECAPREG) — Offset 40h

PCIe Capabilities Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 40h	00920010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO/V	**Interrupt Message Number Field (INTR_MSG_NUM):** PCIe Interrupt Message Number
24	0h RO	**Slot Implemented Field (SLOT_IMPLEMENTED):** Slot Implemented. Tied to 0
23:20	9h RO	**Dev Port Type Field (DEV_PORT_TYPE):** Device Port Type. Taken from strap
19:16	2h RO	**Cap Version Field (CAP_VER):** PCI Capability Version
15:8	00h RO	**Next Capability Pointer Field (NEXT_CAP_PTR):** Next Capability Pointer
7:0	10h RO	**Capability ID Field (PCIE_CAP_ID):** PCIe Capability ID

3.1.14 PCIe Device Capability Register (DEVCAPREG) — Offset 44h

PCIe Device Cap Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 44h	10008FC0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**FLR Capability Field (FLR_CAP):** FLR Capability
27:26	0h RO	**Captured Slot Power Limit Scale Field (CAP_SLOT_PWR_LIM_SCALE):** Captured Slot Power Limit Scale. Tied to 0
25:18	00h RO	**Captured Slot Power Limit Value Field (CAP_SLOT_PWR_LIM_VAL):** Captured Slot Power Limit Value. Tied to 0
17:16	0h RO	**Reserved**
15	1h RO	**RB error PTR Field (RB_ERR_RPTR):** Role Based Error Reporting
14:12	0h RO	**Reserved**
11:9	7h RO	**EP L01 Acceptable Latency Field (EP_L1_ACC_LAT):** L1 Acceptable Latency
8:6	7h RO	**EP L0 Acceptable Latency Field (EP_L0_ACC_LAT):** L0 Acceptable Latency
5	0h RO	**ETF Support Field (ETF_SUPPORT):** Extended Tag Field Support
4:3	0h RO	**Phantom Functions Support Field (PHANTOM_FUNC_SUPPORT):** Phantom Functions SUPPORT. NA for Bridge
2:0	0h RO	**Max Pl Size Support Field (MAX_PL_SIZE_SUPPORT):** Max Payload Size

3.1.15 PCIe Device Control Status Register (DEVCTRLSTAT) — Offset 48h

PCIe Device Status Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO/V	**TXN Pending Field (TXN_PENDING):** Transaction Pending bit
20	0h RO	**Aux Power Detected Field (AUX_PWR_DETECTED):** Aux Power Detected. Always tied to 0
19	0h RW/1C	**UR Field (UR_DETECTED):** Unsupported Request Detected
18	0h RW/1C	**Fatal Error Detected Field (FER_DETECTED):** Fatal Error Detected
17	0h RO	**Non Fatal Err Detected Field (NFER_DETECTED):** Non Fatal Error Detected
16	0h RO	**Correctable Error Detected Field (CER_DETECTED):** Correctable Error Detected
15	0h WO	**Initiate FLR Field (INITIATE_FLR):** Initiate Function Level Reset
14:12	0h RO	**Max Read Request Size Field (MAX_RD_REQ_SIZE):** Max Read Request Size
11	0h RW	**Enable No Snoop Field (EN_NS):** Enable No Snoop
10	0h RO	**Aux Power Detected Field (AUX_PWR_PM_EN):** Aux Power Enable
9	0h RO	**Phantom Function En Field (PHANTOM_FUNC_EN):** Phantom Function Enable. Not support by Bridge
8	0h RW	**ETF En Field (ETF_EN):** Extended Tag Field Enable
7:5	0h RO	**Max Payload Size Field (MAX_PL_SIZE):** Maximum Payload Size
4	0h RW	**Enable Relaxed Ordering Field (EN_RO):** Enable Relaxed Ordering
3	0h RW	**UR Reporting En Field (URR_EN):** Unsupported Request Reporting Enable
2	0h RW	**Fatal Err Reporting En Field (FER_EN):** Fatal Error Reporting Enable
1	0h RW	**Non Fatal Err Reporting En Field (NFER_EN):** Non Fatal Error Reporting Enable
0	0h RW	**Correctable Error Reporting En Field (CER_EN):** Correctable Error Reporting Enable

3.1.16 PCIe Device Capability2 Register (DEVCAPREG2) — Offset 64h

PCIe Device Cap Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RO	**Max End2end TLP Prefix Field (MAX_EE_TLP_PREFIXES):** Max End2End TLP Prefixes
21	0h RO	**End2end TLP Prefix Supported Field (EE_TLP_PREFIX_SUPPORT):** End2End TLP Prefixes Support
20	0h RO	**Ext Format Support Field (EXTD_FMT_SUPPORT):** Extended Format Support
19:18	0h RO	**OBFF Support Field (OBFF_SUPPORT):** PCI OBFF Support
17:14	0h RO	**Reserved**
13:12	0h RO	**TPH Completer Supported Field (TPH_CPL_SUPPORT):** TPH Completer Support
11	0h RO	**LTR Support Field (LTR_SUPPORT):** LTR Support
10	0h RO	**No RO Enable Field (NRO_EN_PRPR_PASS):** No RO based PR-PR Passing
9	0h RO	**CAS Cpl 128 Support Field (CAS_CPL_SUPPORT_128):** CAS128 Support
8	0h RO	**CAS Cpl 64 Support Field (ATM_OP_CPL_SUPPORT_64):** CAS64 Completion Support
7	0h RO	**CAS Cpl 32 Support Field (ATM_OP_CPL_SUPPORT_32):** CAS32 Completion Support
6	0h RO	**Atomic Operation Routing Field (ATOR_SUPPORT):** Atomic Operation Routing Support
5	0h RO	**PCI Ari Forwarding Support Field (ARI_FWD_SUPPORT):** ARI Forwarding Support
4	0h RO	**Cpl Timeout Disable Support Field (CPL_TO_DIS_SUPPORT):** Completion Timeout Disable Support
3:0	0h RO	**Cpl Timeout Range Support Field (CPL_TO_RNG_SUPPORT):** Completion Timeout Ranges Support

3.1.17 PCIe Device Control2 Status Register (DEVCTRLSTAT2) — Offset 68h

PCIe Device Status Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**End2end TLP Prefix Blocking Field (EE_TLP_PREFIX_EN):** End2End TLP Prefixes Blocking
14:13	0h RO	**OBFF Enable Field (OBFF_EN):** OBFF Enable
12:11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable Field (LTR_MECH_EN):** LTR Mechanism Enable
9	0h RO	**IDO Based Cpl Enable Field (IDO_CPL_EN):** IDO Completion Enable
8	0h RO	**IDO Based Request Enable Field (IDO_REQ_EN):** IDO Request Enable
7	0h RO	**Atomic Op Egress Blocking Field (ATM_OP_EGR_BLK):** Atomic Operation Egress Blocking
6	0h RO	**Atomic Op Requester Enable Field (ATM_OP_REQ_EN):** Atomic Operation Requester Enable
5	0h RO	**ARI Fwd Enable Field (ARI_FWD_EN):** ARI Forwarding Enable
4	0h RW	**Cpl Timeout Disable Field (CPL_TO_DIS):** Completion Timeout Disable Support
3:0	0h RW	**Cpl Timeout Value Field (CPL_TO_VAL):** Completion Timeout Value

3.1.18 Power Management Capability ID (POWERCAPID) — Offset 80h

Power Management Capability ID Register points to Next Capability Structure and Power Management Capability with pOwer Management Capabilities Register for PME Support and Version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

3.1.19 Power Management Control and Status Register (PMECTRLSTATUS) — Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable No Soft Reset and Power State.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AMBA Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on Sideband is disabled.
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current power state and to set a new power state

3.1.20 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

3.1.21 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) — Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1]+ 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

3.1.22 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR DWord Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

3.1.23 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE Pointer Register giving details on Device MMIO Offset, Location BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 DWord Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR NUM: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

3.1.24 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and Power Control Enable Register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable: If 1, then hardware may request power gating whenever it has reached an idle condition.
20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** SE: Sleep Enable: If 1, then the function may assert Sleep during power gating. If 0, then function will never asset Sleep to the retention flops. Note that some platforms may default this bit to 0, others to 1.
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If 1, then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

3.1.25 General Purpose Read Write Register1 (GEN_PCI_REGRW1) — Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

3.1.26 General Purpose Read Write Register2 (GEN_PCI_REGRW2) — Offset B4h

General Purpose PCI Read Write Register2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW2):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW2

3.1.27 General Purpose Read Write Register3 (GEN_PCI_REGRW3) — Offset B8h

General Purpose PCI Read Write Register3.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW3):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW3

3.1.28 General Purpose Read Write Register4 (GEN_PCI_REGRW4) — Offset BCh

General Purpose PCI Read Write Register4.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW4):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW4

3.1.29 General Purpose Input Register (GEN_INPUT_REG) — Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

3.1.30 MSI Capability Register (MSI_CAP_REG) — Offset D0h

MSI Capability Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable: If 1, then the PCI Device is allowed to use MSI to request service. The PCI Device is prohibited to use INTx, when MSI is enabled If 0, then the PCI Device is prohibited from using MSI to request service.
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

3.1.31 MSI Message Low Address (MSI_ADDR_LOW) — Offset D4h

MSI Message Low Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

3.1.32 MSI Message High Address (MSI_ADDR_HIGH) — Offset D8h

MSI Message High Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

3.1.33 MSI Message Data (MSI_MSG_DATA) — Offset DCh

MSI Message Data.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

3.1.34 MSI Mask Register (MSI_MASK) — Offset E0h

MSI Mask Bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

3.1.35 MSI Pending Register (MSI_PENDING) — Offset E4h

MSI Pending Bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

3.1.36 Manufacturers ID (MANID) — Offset F8h

Manufacturers ID register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:1] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps.

3.2 TSN GbE Memory Mapped Registers Summary

These are the I/O Registers in Memory Space for this Function that are accessible to BIOS and software running on the Host Root (RS0) processor. The Base Address Register (BAR) is located at offset 10h in PCI Configuration Space.

Table 3-2. Summary of TSN GbE Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MAC_CONFIGURATION	00000000h
4h	4	MAC_EXT_CONFIGURATION	00000000h
8h	4	MAC_PACKET_FILTER	00000000h
Ch	4	MAC_WATCHDOG_TIMEOUT	00000000h
10h	4	MAC_HASH_TABLE_REG0	00000000h
14h	4	MAC_HASH_TABLE_REG1	00000000h
50h	4	MAC_VLAN_TAG_CTRL	00000000h
54h	4	MAC_VLAN_TAG_DATA	00000000h
58h	4	MAC_VLAN_HASH_TABLE	00000000h
60h	4	MAC_VLAN_INCL	00000000h
64h	4	MAC_INNER_VLAN_INCL	00000000h
70h	4	MAC_Q0_TX_FLOW_CTRL	00000000h
74h	4	MAC_Q1_TX_FLOW_CTRL	00000000h
78h	4	MAC_Q2_TX_FLOW_CTRL	00000000h
7Ch	4	MAC_Q3_TX_FLOW_CTRL	00000000h
80h	4	MAC_Q4_TX_FLOW_CTRL	00000000h
84h	4	MAC_Q5_TX_FLOW_CTRL	00000000h
88h	4	MAC_Q6_TX_FLOW_CTRL	00000000h
8Ch	4	MAC_Q7_TX_FLOW_CTRL	00000000h
90h	4	MAC_RX_FLOW_CTRL	00000000h
94h	4	MAC_RXQ_CTRL4	00000000h
98h	4	MAC_TXQ_PRTY_MAP0	00000000h
9Ch	4	MAC_TXQ_PRTY_MAP1	00000000h
A0h	4	MAC_RXQ_CTRL0	00000000h
A4h	4	MAC_RXQ_CTRL1	00000000h
A8h	4	MAC_RXQ_CTRL2	00000000h
ACh	4	MAC_RXQ_CTRL3	00000000h
B0h	4	MAC_INTERRUPT_STATUS	00000000h
B4h	4	MAC_INTERRUPT_ENABLE	00000000h
B8h	4	MAC_RX_TX_STATUS	00000000h
C0h	4	MAC_PMT_CONTROL_STATUS	00000000h
C4h	4	MAC_RWK_PACKET_FILTER	00000000h
D0h	4	MAC_LPI_CONTROL_STATUS	00000000h
D4h	4	MAC_LPI_TIMERS_CONTROL	03E80000h
D8h	4	MAC_LPI_ENTRY_TIMER	00000000h
DCh	4	MAC_1US_TIC_COUNTER	00000063h
F8h	4	MAC_PHYIF_CONTROL_STATUS	00000000h
110h	4	MAC_VERSION	00005152h
114h	4	MAC_DEBUG	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
11Ch	4	MAC_HW_FEATURE0	0EFD73F7h
120h	4	MAC_HW_FEATURE1	119F7A28h
124h	4	MAC_HW_FEATURE2	22DF71C7h
128h	4	MAC_HW_FEATURE3	2C395632h
140h	4	MAC_DPP_FSM_INTERRUPT_STATUS	00000000h
144h	4	MAC_AXI_SLV_DPE_ADDR_STATUS	00000000h
148h	4	MAC_FSM_CONTROL	00000000h
14Ch	4	MAC_FSM_ACT_TIMER	00000000h
150h	4	SNPS_SCS_REG1	00000000h
200h	4	MAC_MDIO_ADDRESS	00000000h
204h	4	MAC_MDIO_DATA	00000000h
208h	4	MAC_GPIO_CONTROL	00000000h
20Ch	4	MAC_GPIO_STATUS	00000000h
210h	4	MAC_ARP_ADDRESS	00000000h
230h	4	MAC_CSR_SW_CTRL	00000000h
234h	4	MAC_FPE_CTRL_STS	00000000h
238h	4	MAC_EXT_CFG1	00000002h
240h	4	MAC_PRESN_TIME_NS	00000000h
244h	4	MAC_PRESN_TIME_UPDT	00000000h
300h	4	MAC_ADDRESS0_HIGH	8000FFFFh
304h	4	MAC_ADDRESS0_LOW	FFFFFFFFh
308h	4	MAC_ADDRESS1_HIGH	0000FFFFh
30Ch	4	MAC_ADDRESS1_LOW	FFFFFFFFh
310h	4	MAC_ADDRESS2_HIGH	0000FFFFh
314h	4	MAC_ADDRESS2_LOW	FFFFFFFFh
318h	4	MAC_ADDRESS3_HIGH	0000FFFFh
31Ch	4	MAC_ADDRESS3_LOW	FFFFFFFFh
320h	4	MAC_ADDRESS4_HIGH	0000FFFFh
324h	4	MAC_ADDRESS4_LOW	FFFFFFFFh
328h	4	MAC_ADDRESS5_HIGH	0000FFFFh
32Ch	4	MAC_ADDRESS5_LOW	FFFFFFFFh
330h	4	MAC_ADDRESS6_HIGH	0000FFFFh
334h	4	MAC_ADDRESS6_LOW	FFFFFFFFh
338h	4	MAC_ADDRESS7_HIGH	0000FFFFh
33Ch	4	MAC_ADDRESS7_LOW	FFFFFFFFh
340h	4	MAC_ADDRESS8_HIGH	0000FFFFh
344h	4	MAC_ADDRESS8_LOW	FFFFFFFFh
348h	4	MAC_ADDRESS9_HIGH	0000FFFFh
34Ch	4	MAC_ADDRESS9_LOW	FFFFFFFFh
350h	4	MAC_ADDRESS10_HIGH	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
354h	4	MAC_ADDRESS10_LOW	FFFFFFFFh
358h	4	MAC_ADDRESS11_HIGH	0000FFFFh
35Ch	4	MAC_ADDRESS11_LOW	FFFFFFFFh
360h	4	MAC_ADDRESS12_HIGH	0000FFFFh
364h	4	MAC_ADDRESS12_LOW	FFFFFFFFh
368h	4	MAC_ADDRESS13_HIGH	0000FFFFh
36Ch	4	MAC_ADDRESS13_LOW	FFFFFFFFh
370h	4	MAC_ADDRESS14_HIGH	0000FFFFh
374h	4	MAC_ADDRESS14_LOW	FFFFFFFFh
378h	4	MAC_ADDRESS15_HIGH	0000FFFFh
37Ch	4	MAC_ADDRESS15_LOW	FFFFFFFFh
380h	4	MAC_ADDRESS16_HIGH	0000FFFFh
384h	4	MAC_ADDRESS16_LOW	FFFFFFFFh
388h	4	MAC_ADDRESS17_HIGH	0000FFFFh
38Ch	4	MAC_ADDRESS17_LOW	FFFFFFFFh
390h	4	MAC_ADDRESS18_HIGH	0000FFFFh
394h	4	MAC_ADDRESS18_LOW	FFFFFFFFh
398h	4	MAC_ADDRESS19_HIGH	0000FFFFh
39Ch	4	MAC_ADDRESS19_LOW	FFFFFFFFh
3A0h	4	MAC_ADDRESS20_HIGH	0000FFFFh
3A4h	4	MAC_ADDRESS20_LOW	FFFFFFFFh
3A8h	4	MAC_ADDRESS21_HIGH	0000FFFFh
3ACh	4	MAC_ADDRESS21_LOW	FFFFFFFFh
3B0h	4	MAC_ADDRESS22_HIGH	0000FFFFh
3B4h	4	MAC_ADDRESS22_LOW	FFFFFFFFh
3B8h	4	MAC_ADDRESS23_HIGH	0000FFFFh
3BCh	4	MAC_ADDRESS23_LOW	FFFFFFFFh
3C0h	4	MAC_ADDRESS24_HIGH	0000FFFFh
3C4h	4	MAC_ADDRESS24_LOW	FFFFFFFFh
3C8h	4	MAC_ADDRESS25_HIGH	0000FFFFh
3CCh	4	MAC_ADDRESS25_LOW	FFFFFFFFh
3D0h	4	MAC_ADDRESS26_HIGH	0000FFFFh
3D4h	4	MAC_ADDRESS26_LOW	FFFFFFFFh
3D8h	4	MAC_ADDRESS27_HIGH	0000FFFFh
3DCh	4	MAC_ADDRESS27_LOW	FFFFFFFFh
3E0h	4	MAC_ADDRESS28_HIGH	0000FFFFh
3E4h	4	MAC_ADDRESS28_LOW	FFFFFFFFh
3E8h	4	MAC_ADDRESS29_HIGH	0000FFFFh
3ECh	4	MAC_ADDRESS29_LOW	FFFFFFFFh
3F0h	4	MAC_ADDRESS30_HIGH	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3F4h	4	MAC_ADDRESS30_LOW	FFFFFFFFh
3F8h	4	MAC_ADDRESS31_HIGH	0000FFFFh
3FCh	4	MAC_ADDRESS31_LOW	FFFFFFFFh
400h	4	MAC_ADDRESS32_HIGH	0000FFFFh
404h	4	MAC_ADDRESS32_LOW	FFFFFFFFh
408h	4	MAC_ADDRESS33_HIGH	0000FFFFh
40Ch	4	MAC_ADDRESS33_LOW	FFFFFFFFh
410h	4	MAC_ADDRESS34_HIGH	0000FFFFh
414h	4	MAC_ADDRESS34_LOW	FFFFFFFFh
418h	4	MAC_ADDRESS35_HIGH	0000FFFFh
41Ch	4	MAC_ADDRESS35_LOW	FFFFFFFFh
420h	4	MAC_ADDRESS36_HIGH	0000FFFFh
424h	4	MAC_ADDRESS36_LOW	FFFFFFFFh
428h	4	MAC_ADDRESS37_HIGH	0000FFFFh
42Ch	4	MAC_ADDRESS37_LOW	FFFFFFFFh
430h	4	MAC_ADDRESS38_HIGH	0000FFFFh
434h	4	MAC_ADDRESS38_LOW	FFFFFFFFh
438h	4	MAC_ADDRESS39_HIGH	0000FFFFh
43Ch	4	MAC_ADDRESS39_LOW	FFFFFFFFh
440h	4	MAC_ADDRESS40_HIGH	0000FFFFh
444h	4	MAC_ADDRESS40_LOW	FFFFFFFFh
448h	4	MAC_ADDRESS41_HIGH	0000FFFFh
44Ch	4	MAC_ADDRESS41_LOW	FFFFFFFFh
450h	4	MAC_ADDRESS42_HIGH	0000FFFFh
454h	4	MAC_ADDRESS42_LOW	FFFFFFFFh
458h	4	MAC_ADDRESS43_HIGH	0000FFFFh
45Ch	4	MAC_ADDRESS43_LOW	FFFFFFFFh
460h	4	MAC_ADDRESS44_HIGH	0000FFFFh
464h	4	MAC_ADDRESS44_LOW	FFFFFFFFh
468h	4	MAC_ADDRESS45_HIGH	0000FFFFh
46Ch	4	MAC_ADDRESS45_LOW	FFFFFFFFh
470h	4	MAC_ADDRESS46_HIGH	0000FFFFh
474h	4	MAC_ADDRESS46_LOW	FFFFFFFFh
478h	4	MAC_ADDRESS47_HIGH	0000FFFFh
47Ch	4	MAC_ADDRESS47_LOW	FFFFFFFFh
480h	4	MAC_ADDRESS48_HIGH	0000FFFFh
484h	4	MAC_ADDRESS48_LOW	FFFFFFFFh
488h	4	MAC_ADDRESS49_HIGH	0000FFFFh
48Ch	4	MAC_ADDRESS49_LOW	FFFFFFFFh
490h	4	MAC_ADDRESS50_HIGH	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
494h	4	MAC_ADDRESS50_LOW	FFFFFFFFh
498h	4	MAC_ADDRESS51_HIGH	0000FFFFh
49Ch	4	MAC_ADDRESS51_LOW	FFFFFFFFh
4A0h	4	MAC_ADDRESS52_HIGH	0000FFFFh
4A4h	4	MAC_ADDRESS52_LOW	FFFFFFFFh
4A8h	4	MAC_ADDRESS53_HIGH	0000FFFFh
4ACh	4	MAC_ADDRESS53_LOW	FFFFFFFFh
4B0h	4	MAC_ADDRESS54_HIGH	0000FFFFh
4B4h	4	MAC_ADDRESS54_LOW	FFFFFFFFh
4B8h	4	MAC_ADDRESS55_HIGH	0000FFFFh
4BCh	4	MAC_ADDRESS55_LOW	FFFFFFFFh
4C0h	4	MAC_ADDRESS56_HIGH	0000FFFFh
4C4h	4	MAC_ADDRESS56_LOW	FFFFFFFFh
4C8h	4	MAC_ADDRESS57_HIGH	0000FFFFh
4CCh	4	MAC_ADDRESS57_LOW	FFFFFFFFh
4D0h	4	MAC_ADDRESS58_HIGH	0000FFFFh
4D4h	4	MAC_ADDRESS58_LOW	FFFFFFFFh
4D8h	4	MAC_ADDRESS59_HIGH	0000FFFFh
4DCh	4	MAC_ADDRESS59_LOW	FFFFFFFFh
4E0h	4	MAC_ADDRESS60_HIGH	0000FFFFh
4E4h	4	MAC_ADDRESS60_LOW	FFFFFFFFh
4E8h	4	MAC_ADDRESS61_HIGH	0000FFFFh
4ECh	4	MAC_ADDRESS61_LOW	FFFFFFFFh
4F0h	4	MAC_ADDRESS62_HIGH	0000FFFFh
4F4h	4	MAC_ADDRESS62_LOW	FFFFFFFFh
4F8h	4	MAC_ADDRESS63_HIGH	0000FFFFh
4FCh	4	MAC_ADDRESS63_LOW	FFFFFFFFh
700h	4	MMC_CONTROL	00000000h
704h	4	MMC_RX_INTERRUPT	00000000h
708h	4	MMC_TX_INTERRUPT	00000000h
70Ch	4	MMC_RX_INTERRUPT_MASK	00000000h
710h	4	MMC_TX_INTERRUPT_MASK	00000000h
714h	4	TX_OCTET_COUNT_GOOD_BAD	00000000h
718h	4	TX_PACKET_COUNT_GOOD_BAD	00000000h
71Ch	4	TX_BROADCAST_PACKETS_GOOD	00000000h
720h	4	TX_MULTICAST_PACKETS_GOOD	00000000h
724h	4	TX_64OCTETS_PACKETS_GOOD_BAD	00000000h
728h	4	TX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
72Ch	4	TX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h
730h	4	TX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
734h	4	TX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
738h	4	TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
73Ch	4	TX_UNICAST_PACKETS_GOOD_BAD	00000000h
740h	4	TX_MULTICAST_PACKETS_GOOD_BAD	00000000h
744h	4	TX_BROADCAST_PACKETS_GOOD_BAD	00000000h
748h	4	TX_UNDERFLOW_ERROR_PACKETS	00000000h
74Ch	4	TX_SINGLE_COLLISION_GOOD_PACKETS	00000000h
750h	4	TX_MULTIPLE_COLLISION_GOOD_PACKETS	00000000h
754h	4	TX_DEFERRED_PACKETS	00000000h
758h	4	TX_LATE_COLLISION_PACKETS	00000000h
75Ch	4	TX_EXCESSIVE_COLLISION_PACKETS	00000000h
760h	4	TX_CARRIER_ERROR_PACKETS	00000000h
764h	4	TX_OCTET_COUNT_GOOD	00000000h
768h	4	TX_PACKET_COUNT_GOOD	00000000h
76Ch	4	TX_EXCESSIVE_DEFERRAL_ERROR	00000000h
770h	4	TX_PAUSE_PACKETS	00000000h
774h	4	TX_VLAN_PACKETS_GOOD	00000000h
778h	4	TX_OSIZE_PACKETS_GOOD	00000000h
780h	4	RX_PACKETS_COUNT_GOOD_BAD	00000000h
784h	4	RX_OCTET_COUNT_GOOD_BAD	00000000h
788h	4	RX_OCTET_COUNT_GOOD	00000000h
78Ch	4	RX_BROADCAST_PACKETS_GOOD	00000000h
790h	4	RX_MULTICAST_PACKETS_GOOD	00000000h
794h	4	RX_CRC_ERROR_PACKETS	00000000h
798h	4	RX_ALIGNMENT_ERROR_PACKETS	00000000h
79Ch	4	RX_RUNT_ERROR_PACKETS	00000000h
7A0h	4	RX_JABBER_ERROR_PACKETS	00000000h
7A4h	4	RX_UNDERSIZE_PACKETS_GOOD	00000000h
7A8h	4	RX_OVERSIZE_PACKETS_GOOD	00000000h
7ACh	4	RX_64OCTETS_PACKETS_GOOD_BAD	00000000h
7B0h	4	RX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
7B4h	4	RX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h
7B8h	4	RX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h
7BCh	4	RX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
7C0h	4	RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
7C4h	4	RX_UNICAST_PACKETS_GOOD	00000000h
7C8h	4	RX_LENGTH_ERROR_PACKETS	00000000h
7CCh	4	RX_OUT_OF_RANGE_TYPE_PACKETS	00000000h
7D0h	4	RX_PAUSE_PACKETS	00000000h
7D4h	4	RX_FIFO_OVERFLOW_PACKETS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7D8h	4	RX_VLAN_PACKETS_GOOD_BAD	00000000h
7DCh	4	RX_WATCHDOG_ERROR_PACKETS	00000000h
7E0h	4	RX_RECEIVE_ERROR_PACKETS	00000000h
7E4h	4	RX_CONTROL_PACKETS_GOOD	00000000h
7ECh	4	TX_LPI_USEC_CNTR	00000000h
7F0h	4	TX_LPI_TRAN_CNTR	00000000h
7F4h	4	RX_LPI_USEC_CNTR	00000000h
7F8h	4	RX_LPI_TRAN_CNTR	00000000h
800h	4	MMC_IPC_RX_INTERRUPT_MASK	00000000h
808h	4	MMC_IPC_RX_INTERRUPT	00000000h
810h	4	RXIPV4_GOOD_PACKETS	00000000h
814h	4	RXIPV4_HEADER_ERROR_PACKETS	00000000h
818h	4	RXIPV4_NO_PAYLOAD_PACKETS	00000000h
81Ch	4	RXIPV4_FRAGMENTED_PACKETS	00000000h
820h	4	RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS	00000000h
824h	4	RXIPV6_GOOD_PACKETS	00000000h
828h	4	RXIPV6_HEADER_ERROR_PACKETS	00000000h
82Ch	4	RXIPV6_NO_PAYLOAD_PACKETS	00000000h
830h	4	RXUDP_GOOD_PACKETS	00000000h
834h	4	RXUDP_ERROR_PACKETS	00000000h
838h	4	RXTCP_GOOD_PACKETS	00000000h
83Ch	4	RXTCP_ERROR_PACKETS	00000000h
840h	4	RXICMP_GOOD_PACKETS	00000000h
844h	4	RXICMP_ERROR_PACKETS	00000000h
850h	4	RXIPV4_GOOD_OCTETS	00000000h
854h	4	RXIPV4_HEADER_ERROR_OCTETS	00000000h
858h	4	RXIPV4_NO_PAYLOAD_OCTETS	00000000h
85Ch	4	RXIPV4_FRAGMENTED_OCTETS	00000000h
860h	4	RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	00000000h
864h	4	RXIPV6_GOOD_OCTETS	00000000h
868h	4	RXIPV6_HEADER_ERROR_OCTETS	00000000h
86Ch	4	RXIPV6_NO_PAYLOAD_OCTETS	00000000h
870h	4	RXUDP_GOOD_OCTETS	00000000h
874h	4	RXUDP_ERROR_OCTETS	00000000h
878h	4	RXTCP_GOOD_OCTETS	00000000h
87Ch	4	RXTCP_ERROR_OCTETS	00000000h
880h	4	RXICMP_GOOD_OCTETS	00000000h
884h	4	RXICMP_ERROR_OCTETS	00000000h
8A0h	4	MMC_FPE_TX_INTERRUPT	00000000h
8A4h	4	MMC_FPE_TX_INTERRUPT_MASK	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8A8h	4	MMC_TX_FPE_FRAGMENT_CNTR	00000000h
8ACh	4	MMC_TX_HOLD_REQ_CNTR	00000000h
8C0h	4	MMC_FPE_RX_INTERRUPT	00000000h
8C4h	4	MMC_FPE_RX_INTERRUPT_MASK	00000000h
8C8h	4	MMC_RX_PACKET_ASSEMBLY_ERR_CNTR	00000000h
8CCh	4	MMC_RX_PACKET_SMD_ERR_CNTR	00000000h
8D0h	4	MMC_RX_PACKET_ASSEMBLY_OK_CNTR	00000000h
8D4h	4	MMC_RX_FPE_FRAGMENT_CNTR	00000000h
900h	4	MAC_L3_L4_CONTROL0	00000000h
904h	4	MAC_LAYER4_ADDRESS0	00000000h
910h	4	MAC_LAYER3_ADDR0_REG0	00000000h
914h	4	MAC_LAYER3_ADDR1_REG0	00000000h
918h	4	MAC_LAYER3_ADDR2_REG0	00000000h
91Ch	4	MAC_LAYER3_ADDR3_REG0	00000000h
930h	4	MAC_L3_L4_CONTROL1	00000000h
934h	4	MAC_LAYER4_ADDRESS1	00000000h
940h	4	MAC_LAYER3_ADDR0_REG1	00000000h
944h	4	MAC_LAYER3_ADDR1_REG1	00000000h
948h	4	MAC_LAYER3_ADDR2_REG1	00000000h
94Ch	4	MAC_LAYER3_ADDR3_REG1	00000000h
B00h	4	MAC_TIMESTAMP_CONTROL	00002000h
B04h	4	MAC_SUB_SECOND_INCREMENT	00000000h
B08h	4	MAC_SYSTEM_TIME_SECONDS	00000000h
B0Ch	4	MAC_SYSTEM_TIME_NANOSECONDS	00000000h
B10h	4	MAC_SYSTEM_TIME_SECONDS_UPDATE	00000000h
B14h	4	MAC_SYSTEM_TIME_NANOSECONDS_UPDATE	00000000h
B18h	4	MAC_TIMESTAMP_ADDEND	00000000h
B1Ch	4	MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS	00000000h
B20h	4	MAC_TIMESTAMP_STATUS	00000000h
B30h	4	MAC_TX_TIMESTAMP_STATUS_NANOSECONDS	00000000h
B34h	4	MAC_TX_TIMESTAMP_STATUS_SECONDS	00000000h
B40h	4	MAC_AUXILIARY_CONTROL	00000000h
B48h	4	MAC_AUXILIARY_TIMESTAMP_NANOSECONDS	00000000h
B4Ch	4	MAC_AUXILIARY_TIMESTAMP_SECONDS	00000000h
B50h	4	MAC_TIMESTAMP_INGRESS_ASYM_CORR	00000000h
B54h	4	MAC_TIMESTAMP_EGRESS_ASYM_CORR	00000000h
B58h	4	MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND	00000000h
B5Ch	4	MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND	00000000h
B60h	4	MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC	00000000h
B64h	4	MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B68h	4	MAC_TIMESTAMP_INGRESS_LATENCY	00000000h
B6Ch	4	MAC_TIMESTAMP_EGRESS_LATENCY	00000000h
B70h	4	MAC_PPS_CONTROL	00000000h
B80h	4	MAC_PPS0_TARGET_TIME_SECONDS	00000000h
B84h	4	MAC_PPS0_TARGET_TIME_NANOSECONDS	00000000h
B88h	4	MAC_PPS0_INTERVAL	00000000h
B8Ch	4	MAC_PPS0_WIDTH	00000000h
B90h	4	MAC_PPS1_TARGET_TIME_SECONDS	00000000h
B94h	4	MAC_PPS1_TARGET_TIME_NANOSECONDS	00000000h
B98h	4	MAC_PPS1_INTERVAL	00000000h
B9Ch	4	MAC_PPS1_WIDTH	00000000h
BC0h	4	MAC_PTO_CONTROL	00000000h
BC4h	4	MAC_SOURCE_PORT_IDENTITY0	00000000h
BC8h	4	MAC_SOURCE_PORT_IDENTITY1	00000000h
BCCh	4	MAC_SOURCE_PORT_IDENTITY2	00000000h
BD0h	4	MAC_LOG_MESSAGE_INTERVAL	00000000h
C00h	4	MTL_OPERATION_MODE	00000000h
C08h	4	MTL_DBG_CTL	00000000h
C0Ch	4	MTL_DBG_STS	00000018h
C10h	4	MTL_FIFO_DEBUG_DATA	00000000h
C20h	4	MTL_INTERRUPT_STATUS	00000000h
C30h	4	MTL_RXQ_DMA_MAP0	00000000h
C34h	4	MTL_RXQ_DMA_MAP1	00000000h
C40h	4	MTL_TBS_CTRL	00000000h
C50h	4	MTL_EST_CONTROL	00000000h
C58h	4	MTL_EST_STATUS	00000000h
C60h	4	MTL_EST_SCH_ERROR	00000000h
C64h	4	MTL_EST_FRM_SIZE_ERROR	00000000h
C68h	4	MTL_EST_FRM_SIZE_CAPTURE	00000000h
C70h	4	MTL_EST_INTR_ENABLE	00000000h
C80h	4	MTL_EST_GCL_CONTROL	00000000h
C84h	4	MTL_EST_GCL_DATA	00000000h
C90h	4	MTL_FPE_CTRL_STS	00000000h
C94h	4	MTL_FPE_ADVANCE	00000000h
CA0h	4	MTL_RXP_CONTROL_STATUS	80FF00FFh
CA4h	4	MTL_RXP_INTERRUPT_CONTROL_STATUS	00000000h
CA8h	4	MTL_RXP_DROP_CNT	00000000h
CACh	4	MTL_RXP_ERROR_CNT	00000000h
CB0h	4	MTL_RXP_INDIRECT_ACC_CONTROL_STATUS	00000000h
CB4h	4	MTL_RXP_INDIRECT_ACC_DATA	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
CC0h	4	MTL_ECC_CONTROL	00000000h
CC4h	4	MTL_SAFETY_INTERRUPT_STATUS	00000000h
CC8h	4	MTL_ECC_INTERRUPT_ENABLE	00000000h
CCCh	4	MTL_ECC_INTERRUPT_STATUS	00000000h
CD0h	4	MTL_ECC_ERR_STS_RCTL	00000000h
CD4h	4	MTL_ECC_ERR_ADDR_STATUS	00000000h
CD8h	4	MTL_ECC_ERR_CNTR_STATUS	00000000h
CE0h	4	MTL_DPP_CONTROL	00000000h
D00h	4	MTL_TXQ0_OPERATION_MODE	00000000h
D04h	4	MTL_TXQ0_UNDERFLOW	00000000h
D08h	4	MTL_TXQ0_DEBUG	00000000h
D14h	4	MTL_TXQ0_ETS_STATUS	00000000h
D18h	4	MTL_TXQ0_QUANTUM_WEIGHT	00000000h
D2Ch	4	MTL_Q0_INTERRUPT_CONTROL_STATUS	00000000h
D30h	4	MTL_RXQ0_OPERATION_MODE	00000000h
D34h	4	MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT	00000000h
D38h	4	MTL_RXQ0_DEBUG	00000000h
D3Ch	4	MTL_RXQ0_CONTROL	00000000h
D40h	4	MTL_TXQ1_OPERATION_MODE	00000000h
D44h	4	MTL_TXQ1_UNDERFLOW	00000000h
D48h	4	MTL_TXQ1_DEBUG	00000000h
D50h	4	MTL_TXQ1_ETS_CONTROL	00000000h
D54h	4	MTL_TXQ1_ETS_STATUS	00000000h
D58h	4	MTL_TXQ1_QUANTUM_WEIGHT	00000000h
D5Ch	4	MTL_TXQ1_SENDSLOPECREDIT	00000000h
D60h	4	MTL_TXQ1_HICREDIT	00000000h
D64h	4	MTL_TXQ1_LOCREDIT	00000000h
D6Ch	4	MTL_Q1_INTERRUPT_CONTROL_STATUS	00000000h
D70h	4	MTL_RXQ1_OPERATION_MODE	00000000h
D74h	4	MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT	00000000h
D78h	4	MTL_RXQ1_DEBUG	00000000h
D7Ch	4	MTL_RXQ1_CONTROL	00000000h
D80h	4	MTL_TXQ2_OPERATION_MODE	00000000h
D84h	4	MTL_TXQ2_UNDERFLOW	00000000h
D88h	4	MTL_TXQ2_DEBUG	00000000h
D90h	4	MTL_TXQ2_ETS_CONTROL	00000000h
D94h	4	MTL_TXQ2_ETS_STATUS	00000000h
D98h	4	MTL_TXQ2_QUANTUM_WEIGHT	00000000h
D9Ch	4	MTL_TXQ2_SENDSLOPECREDIT	00000000h
DA0h	4	MTL_TXQ2_HICREDIT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
DA4h	4	MTL_TXQ2_LOCREDIT	00000000h
DACh	4	MTL_Q2_INTERRUPT_CONTROL_STATUS	00000000h
DB0h	4	MTL_RXQ2_OPERATION_MODE	00000000h
DB4h	4	MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT	00000000h
DB8h	4	MTL_RXQ2_DEBUG	00000000h
DBCh	4	MTL_RXQ2_CONTROL	00000000h
DC0h	4	MTL_TXQ3_OPERATION_MODE	00000000h
DC4h	4	MTL_TXQ3_UNDERFLOW	00000000h
DC8h	4	MTL_TXQ3_DEBUG	00000000h
DD0h	4	MTL_TXQ3_ETS_CONTROL	00000000h
DD4h	4	MTL_TXQ3_ETS_STATUS	00000000h
DD8h	4	MTL_TXQ3_QUANTUM_WEIGHT	00000000h
DDCh	4	MTL_TXQ3_SENDSLOPECREDIT	00000000h
DE0h	4	MTL_TXQ3_HICREDIT	00000000h
DE4h	4	MTL_TXQ3_LOCREDIT	00000000h
DECh	4	MTL_Q3_INTERRUPT_CONTROL_STATUS	00000000h
DF0h	4	MTL_RXQ3_OPERATION_MODE	00000000h
DF4h	4	MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT	00000000h
DF8h	4	MTL_RXQ3_DEBUG	00000000h
DFCh	4	MTL_RXQ3_CONTROL	00000000h
E00h	4	MTL_TXQ4_OPERATION_MODE	00000000h
E04h	4	MTL_TXQ4_UNDERFLOW	00000000h
E08h	4	MTL_TXQ4_DEBUG	00000000h
E10h	4	MTL_TXQ4_ETS_CONTROL	00000000h
E14h	4	MTL_TXQ4_ETS_STATUS	00000000h
E18h	4	MTL_TXQ4_QUANTUM_WEIGHT	00000000h
E1Ch	4	MTL_TXQ4_SENDSLOPECREDIT	00000000h
E20h	4	MTL_TXQ4_HICREDIT	00000000h
E24h	4	MTL_TXQ4_LOCREDIT	00000000h
E2Ch	4	MTL_Q4_INTERRUPT_CONTROL_STATUS	00000000h
E30h	4	MTL_RXQ4_OPERATION_MODE	00000000h
E34h	4	MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT	00000000h
E38h	4	MTL_RXQ4_DEBUG	00000000h
E3Ch	4	MTL_RXQ4_CONTROL	00000000h
E40h	4	MTL_TXQ5_OPERATION_MODE	00000000h
E44h	4	MTL_TXQ5_UNDERFLOW	00000000h
E48h	4	MTL_TXQ5_DEBUG	00000000h
E50h	4	MTL_TXQ5_ETS_CONTROL	00000000h
E54h	4	MTL_TXQ5_ETS_STATUS	00000000h
E58h	4	MTL_TXQ5_QUANTUM_WEIGHT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E5Ch	4	MTL_TXQ5_SENDSLOPECREDIT	00000000h
E60h	4	MTL_TXQ5_HICREDIT	00000000h
E64h	4	MTL_TXQ5_LOCREDIT	00000000h
E6Ch	4	MTL_Q5_INTERRUPT_CONTROL_STATUS	00000000h
E70h	4	MTL_RXQ5_OPERATION_MODE	00000000h
E74h	4	MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT	00000000h
E78h	4	MTL_RXQ5_DEBUG	00000000h
E7Ch	4	MTL_RXQ5_CONTROL	00000000h
E80h	4	MTL_TXQ6_OPERATION_MODE	00000000h
E84h	4	MTL_TXQ6_UNDERFLOW	00000000h
E88h	4	MTL_TXQ6_DEBUG	00000000h
E90h	4	MTL_TXQ6_ETS_CONTROL	00000000h
E94h	4	MTL_TXQ6_ETS_STATUS	00000000h
E98h	4	MTL_TXQ6_QUANTUM_WEIGHT	00000000h
E9Ch	4	MTL_TXQ6_SENDSLOPECREDIT	00000000h
EA0h	4	MTL_TXQ6_HICREDIT	00000000h
EA4h	4	MTL_TXQ6_LOCREDIT	00000000h
EACh	4	MTL_Q6_INTERRUPT_CONTROL_STATUS	00000000h
EB0h	4	MTL_RXQ6_OPERATION_MODE	00000000h
EB4h	4	MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT	00000000h
EB8h	4	MTL_RXQ6_DEBUG	00000000h
EBCh	4	MTL_RXQ6_CONTROL	00000000h
EC0h	4	MTL_TXQ7_OPERATION_MODE	00000000h
EC4h	4	MTL_TXQ7_UNDERFLOW	00000000h
EC8h	4	MTL_TXQ7_DEBUG	00000000h
ED0h	4	MTL_TXQ7_ETS_CONTROL	00000000h
ED4h	4	MTL_TXQ7_ETS_STATUS	00000000h
ED8h	4	MTL_TXQ7_QUANTUM_WEIGHT	00000000h
EDCh	4	MTL_TXQ7_SENDSLOPECREDIT	00000000h
EE0h	4	MTL_TXQ7_HICREDIT	00000000h
EE4h	4	MTL_TXQ7_LOCREDIT	00000000h
EECh	4	MTL_Q7_INTERRUPT_CONTROL_STATUS	00000000h
EF0h	4	MTL_RXQ7_OPERATION_MODE	00000000h
EF4h	4	MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT	00000000h
EF8h	4	MTL_RXQ7_DEBUG	00000000h
EFCh	4	MTL_RXQ7_CONTROL	00000000h
1000h	4	DMA_MODE	00000000h
1004h	4	DMA_SYSBUS_MODE	01010000h
1008h	4	DMA_INTERRUPT_STATUS	00000000h
100Ch	4	DMA_DEBUG_STATUS0	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1010h	4	DMA_DEBUG_STATUS1	00000000h
1014h	4	DMA_DEBUG_STATUS2	00000000h
1020h	4	AXI4_TX_AR_ACE_CONTROL	00000000h
1024h	4	AXI4_RX_AW_ACE_CONTROL	00000000h
1028h	4	AXI4_TXRX_AWAR_ACE_CONTROL	00000000h
1040h	4	AXI_LPI_ENTRY_INTERVAL	00000000h
1050h	4	DMA_TBS_CTRL0	00000000h
1054h	4	DMA_TBS_CTRL1	00000000h
1058h	4	DMA_TBS_CTRL2	00000000h
105Ch	4	DMA_TBS_CTRL3	00000000h
1080h	4	DMA_SAFETY_INTERRUPT_STATUS	00000000h
1084h	4	DMA_ECC_INTERRUPT_ENABLE	00000000h
1088h	4	DMA_ECC_INTERRUPT_STATUS	00000000h
1100h	4	DMA_CH0_CONTROL	00000000h
1104h	4	DMA_CH0_TX_CONTROL	00000000h
1108h	4	DMA_CH0_RX_CONTROL	00000000h
1110h	4	DMA_CH0_TXDESC_LIST_HADDRESS	00000000h
1114h	4	DMA_CH0_TXDESC_LIST_ADDRESS	00000000h
1118h	4	DMA_CH0_RXDESC_LIST_HADDRESS	00000000h
111Ch	4	DMA_CH0_RXDESC_LIST_ADDRESS	00000000h
1120h	4	DMA_CH0_TXDESC_TAIL_POINTER	00000000h
1128h	4	DMA_CH0_RXDESC_TAIL_POINTER	00000000h
112Ch	4	DMA_CH0_TXDESC_RING_LENGTH	00000000h
1130h	4	DMA_CH0_RXDESC_RING_LENGTH	00000000h
1134h	4	DMA_CH0_INTERRUPT_ENABLE	00000000h
1138h	4	DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
113Ch	4	DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1144h	4	DMA_CH0_CURRENT_APP_TXDESC	00000000h
114Ch	4	DMA_CH0_CURRENT_APP_RXDESC	00000000h
1150h	4	DMA_CH0_CURRENT_APP_TXBUFFER_H	00000000h
1154h	4	DMA_CH0_CURRENT_APP_TXBUFFER	00000000h
1158h	4	DMA_CH0_CURRENT_APP_RXBUFFER_H	00000000h
115Ch	4	DMA_CH0_CURRENT_APP_RXBUFFER	00000000h
1160h	4	DMA_CH0_STATUS	00000000h
1164h	4	DMA_CH0_MISS_FRAME_CNT	00000000h
1168h	4	DMA_CH0_RXP_ACCEPT_CNT	00000000h
116Ch	4	DMA_CH0_RX_ERI_CNT	00000000h
1180h	4	DMA_CH1_CONTROL	00000000h
1184h	4	DMA_CH1_TX_CONTROL	00000000h
1188h	4	DMA_CH1_RX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1190h	4	DMA_CH1_TXDESC_LIST_HADDRESS	00000000h
1194h	4	DMA_CH1_TXDESC_LIST_ADDRESS	00000000h
1198h	4	DMA_CH1_RXDESC_LIST_HADDRESS	00000000h
119Ch	4	DMA_CH1_RXDESC_LIST_ADDRESS	00000000h
11A0h	4	DMA_CH1_TXDESC_TAIL_POINTER	00000000h
11A8h	4	DMA_CH1_RXDESC_TAIL_POINTER	00000000h
11ACh	4	DMA_CH1_TXDESC_RING_LENGTH	00000000h
11B0h	4	DMA_CH1_RXDESC_RING_LENGTH	00000000h
11B4h	4	DMA_CH1_INTERRUPT_ENABLE	00000000h
11B8h	4	DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
11BCh	4	DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
11C4h	4	DMA_CH1_CURRENT_APP_TXDESC	00000000h
11CCh	4	DMA_CH1_CURRENT_APP_RXDESC	00000000h
11D0h	4	DMA_CH1_CURRENT_APP_TXBUFFER_H	00000000h
11D4h	4	DMA_CH1_CURRENT_APP_TXBUFFER	00000000h
11D8h	4	DMA_CH1_CURRENT_APP_RXBUFFER_H	00000000h
11DCh	4	DMA_CH1_CURRENT_APP_RXBUFFER	00000000h
11E0h	4	DMA_CH1_STATUS	00000000h
11E4h	4	DMA_CH1_MISS_FRAME_CNT	00000000h
11E8h	4	DMA_CH1_RXP_ACCEPT_CNT	00000000h
11ECh	4	DMA_CH1_RX_ERI_CNT	00000000h
1200h	4	DMA_CH2_CONTROL	00000000h
1204h	4	DMA_CH2_TX_CONTROL	00000000h
1208h	4	DMA_CH2_RX_CONTROL	00000000h
1210h	4	DMA_CH2_TXDESC_LIST_HADDRESS	00000000h
1214h	4	DMA_CH2_TXDESC_LIST_ADDRESS	00000000h
1218h	4	DMA_CH2_RXDESC_LIST_HADDRESS	00000000h
121Ch	4	DMA_CH2_RXDESC_LIST_ADDRESS	00000000h
1220h	4	DMA_CH2_TXDESC_TAIL_POINTER	00000000h
1228h	4	DMA_CH2_RXDESC_TAIL_POINTER	00000000h
122Ch	4	DMA_CH2_TXDESC_RING_LENGTH	00000000h
1230h	4	DMA_CH2_RXDESC_RING_LENGTH	00000000h
1234h	4	DMA_CH2_INTERRUPT_ENABLE	00000000h
1238h	4	DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
123Ch	4	DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1244h	4	DMA_CH2_CURRENT_APP_TXDESC	00000000h
124Ch	4	DMA_CH2_CURRENT_APP_RXDESC	00000000h
1250h	4	DMA_CH2_CURRENT_APP_TXBUFFER_H	00000000h
1254h	4	DMA_CH2_CURRENT_APP_TXBUFFER	00000000h
1258h	4	DMA_CH2_CURRENT_APP_RXBUFFER_H	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
125Ch	4	DMA_CH2_CURRENT_APP_RXBUFFER	00000000h
1260h	4	DMA_CH2_STATUS	00000000h
1264h	4	DMA_CH2_MISS_FRAME_CNT	00000000h
1268h	4	DMA_CH2_RXP_ACCEPT_CNT	00000000h
126Ch	4	DMA_CH2_RX_ERI_CNT	00000000h
1280h	4	DMA_CH3_CONTROL	00000000h
1284h	4	DMA_CH3_TX_CONTROL	00000000h
1288h	4	DMA_CH3_RX_CONTROL	00000000h
1290h	4	DMA_CH3_TXDESC_LIST_HADDRESS	00000000h
1294h	4	DMA_CH3_TXDESC_LIST_ADDRESS	00000000h
1298h	4	DMA_CH3_RXDESC_LIST_HADDRESS	00000000h
129Ch	4	DMA_CH3_RXDESC_LIST_ADDRESS	00000000h
12A0h	4	DMA_CH3_TXDESC_TAIL_POINTER	00000000h
12A8h	4	DMA_CH3_RXDESC_TAIL_POINTER	00000000h
12ACh	4	DMA_CH3_TXDESC_RING_LENGTH	00000000h
12B0h	4	DMA_CH3_RXDESC_RING_LENGTH	00000000h
12B4h	4	DMA_CH3_INTERRUPT_ENABLE	00000000h
12B8h	4	DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
12BCh	4	DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
12C4h	4	DMA_CH3_CURRENT_APP_TXDESC	00000000h
12CCh	4	DMA_CH3_CURRENT_APP_RXDESC	00000000h
12D0h	4	DMA_CH3_CURRENT_APP_TXBUFFER_H	00000000h
12D4h	4	DMA_CH3_CURRENT_APP_TXBUFFER	00000000h
12D8h	4	DMA_CH3_CURRENT_APP_RXBUFFER_H	00000000h
12DCh	4	DMA_CH3_CURRENT_APP_RXBUFFER	00000000h
12E0h	4	DMA_CH3_STATUS	00000000h
12E4h	4	DMA_CH3_MISS_FRAME_CNT	00000000h
12E8h	4	DMA_CH3_RXP_ACCEPT_CNT	00000000h
12ECh	4	DMA_CH3_RX_ERI_CNT	00000000h
1300h	4	DMA_CH4_CONTROL	00000000h
1304h	4	DMA_CH4_TX_CONTROL	00000000h
1308h	4	DMA_CH4_RX_CONTROL	00000000h
1310h	4	DMA_CH4_TXDESC_LIST_HADDRESS	00000000h
1314h	4	DMA_CH4_TXDESC_LIST_ADDRESS	00000000h
1318h	4	DMA_CH4_RXDESC_LIST_HADDRESS	00000000h
131Ch	4	DMA_CH4_RXDESC_LIST_ADDRESS	00000000h
1320h	4	DMA_CH4_TXDESC_TAIL_POINTER	00000000h
1328h	4	DMA_CH4_RXDESC_TAIL_POINTER	00000000h
132Ch	4	DMA_CH4_TXDESC_RING_LENGTH	00000000h
1330h	4	DMA_CH4_RXDESC_RING_LENGTH	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1334h	4	DMA_CH4_INTERRUPT_ENABLE	00000000h
1338h	4	DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
133Ch	4	DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1344h	4	DMA_CH4_CURRENT_APP_TXDESC	00000000h
134Ch	4	DMA_CH4_CURRENT_APP_RXDESC	00000000h
1350h	4	DMA_CH4_CURRENT_APP_TXBUFFER_H	00000000h
1354h	4	DMA_CH4_CURRENT_APP_TXBUFFER	00000000h
1358h	4	DMA_CH4_CURRENT_APP_RXBUFFER_H	00000000h
135Ch	4	DMA_CH4_CURRENT_APP_RXBUFFER	00000000h
1360h	4	DMA_CH4_STATUS	00000000h
1364h	4	DMA_CH4_MISS_FRAME_CNT	00000000h
1368h	4	DMA_CH4_RXP_ACCEPT_CNT	00000000h
136Ch	4	DMA_CH4_RX_ERI_CNT	00000000h
1380h	4	DMA_CH5_CONTROL	00000000h
1384h	4	DMA_CH5_TX_CONTROL	00000000h
1388h	4	DMA_CH5_RX_CONTROL	00000000h
1390h	4	DMA_CH5_TXDESC_LIST_HADDRESS	00000000h
1394h	4	DMA_CH5_TXDESC_LIST_ADDRESS	00000000h
1398h	4	DMA_CH5_RXDESC_LIST_HADDRESS	00000000h
139Ch	4	DMA_CH5_RXDESC_LIST_ADDRESS	00000000h
13A0h	4	DMA_CH5_TXDESC_TAIL_POINTER	00000000h
13A8h	4	DMA_CH5_RXDESC_TAIL_POINTER	00000000h
13ACh	4	DMA_CH5_TXDESC_RING_LENGTH	00000000h
13B0h	4	DMA_CH5_RXDESC_RING_LENGTH	00000000h
13B4h	4	DMA_CH5_INTERRUPT_ENABLE	00000000h
13B8h	4	DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
13BCh	4	DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
13C4h	4	DMA_CH5_CURRENT_APP_TXDESC	00000000h
13CCh	4	DMA_CH5_CURRENT_APP_RXDESC	00000000h
13D0h	4	DMA_CH5_CURRENT_APP_TXBUFFER_H	00000000h
13D4h	4	DMA_CH5_CURRENT_APP_TXBUFFER	00000000h
13D8h	4	DMA_CH5_CURRENT_APP_RXBUFFER_H	00000000h
13DCh	4	DMA_CH5_CURRENT_APP_RXBUFFER	00000000h
13E0h	4	DMA_CH5_STATUS	00000000h
13E4h	4	DMA_CH5_MISS_FRAME_CNT	00000000h
13E8h	4	DMA_CH5_RXP_ACCEPT_CNT	00000000h
13ECh	4	DMA_CH5_RX_ERI_CNT	00000000h
1400h	4	DMA_CH6_CONTROL	00000000h
1404h	4	DMA_CH6_TX_CONTROL	00000000h
1408h	4	DMA_CH6_RX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1410h	4	DMA_CH6_TXDESC_LIST_HADDRESS	00000000h
1414h	4	DMA_CH6_TXDESC_LIST_ADDRESS	00000000h
1418h	4	DMA_CH6_RXDESC_LIST_HADDRESS	00000000h
141Ch	4	DMA_CH6_RXDESC_LIST_ADDRESS	00000000h
1420h	4	DMA_CH6_TXDESC_TAIL_POINTER	00000000h
1428h	4	DMA_CH6_RXDESC_TAIL_POINTER	00000000h
142Ch	4	DMA_CH6_TXDESC_RING_LENGTH	00000000h
1430h	4	DMA_CH6_RXDESC_RING_LENGTH	00000000h
1434h	4	DMA_CH6_INTERRUPT_ENABLE	00000000h
1438h	4	DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
143Ch	4	DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
1444h	4	DMA_CH6_CURRENT_APP_TXDESC	00000000h
144Ch	4	DMA_CH6_CURRENT_APP_RXDESC	00000000h
1450h	4	DMA_CH6_CURRENT_APP_TXBUFFER_H	00000000h
1454h	4	DMA_CH6_CURRENT_APP_TXBUFFER	00000000h
1458h	4	DMA_CH6_CURRENT_APP_RXBUFFER_H	00000000h
145Ch	4	DMA_CH6_CURRENT_APP_RXBUFFER	00000000h
1460h	4	DMA_CH6_STATUS	00000000h
1464h	4	DMA_CH6_MISS_FRAME_CNT	00000000h
1468h	4	DMA_CH6_RXP_ACCEPT_CNT	00000000h
146Ch	4	DMA_CH6_RX_ERI_CNT	00000000h
1480h	4	DMA_CH7_CONTROL	00000000h
1484h	4	DMA_CH7_TX_CONTROL	00000000h
1488h	4	DMA_CH7_RX_CONTROL	00000000h
1490h	4	DMA_CH7_TXDESC_LIST_HADDRESS	00000000h
1494h	4	DMA_CH7_TXDESC_LIST_ADDRESS	00000000h
1498h	4	DMA_CH7_RXDESC_LIST_HADDRESS	00000000h
149Ch	4	DMA_CH7_RXDESC_LIST_ADDRESS	00000000h
14A0h	4	DMA_CH7_TXDESC_TAIL_POINTER	00000000h
14A8h	4	DMA_CH7_RXDESC_TAIL_POINTER	00000000h
14ACh	4	DMA_CH7_TXDESC_RING_LENGTH	00000000h
14B0h	4	DMA_CH7_RXDESC_RING_LENGTH	00000000h
14B4h	4	DMA_CH7_INTERRUPT_ENABLE	00000000h
14B8h	4	DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
14BCh	4	DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
14C4h	4	DMA_CH7_CURRENT_APP_TXDESC	00000000h
14CCh	4	DMA_CH7_CURRENT_APP_RXDESC	00000000h
14D0h	4	DMA_CH7_CURRENT_APP_TXBUFFER_H	00000000h
14D4h	4	DMA_CH7_CURRENT_APP_TXBUFFER	00000000h
14D8h	4	DMA_CH7_CURRENT_APP_RXBUFFER_H	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
14DCh	4	DMA_CH7_CURRENT_APP_RXBUFFER	00000000h
14E0h	4	DMA_CH7_STATUS	00000000h
14E4h	4	DMA_CH7_MISS_FRAME_CNT	00000000h
14E8h	4	DMA_CH7_RXP_ACCEPT_CNT	00000000h
14ECh	4	DMA_CH7_RX_ERI_CNT	00000000h

3.2.1 MAC_CONFIGURATION — Offset 0h

The MAC Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ARP Offload Enable (ARPEN):** When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. 0x0 (DISABLE): ARP Offload is disabled. 0x1 (ENABLE): ARP Offload is enabled.
30:28	0h RW	**Source Address Insertion or Replacement Control (SARC):** This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: - The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: - Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field. 0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field. 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field. 0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field.
27	0h RW	**Checksum Offload (IPC):** When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. 0x0 (DISABLE): IP header/payload checksum checking is disabled. 0x1 (ENABLE): IP header/payload checksum checking is enabled.

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Inter-Packet Gap (IPG):** These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. 0x0 (IPG96): 96 bit times IPG. 0x1 (IPG88): 88 bit times IPG. 0x2 (IPG80): 80 bit times IPG. 0x3 (IPG72): 72 bit times IPG. 0x4 (IPG64): 64 bit times IPG. 0x5 (IPG56): 56 bit times IPG. 0x6 (IPG48): 48 bit times IPG. 0x7 (IPG40): 40 bit times IPG.
23	0h RW	**Giant Packet Size Limit Control Enable (GPSLCE):** When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. 0x0 (DISABLE): Giant Packet Size Limit Control is disabled. 0x1 (ENABLE): Giant Packet Size Limit Control is enabled.
22	0h RW	**IEEE 802.3as Support for 2K Packets (S2KP):** When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. 0x0 (DISABLE): Support upto 2K packet is disabled. 0x1 (ENABLE): Support upto 2K packet is Enabled.
21	0h RW	**CRC stripping for Type packets (CST):** When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. 0x0 (DISABLE): CRC stripping for Type packets is disabled. 0x1 (ENABLE): CRC stripping for Type packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Automatic Pad or CRC Stripping (ACS):** When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. 0x0 (DISABLE): Automatic Pad or CRC Stripping is disabled. 0x1 (ENABLE): Automatic Pad or CRC Stripping is enabled.
19	0h RW	**Watchdog Disable (WD):** When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. 0x0 (ENABLE): Watchdog is enabled. 0x1 (DISABLE): Watchdog is disabled.
18	0h RW	**Packet Burst Enable (BE):** When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0x0 (DISABLE): Packet Burst is disabled. 0x1 (ENABLE): Packet Burst is enabled.
17	0h RW	**Jabber Disable (JD):** When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. 0x0 (ENABLE): Jabber is enabled. 0x1 (DISABLE): Jabber is disabled.
16	0h RW	**Jumbo Packet Enable (JE):** When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0x0 (DISABLE): Jumbo packet is disabled. 0x1 (ENABLE): Jumbo packet is enabled.
15	0h RW	**Port Select (PS):** This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). 0x0 (M_1000_2500M): For 1000 or 2500 Mbps operations. 0x1 (M_10_100M): For 10 or 100 Mbps operations.
14	0h RW	**FES:** This bit selects the speed mode. 0x0 (M_10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0. 0x1 (M_100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0.
13	0h RW	**Duplex Mode (DM):** When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Loopback Mode (LM):** When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. 0x0 (DISABLE): Loopback is disabled. 0x1 (ENABLE): Loopback is enabled.
11	0h RW	**Enable Carrier Sense Before Transmission in Full-Duplex Mode (ECRSFD):** When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal. 0x0 (DISABLE): ECRSFD is disabled. 0x1 (ENABLE): ECRSFD is enabled.
10	0h RW	**Disable Receive Own (DO):** When this bit is set, the MAC disables the reception of packets when the GMII signal TX_EN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode. 0x0 (ENABLE): Enable Receive Own. 0x1 (DISABLE): Disable Receive Own.
9	0h RW	**Disable Carrier Sense During Transmission (DCRS):** When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. 0x0 (ENABLE): Enable Carrier Sense During Transmission. 0x1 (DISABLE): Disable Carrier Sense During Transmission.
8	0h RW	**Disable Retry (DR):** When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. 0x0 (ENABLE): Enable Retry. 0x1 (DISABLE): Disable Retry.
7	0h RO	**Reserved**
6:5	0h RW	**Back-Off Limit (BL):** The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. 0x0 (MIN_N_10): k = min(n,10). 0x1 (MIN_N_8): k = min(n,8). 0x2 (MIN_N_4): k = min(n,4). 0x3 (MIN_N_1): k = min(n,1).

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Deferral Check (DC):** When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. 0x0 (DISABLE): Deferral check function is disabled. 0x1 (ENABLE): Deferral check function is enabled.
3:2	0h RW	**Preamble Length for Transmit packets (PRELEN):** These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 0x0 (M_7BYTES): 7 bytes of preamble. 0x1 (M_5BYTES): 5 bytes of preamble. 0x2 (M_3BYTES): 3 bytes of preamble. 0x3 (RESERVED): Reserved.
1	0h RW	**Transmitter Enable (TE):** When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. 0x0 (DISABLE): Transmitter is disabled. 0x1 (ENABLE): Transmitter is enabled.
0	0h RW	**Receiver Enable (RE):** When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. 0x0 (DISABLE): Receiver is disabled. 0x1 (ENABLE): Receiver is enabled.

3.2.2 MAC_EXT_CONFIGURATION — Offset 4h

The MAC Extended Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**ARP Packet Drop if IP Mismatch (APDIM):** When set, Packet for which Target Protocol Address does not match IPv4 address is dropped in the MTL layer. When reset, when target Protocol Address does not match, packet is forwarded to MTL maintaining backward compatibility. 0x0 (DISABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address disabled. 0x1 (ENABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address enabled.
29:25	00h RW	**Extended Inter-Packet Gap (EIPG):** The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	0h RW	**Extended Inter-Packet Gap Enable (EIPGEN):** When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. 0x0 (DISABLE): Extended Inter-Packet Gap is disabled. 0x1 (ENABLE): Extended Inter-Packet Gap is enabled.
23	0h RO	**Reserved**
22:20	0h RW	**Maximum Size for Splitting the Header Data (HDSMS):** These bits indicate the maximum header size allowed for splitting the header data in the received packet. 0x0 (M_64BYTES): Maximum Size for Splitting the Header Data is 64 bytes. 0x1 (M_128BYTES): Maximum Size for Splitting the Header Data is 128 bytes. 0x2 (M_256BYTES): Maximum Size for Splitting the Header Data is 256 bytes. 0x3 (M_512BYTES): Maximum Size for Splitting the Header Data is 512 bytes. 0x4 (M_1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes. 0x5 (RSVD): Reserved.
19	0h RW	**Packet Duplication Control (PDC):** When this bit is set, the received packet with Multicast/Broadcast Destination address is routed to multiple Receive DMA Channels. The Receive DMA Channels is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Multicast/Broadcast Destination address in the received packet. The DCS field is interpreted to be a one-hot value, each bit corresponding to the Receive DMA Channel. When this bit is reset, the received packet is routed to single Receive DMA Channel. The Receive DMA Channel is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Destination address in the received packet. The DCS field is interpreted as a binary value. 0x0 (DISABLE): Packet Duplication Control is disabled. 0x1 (ENABLE): Packet Duplication Control is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Unicast Slow Protocol Packet Detect (USP):** When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. 0x0 (DISABLE): Unicast Slow Protocol Packet Detection is disabled. 0x1 (ENABLE): Unicast Slow Protocol Packet Detection is enabled.
17	0h RW	**Slow Protocol Detection Enable (SPEN):** When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. 0x0 (DISABLE): Slow Protocol Detection is disabled. 0x1 (ENABLE): Slow Protocol Detection is enabled.
16	0h RW	**Disable CRC Checking for Received Packets (DCRCC):** When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. 0x0 (ENABLE): CRC Checking is enabled. 0x1 (DISABLE): CRC Checking is disabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Giant Packet Size Limit (GPSL):** If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

3.2.3 MAC_PACKET_FILTER — Offset 8h

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Receive All (RA):** When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled. 0x1 (ENABLE): Receive All is enabled.
30:22	0h RO	**Reserved**
21	0h RW	**Drop Non-TCP/UDP over IP Packets (DNTU):** When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0 (FWD): Forward Non-TCP/UDP over IP Packets. 0x1 (DROP): Drop Non-TCP/UDP over IP Packets.
20	0h RW	**Layer 3 and Layer 4 Filter Enable (IPFE):** When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled. 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled.
19:17	0h RO	**Reserved**
16	0h RW	**VLAN Tag Filter Enable (VTFE):** When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. 0x0 (DISABLE): VLAN Tag Filter is disabled. 0x1 (ENABLE): VLAN Tag Filter is enabled.
15:11	0h RO	**Reserved**
10	0h RW	**Hash or Perfect Filter (HPF):** When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. 0x0 (DISABLE): Hash or Perfect Filter is disabled. 0x1 (ENABLE): Hash or Perfect Filter is enabled.
9	0h RW	**Source Address Filter Enable (SAF):** When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in GbE Controller, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA. 0x0 (DISABLE): SA Filtering is disabled. 0x1 (ENABLE): SA Filtering is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SA Inverse Filtering (SAIF):** When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0 (DISABLE): SA Inverse Filtering is disabled. 0x1 (ENABLE): SA Inverse Filtering is enabled.
7:6	0h RW	**Pass Control Packets (PCF):** These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0x0 (FLTR_ALL): MAC filters all control packets from reaching the application. 0x1 (FW_XCPT_PAU): MAC forwards all control packets except Pause packets to the application even if they fail the Address filter. 0x2 (FW_ALL): MAC forwards all control packets to the application even if they fail the Address filter. 0x3 (FW_PASS): MAC forwards the control packets that pass the Address filter.
5	0h RW	**Disable Broadcast Packets (DBF):** When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. 0x0 (ENABLE): Enable Broadcast Packets. 0x1 (DISABLE): Disable Broadcast Packets.
4	0h RW	**Pass All Multicast (PM):** When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. 0x0 (DISABLE): Pass All Multicast is disabled. 0x1 (ENABLE): Pass All Multicast is enabled.
3	0h RW	**DA Inverse Filtering (DAIF):** When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. 0x0 (DISABLE): DA Inverse Filtering is disabled. 0x1 (ENABLE): DA Inverse Filtering is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Hash Multicast (HMC):** When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Multicast is disabled. 0x1 (ENABLE): Hash Multicast is enabled.
1	0h RW	**Hash Unicast (HUC):** When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Unicast is disabled. 0x1 (ENABLE): Hash Unicast is enabled.
0	0h RW	**Promiscuous Mode (PR):** When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. 0x0 (DISABLE): Promiscuous Mode is disabled. 0x1 (ENABLE): Promiscuous Mode is enabled.

3.2.4 MAC_WATCHDOG_TIMEOUT — Offset Ch

The Watchdog Timeout register controls the watchdog timeout for received packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Programmable Watchdog Enable (PWE):** When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. 0x0 (DISABLE): Programmable Watchdog is disabled. 0x1 (ENABLE): Programmable Watchdog is enabled.
7:4	0h RO	**Reserved**
3:0	0h RW	**Watchdog Timeout (WTO):** When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. 0x0 (M_2KBYTES): 2 KB. 0x1 (M_3KBYTES): 3 KB. 0x2 (M_4KBYTES): 4 KB. 0x3 (M_5KBYTES): 5 KB. 0x4 (M_6KBYTES): 6 KB. 0x5 (M_7KBYTES): 7 KB. 0x6 (M_8KBYTES): 8 KB. 0x7 (M_9KBYTES): 9 KB. 0x08 (M_10KBYTES): 10 KB. 0x09 (M_11KBYTES): 11 KB. 0x0A (M_12KBYTES): 12 KB. 0x0B (M_13KBYTES): 13 KB. 0x0C (M_14KBYTES): 14 KB. 0x0D (M_15KBYTES): 15 KB. 0x0E (M_16383BYTES): 16383 Bytes. 0x0F (RESERVED): Reserved.

3.2.5 MAC_HASH_TABLE_REG0 — Offset 10h

The Hash Table Register 0 contains the first 32 bits of the hash table, when the width of the hash table is 128 or 256 bits. This design has set the Hash Table Size (width of the hash table) to 64.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).

- Perform bitwise reversal for the value obtained in Step 1.

- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table First 32 Bits (HT31T0):** This field contains the first 32 Bits [31:0] of the Hash table.

3.2.6 MAC_HASH_TABLE_REG1 — Offset 14h

The Hash Table Register 1 contains the second 32 bits of the hash table.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).

- Perform bitwise reversal for the value obtained in Step 1.

- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table Second 32 Bits (HT63T32):** This field contains the second 32 Bits [63:32] of the Hash table.

3.2.7 MAC_VLAN_TAG_CTRL — Offset 50h

This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Inner VLAN Tag in Rx Status (EIVLRXS):** When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled. 0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled.
30	0h RO	**Reserved**
29:28	0h RW	**Enable Inner VLAN Tag Stripping on Receive (EIVLS):** This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
27	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** When this bit, VTHM bit and the EDVLP field are set, the MAC receiver enables VLAN Hash filtering operation on the inner VLAN Tag (if present). When this bit is reset and VTHM bit is set, the MAC receiver enables VLAN Hash filtering operation on the outer VLAN Tag (if present). The ERSVLM bit and DOVLTC bit determines which VLAN type is enabled for filtering. 0x0 (DISABLE): Inner VLAN tag is disabled. 0x1 (ENABLE): Inner VLAN tag is enabled.
26	0h RW	**Enable Double VLAN Processing (EDVLP):** When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0 (DISABLE): Double VLAN Processing is disabled. 0x1 (ENABLE): Double VLAN Processing is enabled.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**VLAN Tag Hash Table Match Enable (VTHM):** When this bit is set, the most significant four bits of CRC of VLAN Tag are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled. 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled.
24	0h RW	**Enable VLAN Tag in Rx status (EVLRXS):** When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. 0x0 (DISABLE): VLAN Tag in Rx status is disabled. 0x1 (ENABLE): VLAN Tag in Rx status is enabled.
23	0h RO	**Reserved**
22:21	0h RW	**Enable VLAN Tag Stripping on Receive (EVLS):** This field indicates the stripping operation on the outer VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
20	0h RW	**Disable VLAN Type Check for VLAN Hash Filtering (DOVLTC):** When this bit is set, the MAC VLAN Hash Filter does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC VLAN Hash Filter filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. 0x0 (ENABLE): VLAN Type Check is enabled. 0x1 (DISABLE): VLAN Type Check is disabled.
19	0h RW	**Enable Receive S-VLAN Match for VLAN Hash Filtering (ERSVLM):** When this bit is set, the MAC receiver enables VLAN Hash filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables VLAN Hash filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for VLAN Hash filtering or matching. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	**Enable S-VLAN (ESVL):** When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. 0x0 (DISABLE): S-VLAN is disabled. 0x1 (ENABLE): S-VLAN is enabled.
17	0h RW	**VLAN Tag Inverse Match Enable (VTIM):** When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. 0x0 (DISABLE): VLAN Tag Inverse Match is disabled. 0x1 (ENABLE): VLAN Tag Inverse Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Enable 12-Bit VLAN Tag Comparison for VLAN Hash Filtering (ETV):** When this bit is set, a 12-bit VLAN identifier is used for VLAN Hash filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag in the received VLAN-tagged packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for VLAN hash filtering. 0x0 (DISABLE): 12-Bit VLAN Tag Comparison is disabled. 0x1 (ENABLE): 12-Bit VLAN Tag Comparison is enabled.
15:5	0h RO	**Reserved**
4:2	0h RW	**OFS:** This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	0h RW	**Command Type (CT):** This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation. 0x0 (WRITE): Write operation. 0x1 (READ): Read operation.
0	0h RW	**Operation Busy (OB):** This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset. 0x0 (DISABLE): Operation Busy is disabled. 0x1 (ENABLE): Operation Busy is enabled.

3.2.8 MAC_VLAN_TAG_DATA — Offset 54h

This register holds the read/write data for Indirect Access of the Per VLAN Tag registers. During the read access, this field contains valid read data only after the OB bit is reset.

During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:25	0h RW	**DMA Channel Number (DMACHN):** The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	0h RW	**DMA Channel Number Enable (DMACHEN):** This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing. 0x0 (DISABLE): DMA Channel Number is disabled. 0x1 (ENABLE): DMA Channel Number is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** This bit is valid only when Double VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). 0x0 (DISABLE): Inner VLAN tag comparison is disabled. 0x1 (ENABLE): Inner VLAN tag comparison is enabled.
19	0h RW	**Enable S-VLAN Match for received Frames (ERSVLM):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	**Disable VLAN Type Comparison (DOVLTC):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit. 0x0 (ENABLE): VLAN type comparison is enabled. 0x1 (DISABLE): VLAN type comparison is disabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**12bits or 16bits VLAN comparison (ETV):** This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. 0x0 (M_16BIT): 16 bit VLAN comparison. 0x1 (M_12BIT): 12 bit VLAN comparison.
16	0h RW	**VLAN Tag Enable (VEN):** This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields. 0x0 (DISABLE): VLAN Tag is disabled. 0x1 (ENABLE): VLAN Tag is enabled.
15:0	0000h RW	**VLAN Tag ID (VID):** This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

3.2.9 MAC_VLAN_HASH_TABLE — Offset 58h

When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. The upper four bits of the calculated hash value are used to index the contents of the VLAN Hash table. For example, hash value of 4b'1000 selects Bit 8 of the VLAN Hash table.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3).

- Perform bitwise reversal for the value obtained in step 1.

- Take the upper four bits from the value obtained in step 2.

If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] of this register are written.

- If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**VLAN Hash Table (VLHT):** This field contains the 16-bit VLAN Hash Table.

3.2.10 MAC_VLAN_INCL — Offset 60h

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BUSY:** This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register. 0x0 (INACTIVE): Busy status not detected. 0x1 (ACTIVE): Busy status detected.
30	0h RW	**Read write control (RDWR):** This bit controls the read or write operation for indirectly accessing the queue/ channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset. 0x0 (READ): Read operation of indirect access. 0x1 (WRITE): Write operation of indirect access.
29:27	0h RO	**Reserved**
26:24	0h RW	**ADDR:** This field selects one of the queue/channel specific VLAN Inclusion register for read/ write access. This does not have any effect when CBTI is reset.
23:22	0h RO	**Reserved**
21	0h RW	**Channel based tag insertion (CBTI):** When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register. 0x0 (DISABLE): Channel based tag insertion is disabled. 0x1 (ENABLE): Channel based tag insertion is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted in the 13th and 14th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

3.2.11 MAC_INNER_VLAN_INCL — Offset 64h

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 17th and 18th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 17th and 18th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

3.2.12 MAC_Q0_TX_FLOW_CTRL — Offset 70h

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The Busy bit remains set until the control packet is transferred onto the cable. The application must make sure that the Busy bit is cleared before writing to the register.

When the PFCE bit in the MAC_Rx_Flow_Ctrl register is enabled, this register controls the generation of Priority Flow Control (PFC) frames with priorities mapped according to PSRQ0 in the MAC_RxQ_Ctrl2 register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy or Backpressure Activate (FCB_BPA):** This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.13 MAC_Q1_TX_FLOW_CTRL — Offset 74h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.14 MAC_Q2_TX_FLOW_CTRL — Offset 78h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.15 MAC_Q3_TX_FLOW_CTRL — Offset 7Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.16 MAC_Q4_TX_FLOW_CTRL — Offset 80h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.17 MAC_Q5_TX_FLOW_CTRL — Offset 84h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.18 MAC_Q6_TX_FLOW_CTRL — Offset 88h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.19 MAC_Q7_TX_FLOW_CTRL — Offset 8Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

3.2.20 MAC_RX_FLOW_CTRL — Offset 90h

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Priority Based Flow Control Enable (PFCE):** When this bit is set, it enables generation and reception of priority-based flow control (PFC) packets. When this bit is reset, it enables generation and reception of 802.3x Pause control packets. 0x0 (DISABLE): Priority Based Flow Control is disabled. 0x1 (ENABLE): Priority Based Flow Control is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**Unicast Pause Packet Detect (UP):** A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. 0x0 (DISABLE): Unicast Pause Packet Detect disabled. 0x1 (ENABLE): Unicast Pause Packet Detect enabled.
0	0h RW	**Receive Flow Control Enable (RFE):** When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. 0x0 (DISABLE): Receive Flow Control is disabled. 0x1 (ENABLE): Receive Flow Control is enabled.

3.2.21 MAC_RXQ_CTRL4 — Offset 94h

The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW	**VLAN Tag Filter Fail Packets Queue (VFFQ):** This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	0h RW	**VLAN Tag Filter Fail Packets Queuing Enable (VFFQE):** When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled.
15:12	0h RO	**Reserved**
11:9	0h RW	**Multicast Address Filter Fail Packets Queue. (MFFQ):** This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
8	0h RW	**Multicast Address Filter Fail Packets Queuing Enable. (MFFQE):** When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled.
7:4	0h RO	**Reserved**
3:1	0h RW	**Unicast Address Filter Fail Packets Queue. (UFFQ):** This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	0h RW	**Unicast Address Filter Fail Packets Queuing Enable. (UFFQE):** When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled.

3.2.22 MAC_TXQ_PRTY_MAP0 — Offset 98h

The Transmit Queue Priority Mapping 0 register contains the priority values assigned to Tx Queue 0 through Tx Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 3 (PSTQ3):** This bit is similar to the PSTQ0 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 2 (PSTQ2):** This bit is similar to the PSTQ0 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 1 (PSTQ1):** This bit is similar to the PSTQ0 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 0 (PSTQ0):** This field holds the priorities assigned to Tx Queue 0 by the software. This field determines if Tx Queue 0 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

3.2.23 MAC_TXQ_PRTY_MAP1 — Offset 9Ch

The Transmit Queue Priority Mapping 1 register contains the priority values assigned to Tx Queue 4 through Tx Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 7 (PSTQ7):** This bit is similar to the PSTQ4 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 6 (PSTQ6):** This bit is similar to the PSTQ4 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 5 (PSTQ5):** This bit is similar to the PSTQ4 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 4 (PSTQ4):** This field holds the priorities assigned to Tx Queue 4 by the software. This field determines if Tx Queue 4 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

3.2.24 MAC_RXQ_CTRL0 — Offset A0h

The Receive Queue Control 0 register controls the queue management in the MAC Receiver.

Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:14	0h RW	**Receive Queue 7 Enable (RXQ7EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
13:12	0h RW	**Receive Queue 6 Enable (RXQ6EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
11:10	0h RW	**Receive Queue 5 Enable (RXQ5EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
9:8	0h RW	**Receive Queue 4 Enable (RXQ4EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
7:6	0h RW	**Receive Queue 3 Enable (RXQ3EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Receive Queue 2 Enable (RXQ2EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
3:2	0h RW	**Receive Queue 1 Enable (RXQ1EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
1:0	0h RW	**Receive Queue 0 Enable (RXQ0EN):** This field indicates whether Rx Queue 0 is enabled for AV or DCB. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

3.2.25 MAC_RXQ_CTRL1 — Offset A4h

The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**OMCBCQ:** 0x0 (DISABLE): overriding MCBCQ priority disabled. 0x1 (ENABLE): overriding MCBCQ priority enabled.
27	0h RO	**Reserved**
26:24	0h RW	**Frame Preemption Residue Queue (FPRQ):** This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RW	**Tagged PTP over Ethernet Packets Queuing Control. (TPQC):** This field controls the routing of the VLAN Tagged PTPoE packets. The following programmable options are allowed. - 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). - 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). - 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. - 2'b11: Reserved
21	0h RW	**Tagged AV Control Packets Queuing Enable. (TACPQE):** When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers. 0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled. 0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled.
20	0h RW	**Multicast and Broadcast Queue Enable (MCBCQEN):** This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. 0x0 (DISABLE): Multicast and Broadcast Queue is disabled. 0x1 (ENABLE): Multicast and Broadcast Queue is enabled.
19	0h RO	**Reserved**
18:16	0h RW	**Multicast and Broadcast Queue (MCBCQ):** This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
15	0h RO	**Reserved**
14:12	0h RW	**Untagged Packet Queue (UPQ):** This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**DCB Control Packets Queue (DCBCPQ):** This field specifies the Rx queue on which the received DCB control packets are routed. The DCB data packets are routed based on the PSRQ field of the Transmit Flow Control Register of corresponding queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
7	0h RO	**Reserved**
6:4	0h RW	**PTP Packets Queue (PTPQ):** This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
3	0h RO	**Reserved**
2:0	0h RW	**AV Untagged Control Packets Queue (AVCPQ):** This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.

3.2.26 MAC_RXQ_CTRL2 — Offset A8h

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 3 (PSRQ3):** This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 3 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 2 (PSRQ2):** This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 2 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 1 (PSRQ1):** This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 0 (PSRQ0):** This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.

3.2.27 MAC_RXQ_CTRL3 — Offset ACh

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 4 to 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 7 (PSRQ7):** This field decides the priorities assigned to Rx Queue 7. All packets with priorities that match the values set in this field are routed to Rx Queue 7. For example, if PSRQ7[7, 4] are set, packets with USP field equal to 7 or 4 are routed to Rx Queue 7. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 7 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 6 (PSRQ6):** This field decides the priorities assigned to Rx Queue 6. All packets with priorities that match the values set in this field are routed to Rx Queue 6. For example, if PSRQ6[5] are set, packets with USP field equal to 5 are routed to Rx Queue 6. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 6 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 5 (PSRQ5):** This field decides the priorities assigned to Rx Queue 5. All packets with priorities that match the values set in this field are routed to Rx Queue 5. For example, if PSRQ5[6] is set, packets with USP field equal to 6 are routed to Rx Queue 5. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 5 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 4 (PSRQ4):** This field decides the priorities assigned to Rx Queue 4. All packets with priorities that match the values set in this field are routed to Rx Queue 4. For example, if PSRQ4[7:4] is set, packets with USP field equal to 7, 6, 5, or 4 are routed to Rx Queue 4. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 4 crosses the flow control threshold settings.

3.2.28 MAC_INTERRUPT_STATUS — Offset B0h

The Interrupt Status register contains the status of interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**MMC FPE Receive Interrupt Status (MFRIS):** This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active. 0x1 (ACTIVE): MMC FPE Receive Interrupt status active.
19	0h RO	**MMC FPE Transmit Interrupt Status (MFTIS):** This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active. 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active.
18	0h RO	**MDIO Interrupt Status (MDIOIS):** This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): MDIO Interrupt status not active. 0x1 (ACTIVE): MDIO Interrupt status active.
17	0h RO	**Frame Preemption Interrupt Status (FPEIS):** This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt. 0x0 (INACTIVE): Frame Preemption Interrupt status not active. 0x1 (ACTIVE): Frame Preemption Interrupt status active.
16	0h RO	**Reserved**
15	0h RO	**GPI Interrupt Status (GPIIS):** When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field of the MAC_GPIO_Status register and the corresponding GPIE bit is enabled in the MAC_GPIO_Control register. This bit is cleared on reading lane 0 (GPIS) of the MAC_GPIO_Status register. 0x0 (INACTIVE): GPI Interrupt status not active. 0x1 (ACTIVE): GPI Interrupt status active.
14	0h RO	**Receive Status Interrupt (RXSTSIS):** This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Receive Interrupt status not active. 0x1 (ACTIVE): Receive Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Transmit Status Interrupt (TXSTSIS):** This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Transmit Interrupt status not active. 0x1 (ACTIVE): Transmit Interrupt status active.
12	0h RO	**Timestamp Interrupt Status (TSIS):** If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: - The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. - There is an overflow in the Seconds register. - The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. 0x0 (INACTIVE): Timestamp Interrupt status not active. 0x1 (ACTIVE): Timestamp Interrupt status active.
11	0h RO	**MMC Receive Checksum Offload Interrupt Status (MMCRXIPIS):** This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. 0x0 (INACTIVE): MMC Receive Checksum Offload Interrupt status not active. 0x1 (ACTIVE): MMC Receive Checksum Offload Interrupt status active.
10	0h RO	**MMC Transmit Interrupt Status (MMCTXIS):** This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Transmit Interrupt status not active. 0x1 (ACTIVE): MMC Transmit Interrupt status active.
9	0h RO	**MMC Receive Interrupt Status (MMCRXIS):** This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Receive Interrupt status not active. 0x1 (ACTIVE): MMC Receive Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MMC Interrupt Status (MMCIS):** This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Interrupt status not active. 0x1 (ACTIVE): MMC Interrupt status active.
7:6	0h RO	**Reserved**
5	0h RO	**LPI Interrupt Status (LPIIS):** When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): LPI Interrupt status not active. 0x1 (ACTIVE): LPI Interrupt status active.
4	0h RO	**PMT Interrupt Status (PMTIS):** This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. 0x0 (INACTIVE): PMT Interrupt status not active. 0x1 (ACTIVE): PMT Interrupt status active.
3	0h RO	**PHY Interrupt (PHYIS):** This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): PHY Interrupt not detected. 0x1 (ACTIVE): PHY Interrupt detected.
2:1	0h RO	**Reserved**
0	0h RO	**RGMII or SMII Interrupt Status (RGSMIIIS):** This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active. 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active.

3.2.29 MAC_INTERRUPT_ENABLE — Offset B4h

The Interrupt Enable register contains the masks for generating the interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**MDIO Interrupt Enable (MDIOIE):** When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): MDIO Interrupt is disabled. 0x1 (ENABLE): MDIO Interrupt is enabled.
17	0h RW	**Frame Preemption Interrupt Enable (FPEIE):** When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): Frame Preemption Interrupt is disabled. 0x1 (ENABLE): Frame Preemption Interrupt is enabled.
16:15	0h RO	**Reserved**
14	0h RW	**Receive Status Interrupt Enable (RXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Receive Status Interrupt is disabled. 0x1 (ENABLE): Receive Status Interrupt is enabled.
13	0h RW	**Transmit Status Interrupt Enable (TXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Status Interrupt is disabled. 0x1 (ENABLE): Timestamp Status Interrupt is enabled.
12	0h RW	**Timestamp Interrupt Enable (TSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Interrupt is disabled. 0x1 (ENABLE): Timestamp Interrupt is enabled.
11:6	0h RO	**Reserved**
5	0h RW	**LPI Interrupt Enable (LPIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): LPI Interrupt is disabled. 0x1 (ENABLE): LPI Interrupt is enabled.
4	0h RW	**PMT Interrupt Enable (PMTIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PMT Interrupt is disabled. 0x1 (ENABLE): PMT Interrupt is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PHY Interrupt Enable (PHYIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PHY Interrupt is disabled. 0x1 (ENABLE): PHY Interrupt is enabled.
2:1	0h RO	**Reserved**
0	0h RW	**RGMII or SMII Interrupt Enable (RGSMIIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): RGMII or SMII Interrupt is disabled. 0x1 (ENABLE): RGMII or SMII Interrupt is enabled.

3.2.30 MAC_RX_TX_STATUS — Offset B8h

The Receive Transmit Status register contains the Receive and Transmit Error status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO	**Receive Watchdog Timeout (RWT):** This bit is set when a packet with length greater than 2,048 bytes is received (10,240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No receive watchdog timeout. 0x1 (ACTIVE): Receive watchdog timed out.
7:6	0h RO	**Reserved**
5	0h RO	**Excessive Collisions (EXCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Excessive collision is sensed.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Late Collision (LCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Late collision is sensed.
3	0h RO	**Excessive Deferral (EXDEF):** When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Excessive deferral. 0x1 (ACTIVE): Excessive deferral.
2	0h RO	**Loss of Carrier (LCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): Loss of carrier.
1	0h RO	**No Carrier (NCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): No carrier.
0	0h RO	**Transmit Jabber Timeout (TJT):** This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Transmit Jabber Timeout. 0x1 (ACTIVE): Transmit Jabber Timeout occurred.

3.2.31 MAC_PMT_CONTROL_STATUS — Offset C0h

The PMT Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Remote Wake-Up Packet Filter Register Pointer Reset (RWKFILTRST):** When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-Up Packet Filter Register Pointer is not Reset. 0x1 (ENABLE): Remote Wake-Up Packet Filter Register Pointer is Reset.
30:29	0h RO	**Reserved**
28:24	00h RO	**Remote Wake-up FIFO Pointer (RWKPTR):** This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	0h RO	**Reserved**
10	0h RW	**Remote Wake-up Packet Forwarding Enable (RWKPFE):** When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-up Packet Forwarding is disabled. 0x1 (ENABLE): Remote Wake-up Packet Forwarding is enabled.
9	0h RW	**Global Unicast (GLBLUCAST):** When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. 0x0 (DISABLE): Global unicast is disabled. 0x1 (ENABLE): Global unicast is enabled.
8:7	0h RO	**Reserved**
6	0h RO	**Remote Wake-Up Packet Received (RWKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Remote wake-up packet is received. 0x1 (ACTIVE): Remote wake-up packet is received.
5	0h RO	**Magic Packet Received (MGKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Magic packet is received. 0x1 (ACTIVE): Magic packet is received.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RO	**Reserved**
2	0h RW	**Remote Wake-Up Packet Enable (RWKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. 0x0 (DISABLE): Remote wake-up packet is disabled. 0x1 (ENABLE): Remote wake-up packet is enabled.
1	0h RW	**Magic Packet Enable (MGKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a magic packet. 0x0 (DISABLE): Magic Packet is disabled. 0x1 (ENABLE): Magic Packet is enabled.
0	0h RW	**Power Down (PWRDWN):** When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Power down is disabled. 0x1 (ENABLE): Power down is enabled.

3.2.32 MAC_RWK_PACKET_FILTER — Offset C4h

The TSN-GbE implements a filter lookup table programmed through the MAC_RWK_Packet_Filter register in which CRC, offset, and byte mask of the pattern embedded in the remote wakeup packet, and the filter-operation commands are programmed.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**RWK Packet Filter (WKUPFRMFTR):** This field contains the various controls of RWK Packet filter.

3.2.33 MAC_LPI_CONTROL_STATUS — Offset D0h

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**LPI Tx Clock Stop Enable (LPITCSE):** When this bit is set, the MAC indicates that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not indicate that the Tx clock to MAC can be stopped after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. 0x0 (DISABLE): LPI Tx Clock Stop is disabled. 0x1 (ENABLE): LPI Tx Clock Stop is enabled.
20	0h RW	**LPI Timer Enable (LPIATE):** This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. 0x0 (DISABLE): LPI Timer is disabled. 0x1 (ENABLE): LPI Timer is enabled.
19	0h RW	**LPI Tx Automate (LPITXA):** This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. 0x0 (DISABLE): LPI Tx Automate is disabled. 0x1 (ENABLE): LPI Tx Automate is enabled.
18	0h RW	**PHY Link Status Enable (PLSEN):** This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. 0x0 (DISABLE): PHY Link Status is disabled. 0x1 (ENABLE): PHY Link Status is enabled.
17	0h RW	**PHY Link Status (PLS):** This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. 0x0 (DISABLE): link is down. 0x1 (ENABLE): link is okay (UP).

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**LPI Enable (LPIEN):** When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. 0x0 (DISABLE): LPI state is disabled. 0x1 (ENABLE): LPI state is enabled.
15:10	0h RO	**Reserved**
9	0h RO	**Receive LPI State (RLPIST):** When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Receive LPI state not detected. 0x1 (ACTIVE): Receive LPI state detected.
8	0h RO	**Transmit LPI State (TLPIST):** When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Transmit LPI state not detected. 0x1 (ACTIVE): Transmit LPI state detected.
7:4	0h RO	**Reserved**
3	0h RO	**Receive LPI Exit (RLPIEX):** When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI exit not detected. 0x1 (ACTIVE): Receive LPI exit detected.
2	0h RO	**Receive LPI Entry (RLPIEN):** When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI entry not detected. 0x1 (ACTIVE): Receive LPI entry detected.
1	0h RO	**Transmit LPI Exit (TLPIEX):** When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI exit not detected. 0x1 (ACTIVE): Transmit LPI exit detected.
0	0h RO	**Transmit LPI Entry (TLPIEN):** When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI entry not detected. 0x1 (ACTIVE): Transmit LPI entry detected.

3.2.34 MAC_LPI_TIMERS_CONTROL — Offset D4h

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	03E80000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:16	3E8h RW	**LPI LS Timer (LST):** This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	0000h RW	**LPI TW Timer (TWT):** This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

3.2.35 MAC_LPI_ENTRY_TIMER — Offset D8h

This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:3	00000h RW	**LPI Entry Timer (LPIET):** This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	0h RO	**Reserved**

3.2.36 MAC_1US_TIC_COUNTER — Offset DCh

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000063h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	063h RW	**1US TIC Counter (TIC_1US_CNTR):** The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

3.2.37 MAC_PHYIF_CONTROL_STATUS — Offset F8h

The PHY Interface Control and Status register indicates the status signals received by the SGMII or RGMII interface (selected at reset) from the PHY. This register is optional.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO	**Link Status (LNKSTS):** This bit indicates whether the link is up (1'b1) or down (1'b0). 0x0 (INACTIVE): Link down. 0x1 (ACTIVE): Link up.
18:17	0h RO	**Link Speed (LNKSPEED):** This bit indicates the current speed of the link. 0x0 (M_2500K): 2.5 MHz. 0x1 (M_25M): 25 MHz. 0x2 (M_125M): 125 MHz. 0x3 (RSVD): Reserved.
16	0h RO	**Link Mode (LNKMOD):** This bit indicates the current mode of operation of the link. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RW	**Link Up or Down (LUD):** This bit indicates whether the link is up or down during transmission of configuration in the RGMII or SGMII interface. 0x0 (LINKDOWN): Link down. 0x1 (LINKUP): Link up.
0	0h RW	**Transmit Configuration in RGMII or SGMII (TC):** When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: - "Reduced Gigabit Media Independent Interface" - "Serial Media Independent Interface" - "Serial Gigabit Media Independent Interface" 0x0 (DISABLE): Disable Transmit Configuration in RGMII or SGMII. 0x1 (ENABLE): Enable Transmit Configuration in RGMII or SGMII.

3.2.38 MAC_VERSION — Offset 110h

The version register identifies the version of the GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	00005152h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	51h RO	**USERVER:** Version code
7:0	52h RO	**SNPSVER:** Version code

3.2.39 MAC_DEBUG — Offset 114h

The Debug register provides the debug status of various MAC blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RO	**MAC Transmit Packet Controller Status (TFCSTS):** This field indicates the state of the MAC Transmit Packet Controller module. 0x0 (IDLE): Idle state. 0x1 (WAITING): Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over. 0x2 (GEN_TX_PAU): Generating and transmitting a Pause control packet (in full-duplex mode). 0x3 (TRNSFR): Transferring input packet for transmission.
16	0h RO	**MAC GMII or MII Transmit Protocol Engine Status (TPESTS):** When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Transmit Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Transmit Protocol Engine Status detected.
15:3	0h RO	**Reserved**
2:1	0h RO	**MAC Receive Packet Controller FIFO Status (RFCFCSTS):** When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	0h RO	**MAC GMII or MII Receive Protocol Engine Status (RPESTS):** When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected.

3.2.40 MAC_HW_FEATURE0 — Offset 11Ch

This register indicates the presence of first set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	0EFD73F7h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	0h RO	**Active PHY Selected (ACTPHYSEL):** When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. 0x0 (GMII_MII): GMII or MII. 0x1 (RGMII): RGMII. 0x2 (SGMII): SGMII. 0x3 (TBI): TBI. 0x4 (RMII): RMII. 0x5 (RTBI): RTBI. 0x6 (SMII): SMII. 0x7 (REVMIII): RevMII.
27	1h RO	**Source Address or VLAN Insertion Enable (SAVLANINS):** This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected 0x0 (INACTIVE): Source Address or VLAN Insertion Enable option is not selected. 0x1 (ACTIVE): Source Address or VLAN Insertion Enable option is selected.
26:25	3h RO	**Timestamp System Time Source (TSSTSSEL):** This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INTRNL): Internal. 0x1 (EXTRNL): External. 0x2 (BOTH): Both. 0x3 (RSVD): Reserved.
24	0h RO	**MAC Addresses 64-127 Selected (MACADR64SEL):** This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected 0x0 (INACTIVE): MAC Addresses 64-127 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 64-127 Select option is selected.
23	1h RO	**MAC Addresses 32-63 Selected (MACADR32SEL):** This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected 0x0 (INACTIVE): MAC Addresses 32-63 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 32-63 Select option is selected.
22:18	1Fh RO	**MAC Addresses 1-31 Selected (ADDMACADRSEL):** This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option
17	0h RO	**Reserved**
16	1h RO	**Receive Checksum Offload Enabled (RXCOESEL):** This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected 0x0 (INACTIVE): Receive Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Receive Checksum Offload Enable option is selected.
15	0h RO	**Reserved**
14	1h RO	**Transmit Checksum Offload Enabled (TXCOESEL):** This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected 0x0 (INACTIVE): Transmit Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Transmit Checksum Offload Enable option is selected.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RO	**Energy Efficient Ethernet Enabled (EEESEL):** This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected 0x0 (INACTIVE): Energy Efficient Ethernet Enable option is not selected. 0x1 (ACTIVE): Energy Efficient Ethernet Enable option is selected.
12	1h RO	**IEEE 1588-2008 Timestamp Enabled (TSSEL):** This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INACTIVE): IEEE 1588-2008 Timestamp Enable option is not selected. 0x1 (ACTIVE): IEEE 1588-2008 Timestamp Enable option is selected.
11:10	0h RO	**Reserved**
9	1h RO	**ARP Offload Enabled (ARPOFFSEL):** This bit is set to 1 when the Enable IPv4 ARP Offload option is selected 0x0 (INACTIVE): ARP Offload Enable option is not selected. 0x1 (ACTIVE): ARP Offload Enable option is selected.
8	1h RO	**RMON Module Enable (MMCSEL):** This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected 0x0 (INACTIVE): RMON Module Enable option is not selected. 0x1 (ACTIVE): RMON Module Enable option is selected.
7	1h RO	**PMT Magic Packet Enable (MGKSEL):** This bit is set to 1 when the Enable Magic Packet Detection option is selected 0x0 (INACTIVE): PMT Magic Packet Enable option is not selected. 0x1 (ACTIVE): PMT Magic Packet Enable option is selected.
6	1h RO	**PMT Remote Wake-up Packet Enable (RWKSEL):** This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected 0x0 (INACTIVE): PMT Remote Wake-up Packet Enable option is not selected. 0x1 (ACTIVE): PMT Remote Wake-up Packet Enable option is selected.
5	1h RO	**SMA (MDIO) Interface (SMASEL):** This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected 0x0 (INACTIVE): SMA (MDIO) Interface not selected. 0x1 (ACTIVE): SMA (MDIO) Interface selected.
4	1h RO	**VLAN Hash Filter Selected (VLHASH):** This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected 0x0 (INACTIVE): VLAN Hash Filter not selected. 0x1 (ACTIVE): VLAN Hash Filter selected.
3	0h RO	**PCS Registers (TBI, SGMII, or RTBI PHY interface) (PCSSEL):** This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected 0x0 (INACTIVE): No PCS Registers (TBI, SGMII, or RTBI PHY interface). 0x1 (ACTIVE): PCS Registers (TBI, SGMII, or RTBI PHY interface).

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Half-duplex Support (HDSEL):** This bit is set to 1 when the half-duplex mode is selected 0x0 (INACTIVE): No Half-duplex support. 0x1 (ACTIVE): Half-duplex support.
1	1h RO	**1000 Mbps Support (GMIISEL):** This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 1000 Mbps support. 0x1 (ACTIVE): 1000 Mbps support.
0	1h RO	**10 or 100 Mbps Support (MIISEL):** This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 10 or 100 Mbps support. 0x1 (ACTIVE): 10 or 100 Mbps support.

3.2.41 MAC_HW_FEATURE1 — Offset 120h

This register indicates the presence of second set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	119F7A28h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	2h RO	**Total number of L3 or L4 Filters (L3L4FNUM):** This field indicates the total number of L3 or L4 filters: 0x0 (NOFILT): No L3 or L4 Filter. 0x1 (M_1FILT): 1 L3 or L4 Filter. 0x2 (M_2FILT): 2 L3 or L4 Filters. 0x3 (M_3FILT): 3 L3 or L4 Filters. 0x4 (M_4FILT): 4 L3 or L4 Filters. 0x5 (M_5FILT): 5 L3 or L4 Filters. 0x6 (M_6FILT): 6 L3 or L4 Filters. 0x7 (M_7FILT): 7 L3 or L4 Filters. 0x08 (M_8FILT): 8 L3 or L4 Filters.
26	0h RO	**Reserved**
25:24	1h RO	**Hash Table Size (HASHTBLSZ):** This field indicates the size of the hash table: 0x0 (NO_HT): No hash table. 0x1 (M_64): 64. 0x2 (M_128): 128. 0x3 (M_256): 256.

Bit Range	Default & Access	Field Name (ID): Description
23	1h RO	**One Step for PTP over UDP/IP Feature Enable (POUOST):** This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. 0x0 (INACTIVE): One Step for PTP over UDP/IP Feature is not selected. 0x1 (ACTIVE): One Step for PTP over UDP/IP Feature is selected.
22	0h RO	**Reserved**
21	0h RO	**Rx Side Only AV Feature Enable (RAVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. 0x0 (INACTIVE): Rx Side Only AV Feature is not selected. 0x1 (ACTIVE): Rx Side Only AV Feature is selected.
20	1h RO	**AV Feature Enable (AVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option is selected. 0x0 (INACTIVE): AV Feature is not selected. 0x1 (ACTIVE): AV Feature is selected.
19	1h RO	**DMA Debug Registers Enable (DBGMEMA):** This bit is set to 1 when the Debug Mode Enable option is selected 0x0 (INACTIVE): DMA Debug Registers option is not selected. 0x1 (ACTIVE): DMA Debug Registers option is selected.
18	1h RO	**TCP Segmentation Offload Enable (TSOEN):** This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected 0x0 (INACTIVE): TCP Segmentation Offload Feature is not selected. 0x1 (ACTIVE): TCP Segmentation Offload Feature is selected.
17	1h RO	**Split Header Feature Enable (SPHEN):** This bit is set to 1 when the Enable Split Header Structure option is selected 0x0 (INACTIVE): Split Header Feature is not selected. 0x1 (ACTIVE): Split Header Feature is selected.
16	1h RO	**DCB Feature Enable (DCBEN):** This bit is set to 1 when the Enable Data Center Bridging option is selected 0x0 (INACTIVE): DCB Feature is not selected. 0x1 (ACTIVE): DCB Feature is selected.
15:14	1h RO	**Address Width. (ADDR64):** This field indicates the configured address width: 0x0 (M_32): 32. 0x1 (M_40): 40. 0x2 (M_48): 48. 0x3 (RSVD): Reserved.
13	1h RO	**IEEE 1588 High Word Register Enable (ADVTHWORD):** This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected 0x0 (INACTIVE): IEEE 1588 High Word Register option is not selected. 0x1 (ACTIVE): IEEE 1588 High Word Register option is selected.
12	1h RO	**PTP Offload Enable (PTOEN):** This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. 0x0 (INACTIVE): PTP Offload feature is not selected. 0x1 (ACTIVE): PTP Offload feature is selected.
11	1h RO	**One-Step Timestamping Enable (OSTEN):** This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. 0x0 (INACTIVE): One-Step Timestamping feature is not selected. 0x1 (ACTIVE): One-Step Timestamping feature is selected.

Bit Range	Default & Access	Field Name (ID): Description
10:6	08h RO	**MTL Transmit FIFO Size (TXFIFOSIZE):** This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (RSVD): Reserved.
5	1h RO	**Single Port RAM Enable (SPRAM):** This bit is set to 1 when the Use single port RAM Feature is selected. 0x0 (INACTIVE): Single Port RAM feature is not selected. 0x1 (ACTIVE): Single Port RAM feature is selected.
4:0	08h RO	**MTL Receive FIFO Size (RXFIFOSIZE):** This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (M_256KB): 256 KB. 0x0C (RSVD): Reserved.

3.2.42 MAC_HW_FEATURE2 — Offset 124h

This register indicates the presence of third set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	22DF71C7h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	2h RO	**Number of Auxiliary Snapshot Inputs (AUXSNAPNUM):** This field indicates the number of auxiliary snapshot inputs: 0x0 (NO_AUXI): No auxiliary input. 0x1 (M_1_AUXI): 1 auxiliary input. 0x2 (M_2_AUXI): 2 auxiliary input. 0x3 (M_3_AUXI): 3 auxiliary input. 0x4 (M_4_AUXI): 4 auxiliary input. 0x5 (RSVD): Reserved.
27	0h RO	**Reserved**
26:24	2h RO	**Number of PPS Outputs (PPSOUTNUM):** This field indicates the number of PPS outputs: 0x0 (NO_PPSO): No PPS output. 0x1 (M_1_PPSO): 1 PPS output. 0x2 (M_2_PPSO): 2 PPS output. 0x3 (M_3_PPSO): 3 PPS output. 0x4 (M_4_PPSO): 4 PPS output. 0x5 (RSVD): Reserved.
23:22	3h RO	**Tx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (TDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
21:18	7h RO	**Number of DMA Transmit Channels (TXCHCNT):** This field indicates the number of DMA Transmit channels: 0x0 (M_1TXCH): 1 MTL Tx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1TDCSZ): 4. 0x1 (M_2TXCH): 2 MTL Tx Channels. 0x2 (M_2TDCSZ): 8. 0x2 (M_3TXCH): 3 MTL Tx Channels. 0x3 (M_3TDCSZ): 16. 0x3 (M_4TXCH): 4 MTL Tx Channels. 0x4 (M_5TXCH): 5 MTL Tx Channels. 0x5 (M_6TXCH): 6 MTL Tx Channels. 0x6 (M_7TXCH): 7 MTL Tx Channels. 0x7 (M_8TXCH): 8 MTL Tx Channels.
17:16	3h RO	**Rx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (RDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor

Bit Range	Default & Access	Field Name (ID): Description
15:12	7h RO	**Number of DMA Receive Channels (RXCHCNT):** This field indicates the number of DMA Receive channels: 0x0 (M_1RXCH): 1 MTL Rx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1RDCSZ): 4. 0x1 (M_2RXCH): 2 MTL Rx Channels. 0x2 (M_2RDCSZ): 8. 0x2 (M_3RXCH): 3 MTL Rx Channels. 0x3 (M_3RDCSZ): 16. 0x3 (M_4RXCH): 4 MTL Rx Channels. 0x4 (M_5RXCH): 5 MTL Rx Channels. 0x5 (M_6RXCH): 6 MTL Rx Channels. 0x6 (M_7RXCH): 7 MTL Rx Channels. 0x7 (M_8RXCH): 8 MTL Rx Channels.
11:10	0h RO	**Reserved**
9:6	7h RO	**Number of MTL Transmit Queues (TXQCNT):** This field indicates the number of MTL Transmit queues: 0x0 (M_1TXQ): 1 MTL Tx Queue. 0x1 (M_2TXQ): 2 MTL Tx Queues. 0x2 (M_3TXQ): 3 MTL Tx Queues. 0x3 (M_4TXQ): 4 MTL Tx Queues. 0x4 (M_5TXQ): 5 MTL Tx Queues. 0x5 (M_6TXQ): 6 MTL Tx Queues. 0x6 (M_7TXQ): 7 MTL Tx Queues. 0x7 (M_8TXQ): 8 MTL Tx Queues.
5:4	0h RO	**Reserved**
3:0	7h RO	**Number of MTL Receive Queues (RXQCNT):** This field indicates the number of MTL Receive queues: 0x0 (M_1RXQ): 1 MTL Rx Queue. 0x1 (M_2RXQ): 2 MTL Rx Queues. 0x2 (M_3RXQ): 3 MTL Rx Queues. 0x3 (M_4RXQ): 4 MTL Rx Queues. 0x4 (M_5RXQ): 5 MTL Rx Queues. 0x5 (M_6RXQ): 6 MTL Rx Queues. 0x6 (M_7RXQ): 7 MTL Rx Queues. 0x7 (M_8RXQ): 8 MTL Rx Queues.

3.2.43 MAC_HW_FEATURE3 — Offset 128h

This register indicates the presence of fourth set the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	2C395632h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	2h RO	**Automotive Safety Package (ASP):** Following are the encoding for the different Safety features 0x0 (NONE): No Safety features selected. 0x1 (ECC_ONLY): Only "ECC protection for external memory" feature is selected. 0x2 (AS_NPPE): All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature. 0x3 (AS_PPE): All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature.
27	1h RO	**Time Based Scheduling Enable (TBSSEL):** This bit is set to 1 when the Time Based Scheduling feature is selected. 0x0 (INACTIVE): Time Based Scheduling Enable feature is not selected. 0x1 (ACTIVE): Time Based Scheduling Enable feature is selected.
26	1h RO	**Frame Preemption Enable (FPESEL):** This bit is set to 1 when the Enable Frame preemption feature is selected. 0x0 (INACTIVE): Frame Preemption Enable feature is not selected. 0x1 (ACTIVE): Frame Preemption Enable feature is selected.
25:22	0h RO	**Reserved**
21:20	3h RO	**Width of the Time Interval field in the Gate Control List (ESTWID):** This field indicates the width of the Configured Time Interval Field 0x0 (NOWIDTH): Width not configured. 0x1 (WIDTH16): 16. 0x2 (WIDTH20): 20. 0x3 (WIDTH24): 24.
19:17	4h RO	**Depth of the Gate Control List (ESTDEP):** This field indicates the depth of Gate Control list expressed as Log2(512)-5 0x0 (NODEPTH): No Depth configured. 0x1 (DEPTH64): 64. 0x2 (DEPTH128): 128. 0x3 (DEPTH256): 256. 0x4 (DEPTH512): 512. 0x5 (DEPTH1024): 1024. 0x6 (RSVD): Reserved.
16	1h RO	**Enhancements to Scheduling Traffic Enable (ESTSEL):** This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. 0x0 (INACTIVE): Enable Enhancements to Scheduling Traffic feature is not selected. 0x1 (ACTIVE): Enable Enhancements to Scheduling Traffic feature is selected.
15	0h RO	**Reserved**
14:13	2h RO	**Flexible Receive Parser Table Entries size (FRPES):** This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. 0x0 (M_64ENTR): 64 Entries. 0x1 (M_128ENTR): 128 Entries. 0x2 (M_256ENTR): 256 Entries. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12:11	2h RO	**Flexible Receive Parser Buffer size (FRPBS):** This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. 0x0 (M_64BYTES): 64 Bytes. 0x1 (M_128BYTES): 128 Bytes. 0x2 (M_256BYTES): 256 Bytes. 0x3 (RSVD): Reserved.
10	1h RO	**Flexible Receive Parser Selected (FRPSEL):** This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. 0x0 (INACTIVE): Flexible Receive Parser feature is not selected. 0x1 (ACTIVE): Flexible Receive Parser feature is selected.
9	1h RO	**Broadcast/Multicast Packet Duplication (PDUPSEL):** This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. 0x0 (INACTIVE): Broadcast/Multicast Packet Duplication feature is not selected. 0x1 (ACTIVE): Broadcast/Multicast Packet Duplication feature is selected.
8:6	0h RO	**Reserved**
5	1h RO	**Double VLAN Tag Processing Selected (DVLAN):** This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. 0x0 (INACTIVE): Double VLAN option is not selected. 0x1 (ACTIVE): Double VLAN option is selected.
4	1h RO	**Queue/Channel based VLAN tag insertion on Tx Enable (CBTISEL):** This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. 0x0 (INACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected. 0x1 (ACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is selected.
3	0h RO	**Reserved**
2:0	2h RO	**Number of Extended VLAN Tag Filters Enabled (NRVF):** This field indicates the Number of Extended VLAN Tag Filters selected: 0x0 (NO_ERVLAN): No Extended Rx VLAN Filters. 0x1 (M_4_ERVLAN): 4 Extended Rx VLAN Filters. 0x2 (M_8_ERVLAN): 8 Extended Rx VLAN Filters. 0x3 (M_16_ERVLAN): 16 Extended Rx VLAN Filters. 0x4 (M_24_ERVLAN): 24 Extended Rx VLAN Filters. 0x5 (M_32_ERVLAN): 32 Extended Rx VLAN Filters. 0x6 (RSVD): Reserved.

3.2.44 MAC_DPP_FSM_INTERRUPT_STATUS — Offset 140h

This register contains the status of Automotive Safety related Data Path Parity Errors, Interface Timeout Errors, FSM State Parity Errors and FSM State Timeout Errors. All the non-Reserved bits are cleared on read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**FSM State Parity Error Status (FSMPES):** This field when set indicates one of the FSMs State registers has a parity error detected. 0x0 (INACTIVE): FSM State Parity Error Status not detected. 0x1 (ACTIVE): FSM State Parity Error Status detected.
23:18	0h RO	**Reserved**
17	0h RW	**Slave Read/Write Timeout Error Status (SLVTES):** This field when set indicates that an Application/CSR Timeout has occurred on the AXI slave interface. 0x0 (INACTIVE): Slave Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Slave Read/Write Timeout Error Status detected.
16	0h RW	**Master Read/Write Timeout Error Status (MSTTES):** This field when set indicates that an Application/CSR Timeout has occurred on the master (AXI/AHB/ARI/ATI) interface. 0x0 (INACTIVE): Master Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Master Read/Write Timeout Error Status detected.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Status (PTES):** This field when set indicates that one of the PTP FSM Timeout has occurred. 0x0 (INACTIVE): PTP FSM Timeout Error Status not detected. 0x1 (ACTIVE): PTP FSM Timeout Error Status detected.
11	0h RW	**APP FSM Timeout Error Status (ATES):** This field when set indicates that one of the APP FSM Timeout has occurred. 0x0 (INACTIVE): APP FSM Timeout Error Status not detected. 0x1 (ACTIVE): APP FSM Timeout Error Status detected.
10	0h RW	**CSR FSM Timeout Error Status (CTES):** This field when set indicates that one of the CSR FSM Timeout has occurred. 0x0 (INACTIVE): CSR FSM Timeout Error Status not detected. 0x1 (ACTIVE): CSR FSM Timeout Error Status detected.
9	0h RW	**Rx FSM Timeout Error Status (RTES):** This field when set indicates that one of the Rx FSM Timeout has occurred. 0x0 (INACTIVE): Rx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Rx FSM Timeout Error Status detected.
8	0h RW	**Tx FSM Timeout Error Status (TTES):** This field when set indicates that one of the Tx FSM Timeout has occurred. 0x0 (INACTIVE): Tx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Tx FSM Timeout Error Status detected.
7	0h RW	**AXI Slave Read data path Parity checker Error Status (ASRPES):** This bit when set indicates that parity error is detected at the AXI Slave read data interface. 0x0 (INACTIVE): AXI Slave Read data path Parity checker Error Status not detected. 0x1 (ACTIVE): AXI Slave Read data path Parity checker Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**CSR Write data path Parity checker Error Status (CWPES):** This bit when set indicates that parity error is detected at the CSR write data interface on mci_wdata_i (or at PC8 checker as shown in AXI slave Interface Data path parity protection diagram). When EPSI bit of MTL_DPP_Control register is set and if any parity mis-match is detected on the input slave parity ports (or at PC7 checker in the AXI slave Interface Data path parity protection diagram) sets this bit to one. 0x0 (INACTIVE): CSR Write data path Parity checker Error Status not detected. 0x1 (ACTIVE): CSR Write data path Parity checker Error Status detected.
5	0h RW	**Application Receive interface data path Parity Error Status (ARPES):** This bit when set indicates that a parity error is detected by the hardware internally at the interface with the application. 0x0 (INACTIVE): Application Receive interface data path Parity Error Status not detected. 0x1 (ACTIVE): Application Receive interface data path Parity Error Status detected.
4	0h RW	**MTL TX Status data path Parity checker Error Status (MTSPES):** This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL TX Status data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL TX Status data path Parity checker Error Status detected.
3	0h RW	**MTL data path Parity checker Error Status (MPES):** This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL data path Parity checker Error Status detected.
2	0h RW	**Read Descriptor Parity checker Error Status (RDPES):** This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): Read Descriptor Parity checker Error Status not detected. 0x1 (ACTIVE): Read Descriptor Parity checker Error Status detected.
1	0h RW	**TSO data path Parity checker Error Status (TPES):** This bit when set indicates that a parity error is detected at the DMA TSO parity checker (or at PC2 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): TSO data path Parity checker Error Status not detected. 0x1 (ACTIVE): TSO data path Parity checker Error Status detected.
0	0h RO	**Reserved**

3.2.45 MAC_AXI_SLV_DPE_ADDR_STATUS — Offset 144h

This register indicates the CSR address corresponding to the CSR write data on which parity error occured.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RO	**AXI Slave data path Parity Error Address Status (ASPEAS):** This field holds the CSR address for which parity error is detected on the CSR write data. This field holds the first address for which parity error is detected on the write data and is cleared on read.

3.2.46 MAC_FSM_CONTROL — Offset 148h

This register is used to control the FSM State parity and timeout error injection in Debug mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**PTP Large/Normal Mode Select (PLGRNML):** This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for PTP domain. 0x1 (ENABLE): large mode tic generation is used for PTP domain.
27	0h RW	**APP Large/Normal Mode Select (ALGRNML):** This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for APP domain. 0x1 (ENABLE): large mode tic generation is used for APP domain.
26	0h RW	**CSR Large/Normal Mode Select (CLGRNML):** This field when set indicates that large mode tic generation is used for CSR domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for CSR domain. 0x1 (ENABLE): large mode tic generation is used for CSR domain.
25	0h RW	**Rx Large/Normal Mode Select (RLGRNML):** This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Rx domain. 0x1 (ENABLE): large mode tic generation is used for Rx domain.
24	0h RW	**Tx Large/Normal Mode Select (TLGRNML):** This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Tx domain. 0x1 (ENABLE): large mode tic generation is used for Tx domain.
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**PTP FSM Parity Error Injection (PPEIN):** This field when set indicates that Error Injection for PTP FSM Parity is enabled. 0x0 (DISABLE): PTP FSM Parity Error Injection is disabled. 0x1 (ENABLE): PTP FSM Parity Error Injection is enabled.
19	0h RW	**APP FSM Parity Error Injection (APEIN):** This field when set indicates that Error Injection for APP FSM Parity is enabled. 0x0 (DISABLE): APP FSM Parity Error Injection is disabled. 0x1 (ENABLE): APP FSM Parity Error Injection is enabled.
18	0h RW	**CSR FSM Parity Error Injection (CPEIN):** This field when set indicates that Error Injection for CSR Parity is enabled. 0x0 (DISABLE): CSR FSM Parity Error Injection is disabled. 0x1 (ENABLE): CSR FSM Parity Error Injection is enabled.
17	0h RW	**Rx FSM Parity Error Injection (RPEIN):** This field when set indicates that Error Injection for RX FSM Parity is enabled. 0x0 (DISABLE): Rx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Rx FSM Parity Error Injection is enabled.
16	0h RW	**Tx FSM Parity Error Injection (TPEIN):** This field when set indicates that Error Injection for TX FSM Parity is enabled. 0x0 (DISABLE): Tx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Tx FSM Parity Error Injection is enabled.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Injection (PTEIN):** This field when set indicates that Error Injection for PTP FSM timeout is enabled. 0x0 (DISABLE): PTP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): PTP FSM Timeout Error Injection is enabled.
11	0h RW	**APP FSM Timeout Error Injection (ATEIN):** This field when set indicates that Error Injection for APP FSM timeout is enabled. 0x0 (DISABLE): APP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): APP FSM Timeout Error Injection is enabled.
10	0h RW	**CSR FSM Timeout Error Injection (CTEIN):** This field when set indicates that Error Injection for CSR timeout is enabled. 0x0 (DISABLE): CSR FSM Timeout Error Injection is disabled. 0x1 (ENABLE): CSR FSM Timeout Error Injection is enabled.
9	0h RW	**Rx FSM Timeout Error Injection (RTEIN):** This field when set indicates that Error Injection for RX FSM timeout is enabled. 0x0 (DISABLE): Rx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Rx FSM Timeout Error Injection is enabled.
8	0h RW	**Tx FSM Timeout Error Injection (TTEIN):** This field when set indicates that Error Injection for TX FSM timeout is enabled. 0x0 (DISABLE): Tx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Tx FSM Timeout Error Injection is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**PRTYEN:** This bit when set indicates that the FSM parity feature is enabled. 0x0 (DISABLE): FSM Parity feature is disabled. 0x1 (ENABLE): FSM Parity feature is enabled.
0	0h RW	**TMOUTEN:** This bit when set indicates that the FSM timeout feature is enabled. 0x0 (DISABLE): FSM timeout feature is disabled. 0x1 (ENABLE): FSM timeout feature is enabled.

3.2.47 MAC_FSM_ACT_TIMER — Offset 14Ch

This register is used to select the FSM and Interface Timeout values.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**LTMRMD:** This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
19:16	0h RW	**NTMRMD:** This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
15:10	0h RO	**Reserved**
9:0	000h RW	**TMR:** This field indicates the number of CSR clocks required to generate 1us tic.

3.2.48 SNPS_SCS_REG1 — Offset 150h

Reserved

Type	Size	Offset	Default
MMIO	32 bit	BAR + 150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Reserved**

3.2.49 MAC_MDIO_ADDRESS — Offset 200h

The MDIO Address register controls the management cycles to external PHY through a management interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**Preamble Suppression Enable (PSE):** When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. 0x0 (DISABLE): Preamble Suppression disabled. 0x1 (ENABLE): Preamble Suppression enabled.
26	0h RW	**Back to Back transactions (BTB):** When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. 0x0 (DISABLE): Back to Back transactions disabled. 0x1 (ENABLE): Back to Back transactions enabled.
25:21	00h RW	**Physical Layer Address (PA):** This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	00h RW	**Register/Device Address (RDA):** These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	0h RO	**Reserved**
14:12	0h RW	**Number of Trailing Clocks (NTC):** This field controls the number of trailing clock cycles generated on the MDIO Clock (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**CSR Clock Range (CR):** The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: - 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 - 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 - 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 - 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 - 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 - 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 - 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 - 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz freqency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: - 1000: CSR clock/4 - 1001: CSR clock/6 - 1010: CSR clock/8 - 1011: CSR clock/10 - 1100: CSR clock/12 - 1101: CSR clock/14 - 1110: CSR clock/16 - 1111: CSR clock/18
7:5	0h RO	**Reserved**
4	0h RW	**Skip Address Packet (SKAP):** When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0x0 (DISABLE): Skip Address Packet is disabled. 0x1 (ENABLE): Skip Address Packet is enabled.
3	0h RW	**GMII Operation Command 1 (GOC_1):** This bit is higher bit of the operation command to the PHY or GOC_1 and GOC_O are encoded as follows: - 00: Reserved - 01: Write - 10: Post Read Increment Address for Clause 45 PHY - 11: Read When Clause 22 PHY is enabled, only Write and Read commands are valid. 0x0 (DISABLE): GMII Operation Command 1 is disabled. 0x1 (ENABLE): GMII Operation Command 1 is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GMII Operation Command 0 (GOC_0):** This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. 0x0 (DISABLE): GMII Operation Command 0 is disabled. 0x1 (ENABLE): GMII Operation Command 0 is enabled.
1	0h RW	**Clause 45 PHY Enable (C45E):** When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0x0 (DISABLE): Clause 45 PHY is disabled. 0x1 (ENABLE): Clause 45 PHY is enabled.
0	0h RW	**GMII Busy (GB):** The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDI field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): GMII Busy is disabled. 0x1 (ENABLE): GMII Busy is enabled.

3.2.50 MAC_MDIO_DATA — Offset 204h

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Register Address (RA):** This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	0000h RW	**GMII Data (GD):** This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

3.2.51 MAC_GPIO_CONTROL — Offset 208h

The GPIO Control register controls the GPIO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

3.2.52 MAC_GPIO_STATUS — Offset 20Ch

The General Purpose IO register provides the control to drive the following: up to 16 bits of output ports (GPO) and status of up to 16 input ports (GPIS).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20Ch	00000000h

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th colspan="3">Field Name (ID): Description</th></tr>
<tr><td>31:20</td><td>0h
RO</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="7">19:16</td><td rowspan="7">0h
RW</td><td colspan="3">Trigger Snapshot (GPO1):
Active-high signal. The rising edge of this signal triggers snapshot of current PMC ART and System timer values. The system timer value is stored into AUX FIFO. An interrupt is generated upon snapshotting.
The PMC ART timer values is stored in 4x 16-bit ART snapshot register and is read through MDIO registers.</td></tr>
<tr><td>MAC_GPIO[3]</td><td>MAC_GPIO[0]</td><td>PTP REF Clock to GbE MAC</td></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>PSE PLL_PTP = 200MHz</td></tr>
<tr><td colspan="3">19th bit and 16th bit are used for selecting Precision Time Protocol (PTP). This bits programming are used in GbE Time Synchronization CTS Test.

- 19th Bit: MAC_GPIO[3]
- 16th Bit: MAC_GPIO[0]</td></tr>
<tr><td>15:4</td><td>0h
RO</td><td colspan="3">Reserved</td></tr>
<tr><td>3:0</td><td>0h
RW</td><td colspan="3">GPIS:
General Purpose Input Status. This field gives the status of the signals connected to the gpi_i port. This field is of the following types based on the setting of the corresponding GPIT field of MAC_GPIO_Control register:
- Latched-Low (LL): This field is cleared when the corresponding gpi_i input becomes low. This field remains low until the application reads this field after which this field reflects the current value of gpi_i input.
- Latched-High (LH): This field is set when the corresponding gpi_i input becomes high. This field remains high until the application reads this field after which this field reflects the current value of gpi_i input. The number of bits available in this field depends on the GP Input Signal Width option. Other bits are not used (reserved and always reset). 0000H</td></tr>
</table>

3.2.53 MAC_ARP_ADDRESS — Offset 210h

The ARP Address register contains the IPv4 Destination Address of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ARP Protocol Address (ARPPA):** This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

3.2.54 MAC_CSR_SW_CTRL — Offset 230h

This register contains SW programmable controls for changing the CSR access response and status bits clearing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Slave Error Response Enable (SEEN):** When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space. 0x0 (DISABLE): Slave Error Response is disabled. 0x1 (ENABLE): Slave Error Response is enabled.
7:1	0h RO	**Reserved**
0	0h RW	**Register Clear on Write 1 Enable (RCWE):** When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. 0x0 (DISABLE): Register Clear on Write 1 is disabled. 0x1 (ENABLE): Register Clear on Write 1 is enabled.

3.2.55 MAC_FPE_CTRL_STS — Offset 234h

This register controls the operation of Frame Preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Transmitted Respond Frame (TRSP):** Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Respond Frame. 0x1 (ACTIVE): transmitted Respond Frame.
18	0h RW	**Transmitted Verify Frame (TVER):** Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Verify Frame. 0x1 (ACTIVE): transmitted Verify Frame.
17	0h RW	**Received Respond Frame (RRSP):** Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Respond Frame. 0x1 (ACTIVE): Received Respond Frame.
16	0h RW	**Received Verify Frame (RVER):** Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Verify Frame. 0x1 (ACTIVE): Received Verify Frame.
15:4	0h RO	**Reserved**
3	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Send Respond mPacket (SRSP):** When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Respond mPacket is disabled. 0x1 (ENABLE): Send Respond mPacket is enabled.
1	0h RW	**Send Verify mPacket (SVER):** When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Verify mPacket is disabled. 0x1 (ENABLE): Send Verify mPacket is enabled.
0	0h RW	**Enable Tx Frame Preemption (EFPE):** When set Frame Preemption Tx functionality is enabled. 0x0 (DISABLE): Tx Frame Preemption is disabled. 0x1 (ENABLE): Tx Frame Preemption is enabled.

3.2.56 MAC_EXT_CFG1 — Offset 238h

This register contains Split mode control field and offset field for Split Header feature.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000002h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h RW	**Split Mode (SPLM):** These bits indicate the mode of splitting the incoming Rx packets. They are 0x0 (L3L4): Split at L3/L4 header. 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame. 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped. 0x3 (RSVD): Reserved.
7	0h RO	**Reserved**
6:0	02h RW	**Split Offset (SPLOFST):** These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

3.2.57 MAC_PRESN_TIME_NS — Offset 240h

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns.

DWC_EQOS_FLEXI_PPS_OUT_EN=1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MAC 1722 Presentation Time in ns (MPTN):** These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns

3.2.58 MAC_PRESN_TIME_UPDT — Offset 244h

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register).

DWC_EQOS_FLEXI_PPS_OUT_EN=1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC 1722 Presentation Time Update (MPTU):** This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction

3.2.59 MAC_ADDRESS0_HIGH — Offset 300h

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] of the MAC Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 300h	8000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Address Enable (AE):** This bit is always set to 1. 0x0 (DISABLE): INVALID : This bit must be always set to 1. 0x1 (ENABLE): This bit is always set to 1.
30:24	0h RO	**Reserved**
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	FFFFh RW	**MAC Address0[47:32] (ADDRHI):** This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

3.2.60 MAC_ADDRESS0_LOW — Offset 304h

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 304h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address0[31:0] (ADDRLO):** This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

3.2.61 MAC_ADDRESS1_HIGH — Offset 308h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 308h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.62 MAC_ADDRESS1_LOW — Offset 30Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.63 MAC_ADDRESS2_HIGH — Offset 310h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 310h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.64 MAC_ADDRESS2_LOW — Offset 314h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 314h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.65 MAC_ADDRESS3_HIGH — Offset 318h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 318h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.66 MAC_ADDRESS3_LOW — Offset 31Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 31Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.67 MAC_ADDRESS4_HIGH — Offset 320h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 320h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.68 MAC_ADDRESS4_LOW — Offset 324h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 324h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.69 MAC_ADDRESS5_HIGH — Offset 328h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 328h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.70 MAC_ADDRESS5_LOW — Offset 32Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 32Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.71 MAC_ADDRESS6_HIGH — Offset 330h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 330h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.72 MAC_ADDRESS6_LOW — Offset 334h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 334h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.73 MAC_ADDRESS7_HIGH — Offset 338h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 338h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.74 MAC_ADDRESS7_LOW — Offset 33Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 33Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.75 MAC_ADDRESS8_HIGH — Offset 340h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 340h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.76 MAC_ADDRESS8_LOW — Offset 344h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 344h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.77 MAC_ADDRESS9_HIGH — Offset 348h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 348h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.78 MAC_ADDRESS9_LOW — Offset 34Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.79 MAC_ADDRESS10_HIGH — Offset 350h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 350h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.80 MAC_ADDRESS10_LOW — Offset 354h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 354h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.81 MAC_ADDRESS11_HIGH — Offset 358h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 358h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.82 MAC_ADDRESS11_LOW — Offset 35Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 35Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.83 MAC_ADDRESS12_HIGH — Offset 360h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 360h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.84 MAC_ADDRESS12_LOW — Offset 364h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 364h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.85 MAC_ADDRESS13_HIGH — Offset 368h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 368h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.86 MAC_ADDRESS13_LOW — Offset 36Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 36Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.87 MAC_ADDRESS14_HIGH — Offset 370h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 370h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.88 MAC_ADDRESS14_LOW — Offset 374h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 374h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.89 MAC_ADDRESS15_HIGH — Offset 378h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 378h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.90 MAC_ADDRESS15_LOW — Offset 37Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 37Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.91 MAC_ADDRESS16_HIGH — Offset 380h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 380h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.92 MAC_ADDRESS16_LOW — Offset 384h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 384h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.93 MAC_ADDRESS17_HIGH — Offset 388h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 388h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.94 MAC_ADDRESS17_LOW — Offset 38Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.95 MAC_ADDRESS18_HIGH — Offset 390h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 390h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.96 MAC_ADDRESS18_LOW — Offset 394h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 394h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.97 MAC_ADDRESS19_HIGH — Offset 398h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 398h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.98 MAC_ADDRESS19_LOW — Offset 39Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 39Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.99 MAC_ADDRESS20_HIGH — Offset 3A0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.100 MAC_ADDRESS20_LOW — Offset 3A4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.101 MAC_ADDRESS21_HIGH — Offset 3A8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.102 MAC_ADDRESS21_LOW — Offset 3ACh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3ACh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.103 MAC_ADDRESS22_HIGH — Offset 3B0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.104 MAC_ADDRESS22_LOW — Offset 3B4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.105 MAC_ADDRESS23_HIGH — Offset 3B8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.106 MAC_ADDRESS23_LOW — Offset 3BCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3BCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.107 MAC_ADDRESS24_HIGH — Offset 3C0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.108 MAC_ADDRESS24_LOW — Offset 3C4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.109 MAC_ADDRESS25_HIGH — Offset 3C8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.110 MAC_ADDRESS25_LOW — Offset 3CCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3CCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.111 MAC_ADDRESS26_HIGH — Offset 3D0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.112 MAC_ADDRESS26_LOW — Offset 3D4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.113 MAC_ADDRESS27_HIGH — Offset 3D8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3D8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.114 MAC_ADDRESS27_LOW — Offset 3DCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3DCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.115 MAC_ADDRESS28_HIGH — Offset 3E0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.116 MAC_ADDRESS28_LOW — Offset 3E4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.117 MAC_ADDRESS29_HIGH — Offset 3E8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3E8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.118 MAC_ADDRESS29_LOW — Offset 3ECh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3ECh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.119 MAC_ADDRESS30_HIGH — Offset 3F0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.120 MAC_ADDRESS30_LOW — Offset 3F4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.121 MAC_ADDRESS31_HIGH — Offset 3F8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3F8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

3.2.122 MAC_ADDRESS31_LOW — Offset 3FCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3FCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

3.2.123 MAC_ADDRESS32_HIGH — Offset 400h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 400h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.124 MAC_ADDRESS32_LOW — Offset 404h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 404h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.125 MAC_ADDRESS33_HIGH — Offset 408h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 408h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.126 MAC_ADDRESS33_LOW — Offset 40Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.127 MAC_ADDRESS34_HIGH — Offset 410h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 410h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.128 MAC_ADDRESS34_LOW — Offset 414h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 414h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.129 MAC_ADDRESS35_HIGH — Offset 418h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 418h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.130 MAC_ADDRESS35_LOW — Offset 41Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 41Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.131 MAC_ADDRESS36_HIGH — Offset 420h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 420h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.132 MAC_ADDRESS36_LOW — Offset 424h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 424h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.133 MAC_ADDRESS37_HIGH — Offset 428h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 428h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.134 MAC_ADDRESS37_LOW — Offset 42Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 42Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.135 MAC_ADDRESS38_HIGH — Offset 430h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 430h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.136 MAC_ADDRESS38_LOW — Offset 434h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 434h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.137 MAC_ADDRESS39_HIGH — Offset 438h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 438h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.138 MAC_ADDRESS39_LOW — Offset 43Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 43Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.139 MAC_ADDRESS40_HIGH — Offset 440h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 440h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.140 MAC_ADDRESS40_LOW — Offset 444h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 444h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.141 MAC_ADDRESS41_HIGH — Offset 448h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 448h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.142 MAC_ADDRESS41_LOW — Offset 44Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.143 MAC_ADDRESS42_HIGH — Offset 450h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 450h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.144 MAC_ADDRESS42_LOW — Offset 454h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 454h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.145 MAC_ADDRESS43_HIGH — Offset 458h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 458h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.146 MAC_ADDRESS43_LOW — Offset 45Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 45Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.147 MAC_ADDRESS44_HIGH — Offset 460h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 460h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.148 MAC_ADDRESS44_LOW — Offset 464h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 464h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.149 MAC_ADDRESS45_HIGH — Offset 468h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 468h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.150 MAC_ADDRESS45_LOW — Offset 46Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 46Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.151 MAC_ADDRESS46_HIGH — Offset 470h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 470h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.152 MAC_ADDRESS46_LOW — Offset 474h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 474h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.153 MAC_ADDRESS47_HIGH — Offset 478h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 478h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.154 MAC_ADDRESS47_LOW — Offset 47Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 47Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.155 MAC_ADDRESS48_HIGH — Offset 480h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 480h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.156 MAC_ADDRESS48_LOW — Offset 484h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 484h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.157 MAC_ADDRESS49_HIGH — Offset 488h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 488h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.158 MAC_ADDRESS49_LOW — Offset 48Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.159 MAC_ADDRESS50_HIGH — Offset 490h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 490h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.160 MAC_ADDRESS50_LOW — Offset 494h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 494h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.161 MAC_ADDRESS51_HIGH — Offset 498h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 498h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.162 MAC_ADDRESS51_LOW — Offset 49Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 49Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.163 MAC_ADDRESS52_HIGH — Offset 4A0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.164 MAC_ADDRESS52_LOW — Offset 4A4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.165 MAC_ADDRESS53_HIGH — Offset 4A8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4A8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.166 MAC_ADDRESS53_LOW — Offset 4ACh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4ACh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.167 MAC_ADDRESS54_HIGH — Offset 4B0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.168 MAC_ADDRESS54_LOW — Offset 4B4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.169 MAC_ADDRESS55_HIGH — Offset 4B8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4B8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.170 MAC_ADDRESS55_LOW — Offset 4BCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4BCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.171 MAC_ADDRESS56_HIGH — Offset 4C0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.172 MAC_ADDRESS56_LOW — Offset 4C4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.173 MAC_ADDRESS57_HIGH — Offset 4C8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4C8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.174 MAC_ADDRESS57_LOW — Offset 4CCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4CCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.175 MAC_ADDRESS58_HIGH — Offset 4D0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.176 MAC_ADDRESS58_LOW — Offset 4D4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.177 MAC_ADDRESS59_HIGH — Offset 4D8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4D8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.178 MAC_ADDRESS59_LOW — Offset 4DCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4DCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.179 MAC_ADDRESS60_HIGH — Offset 4E0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.180 MAC_ADDRESS60_LOW — Offset 4E4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.181 MAC_ADDRESS61_HIGH — Offset 4E8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4E8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.182 MAC_ADDRESS61_LOW — Offset 4ECh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4ECh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.183 MAC_ADDRESS62_HIGH — Offset 4F0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F0h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.184 MAC_ADDRESS62_LOW — Offset 4F4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F4h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.185 MAC_ADDRESS63_HIGH — Offset 4F8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4F8h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

3.2.186 MAC_ADDRESS63_LOW — Offset 4FCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4FCh	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

3.2.187 MMC_CONTROL — Offset 700h

This register establishes the operating mode of MAC Management Counters.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 700h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Update MMC Counters for Dropped Broadcast Packets (UCDBC):** Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. 0x0 (DISABLE): Update MMC Counters for Dropped Broadcast Packets is disabled. 0x1 (ENABLE): Update MMC Counters for Dropped Broadcast Packets is enabled.
7:6	0h RO	**Reserved**
5	0h RW	**Full-Half Preset (CNTPRSTLVL):** When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. 0x0 (DISABLE): Full-Half Preset is disabled. 0x1 (ENABLE): Full-Half Preset is enabled.
4	0h RW	**Counters Preset (CNTPRST):** When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
3	0h RW	**MMC Counter Freeze (CNTFREEZ):** When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. 0x0 (DISABLE): MMC Counter Freeze is disabled. 0x1 (ENABLE): MMC Counter Freeze is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Reset on Read (RSTONRD):** When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. 0x0 (DISABLE): Reset on Read is disabled. 0x1 (ENABLE): Reset on Read is enabled.
1	0h RW	**Counter Stop Rollover (CNTSTOPRO):** When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0x0 (DISABLE): Counter Stop Rollover is disabled. 0x1 (ENABLE): Counter Stop Rollover is enabled.
0	0h RW	**Counters Reset (CNTRST):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.

3.2.188 MMC_RX_INTERRUPT — Offset 704h

This register maintains the interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur:

- Receive statistic counters reach half of their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter).

- Receive statistic counters cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter).

When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Note: R_SS_RC means that this register bit is set internally, and it is cleared when the Counter register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 704h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Receive LPI transition counter interrupt status (RXLPITRCIS):** This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Receive LPI microsecond counter interrupt status (RXLPIUSCIS):** This bit is set when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Receive Control Packet Counter Interrupt Status (RXCTRLPIS):** This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Control Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Control Packet Counter Interrupt Status detected.
24	0h RO	**MMC Receive Error Packet Counter Interrupt Status (RXRCVERRPIS):** This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Error Packet Counter Interrupt Status detected.
23	0h RO	**MMC Receive Watchdog Error Packet Counter Interrupt Status (RXWDOGPIS):** This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected.
22	0h RO	**MMC Receive VLAN Good Bad Packet Counter Interrupt Status (RXVLANGBPIS):** This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status detected.
21	0h RO	**MMC Receive FIFO Overflow Packet Counter Interrupt Status (RXFOVPIS):** This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**MMC Receive Pause Packet Counter Interrupt Status (RXPAUSPIS):** This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected.
19	0h RO	**MMC Receive Out Of Range Error Packet Counter Interrupt Status. (RXORANGEPIS):** This bit is set when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Receive Length Error Packet Counter Interrupt Status (RXLENERPIS):** This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Length Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Length Error Packet Counter Interrupt Status detected.
17	0h RO	**MMC Receive Unicast Good Packet Counter Interrupt Status (RXUCGPIS):** This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status detected.
16	0h RO	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (RX1024TMAXOCTGBPIS):** This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
15	0h RO	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (RX512T1023OCTGBPIS):** This bit is set when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.
14	0h RO	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status (RX256T511OCTGBPIS):** This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status (RX128T255OCTGBPIS):** This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status (RX65T127OCTGBPIS):** This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status (RX64OCTGBPIS):** This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive Oversize Good Packet Counter Interrupt Status (RXOSIZEGPIS):** This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive Undersize Good Packet Counter Interrupt Status (RXUSIZEGPIS):** This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status detected.
8	0h RO	**MMC Receive Jabber Error Packet Counter Interrupt Status (RXJABERPIS):** This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**MMC Receive Runt Packet Counter Interrupt Status (RXRUNTPIS):** This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Runt Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Runt Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive Alignment Error Packet Counter Interrupt Status (RXALGNERPIS):** This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive CRC Error Packet Counter Interrupt Status (RXCRCERPIS):** This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive Multicast Good Packet Counter Interrupt Status (RXMCGPIS):** This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive Broadcast Good Packet Counter Interrupt Status (RXBCGPIS):** This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive Good Octet Counter Interrupt Status (RXGOCTIS):** This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Octet Counter Interrupt Status detected.
1	0h RO	**MMC Receive Good Bad Octet Counter Interrupt Status (RXGBOCTIS):** This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status detected.
0	0h RO	**MMC Receive Good Bad Packet Counter Interrupt Status (RXGBPKTIS):** This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status detected.

3.2.189 MMC_TX_INTERRUPT — Offset 708h

This register maintains the interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter).

When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read.

The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 708h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Transmit LPI transition counter interrupt status (TXLPITRCIS):** This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Transmit LPI microsecond counter interrupt status (TXLPIUSCIS):** This bit is set when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Transmit Oversize Good Packet Counter Interrupt Status (TXOSIZEGPIS):** This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status detected.
24	0h RO	**MMC Transmit VLAN Good Packet Counter Interrupt Status (TXVLANGPIS):** This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status detected.
23	0h RO	**MMC Transmit Pause Packet Counter Interrupt Status (TXPAUSPIS):** This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected.
22	0h RO	**MMC Transmit Excessive Deferral Packet Counter Interrupt Status (TXEXDEFPIS):** This bit is set when the txexcessdef counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status detected.
21	0h RO	**MMC Transmit Good Packet Counter Interrupt Status (TXGPKTIS):** This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**MMC Transmit Good Octet Counter Interrupt Status (TXGOCTIS):** This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Octet Counter Interrupt Status detected.
19	0h RO	**MMC Transmit Carrier Error Packet Counter Interrupt Status (TXCARERPIS):** This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Transmit Excessive Collision Packet Counter Interrupt Status (TXEXCOLPIS):** This bit is set when the txexesscol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status detected.
17	0h RO	**MMC Transmit Late Collision Packet Counter Interrupt Status (TXLATCOLPIS):** This bit is set when the txlatecol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status detected.
16	0h RO	**MMC Transmit Deferred Packet Counter Interrupt Status (TXDEFPIS):** This bit is set when the txdeferred counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status detected.
15	0h RO	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Status (TXMCOLGPIS):** This bit is set when the txmulticol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status detected.
14	0h RO	**MMC Transmit Single Collision Good Packet Counter Interrupt Status (TXSCOLGPIS):** This bit is set when the txsinglecol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**MMC Transmit Underflow Error Packet Counter Interrupt Status (TXUFLOWERPIS):** This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status (TXBCGBPIS):** This bit is set when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Status (TXMCGBPIS):** The bit is set when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Status (TXUCGBPIS):** This bit is set when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status detected.
9	0h RO	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (TX1024TMAXOCTGBPIS):** This bit is set when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
8	0h RO	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (TX512T1023OCTGBPIS):** This bit is set when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status (TX256T511OCTGBPIS):** This bit is set when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
6	0h RO	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status (TX128T255OCTGBPIS):** This bit is set when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
5	0h RO	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status (TX65T127OCTGBPIS):** This bit is set when the tx65to127octets_gb counter reaches half the maximum value, and also when it reaches the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
4	0h RO	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status (TX64OCTGBPIS):** This bit is set when the tx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status detected.
3	0h RO	**MMC Transmit Multicast Good Packet Counter Interrupt Status (TXMCGPIS):** This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Transmit Broadcast Good Packet Counter Interrupt Status (TXBCGPIS):** This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status detected.
1	0h RO	**MMC Transmit Good Bad Packet Counter Interrupt Status (TXGBPKTIS):** This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status detected.
0	0h RO	**MMC Transmit Good Bad Octet Counter Interrupt Status (TXGBOCTIS):** This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status detected.

3.2.190 MMC_RX_INTERRUPT_MASK — Offset 70Ch

This register maintains the masks for interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values.

This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Receive LPI transition counter interrupt Mask (RXLPITRCIM):** Setting this bit masks the interrupt when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Receive LPI microsecond counter interrupt Mask (RXLPIUSCIM):** Setting this bit masks the interrupt when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI microsecond counter interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**MMC Receive Control Packet Counter Interrupt Mask (RXCTRLPIM):** Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Control Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Control Packet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive Error Packet Counter Interrupt Mask (RXRCVERRPIM):** Setting this bit masks the interrupt when the rxrcverror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Error Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Receive Watchdog Error Packet Counter Interrupt Mask (RXWDOGPIM):** Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Receive VLAN Good Bad Packet Counter Interrupt Mask (RXVLANGBPIM):** Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive FIFO Overflow Packet Counter Interrupt Mask (RXFOVPIM):** Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Receive Pause Packet Counter Interrupt Mask (RXPAUSPIM):** Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive Out Of Range Error Packet Counter Interrupt Mask (RXORANGEPIM):** Setting this bit masks the interrupt when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive Length Error Packet Counter Interrupt Mask (RXLENERPIM):** Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Length Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Length Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**MMC Receive Unicast Good Packet Counter Interrupt Mask (RXUCGPIM):** Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask. (RX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
15	0h RW	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (RX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (RX256T511OCTGBPIM):** Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (RX128T255OCTGBPIM):** Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.
12	0h RW	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (RX65T127OCTGBPIM):** Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask (RX64OCTGBPIM):** Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**MMC Receive Oversize Good Packet Counter Interrupt Mask (RXOSIZEGPIM):** Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive Undersize Good Packet Counter Interrupt Mask (RXUSIZEGPIM):** Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive Jabber Error Packet Counter Interrupt Mask (RXJABERPIM):** Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive Runt Packet Counter Interrupt Mask (RXRUNTPIM):** Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Runt Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Runt Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive Alignment Error Packet Counter Interrupt Mask (RXALGNERPIM):** Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive CRC Error Packet Counter Interrupt Mask (RXCRCERPIM):** Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Receive Multicast Good Packet Counter Interrupt Mask (RXMCGPIM):** Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Receive Broadcast Good Packet Counter Interrupt Mask (RXBCGPIM):** Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MMC Receive Good Octet Counter Interrupt Mask (RXGOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Octet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive Good Bad Octet Counter Interrupt Mask (RXGBOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive Good Bad Packet Counter Interrupt Mask (RXGBPKTIM):** Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is enabled.

3.2.191 MMC_TX_INTERRUPT_MASK — Offset 710h

This register maintains the masks for interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 710h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Transmit LPI transition counter interrupt Mask (TXLPITRCIM):** Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Transmit LPI microsecond counter interrupt Mask (TXLPIUSCIM):** Setting this bit masks the interrupt when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI microsecond counter interrupt Mask is enabled.
25	0h RW	**MMC Transmit Oversize Good Packet Counter Interrupt Mask (TXOSIZEGPIM):** Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**MMC Transmit VLAN Good Packet Counter Interrupt Mask (TXVLANGPIM):** Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Transmit Pause Packet Counter Interrupt Mask (TXPAUSPIM):** Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Transmit Excessive Deferral Packet Counter Interrupt Mask (TXEXDEFPIM):** Setting this bit masks the interrupt when the txexcessdef counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Transmit Good Packet Counter Interrupt Mask (TXGPKTIM):** Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Packet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Transmit Good Octet Counter Interrupt Mask (TXGOCTIM):** Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Transmit Carrier Error Packet Counter Interrupt Mask (TXCARERPIM):** Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Transmit Excessive Collision Packet Counter Interrupt Mask (TXEXCOLPIM):** Setting this bit masks the interrupt when the txexcesscol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Transmit Late Collision Packet Counter Interrupt Mask (TXLATCOLPIM):** Setting this bit masks the interrupt when the txlatecol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Transmit Deferred Packet Counter Interrupt Mask (TXDEFPIM):** Setting this bit masks the interrupt when the txdeferred counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask (TXMCOLGPIM):** Setting this bit masks the interrupt when the txmulticol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Transmit Single Collision Good Packet Counter Interrupt Mask (TXSCOLGPIM):** Setting this bit masks the interrupt when the txsinglecol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Transmit Underflow Error Packet Counter Interrupt Mask (TXUFLOWERPIM):** Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled.
12	0h RW	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask (TXBCGBPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask (TXMCGBPIM):** Setting this bit masks the interrupt when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask (TXUCGBPIM):** Setting this bit masks the interrupt when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask (TX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (TX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (TX256T511OCTGBPIM):** Setting this bit masks the interrupt when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (TX128T255OCTGBPIM):** Setting this bit masks the interrupt when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (TX65T127OCTGBPIM):** Setting this bit masks the interrupt when the tx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask (TX64OCTGBPIM):** Setting this bit masks the interrupt when the tx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Transmit Multicast Good Packet Counter Interrupt Mask (TXMCGPIM):** Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MMC Transmit Broadcast Good Packet Counter Interrupt Mask (TXBCGPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Transmit Good Bad Packet Counter Interrupt Mask (TXGBPKTIM):** Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Good Bad Octet Counter Interrupt Mask (TXGBOCTIM):** Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled.

3.2.192 TX_OCTET_COUNT_GOOD_BAD — Offset 714h

This register provides the number of bytes transmitted by the GbE Controller, exclusive of preamble and retried bytes, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 714h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good Bad (TXOCTGB):** This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

3.2.193 TX_PACKET_COUNT_GOOD_BAD — Offset 718h

This register provides the number of good and bad packets transmitted by GbE Controller, exclusive of retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 718h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good Bad (TXPKTGB):** This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

3.2.194 TX_BROADCAST_PACKETS_GOOD — Offset 71Ch

This register provides the number of good broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 71Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good (TXBCASTG):** This field indicates the number of good broadcast packets transmitted.

3.2.195 TX_MULTICAST_PACKETS_GOOD — Offset 720h

This register provides the number of good multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 720h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good (TXMCASTG):** This field indicates the number of good multicast packets transmitted.

3.2.196 TX_64OCTETS_PACKETS_GOOD_BAD — Offset 724h

This register provides the number of good and bad packets transmitted by GbE Controller with length 64 bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 724h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 64Octets Packets Good_Bad (TX64OCTGB):** This field indicates the number of good and bad packets transmitted with length 64 bytes, exclusive of preamble and retried packets.

3.2.197 TX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 728h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 728h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TX65_127OCTGB:** Tx 65To127Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

3.2.198 TX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 72Ch

This register provides the number of good and bad packets transmitted by GbE Controller with length between 128 to 255 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 72Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 128To255Octets Packets Good Bad (TX128_255OCTGB):** This field indicates the number of good and bad packets transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried packets.

3.2.199 TX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 730h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 256 to 511 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 730h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 256To511Octets Packets Good Bad (TX256_511OCTGB):** This field indicates the number of good and bad packets transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried packets.

3.2.200 TX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 734h

This register provides the number of good and bad packets transmitted by GbE Controller with length 512 to 1023 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 734h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 512To1023Octets Packets Good Bad (TX512_1023OCTGB):** This field indicates the number of good and bad packets transmitted with length between 512 and 1023 (inclusive) bytes, exclusive of preamble and retried packets.

3.2.201 TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 738h

This register provides the number of good and bad packets transmitted by GbE Controller with length 1024 to maxsize (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 738h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 1024ToMaxOctets Packets Good Bad (TX1024_MAXOCTGB):** This field indicates the number of good and bad packets transmitted with length between 1024 and maxsize (inclusive) bytes, exclusive of preamble and retried packets.

3.2.202 TX_UNICAST_PACKETS_GOOD_BAD — Offset 73Ch

This register provides the number of good and bad unicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 73Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Unicast Packets Good Bad (TXUCASTGB):** This field indicates the number of good and bad unicast packets transmitted.

3.2.203 TX_MULTICAST_PACKETS_GOOD_BAD — Offset 740h

This register provides the number of good and bad multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 740h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good Bad (TXMCASTGB):** This field indicates the number of good and bad multicast packets transmitted.

3.2.204 TX_BROADCAST_PACKETS_GOOD_BAD — Offset 744h

This register provides the number of good and bad broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 744h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good Bad (TXBCASTGB):** This field indicates the number of good and bad broadcast packets transmitted.

3.2.205 TX_UNDERFLOW_ERROR_PACKETS — Offset 748h

This register provides the number of packets aborted by GbE Controller because of packets underflow error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 748h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Underflow Error Packets (TXUNDRFLW):** This field indicates the number of packets aborted because of packets underflow error.

3.2.206 TX_SINGLE_COLLISION_GOOD_PACKETS — Offset 74Ch

This register provides the number of successfully transmitted packets by GbE Controller after a single collision in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Single Collision Good Packets (TXSNGLCOLG):** This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

3.2.207 TX_MULTIPLE_COLLISION_GOOD_PACKETS — Offset 750h

This register provides the number of successfully transmitted packets by GbE Controller after multiple collisions in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 750h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multiple Collision Good Packets (TXMULTCOLG):** This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

3.2.208 TX_DEFERRED_PACKETS — Offset 754h

This register provides the number of successfully transmitted by GbE Controller after a deferral in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 754h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Deferred Packets (TXDEFRD):** This field indicates the number of successfully transmitted after a deferral in the half-duplex mode.

3.2.209 TX_LATE_COLLISION_PACKETS — Offset 758h

This register provides the number of packets aborted by GbE Controller because of late collision error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 758h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Late Collision Packets (TXLATECOL):** This field indicates the number of packets aborted because of late collision error.

3.2.210 TX_EXCESSIVE_COLLISION_PACKETS — Offset 75Ch

This register provides the number of packets aborted by GbE Controller because of excessive (16) collision errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 75Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Collision Packets (TXEXSCOL):** This field indicates the number of packets aborted because of excessive (16) collision errors.

3.2.211 TX_CARRIER_ERROR_PACKETS — Offset 760h

This register provides the number of packets aborted by GbE Controller because of carrier sense error (no carrier or loss of carrier).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 760h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Carrier Error Packets (TXCARR):** This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

3.2.212 TX_OCTET_COUNT_GOOD — Offset 764h

This register provides the number of bytes transmitted by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 764h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good (TXOCTG):** This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

3.2.213 TX_PACKET_COUNT_GOOD — Offset 768h

This register provides the number of good packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 768h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good (TXPKTG):** This field indicates the number of good packets transmitted.

3.2.214 TX_EXCESSIVE_DEFERRAL_ERROR — Offset 76Ch

This register provides the number of packets aborted by GbE Controller because of excessive deferral error (deferred for more than two max-sized packet times).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 76Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Deferral Error (TXEXSDEF):** This field indicates the number of packets aborted because of excessive deferral error (deferred for more than two max-sized packet times).

3.2.215 TX_PAUSE_PACKETS — Offset 770h

This register provides the number of good Pause packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 770h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Pause Packets (TXPAUSE):** This field indicates the number of good Pause packets transmitted.

3.2.216 TX_VLAN_PACKETS_GOOD — Offset 774h

This register provides the number of good VLAN packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 774h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx VLAN Packets Good (TXVLANG):** This field provides the number of good VLAN packets transmitted.

3.2.217 TX_OSIZE_PACKETS_GOOD — Offset 778h

This register provides the number of packets transmitted by GbE Controller without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 778h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx OSize Packets Good (TXOSIZG):** This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

3.2.218 RX_PACKETS_COUNT_GOOD_BAD — Offset 780h

This register provides the number of good and bad packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 780h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packets Count Good Bad (RXPKTGB):** This field indicates the number of good and bad packets received.

3.2.219 RX_OCTET_COUNT_GOOD_BAD — Offset 784h

This register provides the number of bytes received, exclusive of preamble, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 784h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good Bad (RXOCTGB):** This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

3.2.220 RX_OCTET_COUNT_GOOD — Offset 788h

This register provides the number of bytes received by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 788h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good (RXOCTG):** This field indicates the number of bytes received, exclusive of preamble, only in good packets.

3.2.221 RX_BROADCAST_PACKETS_GOOD — Offset 78Ch

This register provides the number of good broadcast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Broadcast Packets Good (RXBCASTG):** This field indicates the number of good broadcast packets received.

3.2.222 RX_MULTICAST_PACKETS_GOOD — Offset 790h

This register provides the number of good multicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 790h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Multicast Packets Good (RXMCASTG):** This field indicates the number of good multicast packets received.

3.2.223 RX_CRC_ERROR_PACKETS — Offset 794h

This register provides the number of packets received by GbE Controller with CRC error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 794h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx CRC Error Packets (RXCRCERR):** This field indicates the number of packets received with CRC error.

3.2.224 RX_ALIGNMENT_ERROR_PACKETS — Offset 798h

This register provides the number of packets received by GbE Controller with alignment (dribble) error. It is valid only in 10/100 mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 798h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Alignment Error Packets (RXALGNERR):** This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode.

3.2.225 RX_RUNT_ERROR_PACKETS — Offset 79Ch

This register provides the number of packets received by GbE Controller with runt (length less than 64 bytes and CRC error) error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 79Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Runt Error Packets (RXRUNTERR):** This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error.

3.2.226 RX_JABBER_ERROR_PACKETS — Offset 7A0h

This register provides the number of giant packets received by GbE Controller with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Jabber Error Packets (RXJABERR):** This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

3.2.227 RX_UNDERSIZE_PACKETS_GOOD — Offset 7A4h

This register provides the number of packets received by GbE Controller with length less than 64 bytes, without any errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Undersize Packets Good (RXUNDERSZG):** This field indicates the number of packets received with length less than 64 bytes, without any errors.

3.2.228 RX_OVERSIZE_PACKETS_GOOD — Offset 7A8h

This register provides the number of packets received by GbE Controller without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Oversize Packets Good (RXOVERSZG):** This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

3.2.229 RX_64OCTETS_PACKETS_GOOD_BAD — Offset 7ACh

This register provides the number of good and bad packets received by GbE Controller with length 64 bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 64 Octets Packets Good Bad (RX64OCTGB):** This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble.

3.2.230 RX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 7B0h

This register provides the number of good and bad packets received by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX65_127OCTGB:** Rx 65-127 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

3.2.231 RX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 7B4h

This register provides the number of good and bad packets received by GbE Controller with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX128_255OCTGB:** Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

3.2.232 RX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 7B8h

This register provides the number of good and bad packets received by GbE ControllerGbE Controller with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX256_511OCTGB:** Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

3.2.233 RX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 7BCh

This register provides the number of good and bad packets received by GbE Controller with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX 512-1023 Octets Packets Good Bad (RX512_1023OCTGB):** This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

3.2.234 RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 7C0h

This register provides the number of good and bad packets received by GbE Controller with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 1024-Max Octets Good Bad (RX1024_MAXOCTGB):** This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

3.2.235 RX_UNICAST_PACKETS_GOOD — Offset 7C4h

This register provides the number of good unicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Unicast Packets Good (RXUCASTG):** This field indicates the number of good unicast packets received.

3.2.236 RX_LENGTH_ERROR_PACKETS — Offset 7C8h

This register provides the number of packets received by GbE Controller with length error (Length Type field not equal to packet size), for all packets with valid length field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Length Error Packets (RXLENERR):** This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

3.2.237 RX_OUT_OF_RANGE_TYPE_PACKETS — Offset 7CCh

This register provides the number of packets received by GbE Controller with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Out of Range Type Packet (RXOUTOFRNG):** This field indicates the number of packets received with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

3.2.238 RX_PAUSE_PACKETS — Offset 7D0h

This register provides the number of good and valid Pause packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Pause Packets (RXPAUSEPKT):** This field indicates the number of good and valid Pause packets received.

3.2.239 RX_FIFO_OVERFLOW_PACKETS — Offset 7D4h

This register provides the number of missed received packets because of FIFO overflow in GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FIFO Overflow Packets (RXFIFOOVFL):** This field indicates the number of missed received packets because of FIFO overflow.

3.2.240 RX_VLAN_PACKETS_GOOD_BAD — Offset 7D8h

This register provides the number of good and bad VLAN packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx VLAN Packets Good Bad (RXVLANPKTGB):** This field indicates the number of good and bad VLAN packets received.

3.2.241 RX_WATCHDOG_ERROR_PACKETS — Offset 7DCh

This register provides the number of packets received by GbE Controller with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Watchdog Error Packets (RXWDGERR):** This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

3.2.242 RX_RECEIVE_ERROR_PACKETS — Offset 7E0h

This register provides the number of packets received by GbE Controller with Receive error or Packet Extension error on the GMII or MII interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Receive Error Packets (RXRCVERR):** This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface.

3.2.243 RX_CONTROL_PACKETS_GOOD — Offset 7E4h

This register provides the number of good control packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Control Packets Good (RXCTRLG):** This field indicates the number of good control packets received.

3.2.244 TX_LPI_USEC_CNTR — Offset 7ECh

This register provides the number of microseconds Tx LPI is asserted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Microseconds Counter (TXLPIUSC):** This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

3.2.245 TX_LPI_TRAN_CNTR — Offset 7F0h

This register provides the number of times GbE Controller has entered Tx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Transition counter (TXLPITRC):** This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments.

3.2.246 RX_LPI_USEC_CNTR — Offset 7F4h

This register provides the number of microseconds Rx LPI is sampled by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Microseconds Counter (RXLPIUSC):** This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

3.2.247 RX_LPI_TRAN_CNTR — Offset 7F8h

This register provides the number of times GbE Controller has entered Rx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Transition counter (RXLPITRC):** This field indicates the number of times Rx LPI Entry has occurred.

3.2.248 MMC_IPC_RX_INTERRUPT_MASK — Offset 800h

This register maintains the mask for the interrupt generated from the receive IPC statistic counters.

The MMC Receive Checksum Off load Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Off load) statistic counters reach half their maximum value, and when they reach their maximum values. This register is 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**MMC Receive ICMP Error Octet Counter Interrupt Mask (RXICMPEROIM):** Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled.
28	0h RW	**MMC Receive ICMP Good Octet Counter Interrupt Mask (RXICMPGOIM):** Setting this bit masks the interrupt when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is enabled.
27	0h RW	**MMC Receive TCP Error Octet Counter Interrupt Mask (RXTCPEROIM):** Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is enabled.
26	0h RW	**MMC Receive TCP Good Octet Counter Interrupt Mask (RXTCPGOIM):** Setting this bit masks the interrupt when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is enabled.
25	0h RW	**MMC Receive UDP Good Octet Counter Interrupt Mask (RXUDPEROIM):** Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive IPV6 No Payload Octet Counter Interrupt Mask (RXUDPGOIM):** Setting this bit masks the interrupt when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**MMC Receive IPV6 Header Error Octet Counter Interrupt Mask (RXIPV6NOPAYOIM):** Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6HEROIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6GOIM):** Setting this bit masks the interrupt when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask (RXIPV4UDSBLOIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask (RXIPV4FRAGOIM):** Setting this bit masks the interrupt when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive IPV4 No Payload Octet Counter Interrupt Mask (RXIPV4NOPAYOIM):** Setting this bit masks the interrupt when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Receive IPV4 Header Error Octet Counter Interrupt Mask (RXIPV4HEROIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive IPV4 Good Octet Counter Interrupt Mask (RXIPV4GOIM):** Setting this bit masks the interrupt when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is enabled.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**MMC Receive ICMP Error Packet Counter Interrupt Mask (RXICMPERPIM):** Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled.
12	0h RW	**MMC Receive ICMP Good Packet Counter Interrupt Mask (RXICMPGPIM):** Setting this bit masks the interrupt when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive TCP Error Packet Counter Interrupt Mask (RXTCPERPIM):** Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Receive TCP Good Packet Counter Interrupt Mask (RXTCPGPIM):** Setting this bit masks the interrupt when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive UDP Error Packet Counter Interrupt Mask (RXUDPERPIM):** Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive UDP Good Packet Counter Interrupt Mask (RXUDPGPIM):** Setting this bit masks the interrupt when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive IPV6 No Payload Packet Counter Interrupt Mask (RXIPV6NOPAYPIM):** Setting this bit masks the interrupt when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive IPV6 Header Error Packet Counter Interrupt Mask (RXIPV6HERPIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive IPV6 Good Packet Counter Interrupt Mask (RXIPV6GPIM):** Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask (RXIPV4UDSBLPIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask (RXIPV4FRAGPIM):** Setting this bit masks the interrupt when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Receive IPV4 No Payload Packet Counter Interrupt Mask (RXIPV4NOPAYPIM):** Setting this bit masks the interrupt when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive IPV4 Header Error Packet Counter Interrupt Mask (RXIPV4HERPIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive IPV4 Good Packet Counter Interrupt Mask (RXIPV4GPIM):** Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled.

3.2.249 MMC_IPC_RX_INTERRUPT — Offset 808h

This register maintains the interrupt that the receive IPC statistic counters generate.

The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits[7:0]) must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RO	**MMC Receive ICMP Error Octet Counter Interrupt Status (RXICMPEROIS):** This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status detected.
28	0h RO	**MMC Receive ICMP Good Octet Counter Interrupt Status (RXICMPGOIS):** This bit is set when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status detected.
27	0h RO	**MMC Receive TCP Error Octet Counter Interrupt Status (RXTCPEROIS):** This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status detected.
26	0h RO	**MMC Receive TCP Good Octet Counter Interrupt Status (RXTCPGOIS):** This bit is set when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status detected.
25	0h RO	**MMC Receive UDP Error Octet Counter Interrupt Status (RXUDPEROIS):** This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status detected.
24	0h RO	**MMC Receive UDP Good Octet Counter Interrupt Status (RXUDPGOIS):** This bit is set when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**MMC Receive IPV6 No Payload Octet Counter Interrupt Status (RXIPV6NOPAYOIS):** This bit is set when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status detected.
22	0h RO	**MMC Receive IPV6 Header Error Octet Counter Interrupt Status (RXIPV6HEROIS):** This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected.
21	0h RO	**MMC Receive IPV6 Good Octet Counter Interrupt Status (RXIPV6GOIS):** This bit is set when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status detected.
20	0h RO	**RXIPV4UDSBLOIS:** MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status This bit is set when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status detected.
19	0h RO	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Status (RXIPV4FRAGOIS):** This bit is set when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status detected.
18	0h RO	**MMC Receive IPV4 No Payload Octet Counter Interrupt Status (RXIPV4NOPAYOIS):** This bit is set when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**MMC Receive IPV4 Header Error Octet Counter Interrupt Status (RXIPV4HEROIS):** This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected.
16	0h RO	**MMC Receive IPV4 Good Octet Counter Interrupt Status (RXIPV4GOIS):** This bit is set when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status detected.
15:14	0h RO	**Reserved**
13	0h RO	**MMC Receive ICMP Error Packet Counter Interrupt Status (RXICMPERPIS):** This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive ICMP Good Packet Counter Interrupt Status (RXICMPGPIS):** This bit is set when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive TCP Error Packet Counter Interrupt Status (RXTCPERPIS):** This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive TCP Good Packet Counter Interrupt Status (RXTCPGPIS):** This bit is set when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive UDP Error Packet Counter Interrupt Status (RXUDPERPIS):** This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MC Receive UDP Good Packet Counter Interrupt Status (RXUDPGPIS):** This bit is set when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status detected.
7	0h RO	**MMC Receive IPV6 No Payload Packet Counter Interrupt Status (RXIPV6NOPAYPIS):** This bit is set when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive IPV6 Header Error Packet Counter Interrupt Status (RXIPV6HERPIS):** This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive IPV6 Good Packet Counter Interrupt Status (RXIPV6GPIS):** This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status (RXIPV4UDSBLPIS):** This bit is set when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Status (RXIPV4FRAGPIS):** This bit is set when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive IPV4 No Payload Packet Counter Interrupt Status (RXIPV4NOPAYPIS):** This bit is set when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status detected.
1	0h RO	**MMC Receive IPV4 Header Error Packet Counter Interrupt Status (RXIPV4HERPIS):** This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected.
0	0h RO	**MMC Receive IPV4 Good Packet Counter Interrupt Status (RXIPV4GPIS):** This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status detected.

3.2.250 RXIPV4_GOOD_PACKETS — Offset 810h

This register provides the number of good IPv4 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Packets (RXIPV4GDPKT):** This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

3.2.251 RXIPV4_HEADER_ERROR_PACKETS — Offset 814h

RxIPv4 Header Error Packets

This register provides the number of IPv4 datagrams received by GbE Controller with header (checksum, length, or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Packets (RXIPV4HDRERRPKT):** This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

3.2.252 RXIPV4_NO_PAYLOAD_PACKETS — Offset 818h

This register provides the number of IPv4 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Packets (RXIPV4NOPAYPKT):** This field indicates the number of IPv4 datagram packets received that did not have a TCP, UDP, or ICMP payload.

3.2.253 RXIPV4_FRAGMENTED_PACKETS — Offset 81Ch

This register provides the number of good IPv4 datagrams received by GbE Controller with fragmentation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Packets (RXIPV4FRAGPKT):** This field indicates the number of good IPv4 datagrams received with fragmentation.

3.2.254 RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS — Offset 820h

This register provides the number of good IPv4 datagrams received by GbE Controller that had a UDP payload with checksum disabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disabled Packets (RXIPV4UDSBLPKT):** This field indicates the number of good IPv4 datagrams received that had a UDP payload with checksum disabled.

3.2.255 RXIPV6_GOOD_PACKETS — Offset 824h

This register provides the number of good IPv6 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 824h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Packets (RXIPV6GDPKT):** This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

3.2.256 RXIPV6_HEADER_ERROR_PACKETS — Offset 828h

This register provides the number of IPv6 datagrams received by GbE Controller with header (length or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Packets (RXIPV6HDRERRPKT):** This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

3.2.257 RXIPV6_NO_PAYLOAD_PACKETS — Offset 82Ch

This register provides the number of IPv6 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 82Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Packets (RXIPV6NOPAYPKT):** This field indicates the number of IPv6 datagram packets received that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

3.2.258 RXUDP_GOOD_PACKETS — Offset 830h

This register provides the number of good IP datagrams received by GbE Controller with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Packets (RXUDPGDPKT):** This field indicates the number of good IP datagrams received with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

3.2.259 RXUDP_ERROR_PACKETS — Offset 834h

This register provides the number of good IP datagrams received by GbE Controller whose UDP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Packets (RXUDPERRPKT):** This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

3.2.260 RXTCP_GOOD_PACKETS — Offset 838h

This register provides the number of good IP datagrams received by GbE Controller with a good TCP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Packets (RXTCPGDPKT):** This field indicates the number of good IP datagrams received with a good TCP payload.

3.2.261 RXTCP_ERROR_PACKETS — Offset 83Ch

This register provides the number of good IP datagrams received by GbE Controller whose TCP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Packets (RXTCPERRPKT):** This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

3.2.262 RXICMP_GOOD_PACKETS — Offset 840h

This register provides the number of good IP datagrams received by GbE Controller with a good ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Packets (RXICMPGDPKT):** This field indicates the number of good IP datagrams received with a good ICMP payload.

3.2.263 RXICMP_ERROR_PACKETS — Offset 844h

This register provides the number of good IP datagrams received by GbE Controller whose ICMP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Packets (RXICMPERRPKT):** This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

3.2.264 RXIPV4_GOOD_OCTETS — Offset 850h

This register provides the number of bytes received by GbE Controller in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Octets (RXIPV4GDOCT):** This field indicates the number of bytes received in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.265 RXIPV4_HEADER_ERROR_OCTETS — Offset 854h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 854h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Octets (RXIPV4HDRERROCT):** This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.266 RXIPV4_NO_PAYLOAD_OCTETS — Offset 858h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 858h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Octets (RXIPV4NOPAYOCT):** This field indicates the number of bytes received in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.267 RXIPV4_FRAGMENTED_OCTETS — Offset 85Ch

This register provides the number of bytes received by GbE Controller in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 85Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Octets (RXIPV4FRAGOCT):** This field indicates the number of bytes received in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.268 RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS — Offset 860h

This register provides the number of bytes received by GbE Controller in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 860h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disable Octets (RXIPV4UDSBLOCT):** This field indicates the number of bytes received in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.269 RXIPV6_GOOD_OCTETS — Offset 864h

This register provides the number of bytes received by GbE Controller in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 864h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Octets (RXIPV6GDOCT):** This field indicates the number of bytes received in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.270 RXIPV6_HEADER_ERROR_OCTETS — Offset 868h

This register provides the number of bytes received by GbE Controller in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 868h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Octets (RXIPV6HDRERROCT):** This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.271 RXIPV6_NO_PAYLOAD_OCTETS — Offset 86Ch

This register provides the number of bytes received by GbE Controller in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 86Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Octets (RXIPV6NOPAYOCT):** This field indicates the number of bytes received in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

3.2.272 RXUDP_GOOD_OCTETS — Offset 870h

This register provides the number of bytes received by GbE Controller in a good UDP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 870h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Octets (RXUDPGDOCT):** This field indicates the number of bytes received in a good UDP segment. This counter does not count IP header bytes.

3.2.273 RXUDP_ERROR_OCTETS — Offset 874h

This register provides the number of bytes received by GbE Controller in a UDP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 874h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Octets (RXUDPERROCT):** This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

3.2.274 RXTCP_GOOD_OCTETS — Offset 878h

This register provides the number of bytes received by GbE Controller in a good TCP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 878h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Octets (RXTCPGDOCT):** This field indicates the number of bytes received in a good TCP segment. This counter does not count IP header bytes.

3.2.275 RXTCP_ERROR_OCTETS — Offset 87Ch

This register provides the number of bytes received by GbE Controller in a TCP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 87Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Octets (RXTCPERROCT):** This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

3.2.276 RXICMP_GOOD_OCTETS — Offset 880h

This register provides the number of bytes received by GbE Controller in a good ICMP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 880h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Octets (RXICMPGDOCT):** This field indicates the number of bytes received in a good ICMP segment. This counter does not count IP header bytes.

3.2.277 RXICMP_ERROR_OCTETS — Offset 884h

This register provides the number of bytes received by GbE Controller in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 884h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Octets (RXICMPERROCT):** This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

3.2.278 MMC_FPE_TX_INTERRUPT — Offset 8A0h

This register maintains the interrupts generated from all FPE related Transmit statistics counters. The MMC FPE Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MMC Tx Hold Request Counter Interrupt Status (HRCIS):** This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected.
0	0h RO	**MMC Tx FPE Fragment Counter Interrupt status (FCIS):** This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected. 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected.

3.2.279 MMC_FPE_TX_INTERRUPT_MASK — Offset 8A4h

This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**MMC Transmit Hold Request Counter Interrupt Mask (HRCIM):** Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled.

3.2.280 MMC_TX_FPE_FRAGMENT_CNTR — Offset 8A8h

This register provides the number of additional mPackets transmitted due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx FPE Fragment counter (TXFFC):** This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

3.2.281 MMC_TX_HOLD_REQ_CNTR — Offset 8ACh

This register provides the count of number of times a hold request is given to MAC

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Hold Request Counter (TXHRC):** This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

3.2.282 MMC_FPE_RX_INTERRUPT — Offset 8C0h

This register maintains the interrupts generated from all FPE related Receive statistics counters. The MMC FPE Receive Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**MMC Rx FPE Fragment Counter Interrupt Status (FCIS):** This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Rx Packet Assembly OK Counter Interrupt Status (PAOCIS):** This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected.
1	0h RO	**MMC Rx Packet SMD Error Counter Interrupt Status (PSECIS):** This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected.
0	0h RO	**MMC Rx Packet Assembly Error Counter Interrupt Status (PAECIS):** This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected.

3.2.283 MMC_FPE_RX_INTERRUPT_MASK — Offset 8C4h

This register maintains the masks for interrupts generated from all FPE related Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**MMC Rx FPE Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled.
2	0h RW	**MMC Rx Packet Assembly OK Counter Interrupt Mask (PAOCIM):** Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled.
1	0h RW	**MMC Rx Packet SMD Error Counter Interrupt Mask (PSECIM):** Setting this bit masks the interrupt when the R Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled.
0	0h RW	**MMC Rx Packet Assembly Error Counter Interrupt Mask (PAECIM):** Setting this bit masks the interrupt when the R Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled.

3.2.284 MMC_RX_PACKET_ASSEMBLY_ERR_CNTR — Offset 8C8h

This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly Error Counter (PAEC):** This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

3.2.285 MMC_RX_PACKET_SMD_ERR_CNTR — Offset 8CCh

This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet SMD Error Counter (PSEC):** This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

3.2.286 MMC_RX_PACKET_ASSEMBLY_OK_CNTR — Offset 8D0h

This register provides the number of MAC frames that were successfully reassembled and delivered to MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly OK Counter (PAOC):** This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

3.2.287 MMC_RX_FPE_FRAGMENT_CNTR — Offset 8D4h

This register provides the number of additional mPackets received due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FPE Fragment Counter (FFC):** This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

3.2.288 MAC_L3_L4_CONTROL0 — Offset 900h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 900h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN0):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**
26:24	0h RW	**DMA Channel Number (DMCHN0):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM0):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM0):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Layer 4 Protocol Enable (L4PEN0):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	**L3HDBM0:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM0:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN0):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

3.2.289 MAC_LAYER4_ADDRESS0 — Offset 904h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core.

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 904h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP0):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP0):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

3.2.290 MAC_LAYER3_ADDR0_REG0 — Offset 910h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 910h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A00):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

3.2.291 MAC_LAYER3_ADDR1_REG0 — Offset 914h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 914h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A10):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

3.2.292 MAC_LAYER3_ADDR2_REG0 — Offset 918h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 918h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A20):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

3.2.293 MAC_LAYER3_ADDR3_REG0 — Offset 91Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 91Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A30):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

3.2.294 MAC_L3_L4_CONTROL1 — Offset 930h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 930h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN1):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**
26:24	0h RW	**DMA Channel Number (DMCHN1):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM1):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM1):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	**Reserved**
16	0h RW	**Layer 4 Protocol Enable (L4PEN1):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	**L3HDBM1:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.

Bit Range	Default & Access	Field Name (ID): Description
10:6	00h RW	**L3HSBM1:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN1):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

3.2.295 MAC_LAYER4_ADDRESS1 — Offset 934h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core.

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 934h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP1):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP1):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

3.2.296 MAC_LAYER3_ADDR0_REG1 — Offset 940h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 940h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A01):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

3.2.297 MAC_LAYER3_ADDR1_REG1 — Offset 944h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 944h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A11):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

3.2.298 MAC_LAYER3_ADDR2_REG1 — Offset 948h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 948h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A21):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

3.2.299 MAC_LAYER3_ADDR3_REG1 — Offset 94Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A31):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

3.2.300 MAC_TIMESTAMP_CONTROL — Offset B00h

This register controls the operation of the System Time generator and processing of PTP packets for time stamping in the Receiver.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**AV 802.1AS Mode Enable (AV8021ASMEN):** When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. 0x0 (DISABLE): AV 802.1AS Mode is disabled. 0x1 (ENABLE): AV 802.1AS Mode is enabled.
27:25	0h RO	**Reserved**
24	0h RW	**Transmit Timestamp Status Mode (TXTSSTSM):** When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. 0x0 (DISABLE): Transmit Timestamp Status Mode is disabled. 0x1 (ENABLE): Transmit Timestamp Status Mode is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**External System Time Input (ESTI):** When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: - To take the timestamp provided as status - To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time. 0x0 (DISABLE): External System Time Input is disabled. 0x1 (ENABLE): External System Time Input is enabled.
19	0h RW	**Enable checksum correction during OST for PTP over UDP/IPv4 packets (CSC):** When this bit is set, the last two bytes of PTP message sent over UDP/IPv4 is updated to keep the UDP checksum correct, for changes made to origin timestamp and/or correction field as part of one step timestamp operation. The application shall form the packet with these two dummy bytes. When reset, no updates are done to keep the UDP checksum correct. The application shall form the packet with UDP checksum set to 0. 0x0 (DISABLE): checksum correction during OST for PTP over UDP/IPv4 packets is disabled. 0x1 (ENABLE): checksum correction during OST for PTP over UDP/IPv4 packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Enable MAC Address for PTP Packet Filtering (TSENMACADDR):** When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. 0x0 (DISABLE): MAC Address for PTP Packet Filtering is disabled. 0x1 (ENABLE): MAC Address for PTP Packet Filtering is enabled.
17:16	0h RW	**Select PTP packets for Taking Snapshots (SNAPTYPSEL):** These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	0h RW	**Enable Snapshot for Messages Relevant to Master (TSMSTRENA):** When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. 0x0 (DISABLE): Snapshot for Messages Relevant to Master is disabled. 0x1 (ENABLE): Snapshot for Messages Relevant to Master is enabled.
14	0h RW	**Enable Timestamp Snapshot for Event Messages (TSEVNTENA):** When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. 0x0 (DISABLE): Timestamp Snapshot for Event Messages is disabled. 0x1 (ENABLE): Timestamp Snapshot for Event Messages is enabled.
13	1h RW	**Enable Processing of PTP Packets Sent over IPv4-UDP (TSIPV4ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv4-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv4-UDP is enabled.
12	0h RW	**Enable Processing of PTP Packets Sent over IPv6-UDP (TSIPV6ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv6-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv6-UDP is enabled.
11	0h RW	**Enable Processing of PTP over Ethernet Packets (TSIPENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. 0x0 (DISABLE): Processing of PTP over Ethernet Packets is disabled. 0x1 (ENABLE): Processing of PTP over Ethernet Packets is enabled.
10	0h RW	**Enable PTP Packet Processing for Version 2 Format (TSVER2ENA):** When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. 0x0 (DISABLE): PTP Packet Processing for Version 2 Format is disabled. 0x1 (ENABLE): PTP Packet Processing for Version 2 Format is enabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Timestamp Digital or Binary Rollover Control (TSCTRLSSR):** When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. 0x0 (DISABLE): Timestamp Digital or Binary Rollover Control is disabled. 0x1 (ENABLE): Timestamp Digital or Binary Rollover Control is enabled.
8	0h RW	**Enable Timestamp for All Packets (TSENALL):** When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. 0x0 (DISABLE): Timestamp for All Packets disabled. 0x1 (ENABLE): Timestamp for All Packets enabled.
7	0h RO	**Reserved**
6	0h RW	**Presentation Time Generation Enable (PTGE):** When this bit is set the Presentation Time generation is enabled. 0x0 (DISABLE): Presentation Time Generation is disabled. 0x1 (ENABLE): Presentation Time Generation is enabled.
5	0h RW	**Update Addend Register (TSADDREG):** When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Addend Register is not updated. 0x1 (ENABLE): Addend Register is updated.
4	0h RO	**Reserved**
3	0h RW	**Update Timestamp (TSUPDT):** When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not updated. 0x1 (ENABLE): Timestamp is updated.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Initialize Timestamp (TSINIT):** When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not initialized. 0x1 (ENABLE): Timestamp is initialized.
1	0h RW	**Fine or Coarse Timestamp Update (TSCFUPDT):** When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. 0x0 (COARSE): Coarse method is used to update system timestamp. 0x1 (FINE): Fine method is used to update system timestamp.
0	0h RW	**Enable Timestamp (TSENA):** When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. 0x0 (DISABLE): Timestamp is disabled. 0x1 (ENABLE): Timestamp is enabled.

3.2.301 MAC_SUB_SECOND_INCREMENT — Offset B04h

This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**Sub-second Increment Value (SSINC):** The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:8	00h RW	**Sub-nanosecond Increment Value (SNSINC):** This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C.
7:0	0h RO	**Reserved**

3.2.302 MAC_SYSTEM_TIME_SECONDS — Offset B08h

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Timestamp Second (TSS):** The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

3.2.303 MAC_SYSTEM_TIME_NANOSECONDS — Offset B0Ch

The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Timestamp Sub Seconds (TSSS):** The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

3.2.304 MAC_SYSTEM_TIME_SECONDS_UPDATE — Offset B10h

The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both registers before setting the TSINIT or TSUPDT bits in MAC_Timestamp_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Seconds (TSS):** The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

3.2.305 MAC_SYSTEM_TIME_NANOSECONDS_UPDATE — Offset B14h

MAC System Time Nanoseconds Update register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Add or Subtract Time (ADDSUB):** When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. 0x0 (ADD): Add time. 0x1 (SUB): Subtract time.
30:0	00000000h RW	**Timestamp Sub Seconds (TSSS):** The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

3.2.306 MAC_TIMESTAMP_ADDEND — Offset B18h

Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register). The content of this register is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Addend Register (TSAR):** This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

3.2.307 MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS — Offset B1Ch

System Time - Higher Word Seconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Timestamp Higher Word Register (TSHWR):** This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.

3.2.308 MAC_TIMESTAMP_STATUS — Offset B20h

Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Number of Auxiliary Timestamp Snapshots (ATSNS):** This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	0h RO	**Auxiliary Timestamp Snapshot Trigger Missed (ATSSTM):** This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. 0x0 (INACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status detected.
23:20	0h RO	**Reserved**
19:16	0h RO	**Auxiliary Timestamp Snapshot Trigger Identifier (ATSSTN):** These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: - Bit 16: Auxiliary trigger 0 - Bit 17: Auxiliary trigger 1 - Bit 18: Auxiliary trigger 2 - Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Tx Timestamp Status Interrupt Status (TXTSSIS):** In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Tx Timestamp Status Interrupt status not detected. 0x1 (ACTIVE): Tx Timestamp Status Interrupt status detected.
14:6	0h RO	**Reserved**
5	0h RO	**Timestamp Target Time Error (TSTRGTERR1):** This bit is set when the latest target time programmed in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.
4	0h RO	**Timestamp Target Time Reached for Target Time PPS1 (TSTARGT1):** When this bit is set and MCGREN1 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN1 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[1] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
3	0h RO	**Timestamp Target Time Error (TSTRGTERR0):** This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Auxiliary Timestamp Trigger Snapshot (AUXTSTRIG):** This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Auxiliary Timestamp Trigger Snapshot status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Trigger Snapshot status detected.
1	0h RO	**Timestamp Target Time Reached (TSTARGT0):** When this bit is set and MCGREN0 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN0 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[0] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
0	0h RO	**Timestamp Seconds Overflow (TSSOVF):** When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Seconds Overflow status not detected. 0x1 (ACTIVE): Timestamp Seconds Overflow status detected.

3.2.309 MAC_TX_TIMESTAMP_STATUS_NANOSECONDS — Offset B30h

This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled.

The MAC_Tx_Timestamp_Status_Nanoseconds register, along with MAC_Tx_Timestamp_Status_Seconds, gives the 64-bit timestamp captured for the PTP packet successfully transmitted by the MAC. This value is considered to be read by the application when the last byte (bits [31:24]) of MAC_Tx_Timestamp_Status_Nanoseconds is read.

If the application does not read these registers and timestamp of another packet is captured, then either the current timestamp is lost (overwritten) or the new timestamp is lost (dropped), depending on the setting of the TXTSSTSM bit of the MAC_Timestamp_Control register. The status bit TXTSC bit [15] in MAC_Timestamp_Status register is set whenever the MAC transmitter captures the timestamp.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Transmit Timestamp Status Missed (TXTSSMIS):** When this bit is set, it indicates one of the following: - The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset - The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Transmit Timestamp Status Missed status not detected. 0x1 (ACTIVE): Transmit Timestamp Status Missed status detected.
30:0	00000000h RO	**Transmit Timestamp Status Low (TXTSSLO):** This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

3.2.310 MAC_TX_TIMESTAMP_STATUS_SECONDS — Offset B34h

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmit Timestamp Status High (TXTSSHI):** This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

3.2.311 MAC_AUXILIARY_CONTROL — Offset B40h

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Auxiliary Snapshot 1 Enable (ATSEN1):** This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
4	0h RW	**Auxiliary Snapshot 0 Enable (ATSEN0):** This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Auxiliary Snapshot FIFO Clear (ATSFC):** When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Auxiliary Snapshot FIFO Clear is disabled. 0x1 (ENABLE): Auxiliary Snapshot FIFO Clear is enabled.

3.2.312 MAC_AUXILIARY_TIMESTAMP_NANOSECONDS — Offset B48h

The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected while configuring the core.

You can store multiple snapshots in this FIFO. Bits[29:25] in MAC_Timestamp_Status indicate the fill-level of the FIFO. The top of the FIFO is removed only when the last byte (bits [31:24]) of MAC_Auxiliary_Timestamp_Seconds register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Auxiliary Timestamp (AUXTSLO):** Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

3.2.313 MAC_AUXILIARY_TIMESTAMP_SECONDS — Offset B4Ch

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Auxiliary Timestamp (AUXTSHI):** Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

3.2.314 MAC_TIMESTAMP_INGRESS_ASYM_CORR — Offset B50h

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Ingress Asymmetry Correction (OSTIAC):** This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

3.2.315 MAC_TIMESTAMP_EGRESS_ASYM_CORR — Offset B54h

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Egress Asymmetry Correction (OSTEAC):** This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000(2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216).

3.2.316 MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND — Offset B58h

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Ingress Correction (TSIC):** This field contains the ingress path correction value as defined by the Ingress Correction expression.

3.2.317 MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND — Offset B5Ch

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Egress Correction (TSEC):** This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

3.2.318 MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC — Offset B60h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for ingress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Ingress Correction, sub-nanoseconds (TSICSNS):** This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression.
7:0	0h RO	**Reserved**

3.2.319 MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC — Offset B64h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for egress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Egress Correction, sub-nanoseconds (TSECSNS):** This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression.
7:0	0h RO	**Reserved**

3.2.320 MAC_TIMESTAMP_INGRESS_LATENCY — Offset B68h

This register holds the Ingress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Ingress Timestamp Latency, in sub-nanoseconds (ITLNS):** This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	00h RO	**Ingress Timestamp Latency, in nanoseconds (ITLSNS):** This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	0h RO	**Reserved**

3.2.321 MAC_TIMESTAMP_EGRESS_LATENCY — Offset B6Ch

This register holds the Egress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Egress Timestamp Latency, in nanoseconds (ETLNS):** This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	00h RO	**Egress Timestamp Latency, in sub-nanoseconds (ETLSNS):** This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	0h RO	**Reserved**

3.2.322 MAC_PPS_CONTROL — Offset B70h

PPS Control register.

Bits[30:24] of this register are valid only when four Flexible PPS outputs are selected.
Bits[22:16] are valid only when three or more Flexible PPS outputs are selected.
Bits[14:8] are valid only when two or more Flexible PPS outputs are selected.
Bits[6:4] are valid only when Flexible PPS feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Time Select (TRGTMODSEL1):** When set, 64-bit PTP time is used to capture time at MCGR trigger[0] input. When reset, presentation time is used to capture time at trigger input, maintaining backward compatibility.
27:16	0h RO	**Reserved**
15	0h RW	**MCGR Mode Enable for PPS1 Output (MCGREN1):** This field enables the 1st PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (DISABLE): 1st PPS instance is disabled to operate in PPS or MCGR mode. 0x1 (ENABLE): 1st PPS instance is enabled to operate in PPS or MCGR mode.
14:13	0h RW	**Target Time Register Mode for PPS1 Output (TIMESEL):** This field indicates the Target Time registers (MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds) mode for PPS1 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT1 (MAC_Timestamp_Status[4]). 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
12	0h RO	**Reserved**
11:8	0h RW	**Flexible PPS1 Output Control (PPSCMD1):** This field controls the flexible PPS1 output signal. This field is similar to the PPSCMD0 field. If MCGREN1 is set, then PPSCMD1 indicated by these 4 bits [11:8] are taken as Presentation Time Control bits for media clock generation and recovery for comparator instance 1. This field is similar to the PPSCMD0 Presentation Time Control bits. If MCGREN1 is not set then only 3 bits from [10:8] is used as PPSCMD1 and the 4th bit is to be set as 0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
7	0h RW	**MCGR Mode Enable for PPS0 Output (MCGREN0):** This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode. 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Target Time Register Mode for PPS0 Output (TRGTMODSEL0):** Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT0 (MAC_Timestamp_Status[1]) 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
4	0h RW	**Flexible PPS Output Mode Enable (PPSEN0):** When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). 0x0 (DISABLE): Flexible PPS Output Mode is disabled. 0x1 (ENABLE): Flexible PPS Output Mode is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**PPS Output Frequency Control (PPSCTRL_PPSCMD):** This field controls the frequency of the PPS0 output signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: - 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. - 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. - 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. - 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. - .. - 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output signal has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: - When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms - When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) - When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high) This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. or Flexible PPS Output Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: - 0000: No Command - 0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. - 0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. - 0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. - 0100: STOP Pulse train at time This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. - 0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). - 110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. - 0111-1111: Reserved or Presentation Time Control If MCGREN0 is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: - 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed - 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0100-1000: Reserved - 1001: Toggle output on compare - 1010: Pulse output low on compare for one PTP-clock cycle - 1011: Pulse output high on compare for one PTP-clock cycle - 1100-1111: Reserved

3.2.323 MAC_PPS0_TARGET_TIME_SECONDS — Offset B80h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH0):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

3.2.324 MAC_PPS0_TARGET_TIME_NANOSECONDS — Offset B84h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY0):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL0):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

3.2.325 MAC_PPS0_INTERVAL — Offset B88h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT0):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

3.2.326 MAC_PPS0_WIDTH — Offset B8Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH0):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

3.2.327 MAC_PPS1_TARGET_TIME_SECONDS — Offset B90h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH1):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

3.2.328 MAC_PPS1_TARGET_TIME_NANOSECONDS — Offset B94h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY1):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL1):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

3.2.329 MAC_PPS1_INTERVAL — Offset B98h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT1):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

3.2.330 MAC_PPS1_WIDTH — Offset B9Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH1):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

3.2.331 MAC_PTO_CONTROL — Offset BC0h

This register controls the PTP Offload Engine operation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Domain Number (DN):** This field indicates the domain Number in which the PTP node is operating.
7	0h RW	**Disable Peer Delay Response response generation (PDRDIS):** When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not be generated for received Peer Delay Request (Pdelay_Req) request packet, as required by the programmed mode. Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in Hardware and/or Pdelay_Resp generation is handled by Software. 0x0 (ENABLE): Peer Delay Response response generation is enabled. 0x1 (DISABLE): Peer Delay Response response generation is disabled.
6	0h RW	**Disable PTO Delay Request/Response response generation (DRRDIS):** When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode. 0x0 (ENABLE): PTO Delay Request/Response response generation is enabled. 0x1 (DISABLE): PTO Delay Request/Response response generation is disabled.
5	0h RW	**Automatic PTP Pdelay_Req message Trigger (APDREQTRIG):** When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP Pdelay_Req message Trigger is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message Trigger is enabled.
4	0h RW	**Automatic PTP SYNC message Trigger (ASYNCTRIG):** When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP SYNC message Trigger is disabled. 0x1 (ENABLE): Automatic PTP SYNC message Trigger is enabled.
3	0h RO	**Reserved**
2	0h RW	**Automatic PTP Pdelay_Req message Enable (APDREQEN):** When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode. 0x0 (DISABLE): Automatic PTP Pdelay_Req message is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message is enabled.
1	0h RW	**Automatic PTP SYNC message Enable (ASYNCEN):** When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Master mode. 0x0 (DISABLE): Automatic PTP SYNC message is disabled. 0x1 (ENABLE): Automatic PTP SYNC message is enabled.
0	0h RW	**PTP Offload Enable (PTOEN):** When this bit is set, the PTP Offload feature is enabled. 0x0 (DISABLE): PTP Offload feature is disabled. 0x1 (ENABLE): PTP Offload feature is enabled.

3.2.332 MAC_SOURCE_PORT_IDENTITY0 — Offset BC4h

This register contains Bits[31:0] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 0 (SPI0):** This field indicates bits [31:0] of sourcePortIdentity of PTP node.

3.2.333 MAC_SOURCE_PORT_IDENTITY1 — Offset BC8h

This register contains Bits[63:32] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 1 (SPI1):** This field indicates bits [63:32] of sourcePortIdentity of PTP node.

3.2.334 MAC_SOURCE_PORT_IDENTITY2 — Offset BCCh

This register contains Bits[79:64] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Source Port Identity 2 (SPI2):** This field indicates bits [79:64] of sourcePortIdentity of PTP node.

3.2.335 MAC_LOG_MESSAGE_INTERVAL — Offset BD0h

This register contains the periodic intervals for automatic PTP packet generation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Log Min Pdelay_Req Interval (LMPDRI):** This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15.Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	0h RO	**Reserved**
10:8	0h RW	**DRSYNCR:** Delay_Req to SYNC Ratio In Slave mode, it is used for controlling frequency of Delay_Req messages transmitted. - 0: DelayReq generated for every received SYNC - 1: DelayReq generated every alternate reception of SYNC - 2: for every 4 SYNC messages - 3: for every 8 SYNC messages - 4: for every 16 SYNC messages - 5: for every 32 SYNC messages - 6-7: Reserved The master sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the slave. The GbE Controller Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Slave mode, the host must not write/update this register unless it has to override the received value. In Master mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. 0x0 (SYNC1): DelayReq generated for every received SYNC. 0x1 (SYNC2): DelayReq generated every alternate reception of SYNC. 0x2 (SYNC4): for every 4 SYNC messages. 0x3 (SYNC8): for every 8 SYNC messages. 0x4 (SYNC16): for every 16 SYNC messages. 0x5 (SYNC32): for every 32 SYNC messages. 0x6 (RSVD): Reserved.
7:0	00h RW	**LSI:** Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Master. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.

3.2.336 MTL_OPERATION_MODE — Offset C00h

The Operation Mode register establishes the Transmit and Receive operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Flexible Rx parser Enable (FRPE):** When this bit is set to 1, the Programmable Rx Parser functionality is enabled. When the Rx parser is disabled and if the Rx parser is in the middle of the parsing then it gets disabled only after completing the current packet parsing. When the Rx parser is enabled from disabled state then the Rx parser gets activated for the next immediate packet. 0x0 (DISABLE): Flexible Rx parser is disabled. 0x1 (ENABLE): Flexible Rx parser is enabled.
14	0h RW	**RxParser Software Error/Incomplete Parsing Packet Drop Enable (RXPED):** When set to 0, packets encountering software programming errors (NPE/NVE/frame offset overflow errors) or incomplete parsing are forwarded to application with the corresponding RxParser status. When set to 1, backward compatibility is maintained where all above mentioned packets are dropped (when RA is not set). 0x0 (DISABLE): Flexible Rx parser, packet drop in case software error is disabled. 0x1 (ENABLE): Flexible Rx parser, packet drop in case software error is enabled.
13:10	0h RO	**Reserved**
9	0h RW	**Counters Reset (CNTCLR):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.
8	0h RW	**Counters Preset (CNTPRST):** When this bit is set, - MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
7	0h RO	**Reserved**
6:5	0h RW	**Tx Scheduling Algorithm (SCHALG):** This field indicates the algorithm for Tx scheduling: 0x0 (WRR): WRR algorithm. 0x1 (WFQ): WFQ algorithm when DCB feature is selected.Otherwise, Reserved. 0x2 (DWRR): DWRR algorithm when DCB feature is selected.Otherwise, Reserved. 0x3 (SP): Strict priority algorithm.
4:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Receive Arbitration Algorithm (RAA):** This field is used to select the arbitration algorithm for the Rx side. - 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. - 1: Weighted Strict Priority (WSP) 0x0 (SP): Strict priority (SP). 0x1 (WSP): Weighted Strict Priority (WSP).
1	0h RW	**Drop Transmit Status (DTXSTS):** When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. 0x0 (DISABLE): Drop Transmit Status is disabled. 0x1 (ENABLE): Drop Transmit Status is enabled.
0	0h RO	**Reserved**

3.2.337 MTL_DBG_CTL — Offset C08h

The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RW	**ECC Inject Error Control for Tx, Rx and TSO memories (EIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
16	0h RW	**ECC Inject Error Enable for Tx, Rx and TSO memories (EIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Tx, Rx and TSO memories is disabled. 0x1 (ENABLE): ECC Inject Error for Tx, Rx and TSO memories is enabled.
15	0h RW	**Transmit Status Available Interrupt Status Enable (STSIE):** When this bit is set, an interrupt is generated when Transmit status is available in slave mode. 0x0 (DISABLE): Transmit Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Transmit Packet Available Interrupt Status is enabled.
14	0h RW	**Receive Packet Available Interrupt Status Enable (PKTIE):** When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. 0x0 (DISABLE): Receive Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Receive Packet Available Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**FIFO Selected for Access (FIFOSEL):** This field indicates the FIFO selected for debug access: 0x0 (TXFIFO): Tx FIFO. 0x1 (TXSTSFIFO): Tx Status FIFO (only read access when SLVMOD is set). 0x2 (TSOFIFO): TSO FIFO (cannot be accessed when SLVMOD is set). 0x3 (RXFIFO): Rx FIFO.
11	0h RW	**FIFO Write Enable (FIFOWREN):** When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Write is disabled. 0x1 (ENABLE): FIFO Write is enabled.
10	0h RW	**FIFO Read Enable (FIFORDEN):** When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Read is disabled. 0x1 (ENABLE): FIFO Read is enabled.
9	0h RW	**Reset Pointers of Selected FIFO (RSTSEL):** When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset Pointers of Selected FIFO is disabled. 0x1 (ENABLE): Reset Pointers of Selected FIFO is enabled.
8	0h RW	**Reset All Pointers (RSTALL):** When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset All Pointers is disabled. 0x1 (ENABLE): Reset All Pointers is enabled.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Encoded Packet State (PKTSTATE):** This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
4	0h RO	**Reserved**
3:2	0h RW	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
1	0h RW	**Debug Mode Access to FIFO (DBGMOD):** When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: - Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO - Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: - Write access to the Tx FIFO - Read access to the Rx FIFO and Tx Status FIFO 0x0 (DISABLE): Debug Mode Access to FIFO is disabled. 0x1 (ENABLE): Debug Mode Access to FIFO is enabled.
0	0h RW	**FIFO Debug Access Enable (FDBGEN):** When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. 0x0 (DISABLE): FIFO Debug Access is disabled. 0x1 (ENABLE): FIFO Debug Access is enabled.

3.2.338 MTL_DBG_STS — Offset C0Ch

The FIFO Debug Status register contains the status of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0Ch	00000018h

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RO	**Remaining Locations in the FIFO (LOCR):** Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively.
14:10	0h RO	**Reserved**
9	0h RW	**Transmit Status Available Interrupt Status (STSI):** When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Transmit Status Available Interrupt Status not detected. 0x1 (ACTIVE): Transmit Status Available Interrupt Status detected.
8	0h RW	**Receive Packet Available Interrupt Status (PKTI):** When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Receive Packet Available Interrupt Status not detected. 0x1 (ACTIVE): Receive Packet Available Interrupt Status detected.
7:5	0h RO	**Reserved**
4:3	3h RO	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
2:1	0h RO	**Encoded Packet State (PKTSTATE):** This field is used to get the control or status information of the selected FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
0	0h RO	**FIFO Busy (FIFOBUSY):** When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: - All other fields of this register - All fields of the MTL_FIFO_Debug_Data register 0x0 (INACTIVE): FIFO Busy not detected. 0x1 (ACTIVE): FIFO Busy detected.

3.2.339 MTL_FIFO_DEBUG_DATA — Offset C10h

The FIFO Debug Data register contains the data to be written to or read from the FIFOs.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FIFO Debug Data (FDBGDATA):** During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

3.2.340 MTL_INTERRUPT_STATUS — Offset C20h

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MTL Rx Parser Interrupt Status (MTLPIS):** This bit indicates that there is an interrupt from Rx Parser Block. To reset this bit, the application must read the MTL_ Rxp_Interrupt_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Rx Parser Interrupt status not detected. 0x1 (ACTIVE): MTL Rx Parser Interrupt status detected.
22:19	0h RO	**Reserved**
18	0h RO	**EST (TAS- 802.1Qbv) Interrupt Status (ESTIS):** This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt. 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected. 0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected.
17	0h RO	**Debug Interrupt status (DBGIS):** This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Debug Interrupt status not detected. 0x1 (ACTIVE): Debug Interrupt status detected.
16:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Queue 7 Interrupt status (Q7IS):** This bit indicates that there is an interrupt from Queue 7. To reset this bit, the application must read the MTL_Q7_Interrupt_Control_Status Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 7 Interrupt status not detected. 0x1 (ACTIVE): Queue 7 Interrupt status detected.
6	0h RO	**Queue 6 Interrupt status (Q6IS):** This bit indicates that there is an interrupt from Queue 6. To reset this bit, the application must read the MTL_Q6_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 6 Interrupt status not detected. 0x1 (ACTIVE): Queue 6 Interrupt status detected.
5	0h RO	**Queue 5 Interrupt status (Q5IS):** This bit indicates that there is an interrupt from Queue 5. To reset this bit, the application must read the MTL_Q5_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 5 Interrupt status not detected. 0x1 (ACTIVE): Queue 5 Interrupt status detected.
4	0h RO	**Queue 4 Interrupt status (Q4IS):** This bit indicates that there is an interrupt from Queue 4. To reset this bit, the application must read the MTL_Q4_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 4 Interrupt status not detected. 0x1 (ACTIVE): Queue 4 Interrupt status detected.
3	0h RO	**Queue 3 Interrupt status (Q3IS):** This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 3 Interrupt status not detected. 0x1 (ACTIVE): Queue 3 Interrupt status detected.
2	0h RO	**Queue 2 Interrupt status (Q2IS):** This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 2 Interrupt status not detected. 0x1 (ACTIVE): Queue 2 Interrupt status detected.
1	0h RO	**Queue 1 Interrupt status (Q1IS):** This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 1 Interrupt status not detected. 0x1 (ACTIVE): Queue 1 Interrupt status detected.
0	0h RO	**Queue 0 Interrupt status (Q0IS):** This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 0 Interrupt status not detected. 0x1 (ACTIVE): Queue 0 Interrupt status detected.

3.2.341 MTL_RXQ_DMA_MAP0 — Offset C30h

The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection (Q3DDMACH):** When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]). 0x0 (DISABLE): Queue 3 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 3 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**
26:24	0h RW	**Queue 3 Mapped to DMA Channel (Q3MDMACH):** This field controls the routing of the received packet in Queue 3 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. Note: The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved
23:21	0h RO	**Reserved**
20	0h RW	**Queue 2 Enabled for DA-based DMA Channel Selection (Q2DDMACH):** When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]). 0x0 (DISABLE): Queue 2 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 2 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RW	**Queue 2 Mapped to DMA Channel (Q2MDMACH):** This field controls the routing of the received packet in Queue 2 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 1 Enabled for DA-based DMA Channel Selection (Q1DDMACH):** When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]). 0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**
10:8	0h RW	**Queue 1 Mapped to DMA Channel (Q1MDMACH):** This field controls the routing of the received packet in Queue 1 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Queue 0 Enabled for DA-based DMA Channel Selection (Q0DDMACH):** When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field. 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 0 Mapped to DMA Channel (Q0MDMACH):** This field controls the routing of the packet received in Queue 0 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

3.2.342 MTL_RXQ_DMA_MAP1 — Offset C34h

The Receive Queue and DMA Channel Mapping 1 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 7 Enabled for DA-based DMA Channel Selection (Q7DDMACH):** When set, this bit indicates that the packets received in Queue 7 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 7 are routed to the DMA Channel programmed in the Q7MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Queue 7 Mapped to DMA Channel (Q7MDMACH):** This field controls the routing of the packet received in Queue 7 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q7DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
23:21	0h RO	**Reserved**
20	0h RW	**Queue 6 Enabled for DA-based DMA Channel Selection (Q6DDMACH):** When set, this bit indicates that the packets received in Queue 6 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 6 are routed to the DMA Channel programmed in the Q6MDMACH field. 0x0 (DISABLE): Queue 6 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 6 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**
18:16	0h RW	**Queue 6 Mapped to DMA Channel (Q6MDMACH):** This field controls the routing of the packet received in Queue 6 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q6DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 5 Enabled for DA-based DMA Channel Selection (Q5DDMACH):** When set, this bit indicates that the packets received in Queue 5 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 5 are routed to the DMA Channel programmed in the Q5MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Queue 5 Mapped to DMA Channel (Q5MDMACH):** This field controls the routing of the packets received in Queue 5 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q5DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**
4	0h RW	**Queue 4 Enabled for DA-based DMA Channel Selection (Q4DDMACH):** When set, this bit indicates that the packets received in Queue 4 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 4 are routed to the DMA Channel programmed in the Q4MDMACH field. 0x0 (DISABLE): Queue 4 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 4 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 4 Mapped to DMA Channel (Q4MDMACH):** This field controls the routing of the packet received in Queue 4 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q4DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

3.2.343 MTL_TBS_CTRL — Offset C40h

This register controls the operation of Time Based Scheduling.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**Launch Expiry Offset (LEOS):** The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Launch Expiry GSN Offset (LEGOS):** The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.
3:2	0h RO	**Reserved**
1	0h RW	**Launch Expiry Offset Valid (LEOV):** When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time. 0x0 (INVALID): LEOS field is invalid. 0x1 (VALID): LEOS field is valid.
0	0h RW	**EST offset Mode (ESTM):** When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8]. 0x0 (DISABLE): EST offset Mode is disabled. 0x1 (ENABLE): EST offset Mode is enabled.

3.2.344 MTL_EST_CONTROL — Offset C50h

This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PTP Time Offset Value (PTOV):** The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23:12	000h RW	**Current Time Offset Value (CTOV):** Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Time Interval Left Shift Amount (TILS):** This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. - 000: No left shift needed (equal to x1ns) - 001: Left shift TI by 1 bit (equal to x2ns) - 010: Left shift TI by 2 bits (equal to x4ns) - . - . - 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.
7:6	0h RW	**Loop Count to report Scheduling Error (LCSE):** Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register. 0x0 (M_4_ITERNS): 4 iterations. 0x1 (M_8_ITERNS): 8 iterations. 0x2 (M_16_ITERNS): 16 iterations. 0x3 (M_32_ITERNS): 32 iterations.
5	0h RW	**Drop Frames causing Scheduling Error (DFBS):** When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped. 0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error. 0x1 (DROP): Drop Frames causing Scheduling Error.
4	0h RW	**Do not Drop frames during Frame Size Error (DDBF):** When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register). 0x0 (DROP): Drop frames during Frame Size Error. 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error.
3:2	0h RO	**Reserved**
1	0h RW	**Switch to S/W owned list (SSWL):** When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Switch to S/W owned list is disabled. 0x1 (ENABLE): Switch to S/W owned list is enabled.
0	0h RW	**Enable EST (EEST):** When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. If any uncorrectable error is detected in the EST memory the hardware resets this bit and disables the EST function. 0x0 (DISABLE): EST is disabled. 0x1 (ENABLE): EST is enabled.

3.2.345 MTL_EST_STATUS — Offset C58h

This register provides Status related to Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Current GCL Slot Number (CGSN):** Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:8	00h RO	**BTR Error Loop Count (BTRL):** Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "11111111" indicates the iterations exceeded the value of 128 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	0h RO	**S/W owned list (SWOL):** When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default. 0x0 (INACTIVE): Gate control list number "0" is owned by software. 0x1 (ACTIVE): Gate control list number "1" is owned by software.
6:5	0h RO	**Reserved**
4	0h RW	**Constant Gate Control Error (CGCE):** This error occurs when the list length (LLR) is 1 and the Cycle Time (CTR) is less than or equal to the programmed Time Interval (TI) value after the optional Left Shifting. The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Constant Gate Control Error not detected. 0x1 (ACTIVE): Constant Gate Control Error detected.
3	0h RO	**Head-Of-Line Blocking due to Scheduling (HLBS):** Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Head-Of-Line Blocking due to Frame Size (HLBF):** Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected.
1	0h RW	**BTR Error (BTRE):** When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "11111111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "11111111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): BTR Error not detected. 0x1 (ACTIVE): BTR Error detected.
0	0h RW	**Switch to S/W owned list Complete (SWLC):** When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Switch to S/W owned list Complete not detected. 0x1 (ACTIVE): Switch to S/W owned list Complete detected.

3.2.346 MTL_EST_SCH_ERROR — Offset C60h

This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Schedule Error Queue Number (SEQN):** The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

3.2.347 MTL_EST_FRM_SIZE_ERROR — Offset C64h

This register provides the One Hot encoded Queue Numbers that are having the Frame Size related error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Frame Size Error Queue Number (FEQN):** The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

3.2.348 MTL_EST_FRM_SIZE_CAPTURE — Offset C68h

This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:16	0h RO	**Queue Number of HLBF (HBFQ):** Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	0h RO	**Reserved**
14:0	0000h RO	**Frame Size of HLBF (HBFS):** Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

3.2.349 MTL_EST_INTR_ENABLE — Offset C70h

This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Interrupt Enable for CGCE (CGCE):** When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt 0x0 (DISABLE): Interrupt for CGCE is disabled. 0x1 (ENABLE): Interrupt for CGCE is enabled.
3	0h RW	**Interrupt Enable for HLBS (IEHS):** When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBS is disabled. 0x1 (ENABLE): Interrupt for HLBS is enabled.
2	0h RW	**Interrupt Enable for HLBF (IEHF):** When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBF is disabled. 0x1 (ENABLE): Interrupt for HLBF is enabled.
1	0h RW	**Interrupt Enable for BTR Error (IEBE):** When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for BTR Error is disabled. 0x1 (ENABLE): Interrupt for BTR Error is enabled.
0	0h RW	**Interrupt Enable for Switch List (IECC):** When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for Switch List is disabled. 0x1 (ENABLE): Interrupt for Switch List is enabled.

3.2.350 MTL_EST_GCL_CONTROL — Offset C80h

This register provides the control information for reading/writing to the Gate Control lists.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**ECC Inject Error Control for EST Memory (ESTEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
21	0h RW	**EST ECC Inject Error Enable (ESTEIEE):** When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): EST ECC Inject Error is disabled. 0x1 (ENABLE): EST ECC Inject Error is enabled.
20:17	0h RO	**Reserved**
16:8	000h RW	**Gate Control List Address: (GCLA when GCRR is "0"). (ADDR):** Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. - 000: BTR Low (31:0) - 001: BTR High (63:31) - 010: CTR Low (31:0) - 011: CTR High (39:32) - 100: TER (31:0) - 101: LLR (n:0) (where n is (log{512} / log2)) - Others: Reserved
7:6	0h RO	**Reserved**
5	0h RW	**Debug Mode Bank Select (DBGB):** When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used. 0x0 (BANK0): R/W in debug mode should be directed to Bank 0. 0x1 (BANK1): R/W in debug mode should be directed to Bank 1.
4	0h RW	**Debug Mode (DBGM):** When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use. 0x0 (DISABLE): Debug Mode is disabled. 0x1 (ENABLE): Debug Mode is enabled.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Gate Control Related Registers (GCRR):** When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA. 0x0 (DISABLE): Gate Control Related Registers are disabled. 0x1 (ENABLE): Gate Control Related Registers are enabled.
1	0h RW	**Read '1', Write '0': (R1W0):** When set to '1': Read Operation When set to '0': Write Operation. 0x0 (WRITE): Write Operation. 0x1 (READ): Read Operation.
0	0h RW	**Start Read/Write Op (SRWO):** When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Start Read/Write Op disabled. 0x1 (ENABLE): Start Read/Write Op enabled.

3.2.351 MTL_EST_GCL_DATA — Offset C84h

This register holds the read data or write data in case of reads and writes respectively.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Gate Control Data (GCD):** The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

3.2.352 MTL_FPE_CTRL_STS — Offset C90h

This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**HRS:** Hold/Release Status - 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. - 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State.
27:16	0h RO	**Reserved**
15:8	00h RW	**Preemption Classification (PEC):** When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	0h RO	**Reserved**
1:0	0h RW	**Additional Fragment Size (AFSZ):** used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes

3.2.353 MTL_FPE_ADVANCE — Offset C94h

This register holds the Hold and Release Advance time.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Release Advance (RADV):** The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.
15:0	0000h RW	**Hold Advance (HADV):** The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

3.2.354 MTL_RXP_CONTROL_STATUS — Offset CA0h

The MTL_RXP_Control_Status register establishes the operating mode of Rx Parser and provides some status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CA0h	80FF00FFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**RX Parser in Idle state (RXPI):** This status bit is set to 1 when the Rx parser is in Idle State and waiting for a new packet for processing. This bit is used as a handshake with software when parser gets disables. After disabling, when bit is set then software can update the Rx parser instruction table. 0x0 (INACTIVE): RX Parser not in Idle state. 0x1 (ACTIVE): RX Parser in Idle state.
30:24	0h RO	**Reserved**
23:16	FFh RW	**Number of parsable entries in the Instruction table (NPE):** This control indicates the number of parsable entries in the Instruction Memory. This is used in Rx parser logic to detect programming Error. In case number of parsed entries for a packet is more than this entry then NPEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set.
15:8	0h RO	**Reserved**
7:0	FFh RW	**Number of valid entry address/index in the Instruction table (NVE):** This control indicates the number of valid entries address/index in the Instruction Memory (i.e. when NVE field in register=31, the maximum valid entry address is NVE+1 i.e. addresses/indices=0 to 32, or 33 entries). This is used in Rx parser logic to detect any programming Error. In case while parsing Table address (memory address) found to be more than this maximum valid entry address then NVEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set. Note: The minimum value of this should be 2.

3.2.355 MTL_RXP_INTERRUPT_CONTROL_STATUS — Offset CA4h

The MTL_RXP_Interrupt_Control_Status registers provides enable control for the interrupts and provides interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Packet Drop due to RF Interrupt Enable (PDRFIE):** When this bit is set, the PDRFIS interrupt is enabled. When this bit is reset, the PDRFIS interrupt is disabled. 0x0 (DISABLE): Packet Drop due to RF Interrupt is disabled. 0x1 (ENABLE): Packet Drop due to RF Interrupt is enabled.
18	0h RW	**Frame Offset Overflow Interrupt Enable (FOOVIE):** When this bit is set, the FOOVIS interrupt is enabled. When this bit is reset, the FOOVIS interrupt is disabled. 0x0 (DISABLE): Frame Offset Overflow Interrupt is disabled. 0x1 (ENABLE): Frame Offset Overflow Interrupt is enabled.
17	0h RW	**Number of Parsable Entries Overflow Interrupt Enable (NPEOVIE):** When this bit is set, the NPEOVIS interrupt is enabled. When this bit is reset, the NPEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Parsable Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Parsable Entries Overflow Interrupt is enabled.
16	0h RW	**Number of Valid Entries Overflow Interrupt Enable (NVEOVIE):** When this bit is set, the NVEOVIS interrupt is enabled. When this bit is reset, the NVEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Valid Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Valid Entries Overflow Interrupt is enabled.
15:4	0h RO	**Reserved**
3	0h RW	**Packet Dropped due to RF Interrupt Status (PDRFIS):** If the Rx Parser result says to drop the packet by setting RF=1 in the instruction memory, then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Packet Dropped due to RF Interrupt Status not detected. 0x1 (ACTIVE): Packet Dropped due to RF Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Frame Offset Overflow Interrupt Status (FOOVIS):** While parsing if the Instruction table entry's 'Frame Offset' found to be more than EOF offset, then then this bit is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Frame Offset Overflow Interrupt Status not detected. 0x1 (ACTIVE): Frame Offset Overflow Interrupt Status detected.
1	0h RW	**Number of Parsable Entries Overflow Interrupt Status (NPEOVIS):** While parsing a packet if the number of parsed entries found to be more than NPE[] (Number of Parseable Entries in MTL_RXP_Control register),then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Parsable Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Parsable Entries Overflow Interrupt Status detected.
0	0h RW	**Number of Valid Entry Address/Index Overflow Interrupt Status (NVEOVIS):** While parsing if the Instruction address found to be more than NVE (Number of Valid Entry Address/index in MTL_RXP_Control register), then this bit is set to 1. For example, when NVE field in register=31, the maximum valid entry address/index is NVE+1 i.e. 32 (addresses/indices=0 to 32, or 33 entries), so NVEOVIS is set when currently processed entry indicates next address is 33 or more i.e. 34th or later entries. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Valid Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Valid Entries Overflow Interrupt Status detected.

3.2.356 MTL_RXP_DROP_CNT — Offset CA8h

The MTL_RXP_Drop_Cnt register provides the drop count of Rx Parser initiated drops.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CA8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Drop Counter Overflow Bit (RXPDCOVF):** When set, this bit indicates that the MTL_RXP_Drop_cnt (RXPDC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Drop count overflow not occurred. 0x1 (ACTIVE): Rx Parser Drop count overflow occurred.
30:0	00000000h RO	**Rx Parser Drop count (RXPDC):** This 31-bit counter is implemented whenever a Rx Parser Drops a packet due to RF =1. The counter is cleared when the register is read.

3.2.357 MTL_RXP_ERROR_CNT — Offset CAChh

The MTL_RXP_Error_Cnt register provides the Rx Parser related error occurrence count.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Error Counter Overflow Bit (RXPECOVF):** When set, this bit indicates that the MTL_RXP_Error_cnt (RXPEC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Error count overflow not occurred. 0x1 (ACTIVE): Rx Parser Error count overflow occurred.
30:0	00000000h RO	**Rx Parser Error count (RXPEC):** This 31-bit counter is implemented whenever a Rx Parser encounters following Error scenarios - Entry address >= NVE[] - Number Parsed Entries >= NPE[] - Entry address > EOF data entry address The counter is cleared when the register is read.

3.2.358 MTL_RXP_INDIRECT_ACC_CONTROL_STATUS — Offset CB0h

The MTL_RXP_Indirect_Acc_Control_Status register provides the Indirect Access control and status for Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**FRP Instruction Table Access Busy (STARTBUSY):** When this bit is set to 1 by the software then it indicates to start the Read/Write operation from/to the Rx Parser Memory. Software should read this bit as 0 before issuing read or write request to access the Parser Memory Instructions. This bit when set to 1 indicates that hardware is busy until its gets cleared by hardware and software should not issue any read or write operation. 0x0 (INACTIVE): hardware not busy. 0x1 (ACTIVE): hardware is busy (Read/Write operation from/to the Rx Parser Memory).
30:23	0h RO	**Reserved**
22:21	0h RW	**ECC Inject Error Control for Rx Parser Memory (RXPEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**ECC Inject Error Enable for Rx Parser Memory (RXPEIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Rx Parser Memory is disabled. 0x1 (ENABLE): ECC Inject Error for Rx Parser Memory is enabled.
19:17	0h RO	**Reserved**
16	0h RW	**Read Write Control (WRRDN):** When this bit is set to 1 indicates the write operation to the Rx Parser Memory. When this bit is set to 0 indicates the read operation to the Rx Parser Memory. 0x0 (READ): Read operation to the Rx Parser Memory. 0x1 (WRITE): Write operation to the Rx Parser Memory.
15:10	0h RO	**Reserved**
9:0	000h RW	**FRP Instruction Table Offset Address (ADDR):** This field indicates the ADDR of the 32-bit entry in Rx parser instruction table. Each entry has 128-bit (4x32-bit words). There are 256 FRP entries. This must be written by the software before issuing any Read/Write command. The hardware does not support auto-increment of ADDR.

3.2.359 MTL_RXP_INDIRECT_ACC_DATA — Offset CB4h

The MTL_RXP_Indirect_Acc_Data registers holds the data associated to Indirect Access to Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**FRP Instruction Table Write/Read Data (DATA):** Software should write this register before issuing any write command. The hardware provides the read data from the Rx Parser Memory for read operation when STARTBUSY =0 after read command.

3.2.360 MTL_ECC_CONTROL — Offset CC0h

The MTL_ECC_Control register establishes the operating mode of ECC related to MTL memories.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**MTL ECC Error Address Status Over-ride (MEEAO):** When set, the following error address fields hold the last valid address where the error is detected. When reset, the following error address fields hold the first address where the error is detected. EUEAS/ECEAS of MTL_ECC_Err_Addr_Status register. 0x0 (DISABLE): MTL ECC Error Address Status Over-ride is disabled. 0x1 (ENABLE): MTL ECC Error Address Status Over-ride is enabled.
7:5	0h RO	**Reserved**
4	0h RW	**TSO memory ECC Enable (TSOEE):** When set to 1, enables the ECC feature for TSO memory in DMA. When set to zero, disables the ECC feature for TSO memory in DMA. 0x0 (DISABLE): TSO memory ECC is disabled. 0x1 (ENABLE): TSO memory ECC is enabled.
3	0h RW	**MTL Rx Parser ECC Enable (MRXPEE):** When set to 1, enables the ECC feature for Rx Parser memory. When set to zero, disables the ECC feature for Rx Parser memory. 0x0 (DISABLE): MTL Rx Parser ECC is disabled. 0x1 (ENABLE): MTL Rx Parser ECC is enabled.
2	0h RW	**MTL EST ECC Enable (MESTEE):** When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory. 0x0 (DISABLE): MTL EST ECC is disabled. 0x1 (ENABLE): MTL EST ECC is enabled.
1	0h RW	**MTL Rx FIFO ECC Enable (MRXEE):** When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory. 0x0 (DISABLE): MTL Rx FIFO ECC is disabled. 0x1 (ENABLE): MTL Rx FIFO ECC is enabled.
0	0h RW	**MTL Tx FIFO ECC Enable (MTXEE):** When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory. 0x0 (DISABLE): MTL Tx FIFO ECC is disabled. 0x1 (ENABLE): MTL Tx FIFO ECC is enabled.

3.2.361 MTL_SAFETY_INTERRUPT_STATUS — Offset CC4h

The MTL_Safety_Interrupt_Status registers provides Safety interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MTL ECC Uncorrectable error Interrupt Status (MEUIS):** This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**MTL ECC Correctable error Interrupt Status (MECIS):** This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Correctable error Interrupt Status detected.

3.2.362 MTL_ECC_INTERRUPT_ENABLE — Offset CC8h

The MTL_ECC_Interrupt_Enable register provides enable bits for the ECC interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Rx Parser memory Correctable Error Interrupt Enable (RPCEIE):** When set, generates an interrupt when an uncorrectable error is detected at the Rx Parser memory interface. It is indicated in RPCES status bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx Parser memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx Parser memory Correctable Error Interrupt is enabled.
11:9	0h RO	**Reserved**
8	0h RW	**EST memory Correctable Error Interrupt Enable (ECEIE):** When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): EST memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): EST memory Correctable Error Interrupt is enabled.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Rx memory Correctable Error Interrupt Enable (RXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx memory Correctable Error Interrupt is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Tx memory Correctable Error Interrupt Enable (TXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Tx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Tx memory Correctable Error Interrupt is enabled.

3.2.363 MTL_ECC_INTERRUPT_STATUS — Offset CCCh

The MTL_ECC_Interrupt_Status register provides MTL ECC Interrupt Status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**Rx Parser memory Uncorrectable Error Status (RPUES):** When set, indicates that an uncorrectable error is detected at Rx Parser memory interface. 0x0 (INACTIVE): Rx Parser memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): Rx Parser memory Uncorrectable Error Status detected.
13	0h RW	**MTL Rx Parser memory Address Mismatch Status (RPAMS):** This bit when set indicates that address mismatch is found for address bus of Rx Parser memory. 0x0 (INACTIVE): MTL Rx Parser memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Address Mismatch Status detected.
12	0h RW	**MTL Rx Parser memory Correctable Error Status (RPCES):** This bit when set indicates that correctable error is detected at RX Parser memory interface. 0x0 (INACTIVE): MTL Rx Parser memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Correctable Error Status detected.
11	0h RO	**Reserved**
10	0h RW	**MTL EST memory Uncorrectable Error Status (EUES):** When set, indicates that an uncorrectable error is detected at MTL EST memory interface. 0x0 (INACTIVE): MTL EST memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Uncorrectable Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**MTL EST memory Address Mismatch Status (EAMS):** This bit when set indicates that address mismatch is found for address bus of MTL EST memory. 0x0 (INACTIVE): MTL EST memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL EST memory Address Mismatch Status detected.
8	0h RW	**MTL EST memory Correctable Error Status (ECES):** This bit when set indicates that correctable error is detected at the MTL EST memory. 0x0 (INACTIVE): MTL EST memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Correctable Error Status detected.
7	0h RO	**Reserved**
6	0h RW	**MTL Rx memory Uncorrectable Error Status (RXUES):** When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface. 0x0 (INACTIVE): MTL Rx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory Uncorrectable Error Status detected.
5	0h RW	**MTL Rx memory Address Mismatch Status (RXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx memory Address Mismatch Status detected.
4	0h RW	**MTL Rx memory Correctable Error Status (RXCES):** This bit when set indicates that correctable error is detected at the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory correctable Error Status detected.
3	0h RO	**Reserved**
2	0h RW	**MTL Tx memory Uncorrectable Error Status (TXUES):** When set, indicates that an uncorrectable error is detected at the MTL TX memory interface. 0x0 (INACTIVE): MTL Tx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Uncorrectable Error Status detected.
1	0h RW	**MTL Tx memory Address Mismatch Status (TXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Tx memory Address Mismatch Status detected.
0	0h RW	**MTL Tx memory Correctable Error Status (TXCES):** This bit when set indicates that a correctable error is detected at the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Correctable Error Status detected.

3.2.364 MTL_ECC_ERR_STS_RCTL — Offset CD0h

The MTL_ECC_Err_Sts_Rctl register establishes the control for ECC Error status capture.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Clear Uncorrectable Error Status (CUES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Uncorrectable Error Status not detected. 0x1 (ACTIVE): Clear Uncorrectable Error Status detected.
4	0h RW	**Clear Correctable Error Status (CCES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Correctable Error Status not detected. 0x1 (ACTIVE): Clear Correctable Error Status detected.
3:1	0h RW	**MTL ECC Memory Selection (EMS):** When EESRE bit of this register is set, this field indicates which memory's error status value to be read. The memory selection encoding is as described below. 0x0 (TX_MEM): MTL Tx memory. 0x1 (RX_MEM): MTL Rx memory. 0x2 (EST_MEM): MTL EST memory. 0x3 (RXP_MEM): MTL Rx Parser memory. 0x4 (TSO_MEM): DMA TSO memory.
0	0h RW	**MTL ECC Error Status Read Enable (EESRE):** When this bit is set, based on the EMS field of this register, the respective memory's error status values are captured as described: - The correctable and uncorrectable error count values are captured into MTL_ECC_Err_Cnt_Status register - The address location's of correctable and uncorrectable errors are captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers. 0x0 (DISABLE): MTL ECC Error Status Read is disabled. 0x1 (ENABLE): MTL ECC Error Status Read is enabled.

3.2.365 MTL_ECC_ERR_ADDR_STATUS — Offset CD4h

The MTL_ECC_Err_Addr_Status register provides the memory addresses for the correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**MTL ECC Uncorrectable Error Address Status (EUEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected.
15:0	0000h RO	**MTL ECC Correctable Error Address Status (ECEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected.

3.2.366 MTL_ECC_ERR_CNTR_STATUS — Offset CD8h

The MTL_ECC_Err_Cntr_Status register provides ECC Error count for Correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**MTL ECC Uncorrectable Error Counter Status (EUECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's uncorrectable error count value.
15:8	0h RO	**Reserved**
7:0	00h RO	**MTL ECC Correctable Error Counter Status (ECECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value.

3.2.367 MTL_DPP_CONTROL — Offset CE0h

The MTL_DPP_Control establishes the operating mode of Data Parity protection and error injection.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**Insert Parity error in CSR Read data parity generator (IPECW):** When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in AXI slave Interface Data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in CSR Read data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in CSR Read data parity generator is enabled.
12	0h RW	**Insert Parity error in AXI Slave Write data parity generator (IPEASW):** When set to 1, parity bit of first valid data generated by the AXI parity generator is (or at PG9 as shown in AXI slave Interface Data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in AXI Slave Write data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in AXI Slave Write data parity generator is enabled.
11	0h RW	**Insert Parity error in Rx write-back Descriptor parity generator (IPERD):** When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Receive data path parity protection diagram) is flipped. 0x0 (DISABLE): Insert Parity error in Rx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Rx write-back Descriptor parity generator is enabled.
10	0h RW	**Insert Parity error in Tx write-back Descriptor parity generator (IPETD):** When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in Tx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Tx write-back Descriptor parity generator is enabled.
9	0h RW	**Insert Parity Error in DMA TSO parity generator (IPETSO):** When set to 1, parity bit of first valid data generated by the DMA TSO parity generator is (or at PG3 as shown in Transmit data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA TSO parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA TSO parity generator is enabled.
8	0h RW	**Insert Parity Error in DMA DTX Control word parity generator (IPEDDC):** When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA DTX Control word parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA DTX Control word parity generator is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Insert Parity Error in MTL Rx FIFO read control parity generator (IPEMRF):** When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Receive data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is enabled.
6	0h RW	**Insert Parity Error in MTL Tx Status parity generator (IPEMTS):** When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Tx Status parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Tx Status parity generator is enabled.
5	0h RW	**Insert Parity Error in MTL checksum parity generator (IPEMC):** When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL checksum parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL checksum parity generator is enabled.
4	0h RW	**Insert Parity Error in Interface Data parity generator (IPEID):** When set to 1, parity bit of first valid input data generated by the Interface data parity generator (or at PG1 as shown in Transmit data path parity protection diagram) is flipped. Following are the input data bus on which parity bits are generated based on configuration selected In AHB Config, hrdata_i In AXI config, rdata_m_i In DMA Config, mdc_rdata_i In MTL Config, ati_data_i Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in Interface Data parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in Interface Data parity generator is enabled.
3:2	0h RO	**Reserved**
1	0h RW	**Odd Parity Enable (OPE):** When set to 1, enables odd parity protection on all the external interfaces and when set to 0, enables even parity protection on all the external interfaces. 0x0 (DISABLE): Odd Parity is disabled. 0x1 (ENABLE): Odd Parity is enabled.
0	0h RW	**Enable Data path Parity Protection (EDPP):** When set to 1, enables the parity protection for EQOS datapath by generating and checking the parity on EQOS datapath. When set to 0, disables the parity protection for EQOS datapath. 0x0 (DISABLE): Data path Parity Protection is disabled. 0x1 (ENABLE): Data path Parity Protection is enabled.

3.2.368 MTL_TXQ0_OPERATION_MODE — Offset D00h

The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Reserved - 2'b10: Enabled - 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.369 MTL_TXQ0_UNDERFLOW — Offset D04h

The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.370 MTL_TXQ0_DEBUG — Offset D08h

The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.371 MTL_TXQ0_ETS_STATUS — Offset D14h

The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.372 MTL_TXQ0_QUANTUM_WEIGHT — Offset D18h

The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Quantum or Weights (ISCQW):** When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.

3.2.373 MTL_Q0_INTERRUPT_CONTROL_STATUS — Offset D2Ch

This register contains the interrupt enable and status bits for the queue 0 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.374 MTL_RXQ0_OPERATION_MODE — Offset D30h

The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.375 MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT — Offset D34h

The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.376 MTL_RXQ0_DEBUG — Offset D38h

The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.377 MTL_RXQ0_CONTROL — Offset D3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.378 MTL_TXQ1_OPERATION_MODE — Offset D40h

The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.379 MTL_TXQ1_UNDERFLOW — Offset D44h

The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.380 MTL_TXQ1_DEBUG — Offset D48h

The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.381 MTL_TXQ1_ETS_CONTROL — Offset D50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.382 MTL_TXQ1_ETS_STATUS — Offset D54h

The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.383 MTL_TXQ1_QUANTUM_WEIGHT — Offset D58h

The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.384 MTL_TXQ1_SENDSLOPECREDIT — Offset D5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.385 MTL_TXQ1_HICREDIT — Offset D60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.386 MTL_TXQ1_LOCREDIT — Offset D64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.387 MTL_Q1_INTERRUPT_CONTROL_STATUS — Offset D6Ch

This register contains the interrupt enable and status bits for the queue 1 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.388 MTL_RXQ1_OPERATION_MODE — Offset D70h

The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.389 MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT — Offset D74h

The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.390 MTL_RXQ1_DEBUG — Offset D78h

The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.391 MTL_RXQ1_CONTROL — Offset D7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.392 MTL_TXQ2_OPERATION_MODE — Offset D80h

The Queue 2 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.393 MTL_TXQ2_UNDERFLOW — Offset D84h

The Queue 2 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.394 MTL_TXQ2_DEBUG — Offset D88h

The Queue 2 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.395 MTL_TXQ2_ETS_CONTROL — Offset D90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.396 MTL_TXQ2_ETS_STATUS — Offset D94h

The Queue 2 ETS Status register provides the average traffic transmitted in Queue 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.397 MTL_TXQ2_QUANTUM_WEIGHT — Offset D98h

The Queue 2 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.398 MTL_TXQ2_SENDSLOPECREDIT — Offset D9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.399 MTL_TXQ2_HICREDIT — Offset DA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.400 MTL_TXQ2_LOCREDIT — Offset DA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.401 MTL_Q2_INTERRUPT_CONTROL_STATUS — Offset DACh

This register contains the interrupt enable and status bits for the queue 2 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.402 MTL_RXQ2_OPERATION_MODE — Offset DB0h

The Queue 2 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.403 MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT — Offset DB4h

The Queue 2 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.404 MTL_RXQ2_DEBUG — Offset DB8h

The Queue 2 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.405 MTL_RXQ2_CONTROL — Offset DBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DBCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.406 MTL_TXQ3_OPERATION_MODE — Offset DC0h

The Queue 3 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.407 MTL_TXQ3_UNDERFLOW — Offset DC4h

The Queue 3 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.408 MTL_TXQ3_DEBUG — Offset DC8h

The Queue 3 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.409 MTL_TXQ3_ETS_CONTROL — Offset DD0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.410 MTL_TXQ3_ETS_STATUS — Offset DD4h

The Queue 3 ETS Status register provides the average traffic transmitted in Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.411 MTL_TXQ3_QUANTUM_WEIGHT — Offset DD8h

The Queue 3 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DD8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.412 MTL_TXQ3_SENDSLOPECREDIT — Offset DDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DDCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.413 MTL_TXQ3_HICREDIT — Offset DE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.414 MTL_TXQ3_LOCREDIT — Offset DE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DE4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.415 MTL_Q3_INTERRUPT_CONTROL_STATUS — Offset DECh

This register contains the interrupt enable and status bits for the queue 3 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.416 MTL_RXQ3_OPERATION_MODE — Offset DF0h

The Queue 3 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.417 MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT — Offset DF4h

The Queue 3 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.418 MTL_RXQ3_DEBUG — Offset DF8h

The Queue 3 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.419 MTL_RXQ3_CONTROL — Offset DFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DFCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.420 MTL_TXQ4_OPERATION_MODE — Offset E00h

The Queue 4 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.421 MTL_TXQ4_UNDERFLOW — Offset E04h

The Queue 4 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + E04h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.422 MTL_TXQ4_DEBUG — Offset E08h

The Queue 4 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E08h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.423 MTL_TXQ4_ETS_CONTROL — Offset E10h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.424 MTL_TXQ4_ETS_STATUS — Offset E14h

The Queue 4 ETS Status register provides the average traffic transmitted in Queue 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.425 MTL_TXQ4_QUANTUM_WEIGHT — Offset E18h

The Queue 4 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.426 MTL_TXQ4_SENDSLOPECREDIT — Offset E1Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.427 MTL_TXQ4_HICREDIT — Offset E20h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.428 MTL_TXQ4_LOCREDIT — Offset E24h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.429 MTL_Q4_INTERRUPT_CONTROL_STATUS — Offset E2Ch

This register contains the interrupt enable and status bits for the queue 4 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.430 MTL_RXQ4_OPERATION_MODE — Offset E30h

The Queue 4 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + E30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.431 MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT — Offset E34h

The Queue 4 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.432 MTL_RXQ4_DEBUG — Offset E38h

The Queue 4 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.433 MTL_RXQ4_CONTROL — Offset E3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.434 MTL_TXQ5_OPERATION_MODE — Offset E40h

The Queue 5 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.435 MTL_TXQ5_UNDERFLOW — Offset E44h

The Queue 5 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + E44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.436 MTL_TXQ5_DEBUG — Offset E48h

The Queue 5 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.437 MTL_TXQ5_ETS_CONTROL — Offset E50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.438 MTL_TXQ5_ETS_STATUS — Offset E54h

The Queue 5 ETS Status register provides the average traffic transmitted in Queue 5.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.439 MTL_TXQ5_QUANTUM_WEIGHT — Offset E58h

The Queue 5 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 5.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.440 MTL_TXQ5_SENDSLOPECREDIT — Offset E5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.441 MTL_TXQ5_HICREDIT — Offset E60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.442 MTL_TXQ5_LOCREDIT — Offset E64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.443 MTL_Q5_INTERRUPT_CONTROL_STATUS — Offset E6Ch

This register contains the interrupt enable and status bits for the queue 5 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.444 MTL_RXQ5_OPERATION_MODE — Offset E70h

The Queue 5 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + E70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.445 MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT — Offset E74h

The Queue 5 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.446 MTL_RXQ5_DEBUG — Offset E78h

The Queue 5 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.447 MTL_RXQ5_CONTROL — Offset E7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.448 MTL_TXQ6_OPERATION_MODE — Offset E80h

The Queue 6 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RW	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should be always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.449 MTL_TXQ6_UNDERFLOW — Offset E84h

The Queue 6 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + E84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.450 MTL_TXQ6_DEBUG — Offset E88h

The Queue 6 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.451 MTL_TXQ6_ETS_CONTROL — Offset E90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.452 MTL_TXQ6_ETS_STATUS — Offset E94h

The Queue 6 ETS Status register provides the average traffic transmitted in Queue 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.453 MTL_TXQ6_QUANTUM_WEIGHT — Offset E98h

The Queue 6 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.454 MTL_TXQ6_SENDSLOPECREDIT — Offset E9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.455 MTL_TXQ6_HICREDIT — Offset EA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.456 MTL_TXQ6_LOCREDIT — Offset EA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.457 MTL_Q6_INTERRUPT_CONTROL_STATUS — Offset EACh

This register contains the interrupt enable and status bits for the queue 6 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.458 MTL_RXQ6_OPERATION_MODE — Offset EB0h

The Queue 6 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + EB0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.459 MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT — Offset EB4h

The Queue 6 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EB4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.460 MTL_RXQ6_DEBUG — Offset EB8h

The Queue 6 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EB8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.461 MTL_RXQ6_CONTROL — Offset EBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EBCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.462 MTL_TXQ7_OPERATION_MODE — Offset EC0h

The Queue 7 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EC0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

3.2.463 MTL_TXQ7_UNDERFLOW — Offset EC4h

The Queue 7 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + EC4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.464 MTL_TXQ7_DEBUG — Offset EC8h

The Queue 7 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EC8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

3.2.465 MTL_TXQ7_ETS_CONTROL — Offset ED0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ED0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

3.2.466 MTL_TXQ7_ETS_STATUS — Offset ED4h

The Queue 7 ETS Status register provides the average traffic transmitted in Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ED4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

3.2.467 MTL_TXQ7_QUANTUM_WEIGHT — Offset ED8h

The Queue 7 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ED8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

3.2.468 MTL_TXQ7_SENDSLOPECREDIT — Offset EDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EDCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

3.2.469 MTL_TXQ7_HICREDIT — Offset EE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EE0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

3.2.470 MTL_TXQ7_LOCREDIT — Offset EE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EE4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

3.2.471 MTL_Q7_INTERRUPT_CONTROL_STATUS — Offset EECh

This register contains the interrupt enable and status bits for the queue 7 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

3.2.472 MTL_RXQ7_OPERATION_MODE — Offset EF0h

The Queue 7 Receive Operation Mode register establishes the Receive queue operating modes and command.

The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + EF0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

3.2.473 MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT — Offset EF4h

The Queue 7 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EF4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.474 MTL_RXQ7_DEBUG — Offset EF8h

The Queue 7 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EF8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

3.2.475 MTL_RXQ7_CONTROL — Offset EFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + EFCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

3.2.476 DMA_MODE — Offset 1000h

The Bus Mode register establishes the bus operating modes for the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**Rx DMA's Maximum Number of Descriptors to be fetched in a burst (RNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2
21:20	0h RW	**Tx DMA's Maximum Number of Descriptors to be fetched in a burst (TNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Descriptor Cache Enable (DCHE):** When set enables prefetching of descriptors to the Descriptor Cache. When reset descriptor cache feature is disabled. 0x0 (DISABLE): Descriptor Cache Support is disabled. 0x1 (ENABLE): Descriptor Cache Support is enabled.
18	0h RO	**Reserved**
17:16	0h RW	**Interrupt Mode (INTM):** This field defines the interrupt mode of GbE Controller. The behavior of the following outputs changes depending on the following settings: - sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) - sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) - sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. - 00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. - 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 11: Reserved 0x0 (MODE0): See above description. 0x1 (MODE1): See above description. 0x2 (MODE2): See above description. 0x3 (RSVD): Reserved.
15:11	0h RO	**Reserved**
10	0h RW	**Reserved**
9	0h RO	**Reserved**
8	0h RW	**Descriptor Posted Write (DSPW):** When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. 0x0 (DISABLE): Descriptor Posted Write is disabled. 0x1 (ENABLE): Descriptor Posted Write is enabled.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:2	0h RW	**Transmit Arbitration Algorithm (TAA):** This field is used to select the arbitration algorithm for the Transmit side when multiple Tx DMAs are selected. 0x0 (FP): Fixed priority (Channel 0 has the lowest priority and the last channel has the highest priority). 0x1 (WSP): Weighted Strict Priority (WSP). 0x2 (WRR): Weighted Round-Robin (WRR). 0x3 (RSVD): Reserved (for 3'b011 to 3'b111).
1	0h RO	**Reserved**
0	0h RW	**Software Reset (SWR):** When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all GbE Controller clock domains. Before reprogramming any GbE Controller register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Software Reset is disabled. 0x1 (ENABLE): Software Reset is enabled.

3.2.477 DMA_SYSBUS_MODE — Offset 1004h

The System Bus mode register controls the behavior of the AHB or AXI master. It mainly controls burst splitting and number of outstanding requests.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	01010000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Low Power Interface (LPI) (EN_LPI):** When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. 0x0 (DISABLE): Low Power Interface (LPI) is disabled. 0x1 (ENABLE): Low Power Interface (LPI) is enabled.
30	0h RW	**Unlock on Magic Packet or Remote Wake-Up Packet (LPI_XIT_PKT):** When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. 0x0 (DISABLE): Unlock on Magic Packet or Remote Wake-Up Packet is disabled. 0x1 (ENABLE): Unlock on Magic Packet or Remote Wake-Up Packet is enabled.
29:28	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
27:24	1h RW	**AXI Maximum Write Outstanding Request Limit (WR_OSR_LMT):** This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1
23:20	0h RO	**Reserved**
19:16	1h RW	**AXI Maximum Read Outstanding Request Limit (RD_OSR_LMT):** This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1
15:14	0h RO	**Reserved**
13	0h RW	**1 KB Boundary Crossing Enable for the EQOS-AXI Master (ONEKBBE):** When set, the burst transfers performed by the EQOS-AXI master do not cross 1 KB boundary. When reset, the burst transfers performed by the EQOS-AXI master do not cross 4 KB boundary. 0x0 (DISABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is disabled. 0x1 (ENABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is enabled.
12	0h RW	**Address-Aligned Beats (AAL):** When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. 0x0 (DISABLE): Address-Aligned Beats is disabled. 0x1 (ENABLE): Address-Aligned Beats is enabled.
11	0h RW	**Enhanced Address Mode Enable. (EAME):** When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. 0x0 (DISABLE): Enhanced Address Mode is disabled. 0x1 (ENABLE): Enhanced Address Mode is enabled.
10	0h RW	**Automatic AXI LPI enable (AALE):** When set to 1, enables the AXI master to enter into LPI state when there is no activity in the GbE Controller for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. 0x0 (DISABLE): Automatic AXI LPI is disabled. 0x1 (ENABLE): Automatic AXI LPI is enabled.
9:8	0h RO	**Reserved**
7	0h RW	**AXI Burst Length 256 (BLEN256):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 256 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 256.
6	0h RW	**AXI Burst Length 128 (BLEN128):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 128 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 128.
5	0h RW	**AXI Burst Length 64 (BLEN64):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 64 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 64.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**AXI Burst Length 32 (BLEN32):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 32 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 32.
3	0h RW	**AXI Burst Length 16 (BLEN16):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 16.
2	0h RW	**AXI Burst Length 8 (BLEN8):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 8.
1	0h RW	**AXI Burst Length 4 (BLEN4):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 4.
0	0h RW	**FB:** Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. - Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field - Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. 0x0 (DISABLE): Fixed Burst Length is disabled. 0x1 (ENABLE): Fixed Burst Length is enabled.

3.2.478 DMA_INTERRUPT_STATUS — Offset 1008h

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO	**MAC Interrupt Status (MACIS):** This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MAC Interrupt Status not detected. 0x1 (ACTIVE): MAC Interrupt Status detected.
16	0h RO	**MTL Interrupt Status (MTLIS):** This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Interrupt Status not detected. 0x1 (ACTIVE): MTL Interrupt Status detected.
15:8	0h RO	**Reserved**
7	0h RO	**DMA Channel 7 Interrupt Status (DC7IS):** This bit indicates an interrupt event in DMA Channel 7. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 7 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 7 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 7 Interrupt Status detected.
6	0h RO	**DMA Channel 6 Interrupt Status (DC6IS):** This bit indicates an interrupt event in DMA Channel 6. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 6 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 6 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 6 Interrupt Status detected.
5	0h RO	**DMA Channel 5 Interrupt Status (DC5IS):** This bit indicates an interrupt event in DMA Channel 5. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 5 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 5 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 5 Interrupt Status detected.
4	0h RO	**DMA Channel 4 Interrupt Status (DC4IS):** This bit indicates an interrupt event in DMA Channel 4. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 4 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 4 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 4 Interrupt Status detected.
3	0h RO	**DMA Channel 3 Interrupt Status (DC3IS):** This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 3 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 3 Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**DMA Channel 2 Interrupt Status (DC2IS):** This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 2 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 2 Interrupt Status detected.
1	0h RO	**DMA Channel 1 Interrupt Status (DC1IS):** This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 1 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 1 Interrupt Status detected.
0	0h RO	**DMA Channel 0 Interrupt Status (DC0IS):** This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 0 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 0 Interrupt Status detected.

3.2.479 DMA_DEBUG_STATUS0 — Offset 100Ch

The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 2 Transmit Process State (TPS2):** This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 2 Receive Process State (RPS2):** This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 1 Transmit Process State (TPS1):** This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
19:16	0h RO	**DMA Channel 1 Receive Process State (RPS1):** This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**DMA Channel 0 Transmit Process State (TPS0):** This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
11:8	0h RO	**DMA Channel 0 Receive Process State (RPS0):** This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:2	0h RO	**Reserved**
1	0h RO	**AXI Master Read Channel Status (AXRHSTS):** When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. 0x0 (INACTIVE): AXI Master Read Channel Status not detected. 0x1 (ACTIVE): AXI Master Read Channel Status detected.
0	0h RO	**AXI Master Write Channel (AXWHSTS):** When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. 0x0 (INACTIVE): AXI Master Write Channel or AHB Master Status not detected. 0x1 (ACTIVE): AXI Master Write Channel or AHB Master Status detected.

3.2.480 DMA_DEBUG_STATUS1 — Offset 1010h

The Debug Status1 register gives the Receive and Transmit process status for DMA Channel 3-Channel 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 6 Transmit Process State (TPS6):** This field indicates the Tx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 6 Receive Process State (RPS6):** This field indicates the Rx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 5 Transmit Process State (TPS5):** This field indicates the Tx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
19:16	0h RO	**DMA Channel 5 Receive Process State (RPS5):** This field indicates the Rx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**DMA Channel 4 Transmit Process State (TPS4):** This field indicates the Tx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
11:8	0h RO	**DMA Channel 4 Receive Process State (RPS4):** This field indicates the Rx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:4	0h RO	**DMA Channel 3 Transmit Process State (TPS3):** This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 3 Receive Process State (RPS3):** This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

3.2.481 DMA_DEBUG_STATUS2 — Offset 1014h

The Debug Status Register 2 gives the Receive and Transmit process status for DMA Channel 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1014h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	0h RO	**DMA Channel 7 Transmit Process State (TPS7):** This field indicates the Tx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 7 Receive Process State (RPS7):** This field indicates the Rx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

3.2.482 AXI4_TX_AR_ACE_CONTROL — Offset 1020h

This register is used to control the AXI4 Cache Coherency Signals for read transactions by all the Transmit DMA channels. The following signals of the AXI4 interface are driven with different values as programmed

for corresponding type (descriptor, buffer1, buffer2) of access.

- arcache_m_o[3:0]

- ardomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:20	0h RW	**Transmit DMA First Packet Buffer or TSO Header Domain Control (THD):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO Header data.
19:16	0h RW	**Transmit DMA First Packet Buffer or TSO Header Cache Control (THC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO Header data.
15:14	0h RO	**Reserved**
13:12	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Domain Control (TED):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO payload data.
11:8	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Cache Control (TEC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO payload data.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Read Descriptor Domain Control (TDRD):** This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the Descriptor.
3:0	0h RW	**Transmit DMA Read Descriptor Cache Control (TDRC):** This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor.

3.2.483 AXI4_RX_AW_ACE_CONTROL — Offset 1024h

This register is used to control the AXI4 Cache Coherency Signals for write transactions by all the Receive DMA channels. The following signals of the AXI4 interface are driven with different values as programmed

for corresponding type (descriptor, buffer1, buffer2) of access.

- awcache_m_o[3:0]

- awdomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Receive DMA Buffer Domain Control (RDD):** This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
27:24	0h RW	**Receive DMA Buffer Cache Control (RDC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
23:22	0h RO	**Reserved**
21:20	0h RW	**Receive DMA Header Domain Control (RHD):** This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
19:16	0h RW	**Receive DMA Header Cache Control (RHC):** This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Payload Domain Control (RPD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
11:8	0h RW	**Receive DMA Payload Cache Control (RPC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
7:6	0h RO	**Reserved**
5:4	0h RW	**Receive DMA Write Descriptor Domain Control (RDWD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor.
3:0	0h RW	**Receive DMA Write Descriptor Cache Control (RDWC):** This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor.

3.2.484 AXI4_TXRX_AWAR_ACE_CONTROL — Offset 1028h

This register is used to control the AXI4 Cache Coherency Signals for Descriptor write transactions by all the TxDMA channels and Descriptor read transactions by all the RxDMA channels. It also controls the values to be driven on awprot_m_o and arprot_m_o.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RW	**DMA Write Protection control (WRP):** This field is used to drive awprot_m_o[2:0] signal on the AXI Write Channel.
19	0h RO	**Reserved**
18:16	0h RW	**DMA Read Protection control (RDP):** This field is used to drive arprot_m_o[2:0] signal during all read requests.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Read Descriptor Domain control (RDRD):** This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor.
11:8	0h RW	**Receive DMA Read Descriptor Cache control (RDRC):** This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Write Descriptor Domain control (TDWD):** This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor.
3:0	0h RW	**Transmit DMA Write Descriptor Cache control (TDWC):** This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor.

3.2.485 AXI_LPI_ENTRY_INTERVAL — Offset 1040h

This register is used to control the AXI LPI entry interval.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**LPI Entry Interval (LPIEI):** Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the GbE Controller to enter into the AXI low power state 0 indicates 64 clock cycles

3.2.486 DMA_TBS_CTRL0 — Offset 1050h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

3.2.487 DMA_TBS_CTRL1 — Offset 1054h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

3.2.488 DMA_TBS_CTRL2 — Offset 1058h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

3.2.489 DMA_TBS_CTRL3 — Offset 105Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 105Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

3.2.490 DMA_SAFETY_INTERRUPT_STATUS — Offset 1080h

This register indicates summary (whether error occured in DMA/MTL/MAC and correctable/uncorrectable) of the Automotive Safety related error interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**MAC Safety Uncorrectable Interrupt Status (MCSIS):** Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC. 0x0 (INACTIVE): MAC Safety Uncorrectable Interrupt Status not detected. 0x1 (ACTIVE): MAC Safety Uncorrectable Interrupt Status detected.
30	0h RO	**Reserved**
29	0h RO	**MTL Safety Uncorrectable error Interrupt Status (MSUIS):** This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Uncorrectable error Interrupt Status detected.
28	0h RO	**MTL Safety Correctable error Interrupt Status (MSCIS):** This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Correctable error Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
27:2	0h RO	**Reserved**
1	0h RO	**DMA ECC Uncorrectable error Interrupt Status (DEUIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**DMA ECC Correctable error Interrupt Status (DECIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Correctable error Interrupt Status detected.

3.2.491 DMA_ECC_INTERRUPT_ENABLE — Offset 1084h

This register is used to enable the Automotive Safety related TSO memory ECC error interrupt.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TSO memory Correctable Error Interrupt Enable (TCEIE):** When set, generates an interrupt when a correctable error is detected at the DMA TSO memory interface. It is indicated in the TCES bit of DMA_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): TSO memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): TSO memory Correctable Error Interrupt is enabled.

3.2.492 DMA_ECC_INTERRUPT_STATUS — Offset 1088h

This register indicates the Automotive Safety related TSO memory ECC error interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1088h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**DMA TSO memory Uncorrectable Error status (TUES):** When set, indicates that an uncorrectable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Uncorrectable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Uncorrectable Error status detected.
1	0h RW	**DMA TSO memory Address Mismatch status (TAMS):** This bit when set indicates that address mismatch is found for address bus of DMA TSO memory. 0x0 (INACTIVE): DMA TSO memory Address Mismatch status not detected. 0x1 (ACTIVE): DMA TSO memory Address Mismatch status detected.
0	0h RW	**DMA TSO memory Correctable Error status (TCES):** This bit when set indicates that correctable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Correctable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Correctable Error status detected.

3.2.493 DMA_CH0_CONTROL — Offset 1100h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

3.2.494 DMA_CH0_TX_CONTROL — Offset 1104h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.495 DMA_CH0_RX_CONTROL — Offset 1108h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.496 DMA_CH0_TXDESC_LIST_HADDRESS — Offset 1110h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.497 DMA_CH0_TXDESC_LIST_ADDRESS — Offset 1114h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.498 DMA_CH0_RXDESC_LIST_HADDRESS — Offset 1118h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.499 DMA_CH0_RXDESC_LIST_ADDRESS — Offset 111Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 111Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.500 DMA_CH0_TXDESC_TAIL_POINTER — Offset 1120h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.501 DMA_CH0_RXDESC_TAIL_POINTER — Offset 1128h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.502 DMA_CH0_TXDESC_RING_LENGTH — Offset 112Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 112Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.503 DMA_CH0_RXDESC_RING_LENGTH — Offset 1130h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.504 DMA_CH0_INTERRUPT_ENABLE — Offset 1134h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.505 DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1138h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.506 DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS — Offset 113Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 113Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.507 DMA_CH0_CURRENT_APP_TXDESC — Offset 1144h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.508 DMA_CH0_CURRENT_APP_RXDESC — Offset 114Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.509 DMA_CH0_CURRENT_APP_TXBUFFER_H — Offset 1150h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.510 DMA_CH0_CURRENT_APP_TXBUFFER — Offset 1154h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.511 DMA_CH0_CURRENT_APP_RXBUFFER_H — Offset 1158h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.512 DMA_CH0_CURRENT_APP_RXBUFFER — Offset 115Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 115Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.513 DMA_CH0_STATUS — Offset 1160h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.514 DMA_CH0_MISS_FRAME_CNT — Offset 1164h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.515 DMA_CH0_RXP_ACCEPT_CNT — Offset 1168h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.516 DMA_CH0_RX_ERI_CNT — Offset 116Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 116Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.517 DMA_CH1_CONTROL — Offset 1180h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

3.2.518 DMA_CH1_TX_CONTROL — Offset 1184h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.519 DMA_CH1_RX_CONTROL — Offset 1188h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.520 DMA_CH1_TXDESC_LIST_HADDRESS — Offset 1190h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.521 DMA_CH1_TXDESC_LIST_ADDRESS — Offset 1194h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1194h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.522 DMA_CH1_RXDESC_LIST_HADDRESS — Offset 1198h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.523 DMA_CH1_RXDESC_LIST_ADDRESS — Offset 119Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 119Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.524 DMA_CH1_TXDESC_TAIL_POINTER — Offset 11A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.525 DMA_CH1_RXDESC_TAIL_POINTER — Offset 11A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.526 DMA_CH1_TXDESC_RING_LENGTH — Offset 11ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.527 DMA_CH1_RXDESC_RING_LENGTH — Offset 11B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.528 DMA_CH1_INTERRUPT_ENABLE — Offset 11B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.529 DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER — Offset 11B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.530 DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS — Offset 11BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.531 DMA_CH1_CURRENT_APP_TXDESC — Offset 11C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.532 DMA_CH1_CURRENT_APP_RXDESC — Offset 11CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.533 DMA_CH1_CURRENT_APP_TXBUFFER_H — Offset 11D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.534 DMA_CH1_CURRENT_APP_TXBUFFER — Offset 11D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.535 DMA_CH1_CURRENT_APP_RXBUFFER_H — Offset 11D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.536 DMA_CH1_CURRENT_APP_RXBUFFER — Offset 11DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.537 DMA_CH1_STATUS — Offset 11E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.538 DMA_CH1_MISS_FRAME_CNT — Offset 11E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.539 DMA_CH1_RXP_ACCEPT_CNT — Offset 11E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.540 DMA_CH1_RX_ERI_CNT — Offset 11ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.541 DMA_CH2_CONTROL — Offset 1200h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

3.2.542 DMA_CH2_TX_CONTROL — Offset 1204h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.543 DMA_CH2_RX_CONTROL — Offset 1208h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.544 DMA_CH2_TXDESC_LIST_HADDRESS — Offset 1210h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.545 DMA_CH2_TXDESC_LIST_ADDRESS — Offset 1214h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.546 DMA_CH2_RXDESC_LIST_HADDRESS — Offset 1218h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.547 DMA_CH2_RXDESC_LIST_ADDRESS — Offset 121Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 121Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.548 DMA_CH2_TXDESC_TAIL_POINTER — Offset 1220h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.549 DMA_CH2_RXDESC_TAIL_POINTER — Offset 1228h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.550 DMA_CH2_TXDESC_RING_LENGTH — Offset 122Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 122Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.551 DMA_CH2_RXDESC_RING_LENGTH — Offset 1230h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.552 DMA_CH2_INTERRUPT_ENABLE — Offset 1234h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1234h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.553 DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1238h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.554 DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS — Offset 123Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 123Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.555 DMA_CH2_CURRENT_APP_TXDESC — Offset 1244h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.556 DMA_CH2_CURRENT_APP_RXDESC — Offset 124Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.557 DMA_CH2_CURRENT_APP_TXBUFFER_H — Offset 1250h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1250h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.558 DMA_CH2_CURRENT_APP_TXBUFFER — Offset 1254h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1254h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.559 DMA_CH2_CURRENT_APP_RXBUFFER_H — Offset 1258h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1258h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.560 DMA_CH2_CURRENT_APP_RXBUFFER — Offset 125Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 125Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.561 DMA_CH2_STATUS — Offset 1260h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1260h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.562 DMA_CH2_MISS_FRAME_CNT — Offset 1264h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1264h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.563 DMA_CH2_RXP_ACCEPT_CNT — Offset 1268h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1268h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.564 DMA_CH2_RX_ERI_CNT — Offset 126Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 126Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.565 DMA_CH3_CONTROL — Offset 1280h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1280h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

3.2.566 DMA_CH3_TX_CONTROL — Offset 1284h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1284h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.567 DMA_CH3_RX_CONTROL — Offset 1288h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1288h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.568 DMA_CH3_TXDESC_LIST_HADDRESS — Offset 1290h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1290h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.569 DMA_CH3_TXDESC_LIST_ADDRESS — Offset 1294h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1294h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.570 DMA_CH3_RXDESC_LIST_HADDRESS — Offset 1298h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1298h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.571 DMA_CH3_RXDESC_LIST_ADDRESS — Offset 129Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 129Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.572 DMA_CH3_TXDESC_TAIL_POINTER — Offset 12A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.573 DMA_CH3_RXDESC_TAIL_POINTER — Offset 12A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.574 DMA_CH3_TXDESC_RING_LENGTH — Offset 12ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.575 DMA_CH3_RXDESC_RING_LENGTH — Offset 12B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.576 DMA_CH3_INTERRUPT_ENABLE — Offset 12B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.577 DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER — Offset 12B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.578 DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS — Offset 12BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.579 DMA_CH3_CURRENT_APP_TXDESC — Offset 12C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.580 DMA_CH3_CURRENT_APP_RXDESC — Offset 12CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.581 DMA_CH3_CURRENT_APP_TXBUFFER_H — Offset 12D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.582 DMA_CH3_CURRENT_APP_TXBUFFER — Offset 12D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.583 DMA_CH3_CURRENT_APP_RXBUFFER_H — Offset 12D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.584 DMA_CH3_CURRENT_APP_RXBUFFER — Offset 12DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.585 DMA_CH3_STATUS — Offset 12E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.586 DMA_CH3_MISS_FRAME_CNT — Offset 12E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.587 DMA_CH3_RXP_ACCEPT_CNT — Offset 12E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.588 DMA_CH3_RX_ERI_CNT — Offset 12ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.589 DMA_CH4_CONTROL — Offset 1300h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1300h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

3.2.590 DMA_CH4_TX_CONTROL — Offset 1304h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1304h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.591 DMA_CH4_RX_CONTROL — Offset 1308h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1308h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.592 DMA_CH4_TXDESC_LIST_HADDRESS — Offset 1310h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1310h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.593 DMA_CH4_TXDESC_LIST_ADDRESS — Offset 1314h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1314h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.594 DMA_CH4_RXDESC_LIST_HADDRESS — Offset 1318h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1318h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.595 DMA_CH4_RXDESC_LIST_ADDRESS — Offset 131Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 131Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.596 DMA_CH4_TXDESC_TAIL_POINTER — Offset 1320h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1320h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.597 DMA_CH4_RXDESC_TAIL_POINTER — Offset 1328h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1328h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.598 DMA_CH4_TXDESC_RING_LENGTH — Offset 132Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 132Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.599 DMA_CH4_RXDESC_RING_LENGTH — Offset 1330h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1330h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.600 DMA_CH4_INTERRUPT_ENABLE — Offset 1334h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1334h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.601 DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1338h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1338h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.602 DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS — Offset 133Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 133Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.603 DMA_CH4_CURRENT_APP_TXDESC — Offset 1344h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1344h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.604 DMA_CH4_CURRENT_APP_RXDESC — Offset 134Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 134Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.605 DMA_CH4_CURRENT_APP_TXBUFFER_H — Offset 1350h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1350h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.606 DMA_CH4_CURRENT_APP_TXBUFFER — Offset 1354h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1354h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.607 DMA_CH4_CURRENT_APP_RXBUFFER_H — Offset 1358h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1358h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.608 DMA_CH4_CURRENT_APP_RXBUFFER — Offset 135Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 135Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.609 DMA_CH4_STATUS — Offset 1360h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1360h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.610 DMA_CH4_MISS_FRAME_CNT — Offset 1364h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1364h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.611 DMA_CH4_RXP_ACCEPT_CNT — Offset 1368h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1368h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.612 DMA_CH4_RX_ERI_CNT — Offset 136Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 136Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.613 DMA_CH5_CONTROL — Offset 1380h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1380h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

3.2.614 DMA_CH5_TX_CONTROL — Offset 1384h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1384h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.615 DMA_CH5_RX_CONTROL — Offset 1388h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1388h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.616 DMA_CH5_TXDESC_LIST_HADDRESS — Offset 1390h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1390h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.617 DMA_CH5_TXDESC_LIST_ADDRESS — Offset 1394h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1394h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.618 DMA_CH5_RXDESC_LIST_HADDRESS — Offset 1398h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1398h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.619 DMA_CH5_RXDESC_LIST_ADDRESS — Offset 139Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 139Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.620 DMA_CH5_TXDESC_TAIL_POINTER — Offset 13A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.621 DMA_CH5_RXDESC_TAIL_POINTER — Offset 13A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.622 DMA_CH5_TXDESC_RING_LENGTH — Offset 13ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.623 DMA_CH5_RXDESC_RING_LENGTH — Offset 13B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.624 DMA_CH5_INTERRUPT_ENABLE — Offset 13B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.625 DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER — Offset 13B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.626 DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS — Offset 13BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.627 DMA_CH5_CURRENT_APP_TXDESC — Offset 13C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.628 DMA_CH5_CURRENT_APP_RXDESC — Offset 13CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.629 DMA_CH5_CURRENT_APP_TXBUFFER_H — Offset 13D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.630 DMA_CH5_CURRENT_APP_TXBUFFER — Offset 13D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.631 DMA_CH5_CURRENT_APP_RXBUFFER_H — Offset 13D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.632 DMA_CH5_CURRENT_APP_RXBUFFER — Offset 13DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.633 DMA_CH5_STATUS — Offset 13E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.634 DMA_CH5_MISS_FRAME_CNT — Offset 13E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.635 DMA_CH5_RXP_ACCEPT_CNT — Offset 13E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.636 DMA_CH5_RX_ERI_CNT — Offset 13ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.637 DMA_CH6_CONTROL — Offset 1400h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1400h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

3.2.638 DMA_CH6_TX_CONTROL — Offset 1404h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1404h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.639 DMA_CH6_RX_CONTROL — Offset 1408h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1408h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.640 DMA_CH6_TXDESC_LIST_HADDRESS — Offset 1410h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1410h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.641 DMA_CH6_TXDESC_LIST_ADDRESS — Offset 1414h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1414h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.642 DMA_CH6_RXDESC_LIST_HADDRESS — Offset 1418h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1418h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.643 DMA_CH6_RXDESC_LIST_ADDRESS — Offset 141Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 141Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.644 DMA_CH6_TXDESC_TAIL_POINTER — Offset 1420h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1420h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.645 DMA_CH6_RXDESC_TAIL_POINTER — Offset 1428h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1428h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.646 DMA_CH6_TXDESC_RING_LENGTH — Offset 142Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 142Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.647 DMA_CH6_RXDESC_RING_LENGTH — Offset 1430h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1430h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.648 DMA_CH6_INTERRUPT_ENABLE — Offset 1434h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1434h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.649 DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER — Offset 1438h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1438h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.650 DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS — Offset 143Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 143Ch	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.651 DMA_CH6_CURRENT_APP_TXDESC — Offset 1444h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1444h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.652 DMA_CH6_CURRENT_APP_RXDESC — Offset 144Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.653 DMA_CH6_CURRENT_APP_TXBUFFER_H — Offset 1450h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1450h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.654 DMA_CH6_CURRENT_APP_TXBUFFER — Offset 1454h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1454h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.655 DMA_CH6_CURRENT_APP_RXBUFFER_H — Offset 1458h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1458h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.656 DMA_CH6_CURRENT_APP_RXBUFFER — Offset 145Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 145Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.657 DMA_CH6_STATUS — Offset 1460h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1460h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.658 DMA_CH6_MISS_FRAME_CNT — Offset 1464h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1464h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.659 DMA_CH6_RXP_ACCEPT_CNT — Offset 1468h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1468h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.660 DMA_CH6_RX_ERI_CNT — Offset 146Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 146Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.2.661 DMA_CH7_CONTROL — Offset 1480h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1480h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

3.2.662 DMA_CH7_TX_CONTROL — Offset 1484h

The DMA Channel Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1484h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**TFSEL:**
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

3.2.663 DMA_CH7_RX_CONTROL — Offset 1488h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1488h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

3.2.664 DMA_CH7_TXDESC_LIST_HADDRESS — Offset 1490h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1490h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

3.2.665 DMA_CH7_TXDESC_LIST_ADDRESS — Offset 1494h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1494h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.666 DMA_CH7_RXDESC_LIST_HADDRESS — Offset 1498h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list.

Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1498h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

3.2.667 DMA_CH7_RXDESC_LIST_ADDRESS — Offset 149Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list.

This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 149Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.668 DMA_CH7_TXDESC_TAIL_POINTER — Offset 14A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.669 DMA_CH7_RXDESC_TAIL_POINTER — Offset 14A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

3.2.670 DMA_CH7_TXDESC_RING_LENGTH — Offset 14ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.671 DMA_CH7_RXDESC_RING_LENGTH — Offset 14B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

3.2.672 DMA_CH7_INTERRUPT_ENABLE — Offset 14B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

3.2.673 DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER — Offset 14B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

3.2.674 DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS — Offset 14BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14BCh	000007C0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

3.2.675 DMA_CH7_CURRENT_APP_TXDESC — Offset 14C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.676 DMA_CH7_CURRENT_APP_RXDESC — Offset 14CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.677 DMA_CH7_CURRENT_APP_TXBUFFER_H — Offset 14D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.678 DMA_CH7_CURRENT_APP_TXBUFFER — Offset 14D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

3.2.679 DMA_CH7_CURRENT_APP_RXBUFFER_H — Offset 14D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.680 DMA_CH7_CURRENT_APP_RXBUFFER — Offset 14DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

3.2.681 DMA_CH7_STATUS — Offset 14E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

3.2.682 DMA_CH7_MISS_FRAME_CNT — Offset 14E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

3.2.683 DMA_CH7_RXP_ACCEPT_CNT — Offset 14E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

3.2.684 DMA_CH7_RX_ERI_CNT — Offset 14ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

3.3 PHY Sublayer Registers Accessible via the MDIO Interface Controller

The Management Data Input/Output (MDIO) Interface is defined in IEEE Standard 802.3-2018:

Clause 22 – Chapter 22.2.4 of the IEEE standard specifies the MDIO interface and registers. The MAC device controlling the MDIO is called the Station Management (STA) entity. The STA issues MDIO frames that have the 2-bit, start-of-frame Symbol Time (ST) code of 01 to access registers. See Table below for the Clause 22 frame format and terminology.

Clause 45 – See Chapter 45 of the IEEE standard. This MDIO interface and register format are extensions to the two-signal MDIO Interface specified in Clause 22. For Clause 45, additional registers are added to the address space by defining MDIO frames that use a start-of-frame Symbol Time (ST) code of 00. See Table below for the Clause 45 frame format and terminology.

The TSN-GbE Controller supports both formats. The C45E bit (bit 1) of the MAC_MDIO_Address register at MMIO offset 200h can be programmed to select the Clause 22 or Clause 45 mode of operation of the STA for the particular MDIO frame. The C45E bit must be programmed to support the capability of the PHY that is connected to MDIO.

The PHY sublayer, or grouping of sublayers, is an individually manageable entity referred to as an MDIO Manageable Device (MMD).

Table 3-3. MDIO Clause 22 Management Frame Format

Operation	32-bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	PHY Address (PHYAD)	PHY Register Address (REGAD)	2-Bit Turn-around (TA) Time	Data (16 bits)	High-Z (Idle)
Write	1111...1	01	01	AAAAA	RRRRR	10	16-bit Data to be written to the register	Z
Read	1111...1	01	10	AAAAA	RRRRR	Z0	16-bit Data read from the register	Z

For the Clause 22 frame, the PHY Address (PHYAD) selects one of 32 PHYs attached to the MDIO interface. The PHY Register Address (REGAD) selects one of 32 16-bit registers within each MMD.

Table 3-4. MDIO Clause 45 Management Frame Format

Operation	32-bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	Port Address (PRTAD)	Device Address (DEVAD)	2-Bit Turn-around (TA) Time	Address /Data (16 bits)	High-Z (Idle)
Address	1111...1	00	00	PPPPP	EEEEE	Z0	16-bit Address of the register to be accessed on the next cycle	Z
Write	1111...1	00	01	PPPPP	EEEEE	Z0	16-bit Data to be written to the register	Z
Post-Read-Increment Address	1111...1	00	10	PPPPP	EEEEE	Z0	16-bit Data read from the register	Z
Read	1111...1	00	11	PPPPP	EEEEE	Z0	16-bit Data read from the register	Z

For the Clause 45 frame, the Port Address (PRTAD) selects one of 32 Ports attached to the MDIO interface. The Device Address (DEVAD) selects one of 32 unique MDDs per Port. Notice that the register address and register data are separate MDIO frames.

3.3.1 MDIO – PCS PHY Sublayer Registers – PHY Port Address 16h

The MAC uses the GMII as the data interface to the PHY sublayers of the Ethernet LAN Controller including the Physical Coding Sublayer (PCS). The MAC uses the MDIO as the configuration and management interface to the PHY sublayers. This section describes the PCS MDIO registers which follow the IEEE 802.3 standard register sets for the different MMIO Management Devices (MMD).

The PCS PHY sublayer is an IEEE Std 802.3 Clause-45-capable MDIO entity with the following IEEE 802.3 MDIO frame fields:

- Start-of-Frame Symbol Time (ST) 2-bit code: 00b – Indicates a Clause 45 MDIO frame.
- Port Address (PRTAD) 5-bit ID: 10110b (16h) – This Port contains two MMDs:

- MMD (DEVAD) 5-bit ID: 11110b (1Eh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h though 000Fh. This MMD is named Vendor-Specific 1 (Control MMD). The registers are used to control the other MMDs of the LAN Controller.
- MMD (DEVAD) 5-bit ID: 11111b (1Fh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h though 0E2h. This MMD is named Vendor-Specific MII MMD (VR MII MMD).

Table 3-5. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Eh

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
0000	16	SR Control MMD PMA Device Identifier Register 1 (SR_VSMMD_PMA_ID1)	0000h
0001	16	SR Control MMD PMA Device Identifier Register 2 (SR_VSMMD_PMA_ID2)	0000h
0002	16	SR Control MMD Device Identifier Register 1 (SR_VSMMD_DEV_ID1)	0000h
0003	16	SR Control MMD Device Identifier Register 2 (SR_VSMMD_DEV_ID2)	000h
0004	16	SR Control MMD PCS Device Identifier Register 1 (SR_VSMMD_PCS_ID1)	7996h
0005	16	SR Control MMD PCS Device Identifier Register 2 (SR_VSMMD_PCS_ID2)	CED0h
0006	16	SR Control MMD AN Device Identifier Register 1 (SR_VSMMD_AN_ID1)	0000h
0007	16	SR Control MMD AN Device Identifier Register 2 (SR_VSMMD_AN_ID2)	0000h
0008	16	SR Control MMD Status Register (SR_VSMMD_STS)	8000h
0009	16	SR Control MMD Control Register (SR_VSMMD_CTRL)	0004h
000E	16	SR Control MMD Package Identifier Register 1 (SR_VSMMD_PKGID1)	0000h
000F	16	SR Control MMD Package Identifier Register 2 (SR_VSMMD_PKGID2)	0000h

Table 3-6. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Fh

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
0000	16	SR MII MMD Control Register (SR_MII_CTRL)	1140h
0001	16	SR MII MMD Status Register (SR_MII_STS)	0189h
0002	16	SR MII MMD Device Identifier Register 1 (SR_MII_DEV_ID1)	7996h
0003	16	SR MII MMD Device Identifier Register 2 (SR_MII_DEV_ID2)	CED0h
0004	16	SR MII MMD AN Advertisement Register (SR_MII_AN_ADV)	0020h
0005	16	SR MII MMD AN Link Partner Base Ability Register (SR_MII_LP_BABL)	0000h

Table 3-6. Summary of PCS MDIO Registers, PRTAD = 16h, DEVAD = 1Fh

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
0006	16	SR MII MMD AN Expansion Register (SR_MII_AN_EXPN)	0000h
000F	16	SR MII MMD Extended Status Register (SR_MII_EXT_STS)	C000h
0708	16	SR MII MMD Time Sync Capability Register (SR_MII_TIME_SYNC_ABL)	0003h
0709	16	SR MII MMD Time Sync Tx Max Delay Lower Register (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR)	0038h
070A	16	SR MII MMD Time Sync Tx Max Delay Upper Register (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR)	0000h
070B	16	SR MII MMD Time Sync Tx Min Delay Lower Register (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR)	0038h
070C	16	SR MII MMD Time Sync Tx Min Delay Upper Register (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR)	0000h
070D	16	SR MII MMD Time Sync Rx Max Delay Lower Register (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR)	00B8h
070E	16	SR MII MMD Time Sync Rx Max Delay Upper Register (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR)	0000h
070F	16	SR MII MMD Time Sync Rx Min Delay Lower Register (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR)	0088h
0710	16	SR MII MMD Time Sync Rx Min Delay Upper Register (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR)	0000h
8000	16	VR MII MMD Digital Control1 Register (VR_MII_DIG_CTRL1)	2400h
8001	16	VR MII MMD AN Control Register (VR_MII_AN_CTRL)	0000h
8002	16	VR MII MMD AN Interrupt and Status Register (VR_MII_AN_INTR_STS)	000Ah
8003	16	VR MII MMD Test Control Register (VR_MII_TC)	0000h
8005	16	VR MII MMD Debug Control Register (VR_MII_DBG_CTRL)	0000h
8006	16	VR MII MMD EEE Mode Control Register (VR_MII_EEE_MCTRL0)	899Ch
8008	16	VR MII MMD EEE Tx Timer Register (VR_MII_EEE_TXTIMER)	0000h
8009	16	VR MII MMD EEE Rx Timer Register (VR_MII_EEE_RXTIMER)	0000h
800A	16	VVR MII MMD Link Timer Control Register (VR_MII_LINK_TIMER_CTRL)	0000h
800B	16	VR MII MMD EEE Mode Control 1 Register (VR_MII_EEE_MCTRL1)	0000h
8010	16	VR MII MMD Digital Status Register (VR_MII_DIG_STS)	0000h
8011	16	VR MII MMD Invalid Code Group Error Count1 Register (VR_MII_ICG_ERRCNT1)	0000h
8018	16	VR MII MMD Miscellaneous Status Register (VR_MII_MISC_STS)	0000h
8020	16	VR MII PHY Rx Lane Status Register (VR_MII_RX_LSTS)	0000h
80E1	16	VR MII MMD Digital Control2 Register (VR_MII_DIG_CTRL2)	0000h
80E2	16	VR MII MMD Digital Error Count Select Register (VR_MII_DIG_ERRCNT_SEL)	0000h

3.3.1.1 SR Control MMD PMA Device Identifier Register 1 (SR_VSMMD_PMA_ID1) - 1Eh, Address 0000h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0000h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	0000h	Reserved

3.3.1.2 SR Control MMD PMA Device Identifier Register 2 (SR_VSMMD_PMA_ID2) - 1Eh, Address 0001h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0001h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	0000h	Reserved

3.3.1.3 SR Control MMD Device Identifier Register 1(SR_VSMMD_DEV_ID1) - 1Eh, Address 0002h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0002h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	0000h	Organizationally Unique Identifier [3:18] for Vendor-Specific MMD1 (VSDOUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific MMD1 for identifying the device manufacturer.

3.3.1.4 SR Control MMD Device Identifier Register 2 (SR_VSMMD_DEV_ID2) - 1Eh, Address 0003h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0003h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:10	RW	00h	Organizationally Unique Identifier[19:24] for Vendor-Specific MMD1 (VSDOUI_19_24): Bits 24:19 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific MMD1 for identifying the device manufacturer.
9:4	RW	00h	Model Number for Vendor-Specific MMD1 (VSDMMN_5_0): 6-bit Model number of the vendor-specific MMD1.
3:0	RW	0h	Revision Number for Vendor-Specific MMD1 (VSDRN_3_0): 4-bit Revision number of the vendor-specific MMD1.

3.3.1.5 SR Control MMD PCS Device Identifier Register 1 (SR_VSMMD_PCS_ID1) - 1Eh, Address 0004h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0004h**

Default: 7996h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	7996h	Organizationally Unique Identifier[3:18] for PCS MMD (PCSDOUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific PCS MMD for identifying the device manufacturer.

3.3.1.6 SR Control MMD PCS Device Identifier Register 2 (SR_VSMMD_PCS_ID2) - 1Eh, Address 0005h

This register is RW by software via the MDIO interface. The 24-bit Device Organizationally Unique Identifier (OUI) is default-set to CDA679h. The Model Number default value is 2Dh and the Revision Number default is 0.SR Control MMD AN Device.

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0005h**

Default: CED0h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:10	RW	33h	Organizationally Unique Identifier[19:24] for PCS MMD (PCSDOUI_19_24): Bits 24:19 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific PCS MMD for identifying the device manufacturer.
9:4	RW	2Dh	Model Number for PCS MMD (PCSDMMN_5_0): 6-bit Model number of the vendor-specific PCS MMD.
3:0	RW	0h	Revision Number for PCS MMD (PCSDRN_3_0): 4-bit Revision number of the vendor-specific PCS MMD.

3.3.1.7 SR Control MMD AN Device Identifier Register 1 (SR_VSMMD_AN_ID1) - 1Eh, Address 0006h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0006h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	0000h	Organizationally Unique Identifier [3:18] for Vendor-Specific MMD1 (VSDOUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) for the vendor-specific MMD1 for identifying the device manufacturer.

3.3.1.8 SR Control MMD AN Device Identifier Register 2 (SR_VSMMD_AN_ID2) - 1Eh, Address 0007h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0007h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	0000h	Reserved

3.3.1.9 SR Control MMD Status Register (SR_VSMMD_STS) - 1Eh, Address 0008h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0008h**

Default: 8000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:14	RO/V	10b	Control MMD Device Present (VSDP): This field indicates if the control MMD device is present and responding to this address: 10: Device responding at this address 11, 01, or 00: No device responding at this address
13:0	RO	0000h	Reserved

3.3.1.10 SR Control MMD Control Register (SR_VSMMD_CTRL) - 1Eh, Address 0009hSR Control MMD

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 0009h**

Default: 0004h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:6	RO	0000h	Reserved
5	RW	0b	Power Down Control (PD_CTRL): This bit is used to control the output port 'xpcs_pdown_o'. If this bit is set, xpcs_pdown_o port will NOT be asserted when LPM (Low Power Enable) bit is programmed to 1. If this bit is low, xpcs_down_o port will be asserted when LPM (Low Power Enable) bit is programmed to 1.
4	RW	0b	Fast Simulation Enable (FASTSIM): When set, this bit indicates that the Fast simulation is enabled. When this bit is set to 1, all IEEE Std 802.3 defined long timers that are implemented are reduced to shorter time period in order to reduce the simulation time. The long timers are implemented in Clause 73 and Clause 37 auto-negotiation modules and also EEE Tx and Rx modules.
3	RO	0b	Reserved
2	RW	1b	VS MMD Enable (MII_MMD_EN): When set, this bit indicates that the vendor-specific MMD1 device is accessible. When reset, this bit indicates that the vendor-specific MMD2 (MII MMD) device is not accessible.
1:0	RO	00b	Reserved

3.3.1.11 SR Control MMD Package Identifier Register 1 (SR_VSMMD_PKGID1) - 1Eh, Address 000Eh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 000Eh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	00h	Reserved

3.3.1.12 SR Control MMD Package Identifier Register 2 (SR_VSMMD_PKGID2) - 1Eh, Address 000Fh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Eh** **Register Address: 000Fh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO	00h	Reserved

3.3.1.13 SR MII MMD Control Register (SR_MII_CTRL) - 1Fh, Address 0000h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0000h**

Default: 1140h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RW	0b	Soft Reset (RST): When the host sets this bit, it triggers the software reset process in which all internal blocks of the PCS are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is Self-Cleared by the PCS after 1 MDC clock period of the MDIO interface.
14	RW	0b	Loopback Enable (LBE): This register bit is not used by the design.
13	RW	0b	Speed Selection - LSB (SS13): This bit, along with SS6 (bit 6) of this register, indicates the SGMII speed: SS6 SS13 SGMII Speed 1 0 1000 Mbps 0 1 100 Mbps 0 0 10 Mbps
12	RW	1b	Enable Auto-Negotiation (AN_ENABLE): When set to 1, this bit enables the Clause 37 auto-negotiation process. Default setting is 1.
11	RW	0b	Power-Down Mode (LPM): This bit controls the power-down mode of the PCS. When 0, the PCS operates as normal. When 1, the PCS goes to the Power-Down Mode and clearing this bit resumes PCS normal operation.
10	RO	0b	Reserved
9	RW	0b	Restart Auto-Negotiation (RESTART_AN): When the host writes this bit, the PCS initiates the Auto-Negotiation process. This bit is used to restart the Auto-Negotiation which is already initiated by setting AN_ENABLE (bit 12). The PCS clears this bit after restarting the Auto-Negotiation.
8	RW	1b	Duplex Mode (DUPLEX_MODE): This bit specifies the duplex mode of the PCS. Programming to 0 indicates Half Duplex and 1 (the default value) indicates Full Duplex. For the PHY Link Duplex Mode: If AN_ENABLE (bit 12) is set to 0, this bit determines the PHY Link Duplex Mode. If AN_ENABLE is set to 1, then the PHY Link Duplex Mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 Auto-Negotiation process.
7	RO	0b	Reserved
6	RW	1b	Speed Selection – MSB (SS6): This bit, along with SS13 (bit 23) of this register, indicates the SGMII speed. Default value is 1. See SS13 description.
5:0	RO	000000b	Reserved

3.3.1.14 SR MII MMD Status Register (SR_MII_STS) - 1Fh, Address 0001h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0001h**

Default: 0189h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO	0b	100BASE-T4 Ability (ABL100T4): Not supported. Hardwired to 0.
14	RO	0b	100BASE-X Full-Duplex Ability (FD100ABL): Not supported. Hardwired to 0.
13	RO	0b	100BASE-X Half-Duplex Ability (HD100ABL): Not supported. Hardwired to 0.
12	RO	0b	10 Mbps Full-Duplex Ability (FD10ABL): Not supported. Hardwired to 0.
11	RO	0b	10 Mbps Half-Duplex Ability (HD10ABL): Not supported. Hardwired to 0.
10	RO	0b	100BASE-T2 Full-Duplex Ability (FD100T): Not supported. Hardwired to 0.
9	RO	0b	100BASE-T2 Half-Duplex Ability (HD100T): Not supported. Hardwired to 0.
8	RO/V	1b	Extended Status Information (EXT_STS_ABL): Hardwired to 1 indicating that Extended Status information is present at register address 16'h000F of this MMD device (DEVAD 1Fh).
7	RO	1b	Unidirectional Ability (UN_DIR_ABL): Hardwired to 1 indicating that the PCS is able to transmit GMII irrespective of whether the device has determined the valid link or not.
6	RO	0b	MF Preamble Suppression (MF_PRE_SUP): Hardwired to 0 indicating that The PCS does not accept the MDIO frames with the preamble suppressed.
5	RO	0b	Auto-negotiation Complete (AN_CMPL): When this bit is set to 1, the contents of the AN MMD Advertisement, AN MMD Link partner Ability, and AN MMD Expansion registers are valid. This bit returns 0 if AN_ENABLE is set to 0.
4	RO	0b	Remote Fault (RF): When set to 1, this bit indicates that the PCS detected that the receive link of the link partner is down. This bit is set based on the auto-negotiated (1000BASE-X Auto-Negotiation) information from the link partner. When 0, this bit indicates that the PCS did not detect a Remote Fault.
3	RO	1b	Auto-negotiation Ability (AN_ABL): The PCS always returns this bit as 1 indicating that the PCS is able to perform Auto-Negotiation.
2	RO	0b	Link Status (LINK_STS): When the PCS sets this bit to 1, it indicates that the Rx link is up. If the link goes down, as indicated by 0, this bit is latched by the PCS until the host performs the read operation to this register.
1	RO	0b	Reserved
0	RO	1b	Extended Register Capability (EXT_REG_CAP): The PCS always returns this bit as 1 indicating that the Extended Register Capability exists.

3.3.1.15 SR MII MMD Device Identifier Register 1 (SR_MII_DEV_ID1) - 1Fh, Address 0002h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0002h**

Default: 7996h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	7996h	Organizationally Unique Identifier[3:18] for PCS MMD (VS_MII_DEV_OUI_3_18): Bits 18:3 of the 24-bit Device Organizationally Unique Identifier (OUI) of the device manufacturer. Writing to bits 15:0 of the vendor-specific PCS MMD Device Identifier Register 1 (SR_VSMMD_PCS_ID1) modifies the content of this register.

3.3.1.16 SR MII MMD Device Identifier Register 2 (SR_MII_DEV_ID2) - 1Fh, Address 0003h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0003h**

Default: CED0h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:10	RO/V	33h	Organizationally Unique Identifier [19:24] (VS_MMD_DEV_OUI_19_24): Bits 24:19 of the 24-bit Device Organizationally Unique Identifier (OUI) of the device manufacturer. Writing to bits 15:0 of the vendor-specific PCS MMD Device Identifier Register 2 (SR_VSMMD_PCS_ID2) modifies the content of this register.
9:4	RO/V	2Dh	Model Number (VS_MMD_DEV_MMN_5_0): 6-bit Model number of the vendor-specific PCS MMD. Writing to bits 9:4 of the vendor-specific PCS MMD Device Identifier Register 2 (SR_VSMMD_PCS_ID2) modifies the content of this register.
3:0	RO/V	0h	Revision Number (VS_MMD_DEV_RN_3_0): 4-bit Revision number of the vendor-specific PCS MMD. Writing to bits 3:0 of the vendor-specific PCS MMD Device Identifier Register 2 (SR_VSMMD_PCS_ID2) modifies the content of this register.

3.3.1.17 SR MII MMD AN Advertisement Register (SR_MII_AN_ADV) - 1Fh, Address 0004h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0004h**

Default: 0020h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO/V	0b	Next Page (NP): Not supported. Hardwired to 0.
14	RO	0b	Reserved
13:12	RW	00b	Remote Fault (RF): This field indicates the fault signaling of the local device to be communicated to the link partner. 00: No Error 01: Offline 10: Link Failure 11: Auto-negotiation Error
11:9	RO	000b	Reserved
8:7	RW	00b	Pause Ability (PAUSE): This field indicates the Pause ability of the device: 00: No Pause 01: Asymmetric Pause towards the link partner 10: Symmetric Pause 11: Symmetric Pause and Asymmetric Pause towards the local device. Software can program suitable values based on the capability of the MAC.
6	RW	0b	Half Duplex (HD): When this bit is set, it indicates that the device can operate in the half-duplex mode.
5	RW	1b	Full Duplex (FD): When this bit is set, it indicates that the device can operate in the full-duplex mode.
4:0	R0	00000b	Reserved

3.3.1.18 SR MII MMD AN Link Partner Base Ability Register (SR_MII_LP_BABL) - 1Fh, Address 0005h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0005h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO/V	0b	Next Page (LP_NP): This bit indicates that the link partner can handle Next Page. Note: To exchange information through Next Page, both devices (local and remote) should have the capability to handle Next Page. The PCS does not support Next Page. Therefore, the Next Page exchange does not happen.
14	RO/V	0b	ACK bit from the Link Partner (LP_ACK): This bit indicates that the link partner has successfully received the page sent by the local device.
13:12	RO/V	00b	Remote Fault (LP_RF): This field indicates the fault signaling of the link partner: 00: No Error 01: Offline 10: Link Failure 11: Auto-negotiation Error
11:9	RO	000b	Reserved
8:7	RO/V	00b	Pause Ability (LP_PAUSE): This field indicates the Pause ability of the link partner: 00: No Pause 01: Asymmetric Pause towards the link partner 10: Symmetric Pause 11: Both Symmetric Pause and Asymmetric Pause towards the local device
6	RO/V	0b	Half Duplex (LP_HD): When this bit is set, it indicates that the link partner is capable of operating in the half-duplex mode.
5	RO/V	0b	Full Duplex (LP_FD): When this bit is set, it indicates that the link partner is capable of operating in the full-duplex mode.
4:0	RO	00000b	Reserved

3.3.1.19 SR MII MMD AN Expansion Register (SR_MII_AN_EXPN) - 1Fh, Address 0006h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0006h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:3	RO	00h	Reserved
2	RO/V	00h	Local Device NP Able (LD_NP_ABL): The local device (the PCS) always returns this bit as 0 because it does not support Next Page.
1	RO/V	00h	Page Received (PG_RCVD): This bit indicates that the local device (the PCS) received a page from the link partner. 1: The local device received a new page 0: The local device did not receive a new page
0	RO	00h	Reserved

3.3.1.20 SR MII MMD Extended Status Register (SR_MII_EXT_STS) - 1Fh, Address 000Fh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 000Fh**

Default: C000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RO/V	1b	1000BASE-X Full-Duplex Capable (CAP_1G_X_FD): The PCS always returns 1 because it supports this feature.
14	RO/V	1b	1000BASE-X Half-Duplex Capable (CAP_1G_X_HD): The PCS always returns 1 because it supports this feature.
13	RO/V	0b	1000BASE-T Full-Duplex Capable (CAP_1G_T_FD): The PCS always returns 0 because it does not supports this feature.
12	RO/V	0b	1000BASE-T Half-Duplex Capable (CAP_1G_T_HD): The PCS always returns 0 because it does not supports this feature.
11:0	RO	000h	Reserved

3.3.1.21 SR MII MMD Time Sync Capability Register (SR_MII_TIME_SYNC_ABL) - 1Fh, Address 0708h

Type: MDIO Register PRTAD: 16h DEVAD: 1Fh Register Address: 0708h

Default: 0003h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:2	RO	00h	Reserved
1	RO/V	1b	1000BASE-X Half-Duplex Capable (CAP_1G_X_HD): The PCS always returns 1 because it supports this feature.
0	RO/V	1b	1000BASE-T Full-Duplex Capable (CAP_1G_T_FD): The PCS always returns 0 because it does not supports this feature.

3.3.1.22 SR MII MMD Time Sync Tx Max Delay Lower Register (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR) - 1Fh, Address 0709h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0709h**

Default: 0038h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	38h	Transmit Path Maximum Data Delay, Lower (MII_TX_MAX_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path of the XPCS in nanoseconds.

3.3.1.23 SR MII MMD Time Sync Tx Max Delay Upper Register (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR) - 1Fh, Address 070Ah

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Ah**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Transmit Path Maximum Data Delay, Upper (MII_TX_MAX_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path of the XPCS in nanoseconds.

3.3.1.24 SR MII MMD Time Sync Tx Min Delay Lower Register (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR) - 1Fh, Address 070Bh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Bh**

Default: 0038h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	38h	Transmit Path Minimum Data Delay, Lower (MII_TX_MIN_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path of the XPCS in nanoseconds.

3.3.1.25 SR MII MMD Time Sync Tx Min Delay Upper Register (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR) - 1Fh, Address 070Ch

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Ch**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Transmit Path Minimum Data Delay, Upper (MII_TX_MIN_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path of the XPCS in nanoseconds.

3.3.1.26 SR MII MMD Time Sync Rx Max Delay Lower Register (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR) - 1Fh, Address 070Dh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Dh**

Default: 00B8h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	B8h	Receive Path Maximum Data Delay, Lower (MII_RX_MAX_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path of the XPCS in nanoseconds.

3.3.1.27 SR MII MMD Time Sync Rx Max Delay Upper Register (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR) - 1Fh, Address 070Eh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Eh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Receive Path Maximum Data Delay, Upper (MII_RX_MAX_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path of the XPCS in nanoseconds.

3.3.1.28 SR MII MMD Time Sync Rx Min Delay Lower Register (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR) - 1Fh, Address 070Fh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 070Fh**

Default: 0088h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	88h	Receive Path Minimum Data Delay, Lower (MII_RX_MIN_DLY_LWR): This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path of the XPCS in nanoseconds.

3.3.1.29 SR MII MMD Time Sync Rx Min Delay Upper Register (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR) - 1Fh, Address 0710h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 0710h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	00h	Receive Path Minimum Data Delay, Upper (MII_RX_MIN_DLY_UPR): This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path of the XPCS in nanoseconds.

3.3.1.30 VR MII MMD Digital Control1 Register (VR_MII_DIG_CTRL1) - 1Fh, Address 8000h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8000h**

Default: 2400h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15	RW	0b	Vendor-Specific Soft Reset (VR_RST): When the host sets this bit, it triggers a vendor-specific software reset process in which all internal blocks of the PCS, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is Self-Cleared by the PCS after 1 MDC clock period for the MDIO interface.
14	RW	0b	Rx to Tx Loopback Enable (R2TLBE): This bit controls the loopback path from the GMII Rx to the GMII Tx at the GMII interface. 0: Loopback path is disabled 1: Loopback path is enabled
13	RW	1b	Enable Vendor-Specific MMD1 (EN_VSMMD1): When this bit is set to 1 (default value), the vendor-specific MMD1 (VSMMD1) is enabled. When this bit is set to zero, VSMMD1 is disabled.
12	RO/V	0b	Enable Clause 37 AN in Backplane Configuration (CL37_BP): Does not apply.
11	RO	0b	Reserved

Bits	Access Type	Default	Field Name and Description
10	RW	1b	Clock Stop Enable (CS_EN): This bit should be programmed based on the capability of the MAC during Rx LPI mode. Programming this bit to 1 allows the PHY to stop the clock during LPI mode. Programming to 0, the clock cannot be stopped during LPI mode.
9	RW	0b	Automatic Speed Mode Change after CL37 AN (MAC_AUTO_SW): When this field is set to 1, the PCS automatically switches to the negotiated SGMII after the completion of CL37 AN. This mode is valid only when the PCS is configured as MAC-side SGMII and should be set only when Auto-Negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, the PCS will operate at the speed/duplex mode as per the values programmed to SR MII MMD Control Register. After the completion of CL37 AN, the application has to read the negotiated Speed/Duplex Mode from VR MII MMD AN Interrupt and Status Register and then program SR MII MMD Control Register appropriately. Note: This bit should be set only when the PCS is configured as SGMII MAC, i.e., TX_CONFIG=0.
8	RW	0b	Datapath Initialization Control (INIT): This bit can be set to flush/initialize the various FIFOs implemented inside the PCS. This is Self-Clear bit. After writing 1 to this bit, software should poll this bit continuously. Only after reading this bit as 0 should software proceed to any other operation. When this bit is programmed to 1, RXFIFO_OVF/RXFIFO_UNF bits of the VR MII MMD Digital Status Register might get set incorrectly. Hence, read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIOF_UNF and RXFIFO_UNF bits would be reliable.
7	RO/V	0b	Mask Running Disparity Error (MSK_RD_ERR): When this bit is set, running disparity errors are ignored by XPCS receiver in evaluating the validity of received code-groups.
6	RW	0b	Pre-emption Packet Enable (PRE_EMP): When this bit is set, it allows the XPCS to properly receive/transmit IEEE Std 802.3br pre-emption packets in SGMII 10M/100M Modes.
5	RO	0b	Reserved
4	RW	0b	Tx Lane 0 Disable (DTXLANED_0): When this bit is set, the PCS disables the Tx Lane 0 of the PHY. When reset, the PCS enables the Tx Lane 0 of the PHY.
3	RW	0b	Over-Ride Control for CL37 Link Timer (CL37_TMR_OVR_RIDE): This bit can be set to over-ride the default value of Clause 37 link timer used by the PCS for auto-negotiation. If this bit is set, the value programmed to the VR MII MMD Link Timer Control Register will be used to compute the duration of Link Timer. This bit should be set only after programming the appropriate value to the VR MII MMD Link Timer Control Register.

Bits	Access Type	Default	Field Name and Description
2	RW	0b	Enable 2.5G GMII Mode (EN_2_5G_MODE): Setting this bit 1 enables the 2.5G GMII Mode of operation. This bit drives the hardware pertaining to 2.5 Gbps SGMII operation.
1	RO	0b	Reserved
0	RW	0b	SGMII PHY Mode Control (PHY_MODE_CTRL): This bit controls the CL37_AN when operating in SGMII (Port 0) PHY mode. When this bit is set to 1, the PCS advertises the values of input ports xpcs_sgmii_link_sts_i, xpcs_sgmii_link_speed_i and xpcs_sgmii_full_duplex_i during SGMII (Port 0) Auto-Negotiation. When this bit is set to 0, SGMII (Port0) Auto-Negotiation will advertise the values programmed to all of these: SGMII_LINK_STS (bit 4) of the VR MII MMD AN Control Register SS13 (bit 13) and SS6 (bit 6) of the SR MII MMD Control Register FD (bit 5) of the SR MII MMD AN Advertisement Register Note: This bit should be set only when the PCS is configured as SGMII PHY, i.e., TX_CONFIG (bit 3 of the VR_MII_AN_CTRL register) = 1.

3.3.1.31 VR MII MMD AN Control Register (VR_MII_AN_CTRL) - 1Fh, Address 8001h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8001h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:9	RO	00h	Reserved
8	RO/V	0b	MII Control (MII_CTRL): This bit controls the width of the MAC interface when operating at SGMII speed modes of 10 Mbps or 100 Mbps. 0: 4-bit MII 1: 8-bit MII
7:5	RO	000b	Reserved
4	RW	0b	SGMII Link Status (SGMII_LINK_STS): This bit is used in Bit 15 of the Config_Reg during IEEE 802.3 Clause 37 Auto-Negotiation when the TX_CONFIG bit of this register is set to 1 in the SGMII/QSGMII/USXGMII mode and when the PHY_MODE_CTRL bit of VR MII MMD Digital Control 1 Register is 0. 0: Link Down 1: Link Up

Bits	Access Type	Default	Field Name and Description
3	RW	0b	Transmit Configuration (TX_CONFIG): This bit controls the Config_Reg value to be used during the IEEE 802.3 Clause 37 Auto-Negotiation in the SGMII/QSGMII/USXGMII mode. 1: Configures the PCS as the PHY side SGMII/QSGMII/USXGMII 0: Configures the PCS as the MAC side SGMII/QSGMII/USXGMII
2:1	RW	00b	PCS Mode (PCS_MODE): This field controls the auto-negotiation (and operating) mode. 00: 1000BASE-X mode (Clause 37 Auto-Negotiation is as per 1000BASEX). 10: SGMII mode (Clause 37 Auto-Negotiation is as per SGMII). 11: QSGMII mode (Clause 37 Auto-Negotiation conforms to QSGMII). Note: The default value is 00. Must be programmed to 10 for SGMII-mode Auto-Negotiation.
0	RW	0b	Clause 37 AN Complete Interrupt Enable (MII_AN_INTR_EN): When set to 1, this bit enables the generation of the IEEE 802.3 Clause 37 Auto-Negotiation Complete interrupt output. When set to 0, it disables the generation of Clause 37 Auto-Negotiation Complete interrupt.

3.3.1.32 VR MII MMD AN Interrupt and Status Register (VR_MII_AN_INTR_STS) - 1Fh, Address 8002h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8002h**

Default: 000Ah Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:5	RO	000h	Reserved
4:1	RO/V	5h	Clause 37 AN SGMII Status/QSGMII Port 0 Status (CL37_ANSGM_STS): This field is valid only when the PCS_MODE[1:0] is set to the SGMII/QSGMII mode and the auto-negotiation is complete. It indicates the status received from remote link after the SGMII/QSGMII (Port 0) Auto-Negotiation is complete. CL37_ANSGM_STS[0] 0: Half Duplex 1: Full Duplex (default value) CL37_ANSGM_STS[2:1] 00: 10 Mbps speed link 01: 100 Mbps speed link 10: 1000 Mbps speed link (default value) CL37_ANSGM_STS[3] 0: Link is Down (default value) 1: Link is Up
0	RW	0b	Clause 37 AN Complete Interrupt (CL37_ANCMPLT_INTR): The PCS sets this bit when IEEE 802.3 Clause 37 Auto-Negotiation is complete. The host must clear this bit by writing 0 to it.

3.3.1.33 VR MII MMD Test Control Register (VR_MII_TC) - 1Fh, Address 8003h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8003h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:3	RO	0000h	Reserved
2	RW	0b	Test Pattern Enable Lanes (TPE): This bit indicates that a test pattern can be enabled in the Tx path after the current normal frame transmission is complete. 0: Test pattern disabled 1: Test pattern enabled The specific test pattern that is generated is based on bits 1:0 of this register.
1:0	RW	2'b00	Test Pattern Select (TP): This field indicates the pattern type that is enabled with Bit 2 of this register. The following are the supported test patterns: 00: High Frequency Test Pattern (default value) 01: Low Frequency Test Pattern 10: Mixed Frequency Test Pattern 11: Reserved The definitions of these test patterns are specified in Annex 48A of IEEE 802.3.

3.3.1.34 VR MII MMD Debug Control Register (VR_MII_DBG_CTRL) - 1Fh, Address 8005h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8005h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:9	RO	7'h0	Reserved
8	RW	1'h0	Transmit Preamble Control (TX_PMBL_CTL): This bit can be set to 1 to prevent possible preamble truncation in the PCS transmitter when operating in 1000BASE-X Mode or 2.5G Mode over GMII. As per IEEE spec, it is permissible for a compliant 1000BASE-X PCS transmit process to truncate the first byte of preamble in order to align the start of the packet on the EVEN boundary. If this bit is set to 1, the XPCS does not delete any preamble bytes (received from GMII Tx interface) and passes on the same number of preamble bytes to its output. The XPCS out this operation by adjusting the IPG. This mode is a deviation from Clause 36 of IEEE Std 802.3, but it can prove useful when operating at 2.5G Mode (over clocked SGMII Mode) and the far-end device is compliant to IEEE Std 802.3bz/cb.
7	RO	1'h0	Reserved
6	RO	1'h0	Reserved

Bits	Access Type	Default	Field Name and Description
5	RW	1'h0	Suppress EEE Loss of Signal Detection (SUPRESS_EEE_LOS_DET): When this field is set to 1, Loss of Signal indicated by the PHY is ignored by the PCS while evaluating the Receive link when operating in EEE mode. Receive link will be purely evaluated based the on data received by the PCS from the PHY. When this field is set to 0, Loss of signal indicated by the PHY will be considered by the PCS while evaluating the Receive link status in EEE mode.
4	RW	1'h0	Suppress Loss of Signal Detection (SUPRESS_LOS_DET): When this field is set to 1, Loss of Signal indicated by the PHY is ignored by the PCS while evaluating the Receive link. Receive link will be purely evaluated based the Rx data received on the port of the PCS. When this field is set to 0, Loss of signal indicated by the PHY will be considered by the PCS while evaluating the Receive link status.
3:1	RO	3'h0	Reserved
0	RW	1'h0	Restart Synchronization (RESTAR_SYNC_0): When set to 1, this bit restarts the Rx Synchronization State machine on Lane 0. The host must clear this bit to 0 before setting it to 1 next time.

3.3.1.35 VR MII MMD EEE Mode Control Register (VR_MII_EEE_MCTRL0)- 1Fh, Address 8006h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8006h**

Default: 899Ch Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:12	RW	4'h8	Clock Stop (CLKSTOP): This field holds the count value after which the Rx clock to the MAC can be stopped. The default value is 8. The host should program this value depending on the capability of the MAC.
11:8	RW	4'h9	100 ns Clock Tic Multiplying Factor (MULT_FACT_100NS): This bit is the multiplying factor to the clk_eee_i clock time period to make it closer to 100 ns. For example, if the clk_eee_i clock time period (clk_eee_i_time_period) is 10 ns, the value of this field is 9, that is, 1 less than 10. This value should be programmed such that the clk_eee_i_time_period * (MULT_FACT_100NS + 1) should be within 80 ns to 120 ns. The default value of this register is 9, assuming that the default clk_eee_i time period to be 10 ns.
7	RW	1'h1	Rx Control Enable (RX_EN_CTRL): This bit controls the generation of the xpcs_rx_en_o{lane} signal. When this bit is set to 1, the xpcs_rx_en_o{lane} signal is deasserted when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_rx_en_o{lane} signal is not deasserted when the EEE transmit controller reaches the Quiet state.
6	RW	1'h0	Effective 100ns Tic Value (SIGN_BIT): The host should use this bit to fine-tune the EEE timing requirement. The host should set this bit to 0 when the clk_eee_i_time_period * (MULT_FACT_100NS + 1) value is more than 100 ns. The host should set this bit to 1 when the clk_eee_i clock period * MULT_FACT_100NS + 1) value is less than or equal to 100ns.
5	RO	1'h0	Reserved

Bits	Access Type	Default	Field Name and Description
4	RW	1'h1	Tx Control Enable (TX_EN_CTRL): This bit controls the generation of the signals xpcs_tx_en_o {lane}. When this bit is set to 1, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is de-asserted when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is not deasserted when the EEE transmit controller reaches the Quiet state.
3	RW	1'h1	Rx Quiet Enable (RX_QUIET_EN): This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
2	RW	1'h1	Tx Quiet Enable (TX_QUIET_EN): This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
1	RW	1'h0	LPI Rx Enable (LRX_EN): When set to 1, this bit enables the Energy Efficient Ethernet support in the PCS receive path. When set to 0, it disables the support for Energy Efficient Ethernet in the PCS receive path.
0	RW	1'h0	LPI Tx Enable (LTX_EN): When set to 1, this bit enables the Energy Efficient Ethernet support in the PCS Transmit path. When set to 0, it disables the support for Energy Efficient Ethernet in the PCS Transmit path.

3.3.1.36 VR MII MMD EEE Tx Timer Register (VR_MII_EEE_TXTIMER) - 1Fh, Address 8008h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8008h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:6	RO	10'h000	Reserved
5:0	RW	6'h00	TSL Resolution (TSL_RES): This field stores the resolution value for the Local Sleep Time (TSL) timer. When the generated 100ns tic timer is not exactly 100ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TSL timer. The PCS maintains the default value of the TSL timer as 199, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100ns to produce 19900ns (19.9 us) as per the TSL requirement in the IEEE standard. If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 90, the default TSL timer produces 17910ns (17.91 us) which is lesser than the standard 19.9 us. To make it 19.9 us, you should program this register such that (199 +/- TSL_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) is greater than 19.9 us and less than 20.1 us (max limit), that is, (199 + TSL_RES)*90 = 19.9 us. TWL_RES = 23 meets the requirement which produces 19.98 us. The SIGN_BIT should be programmed as 1.

3.3.1.37 VR MII MMD EEE Rx Timer Register (VR_MII_EEE_RXTIMER) - 1Fh, Address 8009h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8009h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:14	RO	2'h0	Reserved
13:8	RW	6'h00	TWR Resolution (TWR_RES): This field stores the resolution value for the TWR timer. When the generated 100ns tic timer is not exactly 100ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TWR timer. The default value is 11 us for the PCS in this design. This value is as per the requirements specified in the standard assuming that clk_eee_i_time_period * (MULT_FACT_100NS + 1) produces 100ns tick.
7:0	RW	8'h00	100 us Resolution (RES_100U): This field stores the resolution value for the 100 us timer. If the generated 100ns tic timer is not exactly 100ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the 100 us timer. This field is used to control the generation of 100 us time tick using the clk_eee_i clock and MULT_FACT_100NS field. By default, the 100 us timer is generated assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100ns. Therefore, the PCS maintains the default value of the 100 us timer as 1000 to achieve 100000ns (100 us). You should use this field if clk_eee_i_time_period * (MULT_FACT_100NS + 1) is not equal to 100ns. To program this field, use the following equation: (1000 +/- RES_100US)* ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) = 100 us. The SIGN_BIT should be programmed as 1 for (+) and 0 for (-).

3.3.1.38 VR MII MMD Link Timer Control Register (VR_MII_LINK_TIMER_CTRL) - 1Fh, Address 800Ah

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 800Ah**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Programmable Link Timer Value for Clause 37 Auto-Negotiation (CL37_LINK_TIME): This field can be programmed to desired value if application wishes to over-ride the standard specified values for Link Timer used during CL37 Auto negotiation. The PCS has a 24-bit timer that runs at the frequency of clk_xgxs_rx0_i clock. The value programmed to this field will be used as the upper 16-bit of the value to be loaded to this timer. The lower 8-bits are hardcoded as 8'h7D After programming this register, application should perform either of the following two steps, so that the new values takes effect: Set CL37_TMR_OVR_RIDE bit (bit 3) of the VR MII MMD Digital Control 1 Register to 1. FAST_SIM bit of SR Control MMD Control Register should be cleared (if already set) and then set back to 1.

3.3.1.39 VR MII MMD EEE Mode Control 1 Register (VR_MII_EEE_MCTRL1) - 1Fh, Address 800Bh

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 800Bh**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:1	RO	15'h0000	Reserved
0	RW	1'h0	Transparent Tx LPI Mode Enable (TRN_LPI): When set to 1 (along with LTX_EN=1), transparent LPI mode gets activated in the XPCS Transmit path. In this mode the transmit LPI state-machine doesn't move to the TX_QUIET state. On detecting Lower-Power Idle on the GMII Tx interface, the XPCS goes to the TX_SLEEP state and remains in this state until the MAC stops sending LPI. In this mode, the XPCS merely sends the encoded LPI pattern to the serdes. This mode does not involve gating-off of any of the clocks to the XPCS. In addition, the serdes transmitter is not disabled. The MAC should ensure that it does not gate-off the GMII Tx clock to the XPCS during this mode of operation.

3.3.1.40 VR MII MMD Digital Status Register (VR_MII_DIG_STS) - 1Fh, Address 8010h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8010h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:13	RO/V	3'h0	LPI Transmit State (LTX_STATE): This field indicates the current state of the LPI Transmit state Machine: 000: LTX_ACTIVE 001: LTX_SLEEP 010: LTX_QUIET 011: LTX_REF_WAKE 100: LTX_ALERT (does not apply to the PCS design) 101: LTX_SCR_BYP (does not apply to the PCS design)
12:10	RO/V	3'h0	LPI Receive State (LRX_STATE): This field indicates the current state of the LPI Receive State Machine: 000: LRX_ACTIVE (default) 001: LRX_SLEEP 010: LRX_QUIET 011: LRX_WAKE 100: LRX_WTF 101: LRX_LINK_FAIL 110: LRX_LPI_K
9:7	RO	3'h0	Reserved
6	RO/V	1'h0	Rx FIFO Overflow (RXFIFO_OVF): This bit indicates the clock rate compensation FIFO overflow. 0 indicates normal operation and 1 indicates FIFO overflow.
5	RO/V	1'h0	Rx FIFO Underflow (RXFIFO_UNDF): This bit indicates the clock rate compensation FIFO underflow. 0 indicates normal operation and 1 indicates FIFO underflow.
4:0	RO	5'h0	Reserved

3.3.1.41 VR MII MMD Invalid Code Group Error Count1 Register (VR_MII_ICG_ERRCNT1) - 1Fh, Address 8011h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8011h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:8	RO	8'h00	Reserved
7:0	RO/V	8'h00	Invalid Code Group Count Lane 0 (EC0): This field gives the invalid code group count in Lane 0 when bit 4 of VR MII MMD Digital Error Count Select Register is set to 1.

3.3.1.42 VR MII MMD Miscellaneous Status Register (VR_MII_MISC_STS) - 1Fh, Address 8018h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8018h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:4	RO	12'h000	Reserved
7:0	RO/V	4'h0	Bit Shift (BIT_SFT): This field indicates the number of bit-shifts carried-out by the comma-detect logic so as to align the incoming 10-bit XGXS Rx data. The default value of this field can be any value, depending on the status of comma-detect logic.

3.3.1.43 VR MII PHY Rx Lane Status Register (VR_MII_RX_LSTS) - 1Fh, Address 8020h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 8020h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:13	RO/V	3'h0	DPLL Lock Status for Lanes [3:1] (RX_VALID_3_1): This field indicates that the DPLL in the PHY is locked on the serial data in the corresponding lane. xx1: Lane 1 DPLL bit locked x1x: Lane 2 DPLL bit locked 1xx: Lane 3 DPLL bit locked (x indicates don't care)
12	RO/V	1'h0	DPLL Lock Status for Lane 0 (RX_VALID_0): This field indicates that the DPLL in the PHY is locked on the serial data in Lane 0. The value 1'b1 indicates that Lane 0 DPLL bit is locked.
11:5	RO	2'h0	Reserved
4	RO/V	1'h0	Rx Signal Detect for Lane 0 (SIG_DET_0): This bit indicates that the Rx detected the signal on Lane 0. This bit is the complement value of the signals input from the PHY on Lane 0. The value 1'b1 indicates that Lane 0 signal is detected.
3:0	RO	4'h0	Reserved

3.3.1.44 VR MII MMD Digital Control2 Register (VR_MII_DIG_CTRL2) - 1Fh, Address 80E1h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 80E1h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:5	RO	11'h000	Reserved
4	RW	1'h0	Tx Polarity Invert on Lane 0 (TX_POL_INV_0): When set to 1, this bit reverses the data polarity on the Tx differential lines of Lane 0.
3:1	RO	3'h0	Reserved
0	RW	1'h0	Rx Polarity Invert on Lane 0 (ABL100T4): When set, the bits within this field indicate that the data received on Rx serial line is inverted on Lane 0. This reverses the polarity on the data received from the PHY core. The value 1 indicates that Rx data on Lane 0 is inverted.

3.3.1.45 VR MII MMD Digital Error Count Select Register (VR_MII_DIG_ERRCNT_SEL) - 1Fh, Address 80E2h

Type: MDIO Register **PRTAD: 16h** **DEVAD: 1Fh** **Register Address: 80E2h**

Default: 0000h Size: 16 bits MDIO Clause: 45

Bits	Access Type	Default	Field Name and Description
15:5	RO	11'h000	Reserved
4	RW	1'h0	Invalid Code Group Error Counter Enable (INV_EC_EN): When this bit is set, the counting of invalid code group errors is enabled. 0: The counting of errors is disabled 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR MII MMD Invalid Code Group Error Count1 Register.
3:1	RO	3'h0	Reserved
0	RW	1'h0	Clear on Read (COR): When this bit is set and the host reads any error counter, that counter is cleared after the read cycle. 0: Normal operation 1: Clear any error counter that is read

3.3.2 MDIO – Adhoc PHY Sublayer Registers – PHY Address 15h

The Adhoc Registers are accessible as an IEEE Std 802.3 Clause 22 capable PHY MDIO Manageable Device (MMD). Its 5-bit PHY Address (PHYAD) is 15h. Its 32 16-bit data registers are accessible using the 5-bit PHY Register Address (REGAD).

The Adhoc Registers consist of a PHY Global Configuration Register (GCR), one captured 64-bit Always Running Timer (ART) Time Stamp, one six-byte, unique MAC Address provided by the Intel product customer via the system Flash Device, and various status registers and configuration registers related to the PCH internal PHY sublayer circuitry and debug circuity.

Table 3-7. Summary of Adhoc MDIO Registers, PHYAD = 15h

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
00h	16	Global Configuration Register (GCR)	0826h
01h	16	PMC ART Time Capture Register 0 (PMC_ART0)	0000h
02h	16	PMC ART Time Capture Register 1 (PMC_ART1)	0000h
03h	16	PMC ART Time Capture Register 2 (PMC_ART2)	0000h
04h	16	PMC ART Time Capture Register 3 (PMC_ART3)	0000h
05h	16	General Purpose Status Register 0 (GPSR0)	0000h
06h	16	General Purpose Status Register 1 (GPSR1)	0000h
07h	16	General Purpose Status Register 2 (GPSR2)	0000h
08h	16	General Purpose Status Register 3 (GPSR3)	0000h
09h	16	General Purpose Status Register 4 (GPSR4)	0000h
0Ah	16	General Purpose Status Register 5 (GPSR5)	0000h
0Bh	16	General Purpose Configuration Register 0 (GPCR0)	1020h
0Ch	16	General Purpose Configuration Register 1 (GPCR1)	0001h
0Dh	16	General Purpose Configuration Register 2 (GPCR2)	0050h
0Eh	16	General Purpose Configuration Register 3 (GPCR3)	0000h
0Fh	16	General Purpose Configuration Register 4 (GPCR4)	0000h
10h	16	General Purpose Configuration Register 5 (GPCR5)	0000h
11h	16	General Purpose Configuration Register 6 (GPCR6)	0000h
12h	16	General Purpose Configuration Register 7 (GPCR7)	0000h
13h	16	MAC Address Strap Value 0 (MACADDR0)	0000h
14h	16	MAC Address Strap Value 1 (MACADDR1)	0000h
15h	16	MAC Address Strap Value 2 (MACADDR2)	0000h
16h	16	MGBE Hammock Harbor Status (MGBE_HH_STATUS)	0000h
17h	16	MGBE RGMII DLL Status (MGBE_STATUS1)	0000h
18h	16	MGBE STATUS Register2 (MGBE_STATUS2)	0000h
19h	16	MGBE STATUS Register3 (MGBE_STATUS3)	0000h
1Ah	16	MGBE RGMII DLL Configuration Register 1 (MGBE_CONFIG1)	0000h
1Bh	16	MGBE RGMII DLL Configuration Register 2 (MGBE_CONFIG2)	0000h
1Ch	16	MGBE CONFIG Register3 (MGBE_CONFIG3)	0000h

Table 3-7. Summary of Adhoc MDIO Registers, PHYAD = 15h

Register Address (Hex)	Data Size (Bits)	Register Name (Register Symbol)	Default Value [15:0]
1Dh	16	MGBE CONFIG Register4 (MGBE_CONFIG4)	0000h
1Eh	16	MGBE CONFIG Register5 (MGBE_CONFIG5)	0000h
1Fh	16	MGBE CONFIG Register6 (MGBE_CONFIG6)	0000h

3.3.2.1 Global Configuration Register (GCR) - Address 00h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 00h**

Default: 0826h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:12	RW	4'h0	Reserved
11:8	RW	4'h8	Always Running Timer Capture Skew (ART_SKEW): The skew is provided as a number of clock cycles. Default value is 8 cycles for the 19.2-MHz ART Clock.
7	RW	1'b0	Reserved
6	RW	1'b0	PHY to MAC Interrupt Polarity (PHY2MAC_INTR_POL): When programmed to 1, the polarity of the interrupt signal that comes from an external PHY is inverted.
5	RW	1'b1	MAC Function Level Reset Enable (MAC_FLR_ENABLE): When programmed to 1, the Function Level Reset (FLR) mechanism is enabled. When programmed to 0, the FLR mechanism is disabled.
4	RW	1'b0	PHY Interface Mode Override (PHYIF_STRAPOVR): Overrides the PHY interface mode established by Soft Straps or system Fuses: 0: Override is disabled 1: Override is enabled
3	RW	1'b0	PHY Interface Mode (PHYIF_MODE): When the PHYIF_STRAPOVR bit of this register is 1, these bits determine the PHY Interface Mode as follows: 0: RGMII Mode 1: SGMII mode
2:1	RW	2'b11	Link Speed Mode (LINK_MODE): This field configures the Link-Speed Mode when the AUTONEG_DISABLE bit of this register is 1: 11: 2.5 Gbps (this is applicable only in SGMII Mode) 10: 1 Gbps 01: 100 Mbps 00: 10 Mbps
0	RW	1'b0	Auto-Negotiation Disable (AUTONEG_DISABLE): When this bit is 1, the Link Speed is determined by the LINK_MODE bits of this register instead of the PCS Auto-Negotiation value.

3.3.2.2 PMC ART Time Capture Register 0 (PMC_ART0) - Address 01h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 01h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 0 (PMC_ART0_FLD): Bits 15:0 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

3.3.2.3 PMC ART Time Capture Register 1 (PMC_ART1) - Address 02h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 02h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 1 (PMC_ART1_FLD): Bits 31:16 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

3.3.2.4 PMC ART Time Capture Register 2 (PMC_ART2) - Address 03h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 03h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 2 (PMC_ART2_FLD): Bits 47:32 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

3.3.2.5 PMC ART Time Capture Register 3 (PMC_ART3) - Address 04h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 04h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	PMC ART Value 3 (PMC_ART3_FLD): Bits 63:48 of the captured 64-bit Always Running Timer (ART) from the PCH Power Management Controller.

3.3.2.6 General Purpose Status Register 0 (GPSR0) - Address 05h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 05h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RO	1'b0	Reserved
14	RO/V	1'b0	RXSTANDBY_STATUS_FLD (RXSTANDBY_STATUS_FLD): Indicates the value of the fia_tsn_rxstandbystatus signal.
13	RO	1'b0	Reserved
12	RO/V	1'b0	RXELECIDLE_SUS_FLD (RXELECIDLE_SUS_FLD): Indicates the value of the fia_tsn_rxelecidle_sus signal.
11	RO/V	1'b0	PCLKIN_CHG_OK_FLD (PCLKIN_CHG_OK_FLD): Indicates the value of the fia_tsn_pclkin_chg_ok signal.
10:7	RO	3'b000	Reserved
6:4	RO/V	3'b000	POWERDOWN_SUS_FLD (POWERDOWN_SUS_FLD): Indicates the value of the tsn_fia_powerdown_sus_reg[2:0] signals.
3	RO	1'b0	Reserved
2	RO/V	1'b0	PHY_POWER_STATE_FLD (PHY_POWER_STATE_FLD): When this bit is 1, PHY is out of reset state
1	RO	1'b0	Reserved
0	RO/V	1'b0	PLL_CLK_VLD_FLD (PLL_CLK_VLD_FLD): When this bit is 1, it indicates that the PLL Clock to be used by the GBE-TSN is valid. This can either be the MODPHY SATA PLL Clock or the MIPI PLL Clock depending on the FIA lane on which the GBE-TSN is implemented.

3.3.2.7 General Purpose Status Register 1 (GPSR1) - Address 06h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 06h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

3.3.2.8 General Purpose Status Register 2 (GPSR2) - Address 07h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 07h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

3.3.2.9 General Purpose Status Register 3 (GPSR3) - Address 08h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 08h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

3.3.2.10 General Purpose Status Register 4 (GPSR4) - Address 09h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 09h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:8	RO/V	8'h00	FIA_STATUS_SEL2_FLD MGBE_MDIO (FIA_STATUS_SEL2_FLD): Various signals are multiplexed into status bits based on the bits GPCR4[13:8].
7:0	RO/V	8'h00	FIA_STATUS_SEL1_FLD MGBE_MDIO (FIA_STATUS_SEL1_FLD): Various signals are multiplexed into status bits based on the bits GPCR4[5:0].

3.3.2.11 General Purpose Status Register 5 (GPSR5) - Address 0Ah

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Ah**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

3.3.2.12 General Purpose Configuration Register 0 (GPCR0) - Address 0Bh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Bh**

Default: 1020h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RO	1'b0	Reserved
14:12	RW	3'b001	MODPHY_PCLK_RATE_FLD MGBE_MDIO (MODPHY_PCLK_RATE_FLD): Destination is MODPHY signals i_pclkrate[2:0]. This determines the rate of PCLK being sent to the PHY. Used by PHY to determine PCLK:DATA Rate for TX/RX Data valid signaling. When MODPHY is in SATA Mode: 000: 37.5 MHz 001: 75 MHz (default) 010: 150 MHz 011: 300 MHz 100: 600 MHz
11	RW	1'b0	PCLKIN_CHG_ACK_FLD MGBE_MDIO (PCLKIN_CHG_ACK_FLD): Destination is MODPHY signal fia_pclkin_chg_ack.
10	RO	1'b0	Reserved
9:8	RW	2'b00	MODPHY_RATE_FLD MGBE_MDIO (MODPHY_RATE_FLD): Destination is MODPHY signals i_rate[1:0]. For SerDes Mode, the choices are: 00: PCI Express Gen 1 01: PCI Express Gen 2 10: PCI Express Gen 3 11: KX Mode, half rate for GbE (default)
7	RO	1'b0	Reserved

Bits	Access Type	Default	Field Name and Description
6:4	RW	3'b010	MODPHY_POWERDOWN_SIGNL_FLD MGBE_MDIO (MODPHY_POWERDOWN_SIGNL_FLD): Destination is MODPHY signals i_powerdown_sus[2:0]. These signals control the power management state of the MODPHY. The MODPHY Power States: 000: P0 - PHY TX is transmitting data. MAC is providing data bytes to be sent every clock cycle. PHY RX may or may not be receiving data. 001: P1 - PHY TX is not transmitting data and is in electrical idle. PHY behavior is undefined if tx_elecidle is deasserted in this state. PHY RX may or may not be receiving data. 010: P2 - PHY does a receiver detection operation. PHY behavior is undefined if tx_elecidle is deasserted in this state. 011: P3 – (default) PHY is in low power state and is in electrical idle. TX is High-Z state. 100: P4 - PHY is in low power state and is in electrical idle. TX pads sit in common mode. 101: P5 - PHY is in low power state and is in electrical idle. TX pad is in strong pull down. 110: P6 - PHY is in low power state and is in electrical idle. TX pads are in common mode with clock hub bias on. 111: Reserved.
3	RO	1'b0	Reserved
2	RW	1'b0	MODPHY_RST_DATAPATH_INT_FLD MGBE_MDIO (MODPHY_RST_DATAPATH_INT_FLD): Destination is MODPHY signal i_reset_l. Active-low reset signal for both the PIPE and SerDes interface. This signal is equivalent to a lane disable signal.
1	RW	1'b0	PHY Rx Clock Enable: Un-gate PHY Rx Clock CDC.
0	RW	1'b0	PLL_CLK_REQUEST_FLD MGBE_MDIO (PLL_CLK_REQUEST_FLD): Depending on the PLL configuration, MIPI PLL or SATA PLL, this bit provides a signal much like mgbe_mii_refclkreq.

3.3.2.13 General Purpose Configuration Register 1 (GPCR1) - Address 0Ch

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Ch**

Default: 0001h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:13	RO	7'h00	Reserved
12	RW	1'b0	MODPHY_TX_DATA_SEL_FLD MGBE_MDIO (TX_DATA_SEL_FLD): Used as mux select for selecting tsn_fia_txdata[9:0], directly or bit reserved.
11	RW	1'b0	MODPHY_STATUSREG1_BIT_SEL_FLD MGBE_MDIO (STATUSREG1_BIT_SEL_FLD): Used as mux select for selecting bits of status register 1, directly or synchronized.
10:9	RO	2'b00	Reserved

Bits	Access Type	Default	Field Name and Description
8	RW	1'b0	MODPHY_TX_DET_RX_LPBK_FLD MGBE_MDIO (MODPHY_TX_DET_RX_LPBK_FLD): Destination is MODPHY signal i_txdetrxlpbk_sus. Used to tell the PHY to begin a RX detect operation or loopback to signal LFPS during MODPHY power state P0 for USB polling state. Function of this pin depends on the power state and the i_txelecidle signal.
7	RO	1'b0	Reserved
6:4	RW	3'b000	MODPHY_TX_MRGN_FLD MGBE_MDIO (MODPHY_TX_MRGN_FLD): Destination is MODPHY signals i_txmargin[2:0]. Selects the transmitter voltage levels. 000: TxMargin value 0 = ~1Vdiffp2p (Normal operating range).
3	RW	1'b0	MODPHY_TX_SWING_FLD MGBE_MDIO (TX_SWING_FLD): Drives an output signal fia_tx_swing.
2	RO	1'b0	Reserved
1:0	RW	2'b01	MODPHY_TX_DE_EMP_FLD MGBE_MDIO (MODPHY_TX_DE_EMP_FLD): General Purpose Configuration Register2[15:0]. 00: the de-emphasis is -6dB 01: the de-emphasis -3.5 dB 10: the de-emphasis 0dB 11: the de-emphasis -9.5dB

3.3.2.14 General Purpose Configuration Register 2 (GPCR2) - Address 0Dh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Dh**

Default: 0050h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:9	RO	7'h00	Reserved
8	RW	1'b0	MODPHY_HALT_PHY_RDY_FLD MGBE_MDIO (HALT_PHY_RDY_FLD): additional output signal to halt xpcs_phy_rdy, in addition to powerdown state machine.
7	RO	1'b0	Reserved
6	RW	1'b1	MODPHY_RX_INTFLTREN_FLD MGBE_MDIO (RX_INTFLTREN_FLD): Drives an output signal tsn_fia_rxintfltren_l.
5	RO	1'b0	Reserved
4	RW	1'b1	MODPHY_RXTERMEN_H_AON_FLD MGBE_MDIO (MODPHY_RXTERMEN_H_AON_FLD): Destination is MODPHY signal i_rxtermen_h_aon. This signal controls the presence of the RX termination resistors. 1: Terminations are present 0: Terminations are removed from the circuit
3	RO	1'b0	Reserved

Bits	Access Type	Default	Field Name and Description
2	RW	1'b0	MODPHY_RX_SQUELCH_EN_FLD MGBE_MDIO (MODPHY_RX_SQUELCH_EN_FLD): Destination is MODPHY signal i_rxsquelchen. Used in PCIE P2/USB3 P3/ SATA Slumber power states to cycle the squelch and monitor for activity.
1	RO	1'b0	Reserved
0	RW	1'b0	MODPHY_RX_POLARITY_FLD MGBE_MDIO (MODPHY_RX_POLARITY_FLD): Destination is MODPHY signal i_rxpolarity. Configures the PHY to perform polarity inversion on the received data. 0: PHY does no polarity inversion 1: PHY does polarity inversion

3.3.2.15 General Purpose Configuration Register 3 (GPCR3) - Address 0Eh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Eh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

3.3.2.16 General Purpose Configuration Register 4 (GPCR4) - Address 0Fh

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 0Fh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:14	RO	2'b00	Reserved
13:8	RW	6'b000000	MODPHY_STATUS_SIGNL_SEL2_FLD MGBE_MDIO (MODPHY_STATUS_SIGNL_SEL2_FLD): Based on these bits various FIA signals are multiplexed into the GPSR4[15:8].
7:6	RO	2'b00	Reserved
5:0	RW	6'b000000	MODPHY_STATUS_SIGNL_SEL1_FLD MGBE_MDIO (MODPHY_STATUS_SIGNL_SEL1_FLD): Based on these bits various FIA signals are multiplexed into the GPSR4[7:0].

3.3.2.17 General Purpose Configuration Register 5 (GPCR5) - Address 10h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 10h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

3.3.2.18 General Purpose Configuration Register 6 (GPCR6) - Address 11h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 11h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:6	RW	10'h000	MODPHY_FIA_OUTPUT_SEL_FLD MGBE_MDIO (MODPHY_FIA_OUTPUT_SEL_FLD): Used to replace various FIA output signals based on GPCR6[5:0] and GPCR7[5:0] bits.
5:0	RW	6'h00	MODPHY_CONFIG_SIGNL_SEL1_FLD MGBE_MDIO (MODPHY_CONFIG_SIGNL_SEL1_FLD): Selects one of 49 sets of internal signal values to be sent to the FIA and Used as MUX select for selecting values for various output FIA signals.

3.3.2.19 General Purpose Configuration Register 7 (GPCR7) - Address 12h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 12h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:6	RW	10'h000	MODPHY_TX_DATA_FLD MGBE_MDIO (TX_DATA_FLD): Used for replacing FIA Tx data, and some other FIA signals too, based on GPCR7[5:0] configuration.
5:0	RW	6'h00	MODPHY_CONFIG_SIGNL_SEL2_FLD MGBE_MDIO (MODPHY_CONFIG_SIGNL_SEL2_FLD): Used as MUX select for selecting values for various output FIA signals.

3.3.2.20 MAC Address Strap Value 0 (MACADDR0) - Address 13h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 13h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	MAC_ADDR_STRAP0_FLD MGBE_MDIO (MAC_ADDR_STRAP0_FLD): MAC address strap values [15:0] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition.

3.3.2.21 MAC Address Strap Value 1 (MACADDR1) - Address 14h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 14h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	MAC_ADDR_STRAP0_FLD MGBE_MDIO (MAC_ADDR_STRAP0_FLD): MAC address strap values [31:16] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition.

3.3.2.22 MAC Address Strap Value 2 (MACADDR2) - Address 15h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 15h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO/V	16'h0000	MAC_ADDR_STRAP0_FLD MGBE_MDIO (MAC_ADDR_STRAP0_FLD): MAC address strap values [47:32] This is a write-only-once register, and the value is loaded on iosf2axi_fuse_valid low to high transition.

3.3.2.23 MGBE Hammock Harbor Status (MGBE_HH_STATUS) - Address 16h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 16h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:4	RO	12'h000	Reserved
3	RW	1'b0	MMGBE_SBD_SFTY_UE (MGBE_SBD_SFTY_UE): MAC Safety Uncorrectable error status: This bit is set on ac_sbd_ue_intr and cleared by software.
2	RW	1'b0	MGBE_SBD_SFTY_CE (MGBE_SBD_SFTY_CE): MAC Safety Correctable error status: This bit is set on mac_sbd_ce_intr and cleared by software.
1	RW	1'b0	MGBE_TSW_ERR (MGBE_TSW_ERROR): Timestamp error status: Iosf2axi_hh_tsw_status output from bridge latched on avail.
0	RW	1'b0	MGBE_SNAPSHOT_DONE (MGBE_SNAPSHOT_DONE): Snapshot done bit: Set when MGBE received LocalSync for tsw sync timestamp from iosf2axibr (opcode = 51). Cleared when new request gpo1 is initiated.

3.3.2.24 MGBE RGMII DLL Status (MGBE_STATUS1) - Address 17h

This Read-Only Status Register is available to subsystems that are configured to provide the RGMII rather than the PCS module as the external interface. It provides information concerning the Master/Slave DLL module used for RGMII.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 17h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RO/V	1'b0	Master DLL Lock (MDLL_LOCK): Indicates that the Master DDL for RGMII is locked.
14:8	RO	7'h00	Reserved
7:4	RO/V	4'h0	Master DLL Coarse Tuning Value (MDLL_COARSE_TUNE): Indicates the value used for the Master DLL Coarse Tuning for RGMII.
3:0	RO/V	4'h0	Master DLL Fine Tuning Value (MDLL_FINE_TUNE): Indicates the value used for the Master DLL Fine Tuning for RGMII.

3.3.2.25 MGBE STATUS Register2 (MGBE_STATUS2) - Address 18h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 18h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

3.3.2.26 MGBE STATUS Register3 (MGBE_STATUS3) - Address 19h

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 19h**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RO	16'h0000	Reserved

3.3.2.27 MGBE RGMII DLL Configuration Register 1 (MGBE_CONFIG1) - Address 1Ah

This Read-Write Configuration Register is used to configure the Master/Slave DLL module used for RGMII.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Ah**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15	RW	1'b0	Override Master DLL Tuning Values (SW_OVR): 1 -> SW override is enabled. When set, the coarse and fine values to the slave DLLs will be jammed by configA register values. The master DLL coarse and fine values will be bypassed.
14	RW	1'b0	Software Reset (SW_RESETB): Active-low software reset. Resets the master DLL when asserted low.
13	RW	1'b0	MGBE_DLLRX_BYPASS (MGBE_DLLRX_BYPASS): DLL Bypass option for RGMII RX Clock.
12	RW	1'b0	MGBE_DLLTX_BYPASS (MGBE_DLLTX_BYPASS): DLL Bypass option for RGMII TX Clock.
11	RO	1'b0	Reserved
10:8	RW	3'b000	Observe Master DLL Values (MDLL_DFT): DFT inputs for observing various master DLL values.
7:4	RW	4'h0	Override Slave DLL Coarse Tuning Delay (SDLL_COARSE_OVER): Slave DLL coarse tuning delay override value used when the SW_OVR bit of this register is one.
3:0	RW	4'h0	Override Slave DLL Fine Tuning Delay (SDLL_FINE_OVER): Slave DLL fine tuning delay override value used when the SW_OVR bit of this register is one.

3.3.2.28 MGBE RGMII DLL Configuration Register 2 (MGBE_CONFIG2) - Address 1Bh

This Read-Write Configuration Register is used to configure the Master/Slave DLL module used for RGMII.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Bh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:14	RO	2'b00	Reserved
13:8	RW	6'h00	RX Slave DLL Tap Value (RX_SLAVE_TAP_VALUE): The taps are binary coded. Each tap gives 125 ps resolution. Valid values are: 6'b00_0000 -> 0 ns 6'b00_0001 -> 125 ps through… 6'b10_1000 -> 10 ns All other values are reserved.
7:6	RO	2'b00	Reserved
5:0	RW	6'h00	TX Slave DLL Tap Value (TX_SLAVE_TAP_VALUE): The taps are binary coded. Each tap gives 125 ps resolution. For example: 6'b00_0000 -> 0 ns 6'b00_0001 -> 125 ps through… 6'b10_1000 -> 10 ns All other values are reserved.

3.3.2.29 MGBE CONFIG Register3 (MGBE_CONFIG3) - Address 1Ch

This Read-Write Configuration Register is for VC1 mapping.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Ch**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	VC1 Mapping Register (MGBE_CONFIG3_FLD): VC1 mapping register for 8 Tx and 8 Rx DMA channels.

3.3.2.30 MGBE CONFIG Register4 (MGBE_CONFIG4) - Address 1Dh

This Read-Write Configuration Register is reserved by Intel for possible future use.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Dh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

3.3.2.31 MGBE CONFIG Register5 (MGBE_CONFIG5) - Address 1Eh

This Read-Write Configuration Register is reserved by Intel for possible future use.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Eh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

3.3.2.32 MGBE CONFIG Register6 (MGBE_CONFIG6) - Address 1Fh

This Read-Write Configuration Register is reserved by Intel for possible future use.

Type: MDIO Register **PHYAD: 15h** **Register Address (REGAD): 1Fh**

Default: 0000h Size: 16 bits MDIO Clause: 22

Bits	Access Type	Default	Field Name and Description
15:0	RW	16'h0000	Reserved

3.3.3 MDIO – External PHY Sublayer Registers

The MDIO Controller provides the MDIO interface to PHY components that are external to the PCH component. Both Clause 22 capable and Clause 45 capable PHY components are supported. See IEEE Std 802.3-2015 for the MDIO interface and electrical specifications.

4 Direct Memory Access (DMA) Interface

4.1 DMA Configuration Registers Summary

This registers of the Intel® PSE devices. This contains multiple Intel® PSE Direct Memory Access (DMA) Controller devices:

- Intel® PSE DMA Controller #0 - Bus: 0, Device: 29, Function: 3
- Intel® PSE DMA Controller #1 - Bus: 0, Device: 29, Function: 4
- Intel® PSE DMA Controller #2 - Bus: 0, Device: 29, Function: 5

DID Values:

- Intel® PSE DMA Controller #0 - D9: F3 - 4BB4h
- Intel® PSE DMA Controller #1 - D9: F4 - 4BB5h
- Intel® PSE DMA Controller #2 - D9: F5 - 4BB6h

Table 4-1. Summary of Bus: 0, Device: 29, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4BB40000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h

Table 4-1. Summary of Bus: 0, Device: 29, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

4.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4BB40000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BB4h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

4.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

4.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

4.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

4.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

4.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

4.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

4.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

4.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

4.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

4.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

4.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

4.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

4.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

4.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

4.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

4.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

4.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

4.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

4.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

4.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

4.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

4.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

4.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

4.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

4.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

4.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

4.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

4.2 DMA MMIO Registers Summary

Table 4-2. Summary of Bus: 0, Device: 29, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	SAR0	00000000h
8h	4	DAR0	00000000h
10h	4	LLP0	00000000h
18h	4	CTL_LO0	00000000h
1Ch	4	CTL_HI0	00000000h
20h	4	SSTAT0	00000000h
28h	4	DSTAT0	00000000h
30h	4	SSTATAR0	00000000h
38h	4	DSTATAR0	00000000h
40h	4	CFG_LO0	00000203h
44h	4	CFG_HI0	00000000h
58h	4	SAR1	00000000h
60h	4	DAR1	00000000h
68h	4	LLP1	00000000h
70h	4	CTL_LO1	00000000h
74h	4	CTL_HI1	00000000h
78h	4	SSTAT1	00000000h
80h	4	DSTAT1	00000000h
88h	4	SSTATAR1	00000000h
90h	4	DSTATAR1	00000000h
98h	4	CFG_LO1	00000203h
9Ch	4	CFG_HI1	00000000h
B0h	4	SAR2	00000000h
B8h	4	DAR2	00000000h
C0h	4	LLP2	00000000h
C8h	4	CTL_LO2	00000000h
CCh	4	CTL_HI2	00000000h
D0h	4	SSTAT2	00000000h
D8h	4	DSTAT2	00000000h
E0h	4	SSTATAR2	00000000h
E8h	4	DSTATAR2	00000000h
F0h	4	CFG_LO2	00000203h
F4h	4	CFG_HI2	00000000h
108h	4	SAR3	00000000h
110h	4	DAR3	00000000h
118h	4	LLP3	00000000h

Table 4-2. Summary of Bus: 0, Device: 29, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
120h	4	CTL_LO3	00000000h
124h	4	CTL_HI3	00000000h
128h	4	SSTAT3	00000000h
130h	4	DSTAT3	00000000h
138h	4	SSTATAR3	00000000h
140h	4	DSTATAR3	00000000h
148h	4	CFG_LO3	00000203h
14Ch	4	CFG_HI3	00000000h
160h	4	SAR4	00000000h
168h	4	DAR4	00000000h
170h	4	LLP4	00000000h
178h	4	CTL_LO4	00000000h
17Ch	4	CTL_HI4	00000000h
180h	4	SSTAT4	00000000h
188h	4	DSTAT4	00000000h
190h	4	SSTATAR4	00000000h
198h	4	DSTATAR4	00000000h
1A0h	4	CFG_LO4	00000203h
1A4h	4	CFG_HI4	00000000h
1B8h	4	SAR5	00000000h
1C0h	4	DAR5	00000000h
1C8h	4	LLP5	00000000h
1D0h	4	CTL_LO5	00000000h
1D4h	4	CTL_HI5	00000000h
1D8h	4	SSTAT5	00000000h
1E0h	4	DSTAT5	00000000h
1E8h	4	SSTATAR5	00000000h
1F0h	4	DSTATAR5	00000000h
1F8h	4	CFG_LO5	00000203h
1FCh	4	CFG_HI5	00000000h
210h	4	SAR6	00000000h
218h	4	DAR6	00000000h
220h	4	LLP6	00000000h
228h	4	CTL_LO6	00000000h
22Ch	4	CTL_HI6	00000000h
230h	4	SSTAT6	00000000h
238h	4	DSTAT6	00000000h
240h	4	SSTATAR6	00000000h
248h	4	DSTATAR6	00000000h

Table 4-2. Summary of Bus: 0, Device: 29, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
250h	4	CFG_LO6	00000203h
254h	4	CFG_HI6	00000000h
268h	4	SAR7	00000000h
270h	4	DAR7	00000000h
278h	4	LLP7	00000000h
280h	4	CTL_LO7	00000000h
284h	4	CTL_HI7	00000000h
288h	4	SSTAT7	00000000h
290h	4	DSTAT7	00000000h
298h	4	SSTATAR7	00000000h
2A0h	4	DSTATAR7	00000000h
2A8h	4	CFG_LO7	00000203h
2ACh	4	CFG_HI7	00000000h
2C0h	4	RAWTFR	00000000h
2C8h	4	RAWBLOCK	00000000h
2D0h	4	RAWSRCTRAN	00000000h
2D8h	4	RAWDSTTRAN	00000000h
2E0h	4	RAWERR	00000000h
2E8h	4	STATUSTFR	00000000h
2F0h	4	STATUSBLOCK	00000000h
2F8h	4	STATUSSRCTRAN	00000000h
300h	4	STATUSDSTTRAN	00000000h
308h	4	STATUSERR	00000000h
310h	4	MASKTFR	00000000h
318h	4	MASKBLOCK	00000000h
320h	4	MASKSRCTRAN	00000000h
328h	4	MASKDSTTRAN	00000000h
330h	4	MASKERR	00000000h
338h	4	CLEARTFR	00000000h
340h	4	CLEARBLOCK	00000000h
348h	4	CLEARSRCTRAN	00000000h
350h	4	CLEARDSTTRAN	00000000h
358h	4	CLEARERR	00000000h
360h	4	STATUSINT	00000000h
398h	4	DMACFGREG	00000000h
3A0h	4	CHENREG	00000000h
3B8h	4	CLASSPRIORITY0_LO	00000000h
3BCh	4	CLASSPRIORITY0_HI	00000000h
3C0h	4	CLASSPRIORITY1_LO	00000000h

Table 4-2. Summary of Bus: 0, Device: 29, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3C4h	4	CLASSPRIORITY1_HI	00000000h
400h	4	FIFOPARTITION0_LO	00000000h
404h	4	FIFOPARTITION0_HI	00000000h
408h	4	FIFOPARTITION1_LO	00000000h
40Ch	4	FIFOPARTITION1_HI	00000000h
410h	4	SAI_ERR	00000000h
418h	4	GLOBAL_CFG	00000000h
1000h	4	DMA ControlChannel0 (DMA_CTL_CH0)	00000000h
1004h	4	DMA ControlChannel1 (DMA_CTL_CH1)	00000000h
1008h	4	DMA ControlChannel2 (DMA_CTL_CH2)	00000000h
100Ch	4	DMA ControlChannel3 (DMA_CTL_CH3)	00000000h
1010h	4	DMA ControlChannel4 (DMA_CTL_CH4)	00000000h
1014h	4	DMA ControlChannel5 (DMA_CTL_CH5)	00000000h
1018h	4	DMA ControlChannel6 (DMA_CTL_CH6)	00000000h
101Ch	4	DMA ControlChannel7 (DMA_CTL_CH7)	00000000h
1100h	4	DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0)	00000000h
1104h	4	DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1)	00000000h
1108h	4	DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2)	00000000h
110Ch	4	DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3)	00000000h
1110h	4	DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4)	00000000h
1114h	4	DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5)	00000000h
1118h	4	DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6)	00000000h
111Ch	4	DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7)	00000000h
1200h	4	DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0)	00000000h
1204h	4	DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1)	00000000h
1208h	4	DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2)	00000000h
120Ch	4	DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3)	00000000h
1210h	4	DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4)	00000000h
1214h	4	DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5)	00000000h
1218h	4	DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6)	00000000h
121Ch	4	DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7)	00000000h
1300h	4	DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0)	00000000h
1304h	4	DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1)	00000000h

Table 4-2. Summary of Bus: 0, Device: 29, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1308h	4	DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2)	00000000h
130Ch	4	DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3)	00000000h
1310h	4	DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4)	00000000h
1314h	4	DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5)	00000000h
1318h	4	DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6)	00000000h
131Ch	4	DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7)	00000000h
1400h	4	DMA Channel Id Config (DMA_REGACCESS_CHID_CFG)	00000000h
1404h	4	DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP)	00000000h
1410h	4	D0i3 Control (D0I3C)	00000008h
1414h	4	Clock Gating And Soft Reset (CGSR)	00000000h
1418h	4	DMA Interrupt Enable (DMA_INT_EN)	00000000h
2000h	4	DMA VMM Mask (DMA_VMM_MASK)	00000000h

4.2.1 SAR0 - Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer.

While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.2 DAR0 - Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.3 LLP0 - Offset 10h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.4 CTL_LO0 - Offset 18h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.5 CTL_HI0 - Offset 1Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	000h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions: 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.6 SSTAT0 - Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.7 DSTAT0 - Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.8 SSTATAR0 - Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.9 DSTATAR0 - Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.10 CFG_LO0 - Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.11 CFG_HI0 - Offset 44h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***NOTE:*** For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***NOTE:*** For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.12 SAR1 - Offset 58h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.13 DAR1 - Offset 60h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.14 LLP1 - Offset 68h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.15 CTL_LO1 - Offset 70h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.16 CTL_HI1 - Offset 74h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	000h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.17 SSTAT1 - Offs et 78h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be

retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.18 DSTAT1 - Offset 80h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.19 SSTATAR1 - Offset 88h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.20 DSTATAR1 - Offset 90h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.21 CFG_LO1 - Offset 98h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.22 CFG_HI1 - Offset 9Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note:*** For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note:*** For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.23 SAR2 - Offset B0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.24 DAR2 - Offset B8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.25 LLP2 - Offset C0h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.26 CTL_LO2 - Offset C8h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.27 CTL_HI2 - Offset CCh

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	000h RW	**CH_WEIGHT:** Channel Weight: Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.28 SSTAT2 - Offset D0h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.29 DSTAT2 - Offset D8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.30 SSTATAR2 - Offset E0h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.31 DSTATAR2 - Offset E8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.32 CFG_LO2 - Offset F0h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + F0h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.33 CFG_HI2 - Offset F4h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note:*** For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note:*** For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.34 SAR3 - Offset 108h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer.

While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.35 DAR3 - Offset 110h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.36 LLP3 - Offset 118h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC!= 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.37 CTL_LO3 - Offset 120h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.38 CTL_HI3 - Offset 124h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	000h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions: 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.39 SSTAT3 - Offset 128h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be

retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.40 DSTAT3 - Offset 130h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.41 SSTATAR3 - Offset 138h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 138h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.42 DSTATAR3 - Offset 140h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.43 CFG_LO3 - Offset 148h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.44 CFG_HI3 - Offset 14Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.45 SAR4 - Offset 160h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.46 DAR4 - Offset 168h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.47 LLP4 - Offset 170h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC!= 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 170h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.48 CTL_LO4 - Offset 178h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 178h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.49 CTL_HI4 - Offset 17Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 17Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	000h RW	**CH_WEIGHT:** Channel Weight: Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions: 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.50 SSTAT4 - Offset 180h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 180h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.51 DSTAT4 - Offset 188h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.52 SSTATAR4 - Offset 190h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.53 DSTATAR4 - Offset 198h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.54 CFG_LO4 - Offset 1A0h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1A0h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.55 CFG_HI4 - Offset 1A4h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.56 SAR5 - Offset 1B8h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.57 DAR5 - Offset 1C0h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.58 LLP5 - Offset 1C8h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC!= 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.59 CTL_LO5 - Offset 1D0h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.60 CTL_HI5 - Offset 1D4h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	000h RW	**CH_WEIGHT:** Channel Weight: Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions: 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.61 SSTAT5 - Offset 1D8h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.62 DSTAT5 - Offset 1E0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.63 SSTATAR5 - Offset 1E8h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.64 DSTATAR5 - Offset 1F0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.65 CFG_LO5 - Offset 1F8h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1F8h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.66 CFG_HI5 - Offset 1FCh

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.67 SAR6 - Offset 210h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.68 DAR6 - Offset 218h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.69 LLP6 - Offset 220h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC!= 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.70 CTL_LO6 - Offset 228h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.71 CTL_HI6 - Offset 22Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 22Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	000h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.72 SSTAT6 - Offset 230h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.73 DSTAT6 - Offset 238h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.74 SSTATAR6 - Offset 240h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.75 DSTATAR6 - Offset 248h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 248h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.76 CFG_LO6 - Offset 250h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 250h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.77 CFG_HI6 - Offset 254h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Type	Size	Offset	Default
MMIO	32 bit	BAR + 254h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.78 SAR7 - Offset 268h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 268h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: * Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one in an OCP tracker. * If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. * If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. * If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. * Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) * Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. * The read-back behavior of the SAR/DAR registers can be overridden if the default setting of the EXACT_SAR_DAR_RDBACK parameter is changed from (0) to (1), and if of the GLOBAL_CFG. ENABLE_EXACT_SAR_DAR bit default is changed from (0) to (1). By modifying these 2 settings, the read-back behavior can be changed to the following: 1. Once an OCP command (Read/Write) is sent, and its response comes back, the SAR/DAR values will be updated. 2. If a channel is enabled, the SAR/DAR read-back values will indicate the latest updated byte address in INCR mode, while they reflect the programmed fixed values in FIXED mode. 3. If a channel is disabled, the read-back values of SAR/DAR will reflect whatever is physically programmed into these registers (whether through direct programming or through linked-list descriptor fetches). 4. Before the very first read or write take place, the SAR/DAR read-back values will be zeros. 5. Even though this behavior is far more accurate than the default behavior, there is an associated gate count increase. Enabling this feature (through setting the EXACT_SAR_DAR_RDBACK parameter), adds the following number of flops to the design: a. ((OUTSTANDING_READS + OUTSTANDING_WRITES) * (ADDR_WIDTH + 1)) + (2 * N_CHNLS * ADD_WIDTH) b. For N_CHNLS=8, ADDR_WIDTH=32, OUTSTANDING_READS=8 and OUTSTANDING_WRITES=2, this will result in 832 extra flops added to the design.

4.2.79 DAR7 - Offset 270h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 270h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register (Decrementing addresses are not supported). It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one.

4.2.80 LLP7 - Offset 278h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC!= 0 is used to set up the type of DMA transfer-single or multi-block. The method of updating the channel registers is a function of LLP.LOC!= 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC!= 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 278h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**Reserved**

4.2.81 CTL_LO7 - Offset 280h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 280h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	00h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future use. DO NOT change the zero default settings.
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**Reserved**
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	**Reserved**
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**Reserved**
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

4.2.82 CTL_HI7 - Offset 284h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 284h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	000h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	00000h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

4.2.83 SSTAT7 - Offset 288h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note: This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 288h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

4.2.84 DSTAT7 - Offset 290h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 290h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

4.2.85 SSTATAR7 - Offset 298h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 298h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

4.2.86 DSTATAR7 - Offset 2A0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

4.2.87 CFG_LO7 - Offset 2A8h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2A8h	00000203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	**Reserved**
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**Reserved**
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

4.2.88 CFG_HI7 - Offset 2ACh

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes {DST_PER_EXT[1:0], DST_PER[3:0]} which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsis limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes {SRC_PER_EXT[1:0], SRC_PER[3:0]} which covers the (0-63) range.
27:18	000h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	000h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID: Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. ***Note***: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

4.2.89 RAWTFR - Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**RAW:** Raw interrupt status

4.2.90 RAWBLOCK - Offset 2C8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**RAW:** Raw interrupt status

4.2.91 RAWSRCTRAN - Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**RAW:** Raw interrupt status

4.2.92 RAWDSTTRAN - Offset 2D8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**RAW:** Raw interrupt status

4.2.93 RAWERR - Offset 2E0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**RAW:** Raw interrupt status

4.2.94 STATUSTFR - Offset 2E8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**STATUS:** Interrupt status

4.2.95 STATUSBLOCK - Offset 2F0h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**STATUS:** Interrupt status

4.2.96 STATUSSRCTRAN - Offset 2F8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**STATUS:** Interrupt status

4.2.97 STATUSDSTTRAN - Offset 300h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr.Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 300h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**STATUS:** Interrupt status

4.2.98 STATUSERR - Offset 308h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 308h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**STATUS:** Interrupt status

4.2.99 MASKTFR - Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 310h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	00h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

4.2.100 MASKBLOCK - Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 318h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	00h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

4.2.101 MASKSRCTRAN - Offset 320h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 320h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	00h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

4.2.102 MASKDSTTRAN - Offset 328h

The contents of the Raw Status registers are masked with the contents of the

Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allowssoftware to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 328h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	00h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

4.2.103 MASKERR - Offset 330h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 330h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	00h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

4.2.104 CLEARTFR - Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 338h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

4.2.105 CLEARBLOCK - Offset 340h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 340h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

4.2.106 CLEARSRCTRAN - Offset 348h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 348h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

4.2.107 CLEARDSTTRAN - Offset 350h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 350h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

4.2.108 CLEARERR - Offset 358h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 358h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

4.2.109 STATUSINT - Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 360h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

4.2.110 DMACFGREG - Offset 398h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 398h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

4.2.111 CHENREG - Offset 3A0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h WO	**CH_EN_WE:** Channel enable write enable.
7:0	00h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

4.2.112 CLASSPRIORITY0_LO - Offset 3B8h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:11	000h RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	000h RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

4.2.113 CLASSPRIORITY0_HI - Offset 3BCh

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	000h RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	000h RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

4.2.114 CLASSPRIORITY1_LO - Offset 3C0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:11	000h RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	000h RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

4.2.115 CLASSPRIORITY1_HI - Offset 3C4h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:11	000h RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	000h RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

4.2.116 FIFOPARTITION0_LO - Offset 400h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 400h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0000h RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0000h RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

4.2.117 FIFOPARTITION0_HI - Offset 404h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 404h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:13	0000h RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0000h RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

4.2.118 FIFOPARTITION1_LO - Offset 408h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 408h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:13	0000h RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0000h RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

4.2.119 FIFOPARTITION1_HI - Offset 40Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:13	0000h RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0000h RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

4.2.120 SAI_ERR - Offset 410h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 410h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

4.2.121 GLOBAL_CFG - Offset 418h

GLOBAL_CFG: GLOBAL DMA Configuration Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 418h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000000h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits. DO NOT change the zero default settings.
4	0h RW	**DISABLE_EARLY_READ:** 0x1: Under best conditions, new Read command is driven one cycle AFTER last read DW has arrived in the FIFO (when number of outstanding reads is maxed) and/or one cycle AFTER last write DW is issued for same channel (when FIFO partition limit is maxed). 0x0: Under best conditions, new Read command is driven on SAME cycle as last read DW has arrived in the FIFO (when number of outstanding reads is maxed) and/or on SAME cycle as last write DW is issued for same channel (when FIFO partition limit is maxed). *** if Read/Write ports are registered, the read command will show on the bus 1 cycle after.
3	0h RW	**DISABLE_EARLY_DATA:** 0x1: Forces the MDataValid to be delayed from the MCmd on DMA Writes 0x0: Enables the MDataValid to be driven with the MCmd on DMA Writes (when possible)
2	0h RW	**ABORT_ON_OCP_ERR:** 0x1: ERR/FAIL fabric responses to DMA reads or writes triggers an abort sequence of the affected channel 0x0: ERR/FAIL fabric responses to DMA reads or writes does not trigger an abort sequence of the affected channel
1	0h RW	**ENABLE_EXACT_SAR_DAR:** 0x1: Enable exact SAR/DAR Read-back behavior. 0x0: Disables exact SAR/DAR Read-back Behavior. ** The EXACT_SAR_DAR_RDBACK parameter needs to be set to 1 for this field to be functional
0	0h RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers

4.2.122 DMA ControlChannel0 (DMA_CTL_CH0) - Offset 1000h

DMA Control register channel0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel0 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel0 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.123 DMA Control Channel1 (DMA_CTL_CH1) - Offset 1004h

DMA Control register channel1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel1 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel1 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel1. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.124 DMA Control Channel2 (DMA_CTL_CH2) - Offset 1008h

DMA Control register channel2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel2 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel2 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel2. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.125 DMA Control Channel3 (DMA_CTL_CH3) - Offset 100Ch

DMA Control register channel3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel3 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel3 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel3. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.126 DMA ControlChannel4 (DMA_CTL_CH4) - Offset 1010h

DMA Control register channel4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel4 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel4 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel4. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.127 DMA Control Channel5 (DMA_CTL_CH5) - Offset 1014h

DMA Control register channel5.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1014h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel5 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel5 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel5. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.128 DMA Control Channel6 (DMA_CTL_CH6) - Offset 1018h

DMA Control register channel6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1018h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel6 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel6 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel6. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.129 DMA Control Channel7 (DMA_CTL_CH7) - Offset 101Ch

DMA Control register channel7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 101Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 WR (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 RD (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel7 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel7 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel7. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

4.2.130 DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0) - Offset 1100h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.131 DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1) - Offset 1104h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.132 DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2) - Offset 1108h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.133 DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3) - Offset 110Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.134 DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4) - Offset 1110h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.135 DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5) - Offset 1114h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.136 DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6) - Offset 1118h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.137 DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7) - Offset 111Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 111Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.138 DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0) - Offset 1200h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1200h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.139 DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1) - Offset 1204h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.140 DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2) - Offset 1208h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.141 DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3) - Offset 120Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.142 DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4) - Offset 1210h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.143 DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5) - Offset 1214h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.144 DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6) - Offset 1218h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.145 DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7) - Offset 121Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 121Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

4.2.146 DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0) - Offset 1300h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1300h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.147 DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1) - Offset 1304h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1304h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.148 DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2) - Offset 1308h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 2.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1308h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.149 DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3) - Offset 130Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 130Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.150 DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4) - Offset 1310h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1310h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.151 DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5) - Offset 1314h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 5.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1314h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.152 DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6) - Offset 1318h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1318h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.153 DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7) - Offset 131Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 131Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** Device ID of Peripheral to be selected for HW Handshake.

4.2.154 DMA Channel ID Configuration (DMA_REGACCESS_CHID_CFG) - Offset 1400h

This register is used to program the Mreq info the DMA channel to be programmed next by FW.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1400h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**CHID_CFG:** Register access MREQINFO DMA channel id configuration.

4.2.155 DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP) - Offset 1404h

Sresp register for SRAM_base/OCP logic selection at DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1404h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:1	000000h RW/1C	**Peripheral BAR Remap Error Status (PER_BAR_REMAP_ERR):** This Error status bit is set on the peripheral BAR remap error and cleared when '1' is written to it. Bit 1-8 of this register indicate BAR remap error for the peripherals I2C0-7, Bits 9-14 indicate for UART0-5, bits 15-18 indicate for SPI0-3, Bits 19-20 indicate for I2S0-1 resp. and Bit 21 is reserved.
0	0h RW/1C	**Sresp Error Status Bit (ECC_ERR_SRESP):** This Error status bit is set on the RD/WR Sresp error on the DMA Rd/Wr ports and cleared when '1' is written to it.

4.2.156 D0i3 Control (D0I3C) - Offset 1410h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit(bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit(bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit(bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detect logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1410h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RW/1C	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

4.2.157 Clock Gating And Soft Reset (CGSR) - Offset 1414h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1414h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

4.2.158 DMA Interrupt Enable (DMA_INT_EN) - Offset 1418h

This register is used to enable the DMA combined interrupt for VC0/VC1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1418h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA Combined Interrupt For VC0/1 (DMA_COMB_INT_EN):** When set, enables the DMA combined interrupt to be generated on VC1 lines to MSI gen. When reset , enables the DMA Combined interrupt to be generated on VC0 lines to MSI gen.

4.2.159 DMA VMM Mask (DMA_VMM_MASK) - Offset 2000h

This register is used to program the VMM Mask for each peripheral.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Peripheral VMM Mask (PER_VMM_MASK):** When set, enables the VMM Mask for the peripheral. When reset, disables the VMM Mask for the peripheral. Bit 0-7 correspond to I2C0-7, Bits 8-13 correspond to UART0-5, bits 14-17 correspond to SPI0-3, Bits 18-19 correspond to I2S0-1 resp. and Bit 20 is reserved.

5 Pulse Width Modulation (PWM) Interface

5.1 PWM Configuration Registers Summary

This registers in Bus: 0, Device 29, Function 6.

Table 5-1. Summary of Bus: 0, Device: 29, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4BB70000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h

Table 5-1. Summary of Bus: 0, Device: 29, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

5.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4BB70000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BB7h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

5.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

5.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

5.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

5.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

5.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

5.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

5.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

5.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

5.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

5.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

5.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

5.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

5.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

5.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

5.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

5.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

5.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

5.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

5.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

5.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

5.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

5.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

5.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

5.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

5.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

5.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

5.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

5.2 PWM MMIO Registers Summary

Table 5-2. Summary of Bus: 0, Device: 29, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	TIMER1LOADCOUNT	00000000h
4h	4	TIMER1CURRENTVAL	80000000h
8h	4	TIMER1CONTROLREG	00000000h
Ch	4	TIMER1EOI	00000000h
10h	4	TIMER1INTSTAT	00000000h
14h	4	TIMER2LOADCOUNT	00000000h
18h	4	TIMER2CURRENTVAL	80000000h
1Ch	4	TIMER2CONTROLREG	00000000h
20h	4	TIMER2EOI	00000000h
24h	4	TIMER2INTSTAT	00000000h
28h	4	TIMER3LOADCOUNT	00000000h
2Ch	4	TIMER3CURRENTVAL	80000000h
30h	4	TIMER3CONTROLREG	00000000h
34h	4	TIMER3EOI	00000000h
38h	4	TIMER3INTSTAT	00000000h
3Ch	4	TIMER4LOADCOUNT	00000000h

Table 5-2. Summary of Bus: 0, Device: 29, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40h	4	TIMER4CURRENTVAL	80000000h
44h	4	TIMER4CONTROLREG	00000000h
48h	4	TIMER4EOI	00000000h
4Ch	4	TIMER4INTSTAT	00000000h
50h	4	TIMER5LOADCOUNT	00000000h
54h	4	TIMER5CURRENTVAL	80000000h
58h	4	TIMER5CONTROLREG	00000000h
5Ch	4	TIMER5EOI	00000000h
60h	4	TIMER5INTSTAT	00000000h
64h	4	TIMER6LOADCOUNT	00000000h
68h	4	TIMER6CURRENTVAL	80000000h
6Ch	4	TIMER6CONTROLREG	00000000h
70h	4	TIMER6EOI	00000000h
74h	4	TIMER6INTSTAT	00000000h
78h	4	TIMER7LOADCOUNT	00000000h
7Ch	4	TIMER7CURRENTVAL	80000000h
80h	4	TIMER7CONTROLREG	00000000h
84h	4	TIMER7EOI	00000000h
88h	4	TIMER7INTSTAT	00000000h
8Ch	4	TIMER8LOADCOUNT	00000000h
90h	4	TIMER8CURRENTVAL	80000000h
94h	4	TIMER8CONTROLREG	00000000h
98h	4	TIMER8EOI	00000000h
9Ch	4	TIMER8INTSTAT	00000000h
A0h	4	TIMERSINTSTAT	00000000h
A4h	4	TIMERSEOI	00000000h
A8h	4	TIMERSRAWINTSTAT	00000000h
ACh	4	TIMERSCOMPVERSION	3231302Ah
B0h	4	TIMER1LOADCOUNT2	00000000h
B4h	4	TIMER2LOADCOUNT2	00000000h
B8h	4	TIMER3LOADCOUNT2	00000000h
BCh	4	TIMER4LOADCOUNT2	00000000h
C0h	4	TIMER5LOADCOUNT2	00000000h
C4h	4	TIMER6LOADCOUNT2	00000000h
C8h	4	TIMER7LOADCOUNT2	00000000h
CCh	4	TIMER8LOADCOUNT2	00000000h
1000h	4	TIMER1LOADCOUNT	00000000h
1004h	4	TIMER1CURRENTVAL	80000000h
1008h	4	TIMER1CONTROLREG	00000000h

Table 5-2. Summary of Bus: 0, Device: 29, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
100Ch	4	TIMER1EOI	00000000h
1010h	4	TIMER1INTSTAT	00000000h
1014h	4	TIMER2LOADCOUNT	00000000h
1018h	4	TIMER2CURRENTVAL	80000000h
101Ch	4	TIMER2CONTROLREG	00000000h
1020h	4	TIMER2EOI	00000000h
1024h	4	TIMER2INTSTAT	00000000h
1028h	4	TIMER3LOADCOUNT	00000000h
102Ch	4	TIMER3CURRENTVAL	80000000h
1030h	4	TIMER3CONTROLREG	00000000h
1034h	4	TIMER3EOI	00000000h
1038h	4	TIMER3INTSTAT	00000000h
103Ch	4	TIMER4LOADCOUNT	00000000h
1040h	4	TIMER4CURRENTVAL	80000000h
1044h	4	TIMER4CONTROLREG	00000000h
1048h	4	TIMER4EOI	00000000h
104Ch	4	TIMER4INTSTAT	00000000h
1050h	4	TIMER5LOADCOUNT	00000000h
1054h	4	TIMER5CURRENTVAL	80000000h
1058h	4	TIMER5CONTROLREG	00000000h
105Ch	4	TIMER5EOI	00000000h
1060h	4	TIMER5INTSTAT	00000000h
1064h	4	TIMER6LOADCOUNT	00000000h
1068h	4	TIMER6CURRENTVAL	80000000h
106Ch	4	TIMER6CONTROLREG	00000000h
1070h	4	TIMER6EOI	00000000h
1074h	4	TIMER6INTSTAT	00000000h
1078h	4	TIMER7LOADCOUNT	00000000h
107Ch	4	TIMER7CURRENTVAL	80000000h
1080h	4	TIMER7CONTROLREG	00000000h
1084h	4	TIMER7EOI	00000000h
1088h	4	TIMER7INTSTAT	00000000h
108Ch	4	TIMER8LOADCOUNT	00000000h
1090h	4	TIMER8CURRENTVAL	80000000h
1094h	4	TIMER8CONTROLREG	00000000h
1098h	4	TIMER8EOI	00000000h
109Ch	4	TIMER8INTSTAT	00000000h
10A0h	4	TIMERSINTSTAT	00000000h
10A4h	4	TIMERSEOI	00000000h

Table 5-2. Summary of Bus: 0, Device: 29, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
10A8h	4	TIMERSRAWINTSTAT	00000000h
10ACh	4	TIMERSCOMPVERSION	3231302Ah
10B0h	4	TIMER1LOADCOUNT2	00000000h
10B4h	4	TIMER2LOADCOUNT2	00000000h
10B8h	4	TIMER3LOADCOUNT2	00000000h
10BCh	4	TIMER4LOADCOUNT2	00000000h
10C0h	4	TIMER5LOADCOUNT2	00000000h
10C4h	4	TIMER6LOADCOUNT2	00000000h
10C8h	4	TIMER7LOADCOUNT2	00000000h
10CCh	4	TIMER8LOADCOUNT2	00000000h
2000h	4	D0i3 Control (D0I3C)	00000008h
2004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

5.2.1 TIMER1LOADCOUNT - Offset 0h

Timer1 Load Count Register - Name: Timer1 Load Count Register Size: 8-32 bits Address Offset: 0x00 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER1LOADCOUNT:** Value to be loaded into Timer1. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.2 TIMER1CURRENTVAL - Offset 4h

Name: Timer1 Current Value Size: 8-32 bits Address Offset: 4 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER1CURRENTVAL:** Current Value of Timer1. This register is supported only when timer_1_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.3 TIMER1CONTROLREG - Offset 8h

Timer1 Control Register - Name: Timer1 Control Register Size: 4 bits Address Offset: 8 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer1. You can program each Timer1ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_1_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer1. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer1. 0: free_running mode 1: user_defined count mode. ***Note***: You must set the Timer1LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer1. 0: disable 1: enable

5.2.4 TIMER1EOI - Offset Ch

Timer1 End-of-Interrupt Register - Name: Timer1 End-of-Interrupt Register Size: 1 bit Address Offset: 12 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER1EOI:** Reading from this register returns all zeros (0) and clears the interrupt from Timer1.

5.2.5 TIMER1INTSTAT - Offset 10h

Timer1 Interrupt Status Register - Name: Timer1 Interrupt Status Register Size: 1 bit Address Offset: 16 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER1INTSTAT:** Contains the interrupt status for Timer1.

5.2.6 TIMER2LOADCOUNT - Offset 14h

Timer2 Load Count Register - Name: Timer2 Load Count Register Size: 8-32 bits Address Offset: 20 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER2LOADCOUNT:** Value to be loaded into Timer2. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.7 TIMER2CURRENTVAL - Offset 18h

Timer2 Current Value - Name: Timer2 Current Value Size: 8-32 bits Address Offset: 24 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER2CURRENTVAL:** Current Value of Timer2. This register is supported only when timer_2_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.8 TIMER2CONTROLREG - Offset 1Ch

Timer2 Control Register - Name: Timer2 Control Register Size: 3 bits Address Offset: 28 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer2. You can program each Timer2ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_2_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer2. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer2. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer2LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer2. 0: disable 1: enable

5.2.9 TIMER2EOI - Offset 20h

Timer2 End-of-Interrupt Register - Name: Timer2 End-of-Interrupt Register Size: 1 bit Address Offset: 32 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER2EOI:** Reading from this register returns all zeros (0) and clears the interrupt from Timer2.

5.2.10 TIMER2INTSTAT - Offset 24h

Timer2 Interrupt Status Register - Name: Timer2 Interrupt Status Register Size: 1 bit Address Offset: 36 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER2INTSTAT:** Contains the interrupt status for Timer2.

5.2.11 TIMER3LOADCOUNT - Offset 28h

Timer1 Load Count Register - Name: Timer3 Load Count Register Size: 8-32 bits Address Offset: 40 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER3LOADCOUNT:** Value to be loaded into Timer3. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.12 TIMER3CURRENTVAL - Offset 2Ch

Timer3 Current Value - Name: Timer3 Current Value Size: 8-32 bits Address Offset: 44 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2Ch	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER3CURRENTVAL:** Current Value of Timer3. This register is supported only when timer_3_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.13 TIMER3CONTROLREG - Offset 30h

Timer3 Control Register - Name: Timer3 Control Register Size: 4 bits Address Offset: 48 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer3. You can program each Timer3ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_3_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer3. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer3. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer3LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer3. 0: disable 1: enable

5.2.14 TIMER3EOI - Offset 34h

Timer3 End-of-Interrupt Register - Name: Timer3 End-of-Interrupt Register Size: 1 bit Address Offset: 52 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER3EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer3.

5.2.15 TIMER3INTSTAT - Offset 38h

Timer3 Interrupt Status Register - Name: Timer3 Interrupt Status Register Size: 1 bit Address Offset: 56 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER3INTSTAT:** Contains the interrupt status for Timer3.

5.2.16 TIMER4LOADCOUNT - Offset 3Ch

Timer4 Load Count Register - Name: Timer4 Load Count Register Size: 8-32 bits Address Offset: 60 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER4LOADCOUNT:** Value to be loaded into Timer4. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.17 TIMER4CURRENTVAL - Offset 40h

Timer4 Current Value Register - Name: Timer4 Current Value Size: 8-32 bits Address Offset: 64 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER4CURRENTVAL:** Current Value of Timer4. This register is supported only when timer_4_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.18 TIMER4CONTROLREG - Offset 44h

Timer4 Control Register - Name: Timer4 Control Register Size: 4 bits Address Offset: 68 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer4. You can program each Timer4ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_4_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer4. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer4. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer4LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer4. 0: disable 1: enable

5.2.19 TIMER4EOI - Offset 48h

Timer4 End-of-Interrupt Register - Name: Timer4 End-of-Interrupt Register Size: 1 bit Address Offset: 72 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER4EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer4.

5.2.20 TIMER4INTSTAT - Offset 4Ch

Timer4 Interrupt Status Register - Name: Timer4 Interrupt Status Register Size: 1 bit Address Offset: 76 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER4INTSTAT:** Contains the interrupt status for Timer4.

5.2.21 TIMER5LOADCOUNT - Offset 50h

Timer5 Load Count Register - Name: Timer5 Load Count Register Size: 8-32 bits Address Offset: 80 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER5LOADCOUNT:** Value to be loaded into Timer5. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.22 TIMER5CURRENTVAL - Offset 54h

Timer5 Current Value - Name: Timer5 Current Value Size: 8-32 bits Address Offset: 84 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER5CURRENTVAL:** Current Value of Timer5. This register is supported only when timer_5_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.23 TIMER5CONTROLREG - Offset 58h

Timer5 Control Register - Name: Timer5 Control Register Size: 4 bits Address Offset: 88 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer5. You can program each Timer5ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_5_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer5. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer5. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer5LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer5. 0: disable 1: enable

5.2.24 TIMER5EOI - Offset 5Ch

Timer5 End-of-Interrupt Register - Name: Timer5 End-of-Interrupt Register Size: 1 bit Address Offset: 92 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER5EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer5.

5.2.25 TIMER5INTSTAT - Offset 60h

Timer5 Interrupt Status Register - Name: Timer5 Interrupt Status Register Size: 1 bit Address Offset: 96 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER5INTSTAT:** Contains the interrupt status for Timer5.

5.2.26 TIMER6LOADCOUNT - Offset 64h

Timer6 Load Count Register - Name: Timer6 Load Count Register Size: 8-32 bits Address Offset: 100 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER6LOADCOUNT:** Value to be loaded into Timer6. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.27 TIMER6CURRENTVAL - Offset 68h

Timer6 Current Value Register - Name: Timer6 Current Value Size: 8-32 bits Address Offset: 104 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER6CURRENTVAL:** Current Value of Timer6. This register is supported only when timer_6_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.28 TIMER6CONTROLREG - Offset 6Ch

Timer6 Control Register - Name: Timer6 Control Register Size: 4 bits Address Offset: 108 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer6. You can program each Timer6ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_6_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer6. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer6. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer6LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer6. 0: disable 1: enable

5.2.29 TIMER6EOI - Offset 70h

Timer6 End-of-Interrupt Register - Name: Timer6 End-of-Interrupt Register Size: 1 bit Address Offset: 112 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER6EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer6.

5.2.30 TIMER6INTSTAT - Offset 74h

Timer6 Interrupt Status Register - Name: Timer6 Interrupt Status Register Size: 1 bit Address Offset: 116 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER6INTSTAT:** Contains the interrupt status for Timer6.

5.2.31 TIMER7LOADCOUNT - Offset 78h

Timer7 Load Count Register - Name: Timer7 Load Count Register Size: 8-32 bits Address Offset: 120 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER7LOADCOUNT:** Value to be loaded into Timer7. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.32 TIMER7CURRENTVAL - Offset 7Ch

Timer7 Current Register - Name: Timer7 Current Value Size: 8-32 bits Address Offset: 124 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER7CURRENTVAL:** Current Value of Timer7. This register is supported only when timer_7_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.33 TIMER7CONTROLREG - Offset 80h

Timer7 Control Register - Name: Timer7 Control Register Size: 4 bits Address Offset: 128 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer7. You can program each Timer7ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_7_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer7. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer7. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer7LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer7. 0: disable 1: enable

5.2.34 TIMER7EOI - Offset 84h

Timer7 End-of-Interrupt Register - Name: Timer7 End-of-Interrupt Register Size: 1 bit Address Offset: 132 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER7EOI:** Reading from this register returns all zeros (0) and clears the interrupt from Timer7.

5.2.35 TIMER7INTSTAT - Offset 88h

Timer7 Interrupt Status Register - Name: Timer7 Interrupt Status Register Size: 1 bit Address Offset: 136 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER7INTSTAT:** Contains the interrupt status for Timer7.

5.2.36 TIMER8LOADCOUNT - Offset 8Ch

Timer8 Load Count Register - Name: Timer8 Load Count Register Size: 8-32 bits Address Offset: 140 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER8LOADCOUNT:** Value to be loaded into Timer8. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.37 TIMER8CURRENTVAL - Offset 90h

Timer8 Current Value - Name: Timer8 Current Value Size: 8-32 bits Address Offset: 144 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER8CURRENTVAL:** Current Value of Timer8. This register is supported only when timer_8_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.38 TIMER8CONTROLREG - Offset 94h

Timer8 Control Register - Name: Timer8 Control Register Size: 4 bits Address Offset: 148 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer8. You can program each Timer8ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_8_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer8. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer8. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer8LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer8. 0: disable 1: enable

5.2.39 TIMER8EOI - Offset 98h

Timer8 End-of-Interrupt Register - Name: Timer8 End-of-Interrupt Register Size: 1 bit Address Offset: 152 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER8EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer8.

5.2.40 TIMER8INTSTAT - Offset 9Ch

Timer8 Interrupt Status Register - Name: Timer8 Interrupt Status Register Size: 1 bit Address Offset: 156 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER8INTSTAT:** Contains the interrupt status for Timer8.

5.2.41 TIMERSINTSTAT - Offset A0h

Timers Interrupt Status Register - Name: Timers Interrupt Status Register Size: 1-8 bits Address Offset: 0xa0 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSINTSTAT:** Contains the interrupt status of all timers in the component. If a bit of this register is 0, then the corresponding timer interrupt is not active and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts: 0 = either timer_intr or timer_intr_n is not active after masking 1 = either timer_intr or timer_intr_n is active after masking.

5.2.42 TIMERSEOI - Offset A4h

Timers End-of-Interrupt Register - Name: Timers End-of-Interrupt Register Size: 1-8 bits Address Offset: 0xa4 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSEOI:** Reading this register returns all zeros (0) and clears all active interrupts.

5.2.43 TIMERSRAWINTSTAT - Offset A8h

Timers Raw Interrupt Status Register - Name: Timers Raw Interrupt Status Register Size: 1-8 bits Address Offset: 0xa8 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSRAWINTSTAT:** The register contains the unmasked interrupt status of all timers in the component. 0 = either timer_intr or timer_intr_n is not active prior to masking 1 = either timer_intr or timer_intr_n is active prior to masking.

5.2.44 TIMERSCOMPVERSION - Offset ACh

Timers Component Version - Name: Timers Component Version Size: 32 bits Address Offset: 0xac Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	3231302Ah

Bit Range	Default & Access	Field Name (ID): Description
31:0	3231302Ah RO/V	**TIMERSCOMPVERSION:** Current revision number of the DW_apb_timers component.

5.2.45 TIMER1LOADCOUNT2 - Offset B0h

Timer1 Load Count2 Register - Name: Timer1 Load Count2 Register Size: 8-32 bits Address Offset: 0xb0 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER1LOADCOUNT2:** Value to be loaded into Timer1 when timer_1_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_1_toggle output.

5.2.46 TIMER2LOADCOUNT2 - Offset B4h

Timer2 Load Count2 Register - Name: Timer2 Load Count2 Register Size: 8-32 bits Address Offset: 180 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER2LOADCOUNT2:** Value to be loaded into Timer2 when timer_2_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_2_toggle output.

5.2.47 TIMER3LOADCOUNT2 - Offset B8h

Timer3 Load Count2 Register - Name: Timer3 Load Count2 Register Size: 8-32 bits Address Offset: 184 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER3LOADCOUNT2:** Value to be loaded into Timer3 when timer_3_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_3_toggle output.

5.2.48 TIMER4LOADCOUNT2 - Offset BCh

Timer4 Load Count2 Register - Name: Timer4 Load Count2 Register Size: 8-32 bits Address Offset: 188 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER4LOADCOUNT2:** Value to be loaded into Timer4 when timer_4_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_4_toggle output.

5.2.49 TIMER5LOADCOUNT2 - Offset C0h

Timer5 Load Count2 Register - Name: Timer5 Load Count2 Register Size: 8-32 bits Address Offset: 192 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER5LOADCOUNT2:** Value to be loaded into Timer5 when timer_5_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_5_toggle output.

5.2.50 TIMER6LOADCOUNT2 - Offset C4h

Timer6 Load Count2 Register - Name: Timer6 Load Count2 Register Size: 8-32 bits Address Offset: 196 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER6LOADCOUNT2:** Value to be loaded into Timer6 when timer_6_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_6_toggle output.

5.2.51 TIMER7LOADCOUNT2 - Offset C8h

Timer7 Load Count2 Register - Name: Timer7 Load Count2 Register Size: 8-32 bits Address Offset: 200 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER7LOADCOUNT2:** Value to be loaded into Timer7 when timer_7_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_7_toggle output.

5.2.52 TIMER8LOADCOUNT2 - Offset CCh

Timer8 Load Count2 Register - Name: Timer8 Load Count2 Register Size: 8-32 bits Address Offset: 204 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER8LOADCOUNT2:** Value to be loaded into Timer8 when timer_8_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_8_toggle output.

5.2.53 TIMER1LOADCOUNT - Offset 1000h

Timer1 Load Count Register - Name: Timer1 Load Count Register Size: 8-32 bits Address Offset: 0x00 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER1LOADCOUNT:** Value to be loaded into Timer1. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.54 TIMER1CURRENTVAL - Offset 1004h

Name: Timer1 Current Value Size: 8-32 bits Address Offset: 4 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER1CURRENTVAL:** Current Value of Timer1. This register is supported only when timer_1_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.55 TIMER1CONTROLREG - Offset 1008h

Timer1 Control Register - Name: Timer1 Control Register Size: 4 bits Address Offset: 8 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer1. You can program each Timer1ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_1_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer1. 0: not masked 1: masked
1	0h RW	**TIMER_MODE** Timer mode for Timer1. 0: free_running mode 1: user_defined count mode. ***Note***: You must set the Timer1LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer1. 0: disable 1: enable

5.2.56 TIMER1EOI - Offset 100Ch

Timer1 End-of-Interrupt Register - Name: Timer1 End-of-Interrupt Register Size: 1 bit Address Offset: 12 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER1EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer1.

5.2.57 TIMER1INTSTAT - Offset 1010h

Timer1 Interrupt Status Register - Name: Timer1 Interrupt Status Register Size: 1 bit Address Offset: 16 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER1INTSTAT:** Contains the interrupt status for Timer1.

5.2.58 TIMER2LOADCOUNT - Offset 1014h

Timer2 Load Count Register - Name: Timer2 Load Count Register Size: 8-32 bits Address Offset: 20 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1014h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER2LOADCOUNT:** Value to be loaded into Timer2. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.59 TIMER2CURRENTVAL - Offset 1018h

Timer2 Current Value - Name: Timer2 Current Value Size: 8-32 bits Address Offset: 24 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1018h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER2CURRENTVAL:** Current Value of Timer2. This register is supported only when timer_2_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.60 TIMER2CONTROLREG - Offset 101Ch

Timer2 Control Register - Name: Timer2 Control Register Size: 3 bits Address Offset: 28 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer2. You can program each Timer2ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 101Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_2_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer2. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer2. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer2LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer2. 0: disable 1: enable

5.2.61 TIMER2EOI - Offset 1020h

Timer2 End-of-Interrupt Register - Name: Timer2 End-of-Interrupt Register Size: 1 bit Address Offset: 32 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER2EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer2.

5.2.62 TIMER2INTSTAT - Offset 1024h

Timer2 Interrupt Status Register - Name: Timer2 Interrupt Status Register Size: 1 bit Address Offset: 36 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER2INTSTAT:** Contains the interrupt status for Timer2.

5.2.63 TIMER3LOADCOUNT - Offset 1028h

Timer1 Load Count Register - Name: Timer3 Load Count Register Size: 8-32 bits Address Offset: 40 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER3LOADCOUNT:** Value to be loaded into Timer3. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.64 TIMER3CURRENTVAL - Offset 102Ch

Timer3 Current Value - Name: Timer3 Current Value Size: 8-32 bits Address Offset: 44 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 102Ch	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER3CURRENTVAL:** Current Value of Timer3. This register is supported only when timer_3_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.65 TIMER3CONTROLREG - Offset 1030h

Timer3 Control Register - Name: Timer3 Control Register Size: 4 bits Address Offset: 48 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer3. You can program each Timer3ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_3_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer3. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer3. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer3LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer3. 0: disable 1: enable

5.2.66 TIMER3EOI - Offset 1034h

Timer3 End-of-Interrupt Register - Name: Timer3 End-of-Interrupt Register Size: 1 bit Address Offset: 52 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1034h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER3EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer3.

5.2.67 TIMER3INTSTAT - Offset 1038h

Timer3 Interrupt Status Register - Name: Timer3 Interrupt Status Register Size: 1 bit Address Offset: 56 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1038h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER3INTSTAT:** Contains the interrupt status for Timer3.

5.2.68 TIMER4LOADCOUNT - Offset 103Ch

Timer4 Load Count Register - Name: Timer4 Load Count Register Size: 8-32 bits Address Offset: 60 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 103Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER4LOADCOUNT:** Value to be loaded into Timer4. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.69 TIMER4CURRENTVAL - Offset 1040h

Timer4 Current Value Register - Name: Timer4 Current Value Size: 8-32 bits Address Offset: 64 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1040h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER4CURRENTVAL:** Current Value of Timer4. This register is supported only when timer_4_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.70 TIMER4CONTROLREG - Offset 1044h

Timer4 Control Register - Name: Timer4 Control Register Size: 4 bits Address Offset: 68 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer4. You can program each Timer4ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1044h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_4_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer4. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer4. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer4LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer4. 0: disable 1: enable

5.2.71 TIMER4EOI - Offset 1048h

Timer4 End-of-Interrupt Register - Name: Timer4 End-of-Interrupt Register Size: 1 bit Address Offset: 72 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER4EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer4.

5.2.72 TIMER4INTSTAT - Offset 104Ch

Timer4 Interrupt Status Register - Name: Timer4 Interrupt Status Register Size: 1 bit Address Offset: 76 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 104Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER4INTSTAT:** Contains the interrupt status for Timer4.

5.2.73 TIMER5LOADCOUNT - Offset 1050h

Timer5 Load Count Register - Name: Timer5 Load Count Register Size: 8-32 bits Address Offset: 80 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER5LOADCOUNT:** Value to be loaded into Timer5. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.74 TIMER5CURRENTVAL - Offset 1054h

Timer5 Current Value - Name: Timer5 Current Value Size: 8-32 bits Address Offset: 84 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1054h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER5CURRENTVAL:** Current Value of Timer5. This register is supported only when timer_5_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.75 TIMER5CONTROLREG - Offset 1058h

Timer5 Control Register - Name: Timer5 Control Register Size: 4 bits Address Offset: 88 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer5. You can program each Timer5ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_5_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer5. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer5. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer5LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer5. 0: disable 1: enable

5.2.76 TIMER5EOI - Offset 105Ch

Timer5 End-of-Interrupt Register - Name: Timer5 End-of-Interrupt Register Size: 1 bit Address Offset: 92 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 105Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER5EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer5.

5.2.77 TIMER5INTSTAT - Offset 1060h

Timer5 Interrupt Status Register - Name: Timer5 Interrupt Status Register Size: 1 bit Address Offset: 96 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1060h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER5INTSTAT:** Contains the interrupt status for Timer5.

5.2.78 TIMER6LOADCOUNT - Offset 1064h

Timer6 Load Count Register - Name: Timer6 Load Count Register Size: 8-32 bits Address Offset: 100 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1064h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER6LOADCOUNT:** Value to be loaded into Timer6. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.79 TIMER6CURRENTVAL - Offset 1068h

Timer6 Current Value Register - Name: Timer6 Current Value Size: 8-32 bits Address Offset: 104 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1068h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER6CURRENTVAL:** Current Value of Timer6. This register is supported only when timer_6_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.80 TIMER6CONTROLREG - Offset 106Ch

Timer6 Control Register - Name: Timer6 Control Register Size: 4 bits Address Offset: 108 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer6. You can program each Timer6ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 106Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_6_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer6. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer6. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer6LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer6. 0: disable 1: enable

5.2.81 TIMER6EOI - Offset 1070h

Timer6 End-of-Interrupt Register - Name: Timer6 End-of-Interrupt Register Size: 1 bit Address Offset: 112 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1070h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER6EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer6.

5.2.82 TIMER6INTSTAT - Offset 1074h

Timer6 Interrupt Status Register - Name: Timer6 Interrupt Status Register Size: 1 bit Address Offset: 116 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1074h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER6INTSTAT:** Contains the interrupt status for Timer6.

5.2.83 TIMER7LOADCOUNT - Offset 1078h

Timer7 Load Count Register - Name: Timer7 Load Count Register Size: 8-32 bits Address Offset: 120 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1078h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER7LOADCOUNT:** Value to be loaded into Timer7. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.84 TIMER7CURRENTVAL - Offset 107Ch

Timer7 Current Register - Name: Timer7 Current Value Size: 8-32 bits Address Offset: 124 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 107Ch	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER7CURRENTVAL:** Current Value of Timer7. This register is supported only when timer_7_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.85 TIMER7CONTROLREG - Offset 1080h

Timer7 Control Register - Name: Timer7 Control Register Size: 4 bits Address Offset: 128 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer7. You can program each Timer7ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_7_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer7. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer7. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer7LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer7. 0: disable 1: enable

5.2.86 TIMER7EOI - Offset 1084h

Timer7 End-of-Interrupt Register - Name: Timer7 End-of-Interrupt Register Size: 1 bit Address Offset: 132 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER7EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer7.

5.2.87 TIMER7INTSTAT - Offset 1088h

Timer7 Interrupt Status Register - Name: Timer7 Interrupt Status Register Size: 1 bit Address Offset: 136 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1088h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER7INTSTAT:** Contains the interrupt status for Timer7.

5.2.88 TIMER8LOADCOUNT - Offset 108Ch

Timer8 Load Count Register - Name: Timer8 Load Count Register Size: 8-32 bits Address Offset: 140 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 108Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER8LOADCOUNT:** Value to be loaded into Timer8. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

5.2.89 TIMER8CURRENTVAL - Offset 1090h

Timer8 Current Value - Name: Timer8 Current Value Size: 8-32 bits Address Offset: 144 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1090h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER8CURRENTVAL:** Current Value of Timer8. This register is supported only when timer_8_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

5.2.90 TIMER8CONTROLREG - Offset 1094h

Timer8 Control Register - Name: Timer8 Control Register Size: 4 bits Address Offset: 148 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer8. You can program each Timer8ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1094h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_8_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer8. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer8. 0: free-running mode 1: user-defined count mode. ***Note***: You must set the Timer8LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer8. 0: disable 1: enable

5.2.91 TIMER8EOI - Offset 1098h

Timer8 End-of-Interrupt Register - Name: Timer8 End-of-Interrupt Register Size: 1 bit Address Offset: 152 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1098h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER8EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer8.

5.2.92 TIMER8INTSTAT - Offset 109Ch

Timer8 Interrupt Status Register - Name: Timer8 Interrupt Status Register Size: 1 bit Address Offset: 156 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 109Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER8INTSTAT:** Contains the interrupt status for Timer8.

5.2.93 TIMERSINTSTAT - Offset 10A0h

Timers Interrupt Status Register - Name: Timers Interrupt Status Register Size: 1-8 bits Address Offset: 0xa0 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSINTSTAT:** Contains the interrupt status of all timers in the component. If a bit of this register is 0, then the corresponding timer interrupt is not active and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts: 0 = either timer_intr or timer_intr_n is not active after masking 1 = either timer_intr or timer_intr_n is active after masking.

5.2.94 TIMERSEOI - Offset 10A4h

Timers End-of-Interrupt Register - Name: Timers End-of-Interrupt Register Size: 1-8 bits Address Offset: 0xa4 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSEOI:** Reading this register returns all zeroes (0) and clears all active interrupts.

5.2.95 TIMERSRAWINTSTAT - Offset 10A8h

Timers Raw Interrupt Status Register - Name: Timers Raw Interrupt Status Register Size: 1-8 bits Address Offset: 0xa8 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSRAWINTSTAT:** The register contains the unmasked interrupt status of all timers in the component. 0 = either timer_intr or timer_intr_n is not active prior to masking 1 = either timer_intr or timer_intr_n is active prior to masking.

5.2.96 TIMERSCOMPVERSION - Offset 10ACh

Timers Component Version - Name: Timers Component Version Size: 32 bits Address Offset: 0xac Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10ACh	3231302Ah

Bit Range	Default & Access	Field Name (ID): Description
31:0	3231302Ah RO/V	**TIMERSCOMPVERSION:** Current revision number of the DW_apb_timers component.

5.2.97 TIMER1LOADCOUNT2 - Offset 10B0h

Timer1 Load Count2 Register - Name: Timer1 Load Count2 Register Size: 8-32 bits Address Offset: 0xb0 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER1LOADCOUNT2:** Value to be loaded into Timer1 when timer_1_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_1_toggle output.

5.2.98 TIMER2LOADCOUNT2 - Offset 10B4h

Timer2 Load Count2 Register - Name: Timer2 Load Count2 Register Size: 8-32 bits Address Offset: 180 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER2LOADCOUNT2:** Value to be loaded into Timer2 when timer_2_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_2_toggle output.

5.2.99 TIMER3LOADCOUNT2 - Offset 10B8h

Timer3 Load Count2 Register - Name: Timer3 Load Count2 Register Size: 8-32 bits Address Offset: 184 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER3LOADCOUNT2:** Value to be loaded into Timer3 when timer_3_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_3_toggle output.

5.2.100 TIMER4LOADCOUNT2 - Offset 10BCh

Timer4 Load Count2 Register - Name: Timer4 Load Count2 Register Size: 8-32 bits Address Offset: 188 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER4LOADCOUNT2:** Value to be loaded into Timer4 when timer_4_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_4_toggle output.

5.2.101 TIMER5LOADCOUNT2 - Offset 10C0h

Timer5 Load Count2 Register - Name: Timer5 Load Count2 Register Size: 8-32 bits Address Offset: 192 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER5LOADCOUNT2:** Value to be loaded into Timer5 when timer_5_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_5_toggle output.

5.2.102 TIMER6LOADCOUNT2 - Offset 10C4h

Timer6 Load Count2 Register - Name: Timer6 Load Count2 Register Size: 8-32 bits Address Offset: 196 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER6LOADCOUNT2:** Value to be loaded into Timer6 when timer_6_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_6_toggle output.

5.2.103 TIMER7LOADCOUNT2 - Offset 10C8h

Timer7 Load Count2 Register - Name: Timer7 Load Count2 Register Size: 8-32 bits Address Offset: 200 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER7LOADCOUNT2:** Value to be loaded into Timer7 when timer_7_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_7_toggle output.

5.2.104 TIMER8LOADCOUNT2 - Offset 10CCh

Timer8 Load Count2 Register - Name: Timer8 Load Count2 Register Size: 8-32 bits Address Offset: 204 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER8LOADCOUNT2:** Value to be loaded into Timer8 when timer_8_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_8_toggle output.

5.2.105 D0i3 Control (D0I3C) - Offset 2000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

5.2.106 Clock Gating And Soft Reset (CGSR) - Offset 2004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

6 Inter-Integrated Circuit (I2C) Interface

6.1 I2C Configuration Registers Summary

This registers of the Intel® PSE Inter-Integrated Circuit I2C devices. This contains multiple Intel® PSE Inter-Integrated Circuit, I2C controller devices:

- Intel® PSE I2C Controller #0 - Bus: 0, Device: 27, Function: 0
- Intel® PSE I2C Controller #1 - Bus: 0, Device: 27, Function: 1
- Intel® PSE I2C Controller #2 - Bus: 0, Device: 27, Function: 2
- Intel® PSE I2C Controller #3 - Bus: 0, Device: 27, Function: 3
- Intel® PSE I2C Controller #4 - Bus: 0, Device: 27, Function: 4
- Intel® PSE I2C Controller #5 - Bus: 0, Device: 27, Function: 5
- Intel® PSE I2C Controller #6 - Bus: 0, Device: 27, Function: 6

DID Values:

Intel® PSE I2C Controller #0 - D27: F0 - 4BB9h

Intel® PSE I2C Controller #1 - D27: F1 - 4BBAh

Intel® PSE I2C Controller #2 - D27: F2 - 4BBBh

Intel® PSE I2C Controller #3 - D27: F3 - 4BBCh

Intel® PSE I2C Controller #4 - D27: F4 - 4BBDh

Intel® PSE I2C Controller #5 - D27: F5 - 4BBEh

Intel® PSE I2C Controller #6 - D27: F6 - 4BBFh

Table 6-1. Summary of Bus: 0, Device: 27, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4BB90000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h

Table 6-1. Summary of Bus: 0, Device: 27, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

6.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4BB90000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BB9h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

6.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

6.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

6.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device

Bit Range	Default & Access	Field Name (ID): Description
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

6.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

6.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

6.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

6.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

6.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

6.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

6.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

6.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

6.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

6.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

6.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

6.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

6.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

6.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

6.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

6.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

6.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

6.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

6.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

6.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

6.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

6.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

6.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

6.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

6.2 I2C MMIO Registers Summary

Table 6-2. Summary of Bus: 0, Device: 27, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	IC_CON	00000067h
4h	4	IC_TAR	00000055h
8h	4	IC_SAR	00000055h
Ch	4	IC_HS_MADDR	00000001h
10h	4	IC_DATA_CMD	00000000h
14h	4	IC_SS_SCL_HCNT	000001E8h
18h	4	IC_SS_SCL_LCNT	000001F3h
1Ch	4	IC_FS_SCL_HCNT	00000071h
20h	4	IC_FS_SCL_LCNT	0000007Ch
24h	4	IC_HS_SCL_HCNT	00000029h
28h	4	IC_HS_SCL_LCNT	00000032h
2Ch	4	IC_INTR_STAT	00000000h
30h	4	IC_INTR_MASK	000008FFh
34h	4	IC_RAW_INTR_STAT	00000000h
38h	4	IC_RX_TL	00000000h
3Ch	4	IC_TX_TL	00000000h
40h	4	IC_CLR_INTR	00000000h
44h	4	IC_CLR_RX_UNDER	00000000h
48h	4	IC_CLR_RX_OVER	00000000h
4Ch	4	IC_CLR_TX_OVER	00000000h
50h	4	IC_CLR_RD_REQ	00000000h
54h	4	IC_CLR_TX_ABRT	00000000h
58h	4	IC_CLR_RX_DONE	00000000h
5Ch	4	IC_CLR_ACTIVITY	00000000h
60h	4	IC_CLR_STOP_DET	00000000h
64h	4	IC_CLR_START_DET	00000000h
68h	4	IC_CLR_GEN_CALL	00000000h
6Ch	4	IC_ENABLE	00000000h
70h	4	IC_STATUS	00000006h
74h	4	IC_TXFLR	00000000h
78h	4	IC_RXFLR	00000000h
7Ch	4	IC_SDA_HOLD	00000005h
80h	4	IC_TX_ABRT_SOURCE	00000000h
88h	4	IC_DMA_CR	00000000h
8Ch	4	IC_DMA_TDLR	00000000h
90h	4	IC_DMA_RDLR	00000000h

Table 6-2. Summary of Bus: 0, Device: 27, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
94h	4	IC_SDA_SETUP	00000002h
98h	4	IC_ACK_GENERAL_CALL	00000000h
9Ch	4	IC_ENABLE_STATUS	00000000h
A0h	4	IC_FS_SPKLEN	00000005h
A4h	4	IC_HS_SPKLEN	00000002h
A8h	4	IC_CLR_RESTART_DET	00000000h
F4h	4	IC_COMP_PARAM_1	003F3FEEh
F8h	4	IC_COMP_VERSION	3230322Ah
FCh	4	IC_COMP_TYPE	44570140h
1000h	4	D0i3 Control (D0I3C)	00000008h
1004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

6.2.1 IC_CON - Offset 0h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access:
- If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only.
- If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only.
- If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only.
- If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only.
- If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only.
- If configuration parameter IC_SMBUS=0, bit 17 is read only.
- If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000067h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. ***Note***: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the present signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. ***Note***: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) ***Note***: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. ***Note***: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

6.2.2 IC_TAR - Offset 4h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions is true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). **Note**: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000055h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

6.2.3 IC_SAR - Offset 8h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000055h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. ***Note***: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

6.2.4 IC_HS_MADDR - Offset Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

6.2.5 IC_DATA_CMD - Offset 10h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0
Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. ***Note***: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. In order to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

6.2.6 IC_SS_SCL_HCNT - Offset 14h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	000001E8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. ***Note***: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

6.2.7 IC_SS_SCL_LCNT - Offset 18h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	000001F3h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

6.2.8 IC_FS_SCL_HCNT - Offset 1Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000071h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

6.2.9 IC_FS_SCL_LCNT - Offset 20h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	0000007Ch

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

6.2.10 IC_HS_SCL_HCNT - Offset 24h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000029h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

6.2.11 IC_HS_SCL_LCNT - Offset 28h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000032h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

6.2.12 IC_INTR_STAT - Offset 2Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

6.2.13 IC_INTR_MASK - Offset 30h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	000008FFh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

6.2.14 IC_RAW_INTR_STAT - Offset 34h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. ***Note***: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. ***Note***: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. ***Note***: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. ***Note***: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

6.2.15 IC_RX_TL - Offset 38h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

6.2.16 IC_TX_TL - Offset 3Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

6.2.17 IC_CLR_INTR - Offset 40h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

6.2.18 IC_CLR_RX_UNDER - Offset 44h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

6.2.19 IC_CLR_RX_OVER - Offset 48h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

6.2.20 IC_CLR_TX_OVER - Offset 4Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

6.2.21 IC_CLR_RD_REQ - Offset 50h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

6.2.22 IC_CLR_TX_ABRT - Offset 54h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

6.2.23 IC_CLR_RX_DONE - Offset 58h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

6.2.24 IC_CLR_ACTIVITY - Offset 5Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

6.2.25 IC_CLR_STOP_DET - Offset 60h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

6.2.26 IC_CLR_START_DET - Offset 64h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

6.2.27 IC_CLR_GEN_CALL - Offset 68h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

6.2.28 IC_ENABLE - Offset 6Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. ***Note***: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

6.2.29 IC_STATUS - Offset 70h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active **Note**: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty locations, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

6.2.30 IC_TXFLR - Offset 74h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted. The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

6.2.31 IC_RXFLR - Offset 78h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE. The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

6.2.32 IC_SDA_HOLD - Offset 7Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

6.2.33 IC_TX_ABRT_SOURCE - Offset 80h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. ***Note***: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgment for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

6.2.34 IC_DMA_CR - Offset 88h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

6.2.35 IC_DMA_TDLR - Offset 8Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

6.2.36 IC_DMA_RDLR - Offset 90h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

6.2.37 IC_SDA_SETUP - Offset 94h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0.
Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000002h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

6.2.38 IC_ACK_GENERAL_CALL - Offset 98h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

6.2.39 IC_ENABLE_STATUS - Offset 9Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only been valid as soon as bit 0 is read as '0'.
Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. ***Note***: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. ***Note***: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. ***Note***: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. ***Note***: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. ***Note***: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

6.2.40 IC_FS_SPKLEN - Offset A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit. This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. The relevant I2C requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000005h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

6.2.41 IC_HS_SPKLEN - Offset A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. The relevant I2C requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000002h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

6.2.42 IC_CLR_RESTART_DET - Offset A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

6.2.43 IC_COMP_PARAM_1 - Offset F4h

Component Parameter Register 1 - Component Parameter Register 1
Note: This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	BAR + F4h	003F3FEEh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 -0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

6.2.44 IC_COMP_VERSION - Offset F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	3230322Ah

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION**

6.2.45 IC_COMP_TYPE - Offset FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + FCh	44570140h

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Design ware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

6.2.46 D0i3 Control (D0I3C) - Offset 1000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done). The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately

tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

6.2.47 Clock Gating And Soft Reset (CGSR) - Offset 1004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

7 Controller Area Network (CAN) Interface

7.1 CAN Configuration Registers Summary

This registers in Bus: 0, Device 24, Function 1 and 2.

DID Values:

- Intel® PSE CAN Controller #0:- D24: F1 - 4BC1h
- Intel® PSE CAN Controller #1:- D24: F2 - 4BC2h

Table 7-1. Summary of Bus: 0, Device: 24, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4BC10000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h

Table 7-1. Summary of Bus: 0, Device: 24, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

7.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 0h	4BC10000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BC1h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

7.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort

Bit Range	Default & Access	Field Name (ID): Description
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

7.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

7.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

7.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

7.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

7.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

7.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

7.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

7.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

7.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

7.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

7.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

7.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

7.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

7.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

7.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

7.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

7.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

7.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

7.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

7.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

7.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

7.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

7.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

7.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

7.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

7.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:24, F:1] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

7.2 CAN MMIO Registers Summary

Table 7-2. Summary of Bus: 0, Device: 24, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Core Release Register (CREL)	32150323h
4h	4	Endian Register (ENDN)	87654321h
8h	4	Customer Register (CUST)	00000000h
Ch	4	Fast Bit Timing and Prescaler Register (DBTP)	00000A33h
10h	4	Test Register (TEST)	00000000h
14h	4	RAM Watchdog (RWD)	00000000h
18h	4	CC Control Register (CCCR)	00000001h
1Ch	4	Bit Timing and Prescaler Register (BTP)	06000A03h
20h	4	Timestamp Counter Configuration (TSCC)	00000000h
24h	4	Timestamp Counter Value (TSCV)	00000000h
28h	4	Timeout Counter Configuration (TOCC)	FFFF0000h
2Ch	4	Timeout Counter Value (TOCV)	0000FFFFh
40h	4	Error Counter Register (ECR)	00000000h
44h	4	Protocol Status Register (PSR)	00000707h
48h	4	Transmitter Delay Compensation Register (TDCR)	00000000h
50h	4	Interrupt Register (IR)	00000000h

Table 7-2. Summary of Bus: 0, Device: 24, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
54h	4	Interrupt Enable (IE)	00000000h
58h	4	Interrupt Line Select (ILS)	00000000h
5Ch	4	Interrupt Line Enable (ILE)	00000000h
80h	4	Global Filter Configuration (GFC)	00000000h
84h	4	Standard ID Filter Configuration (SIDFC)	00000000h
88h	4	Extended ID Filter Configuration (XIDFC)	00000000h
90h	4	Extended ID AND Mask (XIDAM)	1FFFFFFFh
94h	4	High Priority Message Status (HPMS)	00000000h
98h	4	New Data 1 (NDAT1)	00000000h
9Ch	4	New Data 2 (NDAT2)	00000000h
A0h	4	RX FIFO 0 Configuration (RXF0C)	00000000h
A4h	4	RX FIFO 0 Status (RXF0S)	00000000h
A8h	4	RX FIFO 0 Acknowledge (RXF0A)	00000000h
ACh	4	RX Buffer Configuration (RXBC)	00000000h
B0h	4	RX FIFO 1 Configuration (RXF1C)	00000000h
B4h	4	RX FIFO 1 Status (RXF1S)	00000000h
B8h	4	RX FIFO 1 Acknowledge (RXF1A)	00000000h
BCh	4	Rx Buffer / FIFO Element Size Configuration (RXESC)	00000000h
C0h	4	TX Buffer Configuration (TXBC)	00000000h
C4h	4	TX FIFO/Queue Status (TXFQS)	00000000h
C8h	4	TX Buffer Element Size Configuration (TXESC)	00000000h
CCh	4	TX Buffer Request Pending (TXBRP)	00000000h
D0h	4	TX Buffer Add Request (TXBAR)	00000000h
D4h	4	TX Buffer Cancellation Request (TXBCR)	00000000h
D8h	4	TX Buffer Transmission Occured (TXBTO)	00000000h
DCh	4	TX Buffer Cancellation Finished (TXBCF)	00000000h
E0h	4	TX Buffer Transmission Interrupt Enable (TXBTIE)	00000000h
E4h	4	Tx Buffer Cancellation Finished Interrupt Enable (TXBCIE)	00000000h
F0h	4	TX Event FIFO Configuration (TXEFC)	00000000h
F4h	4	TX Event FIFO Status (TXEFS)	00000000h
F8h	4	TX Event FIFO Acknowledge (TXEFA)	00000000h
100h	4	TT Trigger Memory Configuration (TTTMC)	00000000h
104h	4	TT Reference Message Configuration (TTRMC)	00000000h
108h	4	TT Operation Configuration (TTOCF)	00010000h
10Ch	4	TT Matrix Limits (TTMLM)	00000000h
110h	4	TUR Configuration (TURCF)	10000000h
114h	4	TT Operation Control (TTOCN)	00000000h
118h	4	TT Global Time Preset (TTGTP)	00000000h
11Ch	4	TT Time Mark (TTTMK)	00000000h

Table 7-2. Summary of Bus: 0, Device: 24, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
120h	4	TT Interrupt Register (TTIR)	00000000h
124h	4	TT Interrupt Enable (TTIE)	00000000h
128h	4	TT Interrupt Line Select (TTILS)	00000000h
12Ch	4	TT Operation Status (TTOST)	00000080h
130h	4	TUR Numerator Actual (TURNA)	00000000h
134h	4	TT Local and Global Time (TTLGT)	00000000h
138h	4	TT Cycle Time & Count (TTCTC)	003F0000h
13Ch	4	TT Capture Time (TTCPT)	00000000h
140h	4	TT Cycle Sync Mark (TTCSM)	00000000h
500h	4	Message RAM Size (MSG_RAM_SIZE)	00004600h
504h	4	CTL	00000000h
508h	4	Interrupt Control (INT_CTL)	00000000h
50Ch	4	Interrupt Status (INT_STAT)	00000000h
510h	4	MSGRAM Address Conflict Status (MSGRAM_ADDR_CONFLICT_STAT)	00000000h
514h	4	TTCAN TIMESTAMP CONTROL REGISTER (TIMESTAMP_CTL)	00000000h
518h	4	TTCAN LOCAL TIMESTAMP HIGH (LOCALTIMESTAMP_HIGH)	00000000h
51Ch	4	TTCAN LOCAL TIMESTAMP LOW (LOCALTIMESTAMP_LOW)	00000000h
600h	4	CAN Parity Error Control and Status (PAR_CTL_STAT)	00000003h
604h	4	Parity Error Offset (PAR_ERR_OFFSET)	00000000h
608h	4	Parity Error Injection Control and Status (PAR_EINJ_CTL_STAT)	00000000h
60Ch	4	Parity Error Injection Offset (PAR_EINJ_OFFSET)	00000000h
610h	4	Parity Error Injection Data Mask (PAR_EINJ_DATA_MASK)	00000000h
614h	4	Parity Error Injection Parity Mask (PAR_EINJ_PARITY_MASK)	00000000h
8000h	4	D0i3 Control (D0I3C)	00000008h
8004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

7.2.1 Core Release Register (CREL) - Offset 0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	32150323h

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Core Release (REL):** One digit, BCD-coded. - @@jstokes, Need to wait for IP delivery for reset value
27:24	2h RO	**Step of Core Release (STEP):** One digit, BCD-coded. - @@jstokes, Need to wait for IP delivery for reset value
23:20	1h RO	**Sub-step of Core Release (SUBSTEP):** One digit, BCD-coded. eed to wait for IP delivery for reset value

Bit Range	Default & Access	Field Name (ID): Description
19:16	5h RO	**Time Stamp Year (YEAR):** One digit, BCD-coded. @@jstokes, Need to wait for IP integration for reset value
15:8	03h RO	**Time Stamp Month (MON):** Two digits, BCD-coded. @@jstokes, Need to wait for IP integration for reset value
7:0	23h RO	**Time Stamp Day (DAY):** Two digits, BCD-coded. @@jstokes, Need to wait for IP integration for reset value

7.2.2 Endian Register (ENDN) - Offset 4h

Endianness Test Value

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	87654321h

Bit Range	Default & Access	Field Name (ID): Description
31:0	87654321h RO	**Endianness Test Value (ETV):** The endianness test value is 0x87654321

7.2.3 Customer Register (CUST) - Offset 8h

Address 0x08 is reserved for an optional 32 bit customer-specific register. The Customer Register is intended to hold customer-specific configuration, control, and status bits.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Customer Register Field (CUST_FIELD):** Customer specific register field

7.2.4 Fast Bit Timing and Prescaler Register (DBTP) - Offset Ch

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 25 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 m_ttcan_cclk periods. tq = (FBRP + 1) m_ttcan_cclk period. FTSEG1 is the sum of Prop_Seg and Phase_Seg1. FTSEG2 is Phase_Seg2. Therefore the length of the bit time is (programmed values) [FTSEG1 + FTSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq. The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Note: With a CAN clock (m_ttcan_cclk) of 8 MHz, the reset value of 0x00000A33 configures the M_TTCAN for a fast bit rate of 500 kBit/s.

Note: The bit rate configured for the CAN FD data phase via FBTP must be higher or equal to the bit rate configured for the arbitration phase via BTP.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000A33h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/L	**Transceiver Delay Compensation (TDC):** 0= Transceiver Delay Compensation disabled 1= Transceiver Delay Compensation enabled
22:21	0h RO	**Reserved**
20:16	00h RW/L	**Fast Baud Rate Prescaler (FBRP):** 0x00-0x1F: The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:13	0h RO	**Reserved**
12:8	0Ah RW/L	**Fast time segment before sample point (FTSEG1):** 0x1-0xF: Valid values are 1 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7:4	3h RW/L	**Fast time segment after sample point (FTSEG2):** 0x0-0x7: Valid values are 0 to 7. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
3:0	3h RW/L	**Fast (Re) Synchronization Jump Width (FSJW):** 0x0-0x3: Valid values are 0 to 3. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

7.2.5 Test Register (TEST) - Offset 10h

Write access to the Test Register has to be enabled by setting bit CCCR.TEST to. All Test Register functions are set to their reset values when bit CCCR.TEST is reset. Loop Back Mode and software control of pin can*_tx_o are hardware test modes. Programming of TX not equal to h0 may disturb the message transfer on the CAN bus.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**Receive Pin (RX):** Monitors the actual value of pin can*_rx_i 0= The CAN bus is dominant (can*_rx_i = 0) 1= The CAN bus is recessive (can*_rx_i = 1)
6:5	0h RW/L	**Control of Transmit Pin (TX):** 00 Reset value, can*_tx_o controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin can*_tx_o 10 Dominant (0) level at pin can*_tx_o 11 Recessive (1) at pin m_ttcan_tx
4	0h RW/L	**Loop Back Mode (LBCK):** 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled
3	0h RO	**Check ASC Transmit Control (CAT):** Monitors level at output pin ttcan*_asct_i. 0= Output pin ttcan*_asct_i = 0 1= Output pin ttcan*_asct_i = 1
2	0h RO	**Check ASC Multiplexer Control (CAM):** Monitors level at output pin ttcan*_ascm_i. 0= Output pin ttcan*_ascm_i = 0 1= Output pin ttcan*_ascm_i = 1
1	0h RW/L	**Check ASC Transmit Control (TAT):** Controls output pin ttcan*_asct_i in test mode, ORed with the signal from the FSE 0= Level at pin ttcan*_asct_i controlled by FSE 1= Level at pin ttcan*_asct_i = 1
0	0h RW/L	**Test ASC Transmit Control (TAM):** Controls output pin ttcan*_ascm_i in test mode, ORed with the signal from the FSE 0= Level at pin ttcan*_ascm_i controlled by FSE 1= Level at pin ttcan*_ascm_i = 1

7.2.6 RAM Watchdog (RWD) - Offset 14h

The RAM Watchdog monitors the READY output of the Message RAM (m_ttcan_aeim_ready). A Message RAM access via the M_TTCANs Generic Master Interface (m_ttcan_aeim_sel active) starts the Message RAM Watchdog Counter with the value configured by RWD.WDC. The counter is reloaded with RWD.WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag IR.WDI is set. The RAM Watchdog Counter is clocked by the Host clock (m_ttcan_hclk).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Watchdog Value (WDV):** Actual Message RAM Watchdog Counter Value.
7:0	00h RW/L	**Watchdog Configuration (WDC):** Start value of the Message RAM Watchdog Counter. With the reset value of 00 the counter is disabled.

7.2.7 CC Control Register (CCCR) - Offset 18h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/L	**Non ISO Operation (NISO):** If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO11898-1 1= CAN FD frame format according to Bosch CAN FD Specification V1.0
14	0h RW/L	**Transmit Pause (TXP):** If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame. 0= Transmit pause disabled 1= Transmit pause enabled
13	0h RW/L	**Edge Filtering during Bus Integration (EFBI):** 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization
12	0h RW/L	**Protocol Exception Handling Disable (PXHD):** 0= Protocol exception handling enabled 1= Protocol exception handling disabled
11:10	0h RO	**Reserved**
9	0h RW/L	**Bit Rate Switch Enable (BRSE):** 0 = Bit rate switching for transmission disabled 1 = Bit rate switching for transmission enabled
8	0h RW/L	**FD Operation Enable (FDOE):** 0 = FD operation disabled 1 = FD operation enabled

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/V/L	**Test Mode Enable (TEST):** 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
6	0h RW/L	**Disable Automatic Retransmission (DAR):** 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled
5	0h RW/V/L	**Bus Monitoring Mode (MON):** Bit MON can only be set by the Host when both CCE and INIT are set to 1. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
4	0h RW	**Clock Stop Request (CSR):** 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	0h RO	**Clock Stop Acknowledge (CSA):** 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk
2	0h RW/V/L	**Restricted Operation Mode (ASM):** Bit ASM can only be set by the Host when both CCE and INIT are set to 1. The bit can be reset by the Host at any time. 0= Normal CAN operation 1= Restricted Operation Mode active This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
1	0h RW/L	**Configuration Change Enable (CCE):** 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = 1)
0	1h RW	**INIT:** 0= Normal Operation 1= Initialization is started

7.2.8 Bit Timing and Prescaler Register (BTP) - Offset 1Ch

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 81 time quanta. The CAN time quantum may be programmed in the range of 1 to 1024 m_ttcan_cclk periods. tq = (BRP + 1) m_ttcan_cclk period. TSEG1 is the sum of Prop_Seg and Phase_Seg1. TSEG2 is Phase_Seg2. Therefore the length of the bit time is (programmed values) [TSEG1 + TSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq. The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	06000A03h

Bit Range	Default & Access	Field Name (ID): Description
31:25	03h RW/L	**Nominal (Re) Synchronization Jump Width (NSJW):** 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
24:16	000h RW/L	**Nominal Bit Rate Prescaler (BRP):** 0x000-0x1FF. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 1023. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. ***Note***: With a CAN clock (m_ttcan_cclk) of 8 MHz, the reset value of 0x00000A33 configures the M_TTCAN for a bit rate of 500 kBit/s.
15	0h RO	**Reserved**
14:8	0Ah RW/L	**Time segment before sample point (TSEG1):** 0x01-0xFF. Valid values are 1 to 63. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7	0h RO	**Reserved**
6:0	03h RW/L	**Time segment after sample point (TSEG2):** 0x0-0x7F. Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.

7.2.9 Timestamp Counter Configuration (TSCC) - Offset 20h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW/L	**Timestamp Counter Prescaler (TCP):** 0x0-0xF. Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:2	0h RO	**Reserved**
1:0	0h RW/L	**Timestamp Select (TSS):** 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as 00

7.2.10 Timestamp Counter Value (TSCV) - Offset 24h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C	**Timestamp Counter (TSC):** The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = 01, the Timestamp Counter is incremented in multiples of CAN bit times [116] depending on the configuration of TSCC.TCP. Awr ap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = 10, TSC reflects the external Timestamp Counter value. A write access has no impact. ***Note***: A wrap around is a change of the Timestamp Counter value from non-zero to zero not caused by write access to TSCV.

7.2.11 Timeout Counter Configuration (TOCC) - Offset 28h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	FFFF0000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RW/L	**Timeout Period (TOP):** Start value of the Timeout Counter (down-counter). Configures the Timeout Period.
15:3	0h RO	**Reserved**
2:1	0h RW/L	**Timeout Select (TOS):** When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1
0	0h RW/L	**Enable Timeout Counter (ETOC):** 0= Timeout Counter disabled 1= Timeout Counter enabled

7.2.12 Timeout Counter Value (TOCV) - Offset 2Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2Ch	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	FFFFh RW/1C	**Timeout Counter (TOC):** The Timeout Counter is decremented in multiples of CAN bit times [116] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS.

7.2.13 Error Counter Register (ECR) - Offset 40h

Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented. This enables monitoring of collisions between CAN frames and ASC frames.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RO/C	**CAN Error Logging (CEL):** The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO.
15	0h RO	**Receive Error Passive (RP):** 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128
14:8	00h RO	**Receive Error Counter (REC):** Actual state of the Receive Error Counter, values between 0 and 127
7:0	00h RO	**Transmit Error Counter (TEC):** Actual state of the Transmit Error Counter, values between 0 and 255

7.2.14 Protocol Status Register (PSR) - Offset 44h

Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in FLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.

Note: The Bus_Off recovery sequence cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error

code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000707h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RO	**Transmitter Delay Compensation Value (TDCV):** 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_ttcan_tx to m_ttcan_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point Valid values are 0 to 127 mtq
15	0h RO	**Reserved**
14	0h RO/C	**Protocol Exception Event (PXE):** 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred
13	0h RO/C	**Received a CAN FD Message (RFDF):** This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with EDL flag set has been received
12	0h RO/C	**BRS flag of last received CAN FD Message (RBRS):** This bit is set together with REDL, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set
11	0h RO/C	**ESI flag of last received CAN FD Message (RESI):** This bit is set together with REDL, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set
10:8	7h RO/V	**Fast Last Error Code (FLEC):** Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	0h RO	**Bus_Off Status (B0):** 0= The M_TTCAN is not Bus_Off 1= The M_TTCAN is in Bus_Off state
6	0h RO	**Warning Status (EW):** 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counters has reached the Error_Warning limit of 96

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Error Passive (EP):** 0= The M_TTCAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_TTCAN is in the Error_Passive state
4:3	0h RO	**ACT:** Monitors the modules CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter
2:0	7h RO/V	**Last Error Code (LEC):** The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0 when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value 1), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to 7. When the LEC shows the value 7, no CAN bus event was detected since the last CPU read access to the Protocol Status Register.

7.2.15 Transmitter Delay Compensation Register (TDCR) - Offset 48h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:8	00h RW	**Transmitter Delay Compensation Offset (TDCO):** 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq.
7	0h RO	**Reserved**
6:0	00h RW	**Transmitter Delay Compensation Filter Window Length (TDCF):** 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measure

7.2.16 Interrupt Register (IR) - Offset 50h

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. A flag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. Ahard reset will clear the register. The configuration of IE controls whether an interrupt is generated. The configuration of ILS controls on which interrupt line an interrupt is signaled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**Access to Reserved Address (ARA):** 0 = No access to reserved address occurred 1 = Access to reserved address occurred
28	0h RW/1C	**Protocol Error in Data Phase (Data Bit Time is used) (PED):** 0= No Protocol Error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7)
27	0h RW/1C	**Protocol Error in Arbitration Phase (Nominal Bit Time is used) (PEA):** 0= No Arbitration Error in data phase 1= Arbitration error in data phase detected (PSR.DLEC != 0,7)
26	0h RW/1C	**Watchdog Interrupt (WDI):** 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY
25	0h RW/1C	**Bus_Off Status (BO):** 0= Bus_Off status unchanged 1= Bus_Off status changed
24	0h RW/1C	**Warning Status (EW):** 0= Error_Warning status unchanged 1= Error_Warning status changed

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW/1C	**Error Passive (EP):** 0= Error_Warning status unchanged 1= Error_Warning status changed
22	0h RW/1C	**Error Logging Overflow (ELO):** 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred
21	0h RW/1C	**Bit Error Uncorrected (BEU):** Message RAM bit error detected, uncorrected. Controlled by input signal m_ttcan_aeim_berr[1] generated by an optional external parity / ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to 1. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected (e.g. parity logic)
20	0h RW/1C	**Bit Error Corrected (BEC):** Message RAM bit error detected and corrected. Controlled by input signal m_ttcan_aeim_berr[0] generated by an optional external parity / ECC logic attached to the Message RAM. 0= No bit error detected when reading from Message RAM 1= Bit error detected and corrected (e.g. ECC)
19	0h RW/1C	**Message Stored to Dedicated RX Buffer (DRX):** The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer
18	0h RW/1C	**Timeout Occurred (TOO):** 0= No timeout 1= Timeout reached
17	0h RW/1C	**Message RAM Access Failure (MRAF):** The flag is set, when the Rx Handler * has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. * was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred
16	0h RW/1C	**Timestamp Wraparound (TSW):** 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around
15	0h RW/1C	**TX Event FIFO Element Lost (TEFL):** 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	0h RW/1C	**TX Event FIFO Full (TEFF):** 0= Tx Event FIFO not full 1= Tx Event FIFO full

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**TX Event FIFO Watermark Reached (TEFW):** 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark
12	0h RW/1C	**TX Event FIFO New Entry (TEFN):** 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element
11	0h RW/1C	**TX FIFO Empty (TFE):** 0= Tx FIFO non-empty 1= Tx FIFO empty
10	0h RW/1C	**Transmission Cancellation Finished (TCF):** 0= No transmission cancellation finished 1= Transmission cancellation finished
9	0h RW/1C	**Transmission Completed (TC):** 0= No transmission completed 1= Transmission completed
8	0h RW/1C	**High Priority Message (HPM):** 0= No high priority message received 1= High priority message received
7	0h RW/1C	**RX FIFO 1 Message Lost (RF1L):** 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	0h RW/1C	**RX FIFO 1 Full (RF1F):** 0= Rx FIFO 1 not full 1= Rx FIFO 1 full
5	0h RW/1C	**RX FIFO 1 Watermark Reached (RF1W):** 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark
4	0h RW/1C	**RX FIFO 1 New Message (RF1N):** 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1
3	0h RW/1C	**RX FIFO 0 Message Lost (RF0L):** 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	0h RW/1C	**RX FIFO 0 Full (RF0F):** 0= Rx FIFO 0 not full 1= Rx FIFO 0 full
1	0h RW/1C	**RX FIFO 0 Watermark Reached (RF0W):** 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark
0	0h RW/1C	**RX FIFO 0 New Message (RF0N):** 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0

7.2.17 Interrupt Enable (IE) - Offset 54h

The settings in the Interrupt Enable register determine which status changes in the Interrupt Register will be signaled on an interrupt line.

0= Interrupt disabled

1= Interrupt enabled

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Access to Reserved Address Enable (ARAE):** 0 = No access to reserved address Disabled 1 = Access to reserved address Enabled
28	0h RW	**Protocol Error in Data Phase Enable (PEDE):** 0= Protocol Error in data phase Disabled 1= Protocol error in data phase Enabled
27	0h RW	**Protocol Error in Arbitration Phase Enable (PEAE):** 0= Arbitration Error in data phase Disabled 1= Arbitration error in data phase Enabled
26	0h RW	**Watchdog Interrupt Enable (WDIE):**
25	0h RW	**Bus_Off Status Interrupt Enable (BOE):**
24	0h RW	**Warning Status Interrupt Enable (EWE):**
23	0h RW	**Error Passive Interrupt Enable (EPE):**
22	0h RW	**Error Logging Overflow Interrupt Enable (ELOE):**
21	0h RW	**Bit Error Uncorrected Interrupt Enable (BEUE):**
20	0h RW	**Bit Error Corrected Interrupt Enable (BECE):**
19	0h RW	**Message Stored to Dedicated RX Buffer Interrupt Enable (DRXE):**
18	0h RW	**Timeout Occurred Interrupt Enable (TOOE):**
17	0h RW	**Message RAM Access Failure Interrupt Enable (MRAFE):**
16	0h RW	**Timestamp Wraparound Interrupt Enable (TSWE):**
15	0h RW	**TX Event FIFO Element Lost Interrupt Enable (TEFLE):**
14	0h RW	**TX Event FIFO Full Interrupt Enable (TEFFE):**
13	0h RW	**TX Event FIFO Watermark Reached Interrupt Enable (TEFWE):**
12	0h RW	**TX Event FIFO New Entry Interrupt Enable (TEFNE):**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**TX FIFO Empty Interrupt Enable (TFEE):**
10	0h RW	**Transmission Cancellation Finished Interrupt Enable (TCFE):**
9	0h RW	**Transmission Completed Interrupt Enable (TCE):**
8	0h RW	**High Priority Message Interrupt Enable (HPME):**
7	0h RW	**RX FIFO 1 Message Lost Interrupt Enable (RF1LE):**
6	0h RW	**RX FIFO 1 Full Interrupt Enable (RF1FE):**
5	0h RW	**RX FIFO 1 Watermark Reached Interrupt Enable (RF1WE):**
4	0h RW	**RX FIFO 1 New Message Interrupt Enable (RF1NE):**
3	0h RW	**RX FIFO 0 Message Lost Interrupt Enable (RF0LE):**
2	0h RW	**RX FIFO 0 Full Interrupt Enable (RF0FE):**
1	0h RW	**RX FIFO 0 Watermark Reached Interrupt Enable (RF0WE):**
0	0h RW	**RX FIFO 0 New Message Interrupt Enable (RF0NE):**

7.2.18 Interrupt Line Select (ILS) - Offset 58h

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

0= Interrupt assigned to interrupt line m_ttcan_int0

1= Interrupt assigned to interrupt line m_ttcan_int1

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Access to Reserved Address Interrupt Line (ARAL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
28	0h RW	**Protocol Error in Data Phase Interrupt Line (PEDL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
27	0h RW	**Protocol Error in Arbitration Phase Interrupt Line (PEAL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
26	0h RW	**Watchdog Interrupt Line (WDIL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
25	0h RW	**Bus_Off Status Interrupt Line (BOL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
24	0h RW	**Warning Status Interrupt Line (EWL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
23	0h RW	**Error Passive Interrupt Line (EPL):**
22	0h RW	**Error Logging Overflow Interrupt Line (ELOL):**
21	0h RW	**Bit Error Uncorrected Interrupt Line (BEUL):**
20	0h RW	**Bit Error Corrected Interrupt Line (BECL):**
19	0h RW	**Message Stored to Dedicated RX Buffer Interrupt Line (DRXL):**
18	0h RW	**Timeout Occurred Interrupt Line (TOOL):**
17	0h RW	**Message RAM Access Failure Interrupt Line (MRAFL):**
16	0h RW	**Timestamp Wraparound Interrupt Line (TSWL):**
15	0h RW	**TX Event FIFO Element Lost Interrupt Line (TEFLL):**
14	0h RW	**TX Event FIFO Full Interrupt Line (TEFFL):**
13	0h RW	**TX Event FIFO Watermark Reached Interrupt Line (TEFWL):**
12	0h RW	**TX Event FIFO New Entry Interrupt Line (TEFNL):**
11	0h RW	**TX FIFO Empty Interrupt Line (TFEL):**

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Transmission Cancellation Finished Interrupt Line (TCFL):**
9	0h RW	**Transmission Completed Interrupt Line (TCL):**
8	0h RW	**High Priority Message Interrupt Line (HPML):**
7	0h RW	**RX FIFO 1 Message Lost Interrupt Line (RF1LL):**
6	0h RW	**RX FIFO 1 Full Interrupt Line (RF1FL):**
5	0h RW	**RX FIFO 1 Watermark Reached Interrupt Line (RF1WL):**
4	0h RW	**RX FIFO 1 New Message Interrupt Line (RF1NL):**
3	0h RW	**RX FIFO 0 Message Lost Interrupt Line (RF0LL):**
2	0h RW	**RX FIFO 0 Full Interrupt Line (RF0FL):**
1	0h RW	**RX FIFO 0 Watermark Reached Interrupt Line (RF0WL):**
0	0h RW	**RX FIFO 0 New Message Interrupt Line (RF0NL):**

7.2.19 Interrupt Line Enable (ILE) - Offset 5Ch

Each of the two interrupt lines to the CPU can be enabled / disabled separately by programming bits EINT0 and EINT1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Enable Interrupt Line 1 (EINT1):** 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled
0	0h RW	**Enable Interrupt Line 0 (EINT0):** 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled

7.2.20 Global Filter Configuration (GFC) - Offset 80h

Global settings for Message ID filtering. The Global Filter Configuration controls the filter path for standard and extended messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW/L	**Accept Non-matching Frames Standard (ANFS):** Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject
3:2	0h RW/L	**Accept Non-matching Frames Extended (ANFE):** Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject
1	0h RW/L	**Reject Remote Frames Standard (RRFS):** 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs
0	0h RW/L	**Reject Remote Frames Extended (RRFE):** 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs

7.2.21 Standard ID Filter Configuration (SIDFC) - Offset 84h

Settings for 11-bit standard Message ID filtering. The Standard ID Filter Configuration controls the

filter path for standard messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW/L	**List Size Standard (LSS):** 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements >128= Values greater than 128 are interpreted as 128
15:2	0000h RW/L	**Filter List Standard Start Address (FLSSA):** Start address of standard Message ID filter list (32-bit word address)
1:0	0h RO	**Reserved**

7.2.22 Extended ID Filter Configuration (XIDFC) - Offset 88h

Settings for 29-bit extended Message ID filtering. The Extended ID Filter Configuration controls the filter path for standard messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW/L	**List Size Extended (LSE):** 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements >64= Values greater than 64 are interpreted as 64
15:2	0000h RW/L	**Filter List Extended Start Address (FLESA):** Start address of extended Message ID filter list (32-bit word address).
1:0	0h RO	**Reserved**

7.2.23 Extended ID AND Mask (XIDAM) - Offset 90h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	1FFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	1FFFFFFFh RW/L	**Extended ID Mask (EIDM):** For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

7.2.24 High Priority Message Status (HPMS) - Offset 94h

This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**Filter List (FLST):** Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List
14:8	00h RO	**Filter Index (FIDX):** Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7:6	0h RO	**Message Storage Indicator (MSI):** 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1
5:0	00h RO	**Buffer Index (BIDX):** Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = 1.

7.2.25 New Data 1 (NDAT1) - Offset 98h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**New Data (ND):** The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message

7.2.26 New Data 2 (NDAT2) - Offset 9Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**New Data (ND):** The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message

7.2.27 RX FIFO 0 Configuration (RXF0C) - Offset A0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**FIFO 0 Operation Mode (F0OM):** FIFO 0 can be operated in blocking or in overwrite mode. 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode
30:24	00h RW/L	**RX FIFO 0 Watermark (F0WM):** 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) >64= Watermark interrupt disabled
23	0h RO	**Reserved**
22:16	00h RW/L	**RX FIFO 0 Size (F0S):** 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements >64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1
15:2	0000h RW/L	**RX FIFO 0 Start Address (F0SA):** Start address of Rx FIFO 0 in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

7.2.28 RX FIFO 0 Status (RXF0S) - Offset A4h

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**RX FIFO 0 Message Lost (RF0L):** This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero ***Note***: Overwriting the oldest message when RXF0C.F0OM = 1 will not set this flag.
24	0h RO	**RX FIFO 0 Full (F0F):** 0= Rx FIFO 0 not full 1= Rx FIFO 0 full
23:22	0h RO	**Reserved**
21:16	00h RO	**RX FIFO 0 Put Index (F0PI):** Rx FIFO 0 write index pointer, range 0 to 63.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:8	00h RO	**RX FIFO 0 Get Index (F0GI):** Rx FIFO 0 read index pointer, range 0 to 63.
7	0h RO	**Reserved**
6:0	00h RO	**RX FIFO 0 Fill Level (F0FL):** Number of elements stored in Rx FIFO 0, range 0 to 64.

7.2.29 RX FIFO 0 Acknowledge (RXF0A) - Offset A8h

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RX FIFO 0 Acknowledge Index (F0AI):** After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

7.2.30 RX Buffer Configuration (RXBC) - Offset ACh

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:2	0000h RW/L	**RX Buffer Start Address (RBSA):** Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C.
1:0	0h RO	**Reserved**

7.2.31 RX FIFO 1 Configuration (RXF1C) - Offset B0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**FIFO 1 Operation Mode (F1OM):** FIFO 1 can be operated in blocking or in overwrite mode. 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode
30:24	00h RW/L	**RX FIFO 1 Watermark (F1WM):** 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) >64= Watermark interrupt disabled
23	0h RO	**Reserved**
22:16	00h RW/L	**RX FIFO 1 Size (F1S):** 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements >64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S-1
15:2	0000h RW/L	**RX FIFO 1 Start Address (F1SA):** Start address of Rx FIFO 1 in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

7.2.32 RX FIFO 1 Status (RXF1S) - Offset B4h

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**RX FIFO 1 Message Lost (RF1L):** This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero ***Note***: Overwriting the oldest message when RXF1C.F1OM = 1 will not set this flag.
24	0h RO	**RX FIFO 1 Full (F1F):** 0= Rx FIFO 1 not full 1= Rx FIFO 1 full
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RO	**RX FIFO 1 Put Index (F1PI):** Rx FIFO 1 writes index pointer, range 0 to 63.
15:14	0h RO	**Reserved**
13:8	00h RO	**RX FIFO 1 Get Index (F1GI):** Rx FIFO 1 read index pointer, range 0 to 63.
7	0h RO	**Reserved**
6:0	00h RO	**RX FIFO 1 Fill Level (F1FL):** Number of elements stored in Rx FIFO 1, range 0 to 64.

7.2.33 RX FIFO 1 Acknowledge (RXF1A) - Offset B8h

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RX FIFO 1 Acknowledge Index (F1AI):** After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

7.2.34 Rx Buffer / FIFO Element Size Configuration (RXESC) - Offset BCh

Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frames data field is

ignored.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10:8	0h RW/L	**RX Buffer Data Field Size (RBDS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field
7	0h RO	**Reserved**
6:4	0h RW/L	**RX FIFO 1 Data Field Size (F1DS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field
3	0h RO	**Reserved**
2:0	0h RW/L	**RX FIFO 0 Data Field Size (F0DS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field

7.2.35 TX Buffer Configuration (TXBC) - Offset C0h

Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW/L	**TX FIFO/Queue Mode (TFQM):** 0= Tx FIFO operation 1= Tx Queue operation
29:24	00h RW/L	**Transmit FIFO/Queue Size (TFQS):** 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue >32= Values greater than 32 are interpreted as 32
23:22	0h RO	**Reserved**
21:16	00h RW/L	**Number of Dedicated Transmit Buffers (NDTB):** 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers >32= Values greater than 32 are interpreted as 32
15:2	0000h RW/L	**TX Buffers Start Address (TBSA):** Start address of Tx Buffers section in Message RAM.
1:0	0h RO	**Reserved**

7.2.36 TX FIFO/Queue Status (TXFQS) - Offset C4h

The Tx FIFO/Queue status is related to the pending Tx requests listed in register TXBRP. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (TXBRP not yet updated).

Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers.

Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**TX FIFO/Queue Full (TFQF):** 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full
20:16	00h RO	**TX FIFO/Queue Put Index (TFQPI):** Tx FIFO/Queue write index pointer, range 0 to 31.
15:13	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
12:8	00h RO	**TX FIFO Get Index (TFGI):** Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1).
7:6	0h RO	**Reserved**
5:0	00h RO	**TX FIFO Free Level (TFFL):** Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1)

7.2.37 TX Buffer Element Size Configuration (TXESC) - Offset C8h

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are

intended for CAN FD operation only.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**TX Buffer Data Field Size (TBDS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field ***Note***: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as 0xCC (padding bytes).

7.2.38 TX Buffer Request Pending (TXBRP) - Offset CCh

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmission Request Pending (TRP):** Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been canceled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission. In DAR mode all transmissions are automatically canceled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending ***Note***: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is canceled immediately, the corresponding TXBRP bit is reset.

7.2.39 TX Buffer Add Request (TXBAR) - Offset D0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Add Request (AR):** Each Tx Buffer has its own Add Request bit. Writing a 1 will set the corresponding Add Request bit; writing a 0 has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added ***Note***: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored.

7.2.40 TX Buffer Cancellation Request (TXBCR) - Offset D4h

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cancellation Request (CR):** Each Tx Buffer has its own Cancellation Request bit. Writing a 1 will set the corresponding Cancellation Request bit; writing a 0 has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending

7.2.41 TX Buffer Transmission Occurred (TXBTO) - Offset D8h

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmission Occurred (TO):** Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred

7.2.42 TX Buffer Cancellation Finished (TXBCF) - Offset DCh

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Cancellation Finished (CF):** Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished

7.2.43 TX Buffer Transmission Interrupt Enable (TXBTIE) - Offset E0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Transmission Interrupt Enable (TIE):** Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable

7.2.44 Tx Buffer Cancellation Finished Interrupt Enable (TXBCIE) - Offset E4h

Type	Size	Offset	Default
MMIO	32 bit	BAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cancellation Finished Interrupt Enable (CFIE):** Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled

7.2.45 TX Event FIFO Configuration (TXEFC) - Offset F0h

Type	Size	Offset	Default
MMIO	32 bit	BAR + F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	00h RW/L	**Event FIFO Watermark (EFWM):** 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) >32= Watermark interrupt disabled
23:22	0h RO	**Reserved**
21:16	00h RW/L	**Event FIFO Size (EFS):** 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements >32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1
15:2	0000h RW/L	**Event FIFO Start Address (EFSA):** Start address of Tx Event FIFO in Message RAM.
1:0	0h RO	**Reserved**

7.2.46 TX Event FIFO Status (TXEFS) - Offset F4h

Type	Size	Offset	Default
MMIO	32 bit	BAR + F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TX Event FIFO Lost (TEFL):** This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	0h RO	**Event FIFO Full (EFF):** 0= Tx Event FIFO not full 1= Tx Event FIFO full
23:21	0h RO	**Reserved**
20:16	00h RO	**Event FIFO Put Index (EFPI):** Tx Event FIFO writes index pointer, range 0 to 31.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:8	00h RO	**Event FIFO Get Index (EFGI):** Tx Event FIFO read index pointer, range 0 to 31.
7:6	0h RO	**Reserved**
5:0	00h RO	**Event FIFO Fill Level (EFFL):** Number of elements stored in Tx Event FIFO, range 0 to 32.

7.2.47 TX Event FIFO Acknowledge (TXEFA) - Offset F8h

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Event FIFO Acknowledge Index (EFAI):** After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the FIFO 0 Fill Level TXEFS.EFFL.

7.2.48 TT Trigger Memory Configuration (TTTMC) - Offset 100h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW/P	**Trigger Memory Elements (TME):** b0: No Trigger Memory b1-b1000000: Number of Trigger Memory elements >b1000000: Values greater than 64 are interpreted as 64
15:2	0000h RW/P	**Trigger Memory Start Address (TMSA):** Start address of Trigger Memory in Message RAM.
1:0	0h RO	**Reserved**

7.2.49 TT Reference Message Configuration (TTRMC) - Offset 104h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Reference Message Payload Select (RMPS):** Ignored in case of time slaves. b0: Reference message has no additional payload b1: The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB (Level 1: bytes 2-8, Level 0,2: bytes 5-8)
30	0h RW/P	**Extended Identifier (XTD):** b0: 11-bit standard Identifier b1: 29-bit extended Identifier
29	0h RO	**Reserved**
28:0	00000000h RW/P	**Reference Identifier (RID):** Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference Identifier depending on Bit XTD. A standard Identifier has to be written to ID[28:18].

7.2.50 TT Operation Configuration (TTOCF) - Offset 108h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 108h	00010000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Event Trigger Polarity (EVTP):** b0: Rising edge trigger b1: Falling edge trigger
25	0h RW/P	**Enable Clock Calibration (ECC):** b0: Automatic clock calibration in TTCAN Level 0,2 is disabled b1: Automatic clock calibration in TTCAN Level 0,2 is enabled
24	0h RW/P	**Enable Global Time Filtering (EGTF):** b0: Global time filtering in TTCAN Level 0,2 is disabled b1: Global time filtering in TTCAN Level 0,2 is enabled
23:16	01h RW/P	**Application Watchdog Limit (AWL):** The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF: Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once every 256 NTUs.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/P	**Enable External Clock Synchronization (EECS):** If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. b0: External clock synchronization in TTCAN Level 0,2 disabled b1: External clock synchronization in TTCAN Level 0,2 enabled
14:8	00h RW/P	**Initial Reference Trigger Offset (IRTO):** 0x00-7F: Positive offset, range from 0 to 127
7:5	0h RW/P	**LD of Synchronization Deviation Limit (LDSDL):** The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2^(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7: LD of Synchronization Deviation Limit (SDL less than or equal to 324096)
4	0h RW/P	**Time Master (TM):** b0: Time Master function disabled b1: Potential Time Master
3	0h RW/P	**Gap Enable (GEN):** b0: Strictly time-triggered operation b1: External event-synchronized time-triggered operation
2	0h RO	**Reserved**
1:0	0h RW/P	**Operation Mode (OM):** b0: Event-driven CAN communication, default b1: TTCAN level 1 b10: TTCAN level 2 b11: TTCAN level 0

7.2.51 TT Matrix Limits (TTMLM) - Offset 10Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RW/P	**Expected Number of Tx Triggers (ENTT):** 0x000-FFF: Expected number of Tx Triggers in one Matrix Cycle
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW/P	**Tx Enable Window (TXEW):** Length of Tx enable window, 1-16 NTU cycles
7:6	0h RW/P	**Cycle Start Synchronization (CSS):** b0: No sync pulse b1: Sync pulse at start of basic cycle b10: Sync pulse at start of matrix cycle b11: Reserved
5:0	00h RW/P	**Cycle Count Max (CCM):** 0x00: 1 Basic Cycle per Matrix Cycle 0x01: 2 Basic Cycles per Matrix Cycle 0x03: 4 Basic Cycles per Matrix Cycle 0x07: 8 Basic Cycles per Matrix Cycle 0x0F: 16 Basic Cycles per Matrix Cycle 0x1F: 32 Basic Cycles per Matrix Cycle 0x3F: 64 Basic Cycles per Matrix Cycle Others: Reserved

7.2.52 TUR Configuration (TURCF) - Offset 110h

The length of the NTU is given by: NTU = CAN Clock Period X NC/DC NC is an 18-bit value. It's high part, NCH[17:16] is hard wired to 0b01. Therefore the range of NC is 0x10000...0x1FFFF. The value configured by NCL is the initial value for TURNA.NAV[15:0]. DC is set to 0x1000 by hardware reset and it may not be written to 0x0000. Level 1: NC >= 4 X DC and NTU = CAN bit time Level 0,2: NC >= 8 X DC The actual value of TUR may be changed by the clock drift compensation function of TTCAN Level 0 and Level 2 in order to adjust the nodes local view of the NTU to the time masters view of the NTU. DC will not be changed by the automatic drift compensation, TURNA.NAV may be adjusted around NC in the range of the Synchronization Deviation Limit given by TTOCF.LDSDL. NC and DC should be programmed to the largest suitable values in order to allow the best computational accuracy for the drift compensation process.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	10000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Enable Local Time (ELT):** b0: Local time is stopped, default b1: Local time is enabled ***Note*: Local time is started by setting ELT. It remains active until ELT is reset or until the next hardware reset. TURCF.DC is locked when TURCF.ELT = b1. If ELT is written to b0, the readable value will stay at b1 until the new value has been synchronized into the CAN clock domain. During this time write access to the other bits of the register remains locked.**

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO	**Reserved**
29:16	1000h RW/P	**Denominator configuration (DC):** 0x0000: Illegal value 0x0001-3FFF: Denominator configuration
15:0	0000h RW/P	**Numerator configuration Low (NCL):** Write access to the TUR Numerator configuration Low is only possible during configuration with TURCF.ELT = b0 or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT configuration Mode, the new value takes effect when TTOST.WECS is cleared to b0. NCL is locked TTOST.WECS is b1. 0x0000-FFFF: Numerator configuration Low **Note: If NC < 7 X DC in TTCAN Level 1, then it is required that subsequent time marks in the Trigger Memory must differ by at least 2 NTU.** 49

7.2.53 TT Operation Control (TTOCN) - Offset 114h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**TT Operation Control Register Locked (LCKC):** Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. b0: Write access to TTOCN enabled b1: Write access to TTOCN locked
14	0h RO	**Reserved**
13	0h RW	**External Synchronization Control (ESCN):** If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt. b0: External synchronization disabled b1: External synchronization enabled
12	0h RW	**Next is Gap (NIG):** This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = b1) b0: No action, reset by reception of any reference message b1: Transmit next reference message with Next_is_Gap = b1
11	0h RW	**Time Mark Gap (TMG):** b0: Reset by each reference message b1: Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated
10	0h RW	**Finish Gap (FGP):** Set by the CPU, reset by each reference message b0: No reference message requested b1: Application requested start of reference message

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Gap Control Select (GCS):** b0: Gap control independent from m_ttcan_evt b1: Gap control by input pin m_ttcan_evt
8	0h RW	**Trigger Time Mark Interrupt Pulse Enable (TTIE):** External time mark events are configured by trigger memory element TMEX. A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. b0: Trigger Time Mark Interrupt output m_ttcan_tmp disabled b1: Trigger Time Mark Interrupt output m_ttcan_tmp enabled
7:6	0h RW	**Register Time Mark Compare (TMC):** b00: No Register Time Mark Interrupt generated b01: Register Time Mark Interrupt if Time Mark = cycle time b10: Register Time Mark Interrupt if Time Mark = local time b11: Register Time Mark Interrupt if Time Mark = global time **Note:** When changing the time mark reference (cycle, local, global time), it is recommended to first write TMC = b0, then reconfigure TTTMK, and finally set TMC to the intended time reference**.**
5	0h RW	**Register Time Mark Interrupt Pulse Enable (RTIE):** Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one m_ttcan_clk period is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. b0: Register Time Mark Interrupt output m_ttcan_rtp disabled b1: Register Time Mark Interrupt output m_ttcan_rtp enabled
4:3	0h RW	**Stop Watch Source (SWS):** b00: Stop Watch disabled b01: Actual value of cycle time is copied to TTCPT.SWV b10: Actual value of local time is copied to TTCPT.SWV b11: Actual value of global time is copied to TTCPT.SWV
2	0h RW	**Stop Watch Polarity (SWP):** b0: Rising edge trigger b1: Falling edge trigger
1	0h RW	**External Clock Synchronization (ECS):** Writing a b1 to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle.
0	0h RW	**Set Global time (SGT):** Writing a b1 to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. 51

7.2.54 TT Global Time Preset (TTGTP) - Offset 118h

If TTOST.WGDT is set, the next reference message will be transmitted with the Master_Ref_Mark modified by the preset value and with Disc_Bit = b1, presetting the global time in all nodes simultaneously. TP is reset to 0x0000 each time a reference message with Disc_Bit = b1 becomes valid or if the node is not the current Time Master. TP is locked while TTOST.WGTD = b1 after setting TTOCN.SGT until the reference message with Disc_Bit = b1 becomes valid or until the node is no longer the current Time Master.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Cycle Time Target Phase (CTP):** CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set. 0x0000-FFFF: Defines target value of cycle time when a rising edge of m_ttcan_evt is expected
15:0	0000h RW	**Time Preset (TP):** TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF: Next Master Reference Mark = Master Reference Mark + TP 0x8000: reserved 0x8001-FFFF: Next Master Reference Mark = Master Reference Mark - (0x10000 - TP)

7.2.55 TT Time Mark (TTTMK) - Offset 11Ch

A time mark interrupt (TTIR.RTMI = b1) is generated when the time base indicated by TTOCN.TMC (cycle time, local time, or global time) has the same value as TM.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**TT Time Mark Register Locked (LCKM):** Always set by a write access to register TTOCN. Set by write access to register TTTMK when TTOCN.TMC 00. Reset when the registers have been synchronized into the CAN clock domain. b0: Write access to TTTMK enabled b1: Write access to TTTMK locked
30:23	0h RO	**Reserved**
22:16	00h RW	**Time Mark Cycle Code (TICC):** Cycle count for which the time mark is valid. 0b000000x: valid for all cycles 0b000001c: valid every second cycle at cycle count mod2 = c 0b00001cc: valid every fourth cycle at cycle count mod4 = cc 0b0001ccc: valid every eighth cycle at cycle count mod8 = ccc 0b001cccc: valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc: valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc: valid every sixty-fourth cycle at cycle count mod64 = cccccc
15:0	0000h RW	**Time Mark (TM):** 0x0000-FFFF: Time Mark ***Note*: When using byte access to register TTTMK it is recommended to first disable the time mark compare function (TTOCN.TMC = b0) to avoid compares on inconsistent register values.**

7.2.56 TT Interrupt Register (TTIR) - Offset 120h

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. A flag is cleared by writing a b1 to the corresponding bit position. Writing a b0 has no effect. A hard reset will clear the register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/1C	**Configuration Error (CER):** Trigger out of order. b0: No error found in trigger list b1: Error found in trigger list
17	0h RW/1C	**Application Watchdog (AW):** b0: Application watchdog served in time b1: Application watchdog not served in time
16	0h RW/1C	**Watch Trigger (WT):** b0: No missing reference message b1: Missing reference message (Level 0: cycle time 0xFF00)
15	0h RW/1C	**Initialization Watch Trigger (IWT):** The initialization is restarted by resetting IWT. b0: No missing reference message during system startup b1: No system startup due to missing reference message
14	0h RW/1C	**Error Level Changed (ELC):** Not set when error level changed during initialization. b0: No change in error level b1: Error level changed
13	0h RW/1C	**Scheduling Error 2 (SE2):** b0: No scheduling error 2 b1: Scheduling error 2 occurred
12	0h RW/1C	**Scheduling Error 1 (SE1):** b0: No scheduling error 1 b1: Scheduling error 1 occurred
11	0h RW/1C	**Tx Count Overflow (TXO):** b0: Number of Tx Trigger as expected b1: More Tx trigger than expected in one matrix cycle
10	0h RW/1C	**Tx Count Underflow (TXU):** b0: Number of Tx Trigger as expected b1: Less Tx trigger than expected in one matrix cycle
9	0h RW/1C	**Global Time Error (GTE):** Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. b0: Synchronization deviation within limit b1: Synchronization deviation exceeded limit
8	0h RW/1C	**Global Time Discontinuity (GTD):** b1: No discontinuity of global time b0: Discontinuity of global time
7	0h RW/1C	**Global Time Wrap (GTW):** b0: No global time wrap occurred b1: Global time wrap from 0xFFFF to 0x0000 occurred
6	0h RW/1C	**Stop Watch Event (SWE):** b0: No rising/falling edge at stop watch trigger pin m_ttcan_swt detected b1: Rising/falling edge at stop watch trigger pin m_ttcan_swt detected
5	0h RW/1C	**Trigger Time Mark Event Internal (TTMI):** Internal time mark events are configured by trigger memory element TMIN. Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. b0: Time mark not reached b1: Time mark reached (Level 0: cycle time TTOCF.IRTO X 0x200)
4	0h RW/1C	**Register Time Mark Interrupt (RTMI):** Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. b0: Time mark not reached b1: Time mark reached

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**Start of Gap (SOG):** b0: No reference message seen with Next_is_Gap bit set b1: Reference message with Next_is_Gap bit set becomes valid
2	0h RW/1C	**Change of Synchronization Mode (CSM):** b0: No change in master to slave relation or schedule synchronization b1: Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset
1	0h RW/1C	**Start of Matrix Cycle (SMC):** b0: No Matrix Cycle started since bit has been reset b1: Matrix Cycle started
0	0h RW/1C	**Start of Basic Cycle (SBC):** b0: No Basic Cycle started since bit has been reset b1: Basic Cycle started

7.2.57 TT Interrupt Enable (TTIE) - Offset 124h

The settings in the TT Interrupt Enable register determine which status changes in the TT Interrupt Register will result in an interrupt.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**Configuration Error Interrupt Enable (CERE):** b0: interrupt disabled b1: interrupt enabled
17	0h RW	**Application Watchdog Interrupt Enable (AWE):** b0: interrupt disabled b1: interrupt enabled
16	0h RW	**Watch Trigger Interrupt Enable (WTE):** b0: interrupt disabled b1: interrupt enabled
15	0h RW	**Initialization Watch Trigger Interrupt Enable (IWTE):** b0: interrupt disabled b1: interrupt enabled
14	0h RW	**Change Error Level Interrupt Enable (ELCE):** b0: interrupt disabled b1: interrupt enabled
13	0h RW	**Scheduling Error 2 Interrupt Enable (SE2E):** b0: interrupt disabled b1: interrupt enabled
12	0h RW	**Scheduling Error 1 Interrupt Enable (SE1E):** b0: interrupt disabled b1: interrupt enabled
11	0h RW	**Tx Count Overflow Interrupt Enable (TXOE):** b0: interrupt disabled b1: interrupt enabled
10	0h RW	**Tx Count Underflow Interrupt Enable (TXUE):** b0: interrupt disabled b1: interrupt enabled
9	0h RW	**Global Time Error Interrupt Enable (GTEE):** b0: interrupt disabled b1: interrupt enabled
8	0h RW	**Global Time Discontinuity Interrupt Enable (GTDE):** b0: interrupt disabled b1: interrupt enabled

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Global Time Wrap Interrupt Enable (GTWE):** b0: interrupt disabled b1: interrupt enabled
6	0h RW	**Stop Watch Event Interrupt Enable (SWEE):** b0: interrupt disabled b1: interrupt enabled
5	0h RW	**Trigger Time Mark Event Internal Enable (TTMIE):** b0: interrupt disabled b1: interrupt enabled
4	0h RW	**Register Time Mark Interrupt Enable (RTMIE):** b0: interrupt disabled b1: interrupt enabled
3	0h RW	**Start of Gap Interrupt Enable (SOGE):** b0: interrupt disabled b1: interrupt enabled
2	0h RW	**Change of Synchronization Mode Interrupt Enable (CSME):** b0: interrupt disabled b1: interrupt enabled
1	0h RW	**Start of Matrix Cycle Interrupt Enable (SMCE):** b0: interrupt disabled b1: interrupt enabled
0	0h RW	**Start of Basic Cycle Interrupt Enable (SBCE):** b0: interrupt disabled b1: interrupt enabled

7.2.58 TT Interrupt Line Select (TTILS) - Offset 128h

The TT Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the TT Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1. b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**Configuration Error Interrupt Line (CERL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int1
17	0h RW	**Application Watchdog Interrupt Line (AWL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int2
16	0h RW	**Watch Trigger Interrupt Line (WTL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int3
15	0h RW	**Initialization Watch Trigger Interrupt Line (IWTL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int4
14	0h RW	**Change Error Level Interrupt Line (ELCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int5

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Scheduling Error 2 Interrupt Line (SE2L):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int6
12	0h RW	**Scheduling Error 1 Interrupt Line (SE1L):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int7
11	0h RW	**Tx Count Overflow Interrupt Line (TXOL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int8
10	0h RW	**Tx Count Underflow Interrupt Line (TXUL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int9
9	0h RW	**Global Time Error Interrupt Line (GTEL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int10
8	0h RW	**Global Time Discontinuity Interrupt Line (GTDL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int11
7	0h RW	**Global Time Wrap Interrupt Line (GTWL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int12
6	0h RW	**Stop Watch Event Interrupt Line (SWEL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int13
5	0h RW	**Trigger Time Mark Event Internal Line (TTMIL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int14
4	0h RW	**Register Time Mark Interrupt Line (RTMIL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int15
3	0h RW	**Start of Gap Interrupt Line (SOGL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int16
2	0h RW	**Change of Synchronization Mode Interrupt Line (CSML):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int17
1	0h RW	**Start of Matrix Cycle Interrupt Line (SMCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int18
0	0h RW	**Start of Basic Cycle Interrupt Line (SBCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int19

7.2.59 TT Operation Status (TTOST) - Offset 12Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12Ch	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Schedule Phase Lock (SPL):** The Bit is valid only when external synchronization is enabled (TTOCN.ESCN = b1). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU. b0: Phase outside range b1: Phase inside range
30	0h RO	**Wait for External Clock Synchronization (WECS):** b0: No external clock synchronization pending b1: Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle.
29	0h RO	**Application Watchdog Event (AWE):** The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. b0: Application Watchdog served in time b1: Failed to serve Application Watchdog in time
28	0h RO	**Wait for Event (WFE):** b0: No Gap announced, reset by a reference message with Next_is_Gap = b0 b1: Reference message with Next_is_Gap = b1 received
27	0h RO	**Gap Started Indicator (GSI):** b0: No Gap in schedule, reset by each reference message and for all time slaves b1: Gap time after Basic Cycle has started
26:24	0h RO	**Time Master Priority (TMP):** 0x0-7: Priority of actual Time Master
23	0h RO	**Gap Finished Indicator (GFI):** Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = b1, or via input pin m_ttcan_evt if TTOCN.GCS = b1. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. b0: Reset at the end of each reference message b1: Gap finished by M_TTCAN
22	0h RO	**Wait for Global Time Discontinuity (WGTD):** b0: No global time preset pending b1: Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = b1 or after it received a reference message.
21:16	0h RO	**Reserved**
15:8	00h RO	**Reference Trigger Offset (RTO):** The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = b11), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF: Actual Reference Trigger offset value
7	1h RO	**Quality of Clock Speed (QCS):** Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to b1. b0: Local clock speed not synchronized to Time Master clock speed b1: Synchronization Deviation <= SDL
6	0h RO	**Quality of Global Time Phase (QGTP):** Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to b0. b0: Global time not valid b1: Global time in phase with Time Master

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Synchronization State (SYS):** b00: Out of Synchronization b01: Synchronizing to TTCAN communication b10: Schedule suspended by Gap (In_Gap) b11: Synchronized to schedule (In_Schedule)
3:2	0h RO	**Master State (MS):** b00: Master_Off, no master properties relevant b01: Operating as Time Slave b10: Operating as Backup Time Master b11: Operating as current Time Master
1:0	0h RO	**Error Level (EL):** b00: Severity 0 - No Error b01: Severity 1 - Warning b10: Severity 2 - Error b11: Severity 3 - Severe Error

7.2.60 TUR Numerator Actual (TURNA) - Offset 130h

There is no drift compensation in TTCAN Level 1 (NAV = NC). In TTCAN Level 0 and Level 2, the drift between the nodes local clock and the time masters local clock is calculated. The drift is compensated when the Synchronization Deviation (difference between NC and the calculated NAV) is not more than 2(TTOCF.LDSDL + 5). With TTOCF.LDSDL 7, this results in a maximum range for NAV of (NC - 0x1000) NAV (NC + 0x1000).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:0	00000h RO	**Numerator Actual Value (NAV):** <= 0x0EFFF: Illegal value 0x0F000-20FFF: Actual numerator value >= 0x21000: Illegal value

7.2.61 TT Local and Global Time (TTLGT) - Offset 134h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 134h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Global Time (GT):** Non-fractional part of the sum of the nodes local time and its local offset. 0x0000-FFFF: Global time value of TTCAN network
15:0	0000h RO	**Local Time (LT):** Non-fractional part of local time, incremented once each local NTU. 0x0000-FFFF: Local time value of TTCAN node

7.2.62 TT Cycle Time & Count (TTCTC) - Offset 138h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 138h	003F0000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:16	3Fh RO	**Cycle Count (CC):** 0x00-3F Number of actual Basic Cycle in the System Matrix
15:0	0000h RO	**Cycle Time (CT):** Non-fractional part of the difference of the node's local time and Ref_Mark. 0x0000-FFFF Cycle time value of TTCAN Basic Cycle

7.2.63 TT Capture Time (TTCPT) - Offset 13Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Stop Watch Value (SWV):** On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is not equal to b0 and TTIR.SWE is b0, the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to b1. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF: Captured Stop Watch value
15:6	0h RO	**Reserved**
5:0	00h RO	**Cycle Count Value (CCV):** Cycle count value captured together with SWV. 0x00-3F: Captured cycle count value

7.2.64 TT Cycle Sync Mark (TTCSM) - Offset 140h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RO	**Cycle Sync Mark (CSM):** The Cycle Sync Mark is measured in cycle time. It is updated when the reference message becomes valid and retains its value until the next reference message becomes valid. 0x0000-FFFF Captured cycle time

7.2.65 Message RAM Size (MSG_RAM_SIZE) - Offset 500h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 500h	00004600h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00004600h RO	**Size Bytes (SIZE_B):** Read only value of the size in bytes of the Message RAM of this dby_can instance @@jstokes3, need to set the default value where this RDL is instantiated

7.2.66 CTL - Offset 504h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 504h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**M_TTCAN Disable Error Data Modification on Read (CAN_DIS_MORD):** Set to 1 to prevent reads to ECR.CEL and PSR.LEC from resetting the CAN error data in the register.

7.2.67 Interrupt Control (INT_CTL) - Offset 508h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 508h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**PUNIT Interrupt Enable (PUNIT_INT_EN):** Enables the dby_can PUNIT interrupt output int_punit_o. Software is expected to set PUNIT_INT_EN or PRIMARY_INT_EN to b1, but not both.
0	0h RW	**Primary Interrupt Enable (PRIMARY_INT_EN):** Enables the primary interrupt output int_o. Software is expected to set PUNIT_INT_EN or PRIMARY_INT_EN to b1, but not both.

7.2.68 Interrupt Status (INT_STAT) - Offset 50Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Other CAN Parity Error Interrupt (OTHER_CAN_PERR_INT):** Parity error interrupt for the other CAN instance.
2	0h RO	**Other Controller Interrupt Status (OTHER_CAN_CONT_INT):** If asserted then the other instance of the M_TTCAN controller has its interrupt asserted.
1	0h RO	**This CAN Parity Error Interrupt (THIS_CAN_PERR_INT):** Parity error interrupt for this CAN instance.
0	0h RO	**This CAN Controller Interrupt Status (THIS_CAN_CONT_INT):** If asserted then this instance of the M_TTCAN controller has its interrupt asserted.

7.2.69 MSGRAM Address Conflict Status (MSGRAM_ADDR_CONFLICT_STAT) - Offset 510h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 510h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Address Conflict Occurred (ADDR_CONFLICT_OCCURED):** A flag to indicate that an address conflict has occurred. This can be used to help the debug of the CAN device driver. Note that this does not cause an interrupt.
15	0h RO	**Reserved**
14:0	0000h RO	**M_TTCAN Address Conflict Offset (CAN_ADDR_CONFLICT_OFFSET):** The M_TTCAN address that the conflict between an AHB access to the MSGRAM simultaneous to an M_TTCAN access to MSGRAM.

7.2.70 TTCAN TIMESTAMP CONTROL REGISTER (TIMESTAMP_CTL) - Offset 514h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 514h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Remote Cross Timestamp Valid (RXTSV):**
2	0h RO	**Local Cross Timestamp Valid (LXTSV):**
1	0h RW	**Capture Remote Cross Timestamp (RXTSC):**
0	0h RW	**Capture Local Cross Timestamp (LXTSC):**

7.2.71 TTCAN LOCAL TIMESTAMP HIGH (LOCALTIMESTAMP_HIGH) - Offset 518h

Type	Size	Offset	Default
MMIO	32 bit	BAR + 518h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Local Timestamp High (LTH):**

7.2.72 TTCAN LOCAL TIMESTAMP LOW (LOCALTIMESTAMP_LOW) - Offset 51Ch

Type	Size	Offset	Default
MMIO	32 bit	BAR + 51Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Local Timestamp Low (LTL):**

7.2.73 CAN Parity Error Control and Status (PAR_CTL_STAT) - Offset 600h

Control and Status of Parity Check Functionality

Type	Size	Offset	Default
MMIO	32 bit	BAR + 600h	00000003h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW/1C/P	**Parity Error Occurred (PERR_OCCURED):** Sticky register which asserts when a parity error has been detected on a read from the message RAM. A write of b1 clears this field to b0. If they are enabled, the int_o and int_punit_o interrupt outputs may assert when this field is set to 1. The interrupts will clear when this field is cleared. This register field can only be reset on a powergoodrst_n.
1	1h RO	**Parity Initialisation In Progress (PARITY_INIT_IN_PROG):** Immediately on coming out of a reset (hresetn asserted) the message RAM will be parity initialised with writes of b0. While this is taking place, this field will read as 1. While this PARITY_INIT_IN_PROG is 1, reads to the message RAM will be stalled until completion of parity initialisation.
0	1h RW	**Parity Enable (PARITY_EN):** 1 - Parity bit generation, checking, error reporting and error injection are enabled for dby_can. 0 - All parity functionality is disabled for dby_can. The value of this field can only be updated by software when PARITY_INIT_IN_PROG == 0.

7.2.74 Parity Error Offset (PAR_ERR_OFFSET) - Offset 604h

Stores the message RAM offset at which a parity error occurred in dby_can message RAM space

Type	Size	Offset	Default
MMIO	32 bit	BAR + 604h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/P	**Parity Error In Upper 16 bits (PAR_ERR_UPP):** Indicates a that a parity error was detected in the upper 16 bits of the word at this offset. This register field can only be reset on a powergoodrst_n.
16	0h RO/P	**Parity Error In Lower 16 bits (PAR_ERR_LOW):** Indicates a that a parity error was detected in the lower 16 bits of the word at this offset. This register field can only be reset on a powergoodrst_n.
15	0h RO	**Reserved**
14:0	0000h RO/P	**Parity Error Offset (PAR_ERR_OFFSET):** Captures the message RAM offset at which a parity error occurred. A new offset can only be captured when PERR_OCCURED is b0. This offset is relative to 0x0 in dby_can memory space. This register field can only be reset on a powergoodrst_n.

7.2.75 Parity Error Injection Control and Status (PAR_EINJ_CTL_STAT) - Offset 608h

Control and status for parity error injection to the dby_can message RAM.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 608h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO	**One Time Parity Error Injection Occurred (EINJ_ONE_TIME_ERR_OCCURED):** Asserts when a parity error is injected and EINJ_MODE = 0 (one time error injection). Cleared when EINJ_EN is set to b1 Once the one time parity error is injected, EINJ_EN deasserts. The intention then is that EINJ_ONE_TIME_ERR_OCCURED is the record that an error was injected.
1	0h RW	**Parity Error Injection Mode (EINJ_MODE):** b1: Continuous error injection. All writes to the message RAM are corrupted based on the value of EINJ_MASK b0: One time error injection. Only the first write to the address defined in EINJ_OFFSET is corrupted. After which EINJ_EN is cleared to b0 and EINJ_ONE_TIME_ERR_OCCURED is set to b1.
0	0h RW/AC	**Error Injection Enable (EINJ_EN):** 1 - Parity error injection is enabled 0 - Parity error injection is disabled. Once the one time parity error is injected, EINJ_EN deasserts.

7.2.76 Parity Error Injection Offset (PAR_EINJ_OFFSET) - Offset 60Ch

Parity error injection offset in dby_can message RAM

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:0	0000h RW	**Error Injection Offset (EINJ_OFFSET):** Offset at which an error will be injected, if enabled. This offset is relative to 0x0 in dby_can memory space.

7.2.77 Parity Error Injection Data Mask (PAR_EINJ_DATA_MASK) - Offset 610h

Parity error injection data mask for dby_can

Type	Size	Offset	Default
MMIO	32 bit	BAR + 610h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Error Injection Data Mask (EINJ_DATA_MASK):** This field is XOR'd with the incoming write data in order to flip data bit/bits with respect to the value the parity bit was calculated for

7.2.78 Parity Error Injection Parity Mask (PAR_EINJ_PARITY_MASK) - Offset 614h

Parity error injection data mask for dby_can

Type	Size	Offset	Default
MMIO	32 bit	BAR + 614h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Error Injection Parity Mask (EINJ_PARITY_MASK):** This field is XOR'd with the parity bits in order to flip data bit/bits with respect to the value the parity bit was calculated for

7.2.79 D0i3 Control (D0I3C) - Offset 8000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

7.2.80 Clock Gating And Soft Reset (CGSR) - Offset 8004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

8 Quadrature Encoder Pulse (QEP) Interface

8.1 QEP Configuration Registers Summary

This chapter documents the registers of the Intel® PSE Quadrature Encoder Peripheral, QEP devices. This contains multiple Intel® PSE Quadrature Encoder Peripheral, QEP Controller devices:

- Intel® PSE QEP Controller #0 - Bus: 0, Device: 24, Function: 3
- Intel® PSE QEP Controller #1 - Bus: 0, Device: 24, Function: 4
- Intel® PSE QEP Controller #2 - Bus: 0, Device: 24, Function: 5
- Intel® PSE QEP Controller #3 - Bus: 0, Device: 24, Function: 6

DID Values:

Intel® PSE QEP Controller #0- D24: F3 - 4BC3h

Intel® PSE QEP Controller #1- D24: F4 - 4B81h

Intel® PSE QEP Controller #2- D24: F5 - 4B82h

Intel® PSE QEP Controller #3- D24: F6 - 4B83h

Table 8-1. Summary of Bus: 0, Device: 24, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4BC30000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h

Table 8-1. Summary of Bus: 0, Device: 24, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

8.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4BC30000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4BC3h RO/P	**Device Id Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

8.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

8.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

8.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

8.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

8.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

8.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

8.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

8.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

8.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

8.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

8.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

8.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

8.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

8.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

8.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

8.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

8.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

8.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

8.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

8.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

8.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

8.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

8.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

8.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

8.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

8.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

8.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

8.2 QEP MMIO Registers Summary

Table 8-2. Summary of Bus: 0, Device: 24, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	QEPCON	0000001Ch
4h	4	QEPFLT	00000000h
8h	4	QEPCOUNT	00000000h
Ch	4	QEPMAX	FFFFFFFFh
10h	4	QEPWDT	00000000h
14h	4	QEPCAPDIV	00000000h
18h	4	QEPCNTR	00000000h
1Ch	4	QEPCAPBUF	00000000h
20h	4	QEPINT_STAT	00000000h
24h	4	QEPINT_MASK	00000000h
1000h	4	D0i3 Control (D0I3C)	00000008h
1004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

8.2.1 QEPCON - Offset 0h

QEP Control Register. This register controls the QEP operation and provides status flags for the state of the QEP module

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	0000001Ch

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**FIFO_EMPTY:** Capture FIFO Empty Status Flag. Set when the FIFO is empty
14:12	0h RW/L	**FIFO_THRE:** Capture FIFO Threshold. It contains the number of valid data entries in the FIFO: NUM_DATA_ENTRIES = FIFO_THRE + 1 It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
11	0h RW/L	**CAP_MODE:** Capture Block Mode. It selects the PhaseA event which triggers the FIFO to store the current QEPCNTR value 0 = Single edge 1 = Both edges It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
10:9	0h RW/L	**INDX_GATING:** Index Gating Select. It selects the state of PhaseA and PhaseB signals at which the index pulse will be gated 00 = PhaseA low and PhaseB low 01 = PhaseA low and PhaseB high 10 = PhaseA high and PhaseB low 11 = PhaseA high and PhaseB high It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
8	0h RW/L	**COUNT_RST_MODE:** Position Counter Reset Mode 0 = Position counter reset on index event 1 = Position counter reset on maximum position It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
7	0h RO	**Reserved**
6	0h RW/L	**OP_MODE:** Operating Mode 0 = Quadrature Encoder Peripheral (QEP) 1 = Capture Compare (CC) It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
5	0h RW/L	**SWPAB:** Phase A and Phase B Input Swap Select 0 = Phase A and Phase B inputs are not swapped 1 = Phase A and Phase B inputs are swapped It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
4	1h RW/L	**EDGE_INDX:** Edge selection of the Index input signal 0 = Falling edge 1 = Rising edge It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
3	1h RW/L	**EDGE_B:** Edge selection of the PhaseB input signal 0 = Falling edge 1 = Rising edge It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**EDGE_A:** Edge selection of the PhaseA input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
1	0h RW/L	**FLT_EN:** Noise Filters Enable 0 = Filters disabled 1 = Filters enabled It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
0	0h RW	**EN:** QEP/CC Enable 0 = QEP/CC disabled 1 = QEP/CC enabled

8.2.2 QEPFLT - Offset 4h

QEP Noise Filter Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW/L	**MAX_COUNT:** Noise Filter Maximum Count. It selects the maximum glitch width to remove in terms of peripheral clock cycles: PCLK_CYCLES = MAX_COUNT + 2 It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

8.2.3 QEPCOUNT - Offset 8h

QEP Position Counter Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**POS_COUNT:** Position Count Value. It stores the count value currently reached by the position counter. Disabling the peripheral will automatically clear its content.

8.2.4 QEPMAX - Offset Ch

QEP Maximum Position Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/L	**MAX_COUNT:** Maximum Position Count. It defines the operating range for the position counter. It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

8.2.5 QEPWDT - Offset 10h

QEP Watchdog Timer Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**TOP:** Watchdog Timer Timeout Period. When the WDT reaches this value, a dedicated interrupt is generated to flag a stall event. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

8.2.6 QEPCAPDIV - Offset 14h

QEP Capture Divider Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**CLK_DIV:** Clock Divider Value. It allows the clock to be divided as follows: 000 = clock divided by 1 001 = clock divided by 2 010 = clock divided by 4 011 = clock divided by 8 100 = clock divided by 16 101 = clock divided by 32 110 = clock divided by 64 111 = clock divided by 128 It is write able by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

8.2.7 QEPCNTR - Offset 18h

QEP Capture Counter Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CAP_COUNT:** Capture Count Value. It stores the count value currently reached by the free-running capture counter. Disabling the peripheral will automatically clear its content.

8.2.8 QEPCAPBUF - Offset 1Ch

QEP Capture Data Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** This is the register the processor reads from when retrieving bytes from FIFO

8.2.9 QEPINT_STAT - Offset 20h

QEP Raw Interrupt Status Register. Each bit in this register has a corresponding mask bit in the QEPINT_MASK register. These bits are cleared by writing '1' to the matching interrupt register field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C/V	**FIFOCRIT/QEP_PH_ERR_INTR** : In Capture mode, Capture Function Event FIFO Critical Interrupt. The number of entries in the Capture FIFO has reached the configured threshold level. In Encoder mode, this bit is set when phase error has occurred on the QEP inputs.
4	0h RW/1C/V	**FIFOENTRY:** Capture Function Event FIFO Entry Interrupt. An entry has been added to the 'Capture' FIFO.
3	0h RW/1C/V	**QEPDIR:** QEP Function Change Of Direction Detected Interrupt. The Quadrature Decoder has detected that the attached motor (or user dial device) has changed direction.
2	0h RW/1C/V	**QEPRST_UP:** QEPCOUNT Reset detect with forward count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
1	0h RW/1C/V	**QEPRST_DOWN:** QEPCOUNT Reset detect with reverse count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
0	0h RW/1C/V	**WDT:** Watchdog Timeout Interrupt. The Watchdog Timer value has reached the watchdog comparator value.

8.2.10 QEPINT_MASK - Offset 24h

QEP Interrupt Mask Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**FIFOCRIT:** This bit masks the FIFOCRIT interrupt bit from the QEPINT_STAT register
4	0h RW	**FIFOENTRY:** This bit masks the FIFOENTRY interrupt bit from the QEPINT_STAT register
3	0h RW	**QEPDIR:** This bit masks the QEPDIR interrupt bit from the QEPINT_STAT register

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**QEPRST_UP:** This bit masks the QEPRST_UP interrupt bit from the QEPINT_STAT register
1	0h RW	**QEPRST_DOWN:** This bit masks the QEPRST_DOWN interrupt bit from the QEPINT_STAT register
0	0h RW	**WDT:** This bit masks the WDT interrupt bit from the QEPINT_STAT register

8.2.11 D0i3 Control (D0I3C) - Offset 1000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit(bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit(bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit(bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

8.2.12 Clock Gating And Soft Reset (CGSR) - Offset 1004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

9 Serial Peripheral Interface (SPI) Interface

9.1 SPI Configuration Registers Summary

This chapter documents the registers of the Intel® PSE devices. The processor contains multiple Intel® PSE SPI Controller devices:

- Intel® PSE SPI Controller #0 - Bus: 0, Device: 19, Function: 0
- Intel® PSE SPI Controller #1 - Bus: 0, Device: 19, Function: 1
- Intel® PSE SPI Controller #2 - Bus: 0, Device: 19, Function: 2
- Intel® PSE SPI Controller #3 - Bus: 0, Device: 19, Function: 3

DID Values:

- Intel® PSE SPI Controller #0 - D19: F0 - 4B84h
- Intel® PSE SPI Controller #1 - D19: F1 - 4B85h
- Intel® PSE SPI Controller #2 - D19: F2 - 4B86h
- Intel® PSE SPI Controller #3 - D19: F3 - 4B87h

Table 9-1. Summary of Bus: 0, Device: 19, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4B840000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h

Table 9-1. Summary of Bus: 0, Device: 19, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

9.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4B840000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B84h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

9.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

9.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

9.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

9.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

9.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

9.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

9.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

9.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

9.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

9.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

9.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

9.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

9.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

9.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

9.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

9.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

9.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

9.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

9.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

9.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

9.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

9.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

9.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

9.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

9.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

9.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

9.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

9.2 SPI MMIO Registers Summary

Table 9-2. Summary of Bus: 0, Device: 19, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	CTRLR0	01000007h
4h	4	CTRLR1	00000000h
8h	4	SSIENR	00000000h
Ch	4	MWCR	00000000h
10h	4	SER	00000000h
14h	4	BAUDR	00000000h
18h	4	TXFTLR	00000000h
1Ch	4	RXFTLR	00000000h
20h	4	TXFLR	00000000h
24h	4	RXFLR	00000000h
28h	4	SR	00000006h
2Ch	4	IMR	0000003Fh
30h	4	ISR	00000000h
34h	4	RISR	00000000h
38h	4	TXOICR	00000000h
3Ch	4	RXOICR	00000000h
40h	4	RXUICR	00000000h
44h	4	MSTICR	00000000h
48h	4	ICR	00000000h
4Ch	4	DMACR	00000000h
50h	4	DMATDLR	00000000h
54h	4	DMARDLR	00000000h
58h	4	IDR	FFFFFFFFh
5Ch	4	SSI_VERSION_ID	3430322Ah
60h	4	DR0	00000000h
64h	4	DR1	00000000h
68h	4	DR2	00000000h
6Ch	4	DR3	00000000h
70h	4	DR4	00000000h
74h	4	DR5	00000000h
78h	4	DR6	00000000h
7Ch	4	DR7	00000000h
80h	4	DR8	00000000h
84h	4	DR9	00000000h
88h	4	DR10	00000000h
8Ch	4	DR11	00000000h

Table 9-2. Summary of Bus: 0, Device: 19, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90h	4	DR12	00000000h
94h	4	DR13	00000000h
98h	4	DR14	00000000h
9Ch	4	DR15	00000000h
A0h	4	DR16	00000000h
A4h	4	DR17	00000000h
A8h	4	DR18	00000000h
ACh	4	DR19	00000000h
B0h	4	DR20	00000000h
B4h	4	DR21	00000000h
B8h	4	DR22	00000000h
BCh	4	DR23	00000000h
C0h	4	DR24	00000000h
C4h	4	DR25	00000000h
C8h	4	DR26	00000000h
CCh	4	DR27	00000000h
D0h	4	DR28	00000000h
D4h	4	DR29	00000000h
D8h	4	DR30	00000000h
DCh	4	DR31	00000000h
E0h	4	DR32	00000000h
E4h	4	DR33	00000000h
E8h	4	DR34	00000000h
ECh	4	DR35	00000000h
F0h	4	RX_SAMPLE_DLY	00000000h
FCh	4	RSVD	00000000h
1000h	4	D0i3 Control (D0I3C)	00000008h
1004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

9.2.1 CTRLR0 - Offset 0h

Control Register 0 - This register controls the serial data transfer. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: SSI_CTRLR0_RST

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	01000007h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RW	**SSTE:** Slave Select Toggle Enable. When operating in SPI mode with clock phase (SCPH) set to 0, this register controls the behavior of the slave select line (ss_*_n) between data frames. If this register field is set to 1 the ss_*_n line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while ss_*_n is high; if this register field is set to 0 the ss_*_n will stay low and sclk will run continuously for the duration of the transfer. ***Note***: This register is only valid when SSI_SCPH0_SSTOGGLE is set to 1.
23	0h RO	**Reserved**
22:21	0h RO/V	**SPI_FRF:** SPI Frame Format: Selects data frame format for Transmitting/Receiving the data Bits only valid when SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode. When SSI_SPI_MODE is configured for "Dual Mode", 10/11 combination is reserved. When SSI_SPI_MODE is configured for "Quad Mode", 11 combination is reserved.
20:16	00h RO/V	**DFS_32:** Data Frame Size in 32-bit transfer size mode. Used to select the data frame size in 32-bit transfer mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You are responsible for making sure that transmit data is right-justified before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. ***Note***: When SSI_SPI_MODE is either set to “Dual” or “Quad” or “Octal” mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 0x01, - DFS value should be multiple of 4 if SPI_FRF = 0x10, - DFS value should be multiple of 8 if SPI_FRF = 0x11.
15:12	0h RW	**CFS:** Control Frame Size. Selects the length of the control word for the Microwire frame format.
11	0h RW	**SRL:** Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the DW_apb_ssi is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back
10	0h RO	**Reserved**
9:8	0h RW	**TMOD:** Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the DW_apb_ssi is configured as master device. 00 - Transmit & Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read When SSI_SPI_MODE is either set to “Dual” or “Quad” or "Octal" mode and SPI_FRF is not set to 2'b00. There are only two valid combinations: 10 - Read 01 - Write

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**SCPOL:** Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the DW_apb_ssi master is not actively transferring data on the serial bus.
6	0h RW	**SCPH:** Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.
5:4	0h RW	**FRF:** Frame Format. Selects which serial protocol transfers the data.
3:0	7h RW	**DFS:** Data Frame Size. This register field is only valid when SSI_MAX_XFER_SIZE is configured to 16. If SSI_MAX_XFER_SIZE is configured to 32, then writing to this field will not have any effect. Selects the data frame length. When the data frame size is programmed to be less than 16 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data ***Note***: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 01, - DFS value should be multiple of 4 if SPI_FRF = 10, - DFS value should be multiple of 8 if SPI_FRF = 11.

9.2.2 CTRLR1 - Offset 4h

Control Register 1 - This register exists only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**NDF:** Number of Data Frames. When TMOD = 10 or TMOD = 11 , this register field sets the number of data frames to be continuously received by the DW_apb_ssi. The DW_apb_ssi continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When the DW_apb_ssi is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the DW_apb_ssi is configured as a serial slave.

9.2.3 SSIENR - Offset 8h

SSI Enable Register - This register enables and disables the DW_apb_ssi. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SSI_EN:** SSI Enable. Enables and disables all DW_apb_ssi operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the DW_apb_ssi control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

9.2.4 MWCR - Offset Ch

Microwire Control Register - This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**MHS:** Microwire Handshaking. Relevant only when the DW_apb_ssi is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the DW_apb_ssi checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register.
1	0h RW	**MDD:** Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the DW_apb_ssi MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the DW_apb_ssi MacroCell to the external serial device.
0	0h RW	**MWMOD:** Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

9.2.5 SER - Offset 10h

Slave Enable Register - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the DW_apb_ssi master. Up to 16 slave-select output pins are available on the DW_apb_ssi master. Register bits can be set or cleared when SSI_EN=0. If SSI_EN=1, then register bits can be set (to delay the slave select assertion while TX FIFO is getting filled) but cannot be cleared. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**SER:** Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (ss_x_n) from the DW_apb_ssi master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

9.2.6 BAUDR - Offset 14h

Baud Rate Select - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**SCKDV:** SSI Clock Divider. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fssi_clk/SCKDV where SCKDV is any even value between 2 and 65534. For example, for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz

9.2.7 TXFTLR - Offset 18h

Transmit FIFO Threshold Level - This register controls the threshold value for the transmit FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**TFT:** Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

9.2.8 RXFTLR - Offset 1Ch

Receive FIFO Threshold Level - This register controls the threshold value for the receive FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RFT:** Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

9.2.9 TXFLR - Offset 20h

Transmit FIFO Level Register - This register contains the number of valid data entries in the transmit FIFO memory. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXTFL:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.2.10 RXFLR - Offset 24h

Receive FIFO Level Register - This register contains the number of valid data entries in the receive FIFO memory. This register can be ready at any time. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXTFL:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.2.11 SR - Offset 28h

Status Register - This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt. Reset Value: 0x6

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**DCOL:** Data Collision Error. Relevant only when the DW_apb_ssi is configured as a master device. This bit will be set if ss_in_n input is asserted by other master, when the DW_apb_ssi master is in the middle of the transfer. This informs the processor that the last data transfer was halted before completion. This bit is cleared when read.
5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty locations, this bit is cleared.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.
2	1h RO/V	**TFE:** Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO/V	**BUSY:** SSI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the DW_apb_ssi is idle or disabled.

9.2.12 IMR - Offset 2Ch

Interrupt Mask Register - This read/write reigster masks or enables all interrupts generated by the DW_apb_ssi. When the DW_apb_ssi is configured as a slave device, the MSTIM bit field is not present. This changes the reset value from 0x3F for serial-master configurations to 0x1F for serial-slave configurations. Reset Value: (SSI_IS_MASTER == 1) ? 0x3F : 0x1F

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2Ch	0000003Fh

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW	**MSTIM:** Multi-Master Contention Interrupt Mask. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	1h RW	**RXFIM:** Receive FIFO Full Interrupt Mask
3	1h RW	**RXOIM:** Receive FIFO Overflow Interrupt Mask
2	1h RW	**RXUIM:** Receive FIFO Underflow Interrupt Mask
1	1h RW	**TXOIM:** Transmit FIFO Overflow Interrupt Mask
0	1h RW	**TXEIM:** Transmit FIFO Empty Interrupt Mask

9.2.13 ISR - Offset 30h

Interrupt Status Register - This register reports the status of the DW_apb_ssi interrupts after they have been masked. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIS:** Multi-Master Contention Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIS:** Receive FIFO Full Interrupt Status
3	0h RO/V	**RXOIS:** Receive FIFO Overflow Interrupt Status
2	0h RO/V	**RXUIS:** Receive FIFO Underflow Interrupt Status
1	0h RO/V	**TXOIS:** Transmit FIFO Overflow Interrupt Status
0	0h RO/V	**TXEIS:** Transmit FIFO Empty Interrupt Status

9.2.14 RISR - Offset 34h

Raw Interrupt Status Register - This read-only register reports the status of the DW_apb_ssi interrupts prior to masking. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIR:** Multi-Master Contention Raw Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIR:** Receive FIFO Full Raw Interrupt Status
3	0h RO/V	**RXOIR:** Receive FIFO Overflow Raw Interrupt Status
2	0h RO/V	**RXUIR:** Receive FIFO Underflow Raw Interrupt Status
1	0h RO/V	**TXOIR:** Transmit FIFO Overflow Raw Interrupt Status
0	0h RO/V	**TXEIR:** Transmit FIFO Empty Raw Interrupt Status

9.2.15 TXOICR - Offset 38h

Transmit FIFO Overflow Interrupt Clear Register. Register - Transmit FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TXOICR:** Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

9.2.16 RXOICR - Offset 3Ch

Receive FIFO Overflow Interrupt Clear Register - Receive FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXOICR:** Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

9.2.17 RXUICR - Offset 40h

Receive FIFO Underflow Interrupt Clear Register - Receive FIFO Underflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXUICR:** Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

9.2.18 MSTICR - Offset 44h

Multi-Master Interrupt Clear Register - Multi-Master Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**MSTICR:** Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_mst_intr interrupt; writing has no effect.

9.2.19 ICR - Offset 48h

Interrupt Clear Register - Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**ICR:** Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

9.2.20 DMACR - Offset 4Ch

DMA Control Register - This register is only valid when DW_apb_ssi is configured with a set of DMA Controller interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel

9.2.21 DMATDLR - Offset 50h

DMA Transmit Data Level - This register is only valid when the DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.2.22 DMARDLR - Offset 54h

DMA Receive Data Level - This register is only valid when DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.

9.2.23 IDR - Offset 58h

Identification Register - This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant. Reset Value: SSI_ID

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**IDCODE:** Identification code. The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant.

9.2.24 SSI_VERSION_ID - Offset 5Ch

coreKit version ID Register - This read-only register stores the specific DW_apb_ssi component version. Reset Value: SSI_VERSION_ID

Type	Size	Offset	Default
MMIO	32 bit	BAR + 5Ch	3430322Ah

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**SSI_COMP_VERSION:** Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*.

9.2.25 DR0 - Offset 60h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.26 DR1 - Offset 64h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.27 DR2 - Offset 68h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.28 DR3 - Offset 6Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.29 DR4 - Offset 70h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.30 DR5 - Offset 74h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.31 DR6 - Offset 78h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.32 DR7 - Offset 7Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.33 DR8 - Offset 80h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.34 DR9 - Offset 84h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.35 DR10 - Offset 88h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 88h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.36 DR11 - Offset 8Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.37 DR12 - Offset 90h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.38 DR13 - Offset 94h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.39 DR14 - Offset 98h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.40 DR15 - Offset 9Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.41 DR16 - Offset A0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.42 DR17 - Offset A4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.43 DR18 - Offset A8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.44 DR19 - Offset ACh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.45 DR20 - Offset B0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.46 DR21 - Offset B4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.47 DR22 - Offset B8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.48 DR23 - Offset BCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.49 DR24 - Offset C0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.50 DR25 - Offset C4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.51 DR26 - Offset C8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.52 DR27 - Offset CCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.53 DR28 - Offset D0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.54 DR29 - Offset D4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.55 DR30 - Offset D8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.56 DR31 - Offset DCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.57 DR32 - Offset E0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.58 DR33 - Offset E4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the

transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.59 DR34 - Offset E8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.60 DR35 - Offset ECh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid,

otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.
NOTE: The DR registers in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

9.2.61 RX_SAMPLE_DLY - Offset F0h

RX Sample Delay Register - This register is only valid when the DW_apb_ssi is configured with rxd sample delay logic (SSI_HAS_RX_SAMPLE_DELAY==1). When the DW_apb_ssi is not configured with rxd sample delay logic, this register will not exist and writing to its address location will have no effect; reading from its address will return zero. This register control the number of ssi_clk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	BAR + F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RSD:** Rxd Sample Delay. This register is used to delay the sample of the rxd input port. Each value represents a single ssi_clk delay on the sample of rxd. ***Note***: If this register is programmed with a value that exceeds the depth of the internal shift registers (SSI_RX_DLY_SR_DEPTH) zero delay will be applied to the rxd sample.

9.2.62 RSVD - Offset FCh

Reserved

Type	Size	Offset	Default
MMIO	32 bit	BAR + FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

9.2.63 D0i3 Control (D0I3C) - Offset 1000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

9.2.64 Clock Gating And Soft Reset (CGSR) - Offset 1004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

10 General Purpose Input/Output (GPIO) Interface

10.1 GPIO Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 19, Function 4 and 5.

DID Values:

- Intel® PSE: GPIO Controller #0:- D19: F4 - 4B88h
- Intel® PSE: GPIO Controller #1:- D19: F5 - 4B89h

Table 10-1. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4B880000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h

Table 10-1. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

10.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4B880000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B88h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

10.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort

Bit Range	Default & Access	Field Name (ID): Description
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

10.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

10.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

10.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

10.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

10.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

10.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

10.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

10.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

10.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

10.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

10.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

10.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

10.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

10.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

10.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

10.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

10.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

10.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

10.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

10.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

10.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

10.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

10.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

10.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

10.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

10.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

10.2 GPIO MMIO Registers Summary

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	GPIO Pin DirectionLock (GCCR)	00000000h
4h	4	GPIO Pin Level (GPLR0)	00000000h
8h	4	GPIO Pin Level (GPLR1)	00000000h
1Ch	4	GPIO Pin Direction (GPDR0)	00000000h
20h	4	GPIO Pin Direction (GPDR1)	00000000h
34h	4	GPIO Pin Output Set (GPSR0)	00000000h
38h	4	GPIO Pin Output Set (GPSR1)	00000000h
4Ch	4	GPIO Pin Output Clear (GPCR0)	00000000h
50h	4	GPIO Pin Output Clear (GPCR1)	00000000h
64h	4	GPIO Rising Edge Detect Enable (GRER0)	00000000h
68h	4	GPIO Rising Edge Detect Enable (GRER1)	00000000h
7Ch	4	GPIO Falling Edge Detect Enable (GFER0)	00000000h
80h	4	GPIO Falling Edge Detect Enable (GFER1)	00000000h
94h	4	GPIO Glitch Filter Bypass (GFBR0)	00000000h
98h	4	GPIO Glitch Filter Bypass (GFBR1)	00000000h
ACh	4	GPIO Interrupt Mask (GIMR0)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B0h	4	GPIO Interrupt Mask (GIMR1)	00000000h
C4h	4	GPIO Interrupt Source (GISR0)	00000000h
C8h	4	GPIO Interrupt Source (GISR1)	00000000h
100h	4	GPIO Wake Mask (GWMR0)	00000000h
104h	4	GPIO Wake Mask (GWMR1)	00000000h
118h	4	GPIO Wake Source (GWSR0)	00000000h
11Ch	4	GPIO Wake Source (GWSR1)	00000000h
130h	4	GPIO Secure Input (GSEC)	00000000h
1000h	4	REG TGPIOCTL0 (TGPIO0_CTL_REG)	00002000h
1004h	4	REG TGPIOCOMPV0_31_0 (TGPIO0_COMPV_31_0)	00000000h
1008h	4	REG TGPIOCOMPV0_63_32 (TGPIO0_COMPV_63_32)	00000000h
100Ch	4	REG TGPIOPIV0_31_0 (TGPIO0_PIV_31_0)	00000000h
1010h	4	REG TGPIOPIV0_63:32 (TGPIO0_PIV_63_32)	00000000h
1014h	4	REG TGPIOTCV0_31_0 (TGPIO0_TCV_31_0)	00000000h
1018h	4	REG TGPIOTCV0_63_32 (TGPIO0_TCV_63_32)	00000000h
101Ch	4	REG TGPIOECCV0_31_0 (TGPIO0_ECCV_31_0)	00000000h
1020h	4	REG TGPIOECCV0_63_32 (TGPIO0_ECCV_63_32)	00000000h
1024h	4	REG TGPIOEC0_31_0 (TGPIO0_EC_31_0)	00000000h
1028h	4	REG TGPIOEC0_63_32 (TGPIO0_EC_63_32)	00000000h
102Ch	4	REG TGPIOMATCHMASK0_31_0 (TGPIO0_MATCH_MASK_31_0)	00000000h
1030h	4	REG TGPIOMATCHMASK0_63_32 (TGPIO0_MATCH_MASK_63_32)	00000000h
1040h	4	REG TGPIOCTL1 (TGPIO1_CTL_REG)	00002000h
1044h	4	REG TGPIOCOMPV1_31_0 (TGPIO1_COMPV_31_0)	00000000h
1048h	4	REG TGPIOCOMPV1_63_32 (TGPIO1_COMPV_63_32)	00000000h
104Ch	4	REG TGPIOPIV1_31_0 (TGPIO1_PIV_31_0)	00000000h
1050h	4	REG TGPIOPIV1_63:32 (TGPIO1_PIV_63_32)	00000000h
1054h	4	REG TGPIOTCV1_31_0 (TGPIO1_TCV_31_0)	00000000h
1058h	4	REG TGPIOTCV1_63_32 (TGPIO1_TCV_63_32)	00000000h
105Ch	4	REG TGPIOECCV1_31_0 (TGPIO1_ECCV_31_0)	00000000h
1060h	4	REG TGPIOECCV1_63_32 (TGPIO1_ECCV_63_32)	00000000h
1064h	4	REG TGPIOEC1_31_0 (TGPIO1_EC_31_0)	00000000h
1068h	4	REG TGPIOEC1_63_32 (TGPIO1_EC_63_32)	00000000h
106Ch	4	REG TGPIOMATCHMASK1_31_0 (TGPIO1_MATCH_MASK_31_0)	00000000h
1070h	4	REG TGPIOMATCHMASK1_63_32 (TGPIO1_MATCH_MASK_63_32)	00000000h
1080h	4	REG TGPIOCTL2 (TGPIO2_CTL_REG)	00002000h
1084h	4	REG TGPIOCOMPV2_31_0 (TGPIO2_COMPV_31_0)	00000000h
1088h	4	REG TGPIOCOMPV2_63_32 (TGPIO2_COMPV_63_32)	00000000h
108Ch	4	REG TGPIOPIV2_31_0 (TGPIO2_PIV_31_0)	00000000h
1090h	4	REG TGPIOPIV2_63:32 (TGPIO2_PIV_63_32)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1094h	4	REG TGPIOTCV2_31_0 (TGPIO2_TCV_31_0)	00000000h
1098h	4	REG TGPIOTCV2_63_32 (TGPIO2_TCV_63_32)	00000000h
109Ch	4	REG TGPIOECCV2_31_0 (TGPIO2_ECCV_31_0)	00000000h
10A0h	4	REG TGPIOECCV2_63_32 (TGPIO2_ECCV_63_32)	00000000h
10A4h	4	REG TGPIOEC2_31_0 (TGPIO2_EC_31_0)	00000000h
10A8h	4	REG TGPIOEC2_63_32 (TGPIO2_EC_63_32)	00000000h
10ACh	4	REG TGPIOMATCHMASK2_31_0 (TGPIO2_MATCH_MASK_31_0)	00000000h
10B0h	4	REG TGPIOMATCHMASK2_63_32 (TGPIO2_MATCH_MASK_63_32)	00000000h
10C0h	4	REG TGPIOCTL3 (TGPIO3_CTL_REG)	00002000h
10C4h	4	REG TGPIOCOMPV3_31_0 (TGPIO3_COMPV_31_0)	00000000h
10C8h	4	REG TGPIOCOMPV3_63_32 (TGPIO3_COMPV_63_32)	00000000h
10CCh	4	REG TGPIOPIV3_31_0 (TGPIO3_PIV_31_0)	00000000h
10D0h	4	REG TGPIOPIV3_63:32 (TGPIO3_PIV_63_32)	00000000h
10D4h	4	REG TGPIOTCV3_31_0 (TGPIO3_TCV_31_0)	00000000h
10D8h	4	REG TGPIOTCV3_63_32 (TGPIO3_TCV_63_32)	00000000h
10DCh	4	REG TGPIOECCV3_31_0 (TGPIO3_ECCV_31_0)	00000000h
10E0h	4	REG TGPIOECCV3_63_32 (TGPIO3_ECCV_63_32)	00000000h
10E4h	4	REG TGPIOEC3_31_0 (TGPIO3_EC_31_0)	00000000h
10E8h	4	REG TGPIOEC3_63_32 (TGPIO3_EC_63_32)	00000000h
10ECh	4	REG TGPIOMATCHMASK3_31_0 (TGPIO3_MATCH_MASK_31_0)	00000000h
10F0h	4	REG TGPIOMATCHMASK3_63_32 (TGPIO3_MATCH_MASK_63_32)	00000000h
1100h	4	REG TGPIOCTL4 (TGPIO4_CTL_REG)	00002000h
1104h	4	REG TGPIOCOMPV4_31_0 (TGPIO4_COMPV_31_0)	00000000h
1108h	4	REG TGPIOCOMPV4_63_32 (TGPIO4_COMPV_63_32)	00000000h
110Ch	4	REG TGPIOPIV4_31_0 (TGPIO4_PIV_31_0)	00000000h
1110h	4	REG TGPIOPIV4_63:32 (TGPIO4_PIV_63_32)	00000000h
1114h	4	REG TGPIOTCV4_31_0 (TGPIO4_TCV_31_0)	00000000h
1118h	4	REG TGPIOTCV4_63_32 (TGPIO4_TCV_63_32)	00000000h
111Ch	4	REG TGPIOECCV4_31_0 (TGPIO4_ECCV_31_0)	00000000h
1120h	4	REG TGPIOECCV4_63_32 (TGPIO4_ECCV_63_32)	00000000h
1124h	4	REG TGPIOEC4_31_0 (TGPIO4_EC_31_0)	00000000h
1128h	4	REG TGPIOEC4_63_32 (TGPIO4_EC_63_32)	00000000h
112Ch	4	REG TGPIOMATCHMASK4_31_0 (TGPIO4_MATCH_MASK_31_0)	00000000h
1130h	4	REG TGPIOMATCHMASK4_63_32 (TGPIO4_MATCH_MASK_63_32)	00000000h
1140h	4	REG TGPIOCTL5 (TGPIO5_CTL_REG)	00002000h
1144h	4	REG TGPIOCOMPV5_31_0 (TGPIO5_COMPV_31_0)	00000000h
1148h	4	REG TGPIOCOMPV5_63_32 (TGPIO5_COMPV_63_32)	00000000h
114Ch	4	REG TGPIOPIV5_31_0 (TGPIO5_PIV_31_0)	00000000h
1150h	4	REG TGPIOPIV5_63:32 (TGPIO5_PIV_63_32)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1154h	4	REG TGPIOTCV5_31_0 (TGPIO5_TCV_31_0)	00000000h
1158h	4	REG TGPIOTCV5_63_32 (TGPIO5_TCV_63_32)	00000000h
115Ch	4	REG TGPIOECCV5_31_0 (TGPIO5_ECCV_31_0)	00000000h
1160h	4	REG TGPIOECCV5_63_32 (TGPIO5_ECCV_63_32)	00000000h
1164h	4	REG TGPIOEC5_31_0 (TGPIO5_EC_31_0)	00000000h
1168h	4	REG TGPIOEC5_63_32 (TGPIO5_EC_63_32)	00000000h
116Ch	4	REG TGPIOMATCHMASK5_31_0 (TGPIO5_MATCH_MASK_31_0)	00000000h
1170h	4	REG TGPIOMATCHMASK5_63_32 (TGPIO5_MATCH_MASK_63_32)	00000000h
1180h	4	REG TGPIOCTL6 (TGPIO6_CTL_REG)	00002000h
1184h	4	REG TGPIOCOMPV6_31_0 (TGPIO6_COMPV_31_0)	00000000h
1188h	4	REG TGPIOCOMPV6_63_32 (TGPIO6_COMPV_63_32)	00000000h
118Ch	4	REG TGPIOPIV6_31_0 (TGPIO6_PIV_31_0)	00000000h
1190h	4	REG TGPIOPIV6_63:32 (TGPIO6_PIV_63_32)	00000000h
1194h	4	REG TGPIOTCV6_31_0 (TGPIO6_TCV_31_0)	00000000h
1198h	4	REG TGPIOTCV6_63_32 (TGPIO6_TCV_63_32)	00000000h
119Ch	4	REG TGPIOECCV6_31_0 (TGPIO6_ECCV_31_0)	00000000h
11A0h	4	REG TGPIOECCV6_63_32 (TGPIO6_ECCV_63_32)	00000000h
11A4h	4	REG TGPIOEC6_31_0 (TGPIO6_EC_31_0)	00000000h
11A8h	4	REG TGPIOEC6_63_32 (TGPIO6_EC_63_32)	00000000h
11ACh	4	REG TGPIOMATCHMASK6_31_0 (TGPIO6_MATCH_MASK_31_0)	00000000h
11B0h	4	REG TGPIOMATCHMASK6_63_32 (TGPIO6_MATCH_MASK_63_32)	00000000h
11C0h	4	REG TGPIOCTL7 (TGPIO7_CTL_REG)	00002000h
11C4h	4	REG TGPIOCOMPV7_31_0 (TGPIO7_COMPV_31_0)	00000000h
11C8h	4	REG TGPIOCOMPV7_63_32 (TGPIO7_COMPV_63_32)	00000000h
11CCh	4	REG TGPIOPIV7_31_0 (TGPIO7_PIV_31_0)	00000000h
11D0h	4	REG TGPIOPIV7_63:32 (TGPIO7_PIV_63_32)	00000000h
11D4h	4	REG TGPIOTCV7_31_0 (TGPIO7_TCV_31_0)	00000000h
11D8h	4	REG TGPIOTCV7_63_32 (TGPIO7_TCV_63_32)	00000000h
11DCh	4	REG TGPIOECCV7_31_0 (TGPIO7_ECCV_31_0)	00000000h
11E0h	4	REG TGPIOECCV7_63_32 (TGPIO7_ECCV_63_32)	00000000h
11E4h	4	REG TGPIOEC7_31_0 (TGPIO7_EC_31_0)	00000000h
11E8h	4	REG TGPIOEC7_63_32 (TGPIO7_EC_63_32)	00000000h
11ECh	4	REG TGPIOMATCHMASK7_31_0 (TGPIO7_MATCH_MASK_31_0)	00000000h
11F0h	4	REG TGPIOMATCHMASK7_63_32 (TGPIO7_MATCH_MASK_63_32)	00000000h
1200h	4	REG TGPIOCTL8 (TGPIO8_CTL_REG)	00002000h
1204h	4	REG TGPIOCOMPV8_31_0 (TGPIO8_COMPV_31_0)	00000000h
1208h	4	REG TGPIOCOMPV8_63_32 (TGPIO8_COMPV_63_32)	00000000h
120Ch	4	REG TGPIOPIV8_31_0 (TGPIO8_PIV_31_0)	00000000h
1210h	4	REG TGPIOPIV8_63:32 (TGPIO8_PIV_63_32)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1214h	4	REG TGPIOTCV8_31_0 (TGPIO8_TCV_31_0)	00000000h
1218h	4	REG TGPIOTCV8_63_32 (TGPIO8_TCV_63_32)	00000000h
121Ch	4	REG TGPIOECCV8_31_0 (TGPIO8_ECCV_31_0)	00000000h
1220h	4	REG TGPIOECCV8_63_32 (TGPIO8_ECCV_63_32)	00000000h
1224h	4	REG TGPIOEC8_31_0 (TGPIO8_EC_31_0)	00000000h
1228h	4	REG TGPIOEC8_63_32 (TGPIO8_EC_63_32)	00000000h
122Ch	4	REG TGPIOMATCHMASK8_31_0 (TGPIO8_MATCH_MASK_31_0)	00000000h
1230h	4	REG TGPIOMATCHMASK8_63_32 (TGPIO8_MATCH_MASK_63_32)	00000000h
1240h	4	REG TGPIOCTL9 (TGPIO9_CTL_REG)	00002000h
1244h	4	REG TGPIOCOMPV9_31_0 (TGPIO9_COMPV_31_0)	00000000h
1248h	4	REG TGPIOCOMPV9_63_32 (TGPIO9_COMPV_63_32)	00000000h
124Ch	4	REG TGPIOPIV9_31_0 (TGPIO9_PIV_31_0)	00000000h
1250h	4	REG TGPIOPIV9_63:32 (TGPIO9_PIV_63_32)	00000000h
1254h	4	REG TGPIOTCV9_31_0 (TGPIO9_TCV_31_0)	00000000h
1258h	4	REG TGPIOTCV9_63_32 (TGPIO9_TCV_63_32)	00000000h
125Ch	4	REG TGPIOECCV9_31_0 (TGPIO9_ECCV_31_0)	00000000h
1260h	4	REG TGPIOECCV9_63_32 (TGPIO9_ECCV_63_32)	00000000h
1264h	4	REG TGPIOEC9_31_0 (TGPIO9_EC_31_0)	00000000h
1268h	4	REG TGPIOEC9_63_32 (TGPIO9_EC_63_32)	00000000h
126Ch	4	REG TGPIOMATCHMASK9_31_0 (TGPIO9_MATCH_MASK_31_0)	00000000h
1270h	4	REG TGPIOMATCHMASK9_63_32 (TGPIO9_MATCH_MASK_63_32)	00000000h
1280h	4	REG TGPIOCTL10 (TGPIO10_CTL_REG)	00002000h
1284h	4	REG TGPIOCOMPV10_31_0 (TGPIO10_COMPV_31_0)	00000000h
1288h	4	REG TGPIOCOMPV10_63_32 (TGPIO10_COMPV_63_32)	00000000h
128Ch	4	REG TGPIOPIV10_31_0 (TGPIO10_PIV_31_0)	00000000h
1290h	4	REG TGPIOPIV10_63:32 (TGPIO10_PIV_63_32)	00000000h
1294h	4	REG TGPIOTCV10_31_0 (TGPIO10_TCV_31_0)	00000000h
1298h	4	REG TGPIOTCV10_63_32 (TGPIO10_TCV_63_32)	00000000h
129Ch	4	REG TGPIOECCV10_31_0 (TGPIO10_ECCV_31_0)	00000000h
12A0h	4	REG TGPIOECCV10_63_32 (TGPIO10_ECCV_63_32)	00000000h
12A4h	4	REG TGPIOEC10_31_0 (TGPIO10_EC_31_0)	00000000h
12A8h	4	REG TGPIOEC10_63_32 (TGPIO10_EC_63_32)	00000000h
12ACh	4	REG TGPIOMATCHMASK10_31_0 (TGPIO10_MATCH_MASK_31_0)	00000000h
12B0h	4	REG TGPIOMATCHMASK10_63_32 (TGPIO10_MATCH_MASK_63_32)	00000000h
12C0h	4	REG TGPIOCTL11 (TGPIO11_CTL_REG)	00002000h
12C4h	4	REG TGPIOCOMPV11_31_0 (TGPIO11_COMPV_31_0)	00000000h
12C8h	4	REG TGPIOCOMPV11_63_32 (TGPIO11_COMPV_63_32)	00000000h
12CCh	4	REG TGPIOPIV11_31_0 (TGPIO11_PIV_31_0)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
12D0h	4	REG TGPIOPIV11_63:32 (TGPIO11_PIV_63_32)	00000000h
12D4h	4	REG TGPIOTCV11_31_0 (TGPIO11_TCV_31_0)	00000000h
12D8h	4	REG TGPIOTCV11_63_32 (TGPIO11_TCV_63_32)	00000000h
12DCh	4	REG TGPIOECCV11_31_0 (TGPIO11_ECCV_31_0)	00000000h
12E0h	4	REG TGPIOECCV11_63_32 (TGPIO11_ECCV_63_32)	00000000h
12E4h	4	REG TGPIOEC11_31_0 (TGPIO11_EC_31_0)	00000000h
12E8h	4	REG TGPIOEC11_63_32 (TGPIO11_EC_63_32)	00000000h
12ECh	4	REG TGPIOMATCHMASK11_31_0 (TGPIO11_MATCH_MASK_31_0)	00000000h
12F0h	4	REG TGPIOMATCHMASK11_63_32 (TGPIO11_MATCH_MASK_63_32)	00000000h
1300h	4	REG TGPIOCTL12 (TGPIO12_CTL_REG)	00002000h
1304h	4	REG TGPIOCOMPV12_31_0 (TGPIO12_COMPV_31_0)	00000000h
1308h	4	REG TGPIOCOMPV12_63_32 (TGPIO12_COMPV_63_32)	00000000h
130Ch	4	REG TGPIOPIV12_31_0 (TGPIO12_PIV_31_0)	00000000h
1310h	4	REG TGPIOPIV12_63:32 (TGPIO12_PIV_63_32)	00000000h
1314h	4	REG TGPIOTCV12_31_0 (TGPIO12_TCV_31_0)	00000000h
1318h	4	REG TGPIOTCV12_63_32 (TGPIO12_TCV_63_32)	00000000h
131Ch	4	REG TGPIOECCV12_31_0 (TGPIO12_ECCV_31_0)	00000000h
1320h	4	REG TGPIOECCV12_63_32 (TGPIO12_ECCV_63_32)	00000000h
1324h	4	REG TGPIOEC12_31_0 (TGPIO12_EC_31_0)	00000000h
1328h	4	REG TGPIOEC12_63_32 (TGPIO12_EC_63_32)	00000000h
132Ch	4	REG TGPIOMATCHMASK12_31_0 (TGPIO12_MATCH_MASK_31_0)	00000000h
1330h	4	REG TGPIOMATCHMASK12_63_32 (TGPIO12_MATCH_MASK_63_32)	00000000h
1340h	4	REG TGPIOCTL13 (TGPIO13_CTL_REG)	00002000h
1344h	4	REG TGPIOCOMPV13_31_0 (TGPIO13_COMPV_31_0)	00000000h
1348h	4	REG TGPIOCOMPV13_63_32 (TGPIO13_COMPV_63_32)	00000000h
134Ch	4	REG TGPIOPIV13_31_0 (TGPIO13_PIV_31_0)	00000000h
1350h	4	REG TGPIOPIV13_63:32 (TGPIO13_PIV_63_32)	00000000h
1354h	4	REG TGPIOTCV13_31_0 (TGPIO13_TCV_31_0)	00000000h
1358h	4	REG TGPIOTCV13_63_32 (TGPIO13_TCV_63_32)	00000000h
135Ch	4	REG TGPIOECCV13_31_0 (TGPIO13_ECCV_31_0)	00000000h
1360h	4	REG TGPIOECCV13_63_32 (TGPIO13_ECCV_63_32)	00000000h
1364h	4	REG TGPIOEC13_31_0 (TGPIO13_EC_31_0)	00000000h
1368h	4	REG TGPIOEC13_63_32 (TGPIO13_EC_63_32)	00000000h
136Ch	4	REG TGPIOMATCHMASK13_31_0 (TGPIO13_MATCH_MASK_31_0)	00000000h
1370h	4	REG TGPIOMATCHMASK13_63_32 (TGPIO13_MATCH_MASK_63_32)	00000000h
1380h	4	REG TGPIOCTL14 (TGPIO14_CTL_REG)	00002000h
1384h	4	REG TGPIOCOMPV14_31_0 (TGPIO14_COMPV_31_0)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1388h	4	REG TGPIOCOMPV14_63_32 (TGPIO14_COMPV_63_32)	00000000h
138Ch	4	REG TGPIOPIV14_31_0 (TGPIO14_PIV_31_0)	00000000h
1390h	4	REG TGPIOPIV14_63:32 (TGPIO14_PIV_63_32)	00000000h
1394h	4	REG TGPIOTCV14_31_0 (TGPIO14_TCV_31_0)	00000000h
1398h	4	REG TGPIOTCV14_63_32 (TGPIO14_TCV_63_32)	00000000h
139Ch	4	REG TGPIOECCV14_31_0 (TGPIO14_ECCV_31_0)	00000000h
13A0h	4	REG TGPIOECCV14_63_32 (TGPIO14_ECCV_63_32)	00000000h
13A4h	4	REG TGPIOEC14_31_0 (TGPIO14_EC_31_0)	00000000h
13A8h	4	REG TGPIOEC14_63_32 (TGPIO14_EC_63_32)	00000000h
13ACh	4	REG TGPIOMATCHMASK14_31_0 (TGPIO14_MATCH_MASK_31_0)	00000000h
13B0h	4	REG TGPIOMATCHMASK14_63_32 (TGPIO14_MATCH_MASK_63_32)	00000000h
13C0h	4	REG TGPIOCTL15 (TGPIO15_CTL_REG)	00002000h
13C4h	4	REG TGPIOCOMPV15_31_0 (TGPIO15_COMPV_31_0)	00000000h
13C8h	4	REG TGPIOCOMPV15_63_32 (TGPIO15_COMPV_63_32)	00000000h
13CCh	4	REG TGPIOPIV15_31_0 (TGPIO15_PIV_31_0)	00000000h
13D0h	4	REG TGPIOPIV15_63:32 (TGPIO15_PIV_63_32)	00000000h
13D4h	4	REG TGPIOTCV15_31_0 (TGPIO15_TCV_31_0)	00000000h
13D8h	4	REG TGPIOTCV15_63_32 (TGPIO15_TCV_63_32)	00000000h
13DCh	4	REG TGPIOECCV15_31_0 (TGPIO15_ECCV_31_0)	00000000h
13E0h	4	REG TGPIOECCV15_63_32 (TGPIO15_ECCV_63_32)	00000000h
13E4h	4	REG TGPIOEC15_31_0 (TGPIO15_EC_31_0)	00000000h
13E8h	4	REG TGPIOEC15_63_32 (TGPIO15_EC_63_32)	00000000h
13ECh	4	REG TGPIOMATCHMASK15_31_0 (TGPIO15_MATCH_MASK_31_0)	00000000h
13F0h	4	REG TGPIOMATCHMASK15_63_32 (TGPIO15_MATCH_MASK_63_32)	00000000h
1400h	4	REG TGPIOCTL16 (TGPIO16_CTL_REG)	00002000h
1404h	4	REG TGPIOCOMPV16_31_0 (TGPIO16_COMPV_31_0)	00000000h
1408h	4	REG TGPIOCOMPV16_63_32 (TGPIO16_COMPV_63_32)	00000000h
140Ch	4	REG TGPIOPIV16_31_0 (TGPIO16_PIV_31_0)	00000000h
1410h	4	REG TGPIOPIV16_63:32 (TGPIO16_PIV_63_32)	00000000h
1414h	4	REG TGPIOTCV16_31_0 (TGPIO16_TCV_31_0)	00000000h
1418h	4	REG TGPIOTCV16_63_32 (TGPIO16_TCV_63_32)	00000000h
141Ch	4	REG TGPIOECCV16_31_0 (TGPIO16_ECCV_31_0)	00000000h
1420h	4	REG TGPIOECCV16_63_32 (TGPIO16_ECCV_63_32)	00000000h
1424h	4	REG TGPIOEC16_31_0 (TGPIO16_EC_31_0)	00000000h
1428h	4	REG TGPIOEC16_63_32 (TGPIO16_EC_63_32)	00000000h
142Ch	4	REG TGPIOMATCHMASK16_31_0 (TGPIO16_MATCH_MASK_31_0)	00000000h
1430h	4	REG TGPIOMATCHMASK16_63_32 (TGPIO16_MATCH_MASK_63_32)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1440h	4	REG TGPIOCTL17 (TGPIO17_CTL_REG)	00002000h
1444h	4	REG TGPIOCOMPV17_31_0 (TGPIO17_COMPV_31_0)	00000000h
1448h	4	REG TGPIOCOMPV17_63_32 (TGPIO17_COMPV_63_32)	00000000h
144Ch	4	REG TGPIOPIV17_31_0 (TGPIO17_PIV_31_0)	00000000h
1450h	4	REG TGPIOPIV17_63:32 (TGPIO17_PIV_63_32)	00000000h
1454h	4	REG TGPIOTCV17_31_0 (TGPIO17_TCV_31_0)	00000000h
1458h	4	REG TGPIOTCV17_63_32 (TGPIO17_TCV_63_32)	00000000h
145Ch	4	REG TGPIOECCV17_31_0 (TGPIO17_ECCV_31_0)	00000000h
1460h	4	REG TGPIOECCV17_63_32 (TGPIO17_ECCV_63_32)	00000000h
1464h	4	REG TGPIOEC17_31_0 (TGPIO17_EC_31_0)	00000000h
1468h	4	REG TGPIOEC17_63_32 (TGPIO17_EC_63_32)	00000000h
146Ch	4	REG TGPIOMATCHMASK17_31_0 (TGPIO17_MATCH_MASK_31_0)	00000000h
1470h	4	REG TGPIOMATCHMASK17_63_32 (TGPIO17_MATCH_MASK_63_32)	00000000h
1480h	4	REG TGPIOCTL18 (TGPIO18_CTL_REG)	00002000h
1484h	4	REG TGPIOCOMPV18_31_0 (TGPIO18_COMPV_31_0)	00000000h
1488h	4	REG TGPIOCOMPV18_63_32 (TGPIO18_COMPV_63_32)	00000000h
148Ch	4	REG TGPIOPIV18_31_0 (TGPIO18_PIV_31_0)	00000000h
1490h	4	REG TGPIOPIV18_63:32 (TGPIO18_PIV_63_32)	00000000h
1494h	4	REG TGPIOTCV18_31_0 (TGPIO18_TCV_31_0)	00000000h
1498h	4	REG TGPIOTCV18_63_32 (TGPIO18_TCV_63_32)	00000000h
149Ch	4	REG TGPIOECCV18_31_0 (TGPIO18_ECCV_31_0)	00000000h
14A0h	4	REG TGPIOECCV18_63_32 (TGPIO18_ECCV_63_32)	00000000h
14A4h	4	REG TGPIOEC18_31_0 (TGPIO18_EC_31_0)	00000000h
14A8h	4	REG TGPIOEC18_63_32 (TGPIO18_EC_63_32)	00000000h
14ACh	4	REG TGPIOMATCHMASK18_31_0 (TGPIO18_MATCH_MASK_31_0)	00000000h
14B0h	4	REG TGPIOMATCHMASK18_63_32 (TGPIO18_MATCH_MASK_63_32)	00000000h
14C0h	4	REG TGPIOCTL19 (TGPIO19_CTL_REG)	00002000h
14C4h	4	REG TGPIOCOMPV19_31_0 (TGPIO19_COMPV_31_0)	00000000h
14C8h	4	REG TGPIOCOMPV19_63_32 (TGPIO19_COMPV_63_32)	00000000h
14CCh	4	REG TGPIOPIV19_31_0 (TGPIO19_PIV_31_0)	00000000h
14D0h	4	REG TGPIOPIV19_63:32 (TGPIO19_PIV_63_32)	00000000h
14D4h	4	REG TGPIOTCV19_31_0 (TGPIO19_TCV_31_0)	00000000h
14D8h	4	REG TGPIOTCV19_63_32 (TGPIO19_TCV_63_32)	00000000h
14DCh	4	REG TGPIOECCV19_31_0 (TGPIO19_ECCV_31_0)	00000000h
14E0h	4	REG TGPIOECCV19_63_32 (TGPIO19_ECCV_63_32)	00000000h
14E4h	4	REG TGPIOEC19_31_0 (TGPIO19_EC_31_0)	00000000h
14E8h	4	REG TGPIOEC19_63_32 (TGPIO19_EC_63_32)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
14ECh	4	REG TGPIOMATCHMASK19_31_0 (TGPIO19_MATCH_MASK_31_0)	00000000h
14F0h	4	REG TGPIOMATCHMASK19_63_32 (TGPIO19_MATCH_MASK_63_32)	00000000h
1500h	4	REG TGPIOINTRCTL (TGPIO_INTR_CTL_REG)	00000000h
1504h	4	REG TGPIORIS (TGPIO_INTR_RIS_REG)	00000000h
1508h	4	REG TGPIOMSC (TGPIO_INTR_MSC_REG)	00000000h
150Ch	4	REG TGPIOMIS (TGPIO_INTR_MIS_REG)	00000000h
1510h	4	REG TGPIOICR (TGPIO_INTR_ICR_REG)	00000000h
1514h	4	REG TGPIO_CLK_SEL_REG (TGPIO_CLK_SEL_REG)	00000000h
1518h	4	REG TGPIO_CLK_SEL_REG (TGPIO_XTAL_CG_REG)	00000000h
151Ch	4	Reg TGPIO_PTP_CG_REG (TGPIO_PTP_CG_REG)	00000000h
1520h	4	REG TGPIO_TS_SEL_0_REG (TGPIO_TS_SEL_0_REG)	00000000h
1524h	4	REG TGPIO_TS_SEL_1_REG (TGPIO_TS_SEL_1_REG)	00000000h
1528h	4	REG TMT_CLK_SEL_REG (TGPIO_TMT_CLK_SEL_REG)	00000000h
1530h	4	REG TGPIO_TSC_CTL_REG (TGPIO_CTS_ENABLE_REG)	00000000h
1534h	4	REG TGPIO_TSC_STATUS_REG (TGPIO_CTS_VALID_REG)	00000000h
1600h	4	REG TMTCTL_TSG (TMT_CTL_TSG_REG)	00000000h
1604h	4	REG TMTR_TSG (TMTR_TSG_REG)	00000000h
1608h	4	REG TMTL_TSG (TMTL_TSG_REG)	00000000h
160Ch	4	REG TMTH_TSG (TMTH_TSG_REG)	00000000h
1610h	4	REG TIMINCA_TSG (TMT_TIMINCA_TSG_REG)	00000000h
1614h	4	REG TIMADJ_TSG (TMT_TIMADJ_TSG_REG)	00000000h
1618h	4	REG LXTS_TMT_HIGH_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_1)	00000000h
161Ch	4	REG LXTS_TMT_LOW_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_0)	00000000h
1620h	4	REG LXTS_ART_HIGH_TSG (TMT_ART_SNAPSHOT_TSG_REG_1)	00000000h
1624h	4	REG LXTS_ART_LOW_TSG (TMT_ART_SNAPSHOT_TSG_REG_0)	00000000h
1628h	4	REG RXTS_TMT_HIGH_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_1)	00000000h
162Ch	4	REG RXTS_TMT_LOW_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_0)	00000000h
1640h	4	REG TMTCTL_GLOBAL (TMT_CTL_GLOBAL_REG)	00000000h
1644h	4	REG TMTR_GLOBAL (TMTR_GLOBAL_REG)	00000000h
1648h	4	REG TMTL_GLOBAL (TMTL_GLOBAL_REG)	00000000h
164Ch	4	REG TMTH_GLOBAL (TMTH_GLOBAL_REG)	00000000h
1650h	4	REG TIMINCA_GLOBAL (TMT_TIMINCA_GLOBAL_REG)	00000000h
1654h	4	REG TIMADJ_GLOBAL (TMT_TIMADJ_GLOBAL_REG)	00000000h
1658h	4	REG LXTS_TMT_LOW_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_0)	00000000h
165Ch	4	REG LXTS_TMT_HIGH_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_1)	00000000h
1660h	4	REG LXTS_ART_LOW_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_0)	00000000h

Table 10-2. Summary of Bus: 0, Device: 19, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1664h	4	REG LXTS_ART_HIGH_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_1)	00000000h
1668h	4	REG RXTS_TMT_LOW_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_0)	00000000h
166Ch	4	REG RXTS_TMT_HIGH_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_1)	00000000h
1680h	4	REG TMTCTL_WORKING (TMT_CTL_WORKING_REG)	00000000h
1684h	4	REG TMTR_WORKING (TMTR_WORKING_REG)	00000000h
1688h	4	REG TMTL_WORKING (TMTL_WORKING_REG)	00000000h
168Ch	4	REG TMTH_WORKING (TMTH_WORKING_REG)	00000000h
1690h	4	REG TIMINCA_WORKING (TMT_TIMINCA_WORKING_REG)	00000000h
1694h	4	REG TIMADJ_WORKING (TMT_TIMADJ_WORKING_REG)	00000000h
1698h	4	REG LXTS_TMT_LOW_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_0)	00000000h
169Ch	4	REG LXTS_TMT_HIGH_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_1)	00000000h
16A0h	4	REG LXTS_ART_LOW_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_0)	00000000h
16A4h	4	REG LXTS_ART_HIGH_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_1)	00000000h
16A8h	4	REG RXTS_TMT_LOW_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_0)	00000000h
16ACh	4	REG RXTS_TMT_HIGH_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_1)	00000000h
2000h	4	D0i3 Control (D0I3C)	00000008h
2004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

10.2.1 GPIO Pin DirectionLock (GCCR) - Offset 0h

Register to lock GPIO Pin direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**GPDR_LOCK:** This bit locks the GPDR register from being modified and is a write once bit which is cleared on a powergood assertion. This field is valid both when GPIO is input or output. 0 = GPDR is Unlocked 1 = GPDR is Locked.

10.2.2 GPIO Pin Level (GPLR0) - Offset 4h

Register for reading current value of GPIO pin. Valid when GPIO direction set as input.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GPLR0:** Check the state of each of the GPIO pins by reading the GPIO Pin Level register (GPLR). Each bit in the GPLR corresponds to one pin in the GPIO. GPLR0 31 to 0 correspond to GPIO 31 to 0. Use the GPLRx read-only registers to determine the current value of a particular pin (only available during GPIO input mode). For reserved bits, reads return zero.

10.2.3 GPIO Pin Level (GPLR1) - Offset 8h

Register for reading current value of GPIO pin. Valid when GPIO direction set as input.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GPLR1:** Check the state of each of the GPIO pins by reading the GPIO Pin Level register (GPLR). Each bit in the GPLR corresponds to one pin in the GPIO. GPLR0 31 to 0 correspond to GPIO 31 to 0. Use the GPLRx read-only registers to determine the current value of a particular pin (only available during GPIO input mode). For reserved bits, reads return zero.

10.2.4 GPIO Pin Direction (GPDR0) - Offset 1Ch

Register to set GPIO direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPDR0:** Setting whether a pin is an input or output is controlled by programming the GPIO pin direction registers (GPDR0-5). The GPDR registers contain one direction control bit for each of the 192 GPIO pins. If a direction bit is programmed to 1, the GPIO is an output. If it is programmed to 0, it is an input. A reset clears all bits in the GPDR0-5 registers and configures all GPIO pins as inputs.

10.2.5 GPIO Pin Direction (GPDR1) - Offset 20h

Register to set GPIO direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPDR1:** Setting whether a pin is an input or output is controlled by programming the GPIO pin direction registers (GPDR0-5). The GPDR registers contain one direction control bit for each of the 192 GPIO pins. If a direction bit is programmed to 1, the GPIO is an output. If it is programmed to 0, it is an input. A reset clears all bits in the GPDR0-5 registers and configures all GPIO pins as inputs.

10.2.6 GPIO Pin Output Set (GPSR0) - Offset 34h

Register to assert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPSR0:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin.

10.2.7 GPIO Pin Output Set (GPSR1) - Offset 38h

Register to assert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 38h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPSR1:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin.

10.2.8 GPIO Pin Output Clear (GPCR0) - Offset 4Ch

Register to deassert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPCR0:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin.

10.2.9 GPIO Pin Output Clear (GPCR1) - Offset 50h

Register to deassert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPCR1:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin.

10.2.10 GPIO Rising Edge Detect Enable (GRER0) - Offset 64h

Register to enable rising edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GRER0:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected.

10.2.11 GPIO Rising Edge Detect Enable (GRER1) - Offset 68h

Register to enable rising edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GRER1:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected.

10.2.12 GPIO Falling Edge Detect Enable (GFER0) - Offset 7Ch

Register to enable falling edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFER0:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected.

10.2.13 GPIO Falling Edge Detect Enable (GFER1) - Offset 80h

Register to enable falling edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFER1:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected.

10.2.14 GPIO Glitch Filter Bypass (GFBR0) - Offset 94h

Register to bypass Glitch filter for input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFBR0:** The GPIO Glitch Filter Bypass registers (GFBR0-5) contain a total of 192 bits that correspond to the 192 GPIO pins. When in general purpose mode, all GPIO pins go through the glitch filter logic by default. The glitch filter allows input signals that are stable for a certain number of clock cycles to propagate to the GPIO edge detection logic. Each GPIO pin can be individually configured to bypass this glitch filter.

10.2.15 GPIO Glitch Filter Bypass (GFBR1) - Offset 98h

Register to bypass Glitch filter for input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFBR1:** The GPIO Glitch Filter Bypass registers (GFBR0-5) contain a total of 192 bits that correspond to the 192 GPIO pins. When in general purpose mode, all GPIO pins go through the glitch filter logic by default. The glitch filter allows input signals that are stable for a certain number of clock cycles to propagate to the GPIO edge detection logic. Each GPIO pin can be individually configured to bypass this glitch filter.

10.2.16 GPIO Interrupt Mask (GIMR0) - Offset ACh

Register to mask interrupts for GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GIMR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.17 GPIO Interrupt Mask (GIMR1) - Offset B0h

Register to mask interrupts for GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GIMR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.18 GPIO Interrupt Source (GISR0) - Offset C4h

Register for interrupts status of GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GISR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.19 GPIO Interrupt Source (GISR1) - Offset C8h

Register for interrupts status of GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GISR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.20 GPIO Wake Mask (GWMR0) - Offset 100h

Register to mask wake from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GWMR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.21 GPIO Wake Mask (GWMR1) - Offset 104h

Register to mask wake from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GWMR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.22 GPIO Wake Source (GWSR0) - Offset 118h

Register for indicating wake source from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GWSR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.23 GPIO Wake Source (GWSR1) - Offset 11Ch

Register for indicating wake source from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GWSR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt.

10.2.24 GPIO Secure Input (GSEC) - Offset 130h

UNUSED FOR ISH.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GSEC:** 1 = Hide Pin Level Status Updates to GPLR and Mask Pin Interrupts to IO-APIC 0 = Unhidden.

10.2.25 REG TGPIOCTL0 (TGPIO0_CTL_REG) - Offset 1000h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO0_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO0_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO0_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 - reserved .
13	1h RW	**Freeze Input Timestamp (TGPIO0_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO0_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter
8:5	0h RW	**Pulse Width Stretch (TGPIO0_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles
4	0h RW	**Periodic Mode (PM) (TGPIO0_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled
3:2	0h RW	**Event Polarity (EP) (TGPIO0_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved
1	0h RW	**Direction (DIR) (TGPIO0_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO0_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled

10.2.26 REG TGPIOCOMPV0_31_0 (TGPIO0_COMPV_31_0) - Offset 1004h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO0_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register.

10.2.27 REG TGPIOCOMPV0_63_32 (TGPIO0_COMPV_63_32) - Offset 1008h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO0_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register.

10.2.28 REG TGPIOPIV0_31_0 (TGPIO0_PIV_31_0) - Offset 100Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.29 REG TGPIOPIV0_63:32 (TGPIO0_PIV_63_32) - Offset 1010h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.30 REG TGPIOTCV0_31_0 (TGPIO0_TCV_31_0) - Offset 1014h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1014h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.31 REG TGPIOTCV0_63_32 (TGPIO0_TCV_63_32) - Offset 1018h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1018h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.32 REG TGPIOECCV0_31_0 (TGPIO0_ECCV_31_0) - Offset 101Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 101Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.33 REG TGPIOECCV0_63_32 (TGPIO0_ECCV_63_32) - Offset 1020h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.34 REG TGPIOEC0_31_0 (TGPIO0_EC_31_0) - Offset 1024h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.35 REG TGPIOEC0_63_32 (TGPIO0_EC_63_32) - Offset 1028h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.36 REG TGPIOMATCHMASK0_31_0 (TGPIO0_MATCH_MASK_31_0) - Offset 102Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 102Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.37 REG TGPIOMATCHMASK0_63_32 (TGPIO0_MATCH_MASK_63_32) - Offset 1030h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1030h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.38 REG TGPIOCTL1 (TGPIO1_CTL_REG) - Offset 1040h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1040h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO1_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO1_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO1_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO1_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO1_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO1_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO1_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO1_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO1_CTL_DIR_O):** 0 Output 1 Input .
0	0h RW	**Enable (EN) (TGPIO1_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.39 REG TGPIOCOMPV1_31_0 (TGPIO1_COMPV_31_0) - Offset 1044h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1044h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO1_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register.

10.2.40 REG TGPIOCOMPV1_63_32 (TGPIO1_COMPV_63_32) - Offset 1048h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO1_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register.

10.2.41 REG TGPIOPIV1_31_0 (TGPIO1_PIV_31_0) - Offset 104Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 104Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.42 REG TGPIOPIV1_63:32 (TGPIO1_PIV_63_32) - Offset 1050h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.43 REG TGPIOTCV1_31_0 (TGPIO1_TCV_31_0) - Offset 1054h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.44 REG TGPIOTCV1_63_32 (TGPIO1_TCV_63_32) - Offset 1058h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.45 REG TGPIOECCV1_31_0 (TGPIO1_ECCV_31_0) - Offset 105Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 105Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.46 REG TGPIOECCV1_63_32 (TGPIO1_ECCV_63_32) - Offset 1060h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1060h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.47 REG TGPIOEC1_31_0 (TGPIO1_EC_31_0) - Offset 1064h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1064h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

10.2.48 REG TGPIOEC1_63_32 (TGPIO1_EC_63_32) - Offset 1068h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1068h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

10.2.49 REG TGPIOMATCHMASK1_31_0 (TGPIO1_MATCH_MASK_31_0) - Offset 106Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 106Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.50 REG TGPIOMATCHMASK1_63_32 (TGPIO1_MATCH_MASK_63_32) - Offset 1070h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1070h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.51 REG TGPIOCTL2 (TGPIO2_CTL_REG) - Offset 1080h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1080h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO2_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO2_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO2_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO2_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO2_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO2_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO2_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO2_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO2_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO2_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.52 REG TGPIOCOMPV2_31_0 (TGPIO2_COMPV_31_0) - Offset 1084h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1084h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO2_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register..

10.2.53 REG TGPIOCOMPV2_63_32 (TGPIO2_COMPV_63_32) - Offset 1088h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1088h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO2_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.54 REG TGPIOPIV2_31_0 (TGPIO2_PIV_31_0) - Offset 108Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 108Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.55 REG TGPIOPIV2_63:32 (TGPIO2_PIV_63_32) - Offset 1090h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1090h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.56 REG TGPIOTCV2_31_0 (TGPIO2_TCV_31_0) - Offset 1094h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1094h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.57 REG TGPIOTCV2_63_32 (TGPIO2_TCV_63_32) - Offset 1098h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1098h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.58 REG TGPIOECCV2_31_0 (TGPIO2_ECCV_31_0) - Offset 109Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 109Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.59 REG TGPIOECCV2_63_32 (TGPIO2_ECCV_63_32) - Offset 10A0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.60 REG TGPIOEC2_31_0 (TGPIO2_EC_31_0) - Offset 10A4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

10.2.61 REG TGPIOEC2_63_32 (TGPIO2_EC_63_32) - Offset 10A8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

10.2.62 REG TGPIOMATCHMASK2_31_0 (TGPIO2_MATCH_MASK_31_0) - Offset 10ACh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.63 REG TGPIOMATCHMASK2_63_32 (TGPIO2_MATCH_MASK_63_32) - Offset 10B0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.64 REG TGPIOCTL3 (TGPIO3_CTL_REG) - Offset 10C0h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C0h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO3_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO3_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO3_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO3_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO3_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO3_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO3_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO3_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO3_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO3_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.65 REG TGPIOCOMPV3_31_0 (TGPIO3_COMPV_31_0) - Offset 10C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO3_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.66 REG TGPIOCOMPV3_63_32 (TGPIO3_COMPV_63_32) - Offset 10C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO3_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.67 REG TGPIOPIV3_31_0 (TGPIO3_PIV_31_0) - Offset 10CCh

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.68 REG TGPIOPIV3_63:32 (TGPIO3_PIV_63_32) - Offset 10D0h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.69 REG TGPIOTCV3_31_0 (TGPIO3_TCV_31_0) - Offset 10D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.70 REG TGPIOTCV3_63_32 (TGPIO3_TCV_63_32) - Offset 10D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.71 REG TGPIOECCV3_31_0 (TGPIO3_ECCV_31_0) - Offset 10DCh

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.72 REG TGPIOECCV3_63_32 (TGPIO3_ECCV_63_32) - Offset 10E0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.73 REG TGPIOEC3_31_0 (TGPIO3_EC_31_0) - Offset 10E4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

10.2.74 REG TGPIOEC3_63_32 (TGPIO3_EC_63_32) - Offset 10E8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

10.2.75 REG TGPIOMATCHMASK3_31_0 (TGPIO3_MATCH_MASK_31_0) - Offset 10ECh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.76 REG TGPIOMATCHMASK3_63_32 (TGPIO3_MATCH_MASK_63_32) - Offset 10F0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.77 REG TGPIOCTL4 (TGPIO4_CTL_REG) - Offset 1100h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1100h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO4_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO4_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO4_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO4_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO4_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO4_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO4_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO4_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO4_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO4_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.78 REG TGPIOCOMPV4_31_0 (TGPIO4_COMPV_31_0) - Offset 1104h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1104h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO4_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.79 REG TGPIOCOMPV4_63_32 (TGPIO4_COMPV_63_32) - Offset 1108h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1108h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO4_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.80 REG TGPIOPIV4_31_0 (TGPIO4_PIV_31_0) - Offset 110Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.81 REG TGPIOPIV4_63:32 (TGPIO4_PIV_63_32) - Offset 1110h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1110h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.82 REG TGPIOTCV4_31_0 (TGPIO4_TCV_31_0) - Offset 1114h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1114h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.83 REG TGPIOTCV4_63_32 (TGPIO4_TCV_63_32) - Offset 1118h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1118h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.84 REG TGPIOECCV4_31_0 (TGPIO4_ECCV_31_0) - Offset 111Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 111Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.85 REG TGPIOECCV4_63_32 (TGPIO4_ECCV_63_32) - Offset 1120h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1120h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.86 REG TGPIOEC4_31_0 (TGPIO4_EC_31_0) - Offset 1124h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1124h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.87 REG TGPIOEC4_63_32 (TGPIO4_EC_63_32) - Offset 1128h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1128h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.88 REG TGPIOMATCHMASK4_31_0 (TGPIO4_MATCH_MASK_31_0) - Offset 112Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 112Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.89 REG TGPIOMATCHMASK4_63_32 (TGPIO4_MATCH_MASK_63_32) - Offset 1130h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1130h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.90 REG TGPIOCTL5 (TGPIO5_CTL_REG) - Offset 1140h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1140h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO5_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO5_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO5_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO5_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO5_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO5_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO5_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO5_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO5_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO5_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.91 REG TGPIOCOMPV5_31_0 (TGPIO5_COMPV_31_0) - Offset 1144h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1144h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO5_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.92 REG TGPIOCOMPV5_63_32 (TGPIO5_COMPV_63_32) - Offset 1148h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1148h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO5_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.93 REG TGPIOPIV5_31_0 (TGPIO5_PIV_31_0) - Offset 114Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.94 REG TGPIOPIV5_63:32 (TGPIO5_PIV_63_32) - Offset 1150h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1150h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.95 REG TGPIOTCV5_31_0 (TGPIO5_TCV_31_0) - Offset 1154h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1154h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.96 REG TGPIOTCV5_63_32 (TGPIO5_TCV_63_32) - Offset 1158h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1158h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.97 REG TGPIOECCV5_31_0 (TGPIO5_ECCV_31_0) - Offset 115Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 115Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.98 REG TGPIOECCV5_63_32 (TGPIO5_ECCV_63_32) - Offset 1160h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1160h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.99 REG TGPIOEC5_31_0 (TGPIO5_EC_31_0) - Offset 1164h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1164h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.100 REG TGPIOEC5_63_32 (TGPIO5_EC_63_32) - Offset 1168h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1168h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.101 REG TGPIOMATCHMASK5_31_0 (TGPIO5_MATCH_MASK_31_0) - Offset 116Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 116Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.102 REG TGPIOMATCHMASK5_63_32 (TGPIO5_MATCH_MASK_63_32) - Offset 1170h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1170h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.103 REG TGPIOCTL6 (TGPIO6_CTL_REG) - Offset 1180h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1180h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO6_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO6_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO6_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO6_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO6_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO6_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO6_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO6_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO6_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO6_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.104 REG TGPIOCOMPV6_31_0 (TGPIO6_COMPV_31_0) - Offset 1184h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1184h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO6_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.105 REG TGPIOCOMPV6_63_32 (TGPIO6_COMPV_63_32) - Offset 1188h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1188h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO6_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.106 REG TGPIOPIV6_31_0 (TGPIO6_PIV_31_0) - Offset 118Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 118Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.107 REG TGPIOPIV6_63:32 (TGPIO6_PIV_63_32) - Offset 1190h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1190h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.108 REG TGPIOTCV6_31_0 (TGPIO6_TCV_31_0) - Offset 1194h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1194h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.109 REG TGPIOTCV6_63_32 (TGPIO6_TCV_63_32) - Offset 1198h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1198h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.110 REG TGPIOECCV6_31_0 (TGPIO6_ECCV_31_0) - Offset 119Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 119Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.111 REG TGPIOECCV6_63_32 (TGPIO6_ECCV_63_32) - Offset 11A0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.112 REG TGPIOEC6_31_0 (TGPIO6_EC_31_0) - Offset 11A4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.113 REG TGPIOEC6_63_32 (TGPIO6_EC_63_32) - Offset 11A8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.114 REG TGPIOMATCHMASK6_31_0 (TGPIO6_MATCH_MASK_31_0) - Offset 11ACh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.115 REG TGPIOMATCHMASK6_63_32 (TGPIO6_MATCH_MASK_63_32) - Offset 11B0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.116 REG TGPIOCTL7 (TGPIO7_CTL_REG) - Offset 11C0h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C0h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO7_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO7_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO7_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO7_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO7_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO7_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO7_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO7_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO7_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO7_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.117 REG TGPIOCOMPV7_31_0 (TGPIO7_COMPV_31_0) - Offset 11C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO7_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.118 REG TGPIOCOMPV7_63_32 (TGPIO7_COMPV_63_32) - Offset 11C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO7_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.119 REG TGPIOPIV7_31_0 (TGPIO7_PIV_31_0) - Offset 11CCh

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.120 REG TGPIOPIV7_63:32 (TGPIO7_PIV_63_32) - Offset 11D0h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.121 REG TGPIOTCV7_31_0 (TGPIO7_TCV_31_0) - Offset 11D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.122 REG TGPIOTCV7_63_32 (TGPIO7_TCV_63_32) - Offset 11D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.123 REG TGPIOECCV7_31_0 (TGPIO7_ECCV_31_0) - Offset 11DCh

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.124 REG TGPIOECCV7_63_32 (TGPIO7_ECCV_63_32) - Offset 11E0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.125 REG TGPIOEC7_31_0 (TGPIO7_EC_31_0) - Offset 11E4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.126 REG TGPIOEC7_63_32 (TGPIO7_EC_63_32) - Offset 11E8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.127 REG TGPIOMATCHMASK7_31_0 (TGPIO7_MATCH_MASK_31_0) - Offset 11ECh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.128 REG TGPIOMATCHMASK7_63_32 (TGPIO7_MATCH_MASK_63_32) - Offset 11F0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.129 REG TGPIOCTL8 (TGPIO8_CTL_REG) - Offset 1200h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1200h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO8_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO8_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO8_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO8_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO8_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO8_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO8_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO8_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO8_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO8_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.130 REG TGPIOCOMPV8_31_0 (TGPIO8_COMPV_31_0) - Offset 1204h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1204h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO8_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register.

10.2.131 REG TGPIOCOMPV8_63_32 (TGPIO8_COMPV_63_32) - Offset 1208h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1208h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO8_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.132 REG TGPIOPIV8_31_0 (TGPIO8_PIV_31_0) - Offset 120Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.133 REG TGPIOPIV8_63:32 (TGPIO8_PIV_63_32) - Offset 1210h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1210h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.134 REG TGPIOTCV8_31_0 (TGPIO8_TCV_31_0) - Offset 1214h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1214h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.135 REG TGPIOTCV8_63_32 (TGPIO8_TCV_63_32) - Offset 1218h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1218h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.136 REG TGPIOECCV8_31_0 (TGPIO8_ECCV_31_0) - Offset 121Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 121Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.137 REG TGPIOECCV8_63_32 (TGPIO8_ECCV_63_32) - Offset 1220h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1220h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.138 REG TGPIOEC8_31_0 (TGPIO8_EC_31_0) - Offset 1224h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1224h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.139 REG TGPIOEC8_63_32 (TGPIO8_EC_63_32) - Offset 1228h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1228h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.140 REG TGPIOMATCHMASK8_31_0 (TGPIO8_MATCH_MASK_31_0) - Offset 122Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 122Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.141 REG TGPIOMATCHMASK8_63_32 (TGPIO8_MATCH_MASK_63_32) - Offset 1230h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1230h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.142 REG TGPIOCTL9 (TGPIO9_CTL_REG) - Offset 1240h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1240h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO9_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO9_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO9_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO9_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO9_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO9_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO9_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO9_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO9_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO9_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.143 REG TGPIOCOMPV9_31_0 (TGPIO9_COMPV_31_0) - Offset 1244h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO9_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.144 REG TGPIOCOMPV9_63_32 (TGPIO9_COMPV_63_32) - Offset 1248h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1248h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO9_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.145 REG TGPIOPIV9_31_0 (TGPIO9_PIV_31_0) - Offset 124Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.146 REG TGPIOPIV9_63:32 (TGPIO9_PIV_63_32) - Offset 1250h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1250h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.147 REG TGPIOTCV9_31_0 (TGPIO9_TCV_31_0) - Offset 1254h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1254h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.148 REG TGPIOTCV9_63_32 (TGPIO9_TCV_63_32) - Offset 1258h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1258h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.149 REG TGPIOECCV9_31_0 (TGPIO9_ECCV_31_0) - Offset 125Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 125Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.150 REG TGPIOECCV9_63_32 (TGPIO9_ECCV_63_32) - Offset 1260h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1260h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.151 REG TGPIOEC9_31_0 (TGPIO9_EC_31_0) - Offset 1264h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1264h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.152 REG TGPIOEC9_63_32 (TGPIO9_EC_63_32) - Offset 1268h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1268h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.153 REG TGPIOMATCHMASK9_31_0 (TGPIO9_MATCH_MASK_31_0) - Offset 126Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 126Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.154 REG TGPIOMATCHMASK9_63_32 (TGPIO9_MATCH_MASK_63_32) - Offset 1270h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1270h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.155 REG TGPIOCTL10 (TGPIO10_CTL_REG) - Offset 1280h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1280h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO10_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO10_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO10_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO10_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO10_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO10_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO10_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO10_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO10_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO10_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.156 REG TGPIOCOMPV10_31_0 (TGPIO10_COMPV_31_0) - Offset 1284h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1284h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO10_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.157 REG TGPIOCOMPV10_63_32 (TGPIO10_COMPV_63_32) - Offset 1288h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1288h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO10_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.158 REG TGPIOPIV10_31_0 (TGPIO10_PIV_31_0) - Offset 128Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.159 REG TGPIOPIV10_63:32 (TGPIO10_PIV_63_32) - Offset 1290h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1290h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.160 REG TGPIOTCV10_31_0 (TGPIO10_TCV_31_0) - Offset 1294h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1294h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.161 REG TGPIOTCV10_63_32 (TGPIO10_TCV_63_32) - Offset 1298h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1298h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.162 REG TGPIOECCV10_31_0 (TGPIO10_ECCV_31_0) - Offset 129Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 129Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.163 REG TGPIOECCV10_63_32 (TGPIO10_ECCV_63_32) - Offset 12A0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.164 REG TGPIOEC10_31_0 (TGPIO10_EC_31_0) - Offset 12A4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.165 REG TGPIOEC10_63_32 (TGPIO10_EC_63_32) - Offset 12A8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.166 REG TGPIOMATCHMASK10_31_0 (TGPIO10_MATCH_MASK_31_0) - Offset 12ACh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.167 REG TGPIOMATCHMASK10_63_32 (TGPIO10_MATCH_MASK_63_32) - Offset 12B0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.168 REG TGPIOCTL11 (TGPIO11_CTL_REG) - Offset 12C0h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12C0h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO11_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO11_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO11_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO11_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO11_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO11_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO11_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO11_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO11_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO11_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.169 REG TGPIOCOMPV11_31_0 (TGPIO11_COMPV_31_0) - Offset 12C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO11_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.170 REG TGPIOCOMPV11_63_32 (TGPIO11_COMPV_63_32) - Offset 12C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO11_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.171 REG TGPIOPIV11_31_0 (TGPIO11_PIV_31_0) - Offset 12CCh

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.172 REG TGPIOPIV11_63:32 (TGPIO11_PIV_63_32) - Offset 12D0h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.173 REG TGPIOTCV11_31_0 (TGPIO11_TCV_31_0) - Offset 12D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.174 REG TGPIOTCV11_63_32 (TGPIO11_TCV_63_32) - Offset 12D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.175 REG TGPIOECCV11_31_0 (TGPIO11_ECCV_31_0) - Offset 12DCh

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.176 REG TGPIOECCV11_63_32 (TGPIO11_ECCV_63_32) - Offset 12E0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.177 REG TGPIOEC11_31_0 (TGPIO11_EC_31_0) - Offset 12E4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.178 REG TGPIOEC11_63_32 (TGPIO11_EC_63_32) - Offset 12E8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.179 REG TGPIOMATCHMASK11_31_0 (TGPIO11_MATCH_MASK_31_0) - Offset 12ECh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.180 REG TGPIOMATCHMASK11_63_32 (TGPIO11_MATCH_MASK_63_32) - Offset 12F0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 12F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.181 REG TGPIOCTL12 (TGPIO12_CTL_REG) - Offset 1300h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1300h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO12_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO12_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO12_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO12_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO12_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO12_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO12_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO12_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO12_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO12_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.182 REG TGPIOCOMPV12_31_0 (TGPIO12_COMPV_31_0) - Offset 1304h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1304h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO12_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.183 REG TGPIOCOMPV12_63_32 (TGPIO12_COMPV_63_32) - Offset 1308h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1308h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO12_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.184 REG TGPIOPIV12_31_0 (TGPIO12_PIV_31_0) - Offset 130Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 130Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.185 REG TGPIOPIV12_63:32 (TGPIO12_PIV_63_32) - Offset 1310h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1310h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.186 REG TGPIOTCV12_31_0 (TGPIO12_TCV_31_0) - Offset 1314h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1314h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.187 REG TGPIOTCV12_63_32 (TGPIO12_TCV_63_32) - Offset 1318h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1318h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.188 REG TGPIOECCV12_31_0 (TGPIO12_ECCV_31_0) - Offset 131Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 131Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.189 REG TGPIOECCV12_63_32 (TGPIO12_ECCV_63_32) - Offset 1320h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1320h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.190 REG TGPIOEC12_31_0 (TGPIO12_EC_31_0) - Offset 1324h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1324h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.191 REG TGPIOEC12_63_32 (TGPIO12_EC_63_32) - Offset 1328h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1328h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.192 REG TGPIOMATCHMASK12_31_0 (TGPIO12_MATCH_MASK_31_0) - Offset 132Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 132Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.193 REG TGPIOMATCHMASK12_63_32 (TGPIO12_MATCH_MASK_63_32) - Offset 1330h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1330h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.194 REG TGPIOCTL13 (TGPIO13_CTL_REG) - Offset 1340h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1340h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO13_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO13_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO13_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO13_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO13_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO13_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO13_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO13_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO13_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO13_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.195 REG TGPIOCOMPV13_31_0 (TGPIO13_COMPV_31_0) - Offset 1344h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1344h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO13_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.196 REG TGPIOCOMPV13_63_32 (TGPIO13_COMPV_63_32) - Offset 1348h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1348h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO13_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.197 REG TGPIOPIV13_31_0 (TGPIO13_PIV_31_0) - Offset 134Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 134Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.198 REG TGPIOPIV13_63:32 (TGPIO13_PIV_63_32) - Offset 1350h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1350h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.199 REG TGPIOTCV13_31_0 (TGPIO13_TCV_31_0) - Offset 1354h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1354h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.200 REG TGPIOTCV13_63_32 (TGPIO13_TCV_63_32) - Offset 1358h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1358h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.201 REG TGPIOECCV13_31_0 (TGPIO13_ECCV_31_0) - Offset 135Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 135Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.202 REG TGPIOECCV13_63_32 (TGPIO13_ECCV_63_32) - Offset 1360h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1360h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.203 REG TGPIOEC13_31_0 (TGPIO13_EC_31_0) - Offset 1364h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1364h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.204 REG TGPIOEC13_63_32 (TGPIO13_EC_63_32) - Offset 1368h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1368h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.205 REG TGPIOMATCHMASK13_31_0 (TGPIO13_MATCH_MASK_31_0) - Offset 136Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 136Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.206 REG TGPIOMATCHMASK13_63_32 (TGPIO13_MATCH_MASK_63_32) - Offset 1370h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1370h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.207 REG TGPIOCTL14 (TGPIO14_CTL_REG) - Offset 1380h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1380h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO14_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO14_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO14_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO14_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO14_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO14_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO14_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO14_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO14_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO14_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.208 REG TGPIOCOMPV14_31_0 (TGPIO14_COMPV_31_0) - Offset 1384h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1384h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO14_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.209 REG TGPIOCOMPV14_63_32 (TGPIO14_COMPV_63_32) - Offset 1388h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1388h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO14_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.210 REG TGPIOPIV14_31_0 (TGPIO14_PIV_31_0) - Offset 138Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 138Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.211 REG TGPIOPIV14_63:32 (TGPIO14_PIV_63_32) - Offset 1390h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1390h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.212 REG TGPIOTCV14_31_0 (TGPIO14_TCV_31_0) - Offset 1394h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1394h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.213 REG TGPIOTCV14_63_32 (TGPIO14_TCV_63_32) - Offset 1398h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1398h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.214 REG TGPIOECCV14_31_0 (TGPIO14_ECCV_31_0) - Offset 139Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 139Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.215 REG TGPIOECCV14_63_32 (TGPIO14_ECCV_63_32) - Offset 13A0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.216 REG TGPIOEC14_31_0 (TGPIO14_EC_31_0) - Offset 13A4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.217 REG TGPIOEC14_63_32 (TGPIO14_EC_63_32) - Offset 13A8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.218 REG TGPIOMATCHMASK14_31_0 (TGPIO14_MATCH_MASK_31_0) - Offset 13ACh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.219 REG TGPIOMATCHMASK14_63_32 (TGPIO14_MATCH_MASK_63_32) - Offset 13B0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.220 REG TGPIOCTL15 (TGPIO15_CTL_REG) - Offset 13C0h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13C0h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO15_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO15_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO15_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO15_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO15_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO15_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO15_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO15_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO15_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO15_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.221 REG TGPIOCOMPV15_31_0 (TGPIO15_COMPV_31_0) - Offset 13C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO15_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.222 REG TGPIOCOMPV15_63_32 (TGPIO15_COMPV_63_32) - Offset 13C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO15_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.223 REG TGPIOPIV15_31_0 (TGPIO15_PIV_31_0) - Offset 13CCh

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.224 REG TGPIOPIV15_63:32 (TGPIO15_PIV_63_32) - Offset 13D0h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.225 REG TGPIOTCV15_31_0 (TGPIO15_TCV_31_0) - Offset 13D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.226 REG TGPIOTCV15_63_32 (TGPIO15_TCV_63_32) - Offset 13D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.227 REG TGPIOECCV15_31_0 (TGPIO15_ECCV_31_0) - Offset 13DCh

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.228 REG TGPIOECCV15_63_32 (TGPIO15_ECCV_63_32) - Offset 13E0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.229 REG TGPIOEC15_31_0 (TGPIO15_EC_31_0) - Offset 13E4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.230 REG TGPIOEC15_63_32 (TGPIO15_EC_63_32) - Offset 13E8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.231 REG TGPIOMATCHMASK15_31_0 (TGPIO15_MATCH_MASK_31_0) - Offset 13ECh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.232 REG TGPIOMATCHMASK15_63_32 (TGPIO15_MATCH_MASK_63_32) - Offset 13F0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 13F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.233 REG TGPIOCTL16 (TGPIO16_CTL_REG) - Offset 1400h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1400h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO16_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO16_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO16_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO16_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO16_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO16_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO16_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO16_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO16_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO16_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.234 REG TGPIOCOMPV16_31_0 (TGPIO16_COMPV_31_0) - Offset 1404h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1404h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO16_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.235 REG TGPIOCOMPV16_63_32 (TGPIO16_COMPV_63_32) - Offset 1408h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1408h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO16_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.236 REG TGPIOPIV16_31_0 (TGPIO16_PIV_31_0) - Offset 140Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.237 REG TGPIOPIV16_63:32 (TGPIO16_PIV_63_32) - Offset 1410h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1410h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.238 REG TGPIOTCV16_31_0 (TGPIO16_TCV_31_0) - Offset 1414h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1414h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.239 REG TGPIOTCV16_63_32 (TGPIO16_TCV_63_32) - Offset 1418h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1418h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.240 REG TGPIOECCV16_31_0 (TGPIO16_ECCV_31_0) - Offset 141Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 141Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.241 REG TGPIOECCV16_63_32 (TGPIO16_ECCV_63_32) - Offset 1420h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1420h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.242 REG TGPIOEC16_31_0 (TGPIO16_EC_31_0) - Offset 1424h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1424h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.243 REG TGPIOEC16_63_32 (TGPIO16_EC_63_32) - Offset 1428h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1428h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.244 REG TGPIOMATCHMASK16_31_0 (TGPIO16_MATCH_MASK_31_0) - Offset 142Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 142Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.245 REG TGPIOMATCHMASK16_63_32 (TGPIO16_MATCH_MASK_63_32) - Offset 1430h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1430h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.246 REG TGPIOCTL17 (TGPIO17_CTL_REG) - Offset 1440h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1440h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO17_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO17_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO17_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO17_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO17_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO17_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO17_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO17_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO17_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO17_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.247 REG TGPIOCOMPV17_31_0 (TGPIO17_COMPV_31_0) - Offset 1444h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1444h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO17_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.248 REG TGPIOCOMPV17_63_32 (TGPIO17_COMPV_63_32) - Offset 1448h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1448h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO17_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.249 REG TGPIOPIV17_31_0 (TGPIO17_PIV_31_0) - Offset 144Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.250 REG TGPIOPIV17_63:32 (TGPIO17_PIV_63_32) - Offset 1450h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1450h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.251 REG TGPIOTCV17_31_0 (TGPIO17_TCV_31_0) - Offset 1454h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1454h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.252 REG TGPIOTCV17_63_32 (TGPIO17_TCV_63_32) - Offset 1458h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1458h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.253 REG TGPIOECCV17_31_0 (TGPIO17_ECCV_31_0) - Offset 145Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 145Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.254 REG TGPIOECCV17_63_32 (TGPIO17_ECCV_63_32) - Offset 1460h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1460h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.255 REG TGPIOEC17_31_0 (TGPIO17_EC_31_0) - Offset 1464h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1464h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.256 REG TGPIOEC17_63_32 (TGPIO17_EC_63_32) - Offset 1468h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1468h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.257 REG TGPIOMATCHMASK17_31_0 (TGPIO17_MATCH_MASK_31_0) - Offset 146Ch

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 146Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.258 REG TGPIOMATCHMASK17_63_32 (TGPIO17_MATCH_MASK_63_32) - Offset 1470h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1470h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.259 REG TGPIOCTL18 (TGPIO18_CTL_REG) - Offset 1480h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1480h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO18_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO18_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO18_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO18_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO18_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO18_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO18_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO18_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO18_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO18_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.260 REG TGPIOCOMPV18_31_0 (TGPIO18_COMPV_31_0) - Offset 1484h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1484h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO18_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.261 REG TGPIOCOMPV18_63_32 (TGPIO18_COMPV_63_32) - Offset 1488h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1488h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO18_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.262 REG TGPIOPIV18_31_0 (TGPIO18_PIV_31_0) - Offset 148Ch

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.263 REG TGPIOPIV18_63:32 (TGPIO18_PIV_63_32) - Offset 1490h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1490h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.264 REG TGPIOTCV18_31_0 (TGPIO18_TCV_31_0) - Offset 1494h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1494h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.265 REG TGPIOTCV18_63_32 (TGPIO18_TCV_63_32) - Offset 1498h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1498h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.266 REG TGPIOECCV18_31_0 (TGPIO18_ECCV_31_0) - Offset 149Ch

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 149Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.267 REG TGPIOECCV18_63_32 (TGPIO18_ECCV_63_32) - Offset 14A0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.268 REG TGPIOEC18_31_0 (TGPIO18_EC_31_0) - Offset 14A4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.269 REG TGPIOEC18_63_32 (TGPIO18_EC_63_32) - Offset 14A8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.270 REG TGPIOMATCHMASK18_31_0 (TGPIO18_MATCH_MASK_31_0) - Offset 14ACh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.271 REG TGPIOMATCHMASK18_63_32 (TGPIO18_MATCH_MASK_63_32) - Offset 14B0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.272 REG TGPIOCTL19 (TGPIO19_CTL_REG) - Offset 14C0h

TGPIO Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14C0h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO19_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO19_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO19_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO19_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO19_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO19_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO19_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO19_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO19_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO19_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

10.2.273 REG TGPIOCOMPV19_31_0 (TGPIO19_COMPV_31_0) - Offset 14C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO19_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.274 REG TGPIOCOMPV19_63_32 (TGPIO19_COMPV_63_32) - Offset 14C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO19_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

10.2.275 REG TGPIOPIV19_31_0 (TGPIO19_PIV_31_0) - Offset 14CCh

Periodic Interval Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.276 REG TGPIOPIV19_63:32 (TGPIO19_PIV_63_32) - Offset 14D0h

Periodic Interval Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

10.2.277 REG TGPIOTCV19_31_0 (TGPIO19_TCV_31_0) - Offset 14D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.278 REG TGPIOTCV19_63_32 (TGPIO19_TCV_63_32) - Offset 14D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

10.2.279 REG TGPIOECCV19_31_0 (TGPIO19_ECCV_31_0) - Offset 14DCh

Event Counter Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.280 REG TGPIOECCV19_63_32 (TGPIO19_ECCV_63_32) - Offset 14E0h

Event Counter Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

10.2.281 REG TGPIOEC19_31_0 (TGPIO19_EC_31_0) - Offset 14E4h

Event Counter Value 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.282 REG TGPIOEC19_63_32 (TGPIO19_EC_63_32) - Offset 14E8h

Event Counter Value 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

10.2.283 REG TGPIOMATCHMASK19_31_0 (TGPIO19_MATCH_MASK_31_0) - Offset 14ECh

Comparator Mask Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.284 REG TGPIOMATCHMASK19_63_32 (TGPIO19_MATCH_MASK_63_32) - Offset 14F0h

Comparator Mask Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

10.2.285 REG TGPIOINTRCTL (TGPIO_INTR_CTL_REG) - Offset 1500h

Interrupt Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1500h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Disable Interrupt Coalescing (TGPIO_INTR_COALESCE_DISABLE):** When set will prevent coalescing of interrupts. The default is to enable interrupt coalescing.

10.2.286 REG TGPIORIS (TGPIO_INTR_RIS_REG) - Offset 1504h

Raw Interrupt Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1504h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_GLOBAL:** Set when the TMT GLOBAL nanosecond counter wraps which is about every 1s.
24	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_WORKING:** Set when the TMT WORKING nanosecond counter wraps which is about every 1s.
23	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_TSG:** Set when the TMT TSG nanosecond counter wraps which is about every 1s.
22	0h RO	**Time Adjust Complete TADJ_TMT_GLOBAL_CMPLT (TGPIO_RIS_TADJ_TMT_GLOBAL_CMPLT):** 0-No Interrupt 1-Interrupt.
21	0h RO	**Time Adjust Complete TADJ_TMT_WORKING_CMPLT (TGPIO_RIS_TADJ_TMT_WORKING_CMPLT):** 0-No Interrupt 1-Interrupt.
20	0h RO	**Time Adjust Complete TADJ_TMT_TSG_CMPLT (TGPIO_RIS_TADJ_TMT_TSG_CMPLT):** 0-No Interrupt 1-Interrupt.
19:0	00000h RO	**Event Interrupt (TGPIO_RIS_EVENT_INTR):** 0-No Interrupt 1-Interrupt Pending.

10.2.287 REG TGPIOMSC (TGPIO_INTR_MSC_REG) - Offset 1508h

Interrupt Mask Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1508h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_GLOBAL_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
24	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_WORKING_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
23	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_TSG_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
22	0h RW	**Time Adjust Complete Enable TADJ_TMT_GLOBAL_EN (TGPIO_MSC_TADJ_TMT_GLOBAL_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
21	0h RW	**Time Adjust Complete Enable TADJ_TMT_WORKING_EN (TGPIO_MSC_TADJ_TMT_WORKING_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
20	0h RW	**Time Adjust Complete Enable TADJ_TMT_TSG_EN (TGPIO_MSC_TADJ_TMT_TSG_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
19:0	00000h RW	**Event Interrupt (TGPIO_MSC_EVENT_INTR):** 0-Interrupt Disabled 1-Interrupt Enabled.

10.2.288 REG TGPIOMIS (TGPIO_INTR_MIS_REG) - Offset 150Ch

Masked Interrupt Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 150Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_GLOBAL:** 0- No Interrupt 1-Interrupt.
24	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_WORKING:** 0- No Interrupt 1-Interrupt.
23	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_TSG:** 0- No Interrupt 1-Interrupt.
22	0h RO	**Time Adjust Complete TADJ_TMT_GLOBAL_CMPLT (TGPIO_MIS_TADJ_TMT_GLOBAL):** 0- No Interrupt 1-Interrupt.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**Time Adjust Complete TADJ_TMT_WORKING_CMPLT (TGPIO_MIS_TADJ_TMT_WORKING):** 0- No Interrupt 1-Interrupt.
20	0h RO	**Time Adjust Complete TADJ_TMT_TSG_CMPLT (TGPIO_MIS_TADJ_TMT_TSG):** 0- No Interrupt 1-Interrupt.
19:0	00000h RO	**Event Interrupt (TGPIO_MIS_EVENT_INTR):** 1-No Interrupt 2-Interrupt Pending.

10.2.289 REG TGPIOICR (TGPIO_INTR_ICR_REG) - Offset 1510h

Interrupt Clear Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1510h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_GLOBAL:** 0 No change 1-Clear Interrupt Request.
24	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_WORKING:** 0 No change 1-Clear Interrupt Request.
23	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_TSG:** 0 No change 1-Clear Interrupt Request.
22	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_GLOBAL_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_GLOBAL):** 0 No change 1-Clear Interrupt Request.
21	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_WORKING_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_WORKING):** 0 No change 1-Clear Interrupt Request.
20	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_TSG_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_TSG):** 0 No change 1-Clear Interrupt Request.
19:0	00000h WO	**Clear Event Interrupt [19:0] (TGPIO_ICR_CLR_EVENT_INTR):** 0 No change 1-Clear Interrupt Request.

10.2.290 REG TGPIO_CLK_SEL_REG (TGPIO_CLK_SEL_REG) - Offset 1514h

Timed GPIO Clock Select Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1514h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:0	00000h RW	**Clock Select (TGPIO_CLK_SEL_REG):** Timed GPIO clock select register.

10.2.291 REG TGPIO_CLK_SEL_REG (TGPIO_XTAL_CG_REG) - Offset 1518h

Timed GPIO XTAL Clock Gate Enable Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1518h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TGPIO_XTL_CG_REG:** This clock needs to be gated before writing to the clk_sel register.

10.2.292 Reg TGPIO_PTP_CG_REG (TGPIO_PTP_CG_REG) - Offset 151Ch

Timed GPIO PTP Clock Gate Enable Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 151Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TGPIO_PPT_CG_REG:** This clock needs to be gated before writing to the clk_sel register.

10.2.293 REG TGPIO_TS_SEL_0_REG (TGPIO_TS_SEL_0_REG) - Offset 1520h

TGPIO Input Timestamp Select Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1520h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Select 0 (TGPIO_TS_SEL_0_REG):** TGPIO input timestamp select register 0.

10.2.294 REG TGPIO_TS_SEL_1_REG (TGPIO_TS_SEL_1_REG) - Offset 1524h

TGPIO Input Timestamp Select Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1524h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Timestamp Select 1 (TGPIO_TS_SEL_1_REG):** TGPIO input timestamp select register 1.

10.2.295 REG TMT_CLK_SEL_REG (TGPIO_TMT_CLK_SEL_REG) - Offset 1528h

TMT Clock Select Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1528h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**TMT Clock Select (TGPIO_TMT_CLK_SEL_REG):** TMT clock select register.

10.2.296 REG TGPIO_TSC_CTL_REG (TGPIO_CTS_ENABLE_REG) - Offset 1530h

TGPIO Cross Timestamp Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1530h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW	**TMT CTS En 2 (TMT_CTS_ENABLE_REG_2):** TMT Cross Time Stamp Control [2].
3:2	0h RW	**TMT CTS En 1 (TMT_CTS_ENABLE_REG_1):** TMT Cross Time Stamp Control [1].
1:0	0h RW	**TMT CTS En 0 (TMT_CTS_ENABLE_REG_0):** TMT Cross Time Stamp Control [0].

10.2.297 REG TGPIO_TSC_STATUS_REG (TGPIO_CTS_VALID_REG) - Offset 1534h

TGPIO Cross Timestamp Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1534h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RO	**TMT CTS STATUS 2 (TMT_CTS_VALID_REG_2):** TMT Cross Time Stamp Status [2].
3:2	0h RO	**TMT CTS STATUS 1 (TMT_CTS_VALID_REG_1):** TMT Cross Time Stamp Status [1].
1:0	0h RO	**TMT CTS STATUS 0 (TMT_CTS_VALID_REG_0):** TMT Cross Time Stamp Status [0].

10.2.298 REG TMTCTL_TSG (TMT_CTL_TSG_REG) - Offset 1600h

TMT Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1600h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_TSG_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

10.2.299 REG TMTR_TSG (TMTR_TSG_REG) - Offset 1604h

TMT Timestamp Residue Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1604h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_TSG_REG:** TMT residue value defined with a resolution of 2^-32ns.

10.2.300 REG TMTL_TSG (TMTL_TSG_REG) - Offset 1608h

TMT Timestamp Low Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1608h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_TSG_REG:** Lower Half of the TMT defined in ns..

10.2.301 REG TMTH_TSG (TMTH_TSG_REG) - Offset 160Ch

TMT Timestamp High Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 160Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_TSG_REG:** Upper Half of the TMT defined in ns.

10.2.302 REG TIMINCA_TSG (TMT_TIMINCA_TSG_REG) - Offset 1610h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1610h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_TSG_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_TSG_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

10.2.303 REG TIMADJ_TSG (TMT_TIMADJ_TSG_REG) - Offset 1614h

TMT Time Offset Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1614h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_TSG_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_TSG_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_TSG_TIMADJ_TADJUS:** Time Adjust Value.

10.2.304 REG LXTS_TMT_HIGH_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_1) - Offset 1618h

TMT Local Cross Timestamp Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1618h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_TSG_REG:** TMTH captured when a local cross time stamp capture is enabled.

10.2.305 REG LXTS_TMT_LOW_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_0) - Offset 161Ch

TMT Local Cross Timestamp Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 161Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_TSG_REG:** TMTL captured when a local cross time stamp capture is enabled.

10.2.306 REG LXTS_ART_HIGH_TSG (TMT_ART_SNAPSHOT_TSG_REG_1) - Offset 1620h

TMT Local Cross Timestamp ART Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1620h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_TSG_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

10.2.307 REG LXTS_ART_LOW_TSG (TMT_ART_SNAPSHOT_TSG_REG_0) - Offset 1624h

TMT Local Cross Timestamp ART Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1624h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_TSG_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

10.2.308 REG RXTS_TMT_HIGH_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_1) - Offset 1628h

TMT Remote Cross Timestamp Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1628h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_TSG_REG:** TMTH captured when a remote time stamp capture is enabled.

10.2.309 REG RXTS_TMT_LOW_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_0) - Offset 162Ch

TMT Remote Cross Timestamp Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 162Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_TSG_REG:** TMTL captured when a remote time stamp capture is enabled.

10.2.310 REG TMTCTL_GLOBAL (TMT_CTL_GLOBAL_REG) - Offset 1640h

TMT Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1640h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_GLOBAL_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

10.2.311 REG TMTR_GLOBAL (TMTR_GLOBAL_REG) - Offset 1644h

TMT Timestamp Residue Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1644h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_GLOBAL_REG:** TMT residue value defined with a resolution of 2^-32ns.

10.2.312 REG TMTL_GLOBAL (TMTL_GLOBAL_REG) - Offset 1648h

TMT Timestamp Low Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1648h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_GLOBAL_REG:** Lower Half of the TMT defined in ns..

10.2.313 REG TMTH_GLOBAL (TMTH_GLOBAL_REG) - Offset 164Ch

TMT Timestamp High Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 164Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_GLOBAL_REG:** Upper Half of the TMT defined in ns.

10.2.314 REG TIMINCA_GLOBAL (TMT_TIMINCA_GLOBAL_REG) - Offset 1650h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1650h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_GLOBAL_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_GLOBAL_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

10.2.315 REG TIMADJ_GLOBAL (TMT_TIMADJ_GLOBAL_REG) - Offset 1654h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1654h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_GLOBAL_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_GLOBAL_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_GLOBAL_TIMADJ_TADJUS:** Time Adjust Value.

10.2.316 REG LXTS_TMT_LOW_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_0) - Offset 1658h

TMT Local Cross Timestamp Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1658h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_GLOBAL_REG:** TMTL captured when a local cross time stamp capture is enabled.

10.2.317 REG LXTS_TMT_HIGH_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_1) - Offset 165Ch

TMT Local Cross Timestamp Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 165Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_GLOBAL_REG:** TMTH captured when a local cross time stamp capture is enabled.

10.2.318 REG LXTS_ART_LOW_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_0) - Offset 1660h

TMT Local Cross Timestamp ART Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1660h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_GLOBAL_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

10.2.319 REG LXTS_ART_HIGH_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_1) - Offset 1664h

TMT lOcal Cross Timestamp ART Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1664h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_GLOBAL_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

10.2.320 REG RXTS_TMT_LOW_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_0) - Offset 1668h

TMT Remote Cross Timestamp Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1668h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_GLOBAL_REG:** TMTL captured when a remote time stamp capture is enabled.

10.2.321 REG RXTS_TMT_HIGH_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_1) - Offset 166Ch

TMT Remote Cross Timestamp Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 166Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_GLOBAL_REG:** TMTH captured when a remote time stamp capture is enabled.

10.2.322 REG TMTCTL_WORKING (TMT_CTL_WORKING_REG) - Offset 1680h

TMT Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1680h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_WORKING_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

10.2.323 REG TMTR_WORKING (TMTR_WORKING_REG) - Offset 1684h

TMT Timestamp Residue Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1684h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_WORKING_REG:** TMT residue value defined with a resolution of 2^-32ns.

10.2.324 REG TMTL_WORKING (TMTL_WORKING_REG) - Offset 1688h

TMT Timestamp Low Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1688h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_WORKING_REG:** Lower Half of the TMT defined in ns..

10.2.325 REG TMTH_WORKING (TMTH_WORKING_REG) - Offset 168Ch

TMT Timestamp High Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 168Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_WORKING_REG:** Upper Half of the TMT defined in ns.

10.2.326 REG TIMINCA_WORKING (TMT_TIMINCA_WORKING_REG) - Offset 1690h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1690h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_WORKING_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_WORKING_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

10.2.327 REG TIMADJ_WORKING (TMT_TIMADJ_WORKING_REG) - Offset 1694h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1694h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_WORKING_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_WORKING_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_WORKING_TIMADJ_TADJUS:** Time Adjust Value.

10.2.328 REG LXTS_TMT_LOW_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_0) - Offset 1698h

TMT Local Cross Timestamp Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1698h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_WORKING_REG:** TMTL captured when a local cross time stamp capture is enabled.

10.2.329 REG LXTS_TMT_HIGH_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_1) - Offset 169Ch

TMT Local Cross Timestamp Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 169Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_WORKING_REG:** TMTH captured when a local cross time stamp capture is enabled.

10.2.330 REG LXTS_ART_LOW_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_0) - Offset 16A0h

TMT Local Cross Timestamp ART Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 16A0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_WORKING_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

10.2.331 REG LXTS_ART_HIGH_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_1) - Offset 16A4h

TMT Local Cross Timestamp ART Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 16A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_WORKING_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

10.2.332 REG RXTS_TMT_LOW_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_0) - Offset 16A8h

TMT Remote Cross Timestamp Snapshot Register 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 16A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_WORKING_REG:** TMTL captured when a remote time stamp capture is enabled.

10.2.333 REG RXTS_TMT_HIGH_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_1) - Offset 16ACh

TMT Remote Cross Timestamp Snapshot Register 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 16ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_WORKING_REG:** TMTH captured when a remote time stamp capture is enabled.

10.2.334 D0i3 Control (D0I3C) - Offset 2000h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detect logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

10.2.335 Clock Gating And Soft Reset (CGSR) - Offset 2004h

This register is used to Clock Gate or Soft Reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

11 Universal Asynchronous Receiver-Transmitter (UART) Interface

11.1 UART Configuration Registers Summary

This chapter documents the registers of the Intel® PSE devices. This contains multiple Intel® PSE UART Controller devices:

- Intel® PSE UART Controller #0 - Bus: 0, Device: 17, Function: 0
- Intel® PSE UART Controller #1 - Bus: 0, Device: 17, Function: 1
- Intel® PSE UART Controller #2 - Bus: 0, Device: 17, Function: 2
- Intel® PSE UART Controller #3 - Bus: 0, Device: 17, Function: 3
- Intel® PSE UART Controller #4 - Bus: 0, Device: 17, Function: 4
- Intel® PSE UART Controller #5 - Bus: 0, Device: 17, Function: 5

DID Values:

- Intel® PSE UART Controller #0:- D17: F0 - 4B96h
- Intel® PSE UART Controller #1:- D17: F1 - 4B97h
- Intel® PSE UART Controller #2:- D17: F2 - 4B98h
- Intel® PSE UART Controller #3:- D17: F3 - 4B99h
- Intel® PSE UART Controller #4:- D17: F4 - 4B9Ah
- Intel® PSE UART Controller #5:- D17: F5 - 4B9Bh

Table 11-1. Summary of Bus: 0, Device: 17, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4B960000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h

Table 11-1. Summary of Bus: 0, Device: 17, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

11.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4B960000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B96h RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

11.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

11.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

11.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

11.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

11.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

11.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

11.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

11.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

11.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

11.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

11.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

11.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

11.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

11.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

11.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

11.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

11.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

11.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

11.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

11.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

11.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

11.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

11.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

11.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

11.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

11.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

11.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

11.2 UART MMIO Registers Summary

Table 11-2. Summary of Bus: 0, Device: 17, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	RBR	00000000h
4h	4	IER	00000000h
8h	4	IIR	00000001h
Ch	4	LCR	00000000h
10h	4	MCR	00000000h
14h	4	LSR	00000060h
18h	4	MSR	00000000h
1Ch	4	SCR	00000000h
70h	4	FAR	00000000h
7Ch	4	USR	00000006h
80h	4	TFL	00000000h
84h	4	RFL	00000000h
A4h	4	HTX	00000000h
A8h	4	DMASA	00000000h
ACh	4	TCR	00000006h
B0h	4	DE_EN	00000000h
B4h	4	RE_EN	00000000h
B8h	4	DET	00000000h
BCh	4	TAT	00000000h
C0h	4	DLF	00000000h
C4h	4	RAR	00000000h
C8h	4	TAR	00000000h
CCh	4	LCR_EXT	00000000h
F4h	4	CPR	00043532h
F8h	4	UCV	3430322Ah
FCh	4	CTR	44570110h
1000h	4	D0i3 Control (D0I3C)	00000008h
1004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

11.2.1 RBR - Offset 0h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE!= NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. ***Note***: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

11.2.2 IER - Offset 4h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

11.2.3 FIFO Control (FCR)—Offset 8h

Note that the register can also be used as the Interrupt Identification Register (IIR) when it is read from.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h WO	**RCVR:** This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full
5:4	0h WO	**TET:** This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full
3	0h RO	**Reserved**
2	0h WO	**XFIFOR:** This resets the control portion of the transmit FIFO and treats the FIFO as empty. ***Note:*** This bit is 'self-clearing'. It is not necessary to clear this bit
1	0h WO	**RFIFOR:** This resets the control portion of the receive FIFO and treats the FIFO as empty. ***Note:*** that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h WO	**FIFOE:** This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled

11.2.4 LCR - Offset Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. ***Note***: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

11.2.5 MCR - Offset 10h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable. Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/ disable the IrDA SIR Mode features. ***Note***: To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.
4	0h RW	**LOOPBACK:** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

11.2.6 LSR - Offset 14h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000060h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. ***Note***: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. ***Note***: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

11.2.7 MSR - Offset 18h

Modem Status Register - Whenever bits 0, 1, 2 or 3 are set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

11.2.8 SCR - Offset 1Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

11.2.9 FAR - Offset 70h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

11.2.10 USR - Offset 7Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7Ch	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

11.2.11 TFL - Offset 80h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 80h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

11.2.12 RFL - Offset 84h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 84h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

11.2.13 HTX - Offset A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

11.2.14 DMASA - Offset A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is used to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

11.2.15 TCR - Offset ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485

interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000006h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

11.2.16 DE_EN - Offset B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

11.2.17 RE_EN - Offset B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

11.2.18 DET - Offset B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

11.2.19 TAT - Offset BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. ***Note***: If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. ***Note***: The actual time is the programmed value + 1.

11.2.20 DLF - Offset C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

11.2.21 RAR - Offset C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. ***Note***: This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

11.2.22 TAR - Offset C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. ***Note***: This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

11.2.23 LCR_EXT - Offset CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. ***Note***: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. ***Note***: 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then sub-sequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. ***Note***: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

11.2.24 CPR - Offset F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F4h	00043532h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

11.2.25 UCV - Offset F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	3430322Ah

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

11.2.26 CTR - Offset FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + FCh	44570110h

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

11.2.27 D0i3 Control (D0I3C) - Offset 1000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW.
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the addition to the registers; the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

11.2.28 Clock Gating And Soft Reset (CGSR) - Offset 1004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

12 Inter-IC Sound (I2S) Interface

12.1 I2S Configuration Registers Summary

This chapter documents the registers in Bus: 0, Device 17, Function 6 and 7.

DID Values:

- Intel® PSE I2S Controller #0:- D17: F6 - 4B9Ch
- Intel® PSE I2S Controller #1:- D17: F7 - 4B9Dh

Table 12-1. Summary of Bus: 0, Device: 17, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID) - Offset 0h	4B9C0000h
4h	4	Status And Command (STATUSCOMMAND) - Offset 4h	00100000h
8h	4	Revision ID And Class Code (REVCLASSCODE) - Offset 8h	00000000h
Ch	4	Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch	00000000h
10h	4	Base Address Register (BAR) - Offset 10h	00000000h
14h	4	Base Address Register High (BAR_HIGH) - Offset 14h	00000000h
18h	4	Base Address Register1 (BAR1) - Offset 18h	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH) - Offset 1Ch	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch	00000000h
30h	4	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR) - Offset 34h	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG) - Offset 3Ch	00000100h
80h	4	Power Management Capability ID (POWERCAPID) - Offset 80h	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h	00000008h
90h	4	PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h	01400010h
98h	4	Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG) - Offset C0h	00000000h
D0h	4	MSI Capability Register (MSI_CAP_REG) - Offset D0h	01800005h

Table 12-1. Summary of Bus: 0, Device: 17, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D4h	4	MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h	00000000h
D8h	4	MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h	00000000h
DCh	4	MSI Message Data (MSI_MSG_DATA) - Offset DCh	00000000h
E0h	4	MSI Mask Register (MSI_MASK) - Offset E0h	00000000h
E4h	4	MSI Pending Register (MSI_PENDING) - Offset E4h	00000000h
F8h	4	Manufacturers ID (MANID) - Offset F8h	00000000h

12.1.1 Device ID And Vendor ID Register (DEVVENDID) - Offset 0h

Device ID and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 0h	4B9C0000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4B9Ch RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

12.1.2 Status And Command (STATUSCOMMAND) - Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

12.1.3 Revision ID And Class Code (REVCLASSCODE) - Offset 8h

Revision ID and Class Code

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device

12.1.4 Cache Line Latency Header And BIST (CLLATHEADERBIST) - Offset Ch

Cache Line size as RW with def 0 Latency Timer, RW with def 0 Header Type with Type 0 configuration header and Reserved BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multifunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cache Line Size

12.1.5 Base Address Register (BAR) - Offset 10h

Base Address Register Low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space

12.1.6 Base Address Register High (BAR_HIGH) - Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address High - MSB

12.1.7 Base Address Register1 (BAR1) - Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

12.1.8 Base Address Register1 High (BAR1_HIGH) - Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1_HIGH register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

12.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) - Offset 2Ch

SVID Register along with SID Register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

12.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR) - Offset 30h

Expansion ROM Base Address Register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

12.1.11 Capabilities Pointer (CAPABILITYPTR) - Offset 34h

Capabilities Pointer Register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is

12.1.12 Interrupt Register (INTERRUPTREG) - Offset 3Ch

Interrupt Line Register is not use in Bridge directly. Interrupt Pin Register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirements of latency timers and MAX_LAT register for max latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space
7:0	00h RW/P	**Interrupt Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

12.1.13 Power Management Capability ID (POWERCAPID) - Offset 80h

Power Management Capability ID Register points to next capability structure and Power Management Capability with Power Management Capabilities Register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

12.1.14 Power Management Control And Status Register (PMECTRLSTATUS) - Offset 84h

Power Management Control and Status Register to set and read PME Status, PME Enable, No Soft reset and Power State

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current Power State and to set a new Power State

12.1.15 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) - Offset 90h

PCI Device Vendor Specific Capability Register defines Vendor Specific Capability ID, Revision Length, Next Capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

12.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) - Offset 94h

Extended Vendor Capability Register for VSEC Length, Revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor Specific Extended Capability Revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

12.1.17 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) - Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

12.1.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) - Offset 9Ch

Device Idle Pointer Register giving details on Device MMIO Offset Location, BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** Contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** BAR Num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level

12.1.19 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) - Offset A0h

D0idle_Max_Power_On_Latency Register set at boot and power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If '1' then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If '1' then function will power gate when idle and the PMCSR[1:0] register in the function ='11' (D3)
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency Value

12.1.20 General Purpose Read Write Register1 (GEN_PCI_REGRW1) - Offset B0h

General Purpose PCI Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**General Purpose Read Write Field (GEN_PCI_REG_RW1):** General Purpose PCI Register: This register value is brought out as GEN_PCI_REG_RW1

12.1.21 General Purpose Input Register (GEN_INPUT_REG) - Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

12.1.22 MSI Capability Register (MSI_CAP_REG) - Offset D0h

MSI Capability Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

12.1.23 MSI Message Low Address (MSI_ADDR_LOW) - Offset D4h

MSI Message Low Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address
1:0	0h RO	**Reserved**

12.1.24 MSI Message High Address (MSI_ADDR_HIGH) - Offset D8h

MSI Message High Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

12.1.25 MSI Message Data (MSI_MSG_DATA) - Offset DCh

MSI Message Data

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

12.1.26 MSI Mask Register (MSI_MASK) - Offset E0h

MSI Mask bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

12.1.27 MSI Pending Register (MSI_PENDING) - Offset E4h

MSI Pending bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

12.1.28 Manufacturers ID (MANID) - Offset F8h

Manufacturers ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:29, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps

12.2 I2S MMIO Registers Summary

Table 12-2. Summary of Bus: 0, Device: 17, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	I2S-SC Control (I2S_CTRL)	000001B8h
4h	4	I2S Full Duplex Mode Receiver Control (I2S_CTRL_FDR)	00000010h
8h	4	Transceiver Sample Resolution (I2S_SRES)	00000000h
Ch	4	Full Duplex Mode Receive Samples Resolution (I2S_SRES_FDR)	00000000h
10h	4	Transceiver Sample Rate (I2S_SRATE)	00000000h
14h	4	I2S-SC Status Flags (I2S_STAT)	0003000Ch
18h	4	FIFO Using Level(Read Only) (FIFO_LEVEL)	00000000h
1Ch	4	FIFO Almost Empty Level (FIFO_AEMPTY)	00000000h
20h	4	FIFO Almost Full Level (FIFO_AFULL)	0000001Fh
24h	4	Full Duplex Mode Receiver FIFO Using Level(Read Only) (FIFO_LEVEL_FDR)	00000000h
28h	4	Full Duplex Mode Receiver FIFO Almost Empty Level (FIFO_AEMPTY_FDR)	00000000h
2Ch	4	Full Duplex Mode Receiver FIFO Almost Full Level (FIFO_AFULL_FDR)	0000001Fh
30h	4	Time Division Multiplexing Control (TDM_CTRL)	FFFF0000h
34h	4	Time Division Multiplexing Full Duplex Mode Channels Direction (TDM_FD_DIR)	0000FFFFh

Table 12-2. Summary of Bus: 0, Device: 17, Function: 6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40h	4	TX/RX FIFo (FIFO)	00000000h
1000h	4	D0i3 Control (D0I3C)	00000008h
1004h	4	Clock Gating And Soft Reset (CGSR)	00000000h

12.2.1 I2S-SC Control (I2S_CTRL) - Offset 0h

I2S-SC Control Register After end of reset bit sfr_rst triggers to 1 and bit FIFO_rst triggers to 1. Therefore register value after end of reset is 000001B8.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	000001B8h

FIFO

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Full-Duplex Mode Receiver Samples Resolution (FULL_DUPLEX):** Full-duplex mode enable bit. If HIGH transmitter and receiver data units work simultaneously, otherwise only transmitter or receiver is enable in dependent to dir_cfg bit (I2S_CTRL[1]).
30	0h RW	**FIFO Almost Full Mask Register (FIFO_AFULL_MASK):** Bit masking interrupt request generation after FIFO becomes almost full. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
29	0h RW	**FIFO Full Mask Register (FIFO_FULL_MASK):** Bit masking interrupt request generation after FIFO becomes full. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
28	0h RW	**FIFO Almost Empty Mask Register (FIFO_AEMPTY_MASK):** Bit masking interrupt request generation after FIFO becomes almost empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition. Sampled on the rising edge of the clock.
27	0h RW	**FIFO Empty Mask Register (FIFO_EMPTY_MASK):** Bit masking interrupt request generation after FIFO becomes empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition. Sampled on the rising edge of the clock.
26	0h RW	**I2s Mask Register (I2S_MASK):** Bit masking interrupt request generation after underrun/overrun condition occurrence in I2S-SC transceiver. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for underrun event interrupt. Sampled on the rising edge of the clock.
25	0h RW	**Interrupt Mask Register (INTREQ_MASK):** Bit masking all interrupt requests. When LOW all interrupts are masked, when HIGH interrupts use individual masks. Sampled on the rising edge of the clock.
24	0h RW	**Transceiver Clock Enable. (I2S_STB):** Transceiver clock enable. When LOW the clk_i2s clock is enabled, else clock is disabled. Sampled on the rising edge of the clock.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Audio Data Sample Alignment At Host Data Bus. (HOST_DATA_ALIGN):** Audio data sample alignment at host data bus. When LOW the audio sample data is aligned to the LSB at the host data bus. When HIGH the audio sample data is aligned to the MSB at host data bus.Sampled on the rising edge of the clock.
22	0h RW	**Audio Data Sample Arrangement In Audio Data Slot (DATA_ORDER):** Bit masking interrupt request generation after FIFO becomes almost empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
21	0h RW	**Audio Sample Alignment In Audio Data Time Slot (DATA_ALIGN):** Bit masking interrupt request generation after FIFO becomes empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
20:16	00h RW	**Audio Data Delay After WS Signal (DATA_WS_DEL):** Bit masking interrupt request generation after underrun/overrun condition occurrence in I2S-SC transceiver. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for underrun event interrupt.
15	0h RW	**The Word Select Signal Polarity Selection. (WS_POLAR):** Bit masking all interrupt requests. When LOW all interrupts are masked, when HIGH interrupts use individual masks.
14	0h RW	**The Continuous Serial Clock Active Edge. (SCK_POLAR):** Transceiver clock enable. When LOW the clk_i2s clock is enabled, else clock is disabled.
13	0h RW	**Mono/Stereo Audio Mode Selection (AUDIO_MODE):** Audio data sample alignment at host data bus. When LOW the audio sample data is aligned to the LSB at the host data bus. When HIGH the audio sample data is aligned to the MSB at host data bus.
12	0h RW	**Active Audio Channel In Mono Mode (MONO_MODE):** Active audio channel in mono mode. When LOW left audio channel is active. When HIGH right audio channel is active.
11:8	1h RW	**Word Select Signal (WS) Format. (WS_MODE):** Word select signal (WS) format. TDM mode is not active: Only bit 8 is relevant. If it is set to LOW (even value of ws_mode) WS signal have DSP audio interface specification format. If it is set to HIGH (odd value of ws_mode) WS signal have standard I2S audio interface specification format. TDM mode is active: When field equals 0 WS signal has DSP audio interface specification format, otherwise (ws_mode field equals the value from range 1 &CHN_NO-1) WS.
7:5	5h RW	**Audio Channel Time Slot Width (CHN_WIDTH):** Audio channel time slot width in I2S master or DSP/TDM master and slave modes. 0 8 SCK cycles per audio channel 1 12 SCK cycles per audio channel 2 16 SCK cycles per audio channel 3 18 SCK cycles per audio channel 4 20 SCK cycles per audio channel 5 24 SCK cycles per audio channel 6 28 SCK cycles per audio channel 7 32 SCK cycles per audio channel.
4	1h RW	**FIFO Reset (FIFO_RST):** FIFO reset. When LOW, FIFO pointer is reset to zero. Threshold levels for FIFO are unchanged. This bit is automatically set to HIGH after one clock cycle. In full-duplex mode this bit resets only transmitter FIFO.
3	1h RW	**SFR Block Synchronous Reset (SFR_RST):** SFR block synchronous reset. When LOW, all bits in SFR registers are reset to default values. This bit is automatically set to HIGH after one clock cycle.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Configuration Bit For Transceiver Synchronizing Unit (MS_CFG):** Configuration bit for transceiver synchronizing unit: 1 Master 0 Slave.
1	0h RW	**Direction Of Transmission (DIR_CFG):** 1 Transmitter 0 Receiver.
0	0h RW	**Enable Bit For I2S Transceiver (I2S_EN):** 1 enables transceiver 0 disables transceiver, causes synchronous reset signal, configuration SFR bits are unchanged.

12.2.2 I2S Full Duplex Mode Receiver Control (I2S_CTRL_FDR) - Offset 4h

I2S Full Duplex Mode Receiver Control Register After end of reset bit FIFO_rst triggers to 1. Therefore register value after end of reset is 00000010.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**Full Duplex Almost FIFO Full Mask Register (RFIFO_AFULL_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes almost full. When LOW, masks generation of interrupt request.
29	0h RW	**Full Duplex FIFO Full Mask Register (RFIFO_FULL_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes full. When LOW, masks generation of interrupt request.
28	0h RW	**Full Duplex Almost FIFO Empty Mask Register (RFIFO_AEMPTY_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes almost empty. When LOW, masks generation of interrupt request.
27	0h RW	**Full Duplex FIFO Empty Mask Register (RFIFO_EMPTY_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes empty. When LOW, masks generation of interrupt request.
26	0h RW	**Full Duplex I2s_mask Register (RI2S_MASK):** Bit masking interrupt request generation after overrun condition occurrence in I2S-SC full-duplex mode receiver. When LOW, masks generation of interrupt request.
25:5	0h RO	**Reserved**
4	1h RW	**Full-Duplex Mode Receiver FIFO Reset. (FIFO_RST):** Full-duplex mode receiver FIFO reset. Active only in full-duplex mode. When '0', RFIFO pointer is reset to zero. Threshold levels for RFIFO are unchanged. The bit is automatically set to '1' after one clock cycle.
3:0	0h RO	**Reserved**

12.2.3 Transceiver Sample Resolution (I2S_SRES) - Offset 8h

Transceiver Sample Resolution.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Samples Resolution. (RESOLUTION):** Samples resolution. When full-duplex mode is active, this value specifies resolution only for transmitted samples. Sampled on the rising edge of the clock. It simply should be assigned the value equal to the number of valid bits minus one, for example, 00000B sample resolution = 1 bit 11111B sample resolution = 32 bits.

12.2.4 Full Duplex Mode Receive Samples Resolution (I2S_SRES_FDR) - Offset Ch

Full Duplex Mode Receive Samples Resolution.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**I2s_sres Register - Samples Resolution (RESOLUTION):** Full-duplex mode receives samples resolution. When half-duplex mode is active this value is ignored. It simply should be assigned the value equal to the number of valid bits minus one, for example, 00000B sample resolution = 1 bit 11111B sample resolution = 32 bits.

12.2.5 Transceiver Sample Rate (I2S_SRATE) - Offset 10h

Transceiver Sample Rate.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:0	00000h RW	**SAMPLE_RATE:** In general value of sample rate is the quotient of CLK frequency and I2S rate [bit/s]. The value of sample rate is the higher the CLK frequency is greater than I2S rate.

12.2.6 I2S-SC Status Flags (I2S_STAT) - Offset 14h

I2S-SC Status Flags Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	0003000Ch

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Receive FIFO Almost Full Flag In Full-Duplex Mode (RFIFO_AFULL):** Receive FIFO almost full flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO becomes almost full (rising edge of almost full condition).
18	0h RW	**Receive FIFO Full Flag In Full-Duplex Mode (RFIFO_FULL):** Receive FIFO full flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO is full.
17	1h RW	**Receive FIFO Almost Empty Flag In Full-Duplex Mode (RFIFO_AEMPTY):** Receive FIFO almost empty flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO becomes almost empty (rising edge of almost empty condition).
16	1h RW	**Receive FIFO Empty Flag In Full-Duplex Mode (RFIFO_EMPTY):** Receive FIFO empty flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO is empty.
15:6	0h RO	**Reserved**
5	0h RW	**FIFO Almost Full Flag (FIFO_AFULL):** FIFO almost full flag. Active HIGH. This flag is set to HIGH when FIFO becomes almost full (rising edge of almost full condition). When full-duplex mode is active, this bit is a flag only for transmitter FIFO almost full condition.
4	0h RW	**FIFO Full Flag (FIFO_FULL):** FIFO full flag. Active HIGH. This flag is set to HIGH when FIFO is full. When full-duplex mode is active, this bit is a flag only for transmitter FIFO full condition.
3	1h RW	**FIFO Almost Empty Flag (FIFO_AEMPTY):** FIFO almost empty flag. Active HIGH. This flag is set to HIGH when FIFO becomes almost empty (rising edge of almost empty condition). When full-duplex mode is active, this bit is a flag only for transmitter FIFO almost empty condition.
2	1h RW	**FIFO Empty Flag (FIFO_EMPTY):** FIFO empty flag. Active HIGH. This flag is set to HIGH when FIFO is empty. When full-duplex mode is active, this bit is a flag only for transmitter FIFO empty condition.
1	0h RW	**RDATA_OVRERR:** Indicates data overrun error for transceiver in receiver mode, active HIGH. Sampled and updated on the rising edge of the clock. Writing LOW value to this bit resets the transceiver and the FIFO. The transceiver configuration is preserved.
0	0h RW	**Full Duplex Mode Samples Resolution Register (TDATA_UNDERR):** Indicates data underrun event, active HIGH. This flag is set to HIGH when TX underrun arises (rising edge of underrun condition).

12.2.7 FIFO Using Level (Read Only) (FIFO_LEVEL) - Offset 18h

FIFO Using Level Register (read only).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RO	**FIFO Level Register (FIFO_LEVEL):** Indicates FIFO level. Updated on the rising edge of the clock. When full-duplex mode is active, this register holds value of the transmitter FIFO level. When half-duplex mode is active, this register holds value of the transmitter or receiver FIFO level in dependent to the transmit/receive direction mode.

12.2.8 FIFO Almost Empty Level (FIFO_AEMPTY) - Offset 1Ch

FIFO Almost Empty Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**FIFO Almost Empty Threshold Level (AEMPTY_THRESHOLD):** Determines threshold for almost empty flag in the FIFO. When full-duplex mode is active, this register specifies an almost empty level of the transmitter FIFO level.

12.2.9 FIFO Almost Full Level (FIFO_AFULL) - Offset 20h

FIFO Almost Full Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20h	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	1Fh RW	**FIFO Aempty Threshold Level (AFULL_THRESHOLD):** Determines threshold for almost full flag in the FIFO. When full-duplex mode is active, this register specifies an almost full level of the transmitter FIFO level.

12.2.10 Full Duplex Mode Receiver FIFO Using Level (Read Only) (FIFO_LEVEL_FDR) - Offset 24h

Full Duplex Mode Receiver FIFO Using Level Register (read only).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RO	**Full Duplex FIFO Level (RX_FIFO_LEVEL):** Full-duplex mode receives FIFO level.

12.2.11 Full Duplex Mode Receiver FIFO Almost Empty Level (FIFO_AEMPTY_FDR) - Offset 28h

Full Duplex Mode Receiver FIFO Almost Empty Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Full Duplex FIFO Almost Empty Level (AEMPTY_THRESHOLD):** Determines almost empty level in the receive FIFO in full-duplex mode.

12.2.12 Full Duplex Mode Receiver FIFO Almost Full Level (FIFO_AFULL_FDR) - Offset 2Ch

Full Duplex Mode Receiver FIFO Almost Full Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 2Ch	0000001Fh

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	1Fh RW	**Full Duplex FIFO Almost Full Level (AFULL_THRESHOLD):** Determines almost full level in the receive FIFO in full-duplex mode.

12.2.13 Time Division Multiplexing Control (TDM_CTRL) - Offset 30h

Time Division Multiplexing Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30h	FFFF0000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**TDM Channel Enable 15 (CH15_EN):** TDM interface channel 15 activating bit. When HIGH 15th time slot sample is transmitted and/or received depending on transceiver mode.
30	1h RW	**TDM Channel Enable 14 (CH14_EN):** TDM interface channel 14 activating bit. When HIGH 14th time slot sample is transmitted and/or received depending on transceiver mode.
29	1h RW	**TDM Channel Enable 13 (CH13_EN):** TDM interface channel 13 activating bit. When HIGH 13th time slot sample is transmitted and/or received depending on transceiver mode.
28	1h RW	**TDM Channel Enable 12 (CH12_EN):** TDM interface channel 12 activating bit. When HIGH 12th time slot sample is transmitted and/or received depending on transceiver mode.
27	1h RW	**TDM Channel Enable 11 (CH11_EN):** TDM interface channel 11 activating bit. When HIGH 11th time slot sample is transmitted and/or received depending on transceiver mode.
26	1h RW	**TDM Channel Enable 10 (CH10_EN):** TDM interface channel 10 activating bit. When HIGH 10th time slot sample is transmitted and/or received depending on transceiver mode.
25	1h RW	**TDM Channel Enable 9 (CH9_EN):** TDM interface channel 9 activating bit. When HIGH 9th time slot sample is transmitted and/or received depending on transceiver mode.
24	1h RW	**TDM Channel Enable 8 (CH8_EN):** TDM interface channel 8 activating bit. When HIGH 8th time slot sample is transmitted and/or received depending on transceiver mode.
23	1h RW	**TDM Channel Enable 7 (CH7_EN):** TDM interface channel 7 activating bit. When HIGH 7th time slot sample is transmitted and/or received depending on transceiver mode.
22	1h RW	**TDM Channel Enable 6 (CH6_EN):** TDM interface channel 6 activating bit. When HIGH 6th time slot sample is transmitted and/or received depending on transceiver mode.
21	1h RW	**TDM Channel Enable 5 (CH5_EN):** TDM interface channel 5 activating bit. When HIGH 5th time slot sample is transmitted and/or received depending on transceiver mode.
20	1h RW	**TDM Channel Enable 4 (CH4_EN):** TDM interface channel 4 activating bit. When HIGH 4th time slot sample is transmitted and/or received depending on transceiver mode.
19	1h RW	**TDM Channel Enable 3 (CH3_EN):** TDM interface channel 3 activating bit. When HIGH 3rd time slot sample is transmitted and/or received depending on transceiver mode.
18	1h RW	**TDM Channel Enable 2 (CH2_EN):** TDM interface channel 2 activating bit. When HIGH 2nd time slot sample is transmitted and/or received depending on transceiver mode.

Bit Range	Default & Access	Field Name (ID): Description
17	1h RW	**TDM Channel Enable 1 (CH1_EN):** TDM interface channel 1 activating bit. When HIGH 1st time slot sample is transmitted and/or received depending on transceiver mode.
16	1h RW	**TDM Channel Enable 0 (CH0_EN):** TDM interface channel 0 activating bit. When HIGH zero time slot sample is transmitted and/or received depending on transceiver mode.
15:5	0h RO	**Reserved**
4:1	0h RW	**TDM Register For Number Of Channels Per Frame (CHN_NO):** Number of supported audio channels in TDM compatible interface mode. Written value equals channels number minus 1.
0	0h RW	**Time Division Multiplexing Audio Interface Enable (TDM_EN):** Time Division Multiplexing audio interfaces enable. When HIGH audio interface works in TDM compatible mode determined by this register value. When LOW audio interface works in standard stereo I2S mode.

12.2.14 Time Division MultSDIiplexing Full Duplex Mode Channels Direction (TDM_FD_DIR) - Offset 34h

Time Division Multiplexing Full Duplex Mode Channels Direction Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 34h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Full Duplex Rx Channel Enable 15 (CH15_RXEN):** TDM interface channel 15 receives enable bit. Active only in full-duplex mode. When HIGH and ch15_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 15 time slot.
30	0h RW	**Full Duplex Rx Channel Enable 14 (CH14_RXEN):** TDM interface channel 14 receives enable bit. Active only in full-duplex mode. When HIGH and ch14_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 14 time slot.
29	0h RW	**Full Duplex Rx Channel Enable 13 (CH13_RXEN):** TDM interface channel 13 receives enable bit. Active only in full-duplex mode. When HIGH and ch13_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 13 time slot.
28	0h RW	**Full Duplex Rx Channel Enable 12 (CH12_RXEN):** TDM interface channel 12 receives enable bit. Active only in full-duplex mode. When HIGH and ch12_en bit in TDM_CTRL register is HIGH audio sample is received from SDO line at 12 time slot.
27	0h RW	**Full Duplex Rx Channel Enable 11 (CH11_RXEN):** TDM interface channel 11 receives enable bit. Active only in full-duplex mode. When HIGH and ch11_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 11 time slot.
26	0h RW	**Full Duplex Rx Channel Enable 10 (CH10_RXEN):** TDM interface channel 10 receives enable bit. Active only in full-duplex mode. When HIGH and ch10_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 10 time slot.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**Full Duplex Rx Channel Enable 9 (CH9_RXEN):** TDM interface channel 9 receives enable bit. Active only in full-duplex mode. When HIGH and ch9_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 9 time slot.
24	0h RW	**Full Duplex Rx Channel Enable 8 (CH8_RXEN):** TDM interface channel 8 receives enable bit. Active only in full-duplex mode. When HIGH and ch8_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 8 time slot.
23	0h RW	**Full Duplex Rx Channel Enable 7 (CH7_RXEN):** TDM interface channel 7 receives enable bit. Active only in full-duplex mode. When HIGH and ch7_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 7 time slot.
22	0h RW	**Full Duplex Rx Channel Enable 6 (CH6_RXEN):** TDM interface channel 6 receives enable bit. Active only in full-duplex mode. When HIGH and ch6_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 6 time slot.
21	0h RW	**Full Duplex Rx Channel Enable 5 (CH5_RXEN):** TDM interface channel 5 receives enable bit. Active only in full-duplex mode. When HIGH and ch5_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 5 time slot.
20	0h RW	**Full Duplex Rx Channel Enable 4 (CH4_RXEN):** TDM interface channel 4 receives enable bit. Active only in full-duplex mode. When HIGH and ch4_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 4 time slot.
19	0h RW	**Full Duplex Rx Channel Enable 3 (CH3_RXEN):** TDM interface channel 3 receives enable bit. Active only in full-duplex mode. When HIGH and ch3_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 3 time slot.
18	0h RW	**Full Duplex Rx Channel Enable 2 (CH2_RXEN):** TDM interface channel 2 receives enable bit. Active only in full-duplex mode. When HIGH and ch2_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 2 time slot.
17	0h RW	**Full Duplex Rx Channel Enable 1 (CH1_RXEN):** TDM interface channel 1 receives enable bit. Active only in full-duplex mode. When HIGH and ch1_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 1 time slot.
16	0h RW	**Full Duplex Tx Channel Enable 0 (CH0_TXEN):** TDM interface channel 0 receives enable bit. Active only in full-duplex mode. When HIGH and ch0_en bit in TDM_CTRL register is HIGH audio sample is received from SDI line at 0 time slot.
15	1h RW	**Full Duplex Tx Channel Enable 15 (CH15_TXEN):** TDM interface channel 15 transmit enable bit. Active only in full-duplex mode. When HIGH and ch15_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 15 time slot through SDO line.
14	1h RW	**Full Duplex Tx Channel Enable 14 (CH14_TXEN):** TDM interface channel 14 transmit enable bit. Active only in full-duplex mode. When HIGH and ch14_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 14 time slot through SDO line.
13	1h RW	**Full Duplex Tx Channel Enable 13 (CH13_TXEN):** TDM interface channel 13 transmit enable bit. Active only in full-duplex mode. When HIGH and ch13_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 13 time slot through SDO line.
12	1h RW	**Full Duplex Tx Channel Enable 12 (CH12_TXEN):** TDM interface channel 12 transmit enable bit. Active only in full-duplex mode. When HIGH and ch12_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 12 time slot through SDO line.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Full Duplex Tx Channel Enable 11 (CH11_TXEN):** TDM interface channel 11 transmit enable bit. Active only in full-duplex mode. When HIGH and ch11_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 11 time slot through SDO line.
10	1h RW	**Full Duplex Tx Channel Enable 10 (CH10_TXEN):** TDM interface channel 10 transmit enable bit. Active only in full-duplex mode. When HIGH and ch10_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 10 time slot through SDO line.
9	1h RW	**Full Duplex Tx Channel Enable 9 (CH9_TXEN):** TDM interface channel 9 transmit enable bit. Active only in full-duplex mode. When HIGH and ch9_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 9 time slot through SDO line.
8	1h RW	**Full Duplex Tx Channel Enable 8 (CH8_TXEN):** TDM interface channel 8 transmit enable bit. Active only in full-duplex mode. When HIGH and ch8_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 8th time slot through SDO line.
7	1h RW	**Full Duplex Tx Channel Enable 7 (CH7_TXEN):** TDM interface channel 7 transmit enable bit. Active only in full-duplex mode. When HIGH and ch7_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 7 time slot through SDO line.
6	1h RW	**Full Duplex Tx Channel Enable 6 (CH6_TXEN):** TDM interface channel 6 transmit enable bit. Active only in full-duplex mode. When HIGH and ch6_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 6 time slot through SDO line.
5	1h RW	**Full Duplex Tx Channel Enable 5 (CH5_TXEN):** TDM interface channel 5 transmit enable bit. Active only in full-duplex mode. When HIGH and ch5_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 5 time slot through SDO line.
4	1h RW	**Full Duplex Tx Channel Enable 4 (CH4_TXEN):** TDM interface channel 4 transmit enable bit. Active only in full-duplex mode. When HIGH and ch4_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 4 time slot through SDO line.
3	1h RW	**Full Duplex Tx Channel Enable 3 (CH3_TXEN):** TDM interface channel 3 transmit enable bit. Active only in full-duplex mode. When HIGH and ch3_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 3 time slot through SDO line.
2	1h RW	**Full Duplex Tx Channel Enable 2 (CH2_TXEN):** TDM interface channel 2 transmit enable bit. Active only in full-duplex mode. When HIGH and ch2_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 2 time slot through SDO line.
1	1h RW	**Full Duplex Tx Channel Enable 1 (CH1_TXEN):** TDM interface channel 1 transmit enable bit. Active only in full-duplex mode. When HIGH and ch1_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 1 time slot through SDO line.
0	1h RW	**Full Duplex Rx Channel Enable 0 (CH0_RXEN):** TDM interface channel 0 transmit enable bit. Active only in full-duplex mode. When HIGH and ch0_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 0 time slot through SDO line.

12.2.15 TX/RX FIFO (FIFO) - Offset 40h

TX/RX FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SFR:** Registers for TX and RX FIFO.

12.2.16 D0i3 Control (D0I3C) - Offset 1000h

This register will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done). The description below also includes the type of access expected for the ISH FW for each configuration bit:
1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost.
2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit.
3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW.
4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear).
A simple edge detects logic can be used for the setting of this bit in HW. The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt; In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following:
1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) needs to be connected to a soft strap for ISH with a value of 1.
2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied.
3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

12.2.17 Clock Gating And Soft Reset (CGSR) - Offset 1004h

This register is used to Clock gate or soft reset an IP by Host/Remote Host. Also register field of this register can be used for device idle status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

13 SBEP Interface

This chapter documents the SBEP Host registers.

13.1 SBEP Registers Summary

Table 13-1. Summary of SBEP Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Attribute Reg (DS_ATTRIBUTES)	00000000h
4h	4	Address Reg LO (DS_ADDRESS_LSB)	00000000h
8h	4	Address Reg HI (DS_ADDRESS_MSB)	00000000h
Ch	4	Extended Header (SAIRS) (DS_SAI)	00000000h
10h	4	Received Data (DS_DATA_IN)	00000000h
14h	4	Control And Status (DS_CONTROL_STATUS)	00000000h
18h	4	ISH Source Port ID (DS_SOURCEPORTID)	00000000h
20h	4	Completion Data (DS_CMP_DATA)	00000000h
24h	4	Completion SAI (DS_CMP_SAI)	00000000h
28h	4	Completion Status And Control (DS_CMP_STATUS)	00000000h
40h	4	Status Reg (US_STATUS)	00000000h
44h	4	Command Reg (US_COMMAND)	00000000h
48h	4	Target AddressLO (US_TARGET_LO)	00000000h
4Ch	4	Target AddressHI (US_TARGET_HIGH)	00000000h
50h	4	Target Out Data (US_TARGET_DATA)	00000000h
54h	4	Upstream Attribute (US_ATTRIBUTES)	00000000h
58h	4	Upstream Request SAIRS (US_SAIR)	80000000h
5Ch	4	Upstream Completion Data (US_CMP_DATA)	00000000h
60h	4	Upstream Completion Status And Control (US_CMP_STATUS_CONTROL)	00000000h
64h	4	Upstream Completion SAI (US_CMP_SAIR)	00000034h
68h	4	SAI_WIDTH Reg (SAI_WIDTH)	00000007h
6Ch	4	Side Clk Gate Enable (SIDE_CLK_GATE_EN)	00000000h
74h	4	Received Data (DS_DATA_IN_DW2)	00000000h
80h	4	DN Access Valid Enable (DS_ACCESS_VALID_EN)	00000000h
84h	4	Boot Prep Control (BOOT_PREP_CONTROL_REG)	00000000h

13.1.1 Attribute Reg (DS_ATTRIBUTES) — Offset 0h

Attribute Register. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:24	0h WO	**BYTE_ENABLE_OF_THE_DWORD:** Byte enables. First byte enables.
23:16	00h WO	**OPCODE_OF_MESSAGE:** Opcode of messages.
15:8	00h WO	**SOURCE_PORT_ID:** Source Port ID.
7:0	00h WO	**DESTINATION_PORT_ID:** Destination Port ID.

13.1.2 Address Reg LO (DS_ADDRESS_LSB) — Offset 4h

Downstream Address Register LO. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**ADDRESS_LSB:** Address [31:0].

13.1.3 Address Reg HI (DS_ADDRESS_MSB) — Offset 8h

Downstream Address Register HI. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Address Length (ADDRESS_LENGTH):** Indicates the length of the address field as follows: 0: 16-bit address 1: 48-bit address.
30:16	0h RO	**Reserved**
15:0	0000h WO	**ADDRESS_MSB:** Address [47:32].

13.1.4 Extended Header (SAIRS) (DS_SAI) — Offset Ch

Downstream Extended Header (SAIRS) Register. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**VALID:** EH Present SAI preset- when 1, 23:0 bits are valid.
30:20	0h RO	**Reserved**
19:16	0h WO	**ROOT_SPACE:** Root Space field received in message.
15:0	0000h WO	**SAI:** SAI Security attribute indicator.

13.1.5 Received Data (DS_DATA_IN) — Offset 10h

Downstream Received Data Register DW2. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**DATA_RECEIVED:** Data received in message.

13.1.6 Control And Status (DS_CONTROL_STATUS) — Offset 14h

Downstream Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**MSG_RX_STATUS:** Message received interrupt - Message received interrupt status register. Written by HW and cleared HW itself when MinuteIA writes to upstream completion control register indicating completion is available. When cleared interrupt going to MinuteIA goes low.
30	0h RW	**INTERRUPT_MASK:** Interrupt mask register for message received interrupt. When set to 1 interrupt is not generated to MinuteIA. Mask does not affect interrupt status bit.
29:2	0h RO	**Reserved**
1:0	0h RO	**TYPE_OF_TRANSACTION:** Type of transaction: indicates type of transaction received as follows: 2 b001: Posted message 2 b010: Non-posted message 2 b1011: Completion message

13.1.7 ISH Source Port ID (DS_SOURCEPORTID) — Offset 18h

Downstream Source Port ID.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**SOURCE_PORT_ID:** (Reset value is 0, straps will get loaded runtime) Source ID of ISH. Default value is coming from top level straps.

13.1.8 Completion Data (DS_CMP_DATA) — Offset 20h

Downstream Completion Data Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**COMPLETION_DATA:** Completion data received for upstream non-posted read.

13.1.9 Completion SAI (DS_CMP_SAI) — Offset 24h

Downstream Completion SAI Registers.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**COMPLETION_SAI:** Completion SAI received for upstream non-posted read.

13.1.10 Completion Status And Control (DS_CMP_STATUS) — Offset 28h

Downstream Completion Status and Control Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**COMPLETION_RECEIVED:** Completion received status register. Set by HW and cleared by FW by writing 1 to it.
30	0h RW	**INTERRUPT_MASK:** Interrupt mask register for completion received interrupt. When set to 1 interrupt is not generated to MinuteIA. Mask does not affect interrupt status bit.
29:9	0h RO	**Reserved**
8	0h RO	**DN_CMPL_EHPRESENT:** EH present for Downstream completion (ISH4 Only).
7:3	0h RO	**Reserved**
2:0	0h RO	**Completion Status (COMPLETION_STATUS):** 000: Successful Completion (SC) 001: Unsupported Request (UR)

13.1.11 Status Reg (US_STATUS) — Offset 40h

Upstream Status Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW/1C	**Message Sent (MSG_SENT):** Upstream message sent interrupt status 1, Upstream message has been sent out. This is cleared FW by writing 1 to it.
0	0h RO	**SM Status (STATE_MACHINE_STATUS):** 1 = The Endpoint State Machine is busy. 0 = The Endpoint Status Machine is idle. This is OR of posted SM and NP SM busy signals.

13.1.12 Command Reg (US_COMMAND) — Offset 44h

Upstream Command Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Interrupt Enable (ENABLE_INTERRUPT):** 1 = Cause an interrupt when the transaction completes.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Message Type (TYPE_OF_MSG):** 1 = Transaction will be Posted 0 = Transaction will be non-posted will be hardcoded to 0 indicating NP message. For posted message register (new) this field would be hardcoded to 1.
1	0h RW	**Transaction Command Type (TRANSACTION_TYPE):** 1 = Transaction will be a Read 0 = Transaction will be a Write. For posted message register (new) this bit will be hardcoded to 0 as reads cannot be P.
0	0h RW	**SEND_IOSF_SB_TRANSACTION:** MinuteIA writes a 1 to this bit to cause an IOSF SB Transaction. The type of transaction is determined by Bit 1 in this register. *This bit will always be read as 0 but FW can write it to 1 to start the upstream transaction. In that way it won't be readable as 1 after writing to.

13.1.13 Target Address LO (US_TARGET_LO) — Offset 48h

Target Address Register LO.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Address Low (ADDRESS_LOW):** Address of message. Offset within the Target s IOSF SB Port.

13.1.14 Target Address HI (US_TARGET_HIGH) — Offset 4Ch

Target Address Register HI.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 4Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Length (ADDRESS_LENGTH):** Indicates the length of the address field as follows: 0: 16-bit address 1: 48-bit address
30:16	0h RO	**Reserved**
15:0	0000h RW	**Address MSB (ADDRESS_HIGH):** MSB 16 address bits, valid only when bit 31 is set to 1.

13.1.15 Target Out Data (US_TARGET_DATA) — Offset 50h

Target Out Data Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA_SENT:** The MinuteIA writes the data value that will be sent on the next write IOSF SB Transaction.

13.1.16 Upstream Attribute (US_ATTRIBUTES) — Offset 54h

Upstream Attribute Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**FID:** FID.
23:20	0h RW	**BAR:** BAR for upstream register access.
19:16	0h RW	**BYTE_ENABLE_FOR_THE_MSG:** Upstream byte enables. 19:16 FBE.
15:8	00h RW	**OPCODE:** Message Opcode. This Opcode will go as Opcode for upstream message.
7:0	00h RW	**DESTINATION_PORT_ID:** Destination ID of upstream message. For ex. If when the upstream message is targeted to PMC then.FW writes to this register with destination ID of PMC.

13.1.17 Upstream Request SAIRS (US_SAIR) — Offset 58h

Upstream Request SAIRS Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 58h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**EH Present (EH_PRESET):** Extended header present indication. When set to 1 indicates extended header is present. Currently tied to 1 in RTL as ISH supports only EH=1 transactions.
30:20	0h RO	**Reserved**
19:16	0h RW	**ROOT_SPACE:** Root space.

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10:8	0h RW	**TAG:** Tag.
7:0	00h RO	**SAI_OF_IOSF_SBEP:** ISH SAI to be inserted in all upstream messages with if EH_present bit is set to 1. Reset value is 0, straps will get loaded runtime.

13.1.18 Upstream Completion Data (US_CMP_DATA) — Offset 5Ch

Upstream Completion Data Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**COMPLETION_DATA:** Completion data to be used for upstream completion as a result of downstream read request. This field is valid only downstream when type of transfer register indicates non-posted type of transaction.

13.1.19 Upstream Completion Status And Control (US_CMP_STATUS_CONTROL) — Offset 60h

Upstream Completion Status and Control Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/AC	**IOSF_SB_COMPLETION:** Upstream completion for Downstream request. MinuteIA writes a 1 to this bit to indicate downstream message received is consumed. This internally causes an IOSF SB completion Transaction if original downstream request is non-posted. If original message is posted then upstream completion is not generated by HW. to it. This bit cleared by HW.
30:3	0h RO	**Reserved**
2:0	0h RW	**COMPLETION_STATUS:** Completion Status: 000: Successful Completion (SC) 001: Unsupported Request (UR)

13.1.20 Upstream Completion SAI (US_CMP_SAIR) — Offset 64h

Upstream Completion SAI Register.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 64h	00000034h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	34h RO	**SAI_STRAP_FOR_COMPLETION:** SAI for ISH which will be inserted in upstream completion. Reset value is 0, straps will get loaded runtime.

13.1.21 SAI_WIDTH Reg (SAI_WIDTH) — Offset 68h

Register for SAI_WIDTH.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 68h	00000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	7h RO	**SAI_WIDTH:** Specifies the SAI Width value.

13.1.22 Side Clk Gate Enable (SIDE_CLK_GATE_EN) — Offset 6Ch

Register for Side Clk Gate Enable.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Trunk Clk Gate (JTAG_FORCE_CLKREQ):** 0: Clk request enable 1: Clk is gated
0	0h RW	**Local Clk Gate (CG_CTRL_CLKGATEDEF):** 0: Clk is un-gated 1: Clk is gated

13.1.23 Received Data (DS_DATA_IN_DW2) — Offset 74h

Downstream Received Data Register DW2. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**Data Received (DATA_RECEIVED):** Data received in message. DW2.

13.1.24 DN Access Valid Enable (DS_ACCESS_VALID_EN) — Offset 80h

Downstream Access Valid Enable.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**DS_ACCESS_VALID_EN_RSVD:** Reserved
0	0h RW	**Access Valid Enable For DS (ACCESS_VALID_ENABLE):** Downstream messages PMC access valid Enable: This bit is set by ISH FW to enable SBEP HW to accept downstream cycles from PMC, Hammock Harbor ART agent, Audio, ISP, CSME, GPIO, DFX Trusted0 Red2, DFX Trusted1 Red4, DFX Trusted2 Orange and interrupt ISH upon such an event. Note that ISH HW chooses the SAI value corresponding to this agent. NOTE: If a BOOTPREP message is received, ISH FW is interrupted unconditionally, i.e. irrespective of this bit being 1 or 0.

13.1.25 Boot Prep Control (BOOT_PREP_CONTROL_REG) — Offset 84h

BOOT PREP CONTROL register. This register has only indirect write access from host and non-host agents.

Type	Size	Offset	Default
MMIO	32 bit	FDBE000h + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**Boot Prep Received Status (BOOT_PREP_RECEIVED_STATUS):** This bit is set by SBEP HW upon the reception of Boot Prep message. ISH FW is required to clear this status bit by writing 0, upon issuing Boot Prep Ack message on the upstream path of SBEP HW. SBEP HW will clear this bit, upon auto Ack ing of Boot Prep due to timeout condition.

14 Intel® PSE ARM Registers

This chapter documents Intel® PSE IP for ARM registers. The following table shows the memory map of the registers.

Intel® PSE ARM Address Map						
Section	**Region**	**Sub Region**	**Sub Region Size (KB)**	**Start Address**	**End Address**	**Region Size (MB)**
HBW Fabric	Code			0x00000000	0x20000000	512
		ICCM	512	0x00000000	0x00080000	
	Data			0x20000000	0x40000000	512
		DCCM	512	0x20000000	0x20080000	
Peripheral-0				0x40000000	0x48000000	128
	FABRIC		4	0x40000000	0x40100000	1
	I2C			0x40100000	0x40200000	1
		I2C0	4	0x40100000	0x40101000	
		I2C0_DEVIDLE	4	0x40101000	0x40102000	
		I2C1	4	0x40102000	0x40103000	
		I2C1_DEVIDLE	4	0x40103000	0x40104000	
		I2C2	4	0x40104000	0x40105000	
		I2C2_DEVIDLE	4	0x40105000	0x40106000	
		I2C3	4	0x40106000	0x40107000	
		I2C3_DEVIDLE	4	0x40107000	0x40108000	
		I2C4	4	0x40108000	0x40109000	
		I2C4_DEVIDLE	4	0x40109000	0x4010A000	
		I2C5	4	0x4010A000	0x4010B000	
		I2C5_DEVIDLE	4	0x4010B000	0x4010C000	
		I2C6	4	0x4010C000	0x4010D000	
		I2C6_DEVIDLE	4	0x4010D000	0x4010E000	
		I2C7	4	0x4010E000	0x4010F000	
		I2C7_DEVIDLE	4	0x4010F000	0x40110000	
	GPIO0			0x40200000	0x40300000	1

		GPIO0	4	0x40200000	0x40201000	
		TGPIO0	4	0x40201000	0x40202000	
		GPIO0_DEVIDLE	4	0x40202000	0x40203000	
	GPIO1			0x40300000	0x40400000	1
		GPIO1	4	0x40300000	0x40301000	
		TGPIO1	4	0x40301000	0x40302000	
		GPIO1_DEVIDLE	4	0x40302000	0x40303000	
	IPC			0x40400000	0x40500000	1
		Host	64	0x40400000	0x40410000	
		LH	4	0x40400000	0x40401000	
		Peer	64	0x40410000	0x40420000	
		PMC	4	0x40411000	0x40412000	
	PMU		1024	0x40500000	0x40600000	1
	CCU		4	0x40600000	0x40700000	1
	MISC		4	0x40700000	0x40800000	1
	SBEP		4	0x40800000	0x40900000	1
	DTF		4	0x40900000	0x40A00000	1
	HPET		4	0x40A00000	0x40B00000	1
	WDT		4	0x40B00000	0x40C00000	1
	LDO		4	0x40D00000	0x40E00000	1
	ATT		4	0x40E00000	0x40F00000	1
	OSE_PLL		4	0x41000000	0x41100000	1
Peripheral-1				0x48000000	0x50000000	128
	FABRIC			0x48000000	0x48100000	1

	SPI			0x48100000	0x48200000	1
		SPI0	4	0x48100000	0x48101000	
		SPI0_DEVIDLE	4	0x48101000	0x48102000	
		SPI1	4	0x48102000	0x48103000	
		SPI1_DEVIDLE	4	0x48103000	0x48104000	
		SPI2	4	0x48104000	0x48105000	
		SPI2_DEVIDLE	4	0x48105000	0x48106000	
		SPI3	4	0x48106000	0x48107000	
		SPI3_DEVIDLE	4	0x48107000	0x48108000	
	UART			0x48200000	0x48300000	1
		UART0	4	0x48200000	0x48201000	
		UART0_DEVIDLE	4	0x48201000	0x48202000	
		UART1	4	0x48202000	0x48203000	
		UART1_DEVIDLE	4	0x48203000	0x48204000	
		UART2	4	0x48204000	0x48205000	
		UART2_DEVIDLE	4	0x48205000	0x48206000	
		UART3	4	0x48206000	0x48207000	
		UART3_DEVIDLE	4	0x48207000	0x48208000	
		UART4	4	0x48208000	0x48209000	
		UART4_DEVIDLE	4	0x48209000	0x4820A000	
		UART5	4	0x4820A000	0x4820B000	
		UART5_DEVIDLE	4	0x4820B000	0x4820C000	
	I2S			0x48300000	0x48400000	1
		I2S0	4	0x48300000	0x48301000	
		I2S0_DEVIDLE	4	0x48301000	0x48302000	
		I2S0	4	0x48302000	0x48303000	
		I2S0_DEVIDLE	4	0x48303000	0x48304000	
	PWM			0x48400000	0x48500000	1
		PWM0	4	0x48400000	0x48401000	
		PWM1	4	0x48401000	0x48402000	
		PWM_DEVIDLE	4	0x48402000	0x48403000	
	QEP			0x48600000	0x48700000	1

		QEP0	4	0x48600000	0x48601000	
		QEP0_DEVIDLE	4	0x48601000	0x48602000	
		QEP1	4	0x48602000	0x48603000	
		QEP1_DEVIDLE	4	0x48603000	0x48604000	
		QEP2	4	0x48604000	0x48605000	
		QEP2_DEVIDLE	4	0x48605000	0x48606000	
		QEP3	4	0x48606000	0x48607000	
		QEP3_DEVIDLE	4	0x48607000	0x48608000	
HBW Fabric				0x50000000	0x58000000	128
	FABRIC		4	0x50000000	0x50100000	1
	DMA			0x50100000	0x50200000	1
		DMA0	4	0x50100000	0x50101000	
		DMA0_MISC_ DEVIDLE	4	0x50101000	0x50102000	
		DMA0_VMM_REGS	4	0x50102000	0x50103000	
		DMA1	4	0x50104000	0x50105000	
		DMA1_MISC_ DEVIDLE	4	0x50105000	0x50106000	
		DMA1_VMM_REGS	4	0x50106000	0x50107000	
		DMA2	4	0x50108000	0x50109000	
		DMA2_MISC_ DEVIDLE	4	0x50109000	0x5010A000	
		DMA2_VMM_REGS	4	0x5010A000	0x5010B000	
	GBE			0x50200000	0x50300000	1
		GBE0	64	0x50200000	0x50210000	
		GBE0_MISC_ DEVIDLE	64	0x50210000	0x50220000	
		GBE1	64	0x50220000	0x50230000	
		GBE1_MISC_ DEVIDLE	64	0x50230000	0x50240000	
	CAN			0x50300000	0x50400000	1
		CAN0	32	0x50300000	0x50308000	
		CAN0_DEVIDLE	32	0x50308000	0x50310000	
		CAN1	32	0x50310000	0x50318000	
		CAN1_DEVIDLE	32	0x50318000	0x50320000	

	SRAMC					
		SRAMC_REG	4	0x50400000	0x50500000	1
HBW Fabric	L2 SRAM			0x60000000	0x60200000	2
	AONRF		64	0x70000000	0x70010000	
	BROM		16	0x71000000	0x71004000	
	ATT (Reserved)			0x80000000	0x80C00000	12
HBW Fabric	IOSF2AXI-VC0	Up-Stream		0x100000000	0x200000000	4096
HBW Fabric	IOSF2AXI-VC1	Up-Stream		0x200000000	0x400000000	8192

14.1 I2C Interface Registers

There are eight I2C Interface registers:-

- I2C_0 Registers
- I2C_1 Registers

I2C Interface Registers	Address Offset	Table
I2C_0	40100000h - 401000FCh	Table 14-1
I2C_1	40102000h - 401020FCh	Table 14-2
I2C_2	40104000h - 401040FCh	Table 14-3
I2C_3	40106000h - 401060FCh	Table 14-4
I2C_4	40108000h - 401080FCh	Table 14-5
I2C_5	4010A000h - 4010A0FCh	Table 14-6
I2C_6	4010C000h - 4010C0FCh	Table 14-7
I2C_7	4010E000h - 4010E0FCh	Table 14-8

14.1.1 I2C_0 Registers Summary

Table 14-1. Summary of I2C_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40100000h	4	IC_CON	00000067h
40100004h	4	IC_TAR	00000055h
40100008h	4	IC_SAR	00000055h
4010000Ch	4	IC_HS_MADDR	00000001h
40100010h	4	IC_DATA_CMD	00000000h
40100014h	4	IC_SS_SCL_HCNT	000001E8h
40100018h	4	IC_SS_SCL_LCNT	000001F3h
4010001Ch	4	IC_FS_SCL_HCNT	00000071h
40100020h	4	IC_FS_SCL_LCNT	0000007Ch
40100024h	4	IC_HS_SCL_HCNT	00000029h
40100028h	4	IC_HS_SCL_LCNT	00000032h
4010002Ch	4	IC_INTR_STAT	00000000h
40100030h	4	IC_INTR_MASK	000008FFh
40100034h	4	IC_RAW_INTR_STAT	00000000h
40100038h	4	IC_RX_TL	00000000h
4010003Ch	4	IC_TX_TL	00000000h
40100040h	4	IC_CLR_INTR	00000000h
40100044h	4	IC_CLR_RX_UNDER	00000000h
40100048h	4	IC_CLR_RX_OVER	00000000h
4010004Ch	4	IC_CLR_TX_OVER	00000000h
40100050h	4	IC_CLR_RD_REQ	00000000h
40100054h	4	IC_CLR_TX_ABRT	00000000h
40100058h	4	IC_CLR_RX_DONE	00000000h
4010005Ch	4	IC_CLR_ACTIVITY	00000000h
40100060h	4	IC_CLR_STOP_DET	00000000h
40100064h	4	IC_CLR_START_DET	00000000h
40100068h	4	IC_CLR_GEN_CALL	00000000h
4010006Ch	4	IC_ENABLE	00000000h
40100070h	4	IC_STATUS	00000006h
40100074h	4	IC_TXFLR	00000000h
40100078h	4	IC_RXFLR	00000000h
4010007Ch	4	IC_SDA_HOLD	00000005h
40100080h	4	IC_TX_ABRT_SOURCE	00000000h
40100088h	4	IC_DMA_CR	00000000h
4010008Ch	4	IC_DMA_TDLR	00000000h
40100090h	4	IC_DMA_RDLR	00000000h
40100094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40100098h	4	IC_ACK_GENERAL_CALL	00000000h
4010009Ch	4	IC_ENABLE_STATUS	00000000h
401000A0h	4	IC_FS_SPKLEN	00000005h
401000A4h	4	IC_HS_SPKLEN	00000002h
401000A8h	4	IC_CLR_RESTART_DET	00000000h
401000F4h	4	IC_COMP_PARAM_1	003F3FEEh
401000F8h	4	IC_COMP_VERSION	3230322Ah
401000FCh	4	IC_COMP_TYPE	44570140h

14.1.1.1 IC_CON — Offset 40100000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	40100000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.1.2 IC_TAR — Offset 40100004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is

set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1).

Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	40100004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.1.3 IC_SAR — Offset 40100008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	40100008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.1.4 IC_HS_MADDR — Offset 4010000Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010000Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.1.5 IC_DATA_CMD — Offset 40100010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	40100010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.1.6 IC_SS_SCL_HCNT — Offset 40100014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40100014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.1.7 IC_SS_SCL_LCNT — Offset 40100018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40100018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.1.8 IC_FS_SCL_HCNT — Offset 4010001Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010001Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.1.9 IC_FS_SCL_LCNT — Offset 40100020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40100020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.1.10 IC_HS_SCL_HCNT — Offset 40100024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40100024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.1.11 IC_HS_SCL_LCNT — Offset 40100028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40100028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.1.12 IC_INTR_STAT — Offset 4010002Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010002Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.1.13 IC_INTR_MASK — Offset 40100030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	40100030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.1.14 IC_RAW_INTR_STAT — Offset 40100034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	40100034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.1.15 IC_RX_TL — Offset 40100038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	40100038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.1.16 IC_TX_TL — Offset 4010003Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.1.17 IC_CLR_INTR — Offset 40100040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.1.18 IC_CLR_RX_UNDER — Offset 40100044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.1.19 IC_CLR_RX_OVER — Offset 40100048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.1.20 IC_CLR_TX_OVER — Offset 4010004Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.1.21 IC_CLR_RD_REQ — Offset 40100050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.1.22 IC_CLR_TX_ABRT — Offset 40100054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.1.23 IC_CLR_RX_DONE — Offset 40100058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.1.24 IC_CLR_ACTIVITY — Offset 4010005Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.1.25 IC_CLR_STOP_DET — Offset 40100060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.1.26 IC_CLR_START_DET — Offset 40100064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.1.27 IC_CLR_GEN_CALL — Offset 40100068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40100068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.1.28 IC_ENABLE — Offset 4010006Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010006Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.1.29 IC_STATUS — Offset 40100070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	40100070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.1.30 IC_TXFLR — Offset 40100074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40100074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.1.31 IC_RXFLR — Offset 40100078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40100078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.1.32 IC_SDA_HOLD — Offset 4010007Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010007Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.1.33 IC_TX_ABRT_SOURCE — Offset 40100080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	40100080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.1.34 IC_DMA_CR — Offset 40100088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	40100088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.1.35 IC_DMA_TDLR — Offset 4010008Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010008Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.1.36 IC_DMA_RDLR — Offset 40100090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	40100090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.1.37 IC_SDA_SETUP — Offset 40100094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	40100094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.1.38 IC_ACK_GENERAL_CALL — Offset 40100098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	40100098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.1.39 IC_ENABLE_STATUS — Offset 4010009Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.1.40 IC_FS_SPKLEN — Offset 401000A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	401000A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.1.41 IC_HS_SPKLEN — Offset 401000A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	401000A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.1.42 IC_CLR_RESTART_DET — Offset 401000A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	401000A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.1.43 IC_COMP_PARAM_1 — Offset 401000F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	401000F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.1.44 IC_COMP_VERSION — Offset 401000F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	401000F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.1.45 IC_COMP_TYPE — Offset 401000FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	401000FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.2 I2C_1 Registers Summary

Table 14-2. Summary of I2C_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40102000h	4	IC_CON	00000067h
40102004h	4	IC_TAR	00000055h
40102008h	4	IC_SAR	00000055h
4010200Ch	4	IC_HS_MADDR	00000001h
40102010h	4	IC_DATA_CMD	00000000h
40102014h	4	IC_SS_SCL_HCNT	000001E8h
40102018h	4	IC_SS_SCL_LCNT	000001F3h
4010201Ch	4	IC_FS_SCL_HCNT	00000071h
40102020h	4	IC_FS_SCL_LCNT	0000007Ch
40102024h	4	IC_HS_SCL_HCNT	00000029h
40102028h	4	IC_HS_SCL_LCNT	00000032h
4010202Ch	4	IC_INTR_STAT	00000000h
40102030h	4	IC_INTR_MASK	000008FFh
40102034h	4	IC_RAW_INTR_STAT	00000000h
40102038h	4	IC_RX_TL	00000000h
4010203Ch	4	IC_TX_TL	00000000h
40102040h	4	IC_CLR_INTR	00000000h
40102044h	4	IC_CLR_RX_UNDER	00000000h
40102048h	4	IC_CLR_RX_OVER	00000000h
4010204Ch	4	IC_CLR_TX_OVER	00000000h
40102050h	4	IC_CLR_RD_REQ	00000000h
40102054h	4	IC_CLR_TX_ABRT	00000000h
40102058h	4	IC_CLR_RX_DONE	00000000h
4010205Ch	4	IC_CLR_ACTIVITY	00000000h
40102060h	4	IC_CLR_STOP_DET	00000000h
40102064h	4	IC_CLR_START_DET	00000000h
40102068h	4	IC_CLR_GEN_CALL	00000000h
4010206Ch	4	IC_ENABLE	00000000h
40102070h	4	IC_STATUS	00000006h
40102074h	4	IC_TXFLR	00000000h
40102078h	4	IC_RXFLR	00000000h
4010207Ch	4	IC_SDA_HOLD	00000005h
40102080h	4	IC_TX_ABRT_SOURCE	00000000h
40102088h	4	IC_DMA_CR	00000000h
4010208Ch	4	IC_DMA_TDLR	00000000h
40102090h	4	IC_DMA_RDLR	00000000h
40102094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40102098h	4	IC_ACK_GENERAL_CALL	00000000h
4010209Ch	4	IC_ENABLE_STATUS	00000000h
401020A0h	4	IC_FS_SPKLEN	00000005h
401020A4h	4	IC_HS_SPKLEN	00000002h
401020A8h	4	IC_CLR_RESTART_DET	00000000h
401020F4h	4	IC_COMP_PARAM_1	003F3FEEh
401020F8h	4	IC_COMP_VERSION	3230322Ah
401020FCh	4	IC_COMP_TYPE	44570140h

14.1.2.1 IC_CON — Offset 40102000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	40102000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.2.2 IC_TAR — Offset 40102004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	40102004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.2.3 IC_SAR — Offset 40102008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	40102008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.2.4 IC_HS_MADDR — Offset 4010200Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010200Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.2.5 IC_DATA_CMD — Offset 40102010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	40102010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.2.6 IC_SS_SCL_HCNT — Offset 40102014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40102014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.2.7 IC_SS_SCL_LCNT — Offset 40102018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40102018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.2.8 IC_FS_SCL_HCNT — Offset 4010201Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010201Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.2.9 IC_FS_SCL_LCNT — Offset 40102020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40102020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.2.10 IC_HS_SCL_HCNT — Offset 40102024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40102024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.2.11 IC_HS_SCL_LCNT — Offset 40102028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40102028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.2.12 IC_INTR_STAT — Offset 4010202Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010202Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.2.13 IC_INTR_MASK — Offset 40102030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	40102030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.2.14 IC_RAW_INTR_STAT — Offset 40102034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	40102034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.2.15 IC_RX_TL — Offset 40102038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	40102038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.2.16 IC_TX_TL — Offset 4010203Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010203Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.2.17 IC_CLR_INTR — Offset 40102040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.2.18 IC_CLR_RX_UNDER — Offset 40102044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.2.19 IC_CLR_RX_OVER — Offset 40102048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.2.20 IC_CLR_TX_OVER — Offset 4010204Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010204Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.2.21 IC_CLR_RD_REQ — Offset 40102050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.2.22 IC_CLR_TX_ABRT — Offset 40102054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.2.23 IC_CLR_RX_DONE — Offset 40102058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.2.24 IC_CLR_ACTIVITY — Offset 4010205Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010205Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.2.25 IC_CLR_STOP_DET — Offset 40102060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.2.26 IC_CLR_START_DET — Offset 40102064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.2.27 IC_CLR_GEN_CALL — Offset 40102068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40102068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.2.28 IC_ENABLE — Offset 4010206Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010206Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.2.29 IC_STATUS — Offset 40102070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	40102070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.2.30 IC_TXFLR — Offset 40102074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40102074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.2.31 IC_RXFLR — Offset 40102078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40102078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.2.32 IC_SDA_HOLD — Offset 4010207Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010207Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.2.33 IC_TX_ABRT_SOURCE — Offset 40102080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	40102080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.2.34 IC_DMA_CR — Offset 40102088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	40102088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.2.35 IC_DMA_TDLR — Offset 4010208Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010208Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.2.36 IC_DMA_RDLR — Offset 40102090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	40102090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.2.37 IC_SDA_SETUP — Offset 40102094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	40102094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.2.38 IC_ACK_GENERAL_CALL — Offset 40102098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	40102098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.2.39 IC_ENABLE_STATUS — Offset 4010209Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010209Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.2.40 IC_FS_SPKLEN — Offset 401020A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	401020A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.2.41 IC_HS_SPKLEN — Offset 401020A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	401020A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.2.42 IC_CLR_RESTART_DET — Offset 401020A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	401020A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.2.43 IC_COMP_PARAM_1 — Offset 401020F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	401020F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.2.44 IC_COMP_VERSION — Offset 401020F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	401020F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.2.45 IC_COMP_TYPE — Offset 401020FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	401020FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.3 I2C_2 Registers Summary

Table 14-3. Summary of I2C_2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40104000h	4	IC_CON	00000067h
40104004h	4	IC_TAR	00000055h
40104008h	4	IC_SAR	00000055h
4010400Ch	4	IC_HS_MADDR	00000001h
40104010h	4	IC_DATA_CMD	00000000h
40104014h	4	IC_SS_SCL_HCNT	000001E8h
40104018h	4	IC_SS_SCL_LCNT	000001F3h
4010401Ch	4	IC_FS_SCL_HCNT	00000071h
40104020h	4	IC_FS_SCL_LCNT	0000007Ch
40104024h	4	IC_HS_SCL_HCNT	00000029h
40104028h	4	IC_HS_SCL_LCNT	00000032h
4010402Ch	4	IC_INTR_STAT	00000000h
40104030h	4	IC_INTR_MASK	000008FFh
40104034h	4	IC_RAW_INTR_STAT	00000000h
40104038h	4	IC_RX_TL	00000000h
4010403Ch	4	IC_TX_TL	00000000h
40104040h	4	IC_CLR_INTR	00000000h
40104044h	4	IC_CLR_RX_UNDER	00000000h
40104048h	4	IC_CLR_RX_OVER	00000000h
4010404Ch	4	IC_CLR_TX_OVER	00000000h
40104050h	4	IC_CLR_RD_REQ	00000000h
40104054h	4	IC_CLR_TX_ABRT	00000000h
40104058h	4	IC_CLR_RX_DONE	00000000h
4010405Ch	4	IC_CLR_ACTIVITY	00000000h
40104060h	4	IC_CLR_STOP_DET	00000000h
40104064h	4	IC_CLR_START_DET	00000000h
40104068h	4	IC_CLR_GEN_CALL	00000000h
4010406Ch	4	IC_ENABLE	00000000h
40104070h	4	IC_STATUS	00000006h
40104074h	4	IC_TXFLR	00000000h
40104078h	4	IC_RXFLR	00000000h
4010407Ch	4	IC_SDA_HOLD	00000005h
40104080h	4	IC_TX_ABRT_SOURCE	00000000h
40104088h	4	IC_DMA_CR	00000000h
4010408Ch	4	IC_DMA_TDLR	00000000h
40104090h	4	IC_DMA_RDLR	00000000h
40104094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40104098h	4	IC_ACK_GENERAL_CALL	00000000h
4010409Ch	4	IC_ENABLE_STATUS	00000000h
401040A0h	4	IC_FS_SPKLEN	00000005h
401040A4h	4	IC_HS_SPKLEN	00000002h
401040A8h	4	IC_CLR_RESTART_DET	00000000h
401040F4h	4	IC_COMP_PARAM_1	003F3FEEh
401040F8h	4	IC_COMP_VERSION	3230322Ah
401040FCh	4	IC_COMP_TYPE	44570140h

14.1.3.1 IC_CON — Offset 40104000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	40104000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.3.2 IC_TAR — Offset 40104004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	40104004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.3.3 IC_SAR — Offset 40104008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	40104008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.3.4 IC_HS_MADDR — Offset 4010400Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010400Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.3.5 IC_DATA_CMD — Offset 40104010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	40104010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.3.6 IC_SS_SCL_HCNT — Offset 40104014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40104014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.3.7 IC_SS_SCL_LCNT — Offset 40104018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40104018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.3.8 IC_FS_SCL_HCNT — Offset 4010401Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010401Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.3.9 IC_FS_SCL_LCNT — Offset 40104020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40104020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.3.10 IC_HS_SCL_HCNT — Offset 40104024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40104024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.r The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.3.11 IC_HS_SCL_LCNT — Offset 40104028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40104028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.3.12 IC_INTR_STAT — Offset 4010402Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010402Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.3.13 IC_INTR_MASK — Offset 40104030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	40104030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.3.14 IC_RAW_INTR_STAT — Offset 40104034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	40104034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.3.15 IC_RX_TL — Offset 40104038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	40104038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.3.16 IC_TX_TL — Offset 4010403Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010403Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.3.17 IC_CLR_INTR — Offset 40104040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.3.18 IC_CLR_RX_UNDER — Offset 40104044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.3.19 IC_CLR_RX_OVER — Offset 40104048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.3.20 IC_CLR_TX_OVER — Offset 4010404Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010404Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.3.21 IC_CLR_RD_REQ — Offset 40104050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.3.22 IC_CLR_TX_ABRT — Offset 40104054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.3.23 IC_CLR_RX_DONE — Offset 40104058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.3.24 IC_CLR_ACTIVITY — Offset 4010405Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010405Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.3.25 IC_CLR_STOP_DET — Offset 40104060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.3.26 IC_CLR_START_DET — Offset 40104064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.3.27 IC_CLR_GEN_CALL — Offset 40104068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40104068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.3.28 IC_ENABLE — Offset 4010406Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010406Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation. For a detailed description on how to abort I2C transfers, refer to "Aborting I2C Transfers".
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.3.29 IC_STATUS — Offset 40104070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	40104070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.3.30 IC_TXFLR — Offset 40104074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40104074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.3.31 IC_RXFLR — Offset 40104078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40104078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.3.32 IC_SDA_HOLD — Offset 4010407Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010407Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.3.33 IC_TX_ABRT_SOURCE — Offset 40104080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	40104080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.3.34 IC_DMA_CR — Offset 40104088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	40104088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.3.35 IC_DMA_TDLR — Offset 4010408Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010408Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.3.36 IC_DMA_RDLR — Offset 40104090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	40104090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.3.37 IC_SDA_SETUP — Offset 40104094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	40104094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.3.38 IC_ACK_GENERAL_CALL — Offset 40104098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	40104098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.3.39 IC_ENABLE_STATUS — Offset 4010409Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010409Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.3.40 IC_FS_SPKLEN — Offset 401040A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	401040A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.3.41 IC_HS_SPKLEN — Offset 401040A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	401040A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.3.42 IC_CLR_RESTART_DET — Offset 401040A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	401040A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.3.43 IC_COMP_PARAM_1 — Offset 401040F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	401040F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.3.44 IC_COMP_VERSION — Offset 401040F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	401040F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.3.45 IC_COMP_TYPE — Offset 401040FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	401040FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.4 I2C_3 Registers Summary

Table 14-4. Summary of I2C_3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40106000h	4	IC_CON	00000067h
40106004h	4	IC_TAR	00000055h
40106008h	4	IC_SAR	00000055h
4010600Ch	4	IC_HS_MADDR	00000001h
40106010h	4	IC_DATA_CMD	00000000h
40106014h	4	IC_SS_SCL_HCNT	000001E8h
40106018h	4	IC_SS_SCL_LCNT	000001F3h
4010601Ch	4	IC_FS_SCL_HCNT	00000071h
40106020h	4	IC_FS_SCL_LCNT	0000007Ch
40106024h	4	IC_HS_SCL_HCNT	00000029h
40106028h	4	IC_HS_SCL_LCNT	00000032h
4010602Ch	4	IC_INTR_STAT	00000000h
40106030h	4	IC_INTR_MASK	000008FFh
40106034h	4	IC_RAW_INTR_STAT	00000000h
40106038h	4	IC_RX_TL	00000000h
4010603Ch	4	IC_TX_TL	00000000h
40106040h	4	IC_CLR_INTR	00000000h
40106044h	4	IC_CLR_RX_UNDER	00000000h
40106048h	4	IC_CLR_RX_OVER	00000000h
4010604Ch	4	IC_CLR_TX_OVER	00000000h
40106050h	4	IC_CLR_RD_REQ	00000000h
40106054h	4	IC_CLR_TX_ABRT	00000000h
40106058h	4	IC_CLR_RX_DONE	00000000h
4010605Ch	4	IC_CLR_ACTIVITY	00000000h
40106060h	4	IC_CLR_STOP_DET	00000000h
40106064h	4	IC_CLR_START_DET	00000000h
40106068h	4	IC_CLR_GEN_CALL	00000000h
4010606Ch	4	IC_ENABLE	00000000h
40106070h	4	IC_STATUS	00000006h
40106074h	4	IC_TXFLR	00000000h
40106078h	4	IC_RXFLR	00000000h
4010607Ch	4	IC_SDA_HOLD	00000005h
40106080h	4	IC_TX_ABRT_SOURCE	00000000h
40106088h	4	IC_DMA_CR	00000000h
4010608Ch	4	IC_DMA_TDLR	00000000h
40106090h	4	IC_DMA_RDLR	00000000h
40106094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40106098h	4	IC_ACK_GENERAL_CALL	00000000h
4010609Ch	4	IC_ENABLE_STATUS	00000000h
401060A0h	4	IC_FS_SPKLEN	00000005h
401060A4h	4	IC_HS_SPKLEN	00000002h
401060A8h	4	IC_CLR_RESTART_DET	00000000h
401060F4h	4	IC_COMP_PARAM_1	003F3FEEh
401060F8h	4	IC_COMP_VERSION	3230322Ah
401060FCh	4	IC_COMP_TYPE	44570140h

14.1.4.1 IC_CON — Offset 40106000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	40106000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.4.2 IC_TAR — Offset 40106004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	40106004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.4.3 IC_SAR — Offset 40106008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	40106008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.4.4 IC_HS_MADDR — Offset 4010600Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010600Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.4.5 IC_DATA_CMD — Offset 40106010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	40106010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.4.6 IC_SS_SCL_HCNT — Offset 40106014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40106014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.4.7 IC_SS_SCL_LCNT — Offset 40106018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40106018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.4.8 IC_FS_SCL_HCNT — Offset 4010601Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010601Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.4.9 IC_FS_SCL_LCNT — Offset 40106020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40106020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.4.10 IC_HS_SCL_HCNT — Offset 40106024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40106024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.4.11 IC_HS_SCL_LCNT — Offset 40106028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40106028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.4.12 IC_INTR_STAT — Offset 4010602Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010602Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.4.13 IC_INTR_MASK — Offset 40106030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	40106030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.4.14 IC_RAW_INTR_STAT — Offset 40106034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	40106034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.4.15 IC_RX_TL — Offset 40106038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	40106038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.4.16 IC_TX_TL — Offset 4010603Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010603Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.4.17 IC_CLR_INTR — Offset 40106040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.4.18 IC_CLR_RX_UNDER — Offset 40106044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.4.19 IC_CLR_RX_OVER — Offset 40106048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.4.20 IC_CLR_TX_OVER — Offset 4010604Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010604Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.4.21 IC_CLR_RD_REQ — Offset 40106050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.4.22 IC_CLR_TX_ABRT — Offset 40106054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.4.23 IC_CLR_RX_DONE — Offset 40106058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.4.24 IC_CLR_ACTIVITY — Offset 4010605Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010605Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.4.25 IC_CLR_STOP_DET — Offset 40106060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.4.26 IC_CLR_START_DET — Offset 40106064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.4.27 IC_CLR_GEN_CALL — Offset 40106068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40106068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.4.28 IC_ENABLE — Offset 4010606Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010606Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.4.29 IC_STATUS — Offset 40106070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	40106070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.4.30 IC_TXFLR — Offset 40106074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40106074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.4.31 IC_RXFLR — Offset 40106078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40106078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.4.32 IC_SDA_HOLD — Offset 4010607Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010607Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.4.33 IC_TX_ABRT_SOURCE — Offset 40106080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	40106080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.4.34 IC_DMA_CR — Offset 40106088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	40106088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.4.35 IC_DMA_TDLR — Offset 4010608Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010608Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.4.36 IC_DMA_RDLR — Offset 40106090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	40106090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.4.37 IC_SDA_SETUP — Offset 40106094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	40106094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.4.38 IC_ACK_GENERAL_CALL — Offset 40106098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	40106098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.4.39 IC_ENABLE_STATUS — Offset 4010609Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010609Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.4.40 IC_FS_SPKLEN — Offset 401060A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	401060A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.4.41 IC_HS_SPKLEN — Offset 401060A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	401060A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.4.42 IC_CLR_RESTART_DET — Offset 401060A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	401060A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.4.43 IC_COMP_PARAM_1 — Offset 401060F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	401060F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.4.44 IC_COMP_VERSION — Offset 401060F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	401060F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.4.45 IC_COMP_TYPE — Offset 401060FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	401060FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.5 I2C_4 Registers Summary

Table 14-5. Summary of I2C_4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40108000h	4	IC_CON	00000067h
40108004h	4	IC_TAR	00000055h
40108008h	4	IC_SAR	00000055h
4010800Ch	4	IC_HS_MADDR	00000001h
40108010h	4	IC_DATA_CMD	00000000h
40108014h	4	IC_SS_SCL_HCNT	000001E8h
40108018h	4	IC_SS_SCL_LCNT	000001F3h
4010801Ch	4	IC_FS_SCL_HCNT	00000071h
40108020h	4	IC_FS_SCL_LCNT	0000007Ch
40108024h	4	IC_HS_SCL_HCNT	00000029h
40108028h	4	IC_HS_SCL_LCNT	00000032h
4010802Ch	4	IC_INTR_STAT	00000000h
40108030h	4	IC_INTR_MASK	000008FFh
40108034h	4	IC_RAW_INTR_STAT	00000000h
40108038h	4	IC_RX_TL	00000000h
4010803Ch	4	IC_TX_TL	00000000h
40108040h	4	IC_CLR_INTR	00000000h
40108044h	4	IC_CLR_RX_UNDER	00000000h
40108048h	4	IC_CLR_RX_OVER	00000000h
4010804Ch	4	IC_CLR_TX_OVER	00000000h
40108050h	4	IC_CLR_RD_REQ	00000000h
40108054h	4	IC_CLR_TX_ABRT	00000000h
40108058h	4	IC_CLR_RX_DONE	00000000h
4010805Ch	4	IC_CLR_ACTIVITY	00000000h
40108060h	4	IC_CLR_STOP_DET	00000000h
40108064h	4	IC_CLR_START_DET	00000000h
40108068h	4	IC_CLR_GEN_CALL	00000000h
4010806Ch	4	IC_ENABLE	00000000h
40108070h	4	IC_STATUS	00000006h
40108074h	4	IC_TXFLR	00000000h
40108078h	4	IC_RXFLR	00000000h
4010807Ch	4	IC_SDA_HOLD	00000005h
40108080h	4	IC_TX_ABRT_SOURCE	00000000h
40108088h	4	IC_DMA_CR	00000000h
4010808Ch	4	IC_DMA_TDLR	00000000h
40108090h	4	IC_DMA_RDLR	00000000h
40108094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40108098h	4	IC_ACK_GENERAL_CALL	00000000h
4010809Ch	4	IC_ENABLE_STATUS	00000000h
401080A0h	4	IC_FS_SPKLEN	00000005h
401080A4h	4	IC_HS_SPKLEN	00000002h
401080A8h	4	IC_CLR_RESTART_DET	00000000h
401080F4h	4	IC_COMP_PARAM_1	003F3FEEh
401080F8h	4	IC_COMP_VERSION	3230322Ah
401080FCh	4	IC_COMP_TYPE	44570140h

14.1.5.1 IC_CON — Offset 40108000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	40108000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.5.2 IC_TAR — Offset 40108004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	40108004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.5.3 IC_SAR — Offset 40108008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	40108008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.5.4 IC_HS_MADDR — Offset 4010800Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010800Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.5.5 IC_DATA_CMD — Offset 40108010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	40108010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.5.6 IC_SS_SCL_HCNT — Offset 40108014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40108014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.5.7 IC_SS_SCL_LCNT — Offset 40108018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40108018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.5.8 IC_FS_SCL_HCNT — Offset 4010801Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010801Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.5.9 IC_FS_SCL_LCNT — Offset 40108020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40108020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.5.10 IC_HS_SCL_HCNT — Offset 40108024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	40108024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.5.11 IC_HS_SCL_LCNT — Offset 40108028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	40108028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.5.12 IC_INTR_STAT — Offset 4010802Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010802Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.5.13 IC_INTR_MASK — Offset 40108030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	40108030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.5.14 IC_RAW_INTR_STAT — Offset 40108034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	40108034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.5.15 IC_RX_TL — Offset 40108038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	40108038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.5.16 IC_TX_TL — Offset 4010803Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010803Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.5.17 IC_CLR_INTR — Offset 40108040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.5.18 IC_CLR_RX_UNDER — Offset 40108044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.5.19 IC_CLR_RX_OVER — Offset 40108048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.5.20 IC_CLR_TX_OVER — Offset 4010804Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010804Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.5.21 IC_CLR_RD_REQ — Offset 40108050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.5.22 IC_CLR_TX_ABRT — Offset 40108054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.5.23 IC_CLR_RX_DONE — Offset 40108058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.5.24 IC_CLR_ACTIVITY — Offset 4010805Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010805Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.5.25 IC_CLR_STOP_DET — Offset 40108060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.5.26 IC_CLR_START_DET — Offset 40108064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.5.27 IC_CLR_GEN_CALL — Offset 40108068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	40108068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.5.28 IC_ENABLE — Offset 4010806Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010806Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.5.29 IC_STATUS — Offset 40108070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	40108070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.5.30 IC_TXFLR — Offset 40108074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40108074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.5.31 IC_RXFLR — Offset 40108078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	40108078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.5.32 IC_SDA_HOLD — Offset 4010807Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010807Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.5.33 IC_TX_ABRT_SOURCE — Offset 40108080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	40108080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.5.34 IC_DMA_CR — Offset 40108088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	40108088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.5.35 IC_DMA_TDLR — Offset 4010808Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010808Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.5.36 IC_DMA_RDLR — Offset 40108090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	40108090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.5.37 IC_SDA_SETUP — Offset 40108094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	40108094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.5.38 IC_ACK_GENERAL_CALL — Offset 40108098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	40108098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.5.39 IC_ENABLE_STATUS — Offset 4010809Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010809Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.5.40 IC_FS_SPKLEN — Offset 401080A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	401080A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.5.41 IC_HS_SPKLEN — Offset 401080A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	401080A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.5.42 IC_CLR_RESTART_DET — Offset 401080A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	401080A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.5.43 IC_COMP_PARAM_1 — Offset 401080F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	401080F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.5.44 IC_COMP_VERSION — Offset 401080F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	401080F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.5.45 IC_COMP_TYPE — Offset 401080FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	401080FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.6 I2C_5 Registers Summary

Table 14-6. Summary of I2C_5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4010A000h	4	IC_CON	00000067h
4010A004h	4	IC_TAR	00000055h
4010A008h	4	IC_SAR	00000055h
4010A00Ch	4	IC_HS_MADDR	00000001h
4010A010h	4	IC_DATA_CMD	00000000h
4010A014h	4	IC_SS_SCL_HCNT	000001E8h
4010A018h	4	IC_SS_SCL_LCNT	000001F3h
4010A01Ch	4	IC_FS_SCL_HCNT	00000071h
4010A020h	4	IC_FS_SCL_LCNT	0000007Ch
4010A024h	4	IC_HS_SCL_HCNT	00000029h
4010A028h	4	IC_HS_SCL_LCNT	00000032h
4010A02Ch	4	IC_INTR_STAT	00000000h
4010A030h	4	IC_INTR_MASK	000008FFh
4010A034h	4	IC_RAW_INTR_STAT	00000000h
4010A038h	4	IC_RX_TL	00000000h
4010A03Ch	4	IC_TX_TL	00000000h
4010A040h	4	IC_CLR_INTR	00000000h
4010A044h	4	IC_CLR_RX_UNDER	00000000h
4010A048h	4	IC_CLR_RX_OVER	00000000h
4010A04Ch	4	IC_CLR_TX_OVER	00000000h
4010A050h	4	IC_CLR_RD_REQ	00000000h
4010A054h	4	IC_CLR_TX_ABRT	00000000h
4010A058h	4	IC_CLR_RX_DONE	00000000h
4010A05Ch	4	IC_CLR_ACTIVITY	00000000h
4010A060h	4	IC_CLR_STOP_DET	00000000h
4010A064h	4	IC_CLR_START_DET	00000000h
4010A068h	4	IC_CLR_GEN_CALL	00000000h
4010A06Ch	4	IC_ENABLE	00000000h
4010A070h	4	IC_STATUS	00000006h
4010A074h	4	IC_TXFLR	00000000h
4010A078h	4	IC_RXFLR	00000000h
4010A07Ch	4	IC_SDA_HOLD	00000005h
4010A080h	4	IC_TX_ABRT_SOURCE	00000000h
4010A088h	4	IC_DMA_CR	00000000h
4010A08Ch	4	IC_DMA_TDLR	00000000h
4010A090h	4	IC_DMA_RDLR	00000000h
4010A094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4010A098h	4	IC_ACK_GENERAL_CALL	00000000h
4010A09Ch	4	IC_ENABLE_STATUS	00000000h
4010A0A0h	4	IC_FS_SPKLEN	00000005h
4010A0A4h	4	IC_HS_SPKLEN	00000002h
4010A0A8h	4	IC_CLR_RESTART_DET	00000000h
4010A0F4h	4	IC_COMP_PARAM_1	003F3FEEh
4010A0F8h	4	IC_COMP_VERSION	3230322Ah
4010A0FCh	4	IC_COMP_TYPE	44570140h

14.1.6.1 IC_CON — Offset 4010A000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	4010A000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.6.2 IC_TAR — Offset 4010A004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	4010A004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.6.3 IC_SAR — Offset 4010A008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010A008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.6.4 IC_HS_MADDR — Offset 4010A00Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010A00Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.6.5 IC_DATA_CMD — Offset 4010A010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	4010A010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.6.6 IC_SS_SCL_HCNT — Offset 4010A014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010A014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.6.7 IC_SS_SCL_LCNT — Offset 4010A018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010A018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.6.8 IC_FS_SCL_HCNT — Offset 4010A01Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010A01Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.6.9 IC_FS_SCL_LCNT — Offset 4010A020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010A020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.6.10 IC_HS_SCL_HCNT — Offset 4010A024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010A024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.6.11 IC_HS_SCL_LCNT — Offset 4010A028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010A028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.6.12 IC_INTR_STAT — Offset 4010A02Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010A02Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.6.13 IC_INTR_MASK — Offset 4010A030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	4010A030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.6.14 IC_RAW_INTR_STAT — Offset 4010A034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	4010A034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.6.15 IC_RX_TL — Offset 4010A038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010A038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.6.16 IC_TX_TL — Offset 4010A03Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010A03Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.6.17 IC_CLR_INTR — Offset 4010A040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.6.18 IC_CLR_RX_UNDER — Offset 4010A044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.6.19 IC_CLR_RX_OVER — Offset 4010A048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.6.20 IC_CLR_TX_OVER — Offset 4010A04Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A04Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.6.21 IC_CLR_RD_REQ — Offset 4010A050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.6.22 IC_CLR_TX_ABRT — Offset 4010A054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.6.23 IC_CLR_RX_DONE — Offset 4010A058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.6.24 IC_CLR_ACTIVITY — Offset 4010A05Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A05Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.6.25 IC_CLR_STOP_DET — Offset 4010A060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.6.26 IC_CLR_START_DET — Offset 4010A064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.6.27 IC_CLR_GEN_CALL — Offset 4010A068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.6.28 IC_ENABLE — Offset 4010A06Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010A06Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.6.29 IC_STATUS — Offset 4010A070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	4010A070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.6.30 IC_TXFLR — Offset 4010A074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	4010A074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.6.31 IC_RXFLR — Offset 4010A078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	4010A078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.6.32 IC_SDA_HOLD — Offset 4010A07Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010A07Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.6.33 IC_TX_ABRT_SOURCE — Offset 4010A080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	4010A080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.6.34 IC_DMA_CR — Offset 4010A088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	4010A088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.6.35 IC_DMA_TDLR — Offset 4010A08Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010A08Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.6.36 IC_DMA_RDLR — Offset 4010A090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010A090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.6.37 IC_SDA_SETUP — Offset 4010A094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	4010A094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.6.38 IC_ACK_GENERAL_CALL — Offset 4010A098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	4010A098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.6.39 IC_ENABLE_STATUS — Offset 4010A09Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010A09Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.6.40 IC_FS_SPKLEN — Offset 4010A0A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	4010A0A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.6.41 IC_HS_SPKLEN — Offset 4010A0A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	4010A0A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.6.42 IC_CLR_RESTART_DET — Offset 4010A0A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010A0A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.6.43 IC_COMP_PARAM_1 — Offset 4010A0F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	4010A0F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.6.44 IC_COMP_VERSION — Offset 4010A0F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	4010A0F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.6.45 IC_COMP_TYPE — Offset 4010A0FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	4010A0FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.7 I2C_6 Registers Summary

Table 14-7. Summary of I2C_6 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4010C000h	4	IC_CON	00000067h
4010C004h	4	IC_TAR	00000055h
4010C008h	4	IC_SAR	00000055h
4010C00Ch	4	IC_HS_MADDR	00000001h
4010C010h	4	IC_DATA_CMD	00000000h
4010C014h	4	IC_SS_SCL_HCNT	000001E8h
4010C018h	4	IC_SS_SCL_LCNT	000001F3h
4010C01Ch	4	IC_FS_SCL_HCNT	00000071h
4010C020h	4	IC_FS_SCL_LCNT	0000007Ch
4010C024h	4	IC_HS_SCL_HCNT	00000029h
4010C028h	4	IC_HS_SCL_LCNT	00000032h
4010C02Ch	4	IC_INTR_STAT	00000000h
4010C030h	4	IC_INTR_MASK	000008FFh
4010C034h	4	IC_RAW_INTR_STAT	00000000h
4010C038h	4	IC_RX_TL	00000000h
4010C03Ch	4	IC_TX_TL	00000000h
4010C040h	4	IC_CLR_INTR	00000000h
4010C044h	4	IC_CLR_RX_UNDER	00000000h
4010C048h	4	IC_CLR_RX_OVER	00000000h
4010C04Ch	4	IC_CLR_TX_OVER	00000000h
4010C050h	4	IC_CLR_RD_REQ	00000000h
4010C054h	4	IC_CLR_TX_ABRT	00000000h
4010C058h	4	IC_CLR_RX_DONE	00000000h
4010C05Ch	4	IC_CLR_ACTIVITY	00000000h
4010C060h	4	IC_CLR_STOP_DET	00000000h
4010C064h	4	IC_CLR_START_DET	00000000h
4010C068h	4	IC_CLR_GEN_CALL	00000000h
4010C06Ch	4	IC_ENABLE	00000000h
4010C070h	4	IC_STATUS	00000006h
4010C074h	4	IC_TXFLR	00000000h
4010C078h	4	IC_RXFLR	00000000h
4010C07Ch	4	IC_SDA_HOLD	00000005h
4010C080h	4	IC_TX_ABRT_SOURCE	00000000h
4010C088h	4	IC_DMA_CR	00000000h
4010C08Ch	4	IC_DMA_TDLR	00000000h
4010C090h	4	IC_DMA_RDLR	00000000h
4010C094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4010C098h	4	IC_ACK_GENERAL_CALL	00000000h
4010C09Ch	4	IC_ENABLE_STATUS	00000000h
4010C0A0h	4	IC_FS_SPKLEN	00000005h
4010C0A4h	4	IC_HS_SPKLEN	00000002h
4010C0A8h	4	IC_CLR_RESTART_DET	00000000h
4010C0F4h	4	IC_COMP_PARAM_1	003F3FEEh
4010C0F8h	4	IC_COMP_VERSION	3230322Ah
4010C0FCh	4	IC_COMP_TYPE	44570140h

14.1.7.1 IC_CON — Offset 4010C000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	4010C000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.7.2 IC_TAR — Offset 4010C004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	4010C004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.7.3 IC_SAR — Offset 4010C008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010C008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.7.4 IC_HS_MADDR — Offset 4010C00Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010C00Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.7.5 IC_DATA_CMD — Offset 4010C010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	4010C010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.7.6 IC_SS_SCL_HCNT — Offset 4010C014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010C014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.7.7 IC_SS_SCL_LCNT — Offset 4010C018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010C018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.7.8 IC_FS_SCL_HCNT — Offset 4010C01Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010C01Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.7.9 IC_FS_SCL_LCNT — Offset 4010C020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010C020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.7.10 IC_HS_SCL_HCNT — Offset 4010C024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010C024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed.The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.7.11 IC_HS_SCL_LCNT — Offset 4010C028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010C028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.7.12 IC_INTR_STAT — Offset 4010C02Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010C02Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.7.13 IC_INTR_MASK — Offset 4010C030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	4010C030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.7.14 IC_RAW_INTR_STAT — Offset 4010C034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	4010C034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.7.15 IC_RX_TL — Offset 4010C038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010C038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.7.16 IC_TX_TL — Offset 4010C03Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010C03Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.7.17 IC_CLR_INTR — Offset 4010C040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.7.18 IC_CLR_RX_UNDER — Offset 4010C044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.7.19 IC_CLR_RX_OVER — Offset 4010C048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.7.20 IC_CLR_TX_OVER — Offset 4010C04Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C04Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.7.21 IC_CLR_RD_REQ — Offset 4010C050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.7.22 IC_CLR_TX_ABRT — Offset 4010C054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.7.23 IC_CLR_RX_DONE — Offset 4010C058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.7.24 IC_CLR_ACTIVITY — Offset 4010C05Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C05Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.7.25 IC_CLR_STOP_DET — Offset 4010C060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.7.26 IC_CLR_START_DET — Offset 4010C064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.7.27 IC_CLR_GEN_CALL — Offset 4010C068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.7.28 IC_ENABLE — Offset 4010C06Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010C06Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.7.29 IC_STATUS — Offset 4010C070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	4010C070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.7.30 IC_TXFLR — Offset 4010C074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	4010C074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.7.31 IC_RXFLR — Offset 4010C078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	4010C078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.7.32 IC_SDA_HOLD — Offset 4010C07Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010C07Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.7.33 IC_TX_ABRT_SOURCE — Offset 4010C080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	4010C080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.7.34 IC_DMA_CR — Offset 4010C088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	4010C088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.7.35 IC_DMA_TDLR — Offset 4010C08Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010C08Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.7.36 IC_DMA_RDLR — Offset 4010C090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010C090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.7.37 IC_SDA_SETUP — Offset 4010C094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	4010C094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.7.38 IC_ACK_GENERAL_CALL — Offset 4010C098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	4010C098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.7.39 IC_ENABLE_STATUS — Offset 4010C09Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010C09Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.7.40 IC_FS_SPKLEN — Offset 4010C0A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	4010C0A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.7.41 IC_HS_SPKLEN — Offset 4010C0A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	4010C0A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.7.42 IC_CLR_RESTART_DET — Offset 4010C0A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010C0A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.7.43 IC_COMP_PARAM_1 — Offset 4010C0F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	4010C0F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.7.44 IC_COMP_VERSION — Offset 4010C0F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	4010C0F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.7.45 IC_COMP_TYPE — Offset 4010C0FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	4010C0FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.1.8 I2C_7 Registers Summary

Table 14-8. Summary of I2C_7 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4010E000h	4	IC_CON	00000067h
4010E004h	4	IC_TAR	00000055h
4010E008h	4	IC_SAR	00000055h
4010E00Ch	4	IC_HS_MADDR	00000001h
4010E010h	4	IC_DATA_CMD	00000000h
4010E014h	4	IC_SS_SCL_HCNT	000001E8h
4010E018h	4	IC_SS_SCL_LCNT	000001F3h
4010E01Ch	4	IC_FS_SCL_HCNT	00000071h
4010E020h	4	IC_FS_SCL_LCNT	0000007Ch
4010E024h	4	IC_HS_SCL_HCNT	00000029h
4010E028h	4	IC_HS_SCL_LCNT	00000032h
4010E02Ch	4	IC_INTR_STAT	00000000h
4010E030h	4	IC_INTR_MASK	000008FFh
4010E034h	4	IC_RAW_INTR_STAT	00000000h
4010E038h	4	IC_RX_TL	00000000h
4010E03Ch	4	IC_TX_TL	00000000h
4010E040h	4	IC_CLR_INTR	00000000h
4010E044h	4	IC_CLR_RX_UNDER	00000000h
4010E048h	4	IC_CLR_RX_OVER	00000000h
4010E04Ch	4	IC_CLR_TX_OVER	00000000h
4010E050h	4	IC_CLR_RD_REQ	00000000h
4010E054h	4	IC_CLR_TX_ABRT	00000000h
4010E058h	4	IC_CLR_RX_DONE	00000000h
4010E05Ch	4	IC_CLR_ACTIVITY	00000000h
4010E060h	4	IC_CLR_STOP_DET	00000000h
4010E064h	4	IC_CLR_START_DET	00000000h
4010E068h	4	IC_CLR_GEN_CALL	00000000h
4010E06Ch	4	IC_ENABLE	00000000h
4010E070h	4	IC_STATUS	00000006h
4010E074h	4	IC_TXFLR	00000000h
4010E078h	4	IC_RXFLR	00000000h
4010E07Ch	4	IC_SDA_HOLD	00000005h
4010E080h	4	IC_TX_ABRT_SOURCE	00000000h
4010E088h	4	IC_DMA_CR	00000000h
4010E08Ch	4	IC_DMA_TDLR	00000000h
4010E090h	4	IC_DMA_RDLR	00000000h
4010E094h	4	IC_SDA_SETUP	00000002h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4010E098h	4	IC_ACK_GENERAL_CALL	00000000h
4010E09Ch	4	IC_ENABLE_STATUS	00000000h
4010E0A0h	4	IC_FS_SPKLEN	00000005h
4010E0A4h	4	IC_HS_SPKLEN	00000002h
4010E0A8h	4	IC_CLR_RESTART_DET	00000000h
4010E0F4h	4	IC_COMP_PARAM_1	003F3FEEh
4010E0F8h	4	IC_COMP_VERSION	3230322Ah
4010E0FCh	4	IC_COMP_TYPE	44570140h

14.1.8.1 IC_CON — Offset 4010E000h

I2C Control Register - I2C Control Register. This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Read/Write Access: - If configuration parameter I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. - If configuration parameter IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. - If configuration parameter IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. - If configuration parameter IC_BUS_CLEAR_FEATURE=0, bit 11 is read only - If configuration parameter IC_OPTIONAL_SAR=0, bit 16 is read only - If configuration parameter IC_SMBUS=0, bit 17 is read only - If configuration parameter IC_SMBUS_ARP=0, bits 18 and 19 are read only.

Type	Size	Offset	Default
MMIO	32 bit	4010E000h	00000067h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**STOP_DET_IF_MASTER_ACTIVE:** In Master mode: - 1'b1: issues the STOP_DET interrupt only when master is active. - 1'b0: issues the STOP_DET irrespective of whether master is active or not.
9	0h RW	**RX_FIFO_FULL_HLD_CTRL:** This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.
8	0h RW	**TX_EMPTY_CTRL:** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**STOP_DET_IFADDRESSED:** In slave mode: - 1'b1: issues the STOP_DET interrrupt only when it is addressed. - 0'b0: issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with a 0.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: - Sending a START BYTE - Performing any high-speed mode operation - High-speed mode operation - Performing direction changes in combined format mode - Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. .
4	0h RO/V	**IC_10BITADDR_MASTER_RD_ONLY:** If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 'No' (0), this bit is named IC_10BITADDR_MASTER and controls whether the DW_apb_i2c starts its transfers in 7 or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE is set to 'Yes' (1), the function of this bit is handled by bit 12 of IC_TAR register, and becomes a read-only copy called IC_10BITADDR_MASTER_rd_only. - 0: 7-bit addressing - 1: 10-bit addressing
3	0h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. - 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. - 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE. 1: standard mode (100 kbit/s) 2: fast mode (<=400 kbit/s) or fast mode plus (<=1000Kbit/s) 3: high speed mode (3.4 Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE=1
0	1h RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with '1' then bit 6 should also be written with a '1'.

14.1.8.2 IC_TAR — Offset 4010E004h

I2C Target Address Register - I2C Target Address Register If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0. However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13

bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true: - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the TX FIFO (IC_STATUS[2]=1) You can change the TAR address dynamically without losing the bus, only if the following conditions are met. - DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1). Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0). - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Type	Size	Offset	Default
MMIO	32 bit	4010E004h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. - 0: 7-bit addressing - 1: 10-bit addressing
11	0h RW	**SPECIAL:** This bit indicates whether software performs a Device-ID or General Call or START BYTE command. - 0: ignore bit 10 GC_OR_START and use IC_TAR normally - 1: perform special I2C command as specified in Device_ID or GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. - 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. - 1: START BYTE
9:0	055h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

14.1.8.3 IC_SAR — Offset 4010E008h

I2C Slave Address Register - I2C Slave Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010E008h	00000055h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	055h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value.

14.1.8.4 IC_HS_MADDR — Offset 4010E00Ch

I2C High Speed Master Mode Code Address Register - I2C High Speed Master Mode Code Address Register

Type	Size	Offset	Default
MMIO	32 bit	4010E00Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.

14.1.8.5 IC_DATA_CMD — Offset 4010E010h

I2C Rx/Tx Data Buffer and Command Register - I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO. The size of the register changes as follows: Write: - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 Read: - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

Type	Size	Offset	Default
MMIO	32 bit	4010E010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**FIRST_DATA_BYTE:** Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode. NOTE: In case of APB_DATA_WIDTH=8, 1. The user has to perform two APB Reads to IC_DATA_CMD in order to get status on 11 bit. 2. Inorder to read the 11 bit, the user has to perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) in order to know the status of 11 bit (whether the data received in previous read is a first data byte or not). 3. The 11th bit is an optional read field, user can ignore 2nd byte read [15:8] (offset 0x11) if not interested in FIRST_DATA_BYTE status.
10	0h WO	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 - If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 - If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP:** This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. - 1 - STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. - 0 - STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	00h RW/V	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

14.1.8.6 IC_SS_SCL_HCNT — Offset 4010E014h

Standard Speed I2C Clock SCL High Count Register - Standard Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010E014h	000001E8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01E8h RW	**IC_SS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

14.1.8.7 IC_SS_SCL_LCNT — Offset 4010E018h

Standard Speed I2C Clock SCL Low Count Register - Standard Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010E018h	000001F3h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	01F3h RW	**IC_SS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.8.8 IC_FS_SCL_HCNT — Offset 4010E01Ch

Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010E01Ch	00000071h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0071h RW	**IC_FS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. F This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.8.9 IC_FS_SCL_LCNT — Offset 4010E020h

Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register - Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010E020h	0000007Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	007Ch RW	**IC_FS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

14.1.8.10 IC_HS_SCL_HCNT — Offset 4010E024h

High Speed I2C Clock SCL High Count Register - High Speed I2C Clock SCL High Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010E024h	00000029h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0029h RW	**IC_HS_SCL_HCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.

14.1.8.11 IC_HS_SCL_LCNT — Offset 4010E028h

High Speed I2C Clock SCL Low Count Register - High Speed I2C Clock SCL Low Count Register

Type	Size	Offset	Default
MMIO	32 bit	4010E028h	00000032h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0032h RW	**IC_HS_SCL_LCNT:** This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.

14.1.8.12 IC_INTR_STAT — Offset 4010E02Ch

I2C Interrupt Status Register - I2C Interrupt Status Register Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Type	Size	Offset	Default
MMIO	32 bit	4010E02Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**R_MASTER_ON_HOLD:** See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit.
12	0h RO/V	**R_RESTART_DET:** See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit.
11	0h RO/V	**R_GEN_CALL:** See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**R_START_DET:** See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit.
9	0h RO/V	**R_STOP_DET:** See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit.
8	0h RO/V	**R_ACTIVITY:** See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit.
7	0h RO/V	**R_RX_DONE:** See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit.
6	0h RO/V	**R_TX_ABRT:** See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit.
5	0h RO/V	**R_RD_REQ:** See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit.
4	0h RO/V	**R_TX_EMPTY:** See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit.
3	0h RO/V	**R_TX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit.
2	0h RO/V	**R_RX_FULL:** See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit.
1	0h RO/V	**R_RX_OVER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit.
0	0h RO/V	**R_RX_UNDER:** See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit.

14.1.8.13 IC_INTR_MASK — Offset 4010E030h

I2C Interrupt Mask Register - I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

Type	Size	Offset	Default
MMIO	32 bit	4010E030h	000008FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**M_MASTER_ON_HOLD:** This bit masks the R_MASTER_ON_HOLD interrupt in IC_INTR_STAT register.
12	0h RW	**M_RESTART_DET:** This bit masks the R_RESTART_DET interrupt in IC_INTR_STAT register.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register.
10	0h RW	**M_START_DET:** This bit masks the R_START_DET interrupt in IC_INTR_STAT register.
9	0h RW	**M_STOP_DET:** This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register.
8	0h RW	**M_ACTIVITY:** This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register.
7	1h RW	**M_RX_DONE:** This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register.
6	1h RW	**M_TX_ABRT:** This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register.
5	1h RW	**M_RD_REQ:** This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register.
4	1h RW	**M_TX_EMPTY:** This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register.
3	1h RW	**M_TX_OVER:** This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register.
2	1h RW	**M_RX_FULL:** This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register.
1	1h RW	**M_RX_OVER:** This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register.
0	1h RW	**M_RX_UNDER:** This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register.

14.1.8.14 IC_RAW_INTR_STAT — Offset 4010E034h

I2C Raw Interrupt Status Register - I2C Raw Interrupt Status Register Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.

Type	Size	Offset	Default
MMIO	32 bit	4010E034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**MASTER_ON_HOLD:** Indicates whether master is holding the bus and TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE=1 and IC_EMPTYFIFO_HOLD_MASTER_EN=1.
12	0h RO/V	**RESTART_DET:** Indicates whether a RESTART condition has occurred on the I2C interface when DW_apb_i2c is operating in Slave mode and the slave is being addressed. Enabled only when IC_SLV_RESTART_DET_EN=1. Note: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I2C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt.
11	0h RO/V	**GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register. DW_apb_i2c stores the received data in the Rx buffer.
10	0h RO/V	**START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO/V	**STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: - If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt will be issued only if slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). - If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: - If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE),the STOP_DET interrupt will be issued only if Master is active. - If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED),the STOP_DET interrupt will be issued irrespective of whether master is active or not.
8	0h RO/V	**ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: - Disabling the DW_apb_i2c - Reading the IC_CLR_ACTIVITY register - Reading the IC_CLR_INTR register - System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO/V	**RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a 'transmit abort'. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. Note: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO flush because of TX_ABRT is controlled by the coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT.
5	0h RO/V	**RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the IC_DATA_CMD register. This bit is set to 0 just after the processor reads the IC_CLR_RD_REQ register.
4	0h RO/V	**TX_EMPTY:** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO/V	**TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO/V	**RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO/V	**RX_OVER:** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared. Note: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.
0	0h RO/V	**RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.

14.1.8.15 IC_RX_TL — Offset 4010E038h

I2C Receive FIFO Threshold Register - I2C Receive FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010E038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RX_TL:** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

14.1.8.16 IC_TX_TL — Offset 4010E03Ch

I2C Transmit FIFO Threshold Register - I2C Transmit FIFO Threshold Register

Type	Size	Offset	Default
MMIO	32 bit	4010E03Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

14.1.8.17 IC_CLR_INTR — Offset 4010E040h

Clear Combined and Individual Interrupt Register - Clear Combined and Individual Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.8.18 IC_CLR_RX_UNDER — Offset 4010E044h

Clear RX_UNDER Interrupt Register - Clear RX_UNDER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

14.1.8.19 IC_CLR_RX_OVER — Offset 4010E048h

Clear RX_OVER Interrupt Register - Clear RX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

14.1.8.20 IC_CLR_TX_OVER — Offset 4010E04Ch

Clear TX_OVER Interrupt Register - Clear TX_OVER Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E04Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

14.1.8.21 IC_CLR_RD_REQ — Offset 4010E050h

Clear RD_REQ Interrupt Register - Clear RD_REQ Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

14.1.8.22 IC_CLR_TX_ABRT — Offset 4010E054h

Clear TX_ABRT Interrupt Register - Clear TX_ABRT Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

14.1.8.23 IC_CLR_RX_DONE — Offset 4010E058h

Clear RX_DONE Interrupt Register - Clear RX_DONE Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

14.1.8.24 IC_CLR_ACTIVITY — Offset 4010E05Ch

Clear ACTIVITY Interrupt Register - Clear ACTIVITY Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E05Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

14.1.8.25 IC_CLR_STOP_DET — Offset 4010E060h

Clear STOP_DET Interrupt Register - Clear STOP_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

14.1.8.26 IC_CLR_START_DET — Offset 4010E064h

Clear START_DET Interrupt Register - Clear START_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

14.1.8.27 IC_CLR_GEN_CALL — Offset 4010E068h

Clear GEN_CALL Interrupt Register - Clear GEN_CALL Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

14.1.8.28 IC_ENABLE — Offset 4010E06Ch

I2C ENABLE Register - I2C Enable Register

Type	Size	Offset	Default
MMIO	32 bit	4010E06Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TX_CMD_BLOCK:** In Master mode: - 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. - 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.
1	0h RW	**ABORT:** When set, the controller initiates the transfer abort. - 0: ABORT not initiated or ABORT done - 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. - 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) - 1: Enables DW_apb_i2c Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: - The TX FIFO and RX FIFO get flushed. - Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.

14.1.8.29 IC_STATUS — Offset 4010E070h

I2C STATUS Register - I2C Status Register This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 10 are set to 0 When the master or slave state machines goes to idle and ic_en=0: - Bits 5 and 6 are set to 0

Type	Size	Offset	Default
MMIO	32 bit	4010E070h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RO/V	**SLV_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Slave mode due to Rx FIFO is Full and an additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
9	0h RO/V	**SLV_HOLD_TX_FIFO_EMPTY:** This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.
8	0h RO/V	**MST_HOLD_RX_FIFO_FULL:** This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).
7	0h RO/V	**MST_HOLD_TX_FIFO_EMPTY:** If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set. This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).
6	0h RO/V	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active - 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active
5	0h RO/V	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. - 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active - 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
4	0h RO/V	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. - 0: Receive FIFO is not full - 1: Receive FIFO is full
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. - 0: Receive FIFO is empty - 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. - 0: Transmit FIFO is not empty - 1: Transmit FIFO is empty
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. - 0: Transmit FIFO is full - 1: Transmit FIFO is not full
0	0h RO/V	**ACTIVITY:** I2C Activity Status.

14.1.8.30 IC_TXFLR — Offset 4010E074h

I2C Transmit FIFO Level Register - I2C Transmit FIFO Level Register This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever: - The I2C is disabled - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register - The slave bulk transmit mode is aborted The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Type	Size	Offset	Default
MMIO	32 bit	4010E074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.1.8.31 IC_RXFLR — Offset 4010E078h

I2C Receive FIFO Level Register - I2C Receive FIFO Level Register This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever: - The I2C is disabled - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Type	Size	Offset	Default
MMIO	32 bit	4010E078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.1.8.32 IC_SDA_HOLD — Offset 4010E07Ch

I2C SDA Hold Time Length Register - I2C SDA Hold Time Length Register The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW). The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode. Writes to this register succeed only when IC_ENABLE[0]=0. The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented. The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Type	Size	Offset	Default
MMIO	32 bit	4010E07Ch	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**IC_SDA_RX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver.
15:0	0005h RW	**IC_SDA_TX_HOLD:** Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter.

14.1.8.33 IC_TX_ABRT_SOURCE — Offset 4010E080h

I2C Transmit Abort Source Register - I2C Transmit Abort Source Register This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Type	Size	Offset	Default
MMIO	32 bit	4010E080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO/V	**TX_FLUSH_CNT:** This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
22:17	0h RO	**Reserved**
16	0h RO/V	**ABRT_USER_ABRT:** This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]) Role of DW_apb_i2c: Master-Transmitter
15	0h RO/V	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter
14	0h RO/V	**ABRT_SLV_ARBLOST:** This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter
13	0h RO/V	**ABRT_SLVFLUSH_TXFIFO:** This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Role of DW_apb_i2c: Slave-Transmitter
12	0h RO/V	**ARB_LOST:** This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter
11	0h RO/V	**ABRT_MASTER_DIS:** This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**ABRT_10B_RD_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver
9	0h RO/V	**ABRT_SBYTE_NORSTRT:** To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master
8	0h RO/V	**ABRT_HS_NORSTRT:** This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
7	0h RO/V	**ABRT_SBYTE_ACKDET:** This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
6	0h RO/V	**ABRT_HS_ACKDET:** This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master
5	0h RO/V	**ABRT_GCALL_READ:** This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter
4	0h RO/V	**ABRT_GCALL_NOACK:** This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter
3	0h RO/V	**ABRT_TXDATA_NOACK:** This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter
2	0h RO/V	**ABRT_10ADDR2_NOACK:** This field indicates that the Master is in 10-bit address mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
1	0h RO/V	**ABRT_10ADDR1_NOACK:** This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver
0	0h RO/V	**ABRT_7B_ADDR_NOACK:** This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver

14.1.8.34 IC_DMA_CR — Offset 4010E088h

DMA Control Register - DMA Control Register This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register

address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Type	Size	Offset	Default
MMIO	32 bit	4010E088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel.

14.1.8.35 IC_DMA_TDLR — Offset 4010E08Ch

DMA Transmit Data Level Register - DMA Transmit Data Level Register This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010E08Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.1.8.36 IC_DMA_RDLR — Offset 4010E090h

DMA Transmit Data Level Register - I2C Receive Data Level Register This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4010E090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

14.1.8.37 IC_SDA_SETUP — Offset 4010E094h

I2C SDA Setup Register - I2C SDA Setup Register This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. Writes to this register succeed only when IC_ENABLE[0] = 0. Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Type	Size	Offset	Default
MMIO	32 bit	4010E094h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2.

14.1.8.38 IC_ACK_GENERAL_CALL — Offset 4010E098h

I2C ACK General Call Register - I2C ACK General Call Register The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address. This register is applicable only when the DW_apb_i2c is in slave mode.

Type	Size	Offset	Default
MMIO	32 bit	4010E098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe).

14.1.8.39 IC_ENABLE_STATUS — Offset 4010E09Ch

I2C Enable Status Register - I2C Enable Status Register The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled. If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1. If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'. Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Type	Size	Offset	Default
MMIO	32 bit	4010E09Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO/V	**SLV_RX_DATA_LOST:** Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
1	0h RO/V	**SLV_DISABLED_WHILE_BUSY:** Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
0	0h RO/V	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. - When read as 1, DW_apb_i2c is deemed to be in an enabled state. - When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1).

14.1.8.40 IC_FS_SPKLEN — Offset 4010E0A0h

I2C SS, FS or FM+ spike suppression limit - I2C SS, FS or FM+ spike suppression limit This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic w hen the component is operating in SS, FS or FM+ modes. This register must be programmed with a minimum value of 1.

Type	Size	Offset	Default
MMIO	32 bit	4010E0A0h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	05h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.8.41 IC_HS_SPKLEN — Offset 4010E0A4h

I2C HS spike suppression limit register - I2C HS spike suppression limit register This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

Type	Size	Offset	Default
MMIO	32 bit	4010E0A4h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	02h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set.

14.1.8.42 IC_CLR_RESTART_DET — Offset 4010E0A8h

Clear RESTART_DET Interrupt Register - Clear RESTART_DET Interrupt Register

Type	Size	Offset	Default
MMIO	32 bit	4010E0A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**CLR_RESTART_DET:** Read this register to clear the RESTART_DET interrupt (bit 12) of IC_RAW_INTR_STAT register.

14.1.8.43 IC_COMP_PARAM_1 — Offset 4010E0F4h

Component Parameter Register 1 - Component Parameter Register 1 Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Type	Size	Offset	Default
MMIO	32 bit	4010E0F4h	003F3FEEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	3Fh RO/V	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. - 0x00 = Reserved - 0x01 = 2 - 0x02 = 3 - ... - 0xFF = 256
15:8	3Fh RO/V	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. - 0x00: Reserved - 0x01: 2 - 0x02: 3 - ... - 0xFF: 256
7	1h RO/V	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO/V	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO/V	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter.
3:2	3h RO/V	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. - 0x0: Reserved - 0x1: Standard - 0x2: Fast - 0x3: High
1:0	2h RO/V	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

14.1.8.44 IC_COMP_VERSION — Offset 4010E0F8h

I2C Component Version Register - I2C Component Version Register

Type	Size	Offset	Default
MMIO	32 bit	4010E0F8h	3230322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3230322Ah RO/V	**IC_COMP_VERSION:**

14.1.8.45 IC_COMP_TYPE — Offset 4010E0FCh

I2C Component Type Register - I2C Component Type Register

Type	Size	Offset	Default
MMIO	32 bit	4010E0FCh	44570140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO/V	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number.

14.2 GPIO Interface Registers

There are two GPIO Interface registers:-

- GPIO_0 Registers
- GPIO_1 Registers

GPIO Registers	Address Offset	Table
GPIO_0	40200000h - 40200130h	Table 14-9
GPIO_1	40300000h - 40300130h	Table 14-10

14.2.1 GPIO_0 Registers Summary

Table 14-9. Summary of GPIO_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40200000h	4	GPIO Pin DirectionLock (GCCR)	00000000h
40200004h	4	GPIO Pin Level (GPLR0)	00000000h
40200008h	4	GPIO Pin Level (GPLR1)	00000000h
4020001Ch	4	GPIO Pin Direction (GPDR0)	00000000h
40200020h	4	GPIO Pin Direction (GPDR1)	00000000h
40200034h	4	GPIO Pin Output Set (GPSR0)	00000000h
40200038h	4	GPIO Pin Output Set (GPSR1)	00000000h
4020004Ch	4	GPIO Pin Output Clear (GPCR0)	00000000h
40200050h	4	GPIO Pin Output Clear (GPCR1)	00000000h
40200064h	4	GPIO Rising Edge Detect Enable (GRER0)	00000000h
40200068h	4	GPIO Rising Edge Detect Enable (GRER1)	00000000h
4020007Ch	4	GPIO Falling Edge Detect Enable (GFER0)	00000000h
40200080h	4	GPIO Falling Edge Detect Enable (GFER1)	00000000h
40200094h	4	GPIO Glitch Filter Bypass (GFBR0)	00000000h
40200098h	4	GPIO Glitch Filter Bypass (GFBR1)	00000000h
402000ACh	4	GPIO Interrupt Mask (GIMR0)	00000000h
402000B0h	4	GPIO Interrupt Mask (GIMR1)	00000000h
402000C4h	4	GPIO Interrupt Source (GISR0)	00000000h
402000C8h	4	GPIO Interrupt Source (GISR1)	00000000h
40200100h	4	GPIO Wake Mask (GWMR0)	00000000h
40200104h	4	GPIO Wake Mask (GWMR1)	00000000h
40200118h	4	GPIO Wake Source (GWSR0)	00000000h
4020011Ch	4	GPIO Wake Source (GWSR1)	00000000h
40200130h	4	GPIO Secure Input (GSEC)	00000000h

14.2.1.1 GPIO Pin DirectionLock (GCCR) — Offset 40200000h

Register to lock GPIO Pin direction.

Type	Size	Offset	Default
MMIO	32 bit	40200000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**GPDR_LOCK:** This bit locks the GPDR register from being modified and is a write once bit which is cleared on a powergood assertion. This field is valid both when GPIO is input or output. 0 = GPDR is Unlocked 1 = GPDR is Locked.

14.2.1.2 GPIO Pin Level (GPLR0) — Offset 40200004h

Register for reading current value of GPIO pin. Valid when GPIO direction set as input.

Type	Size	Offset	Default
MMIO	32 bit	40200004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GPLR0:** Check the state of each of the GPIO pins by reading the GPIO Pin Level register (GPLR). Each bit in the GPLR corresponds to one pin in the GPIO. GPLR0 31 to 0 correspond to GPIO 31 to 0. Use the GPLRx read-only registers to determine the current value of a particular pin (only available during GPIO input mode). For reserved bits, reads return zero.

14.2.1.3 GPIO Pin Level (GPLR1) — Offset 40200008h

Register for reading current value of GPIO pin. Valid when GPIO direction set as input.

Type	Size	Offset	Default
MMIO	32 bit	40200008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GPLR1:** Check the state of each of the GPIO pins by reading the GPIO Pin Level register (GPLR). Each bit in the GPLR corresponds to one pin in the GPIO. GPLR0 31 to 0 correspond to GPIO 31 to 0. Use the GPLRx read-only registers to determine the current value of a particular pin (only available during GPIO input mode). For reserved bits, reads return zero.

14.2.1.4 GPIO Pin Direction (GPDR0) — Offset 4020001Ch

Register to set GPIO direction.

Type	Size	Offset	Default
MMIO	32 bit	4020001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPDR0:** Setting whether a pin is an input or output is controlled by programming the GPIO pin direction registers (GPDR0-5). The GPDR registers contain one direction control bit for each of the 192 GPIO pins. If a direction bit is programmed to 1, the GPIO is an output. If it is programmed to 0, it is an input. A reset clears all bits in the GPDR0-5 registers and configures all GPIO pins as inputs..

14.2.1.5 GPIO Pin Direction (GPDR1) — Offset 40200020h

Register to set GPIO direction.

Type	Size	Offset	Default
MMIO	32 bit	40200020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPDR1:** Setting whether a pin is an input or output is controlled by programming the GPIO pin direction registers (GPDR0-5). The GPDR registers contain one direction control bit for each of the 192 GPIO pins. If a direction bit is programmed to 1, the GPIO is an output. If it is programmed to 0, it is an input. A reset clears all bits in the GPDR0-5 registers and configures all GPIO pins as inputs..

14.2.1.6 GPIO Pin Output Set (GPSR0) — Offset 40200034h

Register to assert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	40200034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPSR0:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.1.7 GPIO Pin Output Set (GPSR1) — Offset 40200038h

Register to assert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	40200038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPSR1:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.1.8 GPIO Pin Output Clear (GPCR0) — Offset 4020004Ch

Register to deassert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	4020004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPCR0:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.1.9 GPIO Pin Output Clear (GPCR1) — Offset 40200050h

Register to deassert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	40200050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPCR1:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.1.10 GPIO Rising Edge Detect Enable (GRER0) — Offset 40200064h

Register to enable rising edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GRER0:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.1.11 GPIO Rising Edge Detect Enable (GRER1) — Offset 40200068h

Register to enable rising edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GRER1:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.1.12 GPIO Falling Edge Detect Enable (GFER0) — Offset 4020007Ch

Register to enable falling edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	4020007Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFER0:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.1.13 GPIO Falling Edge Detect Enable (GFER1) — Offset 40200080h

Register to enable falling edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFER1:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.1.14 GPIO Glitch Filter Bypass (GFBR0) — Offset 40200094h

Register to bypass Glitch filter for input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFBR0:** The GPIO Glitch Filter Bypass registers (GFBR0-5) contain a total of 192 bits that correspond to the 192 GPIO pins. When in general purpose mode, all GPIO pins go through the glitch filter logic by default. The glitch filter allows input signals that are stable for a certain number of clock cycles to propagate to the GPIO edge detection logic. Each GPIO pin can be individually configured to bypass this glitch filter..

14.2.1.15 GPIO Glitch Filter Bypass (GFBR1) — Offset 40200098h

Register to bypass Glitch filter for input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFBR1:** The GPIO Glitch Filter Bypass registers (GFBR0-5) contain a total of 192 bits that correspond to the 192 GPIO pins. When in general purpose mode, all GPIO pins go through the glitch filter logic by default. The glitch filter allows input signals that are stable for a certain number of clock cycles to propagate to the GPIO edge detection logic. Each GPIO pin can be individually configured to bypass this glitch filter..

14.2.1.16 GPIO Interrupt Mask (GIMR0) — Offset 402000ACh

Register to mask interrupts for GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	402000ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GIMR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.17 GPIO Interrupt Mask (GIMR1) — Offset 402000B0h

Register to mask interrupts for GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	402000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GIMR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.18 GPIO Interrupt Source (GISR0) — Offset 402000C4h

Register for interrupts status of GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	402000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GISR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.19 GPIO Interrupt Source (GISR1) — Offset 402000C8h

Register for interrupts status of GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	402000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GISR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.20 GPIO Wake Mask (GWMR0) — Offset 40200100h

Register to mask wake from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GWMR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.21 GPIO Wake Mask (GWMR1) — Offset 40200104h

Register to mask wake from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GWMR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.22 GPIO Wake Source (GWSR0) — Offset 40200118h

Register for indicating wake source from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	40200118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GWSR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.23 GPIO Wake Source (GWSR1) — Offset 4020011Ch

Register for indicating wake source from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	4020011Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GWSR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.1.24 GPIO Secure Input (GSEC) — Offset 40200130h

UNUSED FOR ISH.

Type	Size	Offset	Default
MMIO	32 bit	40200130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GSEC:** 1 = Hide Pin Level Status Updates to GPLR and Mask Pin Interrupts to IO-APIC 0 = Unhidden.

14.2.2 GPIO_1 Registers Summary

Table 14-10. Summary of GPIO_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40300000h	4	GPIO Pin DirectionLock (GCCR)	00000000h
40300004h	4	GPIO Pin Level (GPLR0)	00000000h
40300008h	4	GPIO Pin Level (GPLR1)	00000000h
4030001Ch	4	GPIO Pin Direction (GPDR0)	00000000h
40300020h	4	GPIO Pin Direction (GPDR1)	00000000h
40300034h	4	GPIO Pin Output Set (GPSR0)	00000000h
40300038h	4	GPIO Pin Output Set (GPSR1)	00000000h
4030004Ch	4	GPIO Pin Output Clear (GPCR0)	00000000h
40300050h	4	GPIO Pin Output Clear (GPCR1)	00000000h
40300064h	4	GPIO Rising Edge Detect Enable (GRER0)	00000000h
40300068h	4	GPIO Rising Edge Detect Enable (GRER1)	00000000h
4030007Ch	4	GPIO Falling Edge Detect Enable (GFER0)	00000000h
40300080h	4	GPIO Falling Edge Detect Enable (GFER1)	00000000h
40300094h	4	GPIO Glitch Filter Bypass (GFBR0)	00000000h
40300098h	4	GPIO Glitch Filter Bypass (GFBR1)	00000000h
403000ACh	4	GPIO Interrupt Mask (GIMR0)	00000000h
403000B0h	4	GPIO Interrupt Mask (GIMR1)	00000000h
403000C4h	4	GPIO Interrupt Source (GISR0)	00000000h
403000C8h	4	GPIO Interrupt Source (GISR1)	00000000h
40300100h	4	GPIO Wake Mask (GWMR0)	00000000h
40300104h	4	GPIO Wake Mask (GWMR1)	00000000h
40300118h	4	GPIO Wake Source (GWSR0)	00000000h
4030011Ch	4	GPIO Wake Source (GWSR1)	00000000h
40300130h	4	GPIO Secure Input (GSEC)	00000000h

14.2.2.1 GPIO Pin DirectionLock (GCCR) — Offset 40300000h

Register to lock GPIO Pin direction.

Type	Size	Offset	Default
MMIO	32 bit	40300000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**GPDR_LOCK:** This bit locks the GPDR register from being modified and is a write once bit which is cleared on a powergood assertion. This field is valid both when GPIO is input or output. 0 = GPDR is Unlocked 1 = GPDR is Locked.

14.2.2.2 GPIO Pin Level (GPLR0) — Offset 40300004h

Register for reading current value of GPIO pin. Valid when GPIO direction set as input.

Type	Size	Offset	Default
MMIO	32 bit	40300004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GPLR0:** Check the state of each of the GPIO pins by reading the GPIO Pin Level register (GPLR). Each bit in the GPLR corresponds to one pin in the GPIO. GPLR0 31 to 0 correspond to GPIO 31 to 0. Use the GPLRx read-only registers to determine the current value of a particular pin (regardless of the programmed pin direction). For reserved bits, reads return zero.

14.2.2.3 GPIO Pin Level (GPLR1) — Offset 40300008h

Register for reading current value of GPIO pin. Valid when GPIO direction set as input.

Type	Size	Offset	Default
MMIO	32 bit	40300008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GPLR1:** Check the state of each of the GPIO pins by reading the GPIO Pin Level register (GPLR). Each bit in the GPLR corresponds to one pin in the GPIO. GPLR0 31 to 0 correspond to GPIO 31 to 0. Use the GPLRx read-only registers to determine the current value of a particular pin (regardless of the programmed pin direction). For reserved bits, reads return zero.

14.2.2.4 GPIO Pin Direction (GPDR0) — Offset 4030001Ch

Register to set GPIO direction.

Type	Size	Offset	Default
MMIO	32 bit	4030001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPDR0:** Setting whether a pin is an input or output is controlled by programming the GPIO pin direction registers (GPDR0-5). The GPDR registers contain one direction control bit for each of the 192 GPIO pins. If a direction bit is programmed to 1, the GPIO is an output. If it is programmed to 0, it is an input. A reset clears all bits in the GPDR0-5 registers and configures all GPIO pins as inputs..

14.2.2.5 GPIO Pin Direction (GPDR1) — Offset 40300020h

Register to set GPIO direction.

Type	Size	Offset	Default
MMIO	32 bit	40300020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPDR1:** Setting whether a pin is an input or output is controlled by programming the GPIO pin direction registers (GPDR0-5). The GPDR registers contain one direction control bit for each of the 192 GPIO pins. If a direction bit is programmed to 1, the GPIO is an output. If it is programmed to 0, it is an input. A reset clears all bits in the GPDR0-5 registers and configures all GPIO pins as inputs..

14.2.2.6 GPIO Pin Output Set (GPSR0) — Offset 40300034h

Register to assert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	40300034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPSR0:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.2.7 GPIO Pin Output Set (GPSR1) — Offset 40300038h

Register to assert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	40300038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPSR1:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.2.8 GPIO Pin Output Clear (GPCR0) — Offset 4030004Ch

Register to deassert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	4030004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPCR0:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.2.9 GPIO Pin Output Clear (GPCR1) — Offset 40300050h

Register to deassert GPIO output pin, valid for output pins.

Type	Size	Offset	Default
MMIO	32 bit	40300050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**GPCR1:** When a GPIO is configured as an output, the state of the pin is controlled by writing to either the GPIO Pin Output Set registers (GPSR0-5) or the GPIO Pin Output Clear registers (GPCR0-5). An output pin is set by setting to its corresponding bit within the GPSR. To clear an output pin, set the corresponding GPCR bit. Writing 0 to any of the GPSR or GPCR bits has no effect on the state of the pin. Writing 1 to a GPSR or GPCR bit corresponding to a pin that is configured as an input is effective only after the pin is configured as an output. When a GPIO pin is reconfigured as an output, the most recent write to GPSR or GPCR determines the pins output state. The GPIO Pin-Output Set registers (GPSR0-5) and GPIO Pin-Output Clear registers (GPCR0-5) are write-only registers. Reads return unpredictable values. GPSR and GPCR arent actually registers they toggle the Set and Reset pins of a D-Flip-Flop. The reason for this implementation was to prevent the need for read-modify-writes from SW to toggle an external pin. .

14.2.2.10 GPIO Rising Edge Detect Enable (GRER0) — Offset 40300064h

Register to enable rising edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GRER0:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.2.11 GPIO Rising Edge Detect Enable (GRER1) — Offset 40300068h

Register to enable rising edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GRER1:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.2.12 GPIO Falling Edge Detect Enable (GFER0) — Offset 4030007Ch

Register to enable falling edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	4030007Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFER0:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.2.13 GPIO Falling Edge Detect Enable (GFER1) — Offset 40300080h

Register to enable falling edge detect for GPIO Input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFER1:** Each GPIO can also be programmed to detect rising-edge or falling-edge transition on a pin. When an edge is detected that matches the type of edge programmed for the pin, a status bit is set. The GPIO Rising-Edge Detect Enable register (GRERx) and Falling Edge Detect Enable register (GFERx) select the type of transition on a GPIO pin that causes an interrupt or wake to be propogated. For a given GPIO pin, if its corresponding GRER bit is set, an interrupt or wake source bit is set when the pin transitions from logic level zero to logic level one. Likewise, GFER sets the corresponding interrupt or wake source bit when a transition from logic level one to logic level zero occurs on the pin. When the corresponding bits are set in both registers, either a falling- or a rising-edge transition causes will cause the Interrupt or Wake Source registers to be set if they are unmasked. For the interrupt or wake source bits to be set it first has to be unmasked through the Interrupt Mask or Wake Mask register. Minimum pulse-width timing requirements exist to guarantee that an edge or level transition is detected. .

14.2.2.14 GPIO Glitch Filter Bypass (GFBR0) — Offset 40300094h

Register to bypass Glitch filter for input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFBR0:** The GPIO Glitch Filter Bypass registers (GFBR0-5) contain a total of 192 bits that correspond to the 192 GPIO pins. When in general purpose mode, all GPIO pins go through the glitch filter logic by default. The glitch filter allows input signals that are stable for a certain number of clock cycles to propagate to the GPIO edge detection logic. Each GPIO pin can be individually configured to bypass this glitch filter..

14.2.2.15 GPIO Glitch Filter Bypass (GFBR1) — Offset 40300098h

Register to bypass Glitch filter for input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFBR1:** The GPIO Glitch Filter Bypass registers (GFBR0-5) contain a total of 192 bits that correspond to the 192 GPIO pins. When in general purpose mode, all GPIO pins go through the glitch filter logic by default. The glitch filter allows input signals that are stable for a certain number of clock cycles to propagate to the GPIO edge detection logic. Each GPIO pin can be individually configured to bypass this glitch filter..

14.2.2.16 GPIO Interrupt Mask (GIMR0) — Offset 403000ACh

Register to mask interrupts for GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	403000ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GIMR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.17 GPIO Interrupt Mask (GIMR1) — Offset 403000B0h

Register to mask interrupts for GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	403000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GIMR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.18 GPIO Interrupt Source (GISR0) — Offset 403000C4h

Register for interrupts status of GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	403000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GISR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.19 GPIO Interrupt Source (GISR1) — Offset 403000C8h

Register for interrupts status of GPIO input pins.

Type	Size	Offset	Default
MMIO	32 bit	403000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GISR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.20 GPIO Wake Mask (GWMR0) — Offset 40300100h

Register to mask wake from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GWMR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.21 GPIO Wake Mask (GWMR1) — Offset 40300104h

Register to mask wake from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GWMR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.22 GPIO Wake Source (GWSR0) — Offset 40300118h

Register for indicating wake source from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	40300118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GWSR0:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.23 GPIO Wake Source (GWSR1) — Offset 4030011Ch

Register for indicating wake source from GPIO input pin.

Type	Size	Offset	Default
MMIO	32 bit	4030011Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GWSR1:** The GPIO Interrupt Mask, Interrupt Source, Wake Mask, and Wake Source registers are new registers for Tangier and are used to differentiate wakes and interrupts. These registers control if a GPIO pin is wake or interrupt enabled and the source registers contain information on which pin initiated the wake or interrupt..

14.2.2.24 GPIO Secure Input (GSEC) — Offset 40300130h

UNUSED FOR ISH.

Type	Size	Offset	Default
MMIO	32 bit	40300130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GSEC:** 1 = Hide Pin Level Status Updates to GPLR and Mask Pin Interrupts to IO-APIC 0 = Unhidden.

14.3 TGPIO Interface Registers

There are two TGPIO Interface registers:-

- TGPIO_0 Registers
- TGPIO_1 Registers

TGPIO Registers	Address Offset	Table
TGPIO_0	40201000h - 402016ACh	Table 14-11
TGPIO_1	40301000h - 403016ACh	Table 14-12

14.3.1 TGPIO_0 Registers Summary

Table 14-11. Summary of TGPIO_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40201000h	4	REG TGPIOCTL0 (TGPIO0_CTL_REG)	00002000h
40201004h	4	REG TGPIOCOMPV0_31_0 (TGPIO0_COMPV_31_0)	00000000h
40201008h	4	REG TGPIOCOMPV0_63_32 (TGPIO0_COMPV_63_32)	00000000h
4020100Ch	4	REG TGPIOPIV0_31_0 (TGPIO0_PIV_31_0)	00000000h
40201010h	4	REG TGPIOPIV0_63:32 (TGPIO0_PIV_63_32)	00000000h
40201014h	4	REG TGPIOTCV0_31_0 (TGPIO0_TCV_31_0)	00000000h
40201018h	4	REG TGPIOTCV0_63_32 (TGPIO0_TCV_63_32)	00000000h
4020101Ch	4	REG TGPIOECCV0_31_0 (TGPIO0_ECCV_31_0)	00000000h
40201020h	4	REG TGPIOECCV0_63_32 (TGPIO0_ECCV_63_32)	00000000h
40201024h	4	REG TGPIOEC0_31_0 (TGPIO0_EC_31_0)	00000000h
40201028h	4	REG TGPIOEC0_63_32 (TGPIO0_EC_63_32)	00000000h
4020102Ch	4	REG TGPIOMATCHMASK0_31_0 (TGPIO0_MATCH_MASK_31_0)	00000000h
40201030h	4	REG TGPIOMATCHMASK0_63_32 (TGPIO0_MATCH_MASK_63_32)	00000000h
40201040h	4	REG TGPIOCTL1 (TGPIO1_CTL_REG)	00002000h
40201044h	4	REG TGPIOCOMPV1_31_0 (TGPIO1_COMPV_31_0)	00000000h
40201048h	4	REG TGPIOCOMPV1_63_32 (TGPIO1_COMPV_63_32)	00000000h
4020104Ch	4	REG TGPIOPIV1_31_0 (TGPIO1_PIV_31_0)	00000000h
40201050h	4	REG TGPIOPIV1_63:32 (TGPIO1_PIV_63_32)	00000000h
40201054h	4	REG TGPIOTCV1_31_0 (TGPIO1_TCV_31_0)	00000000h
40201058h	4	REG TGPIOTCV1_63_32 (TGPIO1_TCV_63_32)	00000000h
4020105Ch	4	REG TGPIOECCV1_31_0 (TGPIO1_ECCV_31_0)	00000000h
40201060h	4	REG TGPIOECCV1_63_32 (TGPIO1_ECCV_63_32)	00000000h
40201064h	4	REG TGPIOEC1_31_0 (TGPIO1_EC_31_0)	00000000h
40201068h	4	REG TGPIOEC1_63_32 (TGPIO1_EC_63_32)	00000000h
4020106Ch	4	REG TGPIOMATCHMASK1_31_0 (TGPIO1_MATCH_MASK_31_0)	00000000h
40201070h	4	REG TGPIOMATCHMASK1_63_32 (TGPIO1_MATCH_MASK_63_32)	00000000h
40201080h	4	REG TGPIOCTL2 (TGPIO2_CTL_REG)	00002000h
40201084h	4	REG TGPIOCOMPV2_31_0 (TGPIO2_COMPV_31_0)	00000000h
40201088h	4	REG TGPIOCOMPV2_63_32 (TGPIO2_COMPV_63_32)	00000000h
4020108Ch	4	REG TGPIOPIV2_31_0 (TGPIO2_PIV_31_0)	00000000h
40201090h	4	REG TGPIOPIV2_63:32 (TGPIO2_PIV_63_32)	00000000h
40201094h	4	REG TGPIOTCV2_31_0 (TGPIO2_TCV_31_0)	00000000h
40201098h	4	REG TGPIOTCV2_63_32 (TGPIO2_TCV_63_32)	00000000h
4020109Ch	4	REG TGPIOECCV2_31_0 (TGPIO2_ECCV_31_0)	00000000h
402010A0h	4	REG TGPIOECCV2_63_32 (TGPIO2_ECCV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
402010A4h	4	REG TGPIOEC2_31_0 (TGPIO2_EC_31_0)	00000000h
402010A8h	4	REG TGPIOEC2_63_32 (TGPIO2_EC_63_32)	00000000h
402010ACh	4	REG TGPIOMATCHMASK2_31_0 (TGPIO2_MATCH_MASK_31_0)	00000000h
402010B0h	4	REG TGPIOMATCHMASK2_63_32 (TGPIO2_MATCH_MASK_63_32)	00000000h
402010C0h	4	REG TGPIOCTL3 (TGPIO3_CTL_REG)	00002000h
402010C4h	4	REG TGPIOCOMPV3_31_0 (TGPIO3_COMPV_31_0)	00000000h
402010C8h	4	REG TGPIOCOMPV3_63_32 (TGPIO3_COMPV_63_32)	00000000h
402010CCh	4	REG TGPIOPIV3_31_0 (TGPIO3_PIV_31_0)	00000000h
402010D0h	4	REG TGPIOPIV3_63:32 (TGPIO3_PIV_63_32)	00000000h
402010D4h	4	REG TGPIOTCV3_31_0 (TGPIO3_TCV_31_0)	00000000h
402010D8h	4	REG TGPIOTCV3_63_32 (TGPIO3_TCV_63_32)	00000000h
402010DCh	4	REG TGPIOECCV3_31_0 (TGPIO3_ECCV_31_0)	00000000h
402010E0h	4	REG TGPIOECCV3_63_32 (TGPIO3_ECCV_63_32)	00000000h
402010E4h	4	REG TGPIOEC3_31_0 (TGPIO3_EC_31_0)	00000000h
402010E8h	4	REG TGPIOEC3_63_32 (TGPIO3_EC_63_32)	00000000h
402010ECh	4	REG TGPIOMATCHMASK3_31_0 (TGPIO3_MATCH_MASK_31_0)	00000000h
402010F0h	4	REG TGPIOMATCHMASK3_63_32 (TGPIO3_MATCH_MASK_63_32)	00000000h
40201100h	4	REG TGPIOCTL4 (TGPIO4_CTL_REG)	00002000h
40201104h	4	REG TGPIOCOMPV4_31_0 (TGPIO4_COMPV_31_0)	00000000h
40201108h	4	REG TGPIOCOMPV4_63_32 (TGPIO4_COMPV_63_32)	00000000h
4020110Ch	4	REG TGPIOPIV4_31_0 (TGPIO4_PIV_31_0)	00000000h
40201110h	4	REG TGPIOPIV4_63:32 (TGPIO4_PIV_63_32)	00000000h
40201114h	4	REG TGPIOTCV4_31_0 (TGPIO4_TCV_31_0)	00000000h
40201118h	4	REG TGPIOTCV4_63_32 (TGPIO4_TCV_63_32)	00000000h
4020111Ch	4	REG TGPIOECCV4_31_0 (TGPIO4_ECCV_31_0)	00000000h
40201120h	4	REG TGPIOECCV4_63_32 (TGPIO4_ECCV_63_32)	00000000h
40201124h	4	REG TGPIOEC4_31_0 (TGPIO4_EC_31_0)	00000000h
40201128h	4	REG TGPIOEC4_63_32 (TGPIO4_EC_63_32)	00000000h
4020112Ch	4	REG TGPIOMATCHMASK4_31_0 (TGPIO4_MATCH_MASK_31_0)	00000000h
40201130h	4	REG TGPIOMATCHMASK4_63_32 (TGPIO4_MATCH_MASK_63_32)	00000000h
40201140h	4	REG TGPIOCTL5 (TGPIO5_CTL_REG)	00002000h
40201144h	4	REG TGPIOCOMPV5_31_0 (TGPIO5_COMPV_31_0)	00000000h
40201148h	4	REG TGPIOCOMPV5_63_32 (TGPIO5_COMPV_63_32)	00000000h
4020114Ch	4	REG TGPIOPIV5_31_0 (TGPIO5_PIV_31_0)	00000000h
40201150h	4	REG TGPIOPIV5_63:32 (TGPIO5_PIV_63_32)	00000000h
40201154h	4	REG TGPIOTCV5_31_0 (TGPIO5_TCV_31_0)	00000000h
40201158h	4	REG TGPIOTCV5_63_32 (TGPIO5_TCV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4020115Ch	4	REG TGPIOECCV5_31_0 (TGPIO5_ECCV_31_0)	00000000h
40201160h	4	REG TGPIOECCV5_63_32 (TGPIO5_ECCV_63_32)	00000000h
40201164h	4	REG TGPIOEC5_31_0 (TGPIO5_EC_31_0)	00000000h
40201168h	4	REG TGPIOEC5_63_32 (TGPIO5_EC_63_32)	00000000h
4020116Ch	4	REG TGPIOMATCHMASK5_31_0 (TGPIO5_MATCH_MASK_31_0)	00000000h
40201170h	4	REG TGPIOMATCHMASK5_63_32 (TGPIO5_MATCH_MASK_63_32)	00000000h
40201180h	4	REG TGPIOCTL6 (TGPIO6_CTL_REG)	00002000h
40201184h	4	REG TGPIOCOMPV6_31_0 (TGPIO6_COMPV_31_0)	00000000h
40201188h	4	REG TGPIOCOMPV6_63_32 (TGPIO6_COMPV_63_32)	00000000h
4020118Ch	4	REG TGPIOPIV6_31_0 (TGPIO6_PIV_31_0)	00000000h
40201190h	4	REG TGPIOPIV6_63:32 (TGPIO6_PIV_63_32)	00000000h
40201194h	4	REG TGPIOTCV6_31_0 (TGPIO6_TCV_31_0)	00000000h
40201198h	4	REG TGPIOTCV6_63_32 (TGPIO6_TCV_63_32)	00000000h
4020119Ch	4	REG TGPIOECCV6_31_0 (TGPIO6_ECCV_31_0)	00000000h
402011A0h	4	REG TGPIOECCV6_63_32 (TGPIO6_ECCV_63_32)	00000000h
402011A4h	4	REG TGPIOEC6_31_0 (TGPIO6_EC_31_0)	00000000h
402011A8h	4	REG TGPIOEC6_63_32 (TGPIO6_EC_63_32)	00000000h
402011ACh	4	REG TGPIOMATCHMASK6_31_0 (TGPIO6_MATCH_MASK_31_0)	00000000h
402011B0h	4	REG TGPIOMATCHMASK6_63_32 (TGPIO6_MATCH_MASK_63_32)	00000000h
402011C0h	4	REG TGPIOCTL7 (TGPIO7_CTL_REG)	00002000h
402011C4h	4	REG TGPIOCOMPV7_31_0 (TGPIO7_COMPV_31_0)	00000000h
402011C8h	4	REG TGPIOCOMPV7_63_32 (TGPIO7_COMPV_63_32)	00000000h
402011CCh	4	REG TGPIOPIV7_31_0 (TGPIO7_PIV_31_0)	00000000h
402011D0h	4	REG TGPIOPIV7_63:32 (TGPIO7_PIV_63_32)	00000000h
402011D4h	4	REG TGPIOTCV7_31_0 (TGPIO7_TCV_31_0)	00000000h
402011D8h	4	REG TGPIOTCV7_63_32 (TGPIO7_TCV_63_32)	00000000h
402011DCh	4	REG TGPIOECCV7_31_0 (TGPIO7_ECCV_31_0)	00000000h
402011E0h	4	REG TGPIOECCV7_63_32 (TGPIO7_ECCV_63_32)	00000000h
402011E4h	4	REG TGPIOEC7_31_0 (TGPIO7_EC_31_0)	00000000h
402011E8h	4	REG TGPIOEC7_63_32 (TGPIO7_EC_63_32)	00000000h
402011ECh	4	REG TGPIOMATCHMASK7_31_0 (TGPIO7_MATCH_MASK_31_0)	00000000h
402011F0h	4	REG TGPIOMATCHMASK7_63_32 (TGPIO7_MATCH_MASK_63_32)	00000000h
40201200h	4	REG TGPIOCTL8 (TGPIO8_CTL_REG)	00002000h
40201204h	4	REG TGPIOCOMPV8_31_0 (TGPIO8_COMPV_31_0)	00000000h
40201208h	4	REG TGPIOCOMPV8_63_32 (TGPIO8_COMPV_63_32)	00000000h
4020120Ch	4	REG TGPIOPIV8_31_0 (TGPIO8_PIV_31_0)	00000000h
40201210h	4	REG TGPIOPIV8_63:32 (TGPIO8_PIV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40201214h	4	REG TGPIOTCV8_31_0 (TGPIO8_TCV_31_0)	00000000h
40201218h	4	REG TGPIOTCV8_63_32 (TGPIO8_TCV_63_32)	00000000h
4020121Ch	4	REG TGPIOECCV8_31_0 (TGPIO8_ECCV_31_0)	00000000h
40201220h	4	REG TGPIOECCV8_63_32 (TGPIO8_ECCV_63_32)	00000000h
40201224h	4	REG TGPIOEC8_31_0 (TGPIO8_EC_31_0)	00000000h
40201228h	4	REG TGPIOEC8_63_32 (TGPIO8_EC_63_32)	00000000h
4020122Ch	4	REG TGPIOMATCHMASK8_31_0 (TGPIO8_MATCH_MASK_31_0)	00000000h
40201230h	4	REG TGPIOMATCHMASK8_63_32 (TGPIO8_MATCH_MASK_63_32)	00000000h
40201240h	4	REG TGPIOCTL9 (TGPIO9_CTL_REG)	00002000h
40201244h	4	REG TGPIOCOMPV9_31_0 (TGPIO9_COMPV_31_0)	00000000h
40201248h	4	REG TGPIOCOMPV9_63_32 (TGPIO9_COMPV_63_32)	00000000h
4020124Ch	4	REG TGPIOPIV9_31_0 (TGPIO9_PIV_31_0)	00000000h
40201250h	4	REG TGPIOPIV9_63:32 (TGPIO9_PIV_63_32)	00000000h
40201254h	4	REG TGPIOTCV9_31_0 (TGPIO9_TCV_31_0)	00000000h
40201258h	4	REG TGPIOTCV9_63_32 (TGPIO9_TCV_63_32)	00000000h
4020125Ch	4	REG TGPIOECCV9_31_0 (TGPIO9_ECCV_31_0)	00000000h
40201260h	4	REG TGPIOECCV9_63_32 (TGPIO9_ECCV_63_32)	00000000h
40201264h	4	REG TGPIOEC9_31_0 (TGPIO9_EC_31_0)	00000000h
40201268h	4	REG TGPIOEC9_63_32 (TGPIO9_EC_63_32)	00000000h
4020126Ch	4	REG TGPIOMATCHMASK9_31_0 (TGPIO9_MATCH_MASK_31_0)	00000000h
40201270h	4	REG TGPIOMATCHMASK9_63_32 (TGPIO9_MATCH_MASK_63_32)	00000000h
40201280h	4	REG TGPIOCTL10 (TGPIO10_CTL_REG)	00002000h
40201284h	4	REG TGPIOCOMPV10_31_0 (TGPIO10_COMPV_31_0)	00000000h
40201288h	4	REG TGPIOCOMPV10_63_32 (TGPIO10_COMPV_63_32)	00000000h
4020128Ch	4	REG TGPIOPIV10_31_0 (TGPIO10_PIV_31_0)	00000000h
40201290h	4	REG TGPIOPIV10_63:32 (TGPIO10_PIV_63_32)	00000000h
40201294h	4	REG TGPIOTCV10_31_0 (TGPIO10_TCV_31_0)	00000000h
40201298h	4	REG TGPIOTCV10_63_32 (TGPIO10_TCV_63_32)	00000000h
4020129Ch	4	REG TGPIOECCV10_31_0 (TGPIO10_ECCV_31_0)	00000000h
402012A0h	4	REG TGPIOECCV10_63_32 (TGPIO10_ECCV_63_32)	00000000h
402012A4h	4	REG TGPIOEC10_31_0 (TGPIO10_EC_31_0)	00000000h
402012A8h	4	REG TGPIOEC10_63_32 (TGPIO10_EC_63_32)	00000000h
402012ACh	4	REG TGPIOMATCHMASK10_31_0 (TGPIO10_MATCH_MASK_31_0)	00000000h
402012B0h	4	REG TGPIOMATCHMASK10_63_32 (TGPIO10_MATCH_MASK_63_32)	00000000h
402012C0h	4	REG TGPIOCTL11 (TGPIO11_CTL_REG)	00002000h
402012C4h	4	REG TGPIOCOMPV11_31_0 (TGPIO11_COMPV_31_0)	00000000h
402012C8h	4	REG TGPIOCOMPV11_63_32 (TGPIO11_COMPV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
402012CCh	4	REG TGPIOPIV11_31_0 (TGPIO11_PIV_31_0)	00000000h
402012D0h	4	REG TGPIOPIV11_63:32 (TGPIO11_PIV_63_32)	00000000h
402012D4h	4	REG TGPIOTCV11_31_0 (TGPIO11_TCV_31_0)	00000000h
402012D8h	4	REG TGPIOTCV11_63_32 (TGPIO11_TCV_63_32)	00000000h
402012DCh	4	REG TGPIOECCV11_31_0 (TGPIO11_ECCV_31_0)	00000000h
402012E0h	4	REG TGPIOECCV11_63_32 (TGPIO11_ECCV_63_32)	00000000h
402012E4h	4	REG TGPIOEC11_31_0 (TGPIO11_EC_31_0)	00000000h
402012E8h	4	REG TGPIOEC11_63_32 (TGPIO11_EC_63_32)	00000000h
402012ECh	4	REG TGPIOMATCHMASK11_31_0 (TGPIO11_MATCH_MASK_31_0)	00000000h
402012F0h	4	REG TGPIOMATCHMASK11_63_32 (TGPIO11_MATCH_MASK_63_32)	00000000h
40201300h	4	REG TGPIOCTL12 (TGPIO12_CTL_REG)	00002000h
40201304h	4	REG TGPIOCOMPV12_31_0 (TGPIO12_COMPV_31_0)	00000000h
40201308h	4	REG TGPIOCOMPV12_63_32 (TGPIO12_COMPV_63_32)	00000000h
4020130Ch	4	REG TGPIOPIV12_31_0 (TGPIO12_PIV_31_0)	00000000h
40201310h	4	REG TGPIOPIV12_63:32 (TGPIO12_PIV_63_32)	00000000h
40201314h	4	REG TGPIOTCV12_31_0 (TGPIO12_TCV_31_0)	00000000h
40201318h	4	REG TGPIOTCV12_63_32 (TGPIO12_TCV_63_32)	00000000h
4020131Ch	4	REG TGPIOECCV12_31_0 (TGPIO12_ECCV_31_0)	00000000h
40201320h	4	REG TGPIOECCV12_63_32 (TGPIO12_ECCV_63_32)	00000000h
40201324h	4	REG TGPIOEC12_31_0 (TGPIO12_EC_31_0)	00000000h
40201328h	4	REG TGPIOEC12_63_32 (TGPIO12_EC_63_32)	00000000h
4020132Ch	4	REG TGPIOMATCHMASK12_31_0 (TGPIO12_MATCH_MASK_31_0)	00000000h
40201330h	4	REG TGPIOMATCHMASK12_63_32 (TGPIO12_MATCH_MASK_63_32)	00000000h
40201340h	4	REG TGPIOCTL13 (TGPIO13_CTL_REG)	00002000h
40201344h	4	REG TGPIOCOMPV13_31_0 (TGPIO13_COMPV_31_0)	00000000h
40201348h	4	REG TGPIOCOMPV13_63_32 (TGPIO13_COMPV_63_32)	00000000h
4020134Ch	4	REG TGPIOPIV13_31_0 (TGPIO13_PIV_31_0)	00000000h
40201350h	4	REG TGPIOPIV13_63:32 (TGPIO13_PIV_63_32)	00000000h
40201354h	4	REG TGPIOTCV13_31_0 (TGPIO13_TCV_31_0)	00000000h
40201358h	4	REG TGPIOTCV13_63_32 (TGPIO13_TCV_63_32)	00000000h
4020135Ch	4	REG TGPIOECCV13_31_0 (TGPIO13_ECCV_31_0)	00000000h
40201360h	4	REG TGPIOECCV13_63_32 (TGPIO13_ECCV_63_32)	00000000h
40201364h	4	REG TGPIOEC13_31_0 (TGPIO13_EC_31_0)	00000000h
40201368h	4	REG TGPIOEC13_63_32 (TGPIO13_EC_63_32)	00000000h
4020136Ch	4	REG TGPIOMATCHMASK13_31_0 (TGPIO13_MATCH_MASK_31_0)	00000000h
40201370h	4	REG TGPIOMATCHMASK13_63_32 (TGPIO13_MATCH_MASK_63_32)	00000000h
40201380h	4	REG TGPIOCTL14 (TGPIO14_CTL_REG)	00002000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40201384h	4	REG TGPIOCOMPV14_31_0 (TGPIO14_COMPV_31_0)	00000000h
40201388h	4	REG TGPIOCOMPV14_63_32 (TGPIO14_COMPV_63_32)	00000000h
4020138Ch	4	REG TGPIOPIV14_31_0 (TGPIO14_PIV_31_0)	00000000h
40201390h	4	REG TGPIOPIV14_63:32 (TGPIO14_PIV_63_32)	00000000h
40201394h	4	REG TGPIOTCV14_31_0 (TGPIO14_TCV_31_0)	00000000h
40201398h	4	REG TGPIOTCV14_63_32 (TGPIO14_TCV_63_32)	00000000h
4020139Ch	4	REG TGPIOECCV14_31_0 (TGPIO14_ECCV_31_0)	00000000h
402013A0h	4	REG TGPIOECCV14_63_32 (TGPIO14_ECCV_63_32)	00000000h
402013A4h	4	REG TGPIOEC14_31_0 (TGPIO14_EC_31_0)	00000000h
402013A8h	4	REG TGPIOEC14_63_32 (TGPIO14_EC_63_32)	00000000h
402013ACh	4	REG TGPIOMATCHMASK14_31_0 (TGPIO14_MATCH_MASK_31_0)	00000000h
402013B0h	4	REG TGPIOMATCHMASK14_63_32 (TGPIO14_MATCH_MASK_63_32)	00000000h
402013C0h	4	REG TGPIOCTL15 (TGPIO15_CTL_REG)	00002000h
402013C4h	4	REG TGPIOCOMPV15_31_0 (TGPIO15_COMPV_31_0)	00000000h
402013C8h	4	REG TGPIOCOMPV15_63_32 (TGPIO15_COMPV_63_32)	00000000h
402013CCh	4	REG TGPIOPIV15_31_0 (TGPIO15_PIV_31_0)	00000000h
402013D0h	4	REG TGPIOPIV15_63:32 (TGPIO15_PIV_63_32)	00000000h
402013D4h	4	REG TGPIOTCV15_31_0 (TGPIO15_TCV_31_0)	00000000h
402013D8h	4	REG TGPIOTCV15_63_32 (TGPIO15_TCV_63_32)	00000000h
402013DCh	4	REG TGPIOECCV15_31_0 (TGPIO15_ECCV_31_0)	00000000h
402013E0h	4	REG TGPIOECCV15_63_32 (TGPIO15_ECCV_63_32)	00000000h
402013E4h	4	REG TGPIOEC15_31_0 (TGPIO15_EC_31_0)	00000000h
402013E8h	4	REG TGPIOEC15_63_32 (TGPIO15_EC_63_32)	00000000h
402013ECh	4	REG TGPIOMATCHMASK15_31_0 (TGPIO15_MATCH_MASK_31_0)	00000000h
402013F0h	4	REG TGPIOMATCHMASK15_63_32 (TGPIO15_MATCH_MASK_63_32)	00000000h
40201400h	4	REG TGPIOCTL16 (TGPIO16_CTL_REG)	00002000h
40201404h	4	REG TGPIOCOMPV16_31_0 (TGPIO16_COMPV_31_0)	00000000h
40201408h	4	REG TGPIOCOMPV16_63_32 (TGPIO16_COMPV_63_32)	00000000h
4020140Ch	4	REG TGPIOPIV16_31_0 (TGPIO16_PIV_31_0)	00000000h
40201410h	4	REG TGPIOPIV16_63:32 (TGPIO16_PIV_63_32)	00000000h
40201414h	4	REG TGPIOTCV16_31_0 (TGPIO16_TCV_31_0)	00000000h
40201418h	4	REG TGPIOTCV16_63_32 (TGPIO16_TCV_63_32)	00000000h
4020141Ch	4	REG TGPIOECCV16_31_0 (TGPIO16_ECCV_31_0)	00000000h
40201420h	4	REG TGPIOECCV16_63_32 (TGPIO16_ECCV_63_32)	00000000h
40201424h	4	REG TGPIOEC16_31_0 (TGPIO16_EC_31_0)	00000000h
40201428h	4	REG TGPIOEC16_63_32 (TGPIO16_EC_63_32)	00000000h
4020142Ch	4	REG TGPIOMATCHMASK16_31_0 (TGPIO16_MATCH_MASK_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40201430h	4	REG TGPIOMATCHMASK16_63_32 (TGPIO16_MATCH_MASK_63_32)	00000000h
40201440h	4	REG TGPIOCTL17 (TGPIO17_CTL_REG)	00002000h
40201444h	4	REG TGPIOCOMPV17_31_0 (TGPIO17_COMPV_31_0)	00000000h
40201448h	4	REG TGPIOCOMPV17_63_32 (TGPIO17_COMPV_63_32)	00000000h
4020144Ch	4	REG TGPIOPIV17_31_0 (TGPIO17_PIV_31_0)	00000000h
40201450h	4	REG TGPIOPIV17_63:32 (TGPIO17_PIV_63_32)	00000000h
40201454h	4	REG TGPIOTCV17_31_0 (TGPIO17_TCV_31_0)	00000000h
40201458h	4	REG TGPIOTCV17_63_32 (TGPIO17_TCV_63_32)	00000000h
4020145Ch	4	REG TGPIOECCV17_31_0 (TGPIO17_ECCV_31_0)	00000000h
40201460h	4	REG TGPIOECCV17_63_32 (TGPIO17_ECCV_63_32)	00000000h
40201464h	4	REG TGPIOEC17_31_0 (TGPIO17_EC_31_0)	00000000h
40201468h	4	REG TGPIOEC17_63_32 (TGPIO17_EC_63_32)	00000000h
4020146Ch	4	REG TGPIOMATCHMASK17_31_0 (TGPIO17_MATCH_MASK_31_0)	00000000h
40201470h	4	REG TGPIOMATCHMASK17_63_32 (TGPIO17_MATCH_MASK_63_32)	00000000h
40201480h	4	REG TGPIOCTL18 (TGPIO18_CTL_REG)	00002000h
40201484h	4	REG TGPIOCOMPV18_31_0 (TGPIO18_COMPV_31_0)	00000000h
40201488h	4	REG TGPIOCOMPV18_63_32 (TGPIO18_COMPV_63_32)	00000000h
4020148Ch	4	REG TGPIOPIV18_31_0 (TGPIO18_PIV_31_0)	00000000h
40201490h	4	REG TGPIOPIV18_63:32 (TGPIO18_PIV_63_32)	00000000h
40201494h	4	REG TGPIOTCV18_31_0 (TGPIO18_TCV_31_0)	00000000h
40201498h	4	REG TGPIOTCV18_63_32 (TGPIO18_TCV_63_32)	00000000h
4020149Ch	4	REG TGPIOECCV18_31_0 (TGPIO18_ECCV_31_0)	00000000h
402014A0h	4	REG TGPIOECCV18_63_32 (TGPIO18_ECCV_63_32)	00000000h
402014A4h	4	REG TGPIOEC18_31_0 (TGPIO18_EC_31_0)	00000000h
402014A8h	4	REG TGPIOEC18_63_32 (TGPIO18_EC_63_32)	00000000h
402014ACh	4	REG TGPIOMATCHMASK18_31_0 (TGPIO18_MATCH_MASK_31_0)	00000000h
402014B0h	4	REG TGPIOMATCHMASK18_63_32 (TGPIO18_MATCH_MASK_63_32)	00000000h
402014C0h	4	REG TGPIOCTL19 (TGPIO19_CTL_REG)	00002000h
402014C4h	4	REG TGPIOCOMPV19_31_0 (TGPIO19_COMPV_31_0)	00000000h
402014C8h	4	REG TGPIOCOMPV19_63_32 (TGPIO19_COMPV_63_32)	00000000h
402014CCh	4	REG TGPIOPIV19_31_0 (TGPIO19_PIV_31_0)	00000000h
402014D0h	4	REG TGPIOPIV19_63:32 (TGPIO19_PIV_63_32)	00000000h
402014D4h	4	REG TGPIOTCV19_31_0 (TGPIO19_TCV_31_0)	00000000h
402014D8h	4	REG TGPIOTCV19_63_32 (TGPIO19_TCV_63_32)	00000000h
402014DCh	4	REG TGPIOECCV19_31_0 (TGPIO19_ECCV_31_0)	00000000h
402014E0h	4	REG TGPIOECCV19_63_32 (TGPIO19_ECCV_63_32)	00000000h
402014E4h	4	REG TGPIOEC19_31_0 (TGPIO19_EC_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
402014E8h	4	REG TGPIOEC19_63_32 (TGPIO19_EC_63_32)	00000000h
402014ECh	4	REG TGPIOMATCHMASK19_31_0 (TGPIO19_MATCH_MASK_31_0)	00000000h
402014F0h	4	REG TGPIOMATCHMASK19_63_32 (TGPIO19_MATCH_MASK_63_32)	00000000h
40201500h	4	REG TGPIOINTRCTL (TGPIO_INTR_CTL_REG)	00000000h
40201504h	4	REG TGPIORIS (TGPIO_INTR_RIS_REG)	00000000h
40201508h	4	REG TGPIOMSC (TGPIO_INTR_MSC_REG)	00000000h
4020150Ch	4	REG TGPIOMIS (TGPIO_INTR_MIS_REG)	00000000h
40201510h	4	REG TGPIOICR (TGPIO_INTR_ICR_REG)	00000000h
40201514h	4	REG TGPIO_CLK_SEL_REG (TGPIO_CLK_SEL_REG)	00000000h
40201518h	4	REG TGPIO_CLK_SEL_REG (TGPIO_XTAL_CG_REG)	00000000h
4020151Ch	4	Reg TGPIO_PTP_CG_REG (TGPIO_PTP_CG_REG)	00000000h
40201520h	4	REG TGPIO_TS_SEL_0_REG (TGPIO_TS_SEL_0_REG)	00000000h
40201524h	4	REG TGPIO_TS_SEL_1_REG (TGPIO_TS_SEL_1_REG)	00000000h
40201528h	4	REG TMT_CLK_SEL_REG (TGPIO_TMT_CLK_SEL_REG)	00000000h
40201530h	4	REG TGPIO_TSC_CTL_REG (TGPIO_CTS_ENABLE_REG)	00000000h
40201534h	4	REG TGPIO_TSC_STATUS_REG (TGPIO_CTS_VALID_REG)	00000000h
40201600h	4	REG TMTCTL_TSG (TMT_CTL_TSG_REG)	00000000h
40201604h	4	REG TMTR_TSG (TMTR_TSG_REG)	00000000h
40201608h	4	REG TMTL_TSG (TMTL_TSG_REG)	00000000h
4020160Ch	4	REG TMTH_TSG (TMTH_TSG_REG)	00000000h
40201610h	4	REG TIMINCA_TSG (TMT_TIMINCA_TSG_REG)	00000000h
40201614h	4	REG TIMADJ_TSG (TMT_TIMADJ_TSG_REG)	00000000h
40201618h	4	REG LXTS_TMT_HIGH_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_1)	00000000h
4020161Ch	4	REG LXTS_TMT_LOW_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_0)	00000000h
40201620h	4	REG LXTS_ART_HIGH_TSG (TMT_ART_SNAPSHOT_TSG_REG_1)	00000000h
40201624h	4	REG LXTS_ART_LOW_TSG (TMT_ART_SNAPSHOT_TSG_REG_0)	00000000h
40201628h	4	REG RXTS_TMT_HIGH_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_1)	00000000h
4020162Ch	4	REG RXTS_TMT_LOW_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_0)	00000000h
40201640h	4	REG TMTCTL_GLOBAL (TMT_CTL_GLOBAL_REG)	00000000h
40201644h	4	REG TMTR_GLOBAL (TMTR_GLOBAL_REG)	00000000h
40201648h	4	REG TMTL_GLOBAL (TMTL_GLOBAL_REG)	00000000h
4020164Ch	4	REG TMTH_GLOBAL (TMTH_GLOBAL_REG)	00000000h
40201650h	4	REG TIMINCA_GLOBAL (TMT_TIMINCA_GLOBAL_REG)	00000000h
40201654h	4	REG TIMADJ_GLOBAL (TMT_TIMADJ_GLOBAL_REG)	00000000h
40201658h	4	REG LXTS_TMT_LOW_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4020165Ch	4	REG LXTS_TMT_HIGH_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_1)	00000000h
40201660h	4	REG LXTS_ART_LOW_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_0)	00000000h
40201664h	4	REG LXTS_ART_HIGH_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_1)	00000000h
40201668h	4	REG RXTS_TMT_LOW_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_0)	00000000h
4020166Ch	4	REG RXTS_TMT_HIGH_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_1)	00000000h
40201680h	4	REG TMTCTL_WORKING (TMT_CTL_WORKING_REG)	00000000h
40201684h	4	REG TMTR_WORKING (TMTR_WORKING_REG)	00000000h
40201688h	4	REG TMTL_WORKING (TMTL_WORKING_REG)	00000000h
4020168Ch	4	REG TMTH_WORKING (TMTH_WORKING_REG)	00000000h
40201690h	4	REG TIMINCA_WORKING (TMT_TIMINCA_WORKING_REG)	00000000h
40201694h	4	REG TIMADJ_WORKING (TMT_TIMADJ_WORKING_REG)	00000000h
40201698h	4	REG LXTS_TMT_LOW_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_0)	00000000h
4020169Ch	4	REG LXTS_TMT_HIGH_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_1)	00000000h
402016A0h	4	REG LXTS_ART_LOW_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_0)	00000000h
402016A4h	4	REG LXTS_ART_HIGH_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_1)	00000000h
402016A8h	4	REG RXTS_TMT_LOW_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_0)	00000000h
402016ACh	4	REG RXTS_TMT_HIGH_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_1)	00000000h

14.3.1.1 REG TGPIOCTL0 (TGPIO0_CTL_REG) — Offset 40201000h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201000h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO0_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO0_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO0_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 - reserved .
13	1h RW	**Freeze Input Timestamp (TGPIO0_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO0_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO0_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO0_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO0_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved .
1	0h RW	**Direction (DIR) (TGPIO0_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO0_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.2 REG TGPIOCOMPV0_31_0 (TGPIO0_COMPV_31_0) — Offset 40201004h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO0_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.3 REG TGPIOCOMPV0_63_32 (TGPIO0_COMPV_63_32) — Offset 40201008h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO0_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.4 REG TGPIOPIV0_31_0 (TGPIO0_PIV_31_0) — Offset 4020100Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.5 REG TGPIOPIV0_63:32 (TGPIO0_PIV_63_32) — Offset 40201010h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.6 REG TGPIOTCV0_31_0 (TGPIO0_TCV_31_0) — Offset 40201014h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.7 REG TGPIOTCV0_63_32 (TGPIO0_TCV_63_32) — Offset 40201018h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.8 REG TGPIOECCV0_31_0 (TGPIO0_ECCV_31_0) — Offset 4020101Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020101Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.9 REG TGPIOECCV0_63_32 (TGPIO0_ECCV_63_32) — Offset 40201020h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.10 REG TGPIOEC0_31_0 (TGPIO0_EC_31_0) — Offset 40201024h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.11 REG TGPIOEC0_63_32 (TGPIO0_EC_63_32) — Offset 40201028h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.12 REG TGPIOMATCHMASK0_31_0 (TGPIO0_MATCH_MASK_31_0) — Offset 4020102Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020102Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.13 REG TGPIOMATCHMASK0_63_32 (TGPIO0_MATCH_MASK_63_32) — Offset 40201030h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.14 REG TGPIOCTL1 (TGPIO1_CTL_REG) — Offset 40201040h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201040h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO1_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO1_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO1_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO1_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO1_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO1_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO1_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO1_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO1_CTL_DIR_O):** 0 Output 1 Input .
0	0h RW	**Enable (EN) (TGPIO1_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled .

14.3.1.15 REG TGPIOCOMPV1_31_0 (TGPIO1_COMPV_31_0) — Offset 40201044h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO1_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.16 REG TGPIOCOMPV1_63_32 (TGPIO1_COMPV_63_32) — Offset 40201048h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO1_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.17 REG TGPIOPIV1_31_0 (TGPIO1_PIV_31_0) — Offset 4020104Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020104Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.18 REG TGPIOPIV1_63:32 (TGPIO1_PIV_63_32) — Offset 40201050h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.19 REG TGPIOTCV1_31_0 (TGPIO1_TCV_31_0) — Offset 40201054h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.20 REG TGPIOTCV1_63_32 (TGPIO1_TCV_63_32) — Offset 40201058h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.21 REG TGPIOECCV1_31_0 (TGPIO1_ECCV_31_0) — Offset 4020105Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020105Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.22 REG TGPIOECCV1_63_32 (TGPIO1_ECCV_63_32) — Offset 40201060h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.23 REG TGPIOEC1_31_0 (TGPIO1_EC_31_0) — Offset 40201064h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.24 REG TGPIOEC1_63_32 (TGPIO1_EC_63_32) — Offset 40201068h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.25 REG TGPIOMATCHMASK1_31_0 (TGPIO1_MATCH_MASK_31_0) — Offset 4020106Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020106Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.26 REG TGPIOMATCHMASK1_63_32 (TGPIO1_MATCH_MASK_63_32) — Offset 40201070h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.27 REG TGPIOCTL2 (TGPIO2_CTL_REG) — Offset 40201080h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201080h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO2_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO2_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO2_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO2_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO2_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO2_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO2_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO2_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO2_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO2_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.28 REG TGPIOCOMPV2_31_0 (TGPIO2_COMPV_31_0) — Offset 40201084h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO2_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.29 REG TGPIOCOMPV2_63_32 (TGPIO2_COMPV_63_32) — Offset 40201088h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO2_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.30 REG TGPIOPIV2_31_0 (TGPIO2_PIV_31_0) — Offset 4020108Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020108Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.31 REG TGPIOPIV2_63:32 (TGPIO2_PIV_63_32) — Offset 40201090h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.32 REG TGPIOTCV2_31_0 (TGPIO2_TCV_31_0) — Offset 40201094h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.33 REG TGPIOTCV2_63_32 (TGPIO2_TCV_63_32) — Offset 40201098h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.34 REG TGPIOECCV2_31_0 (TGPIO2_ECCV_31_0) — Offset 4020109Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020109Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.35 REG TGPIOECCV2_63_32 (TGPIO2_ECCV_63_32) — Offset 402010A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.36 REG TGPIOEC2_31_0 (TGPIO2_EC_31_0) — Offset 402010A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402010A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.37 REG TGPIOEC2_63_32 (TGPIO2_EC_63_32) — Offset 402010A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.38 REG TGPIOMATCHMASK2_31_0 (TGPIO2_MATCH_MASK_31_0) — Offset 402010ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402010ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.39 REG TGPIOMATCHMASK2_63_32 (TGPIO2_MATCH_MASK_63_32) — Offset 402010B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402010B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.40 REG TGPIOCTL3 (TGPIO3_CTL_REG) — Offset 402010C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	402010C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO3_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO3_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO3_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO3_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO3_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO3_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO3_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO3_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO3_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO3_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.41 REG TGPIOCOMPV3_31_0 (TGPIO3_COMPV_31_0) — Offset 402010C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402010C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO3_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.42 REG TGPIOCOMPV3_63_32 (TGPIO3_COMPV_63_32) — Offset 402010C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO3_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.43 REG TGPIOPIV3_31_0 (TGPIO3_PIV_31_0) — Offset 402010CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	402010CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.44 REG TGPIOPIV3_63:32 (TGPIO3_PIV_63_32) — Offset 402010D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.45 REG TGPIOTCV3_31_0 (TGPIO3_TCV_31_0) — Offset 402010D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402010D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.46 REG TGPIOTCV3_63_32 (TGPIO3_TCV_63_32) — Offset 402010D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.47 REG TGPIOECCV3_31_0 (TGPIO3_ECCV_31_0) — Offset 402010DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	402010DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.48 REG TGPIOECCV3_63_32 (TGPIO3_ECCV_63_32) — Offset 402010E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.49 REG TGPIOEC3_31_0 (TGPIO3_EC_31_0) — Offset 402010E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402010E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.50 REG TGPIOEC3_63_32 (TGPIO3_EC_63_32) — Offset 402010E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402010E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.1.51 REG TGPIOMATCHMASK3_31_0 (TGPIO3_MATCH_MASK_31_0) — Offset 402010ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402010ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.52 REG TGPIOMATCHMASK3_63_32 (TGPIO3_MATCH_MASK_63_32) — Offset 402010F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402010F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.53 REG TGPIOCTL4 (TGPIO4_CTL_REG) — Offset 40201100h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201100h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO4_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO4_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO4_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO4_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO4_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO4_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO4_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO4_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO4_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO4_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.54 REG TGPIOCOMPV4_31_0 (TGPIO4_COMPV_31_0) — Offset 40201104h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO4_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.55 REG TGPIOCOMPV4_63_32 (TGPIO4_COMPV_63_32) — Offset 40201108h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO4_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.56 REG TGPIOPIV4_31_0 (TGPIO4_PIV_31_0) — Offset 4020110Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020110Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.57 REG TGPIOPIV4_63:32 (TGPIO4_PIV_63_32) — Offset 40201110h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.58 REG TGPIOTCV4_31_0 (TGPIO4_TCV_31_0) — Offset 40201114h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.59 REG TGPIOTCV4_63_32 (TGPIO4_TCV_63_32) — Offset 40201118h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.60 REG TGPIOECCV4_31_0 (TGPIO4_ECCV_31_0) — Offset 4020111Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020111Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.61 REG TGPIOECCV4_63_32 (TGPIO4_ECCV_63_32) — Offset 40201120h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.62 REG TGPIOEC4_31_0 (TGPIO4_EC_31_0) — Offset 40201124h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.63 REG TGPIOEC4_63_32 (TGPIO4_EC_63_32) — Offset 40201128h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.64 REG TGPIOMATCHMASK4_31_0 (TGPIO4_MATCH_MASK_31_0) — Offset 4020112Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020112Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.65 REG TGPIOMATCHMASK4_63_32 (TGPIO4_MATCH_MASK_63_32) — Offset 40201130h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.66 REG TGPIOCTL5 (TGPIO5_CTL_REG) — Offset 40201140h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201140h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO5_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO5_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO5_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO5_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO5_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO5_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO5_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO5_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO5_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO5_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.67 REG TGPIOCOMPV5_31_0 (TGPIO5_COMPV_31_0) — Offset 40201144h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO5_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.68 REG TGPIOCOMPV5_63_32 (TGPIO5_COMPV_63_32) — Offset 40201148h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO5_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.69 REG TGPIOPIV5_31_0 (TGPIO5_PIV_31_0) — Offset 4020114Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020114Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.70 REG TGPIOPIV5_63:32 (TGPIO5_PIV_63_32) — Offset 40201150h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.71 REG TGPIOTCV5_31_0 (TGPIO5_TCV_31_0) — Offset 40201154h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201154h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.72 REG TGPIOTCV5_63_32 (TGPIO5_TCV_63_32) — Offset 40201158h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.73 REG TGPIOECCV5_31_0 (TGPIO5_ECCV_31_0) — Offset 4020115Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020115Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.74 REG TGPIOECCV5_63_32 (TGPIO5_ECCV_63_32) — Offset 40201160h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.75 REG TGPIOEC5_31_0 (TGPIO5_EC_31_0) — Offset 40201164h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.76 REG TGPIOEC5_63_32 (TGPIO5_EC_63_32) — Offset 40201168h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.77 REG TGPIOMATCHMASK5_31_0 (TGPIO5_MATCH_MASK_31_0) — Offset 4020116Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020116Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.78 REG TGPIOMATCHMASK5_63_32 (TGPIO5_MATCH_MASK_63_32) — Offset 40201170h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201170h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.79 REG TGPIOCTL6 (TGPIO6_CTL_REG) — Offset 40201180h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201180h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO6_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO6_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO6_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO6_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO6_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO6_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO6_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO6_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO6_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO6_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.80 REG TGPIOCOMPV6_31_0 (TGPIO6_COMPV_31_0) — Offset 40201184h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201184h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO6_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.81 REG TGPIOCOMPV6_63_32 (TGPIO6_COMPV_63_32) — Offset 40201188h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201188h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO6_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.82 REG TGPIOPIV6_31_0 (TGPIO6_PIV_31_0) — Offset 4020118Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020118Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.83 REG TGPIOPIV6_63:32 (TGPIO6_PIV_63_32) — Offset 40201190h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201190h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.84 REG TGPIOTCV6_31_0 (TGPIO6_TCV_31_0) — Offset 40201194h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201194h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.85 REG TGPIOTCV6_63_32 (TGPIO6_TCV_63_32) — Offset 40201198h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201198h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.86 REG TGPIOECCV6_31_0 (TGPIO6_ECCV_31_0) — Offset 4020119Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020119Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.87 REG TGPIOECCV6_63_32 (TGPIO6_ECCV_63_32) — Offset 402011A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.88 REG TGPIOEC6_31_0 (TGPIO6_EC_31_0) — Offset 402011A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402011A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.89 REG TGPIOEC6_63_32 (TGPIO6_EC_63_32) — Offset 402011A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.90 REG TGPIOMATCHMASK6_31_0 (TGPIO6_MATCH_MASK_31_0) — Offset 402011ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402011ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.91 REG TGPIOMATCHMASK6_63_32 (TGPIO6_MATCH_MASK_63_32) — Offset 402011B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402011B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.92 REG TGPIOCTL7 (TGPIO7_CTL_REG) — Offset 402011C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	402011C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO7_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO7_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO7_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO7_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO7_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO7_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO7_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO7_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO7_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO7_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.93 REG TGPIOCOMPV7_31_0 (TGPIO7_COMPV_31_0) — Offset 402011C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402011C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO7_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.94 REG TGPIOCOMPV7_63_32 (TGPIO7_COMPV_63_32) — Offset 402011C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO7_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.95 REG TGPIOPIV7_31_0 (TGPIO7_PIV_31_0) — Offset 402011CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	402011CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.96 REG TGPIOPIV7_63:32 (TGPIO7_PIV_63_32) — Offset 402011D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.97 REG TGPIOTCV7_31_0 (TGPIO7_TCV_31_0) — Offset 402011D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402011D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.98 REG TGPIOTCV7_63_32 (TGPIO7_TCV_63_32) — Offset 402011D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.99 REG TGPIOECCV7_31_0 (TGPIO7_ECCV_31_0) — Offset 402011DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	402011DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.100 REG TGPIOECCV7_63_32 (TGPIO7_ECCV_63_32) — Offset 402011E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.101 REG TGPIOEC7_31_0 (TGPIO7_EC_31_0) — Offset 402011E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402011E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.102 REG TGPIOEC7_63_32 (TGPIO7_EC_63_32) — Offset 402011E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402011E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.103 REG TGPIOMATCHMASK7_31_0 (TGPIO7_MATCH_MASK_31_0) — Offset 402011ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402011ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.104 REG TGPIOMATCHMASK7_63_32 (TGPIO7_MATCH_MASK_63_32) — Offset 402011F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402011F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.105 REG TGPIOCTL8 (TGPIO8_CTL_REG) — Offset 40201200h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201200h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO8_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO8_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO8_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO8_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO8_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO8_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO8_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO8_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO8_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO8_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.106 REG TGPIOCOMPV8_31_0 (TGPIO8_COMPV_31_0) — Offset 40201204h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO8_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.107 REG TGPIOCOMPV8_63_32 (TGPIO8_COMPV_63_32) — Offset 40201208h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO8_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.108 REG TGPIOPIV8_31_0 (TGPIO8_PIV_31_0) — Offset 4020120Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020120Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.109 REG TGPIOPIV8_63:32 (TGPIO8_PIV_63_32) — Offset 40201210h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.110 REG TGPIOTCV8_31_0 (TGPIO8_TCV_31_0) — Offset 40201214h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201214h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.111 REG TGPIOTCV8_63_32 (TGPIO8_TCV_63_32) — Offset 40201218h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201218h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.112 REG TGPIOECCV8_31_0 (TGPIO8_ECCV_31_0) — Offset 4020121Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020121Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.113 REG TGPIOECCV8_63_32 (TGPIO8_ECCV_63_32) — Offset 40201220h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.114 REG TGPIOEC8_31_0 (TGPIO8_EC_31_0) — Offset 40201224h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201224h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.115 REG TGPIOEC8_63_32 (TGPIO8_EC_63_32) — Offset 40201228h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.116 REG TGPIOMATCHMASK8_31_0 (TGPIO8_MATCH_MASK_31_0) — Offset 4020122Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020122Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.117 REG TGPIOMATCHMASK8_63_32 (TGPIO8_MATCH_MASK_63_32) — Offset 40201230h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.118 REG TGPIOCTL9 (TGPIO9_CTL_REG) — Offset 40201240h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201240h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO9_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO9_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO9_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO9_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO9_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO9_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO9_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO9_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO9_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO9_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.119 REG TGPIOCOMPV9_31_0 (TGPIO9_COMPV_31_0) — Offset 40201244h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201244h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO9_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.120 REG TGPIOCOMPV9_63_32 (TGPIO9_COMPV_63_32) — Offset 40201248h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201248h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO9_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.121 REG TGPIOPIV9_31_0 (TGPIO9_PIV_31_0) — Offset 4020124Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020124Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.122 REG TGPIOPIV9_63:32 (TGPIO9_PIV_63_32) — Offset 40201250h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201250h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.123 REG TGPIOTCV9_31_0 (TGPIO9_TCV_31_0) — Offset 40201254h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201254h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.124 REG TGPIOTCV9_63_32 (TGPIO9_TCV_63_32) — Offset 40201258h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201258h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.125 REG TGPIOECCV9_31_0 (TGPIO9_ECCV_31_0) — Offset 4020125Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020125Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.126 REG TGPIOECCV9_63_32 (TGPIO9_ECCV_63_32) — Offset 40201260h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201260h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.127 REG TGPIOEC9_31_0 (TGPIO9_EC_31_0) — Offset 40201264h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201264h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.128 REG TGPIOEC9_63_32 (TGPIO9_EC_63_32) — Offset 40201268h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201268h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.129 REG TGPIOMATCHMASK9_31_0 (TGPIO9_MATCH_MASK_31_0) — Offset 4020126Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020126Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.130 REG TGPIOMATCHMASK9_63_32 (TGPIO9_MATCH_MASK_63_32) — Offset 40201270h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201270h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.131 REG TGPIOCTL10 (TGPIO10_CTL_REG) — Offset 40201280h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201280h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO10_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO10_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO10_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO10_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO10_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO10_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO10_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO10_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO10_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO10_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.132 REG TGPIOCOMPV10_31_0 (TGPIO10_COMPV_31_0) — Offset 40201284h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201284h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO10_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.133 REG TGPIOCOMPV10_63_32 (TGPIO10_COMPV_63_32) — Offset 40201288h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201288h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO10_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.134 REG TGPIOPIV10_31_0 (TGPIO10_PIV_31_0) — Offset 4020128Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020128Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.135 REG TGPIOPIV10_63:32 (TGPIO10_PIV_63_32) — Offset 40201290h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201290h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.136 REG TGPIOTCV10_31_0 (TGPIO10_TCV_31_0) — Offset 40201294h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201294h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.137 REG TGPIOTCV10_63_32 (TGPIO10_TCV_63_32) — Offset 40201298h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201298h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.138 REG TGPIOECCV10_31_0 (TGPIO10_ECCV_31_0) — Offset 4020129Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020129Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.139 REG TGPIOECCV10_63_32 (TGPIO10_ECCV_63_32) — Offset 402012A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.140 REG TGPIOEC10_31_0 (TGPIO10_EC_31_0) — Offset 402012A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402012A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.141 REG TGPIOEC10_63_32 (TGPIO10_EC_63_32) — Offset 402012A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.142 REG TGPIOMATCHMASK10_31_0 (TGPIO10_MATCH_MASK_31_0) — Offset 402012ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402012ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.143 REG TGPIOMATCHMASK10_63_32 (TGPIO10_MATCH_MASK_63_32) — Offset 402012B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402012B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.144 REG TGPIOCTL11 (TGPIO11_CTL_REG) — Offset 402012C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	402012C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO11_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO11_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO11_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO11_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO11_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO11_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO11_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO11_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO11_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO11_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.145 REG TGPIOCOMPV11_31_0 (TGPIO11_COMPV_31_0) — Offset 402012C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402012C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO11_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.146 REG TGPIOCOMPV11_63_32 (TGPIO11_COMPV_63_32) — Offset 402012C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO11_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.147 REG TGPIOPIV11_31_0 (TGPIO11_PIV_31_0) — Offset 402012CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	402012CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.148 REG TGPIOPIV11_63:32 (TGPIO11_PIV_63_32) — Offset 402012D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.149 REG TGPIOTCV11_31_0 (TGPIO11_TCV_31_0) — Offset 402012D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402012D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.150 REG TGPIOTCV11_63_32 (TGPIO11_TCV_63_32) — Offset 402012D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.151 REG TGPIOECCV11_31_0 (TGPIO11_ECCV_31_0) — Offset 402012DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	402012DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.152 REG TGPIOECCV11_63_32 (TGPIO11_ECCV_63_32) — Offset 402012E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.153 REG TGPIOEC11_31_0 (TGPIO11_EC_31_0) — Offset 402012E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402012E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.154 REG TGPIOEC11_63_32 (TGPIO11_EC_63_32) — Offset 402012E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402012E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.155 REG TGPIOMATCHMASK11_31_0 (TGPIO11_MATCH_MASK_31_0) — Offset 402012ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402012ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.156 REG TGPIOMATCHMASK11_63_32 (TGPIO11_MATCH_MASK_63_32) — Offset 402012F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402012F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.157 REG TGPIOCTL12 (TGPIO12_CTL_REG) — Offset 40201300h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201300h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO12_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO12_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO12_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO12_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO12_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO12_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO12_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO12_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO12_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO12_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.158 REG TGPIOCOMPV12_31_0 (TGPIO12_COMPV_31_0) — Offset 40201304h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201304h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO12_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.159 REG TGPIOCOMPV12_63_32 (TGPIO12_COMPV_63_32) — Offset 40201308h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201308h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO12_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.160 REG TGPIOPIV12_31_0 (TGPIO12_PIV_31_0) — Offset 4020130Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020130Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.161 REG TGPIOPIV12_63:32 (TGPIO12_PIV_63_32) — Offset 40201310h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201310h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.162 REG TGPIOTCV12_31_0 (TGPIO12_TCV_31_0) — Offset 40201314h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201314h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.163 REG TGPIOTCV12_63_32 (TGPIO12_TCV_63_32) — Offset 40201318h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201318h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.164 REG TGPIOECCV12_31_0 (TGPIO12_ECCV_31_0) — Offset 4020131Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020131Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.165 REG TGPIOECCV12_63_32 (TGPIO12_ECCV_63_32) — Offset 40201320h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201320h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.166 REG TGPIOEC12_31_0 (TGPIO12_EC_31_0) — Offset 40201324h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201324h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.167 REG TGPIOEC12_63_32 (TGPIO12_EC_63_32) — Offset 40201328h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201328h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.168 REG TGPIOMATCHMASK12_31_0 (TGPIO12_MATCH_MASK_31_0) — Offset 4020132Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020132Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.169 REG TGPIOMATCHMASK12_63_32 (TGPIO12_MATCH_MASK_63_32) — Offset 40201330h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201330h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.170 REG TGPIOCTL13 (TGPIO13_CTL_REG) — Offset 40201340h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201340h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO13_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO13_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO13_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO13_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO13_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO13_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO13_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO13_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO13_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO13_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.171 REG TGPIOCOMPV13_31_0 (TGPIO13_COMPV_31_0) — Offset 40201344h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201344h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO13_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.172 REG TGPIOCOMPV13_63_32 (TGPIO13_COMPV_63_32) — Offset 40201348h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201348h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO13_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.173 REG TGPIOPIV13_31_0 (TGPIO13_PIV_31_0) — Offset 4020134Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020134Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.174 REG TGPIOPIV13_63:32 (TGPIO13_PIV_63_32) — Offset 40201350h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201350h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.175 REG TGPIOTCV13_31_0 (TGPIO13_TCV_31_0) — Offset 40201354h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201354h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.176 REG TGPIOTCV13_63_32 (TGPIO13_TCV_63_32) — Offset 40201358h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201358h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.177 REG TGPIOECCV13_31_0 (TGPIO13_ECCV_31_0) — Offset 4020135Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020135Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.178 REG TGPIOECCV13_63_32 (TGPIO13_ECCV_63_32) — Offset 40201360h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201360h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.179 REG TGPIOEC13_31_0 (TGPIO13_EC_31_0) — Offset 40201364h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201364h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.180 REG TGPIOEC13_63_32 (TGPIO13_EC_63_32) — Offset 40201368h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201368h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.181 REG TGPIOMATCHMASK13_31_0 (TGPIO13_MATCH_MASK_31_0) — Offset 4020136Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020136Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.182 REG TGPIOMATCHMASK13_63_32 (TGPIO13_MATCH_MASK_63_32) — Offset 40201370h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201370h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.183 REG TGPIOCTL14 (TGPIO14_CTL_REG) — Offset 40201380h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201380h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO14_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO14_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO14_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO14_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO14_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO14_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO14_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO14_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO14_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO14_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.184 REG TGPIOCOMPV14_31_0 (TGPIO14_COMPV_31_0) — Offset 40201384h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201384h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO14_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.185 REG TGPIOCOMPV14_63_32 (TGPIO14_COMPV_63_32) — Offset 40201388h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201388h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO14_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.186 REG TGPIOPIV14_31_0 (TGPIO14_PIV_31_0) — Offset 4020138Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020138Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.187 REG TGPIOPIV14_63:32 (TGPIO14_PIV_63_32) — Offset 40201390h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201390h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.188 REG TGPIOTCV14_31_0 (TGPIO14_TCV_31_0) — Offset 40201394h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201394h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.189 REG TGPIOTCV14_63_32 (TGPIO14_TCV_63_32) — Offset 40201398h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201398h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.190 REG TGPIOECCV14_31_0 (TGPIO14_ECCV_31_0) — Offset 4020139Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020139Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.191 REG TGPIOECCV14_63_32 (TGPIO14_ECCV_63_32) — Offset 402013A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.192 REG TGPIOEC14_31_0 (TGPIO14_EC_31_0) — Offset 402013A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402013A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.193 REG TGPIOEC14_63_32 (TGPIO14_EC_63_32) — Offset 402013A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.194 REG TGPIOMATCHMASK14_31_0 (TGPIO14_MATCH_MASK_31_0) — Offset 402013ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402013ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.195 REG TGPIOMATCHMASK14_63_32 (TGPIO14_MATCH_MASK_63_32) — Offset 402013B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402013B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.196 REG TGPIOCTL15 (TGPIO15_CTL_REG) — Offset 402013C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	402013C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO15_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO15_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO15_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO15_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO15_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO15_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO15_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO15_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO15_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO15_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.197 REG TGPIOCOMPV15_31_0 (TGPIO15_COMPV_31_0) — Offset 402013C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402013C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO15_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.198 REG TGPIOCOMPV15_63_32 (TGPIO15_COMPV_63_32) — Offset 402013C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO15_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.199 REG TGPIOPIV15_31_0 (TGPIO15_PIV_31_0) — Offset 402013CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	402013CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.200 REG TGPIOPIV15_63:32 (TGPIO15_PIV_63_32) — Offset 402013D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.201 REG TGPIOTCV15_31_0 (TGPIO15_TCV_31_0) — Offset 402013D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402013D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.202 REG TGPIOTCV15_63_32 (TGPIO15_TCV_63_32) — Offset 402013D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.203 REG TGPIOECCV15_31_0 (TGPIO15_ECCV_31_0) — Offset 402013DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	402013DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.204 REG TGPIOECCV15_63_32 (TGPIO15_ECCV_63_32) — Offset 402013E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.205 REG TGPIOEC15_31_0 (TGPIO15_EC_31_0) — Offset 402013E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402013E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.206 REG TGPIOEC15_63_32 (TGPIO15_EC_63_32) — Offset 402013E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402013E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.207 REG TGPIOMATCHMASK15_31_0 (TGPIO15_MATCH_MASK_31_0) — Offset 402013ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402013ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.208 REG TGPIOMATCHMASK15_63_32 (TGPIO15_MATCH_MASK_63_32) — Offset 402013F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402013F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.209 REG TGPIOCTL16 (TGPIO16_CTL_REG) — Offset 40201400h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201400h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO16_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO16_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO16_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO16_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO16_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO16_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO16_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO16_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO16_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO16_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.210 REG TGPIOCOMPV16_31_0 (TGPIO16_COMPV_31_0) — Offset 40201404h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO16_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.211 REG TGPIOCOMPV16_63_32 (TGPIO16_COMPV_63_32) — Offset 40201408h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201408h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO16_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.212 REG TGPIOPIV16_31_0 (TGPIO16_PIV_31_0) — Offset 4020140Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020140Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.213 REG TGPIOPIV16_63:32 (TGPIO16_PIV_63_32) — Offset 40201410h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201410h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.214 REG TGPIOTCV16_31_0 (TGPIO16_TCV_31_0) — Offset 40201414h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.215 REG TGPIOTCV16_63_32 (TGPIO16_TCV_63_32) — Offset 40201418h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201418h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.216 REG TGPIOECCV16_31_0 (TGPIO16_ECCV_31_0) — Offset 4020141Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020141Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.217 REG TGPIOECCV16_63_32 (TGPIO16_ECCV_63_32) — Offset 40201420h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201420h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.218 REG TGPIOEC16_31_0 (TGPIO16_EC_31_0) — Offset 40201424h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201424h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.219 REG TGPIOEC16_63_32 (TGPIO16_EC_63_32) — Offset 40201428h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201428h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.220 REG TGPIOMATCHMASK16_31_0 (TGPIO16_MATCH_MASK_31_0) — Offset 4020142Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020142Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.221 REG TGPIOMATCHMASK16_63_32 (TGPIO16_MATCH_MASK_63_32) — Offset 40201430h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201430h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.222 REG TGPIOCTL17 (TGPIO17_CTL_REG) — Offset 40201440h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201440h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO17_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO17_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO17_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO17_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO17_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO17_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO17_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO17_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO17_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO17_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.223 REG TGPIOCOMPV17_31_0 (TGPIO17_COMPV_31_0) — Offset 40201444h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201444h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO17_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.224 REG TGPIOCOMPV17_63_32 (TGPIO17_COMPV_63_32) — Offset 40201448h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201448h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO17_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.225 REG TGPIOPIV17_31_0 (TGPIO17_PIV_31_0) — Offset 4020144Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020144Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.226 REG TGPIOPIV17_63:32 (TGPIO17_PIV_63_32) — Offset 40201450h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201450h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.227 REG TGPIOTCV17_31_0 (TGPIO17_TCV_31_0) — Offset 40201454h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201454h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.228 REG TGPIOTCV17_63_32 (TGPIO17_TCV_63_32) — Offset 40201458h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201458h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.229 REG TGPIOECCV17_31_0 (TGPIO17_ECCV_31_0) — Offset 4020145Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020145Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.230 REG TGPIOECCV17_63_32 (TGPIO17_ECCV_63_32) — Offset 40201460h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201460h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.231 REG TGPIOEC17_31_0 (TGPIO17_EC_31_0) — Offset 40201464h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201464h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.232 REG TGPIOEC17_63_32 (TGPIO17_EC_63_32) — Offset 40201468h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201468h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.233 REG TGPIOMATCHMASK17_31_0 (TGPIO17_MATCH_MASK_31_0) — Offset 4020146Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020146Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.234 REG TGPIOMATCHMASK17_63_32 (TGPIO17_MATCH_MASK_63_32) — Offset 40201470h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201470h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.235 REG TGPIOCTL18 (TGPIO18_CTL_REG) — Offset 40201480h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40201480h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO18_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO18_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO18_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO18_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO18_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO18_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO18_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO18_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO18_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO18_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.236 REG TGPIOCOMPV18_31_0 (TGPIO18_COMPV_31_0) — Offset 40201484h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201484h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO18_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.237 REG TGPIOCOMPV18_63_32 (TGPIO18_COMPV_63_32) — Offset 40201488h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201488h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO18_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.238 REG TGPIOPIV18_31_0 (TGPIO18_PIV_31_0) — Offset 4020148Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020148Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.239 REG TGPIOPIV18_63:32 (TGPIO18_PIV_63_32) — Offset 40201490h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201490h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.240 REG TGPIOTCV18_31_0 (TGPIO18_TCV_31_0) — Offset 40201494h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40201494h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.241 REG TGPIOTCV18_63_32 (TGPIO18_TCV_63_32) — Offset 40201498h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40201498h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.242 REG TGPIOECCV18_31_0 (TGPIO18_ECCV_31_0) — Offset 4020149Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4020149Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.243 REG TGPIOECCV18_63_32 (TGPIO18_ECCV_63_32) — Offset 402014A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.244 REG TGPIOEC18_31_0 (TGPIO18_EC_31_0) — Offset 402014A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402014A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.245 REG TGPIOEC18_63_32 (TGPIO18_EC_63_32) — Offset 402014A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.246 REG TGPIOMATCHMASK18_31_0 (TGPIO18_MATCH_MASK_31_0) — Offset 402014ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402014ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.247 REG TGPIOMATCHMASK18_63_32 (TGPIO18_MATCH_MASK_63_32) — Offset 402014B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402014B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.248 REG TGPIOCTL19 (TGPIO19_CTL_REG) — Offset 402014C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	402014C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO19_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO19_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO19_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO19_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO19_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO19_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO19_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO19_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO19_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO19_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.1.249 REG TGPIOCOMPV19_31_0 (TGPIO19_COMPV_31_0) — Offset 402014C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402014C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO19_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.250 REG TGPIOCOMPV19_63_32 (TGPIO19_COMPV_63_32) — Offset 402014C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO19_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.1.251 REG TGPIOPIV19_31_0 (TGPIO19_PIV_31_0) — Offset 402014CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	402014CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.252 REG TGPIOPIV19_63:32 (TGPIO19_PIV_63_32) — Offset 402014D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.1.253 REG TGPIOTCV19_31_0 (TGPIO19_TCV_31_0) — Offset 402014D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	402014D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.254 REG TGPIOTCV19_63_32 (TGPIO19_TCV_63_32) — Offset 402014D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.1.255 REG TGPIOECCV19_31_0 (TGPIO19_ECCV_31_0) — Offset 402014DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	402014DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.256 REG TGPIOECCV19_63_32 (TGPIO19_ECCV_63_32) — Offset 402014E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.1.257 REG TGPIOEC19_31_0 (TGPIO19_EC_31_0) — Offset 402014E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	402014E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.258 REG TGPIOEC19_63_32 (TGPIO19_EC_63_32) — Offset 402014E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	402014E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.1.259 REG TGPIOMATCHMASK19_31_0 (TGPIO19_MATCH_MASK_31_0) — Offset 402014ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	402014ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.260 REG TGPIOMATCHMASK19_63_32 (TGPIO19_MATCH_MASK_63_32) — Offset 402014F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	402014F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.1.261 REG TGPIOINTRCTL (TGPIO_INTR_CTL_REG) — Offset 40201500h

Interrupt control register.

Type	Size	Offset	Default
MMIO	32 bit	40201500h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Disable Interrupt Coalescing (TGPIO_INTR_COALESCE_DISABLE):** When set will prevent coalescing of interrupts. The default is to enable interrupt coalescing.

14.3.1.262 REG TGPIORIS (TGPIO_INTR_RIS_REG) — Offset 40201504h

Raw interrupt status register.

Type	Size	Offset	Default
MMIO	32 bit	40201504h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_GLOBAL:** Set when the TMT GLOBAL nanosecond counter wraps which is about every 1s.
24	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_WORKING:** Set when the TMT WORKING nanosecond counter wraps which is about every 1s.
23	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_TSG:** Set when the TMT TSG nanosecond counter wraps which is about every 1s.
22	0h RO	**Time Adjust Complete TADJ_TMT_GLOBAL_CMPLT (TGPIO_RIS_TADJ_TMT_GLOBAL_CMPLT):** 0-No Interrupt 1-Interrupt.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**Time Adjust Complete TADJ_TMT_WORKING_CMPLT (TGPIO_RIS_TADJ_TMT_WORKING_CMPLT):** 0-No Interrupt 1-Interrupt.
20	0h RO	**Time Adjust Complete TADJ_TMT_TSG_CMPLT (TGPIO_RIS_TADJ_TMT_TSG_CMPLT):** 0-No Interrupt 1-Interrupt.
19:0	00000h RO	**Event Interrupt (TGPIO_RIS_EVENT_INTR):** 0-No Interrupt 1-Interrupt Pending.

14.3.1.263 REG TGPIOMSC (TGPIO_INTR_MSC_REG) — Offset 40201508h

Interrupt mask control register.

Type	Size	Offset	Default
MMIO	32 bit	40201508h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_GLOBAL_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
24	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_WORKING_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
23	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_TSG_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
22	0h RW	**Time Adjust Complete Enable TADJ_TMT_GLOBAL_EN (TGPIO_MSC_TADJ_TMT_GLOBAL_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
21	0h RW	**Time Adjust Complete Enable TADJ_TMT_WORKING_EN (TGPIO_MSC_TADJ_TMT_WORKING_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
20	0h RW	**Time Adjust Complete Enable TADJ_TMT_TSG_EN (TGPIO_MSC_TADJ_TMT_TSG_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
19:0	00000h RW	**Event Interrupt (TGPIO_MSC_EVENT_INTR):** 0-Interrupt Disabled 1-Interrupt Enabled.

14.3.1.264 REG TGPIOMIS (TGPIO_INTR_MIS_REG) — Offset 4020150Ch

Masked interrupt status register.

Type	Size	Offset	Default
MMIO	32 bit	4020150Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_GLOBAL:** 0- No Interrupt 1-Interrupt.
24	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_WORKING:** 0- No Interrupt 1-Interrupt.
23	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_TSG:** 0- No Interrupt 1-Interrupt.
22	0h RO	**Time Adjust Complete TADJ_TMT_GLOBAL_CMPLT (TGPIO_MIS_TADJ_TMT_GLOBAL):** 0- No Interrupt 1-Interrupt.
21	0h RO	**Time Adjust Complete TADJ_TMT_WORKING_CMPLT (TGPIO_MIS_TADJ_TMT_WORKING):** 0- No Interrupt 1-Interrupt.
20	0h RO	**Time Adjust Complete TADJ_TMT_TSG_CMPLT (TGPIO_MIS_TADJ_TMT_TSG):** 0- No Interrupt 1-Interrupt.
19:0	00000h RO	**Event Interrupt (TGPIO_MIS_EVENT_INTR):** 1-No Interrupt 2-Interrupt Pending.

14.3.1.265 REG TGPIOICR (TGPIO_INTR_ICR_REG) — Offset 40201510h

Interrupt clear register.

Type	Size	Offset	Default
MMIO	32 bit	40201510h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_GLOBAL:** 0 No change 1-Clear Interrupt Request.
24	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_WORKING:** 0 No change 1-Clear Interrupt Request.
23	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_TSG:** 0 No change 1-Clear Interrupt Request.
22	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_GLOBAL_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_GLOBAL):** 0 No change 1-Clear Interrupt Request.
21	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_WORKING_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_WORKING):** 0 No change 1-Clear Interrupt Request.
20	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_TSG_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_TSG):** 0 No change 1-Clear Interrupt Request.
19:0	00000h WO	**Clear Event Interrupt [19:0] (TGPIO_ICR_CLR_EVENT_INTR):** 0 No change 1-Clear Interrupt Request.

14.3.1.266 REG TGPIO_CLK_SEL_REG (TGPIO_CLK_SEL_REG) — Offset 40201514h

Timed GPIO clock select register.

Type	Size	Offset	Default
MMIO	32 bit	40201514h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:0	00000h RW	**Clock Select (TGPIO_CLK_SEL_REG):** Timed GPIO clock select register.

14.3.1.267 REG TGPIO_CLK_SEL_REG (TGPIO_XTAL_CG_REG) — Offset 40201518h

Timed GPIO XTAL Clock Gate enable registe.

Type	Size	Offset	Default
MMIO	32 bit	40201518h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TGPIO_XTL_CG_REG:** This clock needs to be gated before writing to the clk_sel register.

14.3.1.268 Reg TGPIO_PTP_CG_REG (TGPIO_PTP_CG_REG) — Offset 4020151Ch

Timed GPIO PTP Clock Gate enable register.

Type	Size	Offset	Default
MMIO	32 bit	4020151Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TGPIO_PPT_CG_REG:** This clock needs to be gated before writing to the clk_sel register.

14.3.1.269 REG TGPIO_TS_SEL_0_REG (TGPIO_TS_SEL_0_REG) — Offset 40201520h

TGPIO input timestamp select register 0.

Type	Size	Offset	Default
MMIO	32 bit	40201520h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Select 0 (TGPIO_TS_SEL_0_REG):** TGPIO input timestamp select register 0.

14.3.1.270 REG TGPIO_TS_SEL_1_REG (TGPIO_TS_SEL_1_REG) — Offset 40201524h

TGPIO input timestamp select register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201524h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Timestamp Select 1 (TGPIO_TS_SEL_1_REG):** TGPIO input timestamp select register 1.

14.3.1.271 REG TMT_CLK_SEL_REG (TGPIO_TMT_CLK_SEL_REG) — Offset 40201528h

TMT clock select register.

Type	Size	Offset	Default
MMIO	32 bit	40201528h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**TMT Clock Select (TGPIO_TMT_CLK_SEL_REG):** TMT clock select register.

14.3.1.272 REG TGPIO_TSC_CTL_REG (TGPIO_CTS_ENABLE_REG) — Offset 40201530h

TGPIO cross timestamp control register.

Type	Size	Offset	Default
MMIO	32 bit	40201530h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW	**TMT CTS En 2 (TMT_CTS_ENABLE_REG_2):** TMT Cross Time Stamp Control [2].
3:2	0h RW	**TMT CTS En 1 (TMT_CTS_ENABLE_REG_1):** TMT Cross Time Stamp Control [1].
1:0	0h RW	**TMT CTS En 0 (TMT_CTS_ENABLE_REG_0):** TMT Cross Time Stamp Control [0].

14.3.1.273 REG TGPIO_TSC_STATUS_REG (TGPIO_CTS_VALID_REG) — Offset 40201534h

TGPIO cross timestamp status register.

Type	Size	Offset	Default
MMIO	32 bit	40201534h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RO	**TMT CTS STATUS 2 (TMT_CTS_VALID_REG_2):** TMT Cross Time Stamp Status [2].
3:2	0h RO	**TMT CTS STATUS 1 (TMT_CTS_VALID_REG_1):** TMT Cross Time Stamp Status [1].
1:0	0h RO	**TMT CTS STATUS 0 (TMT_CTS_VALID_REG_0):** TMT Cross Time Stamp Status [0].

14.3.1.274 REG TMTCTL_TSG (TMT_CTL_TSG_REG) — Offset 40201600h

TMT control register.

Type	Size	Offset	Default
MMIO	32 bit	40201600h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_TSG_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

14.3.1.275 REG TMTR_TSG (TMTR_TSG_REG) — Offset 40201604h

TMT timestamp residue register.

Type	Size	Offset	Default
MMIO	32 bit	40201604h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_TSG_REG:** TMT residue value defined with a resolution of 2^-32ns.

14.3.1.276 REG TMTL_TSG (TMTL_TSG_REG) — Offset 40201608h

TMT timestamp low register.

Type	Size	Offset	Default
MMIO	32 bit	40201608h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_TSG_REG:** Lower Half of the TMT defined in ns..

14.3.1.277 REG TMTH_TSG (TMTH_TSG_REG) — Offset 4020160Ch

TMT timestamp high register.

Type	Size	Offset	Default
MMIO	32 bit	4020160Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_TSG_REG:** Upper Half of the TMT defined in ns.

14.3.1.278 REG TIMINCA_TSG (TMT_TIMINCA_TSG_REG) — Offset 40201610h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	40201610h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_TSG_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_TSG_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

14.3.1.279 REG TIMADJ_TSG (TMT_TIMADJ_TSG_REG) — Offset 40201614h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	40201614h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_TSG_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_TSG_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_TSG_TIMADJ_TADJUS:** Time Adjust Value.

14.3.1.280 REG LXTS_TMT_HIGH_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_1) — Offset 40201618h

TMT local cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201618h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_TSG_REG:** TMTH captured when a local cross time stamp capture is enabled.

14.3.1.281 REG LXTS_TMT_LOW_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_0) — Offset 4020161Ch

TMT local cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020161Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_TSG_REG:** TMTL captured when a local cross time stamp capture is enabled.

14.3.1.282 REG LXTS_ART_HIGH_TSG (TMT_ART_SNAPSHOT_TSG_REG_1) — Offset 40201620h

TMT local cross timestamp ART snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201620h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_TSG_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

14.3.1.283 REG LXTS_ART_LOW_TSG (TMT_ART_SNAPSHOT_TSG_REG_0) — Offset 40201624h

TMT local cross timestamp ART snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40201624h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_TSG_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

14.3.1.284 REG RXTS_TMT_HIGH_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_1) — Offset 40201628h

TMT remote cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201628h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_TSG_REG:** TMTH captured when a remote time stamp capture is enabled.

14.3.1.285 REG RXTS_TMT_LOW_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_0) — Offset 4020162Ch

TMT remote cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	4020162Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_TSG_REG:** TMTL captured when a remote time stamp capture is enabled.

14.3.1.286 REG TMTCTL_GLOBAL (TMT_CTL_GLOBAL_REG) — Offset 40201640h

TMT control register.

Type	Size	Offset	Default
MMIO	32 bit	40201640h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_GLOBAL_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

14.3.1.287 REG TMTR_GLOBAL (TMTR_GLOBAL_REG) — Offset 40201644h

TMT timestamp residue register.

Type	Size	Offset	Default
MMIO	32 bit	40201644h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_GLOBAL_REG:** TMT residue value defined with a resolution of 2^-32ns.

14.3.1.288 REG TMTL_GLOBAL (TMTL_GLOBAL_REG) — Offset 40201648h

TMT timestamp low register.

Type	Size	Offset	Default
MMIO	32 bit	40201648h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_GLOBAL_REG:** Lower Half of the TMT defined in ns..

14.3.1.289 REG TMTH_GLOBAL (TMTH_GLOBAL_REG) — Offset 4020164Ch

TMT timestamp high register.

Type	Size	Offset	Default
MMIO	32 bit	4020164Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_GLOBAL_REG:** Upper Half of the TMT defined in ns.

14.3.1.290 REG TIMINCA_GLOBAL (TMT_TIMINCA_GLOBAL_REG) — Offset 40201650h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	40201650h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_GLOBAL_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_GLOBAL_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

14.3.1.291 REG TIMADJ_GLOBAL (TMT_TIMADJ_GLOBAL_REG) — Offset 40201654h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	40201654h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_GLOBAL_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_GLOBAL_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_GLOBAL_TIMADJ_TADJUS:** Time Adjust Value.

14.3.1.292 REG LXTS_TMT_LOW_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_0) — Offset 40201658h

TMT local cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40201658h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_GLOBAL_REG:** TMTL captured when a local cross time stamp capture is enabled.

14.3.1.293 REG LXTS_TMT_HIGH_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_1) — Offset 4020165Ch

TMT local cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	4020165Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_GLOBAL_REG:** TMTH captured when a local cross time stamp capture is enabled.

14.3.1.294 REG LXTS_ART_LOW_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_0) — Offset 40201660h

TMT local cross timestamp ART snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40201660h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_GLOBAL_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

14.3.1.295 REG LXTS_ART_HIGH_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_1) — Offset 40201664h

TMT local cross timestamp ART snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40201664h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_GLOBAL_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

14.3.1.296 REG RXTS_TMT_LOW_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_0) — Offset 40201668h

TMT remote cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40201668h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_GLOBAL_REG:** TMTL captured when a remote time stamp capture is enabled.

14.3.1.297 REG RXTS_TMT_HIGH_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_1) — Offset 4020166Ch

TMT remote cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	4020166Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_GLOBAL_REG:** TMTH captured when a remote time stamp capture is enabled.

14.3.1.298 REG TMTCTL_WORKING (TMT_CTL_WORKING_REG) — Offset 40201680h

TMT control register.

Type	Size	Offset	Default
MMIO	32 bit	40201680h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_WORKING_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

14.3.1.299 REG TMTR_WORKING (TMTR_WORKING_REG) — Offset 40201684h

TMT timestamp residue register.

Type	Size	Offset	Default
MMIO	32 bit	40201684h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_WORKING_REG:** TMT residue value defined with a resolution of 2^-32ns.

14.3.1.300 REG TMTL_WORKING (TMTL_WORKING_REG) — Offset 40201688h

TMT timestamp low register.

Type	Size	Offset	Default
MMIO	32 bit	40201688h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_WORKING_REG:** Lower Half of the TMT defined in ns..

14.3.1.301 REG TMTH_WORKING (TMTH_WORKING_REG) — Offset 4020168Ch

TMT timestamp high register.

Type	Size	Offset	Default
MMIO	32 bit	4020168Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_WORKING_REG:** Upper Half of the TMT defined in ns.

14.3.1.302 REG TIMINCA_WORKING (TMT_TIMINCA_WORKING_REG) — Offset 40201690h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	40201690h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_WORKING_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_WORKING_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

14.3.1.303 REG TIMADJ_WORKING (TMT_TIMADJ_WORKING_REG) — Offset 40201694h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	40201694h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_WORKING_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_WORKING_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_WORKING_TIMADJ_TADJUS:** Time Adjust Value.

14.3.1.304 REG LXTS_TMT_LOW_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_0) — Offset 40201698h

TMT local cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40201698h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_WORKING_REG:** TMTL captured when a local cross time stamp capture is enabled.

14.3.1.305 REG LXTS_TMT_HIGH_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_1) — Offset 4020169Ch

TMT local cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	4020169Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_WORKING_REG:** TMTH captured when a local cross time stamp capture is enabled.

14.3.1.306 REG LXTS_ART_LOW_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_0) — Offset 402016A0h

TMT local cross timestamp ART snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	402016A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_WORKING_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

14.3.1.307 REG LXTS_ART_HIGH_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_1) — Offset 402016A4h

TMT local cross timestamp ART snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	402016A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_WORKING_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

14.3.1.308 REG RXTS_TMT_LOW_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_0) — Offset 402016A8h

TMT remote cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	402016A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_WORKING_REG:** TMTL captured when a remote time stamp capture is enabled.

14.3.1.309 REG RXTS_TMT_HIGH_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_1) — Offset 402016ACh

TMT remote cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	402016ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_WORKING_REG:** TMTH captured when a remote time stamp capture is enabled.

14.3.2 TGPIO_1 Registers Summary

Table 14-12. Summary of TGPIO_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403010 00h	4	REG TGPIOCTL0 (TGPIO0_CTL_REG)	00002000h
403010 04h	4	REG TGPIOCOMPV0_31_0 (TGPIO0_COMPV_31_0)	00000000h
403010 08h	4	REG TGPIOCOMPV0_63_32 (TGPIO0_COMPV_63_32)	00000000h
403010 0Ch	4	REG TGPIOPIV0_31_0 (TGPIO0_PIV_31_0)	00000000h
403010 10h	4	REG TGPIOPIV0_63:32 (TGPIO0_PIV_63_32)	00000000h
403010 14h	4	REG TGPIOTCV0_31_0 (TGPIO0_TCV_31_0)	00000000h
403010 18h	4	REG TGPIOTCV0_63_32 (TGPIO0_TCV_63_32)	00000000h
403010 1Ch	4	REG TGPIOECCV0_31_0 (TGPIO0_ECCV_31_0)	00000000h
403010 20h	4	REG TGPIOECCV0_63_32 (TGPIO0_ECCV_63_32)	00000000h
403010 24h	4	REG TGPIOEC0_31_0 (TGPIO0_EC_31_0)	00000000h
403010 28h	4	REG TGPIOEC0_63_32 (TGPIO0_EC_63_32)	00000000h
403010 2Ch	4	REG TGPIOMATCHMASK0_31_0 (TGPIO0_MATCH_MASK_31_0)	00000000h
403010 30h	4	REG TGPIOMATCHMASK0_63_32 (TGPIO0_MATCH_MASK_63_32)	00000000h
403010 40h	4	REG TGPIOCTL1 (TGPIO1_CTL_REG)	00002000h
403010 44h	4	REG TGPIOCOMPV1_31_0 (TGPIO1_COMPV_31_0)	00000000h
403010 48h	4	REG TGPIOCOMPV1_63_32 (TGPIO1_COMPV_63_32)	00000000h
403010 4Ch	4	REG TGPIOPIV1_31_0 (TGPIO1_PIV_31_0)	00000000h
403010 50h	4	REG TGPIOPIV1_63:32 (TGPIO1_PIV_63_32)	00000000h
403010 54h	4	REG TGPIOTCV1_31_0 (TGPIO1_TCV_31_0)	00000000h
403010 58h	4	REG TGPIOTCV1_63_32 (TGPIO1_TCV_63_32)	00000000h
403010 5Ch	4	REG TGPIOECCV1_31_0 (TGPIO1_ECCV_31_0)	00000000h
403010 60h	4	REG TGPIOECCV1_63_32 (TGPIO1_ECCV_63_32)	00000000h
403010 64h	4	REG TGPIOEC1_31_0 (TGPIO1_EC_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403010 68h	4	REG TGPIOEC1_63_32 (TGPIO1_EC_63_32)	00000000h
403010 6Ch	4	REG TGPIOMATCHMASK1_31_0 (TGPIO1_MATCH_MASK_31_0)	00000000h
403010 70h	4	REG TGPIOMATCHMASK1_63_32 (TGPIO1_MATCH_MASK_63_32)	00000000h
403010 80h	4	REG TGPIOCTL2 (TGPIO2_CTL_REG)	00002000h
403010 84h	4	REG TGPIOCOMPV2_31_0 (TGPIO2_COMPV_31_0)	00000000h
403010 88h	4	REG TGPIOCOMPV2_63_32 (TGPIO2_COMPV_63_32)	00000000h
403010 8Ch	4	REG TGPIOPIV2_31_0 (TGPIO2_PIV_31_0)	00000000h
403010 90h	4	REG TGPIOPIV2_63:32 (TGPIO2_PIV_63_32)	00000000h
403010 94h	4	REG TGPIOTCV2_31_0 (TGPIO2_TCV_31_0)	00000000h
403010 98h	4	REG TGPIOTCV2_63_32 (TGPIO2_TCV_63_32)	00000000h
403010 9Ch	4	REG TGPIOECCV2_31_0 (TGPIO2_ECCV_31_0)	00000000h
403010 A0h	4	REG TGPIOECCV2_63_32 (TGPIO2_ECCV_63_32)	00000000h
403010 A4h	4	REG TGPIOEC2_31_0 (TGPIO2_EC_31_0)	00000000h
403010 A8h	4	REG TGPIOEC2_63_32 (TGPIO2_EC_63_32)	00000000h
403010 ACh	4	REG TGPIOMATCHMASK2_31_0 (TGPIO2_MATCH_MASK_31_0)	00000000h
403010 B0h	4	REG TGPIOMATCHMASK2_63_32 (TGPIO2_MATCH_MASK_63_32)	00000000h
403010 C0h	4	REG TGPIOCTL3 (TGPIO3_CTL_REG)	00002000h
403010 C4h	4	REG TGPIOCOMPV3_31_0 (TGPIO3_COMPV_31_0)	00000000h
403010 C8h	4	REG TGPIOCOMPV3_63_32 (TGPIO3_COMPV_63_32)	00000000h
403010 CCh	4	REG TGPIOPIV3_31_0 (TGPIO3_PIV_31_0)	00000000h
403010 D0h	4	REG TGPIOPIV3_63:32 (TGPIO3_PIV_63_32)	00000000h
403010 D4h	4	REG TGPIOTCV3_31_0 (TGPIO3_TCV_31_0)	00000000h
403010 D8h	4	REG TGPIOTCV3_63_32 (TGPIO3_TCV_63_32)	00000000h
403010 DCh	4	REG TGPIOECCV3_31_0 (TGPIO3_ECCV_31_0)	00000000h
403010 E0h	4	REG TGPIOECCV3_63_32 (TGPIO3_ECCV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403010 E4h	4	REG TGPIOEC3_31_0 (TGPIO3_EC_31_0)	00000000h
403010 E8h	4	REG TGPIOEC3_63_32 (TGPIO3_EC_63_32)	00000000h
403010 ECh	4	REG TGPIOMATCHMASK3_31_0 (TGPIO3_MATCH_MASK_31_0)	00000000h
403010 F0h	4	REG TGPIOMATCHMASK3_63_32 (TGPIO3_MATCH_MASK_63_32)	00000000h
403011 00h	4	REG TGPIOCTL4 (TGPIO4_CTL_REG)	00002000h
403011 04h	4	REG TGPIOCOMPV4_31_0 (TGPIO4_COMPV_31_0)	00000000h
403011 08h	4	REG TGPIOCOMPV4_63_32 (TGPIO4_COMPV_63_32)	00000000h
403011 0Ch	4	REG TGPIOPIV4_31_0 (TGPIO4_PIV_31_0)	00000000h
403011 10h	4	REG TGPIOPIV4_63:32 (TGPIO4_PIV_63_32)	00000000h
403011 14h	4	REG TGPIOTCV4_31_0 (TGPIO4_TCV_31_0)	00000000h
403011 18h	4	REG TGPIOTCV4_63_32 (TGPIO4_TCV_63_32)	00000000h
403011 1Ch	4	REG TGPIOECCV4_31_0 (TGPIO4_ECCV_31_0)	00000000h
403011 20h	4	REG TGPIOECCV4_63_32 (TGPIO4_ECCV_63_32)	00000000h
403011 24h	4	REG TGPIOEC4_31_0 (TGPIO4_EC_31_0)	00000000h
403011 28h	4	REG TGPIOEC4_63_32 (TGPIO4_EC_63_32)	00000000h
403011 2Ch	4	REG TGPIOMATCHMASK4_31_0 (TGPIO4_MATCH_MASK_31_0)	00000000h
403011 30h	4	REG TGPIOMATCHMASK4_63_32 (TGPIO4_MATCH_MASK_63_32)	00000000h
403011 40h	4	REG TGPIOCTL5 (TGPIO5_CTL_REG)	00002000h
403011 44h	4	REG TGPIOCOMPV5_31_0 (TGPIO5_COMPV_31_0)	00000000h
403011 48h	4	REG TGPIOCOMPV5_63_32 (TGPIO5_COMPV_63_32)	00000000h
403011 4Ch	4	REG TGPIOPIV5_31_0 (TGPIO5_PIV_31_0)	00000000h
403011 50h	4	REG TGPIOPIV5_63:32 (TGPIO5_PIV_63_32)	00000000h
403011 54h	4	REG TGPIOTCV5_31_0 (TGPIO5_TCV_31_0)	00000000h
403011 58h	4	REG TGPIOTCV5_63_32 (TGPIO5_TCV_63_32)	00000000h
403011 5Ch	4	REG TGPIOECCV5_31_0 (TGPIO5_ECCV_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403011 60h	4	REG TGPIOECCV5_63_32 (TGPIO5_ECCV_63_32)	00000000h
403011 64h	4	REG TGPIOEC5_31_0 (TGPIO5_EC_31_0)	00000000h
403011 68h	4	REG TGPIOEC5_63_32 (TGPIO5_EC_63_32)	00000000h
403011 6Ch	4	REG TGPIOMATCHMASK5_31_0 (TGPIO5_MATCH_MASK_31_0)	00000000h
403011 70h	4	REG TGPIOMATCHMASK5_63_32 (TGPIO5_MATCH_MASK_63_32)	00000000h
403011 80h	4	REG TGPIOCTL6 (TGPIO6_CTL_REG)	00002000h
403011 84h	4	REG TGPIOCOMPV6_31_0 (TGPIO6_COMPV_31_0)	00000000h
403011 88h	4	REG TGPIOCOMPV6_63_32 (TGPIO6_COMPV_63_32)	00000000h
403011 8Ch	4	REG TGPIOPIV6_31_0 (TGPIO6_PIV_31_0)	00000000h
403011 90h	4	REG TGPIOPIV6_63:32 (TGPIO6_PIV_63_32)	00000000h
403011 94h	4	REG TGPIOTCV6_31_0 (TGPIO6_TCV_31_0)	00000000h
403011 98h	4	REG TGPIOTCV6_63_32 (TGPIO6_TCV_63_32)	00000000h
403011 9Ch	4	REG TGPIOECCV6_31_0 (TGPIO6_ECCV_31_0)	00000000h
403011 A0h	4	REG TGPIOECCV6_63_32 (TGPIO6_ECCV_63_32)	00000000h
403011 A4h	4	REG TGPIOEC6_31_0 (TGPIO6_EC_31_0)	00000000h
403011 A8h	4	REG TGPIOEC6_63_32 (TGPIO6_EC_63_32)	00000000h
403011 ACh	4	REG TGPIOMATCHMASK6_31_0 (TGPIO6_MATCH_MASK_31_0)	00000000h
403011 B0h	4	REG TGPIOMATCHMASK6_63_32 (TGPIO6_MATCH_MASK_63_32)	00000000h
403011 C0h	4	REG TGPIOCTL7 (TGPIO7_CTL_REG)	00002000h
403011 C4h	4	REG TGPIOCOMPV7_31_0 (TGPIO7_COMPV_31_0)	00000000h
403011 C8h	4	REG TGPIOCOMPV7_63_32 (TGPIO7_COMPV_63_32)	00000000h
403011 CCh	4	REG TGPIOPIV7_31_0 (TGPIO7_PIV_31_0)	00000000h
403011 D0h	4	REG TGPIOPIV7_63:32 (TGPIO7_PIV_63_32)	00000000h
403011 D4h	4	REG TGPIOTCV7_31_0 (TGPIO7_TCV_31_0)	00000000h
403011 D8h	4	REG TGPIOTCV7_63_32 (TGPIO7_TCV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403011 DCh	4	REG TGPIOECCV7_31_0 (TGPIO7_ECCV_31_0)	00000000h
403011 E0h	4	REG TGPIOECCV7_63_32 (TGPIO7_ECCV_63_32)	00000000h
403011 E4h	4	REG TGPIOEC7_31_0 (TGPIO7_EC_31_0)	00000000h
403011 E8h	4	REG TGPIOEC7_63_32 (TGPIO7_EC_63_32)	00000000h
403011 ECh	4	REG TGPIOMATCHMASK7_31_0 (TGPIO7_MATCH_MASK_31_0)	00000000h
403011 F0h	4	REG TGPIOMATCHMASK7_63_32 (TGPIO7_MATCH_MASK_63_32)	00000000h
403012 00h	4	REG TGPIOCTL8 (TGPIO8_CTL_REG)	00002000h
403012 04h	4	REG TGPIOCOMPV8_31_0 (TGPIO8_COMPV_31_0)	00000000h
403012 08h	4	REG TGPIOCOMPV8_63_32 (TGPIO8_COMPV_63_32)	00000000h
403012 0Ch	4	REG TGPIOPIV8_31_0 (TGPIO8_PIV_31_0)	00000000h
403012 10h	4	REG TGPIOPIV8_63:32 (TGPIO8_PIV_63_32)	00000000h
403012 14h	4	REG TGPIOTCV8_31_0 (TGPIO8_TCV_31_0)	00000000h
403012 18h	4	REG TGPIOTCV8_63_32 (TGPIO8_TCV_63_32)	00000000h
403012 1Ch	4	REG TGPIOECCV8_31_0 (TGPIO8_ECCV_31_0)	00000000h
403012 20h	4	REG TGPIOECCV8_63_32 (TGPIO8_ECCV_63_32)	00000000h
403012 24h	4	REG TGPIOEC8_31_0 (TGPIO8_EC_31_0)	00000000h
403012 28h	4	REG TGPIOEC8_63_32 (TGPIO8_EC_63_32)	00000000h
403012 2Ch	4	REG TGPIOMATCHMASK8_31_0 (TGPIO8_MATCH_MASK_31_0)	00000000h
403012 30h	4	REG TGPIOMATCHMASK8_63_32 (TGPIO8_MATCH_MASK_63_32)	00000000h
403012 40h	4	REG TGPIOCTL9 (TGPIO9_CTL_REG)	00002000h
403012 44h	4	REG TGPIOCOMPV9_31_0 (TGPIO9_COMPV_31_0)	00000000h
403012 48h	4	REG TGPIOCOMPV9_63_32 (TGPIO9_COMPV_63_32)	00000000h
403012 4Ch	4	REG TGPIOPIV9_31_0 (TGPIO9_PIV_31_0)	00000000h
403012 50h	4	REG TGPIOPIV9_63:32 (TGPIO9_PIV_63_32)	00000000h
403012 54h	4	REG TGPIOTCV9_31_0 (TGPIO9_TCV_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403012 58h	4	REG TGPIOTCV9_63_32 (TGPIO9_TCV_63_32)	00000000h
403012 5Ch	4	REG TGPIOECCV9_31_0 (TGPIO9_ECCV_31_0)	00000000h
403012 60h	4	REG TGPIOECCV9_63_32 (TGPIO9_ECCV_63_32)	00000000h
403012 64h	4	REG TGPIOEC9_31_0 (TGPIO9_EC_31_0)	00000000h
403012 68h	4	REG TGPIOEC9_63_32 (TGPIO9_EC_63_32)	00000000h
403012 6Ch	4	REG TGPIOMATCHMASK9_31_0 (TGPIO9_MATCH_MASK_31_0)	00000000h
403012 70h	4	REG TGPIOMATCHMASK9_63_32 (TGPIO9_MATCH_MASK_63_32)	00000000h
403012 80h	4	REG TGPIOCTL10 (TGPIO10_CTL_REG)	00002000h
403012 84h	4	REG TGPIOCOMPV10_31_0 (TGPIO10_COMPV_31_0)	00000000h
403012 88h	4	REG TGPIOCOMPV10_63_32 (TGPIO10_COMPV_63_32)	00000000h
403012 8Ch	4	REG TGPIOPIV10_31_0 (TGPIO10_PIV_31_0)	00000000h
403012 90h	4	REG TGPIOPIV10_63:32 (TGPIO10_PIV_63_32)	00000000h
403012 94h	4	REG TGPIOTCV10_31_0 (TGPIO10_TCV_31_0)	00000000h
403012 98h	4	REG TGPIOTCV10_63_32 (TGPIO10_TCV_63_32)	00000000h
403012 9Ch	4	REG TGPIOECCV10_31_0 (TGPIO10_ECCV_31_0)	00000000h
403012 A0h	4	REG TGPIOECCV10_63_32 (TGPIO10_ECCV_63_32)	00000000h
403012 A4h	4	REG TGPIOEC10_31_0 (TGPIO10_EC_31_0)	00000000h
403012 A8h	4	REG TGPIOEC10_63_32 (TGPIO10_EC_63_32)	00000000h
403012 ACh	4	REG TGPIOMATCHMASK10_31_0 (TGPIO10_MATCH_MASK_31_0)	00000000h
403012 B0h	4	REG TGPIOMATCHMASK10_63_32 (TGPIO10_MATCH_MASK_63_32)	00000000h
403012 C0h	4	REG TGPIOCTL11 (TGPIO11_CTL_REG)	00002000h
403012 C4h	4	REG TGPIOCOMPV11_31_0 (TGPIO11_COMPV_31_0)	00000000h
403012 C8h	4	REG TGPIOCOMPV11_63_32 (TGPIO11_COMPV_63_32)	00000000h
403012 CCh	4	REG TGPIOPIV11_31_0 (TGPIO11_PIV_31_0)	00000000h
403012 D0h	4	REG TGPIOPIV11_63:32 (TGPIO11_PIV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403012 D4h	4	REG TGPIOTCV11_31_0 (TGPIO11_TCV_31_0)	00000000h
403012 D8h	4	REG TGPIOTCV11_63_32 (TGPIO11_TCV_63_32)	00000000h
403012 DCh	4	REG TGPIOECCV11_31_0 (TGPIO11_ECCV_31_0)	00000000h
403012 E0h	4	REG TGPIOECCV11_63_32 (TGPIO11_ECCV_63_32)	00000000h
403012 E4h	4	REG TGPIOEC11_31_0 (TGPIO11_EC_31_0)	00000000h
403012 E8h	4	REG TGPIOEC11_63_32 (TGPIO11_EC_63_32)	00000000h
403012 ECh	4	REG TGPIOMATCHMASK11_31_0 (TGPIO11_MATCH_MASK_31_0)	00000000h
403012 F0h	4	REG TGPIOMATCHMASK11_63_32 (TGPIO11_MATCH_MASK_63_32)	00000000h
403013 00h	4	REG TGPIOCTL12 (TGPIO12_CTL_REG)	00002000h
403013 04h	4	REG TGPIOCOMPV12_31_0 (TGPIO12_COMPV_31_0)	00000000h
403013 08h	4	REG TGPIOCOMPV12_63_32 (TGPIO12_COMPV_63_32)	00000000h
403013 0Ch	4	REG TGPIOPIV12_31_0 (TGPIO12_PIV_31_0)	00000000h
403013 10h	4	REG TGPIOPIV12_63:32 (TGPIO12_PIV_63_32)	00000000h
403013 14h	4	REG TGPIOTCV12_31_0 (TGPIO12_TCV_31_0)	00000000h
403013 18h	4	REG TGPIOTCV12_63_32 (TGPIO12_TCV_63_32)	00000000h
403013 1Ch	4	REG TGPIOECCV12_31_0 (TGPIO12_ECCV_31_0)	00000000h
403013 20h	4	REG TGPIOECCV12_63_32 (TGPIO12_ECCV_63_32)	00000000h
403013 24h	4	REG TGPIOEC12_31_0 (TGPIO12_EC_31_0)	00000000h
403013 28h	4	REG TGPIOEC12_63_32 (TGPIO12_EC_63_32)	00000000h
403013 2Ch	4	REG TGPIOMATCHMASK12_31_0 (TGPIO12_MATCH_MASK_31_0)	00000000h
403013 30h	4	REG TGPIOMATCHMASK12_63_32 (TGPIO12_MATCH_MASK_63_32)	00000000h
403013 40h	4	REG TGPIOCTL13 (TGPIO13_CTL_REG)	00002000h
403013 44h	4	REG TGPIOCOMPV13_31_0 (TGPIO13_COMPV_31_0)	00000000h
403013 48h	4	REG TGPIOCOMPV13_63_32 (TGPIO13_COMPV_63_32)	00000000h
403013 4Ch	4	REG TGPIOPIV13_31_0 (TGPIO13_PIV_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403013 50h	4	REG TGPIOPIV13_63:32 (TGPIO13_PIV_63_32)	00000000h
403013 54h	4	REG TGPIOTCV13_31_0 (TGPIO13_TCV_31_0)	00000000h
403013 58h	4	REG TGPIOTCV13_63_32 (TGPIO13_TCV_63_32)	00000000h
403013 5Ch	4	REG TGPIOECCV13_31_0 (TGPIO13_ECCV_31_0)	00000000h
403013 60h	4	REG TGPIOECCV13_63_32 (TGPIO13_ECCV_63_32)	00000000h
403013 64h	4	REG TGPIOEC13_31_0 (TGPIO13_EC_31_0)	00000000h
403013 68h	4	REG TGPIOEC13_63_32 (TGPIO13_EC_63_32)	00000000h
403013 6Ch	4	REG TGPIOMATCHMASK13_31_0 (TGPIO13_MATCH_MASK_31_0)	00000000h
403013 70h	4	REG TGPIOMATCHMASK13_63_32 (TGPIO13_MATCH_MASK_63_32)	00000000h
403013 80h	4	REG TGPIOCTL14 (TGPIO14_CTL_REG)	00002000h
403013 84h	4	REG TGPIOCOMPV14_31_0 (TGPIO14_COMPV_31_0)	00000000h
403013 88h	4	REG TGPIOCOMPV14_63_32 (TGPIO14_COMPV_63_32)	00000000h
403013 8Ch	4	REG TGPIOPIV14_31_0 (TGPIO14_PIV_31_0)	00000000h
403013 90h	4	REG TGPIOPIV14_63:32 (TGPIO14_PIV_63_32)	00000000h
403013 94h	4	REG TGPIOTCV14_31_0 (TGPIO14_TCV_31_0)	00000000h
403013 98h	4	REG TGPIOTCV14_63_32 (TGPIO14_TCV_63_32)	00000000h
403013 9Ch	4	REG TGPIOECCV14_31_0 (TGPIO14_ECCV_31_0)	00000000h
403013 A0h	4	REG TGPIOECCV14_63_32 (TGPIO14_ECCV_63_32)	00000000h
403013 A4h	4	REG TGPIOEC14_31_0 (TGPIO14_EC_31_0)	00000000h
403013 A8h	4	REG TGPIOEC14_63_32 (TGPIO14_EC_63_32)	00000000h
403013 ACh	4	REG TGPIOMATCHMASK14_31_0 (TGPIO14_MATCH_MASK_31_0)	00000000h
403013 B0h	4	REG TGPIOMATCHMASK14_63_32 (TGPIO14_MATCH_MASK_63_32)	00000000h
403013 C0h	4	REG TGPIOCTL15 (TGPIO15_CTL_REG)	00002000h
403013 C4h	4	REG TGPIOCOMPV15_31_0 (TGPIO15_COMPV_31_0)	00000000h
403013 C8h	4	REG TGPIOCOMPV15_63_32 (TGPIO15_COMPV_63_32)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403013 CCh	4	REG TGPIOPIV15_31_0 (TGPIO15_PIV_31_0)	00000000h
403013 D0h	4	REG TGPIOPIV15_63:32 (TGPIO15_PIV_63_32)	00000000h
403013 D4h	4	REG TGPIOTCV15_31_0 (TGPIO15_TCV_31_0)	00000000h
403013 D8h	4	REG TGPIOTCV15_63_32 (TGPIO15_TCV_63_32)	00000000h
403013 DCh	4	REG TGPIOECCV15_31_0 (TGPIO15_ECCV_31_0)	00000000h
403013 E0h	4	REG TGPIOECCV15_63_32 (TGPIO15_ECCV_63_32)	00000000h
403013 E4h	4	REG TGPIOEC15_31_0 (TGPIO15_EC_31_0)	00000000h
403013 E8h	4	REG TGPIOEC15_63_32 (TGPIO15_EC_63_32)	00000000h
403013 ECh	4	REG TGPIOMATCHMASK15_31_0 (TGPIO15_MATCH_MASK_31_0)	00000000h
403013 F0h	4	REG TGPIOMATCHMASK15_63_32 (TGPIO15_MATCH_MASK_63_32)	00000000h
403014 00h	4	REG TGPIOCTL16 (TGPIO16_CTL_REG)	00002000h
403014 04h	4	REG TGPIOCOMPV16_31_0 (TGPIO16_COMPV_31_0)	00000000h
403014 08h	4	REG TGPIOCOMPV16_63_32 (TGPIO16_COMPV_63_32)	00000000h
403014 0Ch	4	REG TGPIOPIV16_31_0 (TGPIO16_PIV_31_0)	00000000h
403014 10h	4	REG TGPIOPIV16_63:32 (TGPIO16_PIV_63_32)	00000000h
403014 14h	4	REG TGPIOTCV16_31_0 (TGPIO16_TCV_31_0)	00000000h
403014 18h	4	REG TGPIOTCV16_63_32 (TGPIO16_TCV_63_32)	00000000h
403014 1Ch	4	REG TGPIOECCV16_31_0 (TGPIO16_ECCV_31_0)	00000000h
403014 20h	4	REG TGPIOECCV16_63_32 (TGPIO16_ECCV_63_32)	00000000h
403014 24h	4	REG TGPIOEC16_31_0 (TGPIO16_EC_31_0)	00000000h
403014 28h	4	REG TGPIOEC16_63_32 (TGPIO16_EC_63_32)	00000000h
403014 2Ch	4	REG TGPIOMATCHMASK16_31_0 (TGPIO16_MATCH_MASK_31_0)	00000000h
403014 30h	4	REG TGPIOMATCHMASK16_63_32 (TGPIO16_MATCH_MASK_63_32)	00000000h
403014 40h	4	REG TGPIOCTL17 (TGPIO17_CTL_REG)	00002000h
403014 44h	4	REG TGPIOCOMPV17_31_0 (TGPIO17_COMPV_31_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403014 48h	4	REG TGPIOCOMPV17_63_32 (TGPIO17_COMPV_63_32)	00000000h
403014 4Ch	4	REG TGPIOPIV17_31_0 (TGPIO17_PIV_31_0)	00000000h
403014 50h	4	REG TGPIOPIV17_63:32 (TGPIO17_PIV_63_32)	00000000h
403014 54h	4	REG TGPIOTCV17_31_0 (TGPIO17_TCV_31_0)	00000000h
403014 58h	4	REG TGPIOTCV17_63_32 (TGPIO17_TCV_63_32)	00000000h
403014 5Ch	4	REG TGPIOECCV17_31_0 (TGPIO17_ECCV_31_0)	00000000h
403014 60h	4	REG TGPIOECCV17_63_32 (TGPIO17_ECCV_63_32)	00000000h
403014 64h	4	REG TGPIOEC17_31_0 (TGPIO17_EC_31_0)	00000000h
403014 68h	4	REG TGPIOEC17_63_32 (TGPIO17_EC_63_32)	00000000h
403014 6Ch	4	REG TGPIOMATCHMASK17_31_0 (TGPIO17_MATCH_MASK_31_0)	00000000h
403014 70h	4	REG TGPIOMATCHMASK17_63_32 (TGPIO17_MATCH_MASK_63_32)	00000000h
403014 80h	4	REG TGPIOCTL18 (TGPIO18_CTL_REG)	00002000h
403014 84h	4	REG TGPIOCOMPV18_31_0 (TGPIO18_COMPV_31_0)	00000000h
403014 88h	4	REG TGPIOCOMPV18_63_32 (TGPIO18_COMPV_63_32)	00000000h
403014 8Ch	4	REG TGPIOPIV18_31_0 (TGPIO18_PIV_31_0)	00000000h
403014 90h	4	REG TGPIOPIV18_63:32 (TGPIO18_PIV_63_32)	00000000h
403014 94h	4	REG TGPIOTCV18_31_0 (TGPIO18_TCV_31_0)	00000000h
403014 98h	4	REG TGPIOTCV18_63_32 (TGPIO18_TCV_63_32)	00000000h
403014 9Ch	4	REG TGPIOECCV18_31_0 (TGPIO18_ECCV_31_0)	00000000h
403014 A0h	4	REG TGPIOECCV18_63_32 (TGPIO18_ECCV_63_32)	00000000h
403014 A4h	4	REG TGPIOEC18_31_0 (TGPIO18_EC_31_0)	00000000h
403014 A8h	4	REG TGPIOEC18_63_32 (TGPIO18_EC_63_32)	00000000h
403014 ACh	4	REG TGPIOMATCHMASK18_31_0 (TGPIO18_MATCH_MASK_31_0)	00000000h
403014 B0h	4	REG TGPIOMATCHMASK18_63_32 (TGPIO18_MATCH_MASK_63_32)	00000000h
403014 C0h	4	REG TGPIOCTL19 (TGPIO19_CTL_REG)	00002000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403014 C4h	4	REG TGPIOCOMPV19_31_0 (TGPIO19_COMPV_31_0)	00000000h
403014 C8h	4	REG TGPIOCOMPV19_63_32 (TGPIO19_COMPV_63_32)	00000000h
403014 CCh	4	REG TGPIOPIV19_31_0 (TGPIO19_PIV_31_0)	00000000h
403014 D0h	4	REG TGPIOPIV19_63:32 (TGPIO19_PIV_63_32)	00000000h
403014 D4h	4	REG TGPIOTCV19_31_0 (TGPIO19_TCV_31_0)	00000000h
403014 D8h	4	REG TGPIOTCV19_63_32 (TGPIO19_TCV_63_32)	00000000h
403014 DCh	4	REG TGPIOECCV19_31_0 (TGPIO19_ECCV_31_0)	00000000h
403014 E0h	4	REG TGPIOECCV19_63_32 (TGPIO19_ECCV_63_32)	00000000h
403014 E4h	4	REG TGPIOEC19_31_0 (TGPIO19_EC_31_0)	00000000h
403014 E8h	4	REG TGPIOEC19_63_32 (TGPIO19_EC_63_32)	00000000h
403014 ECh	4	REG TGPIOMATCHMASK19_31_0 (TGPIO19_MATCH_MASK_31_0)	00000000h
403014 F0h	4	REG TGPIOMATCHMASK19_63_32 (TGPIO19_MATCH_MASK_63_32)	00000000h
403015 00h	4	REG TGPIOINTRCTL (TGPIO_INTR_CTL_REG)	00000000h
403015 04h	4	REG TGPIORIS (TGPIO_INTR_RIS_REG)	00000000h
403015 08h	4	REG TGPIOMSC (TGPIO_INTR_MSC_REG)	00000000h
403015 0Ch	4	REG TGPIOMIS (TGPIO_INTR_MIS_REG)	00000000h
403015 10h	4	REG TGPIOICR (TGPIO_INTR_ICR_REG)	00000000h
403015 14h	4	REG TGPIO_CLK_SEL_REG (TGPIO_CLK_SEL_REG)	00000000h
403015 18h	4	REG TGPIO_CLK_SEL_REG (TGPIO_XTAL_CG_REG)	00000000h
403015 1Ch	4	Reg TGPIO_PTP_CG_REG (TGPIO_PTP_CG_REG)	00000000h
403015 20h	4	REG TGPIO_TS_SEL_0_REG (TGPIO_TS_SEL_0_REG)	00000000h
403015 24h	4	REG TGPIO_TS_SEL_1_REG (TGPIO_TS_SEL_1_REG)	00000000h
403015 28h	4	REG TMT_CLK_SEL_REG (TGPIO_TMT_CLK_SEL_REG)	00000000h
403015 30h	4	REG TGPIO_TSC_CTL_REG (TGPIO_CTS_ENABLE_REG)	00000000h
403015 34h	4	REG TGPIO_TSC_STATUS_REG (TGPIO_CTS_VALID_REG)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403016 00h	4	REG TMTCTL_TSG (TMT_CTL_TSG_REG)	00000000h
403016 04h	4	REG TMTR_TSG (TMTR_TSG_REG)	00000000h
403016 08h	4	REG TMTL_TSG (TMTL_TSG_REG)	00000000h
403016 0Ch	4	REG TMTH_TSG (TMTH_TSG_REG)	00000000h
403016 10h	4	REG TIMINCA_TSG (TMT_TIMINCA_TSG_REG)	00000000h
403016 14h	4	REG TIMADJ_TSG (TMT_TIMADJ_TSG_REG)	00000000h
403016 18h	4	REG LXTS_TMT_HIGH_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_1)	00000000h
403016 1Ch	4	REG LXTS_TMT_LOW_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_0)	00000000h
403016 20h	4	REG LXTS_ART_HIGH_TSG (TMT_ART_SNAPSHOT_TSG_REG_1)	00000000h
403016 24h	4	REG LXTS_ART_LOW_TSG (TMT_ART_SNAPSHOT_TSG_REG_0)	00000000h
403016 28h	4	REG RXTS_TMT_HIGH_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_1)	00000000h
403016 2Ch	4	REG RXTS_TMT_LOW_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_0)	00000000h
403016 40h	4	REG TMTCTL_GLOBAL (TMT_CTL_GLOBAL_REG)	00000000h
403016 44h	4	REG TMTR_GLOBAL (TMTR_GLOBAL_REG)	00000000h
403016 48h	4	REG TMTL_GLOBAL (TMTL_GLOBAL_REG)	00000000h
403016 4Ch	4	REG TMTH_GLOBAL (TMTH_GLOBAL_REG)	00000000h
403016 50h	4	REG TIMINCA_GLOBAL (TMT_TIMINCA_GLOBAL_REG)	00000000h
403016 54h	4	REG TIMADJ_GLOBAL (TMT_TIMADJ_GLOBAL_REG)	00000000h
403016 58h	4	REG LXTS_TMT_LOW_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_0)	00000000h
403016 5Ch	4	REG LXTS_TMT_HIGH_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_1)	00000000h
403016 60h	4	REG LXTS_ART_LOW_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_0)	00000000h
403016 64h	4	REG LXTS_ART_HIGH_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_1)	00000000h
403016 68h	4	REG RXTS_TMT_LOW_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_0)	00000000h
403016 6Ch	4	REG RXTS_TMT_HIGH_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_1)	00000000h
403016 80h	4	REG TMTCTL_WORKING (TMT_CTL_WORKING_REG)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
403016 84h	4	REG TMTR_WORKING (TMTR_WORKING_REG)	00000000h
403016 88h	4	REG TMTL_WORKING (TMTL_WORKING_REG)	00000000h
403016 8Ch	4	REG TMTH_WORKING (TMTH_WORKING_REG)	00000000h
403016 90h	4	REG TIMINCA_WORKING (TMT_TIMINCA_WORKING_REG)	00000000h
403016 94h	4	REG TIMADJ_WORKING (TMT_TIMADJ_WORKING_REG)	00000000h
403016 98h	4	REG LXTS_TMT_LOW_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_0)	00000000h
403016 9Ch	4	REG LXTS_TMT_HIGH_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_1)	00000000h
403016 A0h	4	REG LXTS_ART_LOW_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_0)	00000000h
403016 A4h	4	REG LXTS_ART_HIGH_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_1)	00000000h
403016 A8h	4	REG RXTS_TMT_LOW_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_0)	00000000h
403016 ACh	4	REG RXTS_TMT_HIGH_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_1)	00000000h

14.3.2.1 REG TGPIOCTL0 (TGPIO0_CTL_REG) — Offset 40301000h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301000h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO0_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO0_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	**Input Event Control (TGPIO0_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 - reserved .
13	1h RW	**Freeze Input Timestamp (TGPIO0_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO0_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.
8:5	0h RW	**Pulse Width Stretch (TGPIO0_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO0_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO0_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved .
1	0h RW	**Direction (DIR) (TGPIO0_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO0_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.2 REG TGPIOCOMPV0_31_0 (TGPIO0_COMPV_31_0) — Offset 40301004h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO0_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.3 REG TGPIOCOMPV0_63_32 (TGPIO0_COMPV_63_32) — Offset 40301008h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO0_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.4 REG TGPIOPIV0_31_0 (TGPIO0_PIV_31_0) — Offset 4030100Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.5 REG TGPIOPIV0_63:32 (TGPIO0_PIV_63_32) — Offset 40301010h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.6 REG TGPIOTCV0_31_0 (TGPIO0_TCV_31_0) — Offset 40301014h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.7 REG TGPIOTCV0_63_32 (TGPIO0_TCV_63_32) — Offset 40301018h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.8 REG TGPIOECCV0_31_0 (TGPIO0_ECCV_31_0) — Offset 4030101Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030101Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.9 REG TGPIOECCV0_63_32 (TGPIO0_ECCV_63_32) — Offset 40301020h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.10 REG TGPIOEC0_31_0 (TGPIO0_EC_31_0) — Offset 40301024h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.11 REG TGPIOEC0_63_32 (TGPIO0_EC_63_32) — Offset 40301028h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO0_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.12 REG TGPIOMATCHMASK0_31_0 (TGPIO0_MATCH_MASK_31_0) — Offset 4030102Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030102Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.13 REG TGPIOMATCHMASK0_63_32 (TGPIO0_MATCH_MASK_63_32) — Offset 40301030h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO0_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.14 REG TGPIOCTL1 (TGPIO1_CTL_REG) — Offset 40301040h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301040h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO1_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO1_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO1_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO1_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO1_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO1_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO1_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO1_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO1_CTL_DIR_O):** 0 Output 1 Input .
0	0h RW	**Enable (EN) (TGPIO1_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled .

14.3.2.15 REG TGPIOCOMPV1_31_0 (TGPIO1_COMPV_31_0) — Offset 40301044h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO1_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.16 REG TGPIOCOMPV1_63_32 (TGPIO1_COMPV_63_32) — Offset 40301048h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO1_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.17 REG TGPIOPIV1_31_0 (TGPIO1_PIV_31_0) — Offset 4030104Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030104Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.18 REG TGPIOPIV1_63:32 (TGPIO1_PIV_63_32) — Offset 40301050h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.19 REG TGPIOTCV1_31_0 (TGPIO1_TCV_31_0) — Offset 40301054h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.20 REG TGPIOTCV1_63_32 (TGPIO1_TCV_63_32) — Offset 40301058h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.21 REG TGPIOECCV1_31_0 (TGPIO1_ECCV_31_0) — Offset 4030105Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030105Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.22 REG TGPIOECCV1_63_32 (TGPIO1_ECCV_63_32) — Offset 40301060h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.23 REG TGPIOEC1_31_0 (TGPIO1_EC_31_0) — Offset 40301064h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.24 REG TGPIOEC1_63_32 (TGPIO1_EC_63_32) — Offset 40301068h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO1_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.25 REG TGPIOMATCHMASK1_31_0 (TGPIO1_MATCH_MASK_31_0) — Offset 4030106Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030106Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.26 REG TGPIOMATCHMASK1_63_32 (TGPIO1_MATCH_MASK_63_32) — Offset 40301070h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO1_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.27 REG TGPIOCTL2 (TGPIO2_CTL_REG) — Offset 40301080h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301080h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO2_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO2_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO2_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO2_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO2_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO2_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO2_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO2_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO2_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO2_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.28 REG TGPIOCOMPV2_31_0 (TGPIO2_COMPV_31_0) — Offset 40301084h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO2_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.29 REG TGPIOCOMPV2_63_32 (TGPIO2_COMPV_63_32) — Offset 40301088h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO2_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.30 REG TGPIOPIV2_31_0 (TGPIO2_PIV_31_0) — Offset 4030108Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030108Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.31 REG TGPIOPIV2_63:32 (TGPIO2_PIV_63_32) — Offset 40301090h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.32 REG TGPIOTCV2_31_0 (TGPIO2_TCV_31_0) — Offset 40301094h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.33 REG TGPIOTCV2_63_32 (TGPIO2_TCV_63_32) — Offset 40301098h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.34 REG TGPIOECCV2_31_0 (TGPIO2_ECCV_31_0) — Offset 4030109Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030109Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.35 REG TGPIOECCV2_63_32 (TGPIO2_ECCV_63_32) — Offset 403010A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.36 REG TGPIOEC2_31_0 (TGPIO2_EC_31_0) — Offset 403010A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403010A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.37 REG TGPIOEC2_63_32 (TGPIO2_EC_63_32) — Offset 403010A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO2_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.38 REG TGPIOMATCHMASK2_31_0 (TGPIO2_MATCH_MASK_31_0) — Offset 403010ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403010ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.39 REG TGPIOMATCHMASK2_63_32 (TGPIO2_MATCH_MASK_63_32) — Offset 403010B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403010B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO2_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.40 REG TGPIOCTL3 (TGPIO3_CTL_REG) — Offset 403010C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	403010C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO3_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO3_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO3_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO3_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO3_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO3_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO3_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO3_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO3_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO3_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.41 REG TGPIOCOMPV3_31_0 (TGPIO3_COMPV_31_0) — Offset 403010C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403010C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO3_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.42 REG TGPIOCOMPV3_63_32 (TGPIO3_COMPV_63_32) — Offset 403010C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO3_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.43 REG TGPIOPIV3_31_0 (TGPIO3_PIV_31_0) — Offset 403010CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	403010CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.44 REG TGPIOPIV3_63:32 (TGPIO3_PIV_63_32) — Offset 403010D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.45 REG TGPIOTCV3_31_0 (TGPIO3_TCV_31_0) — Offset 403010D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403010D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.46 REG TGPIOTCV3_63_32 (TGPIO3_TCV_63_32) — Offset 403010D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.47 REG TGPIOECCV3_31_0 (TGPIO3_ECCV_31_0) — Offset 403010DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	403010DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.48 REG TGPIOECCV3_63_32 (TGPIO3_ECCV_63_32) — Offset 403010E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.49 REG TGPIOEC3_31_0 (TGPIO3_EC_31_0) — Offset 403010E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403010E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.50 REG TGPIOEC3_63_32 (TGPIO3_EC_63_32) — Offset 403010E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403010E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO3_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. .

14.3.2.51 REG TGPIOMATCHMASK3_31_0 (TGPIO3_MATCH_MASK_31_0) — Offset 403010ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403010ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.52 REG TGPIOMATCHMASK3_63_32 (TGPIO3_MATCH_MASK_63_32) — Offset 403010F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403010F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO3_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.53 REG TGPIOCTL4 (TGPIO4_CTL_REG) — Offset 40301100h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301100h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO4_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO4_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO4_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO4_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO4_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO4_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO4_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO4_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO4_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO4_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.54 REG TGPIOCOMPV4_31_0 (TGPIO4_COMPV_31_0) — Offset 40301104h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO4_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.55 REG TGPIOCOMPV4_63_32 (TGPIO4_COMPV_63_32) — Offset 40301108h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO4_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.56 REG TGPIOPIV4_31_0 (TGPIO4_PIV_31_0) — Offset 4030110Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030110Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.57 REG TGPIOPIV4_63:32 (TGPIO4_PIV_63_32) — Offset 40301110h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.58 REG TGPIOTCV4_31_0 (TGPIO4_TCV_31_0) — Offset 40301114h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.59 REG TGPIOTCV4_63_32 (TGPIO4_TCV_63_32) — Offset 40301118h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.60 REG TGPIOECCV4_31_0 (TGPIO4_ECCV_31_0) — Offset 4030111Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030111Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.61 REG TGPIOECCV4_63_32 (TGPIO4_ECCV_63_32) — Offset 40301120h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.62 REG TGPIOEC4_31_0 (TGPIO4_EC_31_0) — Offset 40301124h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.63 REG TGPIOEC4_63_32 (TGPIO4_EC_63_32) — Offset 40301128h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO4_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.64 REG TGPIOMATCHMASK4_31_0 (TGPIO4_MATCH_MASK_31_0) — Offset 4030112Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030112Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.65 REG TGPIOMATCHMASK4_63_32 (TGPIO4_MATCH_MASK_63_32) — Offset 40301130h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO4_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.66 REG TGPIOCTL5 (TGPIO5_CTL_REG) — Offset 40301140h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301140h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO5_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO5_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO5_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO5_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO5_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO5_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO5_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO5_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO5_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO5_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.67 REG TGPIOCOMPV5_31_0 (TGPIO5_COMPV_31_0) — Offset 40301144h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO5_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.68 REG TGPIOCOMPV5_63_32 (TGPIO5_COMPV_63_32) — Offset 40301148h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO5_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.69 REG TGPIOPIV5_31_0 (TGPIO5_PIV_31_0) — Offset 4030114Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030114Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.70 REG TGPIOPIV5_63:32 (TGPIO5_PIV_63_32) — Offset 40301150h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.71 REG TGPIOTCV5_31_0 (TGPIO5_TCV_31_0) — Offset 40301154h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301154h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.72 REG TGPIOTCV5_63_32 (TGPIO5_TCV_63_32) — Offset 40301158h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.73 REG TGPIOECCV5_31_0 (TGPIO5_ECCV_31_0) — Offset 4030115Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030115Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.74 REG TGPIOECCV5_63_32 (TGPIO5_ECCV_63_32) — Offset 40301160h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.75 REG TGPIOEC5_31_0 (TGPIO5_EC_31_0) — Offset 40301164h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.76 REG TGPIOEC5_63_32 (TGPIO5_EC_63_32) — Offset 40301168h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO5_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.77 REG TGPIOMATCHMASK5_31_0 (TGPIO5_MATCH_MASK_31_0) — Offset 4030116Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030116Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.78 REG TGPIOMATCHMASK5_63_32 (TGPIO5_MATCH_MASK_63_32) — Offset 40301170h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301170h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO5_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.79 REG TGPIOCTL6 (TGPIO6_CTL_REG) — Offset 40301180h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301180h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO6_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO6_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO6_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO6_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO6_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO6_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO6_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO6_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO6_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO6_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.80 REG TGPIOCOMPV6_31_0 (TGPIO6_COMPV_31_0) — Offset 40301184h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301184h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO6_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.81 REG TGPIOCOMPV6_63_32 (TGPIO6_COMPV_63_32) — Offset 40301188h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301188h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO6_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.82 REG TGPIOPIV6_31_0 (TGPIO6_PIV_31_0) — Offset 4030118Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030118Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.83 REG TGPIOPIV6_63:32 (TGPIO6_PIV_63_32) — Offset 40301190h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301190h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.84 REG TGPIOTCV6_31_0 (TGPIO6_TCV_31_0) — Offset 40301194h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301194h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.85 REG TGPIOTCV6_63_32 (TGPIO6_TCV_63_32) — Offset 40301198h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301198h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.86 REG TGPIOECCV6_31_0 (TGPIO6_ECCV_31_0) — Offset 4030119Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030119Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.87 REG TGPIOECCV6_63_32 (TGPIO6_ECCV_63_32) — Offset 403011A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.88 REG TGPIOEC6_31_0 (TGPIO6_EC_31_0) — Offset 403011A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403011A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.89 REG TGPIOEC6_63_32 (TGPIO6_EC_63_32) — Offset 403011A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO6_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.90 REG TGPIOMATCHMASK6_31_0 (TGPIO6_MATCH_MASK_31_0) — Offset 403011ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403011ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.91 REG TGPIOMATCHMASK6_63_32 (TGPIO6_MATCH_MASK_63_32) — Offset 403011B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403011B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO6_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.92 REG TGPIOCTL7 (TGPIO7_CTL_REG) — Offset 403011C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	403011C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO7_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO7_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle. .
15:14	0h RW	**Input Event Control (TGPIO7_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO7_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO7_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO7_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO7_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO7_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO7_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO7_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.93 REG TGPIOCOMPV7_31_0 (TGPIO7_COMPV_31_0) — Offset 403011C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403011C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO7_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.94 REG TGPIOCOMPV7_63_32 (TGPIO7_COMPV_63_32) — Offset 403011C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO7_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.95 REG TGPIOPIV7_31_0 (TGPIO7_PIV_31_0) — Offset 403011CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	403011CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.96 REG TGPIOPIV7_63:32 (TGPIO7_PIV_63_32) — Offset 403011D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.97 REG TGPIOTCV7_31_0 (TGPIO7_TCV_31_0) — Offset 403011D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403011D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.98 REG TGPIOTCV7_63_32 (TGPIO7_TCV_63_32) — Offset 403011D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.99 REG TGPIOECCV7_31_0 (TGPIO7_ECCV_31_0) — Offset 403011DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	403011DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.100 REG TGPIOECCV7_63_32 (TGPIO7_ECCV_63_32) — Offset 403011E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.101 REG TGPIOEC7_31_0 (TGPIO7_EC_31_0) — Offset 403011E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403011E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.102 REG TGPIOEC7_63_32 (TGPIO7_EC_63_32) — Offset 403011E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403011E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO7_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.103 REG TGPIOMATCHMASK7_31_0 (TGPIO7_MATCH_MASK_31_0) — Offset 403011ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403011ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.104 REG TGPIOMATCHMASK7_63_32 (TGPIO7_MATCH_MASK_63_32) — Offset 403011F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403011F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO7_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.105 REG TGPIOCTL8 (TGPIO8_CTL_REG) — Offset 40301200h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301200h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO8_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO8_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO8_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO8_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO8_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO8_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO8_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO8_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO8_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO8_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.106 REG TGPIOCOMPV8_31_0 (TGPIO8_COMPV_31_0) — Offset 40301204h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO8_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.107 REG TGPIOCOMPV8_63_32 (TGPIO8_COMPV_63_32) — Offset 40301208h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO8_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.108 REG TGPIOPIV8_31_0 (TGPIO8_PIV_31_0) — Offset 4030120Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030120Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.109 REG TGPIOPIV8_63:32 (TGPIO8_PIV_63_32) — Offset 40301210h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.110 REG TGPIOTCV8_31_0 (TGPIO8_TCV_31_0) — Offset 40301214h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301214h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.111 REG TGPIOTCV8_63_32 (TGPIO8_TCV_63_32) — Offset 40301218h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301218h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.112 REG TGPIOECCV8_31_0 (TGPIO8_ECCV_31_0) — Offset 4030121Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030121Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.113 REG TGPIOECCV8_63_32 (TGPIO8_ECCV_63_32) — Offset 40301220h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.114 REG TGPIOEC8_31_0 (TGPIO8_EC_31_0) — Offset 40301224h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301224h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.115 REG TGPIOEC8_63_32 (TGPIO8_EC_63_32) — Offset 40301228h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO8_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.116 REG TGPIOMATCHMASK8_31_0 (TGPIO8_MATCH_MASK_31_0) — Offset 4030122Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030122Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.117 REG TGPIOMATCHMASK8_63_32 (TGPIO8_MATCH_MASK_63_32) — Offset 40301230h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO8_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.118 REG TGPIOCTL9 (TGPIO9_CTL_REG) — Offset 40301240h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301240h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO9_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO9_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO9_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO9_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO9_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO9_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO9_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO9_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO9_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO9_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.119 REG TGPIOCOMPV9_31_0 (TGPIO9_COMPV_31_0) — Offset 40301244h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301244h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO9_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.120 REG TGPIOCOMPV9_63_32 (TGPIO9_COMPV_63_32) — Offset 40301248h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301248h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO9_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.121 REG TGPIOPIV9_31_0 (TGPIO9_PIV_31_0) — Offset 4030124Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030124Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.122 REG TGPIOPIV9_63:32 (TGPIO9_PIV_63_32) — Offset 40301250h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301250h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.123 REG TGPIOTCV9_31_0 (TGPIO9_TCV_31_0) — Offset 40301254h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301254h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.124 REG TGPIOTCV9_63_32 (TGPIO9_TCV_63_32) — Offset 40301258h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301258h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.125 REG TGPIOECCV9_31_0 (TGPIO9_ECCV_31_0) — Offset 4030125Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030125Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.126 REG TGPIOECCV9_63_32 (TGPIO9_ECCV_63_32) — Offset 40301260h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301260h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.127 REG TGPIOEC9_31_0 (TGPIO9_EC_31_0) — Offset 40301264h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301264h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.128 REG TGPIOEC9_63_32 (TGPIO9_EC_63_32) — Offset 40301268h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301268h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO9_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.129 REG TGPIOMATCHMASK9_31_0 (TGPIO9_MATCH_MASK_31_0) — Offset 4030126Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030126Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.130 REG TGPIOMATCHMASK9_63_32 (TGPIO9_MATCH_MASK_63_32) — Offset 40301270h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301270h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO9_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.131 REG TGPIOCTL10 (TGPIO10_CTL_REG) — Offset 40301280h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301280h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO10_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO10_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO10_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO10_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO10_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO10_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO10_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO10_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO10_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO10_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.132 REG TGPIOCOMPV10_31_0 (TGPIO10_COMPV_31_0) — Offset 40301284h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301284h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO10_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.133 REG TGPIOCOMPV10_63_32 (TGPIO10_COMPV_63_32) — Offset 40301288h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301288h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO10_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.134 REG TGPIOPIV10_31_0 (TGPIO10_PIV_31_0) — Offset 4030128Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030128Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.135 REG TGPIOPIV10_63:32 (TGPIO10_PIV_63_32) — Offset 40301290h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301290h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.136 REG TGPIOTCV10_31_0 (TGPIO10_TCV_31_0) — Offset 40301294h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301294h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.137 REG TGPIOTCV10_63_32 (TGPIO10_TCV_63_32) — Offset 40301298h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301298h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.138 REG TGPIOECCV10_31_0 (TGPIO10_ECCV_31_0) — Offset 4030129Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030129Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.139 REG TGPIOECCV10_63_32 (TGPIO10_ECCV_63_32) — Offset 403012A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.140 REG TGPIOEC10_31_0 (TGPIO10_EC_31_0) — Offset 403012A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403012A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.141 REG TGPIOEC10_63_32 (TGPIO10_EC_63_32) — Offset 403012A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO10_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.142 REG TGPIOMATCHMASK10_31_0 (TGPIO10_MATCH_MASK_31_0) — Offset 403012ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403012ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.143 REG TGPIOMATCHMASK10_63_32 (TGPIO10_MATCH_MASK_63_32) — Offset 403012B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403012B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO10_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.144 REG TGPIOCTL11 (TGPIO11_CTL_REG) — Offset 403012C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	403012C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO11_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO11_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO11_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO11_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO11_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO11_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO11_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO11_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO11_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO11_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.145 REG TGPIOCOMPV11_31_0 (TGPIO11_COMPV_31_0) — Offset 403012C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403012C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO11_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.146 REG TGPIOCOMPV11_63_32 (TGPIO11_COMPV_63_32) — Offset 403012C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO11_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.147 REG TGPIOPIV11_31_0 (TGPIO11_PIV_31_0) — Offset 403012CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	403012CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.148 REG TGPIOPIV11_63:32 (TGPIO11_PIV_63_32) — Offset 403012D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.149 REG TGPIOTCV11_31_0 (TGPIO11_TCV_31_0) — Offset 403012D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403012D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.150 REG TGPIOTCV11_63_32 (TGPIO11_TCV_63_32) — Offset 403012D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.151 REG TGPIOECCV11_31_0 (TGPIO11_ECCV_31_0) — Offset 403012DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	403012DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.152 REG TGPIOECCV11_63_32 (TGPIO11_ECCV_63_32) — Offset 403012E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.153 REG TGPIOEC11_31_0 (TGPIO11_EC_31_0) — Offset 403012E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403012E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.154 REG TGPIOEC11_63_32 (TGPIO11_EC_63_32) — Offset 403012E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403012E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO11_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.155 REG TGPIOMATCHMASK11_31_0 (TGPIO11_MATCH_MASK_31_0) — Offset 403012ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403012ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.156 REG TGPIOMATCHMASK11_63_32 (TGPIO11_MATCH_MASK_63_32) — Offset 403012F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403012F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO11_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.157 REG TGPIOCTL12 (TGPIO12_CTL_REG) — Offset 40301300h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301300h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO12_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO12_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO12_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO12_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO12_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO12_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO12_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO12_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO12_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO12_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.158 REG TGPIOCOMPV12_31_0 (TGPIO12_COMPV_31_0) — Offset 40301304h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301304h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO12_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.159 REG TGPIOCOMPV12_63_32 (TGPIO12_COMPV_63_32) — Offset 40301308h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301308h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO12_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.160 REG TGPIOPIV12_31_0 (TGPIO12_PIV_31_0) — Offset 4030130Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030130Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.161 REG TGPIOPIV12_63:32 (TGPIO12_PIV_63_32) — Offset 40301310h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301310h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.162 REG TGPIOTCV12_31_0 (TGPIO12_TCV_31_0) — Offset 40301314h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301314h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.163 REG TGPIOTCV12_63_32 (TGPIO12_TCV_63_32) — Offset 40301318h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301318h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.164 REG TGPIOECCV12_31_0 (TGPIO12_ECCV_31_0) — Offset 4030131Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030131Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.165 REG TGPIOECCV12_63_32 (TGPIO12_ECCV_63_32) — Offset 40301320h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301320h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.166 REG TGPIOEC12_31_0 (TGPIO12_EC_31_0) — Offset 40301324h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301324h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.167 REG TGPIOEC12_63_32 (TGPIO12_EC_63_32) — Offset 40301328h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301328h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO12_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.168 REG TGPIOMATCHMASK12_31_0 (TGPIO12_MATCH_MASK_31_0) — Offset 4030132Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030132Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.169 REG TGPIOMATCHMASK12_63_32 (TGPIO12_MATCH_MASK_63_32) — Offset 40301330h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301330h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO12_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.170 REG TGPIOCTL13 (TGPIO13_CTL_REG) — Offset 40301340h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301340h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO13_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO13_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO13_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO13_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO13_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO13_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO13_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO13_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO13_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO13_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.171 REG TGPIOCOMPV13_31_0 (TGPIO13_COMPV_31_0) — Offset 40301344h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301344h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO13_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.172 REG TGPIOCOMPV13_63_32 (TGPIO13_COMPV_63_32) — Offset 40301348h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301348h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO13_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.173 REG TGPIOPIV13_31_0 (TGPIO13_PIV_31_0) — Offset 4030134Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030134Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.174 REG TGPIOPIV13_63:32 (TGPIO13_PIV_63_32) — Offset 40301350h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301350h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.175 REG TGPIOTCV13_31_0 (TGPIO13_TCV_31_0) — Offset 40301354h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301354h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.176 REG TGPIOTCV13_63_32 (TGPIO13_TCV_63_32) — Offset 40301358h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301358h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.177 REG TGPIOECCV13_31_0 (TGPIO13_ECCV_31_0) — Offset 4030135Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030135Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.178 REG TGPIOECCV13_63_32 (TGPIO13_ECCV_63_32) — Offset 40301360h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301360h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.179 REG TGPIOEC13_31_0 (TGPIO13_EC_31_0) — Offset 40301364h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301364h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.180 REG TGPIOEC13_63_32 (TGPIO13_EC_63_32) — Offset 40301368h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301368h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO13_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.181 REG TGPIOMATCHMASK13_31_0 (TGPIO13_MATCH_MASK_31_0) — Offset 4030136Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030136Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.182 REG TGPIOMATCHMASK13_63_32 (TGPIO13_MATCH_MASK_63_32) — Offset 40301370h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301370h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO13_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.183 REG TGPIOCTL14 (TGPIO14_CTL_REG) — Offset 40301380h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301380h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO14_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO14_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO14_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO14_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO14_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO14_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO14_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO14_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO14_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO14_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.184 REG TGPIOCOMPV14_31_0 (TGPIO14_COMPV_31_0) — Offset 40301384h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301384h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO14_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.185 REG TGPIOCOMPV14_63_32 (TGPIO14_COMPV_63_32) — Offset 40301388h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301388h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO14_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.186 REG TGPIOPIV14_31_0 (TGPIO14_PIV_31_0) — Offset 4030138Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030138Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.187 REG TGPIOPIV14_63:32 (TGPIO14_PIV_63_32) — Offset 40301390h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301390h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.188 REG TGPIOTCV14_31_0 (TGPIO14_TCV_31_0) — Offset 40301394h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301394h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.189 REG TGPIOTCV14_63_32 (TGPIO14_TCV_63_32) — Offset 40301398h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301398h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.190 REG TGPIOECCV14_31_0 (TGPIO14_ECCV_31_0) — Offset 4030139Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030139Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.191 REG TGPIOECCV14_63_32 (TGPIO14_ECCV_63_32) — Offset 403013A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.192 REG TGPIOEC14_31_0 (TGPIO14_EC_31_0) — Offset 403013A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403013A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.193 REG TGPIOEC14_63_32 (TGPIO14_EC_63_32) — Offset 403013A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO14_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.194 REG TGPIOMATCHMASK14_31_0 (TGPIO14_MATCH_MASK_31_0) — Offset 403013ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403013ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.195 REG TGPIOMATCHMASK14_63_32 (TGPIO14_MATCH_MASK_63_32) — Offset 403013B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403013B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO14_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.196 REG TGPIOCTL15 (TGPIO15_CTL_REG) — Offset 403013C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	403013C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO15_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO15_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO15_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO15_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO15_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO15_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO15_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO15_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO15_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO15_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.197 REG TGPIOCOMPV15_31_0 (TGPIO15_COMPV_31_0) — Offset 403013C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403013C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO15_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.198 REG TGPIOCOMPV15_63_32 (TGPIO15_COMPV_63_32) — Offset 403013C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO15_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.199 REG TGPIOPIV15_31_0 (TGPIO15_PIV_31_0) — Offset 403013CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	403013CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.200 REG TGPIOPIV15_63:32 (TGPIO15_PIV_63_32) — Offset 403013D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.201 REG TGPIOTCV15_31_0 (TGPIO15_TCV_31_0) — Offset 403013D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403013D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.202 REG TGPIOTCV15_63_32 (TGPIO15_TCV_63_32) — Offset 403013D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.203 REG TGPIOECCV15_31_0 (TGPIO15_ECCV_31_0) — Offset 403013DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	403013DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.204 REG TGPIOECCV15_63_32 (TGPIO15_ECCV_63_32) — Offset 403013E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.205 REG TGPIOEC15_31_0 (TGPIO15_EC_31_0) — Offset 403013E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403013E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.206 REG TGPIOEC15_63_32 (TGPIO15_EC_63_32) — Offset 403013E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403013E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO15_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.207 REG TGPIOMATCHMASK15_31_0 (TGPIO15_MATCH_MASK_31_0) — Offset 403013ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403013ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.208 REG TGPIOMATCHMASK15_63_32 (TGPIO15_MATCH_MASK_63_32) — Offset 403013F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403013F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO15_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.209 REG TGPIOCTL16 (TGPIO16_CTL_REG) — Offset 40301400h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301400h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO16_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO16_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO16_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO16_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO16_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO16_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO16_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO16_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO16_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO16_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.210 REG TGPIOCOMPV16_31_0 (TGPIO16_COMPV_31_0) — Offset 40301404h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO16_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.211 REG TGPIOCOMPV16_63_32 (TGPIO16_COMPV_63_32) — Offset 40301408h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301408h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO16_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.212 REG TGPIOPIV16_31_0 (TGPIO16_PIV_31_0) — Offset 4030140Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030140Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.213 REG TGPIOPIV16_63:32 (TGPIO16_PIV_63_32) — Offset 40301410h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301410h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.214 REG TGPIOTCV16_31_0 (TGPIO16_TCV_31_0) — Offset 40301414h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.215 REG TGPIOTCV16_63_32 (TGPIO16_TCV_63_32) — Offset 40301418h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301418h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.216 REG TGPIOECCV16_31_0 (TGPIO16_ECCV_31_0) — Offset 4030141Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030141Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.217 REG TGPIOECCV16_63_32 (TGPIO16_ECCV_63_32) — Offset 40301420h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301420h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.218 REG TGPIOEC16_31_0 (TGPIO16_EC_31_0) — Offset 40301424h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301424h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.219 REG TGPIOEC16_63_32 (TGPIO16_EC_63_32) — Offset 40301428h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301428h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO16_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.220 REG TGPIOMATCHMASK16_31_0 (TGPIO16_MATCH_MASK_31_0) — Offset 4030142Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030142Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.221 REG TGPIOMATCHMASK16_63_32 (TGPIO16_MATCH_MASK_63_32) — Offset 40301430h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301430h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO16_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.222 REG TGPIOCTL17 (TGPIO17_CTL_REG) — Offset 40301440h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301440h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO17_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO17_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO17_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO17_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO17_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO17_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO17_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO17_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO17_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO17_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.223 REG TGPIOCOMPV17_31_0 (TGPIO17_COMPV_31_0) — Offset 40301444h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301444h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO17_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.224 REG TGPIOCOMPV17_63_32 (TGPIO17_COMPV_63_32) — Offset 40301448h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301448h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO17_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.225 REG TGPIOPIV17_31_0 (TGPIO17_PIV_31_0) — Offset 4030144Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030144Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.226 REG TGPIOPIV17_63:32 (TGPIO17_PIV_63_32) — Offset 40301450h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301450h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.227 REG TGPIOTCV17_31_0 (TGPIO17_TCV_31_0) — Offset 40301454h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301454h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.228 REG TGPIOTCV17_63_32 (TGPIO17_TCV_63_32) — Offset 40301458h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301458h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.229 REG TGPIOECCV17_31_0 (TGPIO17_ECCV_31_0) — Offset 4030145Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030145Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.230 REG TGPIOECCV17_63_32 (TGPIO17_ECCV_63_32) — Offset 40301460h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301460h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.231 REG TGPIOEC17_31_0 (TGPIO17_EC_31_0) — Offset 40301464h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301464h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.232 REG TGPIOEC17_63_32 (TGPIO17_EC_63_32) — Offset 40301468h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301468h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO17_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.233 REG TGPIOMATCHMASK17_31_0 (TGPIO17_MATCH_MASK_31_0) — Offset 4030146Ch

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030146Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.234 REG TGPIOMATCHMASK17_63_32 (TGPIO17_MATCH_MASK_63_32) — Offset 40301470h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301470h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO17_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.235 REG TGPIOCTL18 (TGPIO18_CTL_REG) — Offset 40301480h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	40301480h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO18_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO18_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO18_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO18_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO18_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO18_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO18_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO18_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO18_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO18_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.236 REG TGPIOCOMPV18_31_0 (TGPIO18_COMPV_31_0) — Offset 40301484h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301484h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO18_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.237 REG TGPIOCOMPV18_63_32 (TGPIO18_COMPV_63_32) — Offset 40301488h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301488h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO18_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.238 REG TGPIOPIV18_31_0 (TGPIO18_PIV_31_0) — Offset 4030148Ch

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030148Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.239 REG TGPIOPIV18_63:32 (TGPIO18_PIV_63_32) — Offset 40301490h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301490h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.240 REG TGPIOTCV18_31_0 (TGPIO18_TCV_31_0) — Offset 40301494h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	40301494h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.241 REG TGPIOTCV18_63_32 (TGPIO18_TCV_63_32) — Offset 40301498h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	40301498h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.242 REG TGPIOECCV18_31_0 (TGPIO18_ECCV_31_0) — Offset 4030149Ch

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	4030149Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.243 REG TGPIOECCV18_63_32 (TGPIO18_ECCV_63_32) — Offset 403014A0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.244 REG TGPIOEC18_31_0 (TGPIO18_EC_31_0) — Offset 403014A4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403014A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.245 REG TGPIOEC18_63_32 (TGPIO18_EC_63_32) — Offset 403014A8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO18_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.246 REG TGPIOMATCHMASK18_31_0 (TGPIO18_MATCH_MASK_31_0) — Offset 403014ACh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403014ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.247 REG TGPIOMATCHMASK18_63_32 (TGPIO18_MATCH_MASK_63_32) — Offset 403014B0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403014B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO18_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.248 REG TGPIOCTL19 (TGPIO19_CTL_REG) — Offset 403014C0h

TGPIO control register.

Type	Size	Offset	Default
MMIO	32 bit	403014C0h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24:17	00h RW	**Periodic Sequence Length (TGPIO19_CTL_PRDC_SEQ_LEN_O):** 8'b0 = continues infinitely, Any other value defines the length of sequence.
16	0h RW	**EC Counter (TGPIO19_CTL_EC_CTR_O):** Applicable only when the GPIO is configured as an output. 1 b0 EC not used 1 b1 EC increments from whatever initial value was programmed every clock cycle.
15:14	0h RW	**Input Event Control (TGPIO19_CTL_IN_EVNT_CTL_O):** This is applicable only when the GPIO is configured as an Input. 2 b00 An input transition will cause the EC to increment, Time Stamp to be captured in TCV and interrupt to be signaled if enabled. 2 b01 An input transition causes the EC to be incremented only. The EC value could be fed back by connecting the Output Event Counter to the Input Event counter pins. An interrupt could be signaled when a match occurs with the programmed value in the COMPV. 2 b10 - reserved 2 b11 reserved.
13	1h RW	**Freeze Input Timestamp (TGPIO19_FREEZE_IN_TS_O):** When set the an input time stamp is captured and not cleared until the corresponding raw interrupt status bit is cleared.
12:10	0h RO	**Reserved**
9	0h RW	**Input Counter Select (TGPIO19_CTL_IN_CTR_SEL_O):** 0 Select Input Time Stamp Counter 1 Select Input Event Counter.

Bit Range	Default & Access	Field Name (ID): Description
8:5	0h RW	**Pulse Width Stretch (TGPIO19_CTL_PW_STRETCH_O):** Default - 2 clk cycles Range - 2 to 17 clk cycles.
4	0h RW	**Periodic Mode (PM) (TGPIO19_CTL_PM_O):** 0 Periodic mode is disabled 1 Periodic mode is enabled.
3:2	0h RW	**Event Polarity (EP) (TGPIO19_CTL_EP_O):** 00 Rising edge 01 Falling edge 10 Toggle edge 11 Reserved.
1	0h RW	**Direction (DIR) (TGPIO19_CTL_DIR_O):** 0 Output 1 Input.
0	0h RW	**Enable (EN) (TGPIO19_CTL_EN_O):** 0 Timed GPIO is disabled 1 Timed GPIO is enabled.

14.3.2.249 REG TGPIOCOMPV19_31_0 (TGPIO19_COMPV_31_0) — Offset 403014C4h

Comparator Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403014C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO19_COMPV_REG_31_0:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.250 REG TGPIOCOMPV19_63_32 (TGPIO19_COMPV_63_32) — Offset 403014C8h

Comparator Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO19_COMPV_REG_63_32:** If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. .

14.3.2.251 REG TGPIOPIV19_31_0 (TGPIO19_PIV_31_0) — Offset 403014CCh

Periodic Interval value 0.

Type	Size	Offset	Default
MMIO	32 bit	403014CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_PIV_REG_31_0:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.252 REG TGPIOPIV19_63:32 (TGPIO19_PIV_63_32) — Offset 403014D0h

Periodic Interval value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_PIV_REG_63_32:** The value in this register is written by SW to set the interval for the periodic Timed GPIO event.

14.3.2.253 REG TGPIOTCV19_31_0 (TGPIO19_TCV_31_0) — Offset 403014D4h

Timestamp Capture Value 0.

Type	Size	Offset	Default
MMIO	32 bit	403014D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_TCV_REG_31_0:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.254 REG TGPIOTCV19_63_32 (TGPIO19_TCV_63_32) — Offset 403014D8h

Timestamp Capture Value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_TCV_REG_63_32:** When Timed GPIO event triggers, HW captures the current ART time into this register.

14.3.2.255 REG TGPIOECCV19_31_0 (TGPIO19_ECCV_31_0) — Offset 403014DCh

Event Counter capture value 0.

Type	Size	Offset	Default
MMIO	32 bit	403014DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_ECCV_REG_31_0:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.256 REG TGPIOECCV19_63_32 (TGPIO19_ECCV_63_32) — Offset 403014E0h

Event Counter capture value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_ECCV_REG_63_32:** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register.

14.3.2.257 REG TGPIOEC19_31_0 (TGPIO19_EC_31_0) — Offset 403014E4h

Event counter value 0.

Type	Size	Offset	Default
MMIO	32 bit	403014E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_EC_REG_31_0:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.258 REG TGPIOEC19_63_32 (TGPIO19_EC_63_32) — Offset 403014E8h

Event counter value 1.

Type	Size	Offset	Default
MMIO	32 bit	403014E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TGPIO19_EC_REG_63_32:** When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated.

14.3.2.259 REG TGPIOMATCHMASK19_31_0 (TGPIO19_MATCH_MASK_31_0) — Offset 403014ECh

Comparator mask register 0.

Type	Size	Offset	Default
MMIO	32 bit	403014ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_MATCH_MSK_REG_31_0:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.260 REG TGPIOMATCHMASK19_63_32 (TGPIO19_MATCH_MASK_63_32) — Offset 403014F0h

Comparator mask register 1.

Type	Size	Offset	Default
MMIO	32 bit	403014F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TGPIO19_MATCH_MSK_REG_63_32:** When a bit in this register is set then the corresponding match function between the corresponding COMPV and input Timer Value are ignored and a match is forced.

14.3.2.261 REG TGPIOINTRCTL (TGPIO_INTR_CTL_REG) — Offset 40301500h

Interrupt control register.

Type	Size	Offset	Default
MMIO	32 bit	40301500h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Disable Interrupt Coalescing (TGPIO_INTR_COALESCE_DISABLE):** When set will prevent coalescing of interrupts. The default is to enable interrupt coalescing.

14.3.2.262 REG TGPIORIS (TGPIO_INTR_RIS_REG) — Offset 40301504h

Raw interrupt status register.

Type	Size	Offset	Default
MMIO	32 bit	40301504h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_GLOBAL:** Set when the TMT GLOBAL nanosecond counter wraps which is about every 1s.
24	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_WORKING:** Set when the TMT WORKING nanosecond counter wraps which is about every 1s.
23	0h RO	**TGPIO_RIS_TMT_NESC_WRAP_TSG:** Set when the TMT TSG nanosecond counter wraps which is about every 1s.
22	0h RO	**Time Adjust Complete TADJ_TMT_GLOBAL_CMPLT (TGPIO_RIS_TADJ_TMT_GLOBAL_CMPLT):** 0-No Interrupt 1-Interrupt.
21	0h RO	**Time Adjust Complete TADJ_TMT_WORKING_CMPLT (TGPIO_RIS_TADJ_TMT_WORKING_CMPLT):** 0-No Interrupt 1-Interrupt.
20	0h RO	**Time Adjust Complete TADJ_TMT_TSG_CMPLT (TGPIO_RIS_TADJ_TMT_TSG_CMPLT):** 0-No Interrupt 1-Interrupt.
19:0	00000h RO	**Event Interrupt (TGPIO_RIS_EVENT_INTR):** 0-No Interrupt 1-Interrupt Pending.

14.3.2.263 REG TGPIOMSC (TGPIO_INTR_MSC_REG) — Offset 40301508h

Interrupt mask control register.

Type	Size	Offset	Default
MMIO	32 bit	40301508h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_GLOBAL_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
24	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_WORKING_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
23	0h RW	**TGPIO_MSC_TMT_NESC_WRAP_TSG_EN:** 0-Interrupt Disabled 1-Interrupt Enabled.
22	0h RW	**Time Adjust Complete Enable TADJ_TMT_GLOBAL_EN (TGPIO_MSC_TADJ_TMT_GLOBAL_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
21	0h RW	**Time Adjust Complete Enable TADJ_TMT_WORKING_EN (TGPIO_MSC_TADJ_TMT_WORKING_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
20	0h RW	**Time Adjust Complete Enable TADJ_TMT_TSG_EN (TGPIO_MSC_TADJ_TMT_TSG_EN):** 0-Interrupt Disabled 1-Interrupt Enabled.
19:0	00000h RW	**Event Interrupt (TGPIO_MSC_EVENT_INTR):** 0-Interrupt Disabled 1-Interrupt Enabled.

14.3.2.264 REG TGPIOMIS (TGPIO_INTR_MIS_REG) — Offset 4030150Ch

Masked interrupt status register.

Type	Size	Offset	Default
MMIO	32 bit	4030150Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_GLOBAL:** 0- No Interrupt 1-Interrupt.
24	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_WORKING:** 0- No Interrupt 1-Interrupt.
23	0h RO	**TGPIO_MIS_TMT_NESC_WRAP_TSG:** 0- No Interrupt 1-Interrupt.
22	0h RO	**Time Adjust Complete TADJ_TMT_GLOBAL_CMPLT (TGPIO_MIS_TADJ_TMT_GLOBAL):** 0- No Interrupt 1-Interrupt.
21	0h RO	**Time Adjust Complete TADJ_TMT_WORKING_CMPLT (TGPIO_MIS_TADJ_TMT_WORKING):** 0- No Interrupt 1-Interrupt.
20	0h RO	**Time Adjust Complete TADJ_TMT_TSG_CMPLT (TGPIO_MIS_TADJ_TMT_TSG):** 0- No Interrupt 1-Interrupt.
19:0	00000h RO	**Event Interrupt (TGPIO_MIS_EVENT_INTR):** 1-No Interrupt 2-Interrupt Pending.

14.3.2.265 REG TGPIOICR (TGPIO_INTR_ICR_REG) — Offset 40301510h

Interrupt clear register.

Type	Size	Offset	Default
MMIO	32 bit	40301510h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_GLOBAL:** 0 No change 1-Clear Interrupt Request.
24	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_WORKING:** 0 No change 1-Clear Interrupt Request.
23	0h WO	**TGPIO_ICR_TMT_NESC_WRAP_TSG:** 0 No change 1-Clear Interrupt Request.
22	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_GLOBAL_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_GLOBAL):** 0 No change 1-Clear Interrupt Request.
21	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_WORKING_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_WORKING):** 0 No change 1-Clear Interrupt Request.
20	0h WO	**Clear Time Adjust Complete CLR_TADJ_TMT_TSG_CMPLT (TGPIO_ICR_CLR_TADJ_TMT_TSG):** 0 No change 1-Clear Interrupt Request.
19:0	00000h WO	**Clear Event Interrupt [19:0] (TGPIO_ICR_CLR_EVENT_INTR):** 0 No change 1-Clear Interrupt Request.

14.3.2.266 REG TGPIO_CLK_SEL_REG (TGPIO_CLK_SEL_REG) — Offset 40301514h

Timed GPIO clock select register.

Type	Size	Offset	Default
MMIO	32 bit	40301514h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:0	00000h RW	**Clock Select (TGPIO_CLK_SEL_REG):** Timed GPIO clock select register.

14.3.2.267 REG TGPIO_CLK_SEL_REG (TGPIO_XTAL_CG_REG) — Offset 40301518h

Timed GPIO XTAL Clock Gate enable registe.

Type	Size	Offset	Default
MMIO	32 bit	40301518h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TGPIO_XTL_CG_REG:** This clock needs to be gated before writing to the clk_sel register.

14.3.2.268 Reg TGPIO_PTP_CG_REG (TGPIO_PTP_CG_REG) — Offset 4030151Ch

Timed GPIO PTP Clock Gate enable register.

Type	Size	Offset	Default
MMIO	32 bit	4030151Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TGPIO_PPT_CG_REG:** This clock needs to be gated before writing to the clk_sel register.

14.3.2.269 REG TGPIO_TS_SEL_0_REG (TGPIO_TS_SEL_0_REG) — Offset 40301520h

TGPIO input timestamp select register 0.

Type	Size	Offset	Default
MMIO	32 bit	40301520h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Select 0 (TGPIO_TS_SEL_0_REG):** TGPIO input timestamp select register 0.

14.3.2.270 REG TGPIO_TS_SEL_1_REG (TGPIO_TS_SEL_1_REG) — Offset 40301524h

TGPIO input timestamp select register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301524h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Timestamp Select 1 (TGPIO_TS_SEL_1_REG):** TGPIO input timestamp select register 1.

14.3.2.271 REG TMT_CLK_SEL_REG (TGPIO_TMT_CLK_SEL_REG) — Offset 40301528h

TMT clock select register.

Type	Size	Offset	Default
MMIO	32 bit	40301528h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**TMT Clock Select (TGPIO_TMT_CLK_SEL_REG):** TMT clock select register.

14.3.2.272 REG TGPIO_TSC_CTL_REG (TGPIO_CTS_ENABLE_REG) — Offset 40301530h

TGPIO cross timestamp control register.

Type	Size	Offset	Default
MMIO	32 bit	40301530h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW	**TMT CTS En 2 (TMT_CTS_ENABLE_REG_2):** TMT Cross Time Stamp Control [2].
3:2	0h RW	**TMT CTS En 1 (TMT_CTS_ENABLE_REG_1):** TMT Cross Time Stamp Control [1].
1:0	0h RW	**TMT CTS En 0 (TMT_CTS_ENABLE_REG_0):** TMT Cross Time Stamp Control [0].

14.3.2.273 REG TGPIO_TSC_STATUS_REG (TGPIO_CTS_VALID_REG) — Offset 40301534h

TGPIO cross timestamp status register.

Type	Size	Offset	Default
MMIO	32 bit	40301534h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RO	**TMT CTS STATUS 2 (TMT_CTS_VALID_REG_2):** TMT Cross Time Stamp Status [2].
3:2	0h RO	**TMT CTS STATUS 1 (TMT_CTS_VALID_REG_1):** TMT Cross Time Stamp Status [1].
1:0	0h RO	**TMT CTS STATUS 0 (TMT_CTS_VALID_REG_0):** TMT Cross Time Stamp Status [0].

14.3.2.274 REG TMTCTL_TSG (TMT_CTL_TSG_REG) — Offset 40301600h

TMT control register.

Type	Size	Offset	Default
MMIO	32 bit	40301600h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_TSG_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

14.3.2.275 REG TMTR_TSG (TMTR_TSG_REG) — Offset 40301604h

TMT timestamp residue register.

Type	Size	Offset	Default
MMIO	32 bit	40301604h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_TSG_REG:** TMT residue value defined with a resolution of 2^-32ns.

14.3.2.276 REG TMTL_TSG (TMTL_TSG_REG) — Offset 40301608h

TMT timestamp low register.

Type	Size	Offset	Default
MMIO	32 bit	40301608h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_TSG_REG:** Lower Half of the TMT defined in ns..

14.3.2.277 REG TMTH_TSG (TMTH_TSG_REG) — Offset 4030160Ch

TMT timestamp high register.

Type	Size	Offset	Default
MMIO	32 bit	4030160Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_TSG_REG:** Upper Half of the TMT defined in ns.

14.3.2.278 REG TIMINCA_TSG (TMT_TIMINCA_TSG_REG) — Offset 40301610h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	40301610h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_TSG_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_TSG_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

14.3.2.279 REG TIMADJ_TSG (TMT_TIMADJ_TSG_REG) — Offset 40301614h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	40301614h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_TSG_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_TSG_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_TSG_TIMADJ_TADJUS:** Time Adjust Value.

14.3.2.280 REG LXTS_TMT_HIGH_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_1) — Offset 40301618h

TMT local cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301618h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_TSG_REG:** TMTH captured when a local cross time stamp capture is enabled.

14.3.2.281 REG LXTS_TMT_LOW_TSG (TMT_LXTS_SNAPSHOT_TSG_REG_0) — Offset 4030161Ch

TMT local cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030161Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_TSG_REG:** TMTL captured when a local cross time stamp capture is enabled.

14.3.2.282 REG LXTS_ART_HIGH_TSG (TMT_ART_SNAPSHOT_TSG_REG_1) — Offset 40301620h

TMT local cross timestamp ART snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301620h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_TSG_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

14.3.2.283 REG LXTS_ART_LOW_TSG (TMT_ART_SNAPSHOT_TSG_REG_0) — Offset 40301624h

TMT local cross timestamp ART snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40301624h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_TSG_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

14.3.2.284 REG RXTS_TMT_HIGH_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_1) — Offset 40301628h

TMT remote cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301628h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_TSG_REG:** TMTH captured when a remote time stamp capture is enabled.

14.3.2.285 REG RXTS_TMT_LOW_TSG (TMT_RXTS_SNAPSHOT_TSG_REG_0) — Offset 4030162Ch

TMT remote cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	4030162Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_TSG_REG:** TMTL captured when a remote time stamp capture is enabled.

14.3.2.286 REG TMTCTL_GLOBAL (TMT_CTL_GLOBAL_REG) — Offset 40301640h

TMT control register.

Type	Size	Offset	Default
MMIO	32 bit	40301640h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_GLOBAL_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

14.3.2.287 REG TMTR_GLOBAL (TMTR_GLOBAL_REG) — Offset 40301644h

TMT timestamp residue register.

Type	Size	Offset	Default
MMIO	32 bit	40301644h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_GLOBAL_REG:** TMT residue value defined with a resolution of 2^-32ns.

14.3.2.288 REG TMTL_GLOBAL (TMTL_GLOBAL_REG) — Offset 40301648h

TMT timestamp low register.

Type	Size	Offset	Default
MMIO	32 bit	40301648h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_GLOBAL_REG:** Lower Half of the TMT defined in ns..

14.3.2.289 REG TMTH_GLOBAL (TMTH_GLOBAL_REG) — Offset 4030164Ch

TMT timestamp high register.

Type	Size	Offset	Default
MMIO	32 bit	4030164Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_GLOBAL_REG:** Upper Half of the TMT defined in ns.

14.3.2.290 REG TIMINCA_GLOBAL (TMT_TIMINCA_GLOBAL_REG) — Offset 40301650h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	40301650h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_GLOBAL_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_GLOBAL_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

14.3.2.291 REG TIMADJ_GLOBAL (TMT_TIMADJ_GLOBAL_REG) — Offset 40301654h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	40301654h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_GLOBAL_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_GLOBAL_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_GLOBAL_TIMADJ_TADJUS:** Time Adjust Value.

14.3.2.292 REG LXTS_TMT_LOW_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_0) — Offset 40301658h

TMT local cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40301658h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_GLOBAL_REG:** TMTL captured when a local cross time stamp capture is enabled.

14.3.2.293 REG LXTS_TMT_HIGH_GLOBAL (TMT_LXTS_SNAPSHOT_GLOBAL_REG_1) — Offset 4030165Ch

TMT local cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	4030165Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_GLOBAL_REG:** TMTH captured when a local cross time stamp capture is enabled.

14.3.2.294 REG LXTS_ART_LOW_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_0) — Offset 40301660h

TMT local cross timestamp ART snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40301660h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_GLOBAL_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

14.3.2.295 REG LXTS_ART_HIGH_GLOBAL (TMT_ART_SNAPSHOT_GLOBAL_REG_1) — Offset 40301664h

TMT local cross timestamp ART snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	40301664h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_GLOBAL_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

14.3.2.296 REG RXTS_TMT_LOW_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_0) — Offset 40301668h

TMT remote cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40301668h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_GLOBAL_REG:** TMTL captured when a remote time stamp capture is enabled.

14.3.2.297 REG RXTS_TMT_HIGH_GLOBAL (TMT_RXTS_SNAPSHOT_GLOBAL_REG_1) — Offset 4030166Ch

TMT remote cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	4030166Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_GLOBAL_REG:** TMTH captured when a remote time stamp capture is enabled.

14.3.2.298 REG TMTCTL_WORKING (TMT_CTL_WORKING_REG) — Offset 40301680h

TMT control register.

Type	Size	Offset	Default
MMIO	32 bit	40301680h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TMT ENABLE (TGPIO_TMT_CTRL_WORKING_REG):** Enables incrementing TMT when set Should be cleared before initializing TMT.

14.3.2.299 REG TMTR_WORKING (TMTR_WORKING_REG) — Offset 40301684h

TMT timestamp residue register.

Type	Size	Offset	Default
MMIO	32 bit	40301684h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTR_WORKING_REG:** TMT residue value defined with a resolution of 2^-32ns.

14.3.2.300 REG TMTL_WORKING (TMTL_WORKING_REG) — Offset 40301688h

TMT timestamp low register.

Type	Size	Offset	Default
MMIO	32 bit	40301688h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:0	00000000h RW/V	**TGPIO_TMT_TMTL_WORKING_REG:** Lower Half of the TMT defined in ns..

14.3.2.301 REG TMTH_WORKING (TMTH_WORKING_REG) — Offset 4030168Ch

TMT timestamp high register.

Type	Size	Offset	Default
MMIO	32 bit	4030168Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TGPIO_TMT_TMTH_WORKING_REG:** Upper Half of the TMT defined in ns.

14.3.2.302 REG TIMINCA_WORKING (TMT_TIMINCA_WORKING_REG) — Offset 40301690h

TMT Time Increment Adjust Register.

Type	Size	Offset	Default
MMIO	32 bit	40301690h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_WORKING_TIMINCA_ISIGN:** Increment Sign 0 Each 5ns cycle add to the TMT Timer a value of 5ns + Incvalue*2^-32ns 1 Each 5ns cycle add to the TMT Timer a value of 5ns IncValue*2^-32ns.
30:0	00000000h RW	**TGPIO_TMT_WORKING_TIMINCA_INC_VALUE:** Increment Value to be added or subtracted from 5ns clock cycle.

14.3.2.303 REG TIMADJ_WORKING (TMT_TIMADJ_WORKING_REG) — Offset 40301694h

TMT Time Offset Adjust register.

Type	Size	Offset	Default
MMIO	32 bit	40301694h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TGPIO_TMT_WORKING_TIMADJ_SIGN:** 0 = positive 1 = Negative.
30	0h RW	**Zero Bit (TGPIO_TMT_WORKING_TIMADJ_ZERO_BIT):** Zero bit.
29:0	00000000h RW	**TGPIO_TMT_WORKING_TIMADJ_TADJUS:** Time Adjust Value.

14.3.2.304 REG LXTS_TMT_LOW_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_0) — Offset 40301698h

TMT local cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	40301698h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTL_WORKING_REG:** TMTL captured when a local cross time stamp capture is enabled.

14.3.2.305 REG LXTS_TMT_HIGH_WORKING (TMT_LXTS_SNAPSHOT_WORKING_REG_1) — Offset 4030169Ch

TMT local cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	4030169Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_TMTH_WORKING_REG:** TMTH captured when a local cross time stamp capture is enabled.

14.3.2.306 REG LXTS_ART_LOW_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_0) — Offset 403016A0h

TMT local cross timestamp ART snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	403016A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_LOW_WORKING_REG:** ART bits [31:0]captured when a local cross time stamp capture is enabled.

14.3.2.307 REG LXTS_ART_HIGH_WORKING (TMT_ART_SNAPSHOT_WORKING_REG_1) — Offset 403016A4h

TMT local cross timestamp ART snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	403016A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_LXTS_ART_HIGH_WORKING_REG:** ART bits [63:0] captured when a local cross time stamp capture is enabled.

14.3.2.308 REG RXTS_TMT_LOW_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_0) — Offset 403016A8h

TMT remote cross timestamp snapshot register 0.

Type	Size	Offset	Default
MMIO	32 bit	403016A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTL_WORKING_REG:** TMTL captured when a remote time stamp capture is enabled.

14.3.2.309 REG RXTS_TMT_HIGH_WORKING (TMT_RXTS_SNAPSHOT_WORKING_REG_1) — Offset 403016ACh

TMT remote cross timestamp snapshot register 1.

Type	Size	Offset	Default
MMIO	32 bit	403016ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TGPIO_RXTS_TMTH_WORKING_REG:** TMTH captured when a remote time stamp capture is enabled.

14.4 IPC Registers

The IPC registers contain:

- Host Registers
- PMC Registers

IPC Registers	Address Offset	Table
Host	40400000h - 40400C54h	Table 14-13
PMC	40411000h - 404116D4h	Table 14-14

14.4.1 Host Registers Summary

Table 14-13. Summary of Host Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40400000h	4	Peripheral Interrupt Status - LH2OSE (PISR_LH2OSE)	00000000h
40400004h	4	Peripheral Interrupt Mask - LH2OSE (PIMR_LH2OSE)	00000000h
40400008h	4	LH2OSE Peripheral Interrupt Mask (HOST_PIMR_LH2OSE)	00000101h
4040000Ch	4	LH2OSE Peripheral Interrupt Status (HOST_PISR_LH2OSE)	00000000h
40400010h	4	LH2OSE Channel Interrupt Mask (CIM_LH2OSE)	00000000h
40400014h	4	LH2OSE Channel Interrupt Status (CIS_LH2OSE)	00000000h
40400034h	4	LH2OSE Firmware Status (ISH_HOST_FWSTS_LH2OSE)	00000000h
40400038h	4	LH2OSE Communication (HOST_COMM_LH2OSE)	00000000h
40400048h	4	Inbound DoorbellLH2OSE To ISH (HOST2ISH_DOORBELL_LH2OSE)	00000000h
40400054h	4	Outbound DoorbellISH To LH2OSE (ISH2HOST_DOORBELL_LH2OSE)	00000000h
40400060h	4	Outbound Inter Processor Message 1 From ISH To LH2OSE (ISH2HOST_MSG1_LH2OSE)	00000000h
40400064h	4	Outbound Inter Processor Message 2 From ISH To LH2OSE (ISH2HOST_MSG2_LH2OSE)	00000000h
40400068h	4	Outbound Inter Processor Message 3 From ISH To LH2OSE (ISH2HOST_MSG3_LH2OSE)	00000000h
4040006Ch	4	Outbound Inter Processor Message 4 From ISH To LH2OSE (ISH2HOST_MSG4_LH2OSE)	00000000h
40400070h	4	Outbound Inter Processor Message 5 From ISH To LH2OSE (ISH2HOST_MSG5_LH2OSE)	00000000h
40400074h	4	Outbound Inter Processor Message 6 From ISH To LH2OSE (ISH2HOST_MSG6_LH2OSE)	00000000h
40400078h	4	Outbound Inter Processor Message 7 From ISH To LH2OSE (ISH2HOST_MSG7_LH2OSE)	00000000h
4040007Ch	4	Outbound Inter Processor Message 8 From ISH To LH2OSE (ISH2HOST_MSG8_LH2OSE)	00000000h
40400080h	4	Outbound Inter Processor Message 9 From ISH To LH2OSE (ISH2HOST_MSG9_LH2OSE)	00000000h
40400084h	4	Outbound Inter Processor Message 10 From ISH To LH2OSE (ISH2HOST_MSG10_LH2OSE)	00000000h
40400088h	4	Outbound Inter Processor Message 11 From ISH To LH2OSE (ISH2HOST_MSG11_LH2OSE)	00000000h
4040008Ch	4	Outbound Inter Processor Message 12 From ISH To LH2OSE (ISH2HOST_MSG12_LH2OSE)	00000000h
40400090h	4	Outbound Inter Processor Message 13 From ISH To LH2OSE (ISH2HOST_MSG13_LH2OSE)	00000000h
40400094h	4	Outbound Inter Processor Message 14 From ISH To LH2OSE (ISH2HOST_MSG14_LH2OSE)	00000000h
40400098h	4	Outbound Inter Processor Message 15 From ISH To LH2OSE (ISH2HOST_MSG15_LH2OSE)	00000000h
4040009Ch	4	Outbound Inter Processor Message 16 From ISH To LH2OSE (ISH2HOST_MSG16_LH2OSE)	00000000h
404000A0h	4	Outbound Inter Processor Message 17 From ISH To LH2OSE (ISH2HOST_MSG17_LH2OSE)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
404000A4h	4	Outbound Inter Processor Message 18 From ISH To LH2OSE (ISH2HOST_MSG18_LH2OSE)	00000000h
404000A8h	4	Outbound Inter Processor Message 19 From ISH To LH2OSE (ISH2HOST_MSG19_LH2OSE)	00000000h
404000ACh	4	Outbound Inter Processor Message 20 From ISH To LH2OSE (ISH2HOST_MSG20_LH2OSE)	00000000h
404000B0h	4	Outbound Inter Processor Message 21 From ISH To LH2OSE (ISH2HOST_MSG21_LH2OSE)	00000000h
404000B4h	4	Outbound Inter Processor Message 22 From ISH To LH2OSE (ISH2HOST_MSG22_LH2OSE)	00000000h
404000B8h	4	Outbound Inter Processor Message 23 From ISH To LH2OSE (ISH2HOST_MSG23_LH2OSE)	00000000h
404000BCh	4	Outbound Inter Processor Message 24 From ISH To LH2OSE (ISH2HOST_MSG24_LH2OSE)	00000000h
404000C0h	4	Outbound Inter Processor Message 25 From ISH To LH2OSE (ISH2HOST_MSG25_LH2OSE)	00000000h
404000C4h	4	Outbound Inter Processor Message 26 From ISH To LH2OSE (ISH2HOST_MSG26_LH2OSE)	00000000h
404000C8h	4	Outbound Inter Processor Message 27 From ISH To LH2OSE (ISH2HOST_MSG27_LH2OSE)	00000000h
404000CCh	4	Outbound Inter Processor Message 28 From ISH To LH2OSE (ISH2HOST_MSG28_LH2OSE)	00000000h
404000D0h	4	Outbound Inter Processor Message 29 From ISH To LH2OSE (ISH2HOST_MSG29_LH2OSE)	00000000h
404000D4h	4	Outbound Inter Processor Message 30 From ISH To LH2OSE (ISH2HOST_MSG30_LH2OSE)	00000000h
404000D8h	4	Outbound Inter Processor Message 31 From ISH To LH2OSE (ISH2HOST_MSG31_LH2OSE)	00000000h
404000DCh	4	Outbound Inter Processor Message 32 From ISH To LH2OSE (ISH2HOST_MSG32_LH2OSE)	00000000h
404000E0h	4	Inbound Inter Processor Message 1 From LH2OSE To ISH (HOST2ISH_MSG1_LH2OSE)	00000000h
404000E4h	4	Inbound Inter Processor Message 2 From LH2OSE To ISH (HOST2ISH_MSG2_LH2OSE)	00000000h
404000E8h	4	Inbound Inter Processor Message 3 From LH2OSE To ISH (HOST2ISH_MSG3_LH2OSE)	00000000h
404000ECh	4	Inbound Inter Processor Message 4 From LH2OSE To ISH (HOST2ISH_MSG4_LH2OSE)	00000000h
404000F0h	4	Inbound Inter Processor Message 5 From LH2OSE To ISH (HOST2ISH_MSG5_LH2OSE)	00000000h
404000F4h	4	Inbound Inter Processor Message 6 From LH2OSE To ISH (HOST2ISH_MSG6_LH2OSE)	00000000h
404000F8h	4	Inbound Inter Processor Message 7 From LH2OSE To ISH (HOST2ISH_MSG7_LH2OSE)	00000000h
404000FCh	4	Inbound Inter Processor Message 8 From LH2OSE To ISH (HOST2ISH_MSG8_LH2OSE)	00000000h
40400100h	4	Inbound Inter Processor Message 9 From LH2OSE To ISH (HOST2ISH_MSG9_LH2OSE)	00000000h
40400104h	4	Inbound Inter Processor Message 10 From LH2OSE To ISH (HOST2ISH_MSG10_LH2OSE)	00000000h
40400108h	4	Inbound Inter Processor Message 11 From LH2OSE To ISH (HOST2ISH_MSG11_LH2OSE)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4040010Ch	4	Inbound Inter Processor Message 12 From LH2OSE To ISH (HOST2ISH_MSG12_LH2OSE)	00000000h
40400110h	4	Inbound Inter Processor Message 13 From LH2OSE To ISH (HOST2ISH_MSG13_LH2OSE)	00000000h
40400114h	4	Inbound Inter Processor Message 14 From LH2OSE To ISH (HOST2ISH_MSG14_LH2OSE)	00000000h
40400118h	4	Inbound Inter Processor Message 15 From LH2OSE To ISH (HOST2ISH_MSG15_LH2OSE)	00000000h
4040011Ch	4	Inbound Inter Processor Message 16 From LH2OSE To ISH (HOST2ISH_MSG16_LH2OSE)	00000000h
40400120h	4	Inbound Inter Processor Message 17 From LH2OSE To ISH (HOST2ISH_MSG17_LH2OSE)	00000000h
40400124h	4	Inbound Inter Processor Message 18 From LH2OSE To ISH (HOST2ISH_MSG18_LH2OSE)	00000000h
40400128h	4	Inbound Inter Processor Message 19 From LH2OSE To ISH (HOST2ISH_MSG19_LH2OSE)	00000000h
4040012Ch	4	Inbound Inter Processor Message 20 From LH2OSE To ISH (HOST2ISH_MSG20_LH2OSE)	00000000h
40400130h	4	Inbound Inter Processor Message 21 From LH2OSE To ISH (HOST2ISH_MSG21_LH2OSE)	00000000h
40400134h	4	Inbound Inter Processor Message 22 From LH2OSE To ISH (HOST2ISH_MSG22_LH2OSE)	00000000h
40400138h	4	Inbound Inter Processor Message 23 From LH2OSE To ISH (HOST2ISH_MSG23_LH2OSE)	00000000h
4040013Ch	4	Inbound Inter Processor Message 24 From LH2OSE To ISH (HOST2ISH_MSG24_LH2OSE)	00000000h
40400140h	4	Inbound Inter Processor Message 25 From LH2OSE To ISH (HOST2ISH_MSG25_LH2OSE)	00000000h
40400144h	4	Inbound Inter Processor Message 26 From LH2OSE To ISH (HOST2ISH_MSG26_LH2OSE)	00000000h
40400148h	4	Inbound Inter Processor Message 27 From LH2OSE To ISH (HOST2ISH_MSG27_LH2OSE)	00000000h
4040014Ch	4	Inbound Inter Processor Message 28 From LH2OSE To ISH (HOST2ISH_MSG28_LH2OSE)	00000000h
40400150h	4	Inbound Inter Processor Message 29 From LH2OSE To ISH (HOST2ISH_MSG29_LH2OSE)	00000000h
40400154h	4	Inbound Inter Processor Message 30 From LH2OSE To ISH (HOST2ISH_MSG30_LH2OSE)	00000000h
40400158h	4	Inbound Inter Processor Message 31 From LH2OSE To ISH (HOST2ISH_MSG31_LH2OSE)	00000000h
4040015Ch	4	Inbound Inter Processor Message 32 From LH2OSE To ISH (HOST2ISH_MSG32_LH2OSE)	00000000h
40400360h	4	Remap0 For LH2OSE (REMAP0_LH2OSE)	00000000h
40400364h	4	Remap1 For LH2OSE (REMAP1_LH2OSE)	00000000h
40400368h	4	Remap2 For LH2OSE (REMAP2_LH2OSE)	00000000h
4040036Ch	4	Remap3 For LH2OSE (REMAP3_LH2OSE)	00000000h
40400370h	4	Remap4 For LH2OSE (REMAP4_LH2OSE)	00000000h
40400374h	4	Remap5 For LH2OSE (REMAP5_LH2OSE)	00000000h
40400378h	4	ISH IPC Busy Clear For LH2OSE (ISH_IPC_BUSY_CLEAR_LH2OSE)	00000000h
404006D0h	4	D0i3 Control For LH2OSE (IPC_D0I3C_LH2OSE)	00000008h

14.4.1.1 Peripheral Interrupt Status - LH2OSE (PISR_LH2OSE) — Offset 40400000h

This register contains the inbound interrupt status bits for the LH2OSE IPC channel. Interrupts are generated when PISR[x] & PIMR[x] are both set.

Type	Size	Offset	Default
MMIO	32 bit	40400000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW/1C	**PISR_H2IBCISC:** Host2ISH busy clear interrupt status clear interrupt: 1 -> Interrupt is active 0 -> Interrupt is inactive. Writing 1 to this bit clears it.
26:1	0h RO	**Reserved**
0	0h RO	**PISR_HOST2ISH:** Inbound IPC request from HOST to ISH status: 1 -> Interrupt is active 0 -> Interrupt is inactive.

14.4.1.2 Peripheral Interrupt Mask - LH2OSE (PIMR_LH2OSE) — Offset 40400004h

This register enables or disables Inbound interrupts from LH2OSE to ISH. This register is not accessible by LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	40400004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**H2IBCISC_IE:** Mask bit for H2IBCISC interrupt mask 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
26:12	0h RO	**Reserved**
11	0h RW	**PIMR_ISH2HOST_BUSY_CLEAR:** Mask bit for ISH2HOST busy clear interrupt 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
10:1	0h RO	**Reserved**
0	0h RW	**PIMR_HOST2ISH:** Reserved

14.4.1.3 LH2OSE Peripheral Interrupt Mask (HOST_PIMR_LH2OSE) — Offset 40400008h

This register is for enabling the interrupts generated by ISH towards LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	40400008h	00000101h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	1h NA	**PIMR_HOST2ISH_BUSY_CLEAR:** Host2ISH busy clear interrupt mask bit 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
7:1	0h RO	**Reserved**
0	1h NA	**PIMR_ISH2HOST_IPC_REG:** Outbound IPC request from ISH to HOST Mask 1 -> Interrupt is unmasked 0 -> Interrupt is masked.

14.4.1.4 LH2OSE Peripheral Interrupt Status (HOST_PISR_LH2OSE) — Offset 4040000Ch

Interrupt status register for interrupts to LH2OSE.

Type	Size	Offset	Default
MMIO	32 bit	4040000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h NA	**PISR_HOST2ISH_BUSY_CLEAR:** Host2ISH busy clear interrupt status bit 1 -> Interrupt is active.
7:1	0h RO	**Reserved**
0	0h NA	**PISR_ISH2HOST_IPC_REG:** Outbound IPC request from ISH to HOST Status 1 -> Interrupt.

14.4.1.5 LH2OSE Channel Interrupt Mask (CIM_LH2OSE) — Offset 40400010h

This register is for masking the per channel interrupt, caused by any of the interrupt sources towards mIA in the IPC Channel.

Type	Size	Offset	Default
MMIO	32 bit	40400010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**CH_INTR_MASK:** Enable interrupts towards MIA for the channel. 1 -> Interrupt is masked 0 -> Interrupt is enabled.

14.4.1.6 LH2OSE Channel Interrupt Status (CIS_LH2OSE) — Offset 40400014h

This register provides the per channel interrupt status, this is set if any of the interrupt sources towards mIA are set in the IPC Channel.

Type	Size	Offset	Default
MMIO	32 bit	40400014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CH_INTR_STATUS:** Interrupt status for the interrupts to MIA for the channel. This will be set if any of the interrupt soruces are enabled and their status is high.

14.4.1.7 LH2OSE Firmware Status (ISH_HOST_FWSTS_LH2OSE) — Offset 40400034h

Writeable by ISH, RO by LH2OSE, this is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. As the firmware comes up after the reset or power cycle it sets bits of this register to 1b1 to indicate its status.

Type	Size	Offset	Default
MMIO	32 bit	40400034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**ISH_HOST_FWSTS:** ISH Host firmware status.

14.4.1.8 LH2OSE Communication (HOST_COMM_LH2OSE) — Offset 40400038h

Wrtieable by LH2OSE, RO by ISH, this is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. The Host sets bits of this register to 1b1 to communicate with the ISH.

Type	Size	Offset	Default
MMIO	32 bit	40400038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HOST_COMM:** Host communication register.

14.4.1.9 Inbound DoorbellLH2OSE To ISH (HOST2ISH_DOORBELL_LH2OSE) — Offset 40400048h

Inbound doorbell register, from LH2OSE core to interrupt ISH. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. When software writes the message in to respective message register, it should set bit 31(BUSY Bit) of doorbell register to indicate that new data is written. The ISH will assert a level sensitive interrupt to the IOAPIC as long as the BUSY bit is set. When the ISH reads the message code from this register it should write back to this register and clear the BUSY bit.

Type	Size	Offset	Default
MMIO	32 bit	40400048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the ISH CPU is Ready to accept a new message.
30:0	00000000h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

14.4.1.10 Outbound DoorbellISH To LH2OSE (ISH2HOST_DOORBELL_LH2OSE) — Offset 40400054h

Outbound doorbell register for the ISH to interrupt LH2OSE. Setting bit 31 of this register causes the Host to receive a IRQn interrupt. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. The ISH will set bit 31 of this reg to ring the doorbell after it has completed programming the message to Host. When the Host reads the message code from this register it should write back to this register and clear the BUSY bit.

Type	Size	Offset	Default
MMIO	32 bit	40400054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the HOST CPU is Ready to accept a new message.
30:0	00000000h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

14.4.1.11 Outbound Inter Processor Message 1 From ISH To LH2OSE (ISH2HOST_MSG1_LH2OSE) — Offset 40400060h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	40400060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from ISH to LH2OSE.

14.4.1.12 Outbound Inter Processor Message 2 From ISH To LH2OSE (ISH2HOST_MSG2_LH2OSE) — Offset 40400064h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.13 Outbound Inter Processor Message 3 From ISH To LH2OSE (ISH2HOST_MSG3_LH2OSE) — Offset 40400068h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.14 Outbound Inter Processor Message 4 From ISH To LH2OSE (ISH2HOST_MSG4_LH2OSE) — Offset 4040006Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.15 Outbound Inter Processor Message 5 From ISH To LH2OSE (ISH2HOST_MSG5_LH2OSE) — Offset 40400070h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.16 Outbound Inter Processor Message 6 From ISH To LH2OSE (ISH2HOST_MSG6_LH2OSE) — Offset 40400074h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.17 Outbound Inter Processor Message 7 From ISH To LH2OSE (ISH2HOST_MSG7_LH2OSE) — Offset 40400078h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.18 Outbound Inter Processor Message 8 From ISH To LH2OSE (ISH2HOST_MSG8_LH2OSE) — Offset 4040007Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.19 Outbound Inter Processor Message 9 From ISH To LH2OSE (ISH2HOST_MSG9_LH2OSE) — Offset 40400080h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.20 Outbound Inter Processor Message 10 From ISH To LH2OSE (ISH2HOST_MSG10_LH2OSE) — Offset 40400084h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.21 Outbound Inter Processor Message 11 From ISH To LH2OSE (ISH2HOST_MSG11_LH2OSE) — Offset 40400088h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.22 Outbound Inter Processor Message 12 From ISH To LH2OSE (ISH2HOST_MSG12_LH2OSE) — Offset 4040008Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.23 Outbound Inter Processor Message 13 From ISH To LH2OSE (ISH2HOST_MSG13_LH2OSE) — Offset 40400090h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.24 Outbound Inter Processor Message 14 From ISH To LH2OSE (ISH2HOST_MSG14_LH2OSE) — Offset 40400094h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.25 Outbound Inter Processor Message 15 From ISH To LH2OSE (ISH2HOST_MSG15_LH2OSE) — Offset 40400098h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.26 Outbound Inter Processor Message 16 From ISH To LH2OSE (ISH2HOST_MSG16_LH2OSE) — Offset 4040009Ch

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.27 Outbound Inter Processor Message 17 From ISH To LH2OSE (ISH2HOST_MSG17_LH2OSE) — Offset 404000A0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.28 Outbound Inter Processor Message 18 From ISH To LH2OSE (ISH2HOST_MSG18_LH2OSE) — Offset 404000A4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.29 Outbound Inter Processor Message 19 From ISH To LH2OSE (ISH2HOST_MSG19_LH2OSE) — Offset 404000A8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.30 Outbound Inter Processor Message 20 From ISH To LH2OSE (ISH2HOST_MSG20_LH2OSE) — Offset 404000ACh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.31 Outbound Inter Processor Message 21 From ISH To LH2OSE (ISH2HOST_MSG21_LH2OSE) — Offset 404000B0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.32 Outbound Inter Processor Message 22 From ISH To LH2OSE (ISH2HOST_MSG22_LH2OSE) — Offset 404000B4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.33 Outbound Inter Processor Message 23 From ISH To LH2OSE (ISH2HOST_MSG23_LH2OSE) — Offset 404000B8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.34 Outbound Inter Processor Message 24 From ISH To LH2OSE (ISH2HOST_MSG24_LH2OSE) — Offset 404000BCh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.35 Outbound Inter Processor Message 25 From ISH To LH2OSE (ISH2HOST_MSG25_LH2OSE) — Offset 404000C0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.36 Outbound Inter Processor Message 26 From ISH To LH2OSE (ISH2HOST_MSG26_LH2OSE) — Offset 404000C4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.37 Outbound Inter Processor Message 27 From ISH To LH2OSE (ISH2HOST_MSG27_LH2OSE) — Offset 404000C8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.38 Outbound Inter Processor Message 28 From ISH To LH2OSE (ISH2HOST_MSG28_LH2OSE) — Offset 404000CCh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.39 Outbound Inter Processor Message 29 From ISH To LH2OSE (ISH2HOST_MSG29_LH2OSE) — Offset 404000D0h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.40 Outbound Inter Processor Message 30 From ISH To LH2OSE (ISH2HOST_MSG30_LH2OSE) — Offset 404000D4h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.41 Outbound Inter Processor Message 31 From ISH To LH2OSE (ISH2HOST_MSG31_LH2OSE) — Offset 404000D8h

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.42 Outbound Inter Processor Message 32 From ISH To LH2OSE (ISH2HOST_MSG32_LH2OSE) — Offset 404000DCh

Inter-process Message registers for ISH core to communicate to LH2OSE. These are eight 32bit registers that hold the message payload from the ISH to LH2OSE. These registers are meant to be written by the ISH and read by LH2OSE. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as ISH2HOST_MSG1_LH2OSE, offset 40400060h.

14.4.1.43 Inbound Inter Processor Message 1 From LH2OSE To ISH (HOST2ISH_MSG1_LH2OSE) — Offset 404000E0h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	404000E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSG:** Message from LH2OSE to ISH.

14.4.1.44 Inbound Inter Processor Message 2 From LH2OSE To ISH (HOST2ISH_MSG2_LH2OSE) — Offset 404000E4h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.45 Inbound Inter Processor Message 3 From LH2OSE To ISH (HOST2ISH_MSG3_LH2OSE) — Offset 404000E8h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.46 Inbound Inter Processor Message 4 From LH2OSE To ISH (HOST2ISH_MSG4_LH2OSE) — Offset 404000ECh

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.47 Inbound Inter Processor Message 5 From LH2OSE To ISH (HOST2ISH_MSG5_LH2OSE) — Offset 404000F0h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.48 Inbound Inter Processor Message 6 From LH2OSE To ISH (HOST2ISH_MSG6_LH2OSE) — Offset 404000F4h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.49 Inbound Inter Processor Message 7 From LH2OSE To ISH (HOST2ISH_MSG7_LH2OSE) — Offset 404000F8h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.50 Inbound Inter Processor Message 8 From LH2OSE To ISH (HOST2ISH_MSG8_LH2OSE) — Offset 404000FCh

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.51 Inbound Inter Processor Message 9 From LH2OSE To ISH (HOST2ISH_MSG9_LH2OSE) — Offset 40400100h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.52 Inbound Inter Processor Message 10 From LH2OSE To ISH (HOST2ISH_MSG10_LH2OSE) — Offset 40400104h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.53 Inbound Inter Processor Message 11 From LH2OSE To ISH (HOST2ISH_MSG11_LH2OSE) — Offset 40400108h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.54 Inbound Inter Processor Message 12 From LH2OSE To ISH (HOST2ISH_MSG12_LH2OSE) — Offset 4040010Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.55 Inbound Inter Processor Message 13 From LH2OSE To ISH (HOST2ISH_MSG13_LH2OSE) — Offset 40400110h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.56 Inbound Inter Processor Message 14 From LH2OSE To ISH (HOST2ISH_MSG14_LH2OSE) — Offset 40400114h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.57 Inbound Inter Processor Message 15 From LH2OSE To ISH (HOST2ISH_MSG15_LH2OSE) — Offset 40400118h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.58 Inbound Inter Processor Message 16 From LH2OSE To ISH (HOST2ISH_MSG16_LH2OSE) — Offset 4040011Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.59 Inbound Inter Processor Message 17 From LH2OSE To ISH (HOST2ISH_MSG17_LH2OSE) — Offset 40400120h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.60 Inbound Inter Processor Message 18 From LH2OSE To ISH (HOST2ISH_MSG18_LH2OSE) — Offset 40400124h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.61 Inbound Inter Processor Message 19 From LH2OSE To ISH (HOST2ISH_MSG19_LH2OSE) — Offset 40400128h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.62 Inbound Inter Processor Message 20 From LH2OSE To ISH (HOST2ISH_MSG20_LH2OSE) — Offset 4040012Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.63 Inbound Inter Processor Message 21 From LH2OSE To ISH (HOST2ISH_MSG21_LH2OSE) — Offset 40400130h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.64 Inbound Inter Processor Message 22 From LH2OSE To ISH (HOST2ISH_MSG22_LH2OSE) — Offset 40400134h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.65 Inbound Inter Processor Message 23 From LH2OSE To ISH (HOST2ISH_MSG23_LH2OSE) — Offset 40400138h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.66 Inbound Inter Processor Message 24 From LH2OSE To ISH (HOST2ISH_MSG24_LH2OSE) — Offset 4040013Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.67 Inbound Inter Processor Message 25 From LH2OSE To ISH (HOST2ISH_MSG25_LH2OSE) — Offset 40400140h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.68 Inbound Inter Processor Message 26 From LH2OSE To ISH (HOST2ISH_MSG26_LH2OSE) — Offset 40400144h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.69 Inbound Inter Processor Message 27 From LH2OSE To ISH (HOST2ISH_MSG27_LH2OSE) — Offset 40400148h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.70 Inbound Inter Processor Message 28 From LH2OSE To ISH (HOST2ISH_MSG28_LH2OSE) — Offset 4040014Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.71 Inbound Inter Processor Message 29 From LH2OSE To ISH (HOST2ISH_MSG29_LH2OSE) — Offset 40400150h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.72 Inbound Inter Processor Message 30 From LH2OSE To ISH (HOST2ISH_MSG30_LH2OSE) — Offset 40400154h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.73 Inbound Inter Processor Message 31 From LH2OSE To ISH (HOST2ISH_MSG31_LH2OSE) — Offset 40400158h

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.74 Inbound Inter Processor Message 32 From LH2OSE To ISH (HOST2ISH_MSG32_LH2OSE) — Offset 4040015Ch

Inter-process Message registers for LH2OSE to communicate to the ISH. These are eight 32bit registers that hold the message payload from LH2OSE to ISH. These registers are meant to be written by LH2OSE and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_LH2OSE, offset 404000E0h.

14.4.1.75 Remap0 For LH2OSE (REMAP0_LH2OSE) — Offset 40400360h

General purpose Remap regs.

Type	Size	Offset	Default
MMIO	32 bit	40400360h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**REMAP:** Remap.

14.4.1.76 Remap1 For LH2OSE (REMAP1_LH2OSE) — Offset 40400364h

General purpose Remap regs.

Note: Bit definitions are the same as REMAP0_LH2OSE, offset 40400360h.

14.4.1.77 Remap2 For LH2OSE (REMAP2_LH2OSE) — Offset 40400368h

General purpose Remap regs.

Note: Bit definitions are the same as REMAP0_LH2OSE, offset 40400360h.

14.4.1.78 Remap3 For LH2OSE (REMAP3_LH2OSE) — Offset 4040036Ch

General purpose Remap regs.

Note: Bit definitions are the same as REMAP0_LH2OSE, offset 40400360h.

14.4.1.79 Remap4 For LH2OSE (REMAP4_LH2OSE) — Offset 40400370h

General purpose Remap regs.

Note: Bit definitions are the same as REMAP0_LH2OSE, offset 40400360h.

14.4.1.80 Remap5 For LH2OSE (REMAP5_LH2OSE) — Offset 40400374h

General purpose Remap regs.

Note: Bit definitions are the same as REMAP0_LH2OSE, offset 40400360h.

14.4.1.81 ISH IPC Busy Clear For LH2OSE (ISH_IPC_BUSY_CLEAR_LH2OSE) — Offset 40400378h

This register holds the status of the ISH IPC busy clear interrupts. ISH IPC busy clear interrupt is set when busy bit of respective outbound doorbell register gets cleared and interrupt is cleared when ISH writes 1 to respective bit in ISH IPC busy clear register.

Type	Size	Offset	Default
MMIO	32 bit	40400378h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**ISH2HOST_BUSY_CLEAR:** Busy clear interrupt bit of ISH2HOST IPC 1 -> Interrupt active 0 -> Interrupt inactive.

14.4.1.82 D0i3 Control For LH2OSE (IPC_D0I3C_LH2OSE) — Offset 404006D0h

This register is will be used for D0i3 SW flow. The description below also includes the type of access expected for the ISH FW for each configuration bit: 1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost. 2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit. 3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW. 4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear). The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following: 1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1. 2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied. 3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	404006D0h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

14.4.2 PMC Registers Summary

Table 14-14. Summary of PMC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40411000h	4	Peripheral Interrupt Status - PMC (PISR_PMC)	00000000h
40411004h	4	Peripheral Interrupt Mask - PMC (PIMR_PMC)	00000000h
40411008h	4	PMC Peripheral Interrupt Mask (HOST_PIMR_PMC)	00000101h
4041100Ch	4	PMC Peripheral Interrupt Status (HOST_PISR_PMC)	00000000h
40411010h	4	PMC Channel Interrupt Mask (CIM_PMC)	00000000h
40411014h	4	PMC Channel Interrupt Status (CIS_PMC)	00000000h
40411048h	4	Inbound DoorbellPMC To ISH (HOST2ISH_DOORBELL_PMC)	00000000h
40411054h	4	Outbound DoorbellISH To PMC (ISH2HOST_DOORBELL_PMC)	00000000h
404110E0h	4	Inbound Inter Processor Message 1 From PMC To ISH (HOST2ISH_MSG1_PMC)	00000000h
404110E4h	4	Inbound Inter Processor Message 2 From PMC To ISH (HOST2ISH_MSG2_PMC)	00000000h
404110E8h	4	Inbound Inter Processor Message 3 From PMC To ISH (HOST2ISH_MSG3_PMC)	00000000h
404110ECh	4	Inbound Inter Processor Message 4 From PMC To ISH (HOST2ISH_MSG4_PMC)	00000000h
404110F0h	4	Inbound Inter Processor Message 5 From PMC To ISH (HOST2ISH_MSG5_PMC)	00000000h
404110F4h	4	Inbound Inter Processor Message 6 From PMC To ISH (HOST2ISH_MSG6_PMC)	00000000h
404110F8h	4	Inbound Inter Processor Message 7 From PMC To ISH (HOST2ISH_MSG7_PMC)	00000000h
404110FCh	4	Inbound Inter Processor Message 8 From PMC To ISH (HOST2ISH_MSG8_PMC)	00000000h
40411100h	4	Inbound Inter Processor Message 9 From PMC To ISH (HOST2ISH_MSG9_PMC)	00000000h
40411104h	4	Inbound Inter Processor Message 10 From PMC To ISH (HOST2ISH_MSG10_PMC)	00000000h
40411108h	4	Inbound Inter Processor Message 11 From PMC To ISH (HOST2ISH_MSG11_PMC)	00000000h
4041110Ch	4	Inbound Inter Processor Message 12 From PMC To ISH (HOST2ISH_MSG12_PMC)	00000000h
40411110h	4	Inbound Inter Processor Message 13 From PMC To ISH (HOST2ISH_MSG13_PMC)	00000000h
40411114h	4	Inbound Inter Processor Message 14 From PMC To ISH (HOST2ISH_MSG14_PMC)	00000000h
40411118h	4	Inbound Inter Processor Message 15 From PMC To ISH (HOST2ISH_MSG15_PMC)	00000000h
4041111Ch	4	Inbound Inter Processor Message 16 From PMC To ISH (HOST2ISH_MSG16_PMC)	00000000h
40411120h	4	Inbound Inter Processor Message 17 From PMC To ISH (HOST2ISH_MSG17_PMC)	00000000h
40411124h	4	Inbound Inter Processor Message 18 From PMC To ISH (HOST2ISH_MSG18_PMC)	00000000h
40411128h	4	Inbound Inter Processor Message 19 From PMC To ISH (HOST2ISH_MSG19_PMC)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4041112Ch	4	Inbound Inter Processor Message 20 From PMC To ISH (HOST2ISH_MSG20_PMC)	00000000h
40411130h	4	Inbound Inter Processor Message 21 From PMC To ISH (HOST2ISH_MSG21_PMC)	00000000h
40411134h	4	Inbound Inter Processor Message 22 From PMC To ISH (HOST2ISH_MSG22_PMC)	00000000h
40411138h	4	Inbound Inter Processor Message 23 From PMC To ISH (HOST2ISH_MSG23_PMC)	00000000h
4041113Ch	4	Inbound Inter Processor Message 24 From PMC To ISH (HOST2ISH_MSG24_PMC)	00000000h
40411140h	4	Inbound Inter Processor Message 25 From PMC To ISH (HOST2ISH_MSG25_PMC)	00000000h
40411144h	4	Inbound Inter Processor Message 26 From PMC To ISH (HOST2ISH_MSG26_PMC)	00000000h
40411148h	4	Inbound Inter Processor Message 27 From PMC To ISH (HOST2ISH_MSG27_PMC)	00000000h
4041114Ch	4	Inbound Inter Processor Message 28 From PMC To ISH (HOST2ISH_MSG28_PMC)	00000000h
40411150h	4	Inbound Inter Processor Message 29 From PMC To ISH (HOST2ISH_MSG29_PMC)	00000000h
40411154h	4	Inbound Inter Processor Message 30 From PMC To ISH (HOST2ISH_MSG30_PMC)	00000000h
40411158h	4	Inbound Inter Processor Message 31 From PMC To ISH (HOST2ISH_MSG31_PMC)	00000000h
4041115Ch	4	Inbound Inter Processor Message 32 From PMC To ISH (HOST2ISH_MSG32_PMC)	00000000h
40411378h	4	ISH IPC Busy Clear For PMC (ISH_IPC_BUSY_CLEAR_PMC)	00000000h
404116D4h	4	PMC To ISH Control And Status (PMC2ISH_CSR_PMC)	00000000h

14.4.2.1 Peripheral Interrupt Status - PMC (PISR_PMC) — Offset 40411000h

This register contains the inbound interrupt status bits for the PMC IPC channel. Interrupts are generated when PISR[x] & PIMR[x] are both set.

Type	Size	Offset	Default
MMIO	32 bit	40411000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW/1C	**PISR_H2IBCISC:** Host2ISH busy clear interrupt status clear interrupt: 1 -> Interrupt is active 0 -> Interrupt is inactive. Writing 1 to this bit clears it.
26:1	0h RO	**Reserved**
0	0h RO	**PISR_HOST2ISH:** Inbound IPC request from HOST to ISH status: 1 -> Interrupt is active 0 -> Interrupt is inactive.

14.4.2.2 Peripheral Interrupt Mask - PMC (PIMR_PMC) — Offset 40411004h

This register enables or disables Inbound interrupts from PMC to ISH. This register is not accessible by PMC.

Type	Size	Offset	Default
MMIO	32 bit	40411004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**H2IBCISC_IE:** Mask bit for H2IBCISC interrupt mask 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
26:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**PIMR_ISH2HOST_BUSY_CLEAR:** Mask bit for ISH2HOST busy clear interrupt 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
10:1	0h RO	**Reserved**
0	0h RW	**PIMR_HOST2ISH:** Reserved

14.4.2.3 PMC Peripheral Interrupt Mask (HOST_PIMR_PMC) — Offset 40411008h

This register is for enabling the interrupts generated by ISH towards PMC.

Type	Size	Offset	Default
MMIO	32 bit	40411008h	00000101h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	1h NA	**PIMR_HOST2ISH_BUSY_CLEAR:** Host2ISH busy clear interrupt mask bit 1 -> Interrupt is unmasked 0 -> Interrupt is masked.
7:1	0h RO	**Reserved**
0	1h NA	**PIMR_ISH2HOST_IPC_REG:** Outbound IPC request from ISH to HOST Mask 1 -> Interrupt is unmasked 0 -> Interrupt is masked.

14.4.2.4 PMC Peripheral Interrupt Status (HOST_PISR_PMC) — Offset 4041100Ch

Interrupt status register for interrupts to PMC.

Type	Size	Offset	Default
MMIO	32 bit	4041100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h NA	**PISR_HOST2ISH_BUSY_CLEAR:** Host2ISH busy clear interrupt status bit 1 -> Interrupt is active.
7:1	0h RO	**Reserved**
0	0h NA	**PISR_ISH2HOST_IPC_REG:** Outbound IPC request from ISH to HOST Status 1 -> Interrupt.

14.4.2.5 PMC Channel Interrupt Mask (CIM_PMC) — Offset 40411010h

This register is for masking the per channel interrupt, caused by any of the interrupt sources towards mIA in the IPC Channel.

Type	Size	Offset	Default
MMIO	32 bit	40411010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**CH_INTR_MASK:** Enable interrupts towards MIA for the channel. 1 -> Interrupt is masked 0 -> Interrupt is enabled.

14.4.2.6 PMC Channel Interrupt Status (CIS_PMC) — Offset 40411014h

This register provides the per channel interrupt status, this is set if any of the interrupt sources towards mIA are set in the IPC Channel.

Type	Size	Offset	Default
MMIO	32 bit	40411014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**CH_INTR_STATUS:** Interrupt status for the interrupts to MIA for the channel. This will be set if any of the interrupt soruces are enabled and their status is high.

14.4.2.7 Inbound DoorbellPMC To ISH (HOST2ISH_DOORBELL_PMC) — Offset 40411048h

Inbound doorbell register, from PMC core to interrupt ISH. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. When software writes the message in to respective message register, it should set bit 31(BUSY Bit) of doorbell register to indicate that new data is written. The ISH will assert a level sensitive interrupt to the IOAPIC as long as the BUSY bit is set. When the ISH reads the message code from this register it should write back to this register and clear the BUSY bit.

Type	Size	Offset	Default
MMIO	32 bit	40411048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the ISH CPU is Ready to accept a new message.
30:0	00000000h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

14.4.2.8 Outbound DoorbellISH To PMC (ISH2HOST_DOORBELL_PMC) — Offset 40411054h

Outbound doorbell register for the ISH to interrupt PMC. Setting bit 31 of this register causes the Host to receive a IRQn interrupt. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or

256bit payload registers. The ISH will set bit 31 of this reg to ring the doorbell after it has completed programming the message to Host. When the Host reads the message code from this register it should write back to this register and clear the BUSY bit.

Type	Size	Offset	Default
MMIO	32 bit	40411054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the HOST CPU is Ready to accept a new message.
30:0	00000000h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

14.4.2.9 Inbound Inter Processor Message 1 From PMC To ISH (HOST2ISH_MSG1_PMC) — Offset 404110E0h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Type	Size	Offset	Default
MMIO	32 bit	404110E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSG:** Message from PMC to ISH.

14.4.2.10 Inbound Inter Processor Message 2 From PMC To ISH (HOST2ISH_MSG2_PMC) — Offset 404110E4h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.11 Inbound Inter Processor Message 3 From PMC To ISH (HOST2ISH_MSG3_PMC) — Offset 404110E8h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.12 Inbound Inter Processor Message 4 From PMC To ISH (HOST2ISH_MSG4_PMC) — Offset 404110ECh

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.13 Inbound Inter Processor Message 5 From PMC To ISH (HOST2ISH_MSG5_PMC) — Offset 404110F0h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.14 Inbound Inter Processor Message 6 From PMC To ISH (HOST2ISH_MSG6_PMC) — Offset 404110F4h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.15 Inbound Inter Processor Message 7 From PMC To ISH (HOST2ISH_MSG7_PMC) — Offset 404110F8h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.16 Inbound Inter Processor Message 8 From PMC To ISH (HOST2ISH_MSG8_PMC) — Offset 404110FCh

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.17 Inbound Inter Processor Message 9 From PMC To ISH (HOST2ISH_MSG9_PMC) — Offset 40411100h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.18 Inbound Inter Processor Message 10 From PMC To ISH (HOST2ISH_MSG10_PMC) — Offset 40411104h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.19 Inbound Inter Processor Message 11 From PMC To ISH (HOST2ISH_MSG11_PMC) — Offset 40411108h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.20 Inbound Inter Processor Message 12 From PMC To ISH (HOST2ISH_MSG12_PMC) — Offset 4041110Ch

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.21 Inbound Inter Processor Message 13 From PMC To ISH (HOST2ISH_MSG13_PMC) — Offset 40411110h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.22 Inbound Inter Processor Message 14 From PMC To ISH (HOST2ISH_MSG14_PMC) — Offset 40411114h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.23 Inbound Inter Processor Message 15 From PMC To ISH (HOST2ISH_MSG15_PMC) — Offset 40411118h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.24 Inbound Inter Processor Message 16 From PMC To ISH (HOST2ISH_MSG16_PMC) — Offset 4041111Ch

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.25 Inbound Inter Processor Message 17 From PMC To ISH (HOST2ISH_MSG17_PMC) — Offset 40411120h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.26 Inbound Inter Processor Message 18 From PMC To ISH (HOST2ISH_MSG18_PMC) — Offset 40411124h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.27 Inbound Inter Processor Message 19 From PMC To ISH (HOST2ISH_MSG19_PMC) — Offset 40411128h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.28 Inbound Inter Processor Message 20 From PMC To ISH (HOST2ISH_MSG20_PMC) — Offset 4041112Ch

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.29 Inbound Inter Processor Message 21 From PMC To ISH (HOST2ISH_MSG21_PMC) — Offset 40411130h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.30 Inbound Inter Processor Message 22 From PMC To ISH (HOST2ISH_MSG22_PMC) — Offset 40411134h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.31 Inbound Inter Processor Message 23 From PMC To ISH (HOST2ISH_MSG23_PMC) — Offset 40411138h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.32 Inbound Inter Processor Message 24 From PMC To ISH (HOST2ISH_MSG24_PMC) — Offset 4041113Ch

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.33 Inbound Inter Processor Message 25 From PMC To ISH (HOST2ISH_MSG25_PMC) — Offset 40411140h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.34 Inbound Inter Processor Message 26 From PMC To ISH (HOST2ISH_MSG26_PMC) — Offset 40411144h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.35 Inbound Inter Processor Message 27 From PMC To ISH (HOST2ISH_MSG27_PMC) — Offset 40411148h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.36 Inbound Inter Processor Message 28 From PMC To ISH (HOST2ISH_MSG28_PMC) — Offset 4041114Ch

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.37 Inbound Inter Processor Message 29 From PMC To ISH (HOST2ISH_MSG29_PMC) — Offset 40411150h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.38 Inbound Inter Processor Message 30 From PMC To ISH (HOST2ISH_MSG30_PMC) — Offset 40411154h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.39 Inbound Inter Processor Message 31 From PMC To ISH (HOST2ISH_MSG31_PMC) — Offset 40411158h

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.40 Inbound Inter Processor Message 32 From PMC To ISH (HOST2ISH_MSG32_PMC) — Offset 4041115Ch

Inter-process Message registers for PMC to communicate to the ISH. These are eight 32bit registers that hold the message payload from PMC to ISH. These registers are meant to be written by PMC and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Note: Bit definitions are the same as HOST2ISH_MSG1_PMC, offset 404110E0h.

14.4.2.41 ISH IPC Busy Clear For PMC (ISH_IPC_BUSY_CLEAR_PMC) — Offset 40411378h

This register holds the status of the ISH IPC busy clear interrupts. ISH IPC busy clear interrupt is set when busy bit of respective outbound doorbell register gets cleared and interrupt is cleared when ISH writes 1 to respective bit in ISH IPC busy clear register.

Type	Size	Offset	Default
MMIO	32 bit	40411378h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**ISH2HOST_BUSY_CLEAR:** Busy clear interrupt bit of ISH2HOST IPC 1 -> Interrupt active 0 -> Interrupt inactive.

14.4.2.42 PMC To ISH Control And Status (PMC2ISH_CSR_PMC) — Offset 404116D4h

This is a control and status register for enabling PMC to interrupt mIA by setting any of the bits of the register. The Interrupt is then cleared by mIA by writing 1 b1 to this register after the appropriate ISR is serviced. The definitions of these bits are defined by the software.

Type	Size	Offset	Default
MMIO	32 bit	404116D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**Control Status (CSR):** Control and status information transfer between ISH and PMC Fws and interrupt generation to mIA.

14.5 PMU Registers

PMU Registers	Address Offset	Table
PMU	40500000h - 40500F40h	Table 14-15

14.5.1 PMU Registers Summary

Table 14-15. Summary of PMU Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40500000h	4	SRAM Bank Power Gate Enable (PMU_SRAM_PG_EN)	03FFFFFFh
40500010h	4	Wake Mask-1 (PMU_ISH_MASK_EVENT)	00000000h
40500018h	4	Fabric Idle And Time Out Count Configuration (PMU_ISH_FABRIC_CNT)	3A980008h
4050001Ch	4	Glitch Bypass Enable (PMU_ISH_GLITCH_BYPASS)	00000001h
40500020h	4	RF And ROM Clock Gate To Isolation Enable Count. (PMU_RF_ROM_CLKGATE_TO_ISOEN_CTRL)	00000002h
40500024h	4	RF And ROM Isolation Enable To Power Gate Count. (PMU_RF_ROM_ISOEN_TO_PWRGATE_CTRL)	00000002h
40500028h	4	RF And ROM Power Ungate To Isolation Disable Count (PMU_RF_ROM_PWRUNGATE_TO_ISODIS_CTRL)	00000002h
4050002Ch	4	RF And ROM Isolation Disable To Clock Gate Exit Count (PMU_RF_ROM_ISODIS_TO_CLKGATEEXIT_CTRL)	00000002h
40500030h	4	RF And ROM Power Gating Control (PMU_RF_ROM_PWR_CTRL)	00000000h
40500034h	4	SRAM Isolation Disable To Idle Count (PMU_SRAM_PWR_CTRL)	0F0F0F02h
4050003Ch	4	VNN Req Assert (PMU_VNN_REQ_31_0)	00000000h
40500040h	4	Vnn_req/Ack Live Status, Interrupts And Interrupt Masks Record (PMU_VNN_REQ_ACK)	00000000h
4050004Ch	4	Wake Mask-2 (PMU_ISH_MASK_EVENT2)	000FFC00h
40500054h	4	PGCB Clock Gating Control (PMU_PGCB_CLK_GATE_CTRL)	00000100h
40500058h	4	Vnnaon Reduction Enable (PMU_VNNAON_RED_EN)	00000000h
4050005Ch	4	Reset Prep (PMU_RESET_PREP_REG)	00000000h
40500060h	4	Fabric Idle Time Out Snapshot (PMU_FABRIC_SNAPSHOT_REG)	00000000h
40500064h	4	Context Propagation Enable (PMU_CP_EN_REG)	00000000h
40500068h	4	Clock Gating And Power Gating Status (PMU_CG_PG_STATUS_REG)	00000000h
4050006Ch	4	VNN Req Assert (PMU_VNN_REQ_63_32)	00000000h
40500070h	4	Host Wake (PMU_HOST_WAKEUP_0)	00000000h
40500074h	4	Host Wake (PMU_HOST_WAKEUP_1)	00000000h
40500078h	4	PME Status Clear Interrupt Mask (PMU_STATUS_CLR_INTR_MSK_0)	00000000h
4050007Ch	4	PME Status Clear Interrupt Mask (PMU_STATUS_CLR_INTR_MSK_1)	00000000h
40500080h	4	PME Status Clear Interrupt Status (PMU_PME_STATUS_CLR_INTR_STS_0)	00000000h
40500084h	4	PME Status Clear Interrupt Status (PMU_PME_STATUS_CLR_INTR_STS_1)	00000000h
40500088h	4	PME Live Status (PMC_STS_SHADOW_0)	00000000h
4050008Ch	4	PME Live Status (PMC_STS_SHADOW_1)	00000000h
40500100h	4	PCE ShadowFor PCI Function 0 (PCE_STATUS_0)	00000000h
40500104h	4	PCE ShadowFor PCI Function 1 (PCE_STATUS_1)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40500108h	4	PCE ShadowFor PCI Function 2 (PCE_STATUS_2)	00000000h
4050010Ch	4	PCE ShadowFor PCI Function 3 (PCE_STATUS_3)	00000000h
40500110h	4	PCE ShadowFor PCI Function 4 (PCE_STATUS_4)	00000000h
40500114h	4	PCE ShadowFor PCI Function 5 (PCE_STATUS_5)	00000000h
40500118h	4	PCE ShadowFor PCI Function 6 (PCE_STATUS_6)	00000000h
4050011Ch	4	PCE ShadowFor PCI Function 7 (PCE_STATUS_7)	00000000h
40500120h	4	PCE ShadowFor PCI Function 8 (PCE_STATUS_8)	00000000h
40500124h	4	PCE ShadowFor PCI Function 9 (PCE_STATUS_9)	00000000h
40500128h	4	PCE ShadowFor PCI Function 10 (PCE_STATUS_10)	00000000h
4050012Ch	4	PCE ShadowFor PCI Function 11 (PCE_STATUS_11)	00000000h
40500130h	4	PCE ShadowFor PCI Function 12 (PCE_STATUS_12)	00000000h
40500134h	4	PCE ShadowFor PCI Function 13 (PCE_STATUS_13)	00000000h
40500138h	4	PCE ShadowFor PCI Function 14 (PCE_STATUS_14)	00000000h
4050013Ch	4	PCE ShadowFor PCI Function 15 (PCE_STATUS_15)	00000000h
40500140h	4	PCE ShadowFor PCI Function 16 (PCE_STATUS_16)	00000000h
40500144h	4	PCE ShadowFor PCI Function 17 (PCE_STATUS_17)	00000000h
40500148h	4	PCE ShadowFor PCI Function 18 (PCE_STATUS_18)	00000000h
4050014Ch	4	PCE ShadowFor PCI Function 19 (PCE_STATUS_19)	00000000h
40500150h	4	PCE ShadowFor PCI Function 20 (PCE_STATUS_20)	00000000h
40500154h	4	PCE ShadowFor PCI Function 21 (PCE_STATUS_21)	00000000h
40500158h	4	PCE ShadowFor PCI Function 22 (PCE_STATUS_22)	00000000h
4050015Ch	4	PCE ShadowFor PCI Function 23 (PCE_STATUS_23)	00000000h
40500160h	4	PCE ShadowFor PCI Function 24 (PCE_STATUS_24)	00000000h
40500164h	4	PCE ShadowFor PCI Function 25 (PCE_STATUS_25)	00000000h
40500168h	4	PCE ShadowFor PCI Function 26 (PCE_STATUS_26)	00000000h
4050016Ch	4	PCE ShadowFor PCI Function 27 (PCE_STATUS_27)	00000000h
40500170h	4	PCE ShadowFor PCI Function 28 (PCE_STATUS_28)	00000000h
40500174h	4	PCE ShadowFor PCI Function 29 (PCE_STATUS_29)	00000000h
40500178h	4	PCE ShadowFor PCI Function 30 (PCE_STATUS_30)	00000000h
4050017Ch	4	PCE ShadowFor PCI Function 31 (PCE_STATUS_31)	00000000h
40500180h	4	PCE ShadowFor PCI Function 32 (PCE_STATUS_32)	00000000h
40500184h	4	PCE ShadowFor PCI Function 33 (PCE_STATUS_33)	00000000h
40500188h	4	PCE ShadowFor PCI Function 34 (PCE_STATUS_34)	00000000h
4050018Ch	4	PCE ShadowFor PCI Function 35 (PCE_STATUS_35)	00000000h
40500200h	4	Bridge D3 Rise Interrupt Wake Mask 0 (D3_RISE_INTR_MASK_REG_0)	00000000h
40500204h	4	Bridge D3 Rise Interrupt Wake Mask 1 (D3_RISE_INTR_MASK_REG_1)	00000000h
40500208h	4	Bridge D3 Fall Interrupt Wake Mask 0 (D3_FALL_INTR_MASK_REG_0)	00000000h
4050020Ch	4	Bridge D3 Fall Interrupt Wake Mask 1 (D3_FALL_INTR_MASK_REG_1)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40500210h	4	Bridge D3 Rise Interrupt Wake0 (D3_RISE_INTR_REG_31_0)	00000000h
40500214h	4	Bridge D3 Rise Interrupt Wake1 (D3_RISE_INTR_REG_35_32)	00000000h
40500218h	4	Bridge D3 Fall Interrupt Wake0 (D3_FALL_INTR_REG_31_0)	00000000h
4050021Ch	4	Bridge D3 Fall Interrupt Wake1 (D3_FALL_INTR_REG_35_32)	00000000h
40500220h	4	BME Rise Interrupt Wake Mask 0 (BME_RISE_INTR_MASK_REG_0)	00000000h
40500224h	4	BME Rise Interrupt Wake Mask 1 (BME_RISE_INTR_MASK_REG_1)	00000000h
40500228h	4	BME Fall Interrupt Wake Mask 0 (BME_FALL_INTR_MASK_REG_0)	00000000h
4050022Ch	4	BME Fall Interrupt Wake Mask 1 (BME_FALL_INTR_MASK_REG_1)	00000000h
40500230h	4	BME Rise Interrupt Wake0 (BME_RISE_INTR_REG_0)	00000000h
40500234h	4	BME Rise Interrupt Wake1 (BME_RISE_INTR_REG_1)	00000000h
40500238h	4	BME Fall Interrupt Wake0 (BME_FALL_INTR_REG_0)	00000000h
4050023Ch	4	BME Fall Interrupt Wake1 (BME_FALL_INTR_REG_1)	00000000h
40500240h	4	Bridge D3 Interrupt Wake Mask 0 (D3_INTR_MASK_REG_0)	00000000h
40500244h	4	Bridge D3 Interrupt Wake Mask 1 (D3_INTR_MASK_REG_1)	00000000h
40500248h	4	Bridge D3 Interrupt Wake0 (D3_INTR_REG_0)	00000000h
4050024Ch	4	Bridge D3 Interrupt Wake1 (D3_INTR_REG_1)	00000000h
40500250h	4	GPIO Wake Mask0 (GPIO_INTR_WK_MASK_REG_0)	00000000h
40500254h	4	GPIO Wake Mask1 (GPIO_INTR_WK_MASK_REG_1)	00000000h
40500258h	4	GPIO Wake Mask2 (GPIO_INTR_WK_MASK_REG_2)	00000000h
4050025Ch	4	GPIO Wake Mask3 (GPIO_INTR_WK_MASK_REG_3)	00000000h
40500270h	4	GPIO Wake Interrupt Record 0 (GPIO_INTR_REG_0)	00000000h
40500274h	4	GPIO Wake Interrupt Record 1 (GPIO_INTR_REG_1)	00000000h
40500278h	4	GPIO Wake Interrupt Record 2 (GPIO_INTR_REG_2)	00000000h
4050027Ch	4	GPIO Wake Interrupt Record 3 (GPIO_INTR_REG_3)	00000000h
40500290h	4	PWM And I2S Wake Interrupt (I2S_INTR_REG)	00000000h
40500294h	4	I2S Interrupt Mask (I2S_INTR_MASK_REG)	00000000h
40500298h	4	IETHERNET Wake Interrupt (ETHER_INTR_REG)	00000000h
4050029Ch	4	ETHERNET Interrupt Mask (ETHERNET_INTR_MASK_REG)	00000000h
405002A0h	4	QEP Wake Interrupt (QEP_INTR_REG)	00000000h
405002A4h	4	QEP Interrupt Mask (QEP_INTR_MASK_REG)	00000000h
405002A8h	4	PMU LART Update (ADR_LART_UPD_REG)	00000000h
405002ACh	4	ISH HOST DEV Interrupt (HOST_DEV_REG)	00000000h
405002B0h	4	PCI Interrupt0 (PCE_INTR_REG_0)	00000000h
405002B4h	4	PCI Interrupt1 (PCE_INTR_REG_1)	00000000h
405002B8h	4	D0I3 Interrupt0 (ADR_D0I3_INTR_0_REG)	00000000h
405002BCh	4	D0I3 Interrupt1 (ADR_D0I3_INTR_1_REG)	00000000h
405002C0h	4	XTAL Clk Reg (PMU_XTAL_CLK_REQ_REG)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
405002C4h	4	PMU CLKOCK SWITCH INTR (PMU_CLK_SWITCH_INTR)	00000000h
405002CCh	4	PMU VNNAON Metastability Fix Enable (PMU_VNNAON_METAFIX_EN_REG)	00000001h
405002D0h	4	PLL Power Up Sequence (PLL_PUSEQ_REG)	00020000h
405002D4h	4	PLL INTR (PLL_INT_REG)	098C6318h
405002D8h	4	ISH UART IDLE Mask (ADR_PMU_UART_IDLE_MASK_REG)	00000000h
405002DCh	4	PMU_TCG_EXIT_INTR_REG	00000000h
405002E0h	4	Address D3 Live Status0 (ADR_D3_STATUS_0_REG)	00000000h
405002E4h	4	Address D3 Live Status1 (ADR_D3_STATUS_1_REG)	00000000h
405002E8h	4	D0i3 Bit2 Status0 (ADR_D0I3_BIT2_STATUS_0_REG)	00000000h
405002ECh	4	D0i3 Bit2 Status1 (ADR_D0I3_BIT2_STATUS_1_REG)	00000000h
405002F0h	4	D0i3 Bit0 Status0 (ADR_D0I3_BIT0_STATUS_0_REG)	00000000h
405002F4h	4	D0i3 Bit0 Status1 (ADR_D0I3_BIT0_STATUS_1_REG)	00000000h
405002F8h	4	D0i3 Interrupt Mask 0 (ADR_D0I3C_INTR_STATUS_CLR_MSK_0_REG)	00000000h
405002FCh	4	D0i3 Interrupt Mask 1 (ADR_D0I3C_INTR_STATUS_CLR_MSK_1_REG)	00000000h
40500F00h	4	Power Status (PMU_PWR_ST_REG)	00000000h
40500F04h	4	IPAPG Scrath-Pad0 (IPAPG_SC_PAD0)	00000000h
40500F08h	4	IPAPG Scratch-Pad1 (IPAPG_SC_PAD1)	00000000h
40500F10h	4	IP Accessible PG Enable (IPAPG_EN_REG)	00000000h
40500F14h	4	SW PG REQ Interrupt (SW_PG_REQ_INTR)	00000018h
40500F18h	4	ISH PMC WAKE INTR (PMC_WAKE_INT_REG)	00000018h
40500F24h	4	ISH BRIDGEISOL CTL(Supported Only When There Is Sx Usage) (PMU_BRISOLCTL_REG)	00000030h
40500F28h	4	CDC Config Clock Gate Disable(Required Only During Sx Usage) (PMU_CDCCGDIS_REG)	00000000h
40500F30h	4	PCE ISH FW Local (PMU_PCE_LOCAL_REG)	00000200h
40500F34h	4	ISH SRAM Bitline Float Enable (ADR_SRAM_SLEEPB)	00000000h
40500F38h	4	ISH SRAM Array Sleep Enable (ADR_SRAM_ARSLEEP)	00000000h
40500F40h	4	IP In-Accessible PG Exit Status (IPIAPG_EN_REG)	00000000h

14.5.1.1 SRAM Bank Power Gate Enable (PMU_SRAM_PG_EN) — Offset 40500000h

Register for enabling power gating of SRAM banks.

Type	Size	Offset	Default
MMIO	32 bit	40500000h	03FFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	1h RW	**PG Enable For Bank 25 (SRAM_PG_EN_BANK25):** PG Enable/Disable for SRAM Bank 25. 1-Enable 0-Disable.
24	1h RW	**PG Enable For Bank 24 (SRAM_PG_EN_BANK24):** PG Enable/Disable for SRAM Bank 24. 1-Enable 0-Disable.
23	1h RW	**PG Enable For Bank 23 (SRAM_PG_EN_BANK23):** PG Enable/Disable for SRAM Bank 23. 1-Enable 0-Disable.
22	1h RW	**PG Enable For Bank 22 (SRAM_PG_EN_BANK22):** PG Enable/Disable for SRAM Bank 22. 1-Enable 0-Disable.
21	1h RW	**PG Enable For Bank 21 (SRAM_PG_EN_BANK21):** PG Enable/Disable for SRAM Bank 21. 1-Enable 0-Disable.
20	1h RW	**PG Enable For Bank 20 (SRAM_PG_EN_BANK20):** PG Enable/Disable for SRAM Bank 20. 1-Enable 0-Disable.
19	1h RW	**PG Enable For Bank 19 (SRAM_PG_EN_BANK19):** PG Enable/Disable for SRAM Bank 19. 1-Enable 0-Disable.
18	1h RW	**PG Enable For Bank 18 (SRAM_PG_EN_BANK18):** PG Enable/Disable for SRAM Bank 18. 1-Enable 0-Disable.
17	1h RW	**PG Enable For Bank 17 (SRAM_PG_EN_BANK17):** PG Enable/Disable for SRAM Bank 17. 1-Enable 0-Disable.
16	1h RW	**PG Enable For Bank 16 (SRAM_PG_EN_BANK16):** PG Enable/Disable for SRAM Bank 16. 1-Enable 0-Disable.
15	1h RW	**PG Enable For Bank 15 (SRAM_PG_EN_BANK15):** PG Enable/Disable for SRAM Bank 15. 1-Enable 0-Disable.
14	1h RW	**PG Enable For Bank 14 (SRAM_PG_EN_BANK14):** PG Enable/Disable for SRAM Bank 14. 1-Enable 0-Disable.
13	1h RW	**PG Enable For Bank 13 (SRAM_PG_EN_BANK13):** PG Enable/Disable for SRAM Bank 13. 1-Enable 0-Disable.
12	1h RW	**PG Enable For Bank 12 (SRAM_PG_EN_BANK12):** PG Enable/Disable for SRAM Bank 12. 1-Enable 0-Disable.
11	1h RW	**PG Enable For Bank 11 (SRAM_PG_EN_BANK11):** PG Enable/Disable for SRAM Bank 11. 1-Enable 0-Disable.
10	1h RW	**PG Enable For Bank 10 (SRAM_PG_EN_BANK10):** PG Enable/Disable for SRAM Bank 10. 1-Enable 0-Disable.
9	1h RW	**PG Enable For Bank 9 (SRAM_PG_EN_BANK9):** PG Enable/Disable for SRAM Bank 9. 1-Enable 0-Disable.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**PG Enable For Bank 8 (SRAM_PG_EN_BANK8):** PG Enable/Disable for SRAM Bank 8. 1-Enable 0-Disable.
7	1h RW	**PG Enable For Bank 7 (SRAM_PG_EN_BANK7):** PG Enable/Disable for SRAM Bank 7. 1-Enable 0-Disable.
6	1h RW	**PG Enable For Bank 6 (SRAM_PG_EN_BANK6):** PG Enable/Disable for SRAM Bank 6. 1-Enable 0-Disable.
5	1h RW	**PG Enable For Bank 5 (SRAM_PG_EN_BANK5):** PG Enable/Disable for SRAM Bank 5. 1-Enable 0-Disable.
4	1h RW	**PG Enable For Bank 4 (SRAM_PG_EN_BANK4):** PG Enable/Disable for SRAM Bank 4. 1-Enable 0-Disable.
3	1h RW	**PG Enable For Bank 3 (SRAM_PG_EN_BANK3):** PG Enable/Disable for SRAM Bank 3. 1-Enable 0-Disable.
2	1h RW	**PG Enable For Bank 2 (SRAM_PG_EN_BANK2):** PG Enable/Disable for SRAM Bank 2. 1-Enable 0-Disable.
1	1h RW	**PG Enable For Bank 1 (SRAM_PG_EN_BANK1):** PG Enable/Disable for SRAM Bank 1. 1-Enable 0-Disable.
0	1h RW	**PG Enable For Bank 0 (SRAM_PG_EN_BANK0):** PG Enable/Disable for SRAM Bank 0. 1-Enable 0-Disable.

14.5.1.2 Wake Mask-1 (PMU_ISH_MASK_EVENT) — Offset 40500010h

This register is used for masking a wake event to ensure clock gate exit.

Type	Size	Offset	Default
MMIO	32 bit	40500010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Vnn_ack Wake Fall Interrupt Mask (MASK_VNN_ACK_FALLING_WAKE_INTERRUPTS):** Mask VNN ACK falling wake interrupts 1-Mask wake from VNN ACK falling event 0-No mask for wake from VNN ACK falling event.
30	0h RW	**Vnn_ack Wake Rise Interrupt Mask (MASK_VNN_ACK_RISING_WAKE_INTERRUPTS):** Mask VNN ACK rising wake interrupts 1-Mask wake from VNN ACK rising event 0-No mask for wake from VNN ACK rising event.
29	0h RW	**D0i3 Wake Mask. (MASK_D0I3_WAKE_INTERRUPTS):** Mask D0I3 wake interrupts 1-Mask wake from D0I3 event 0-No mask for wake from D0I3 event.
28	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**SPI1 Wake Mask 1-Mask Wake From SPI1 Event 0-No Mask For Wake From SPI1 Event (MASK_SPI1_WAKE_INTERRUPTS):** Mask SPI1 wake interrupts 1-Mask wake from SPI1 event 0-No mask for wake from SPI1 event.
26	0h RW	**SBEP Wake Mask 1-Mask Wake From SBEP Event 0-No Mask For Wake From SBEP Event (MASK_SBEP_WAKE_INTERRUPTS):** Mask SBEP wake interrupts 1-Mask wake from SBEP event 0-No mask for wake from SBEP event.
25	0h RW	**I2C2 Wake Mask (MASK_I2C2_WAKE_INTERRUPTS):** Mask I2C2 wake interrupts 1-Mask wake from I2C2 event 0-No mask for wake from I2C2 event.
24	0h RO	**Reserved**
23	0h RW	**UART Wake Mask 1-Mask Wake From UART Event 0-No Mask For Wake From UART Event (MASK_UART_WAKE_INTERRUPTS):** Mask UART wake interrupts 1-Mask wake from UART event 0-No mask for wake from UART event.
22	0h RW	**SPI0 Wake Interrupts 1-Mask Wake From SPI0 Event 0-No Mask For Wake From SPI0 Event (MASK_SPI_WAKE_INTERUPTS):** Masks SPI wake interrupts 1-Mask Wake from SPI event 0-No mask for wake from SPI event.
21	0h RW	**I2C1 Wake Mask (MASK_I2C1_WAKE_INTERRUPTS):** Masks I2C1 wake interrupts 1-Mask Wake from I2C1 event 0-No mask for wake from I2C1 event.
20	0h RW	**I2C0 Wake Mask (MASK_I2C0_WAKE_INTERRUPTS):** Masks I2C0 wake interrupts 1-Mask Wake from I2C0 event 0-No mask for wake from I2C0 event.
19	0h RW	**DMA Wake Mask 1-Mask Wake From DMA Event 0-No Mask For Wake From DMA Event (MASK_DMA_WAKE_INTERRUPTS):** Masks DMA wake interrupts 1-Mask Wake from DMA event 0-No mask for wake from DMA event.
18	0h RO	**Reserved**
17	0h RW	**Host IPC Wake Mask 1-Mask Wake From IPC 0-No Mask For Wake From IPC (MASK_HOST_IPC_INTERRUPTS):** Masks Host IPC interrupts 1-Mask Wake from IPC 0-No mask for wake from IPC.
16	0h RW	**HPET Timer Wake Mask 1-Mask Wake From Timer Event 0-No Mask For Wake From Timer Event (MASK_TIMER_WAKE_INERRUPTS):** Masks Timer wake interrupts 1-Mask Wake from Timer event 0-No mask for wake from Timer event.
15:0	0h RO	**Reserved**

14.5.1.3 Fabric Idle And Time Out Count Configuration (PMU_ISH_FABRIC_CNT) — Offset 40500018h

This register stores the value of Idle count and time out count used by Func clock gate FSM during WAIT state to detect fabric idle condition and time out condition respectively.

Type	Size	Offset	Default
MMIO	32 bit	40500018h	3A980008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	3A98h RW	**Time Out Value For PMU Fabric Timeout Counter (PMU_FABRIC_TIMEOUT_CNT):** Timeout value for PMU Fabric timeout counter.
15:0	0008h RW	**Value For The Idle Counter 0 - 16 (PMU_FABRIC_IDLE_CNT):** Count value for the idle counter 0 - 16.

14.5.1.4 Glitch Bypass Enable (PMU_ISH_GLITCH_BYPASS) — Offset 4050001Ch

This register is used to enable/disable glitch bypass circuit inside the PM for all the GPIO input signals.

Type	Size	Offset	Default
MMIO	32 bit	4050001Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RW	**Glitch Bypass Enable Bit (GLITCH_BYPASS):** This bit is used to enable glitch filter logic in PMU. 0 Do not bypass glitch filter 1 Bypass Glitch filter.

14.5.1.5 RF And ROM Clock Gate To Isolation Enable Count. (PMU_RF_ROM_CLKGATE_TO_ISOEN_CTRL) — Offset 40500020h

This register is used by FW to program the count value for the number of clocks between CLKGATE state and ISOEN state in func clkgate fsm.

Type	Size	Offset	Default
MMIO	32 bit	40500020h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0002h RW	**ClkGate To ISOEN Count (CLKGATE_TO_ISOEN_COUNTER):** Count value for ClkGate to ISOEN state 0-16.

14.5.1.6 RF And ROM Isolation Enable To Power Gate Count. (PMU_RF_ROM_ISOEN_TO_PWRGATE_CTRL) — Offset 40500024h

This register is used by FW to program the count value for the number of clocks between ISOEN and PWRGATE state in func clkgate fsm.

Type	Size	Offset	Default
MMIO	32 bit	40500024h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0002h RW	**ISOEN To POWRGATE Count (ISOEN_TO_PWRGATE_COUNTER):** Count value for ISOEN to PWRGATE state 0-16.

14.5.1.7 RF And ROM Power Ungate To Isolation Disable Count (PMU_RF_ROM_PWRUNGATE_TO_ISODIS_CTRL) — Offset 40500028h

This register is used by FW to program the count value for the number of clocks between PWRUNGATE and ISODIS states of func clock gate FSM.

Type	Size	Offset	Default
MMIO	32 bit	40500028h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0002h RW	**PWRUNGATE To ISODIS Count (PWRUNGATE_TO_ISODIS_COUNTER):** Count value for PWRUNGATE to ISODIS state 0-16.

14.5.1.8 RF And ROM Isolation Disable To Clock Gate Exit Count (PMU_RF_ROM_ISODIS_TO_CLKGATEEXIT_CTRL) — Offset 4050002Ch

This register is used by FW to program the count value for the number of clocks between PWRUNGATE and ISODIS states of func clock gate FSM.

Type	Size	Offset	Default
MMIO	32 bit	4050002Ch	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0002h RW	**ISODIS To CLKGATEEXIT Count (ISODIS_TO_CLKGATEEXIT_COUNTER):** Count value for ISODIS to CLKGATEEXIT state 0-16.

14.5.1.9 RF And ROM Power Gating Control (PMU_RF_ROM_PWR_CTRL) — Offset 40500030h

This register is used by FW to enable power gating of RF (Cache and other IP RFs).

Type	Size	Offset	Default
MMIO	32 bit	40500030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**AON RF DeepsleepEnable 1-Enable AON_RF Deepsleep Mode 0-Disable AONRF Deepsleep Mode (AONRF_DEEPSLEEP_EN):** AONRF Deepsleep mode enable 1-AONRF enters deepsleep mode when firewall enable is high 0-AONRF deepsleep mode is disabled.
0	0h RW	**RF And ROM Power Gating Enable 1-RF ROM Power Gating Enable 0-RF ROM Power Gating Disable (RF_ROM_POWER_GATING_ENABLE):** RF ROM power gating enable 1-RF ROM power gating enable 0-RF ROM power gating disable.

14.5.1.10 SRAM Isolation Disable To Idle Count (PMU_SRAM_PWR_CTRL) — Offset 40500034h

This register is used by FW to program the count value for the number of clocks between ISODIS and IDLE states of SRAM PG FSM.

Type	Size	Offset	Default
MMIO	32 bit	40500034h	0F0F0F02h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:24	Fh RW	**SRAM ISODIS To IDLE Count (SRAM_ISODIS_TO_IDLE_COUNTER_):** Count value for SRAM ISODIS to IDLE state 0-3.
23:20	0h RO	**Reserved**
19:16	Fh RW	**SRAM POWERUNGATE To ISODIS Count (SRAM_POWERUNGATE_TO_ISODIS_COUNTER):** Count value for SRAM POWERUNGATE to ISODIS state 0-3.
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**SRAM POWERGATE To POWERUNGATE Count (SRAM_POWERGATE_TO_POWERUNGATE_COUNTER):** Count value for SRAM POWERGATE to POWERUNGATE state 0-3.
7:4	0h RO	**Reserved**
3:0	2h RW	**SRAM ISOEN To POWERGATE Count (SRAM_ISOEN_TO_POWERGATE_COUNTER):** Count value for SRAM ISOEN to POWERGATE state 0-3.

14.5.1.11 VNN Req Assert (PMU_VNN_REQ_31_0) — Offset 4050003Ch

This register is used by ISH FW to assert ish_pmc_vnn_req indication towards PMC.

Type	Size	Offset	Default
MMIO	32 bit	4050003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 31 (VNN_REQ_31_0_31):** Vnn_req bit31. 1-vnn_req set 0-vnn_req reset.
30	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 30 (VNN_REQ_31_0_30):** Vnn_req bit30. 1-vnn_req set 0-vnn_req reset.
29	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 29 (VNN_REQ_31_0_29):** Vnn_req bit29. 1-vnn_req set 0-vnn_req reset.
28	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 28 (VNN_REQ_31_0_28):** Vnn_req bit28. 1-vnn_req set 0-vnn_req reset.
27	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 27 (VNN_REQ_31_0_27):** Vnn_req bit27. 1-vnn_req set 0-vnn_req reset.
26	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 26 (VNN_REQ_31_0_26):** Vnn_req bit26. 1-vnn_req set 0-vnn_req reset.
25	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 25 (VNN_REQ_31_0_25):** Vnn_req bit25. 1-vnn_req set 0-vnn_req reset.
24	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 24 (VNN_REQ_31_0_24):** Vnn_req bit24. 1-vnn_req set 0-vnn_req reset.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 23 (VNN_REQ_31_0_23):** Vnn_req bit23. 1-vnn_req set 0-vnn_req reset.
22	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 22 (VNN_REQ_31_0_22):** Vnn_req bit22. 1-vnn_req set 0-vnn_req reset.
21	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 21 (VNN_REQ_31_0_21):** Vnn_req bit21. 1-vnn_req set 0-vnn_req reset.
20	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 20 (VNN_REQ_31_0_20):** Vnn_req bit20. 1-vnn_req set 0-vnn_req reset.
19	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 19 (VNN_REQ_31_0_19):** Vnn_req bit19. 1-vnn_req set 0-vnn_req reset.
18	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 18 (VNN_REQ_31_0_18):** Vnn_req bit18. 1-vnn_req set 0-vnn_req reset.
17	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 17 (VNN_REQ_31_0_17):** Vnn_req bit17. 1-vnn_req set 0-vnn_req reset.
16	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 16 (VNN_REQ_31_0_16):** Vnn_req bit16. 1-vnn_req set 0-vnn_req reset.
15	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 15 (VNN_REQ_31_0_15):** Vnn_req bit15. 1-vnn_req set 0-vnn_req reset.
14	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 14 (VNN_REQ_31_0_14):** Vnn_req bit14. 1-vnn_req set 0-vnn_req reset.
13	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 13 (VNN_REQ_31_0_13):** Vnn_req bit13. 1-vnn_req set 0-vnn_req reset.
12	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 12 (VNN_REQ_31_0_12):** Vnn_req bit12. 1-vnn_req set 0-vnn_req reset.
11	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 11 (VNN_REQ_31_0_11):** Vnn_req bit11. 1-vnn_req set 0-vnn_req reset.
10	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 10 (VNN_REQ_31_0_10):** Vnn_req bit10. 1-vnn_req set 0-vnn_req reset.
9	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 9 (VNN_REQ_31_0_9):** Vnn_req bit9. 1-vnn_req set 0-vnn_req reset.
8	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 8 (VNN_REQ_31_0_8):** Vnn_req bit8. 1-vnn_req set 0-vnn_req reset.
7	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 7 (VNN_REQ_31_0_7):** Vnn_req bit7. 1-vnn_req set 0-vnn_req reset.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 6 (VNN_REQ_31_0_6):** Vnn_req bit6. 1-vnn_req set 0-vnn_req reset.
5	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 5 (VNN_REQ_31_0_5):** Vnn_req bit5. 1-vnn_req set 0-vnn_req reset.
4	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 4 (VNN_REQ_31_0_4):** Vnn_req bit4. 1-vnn_req set 0-vnn_req reset.
3	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 3 (VNN_REQ_31_0_3):** Vnn_req bit3. 1-vnn_req set 0-vnn_req reset.
2	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 2 (VNN_REQ_31_0_2):** Vnn_req bit2. 1-vnn_req set 0-vnn_req reset.
1	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 1 (VNN_REQ_31_0_1):** Vnn_req bit1. 1-vnn_req set 0-vnn_req reset.
0	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 0 (VNN_REQ_31_0_0):** Vnn_req bit0. 1-vnn_req set 0-vnn_req reset.

14.5.1.12 Vnn_req/Ack Live Status, Interrupts And Interrupt Masks Record (PMU_VNN_REQ_ACK) — Offset 40500040h

This register records the vnn_ack live status, rise and fall edge interrupts along with the req & ack status. The associated interrupt masks that are to be programmed by the ISH FW is also part of this register.

Type	Size	Offset	Default
MMIO	32 bit	40500040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Interrupt Mask For Vnn_ack Fall Interrupt (VNN_ACK_FALLING_EDGE_INTERRUPT_MASK):** Masks vnn_ack fall interrupt 1-mask vnn_ack fall interrupt 0-No mask for vnn_ack fall interrupt.
4	0h RW	**Interrupt Mask For Vnn_ack Rise Interrupt (VNN_ACK_RISING_EDGE_INTERRUPT_MASK):** Masks vnn_ack rise interrupts 1-Mask vnn_ack rise interrupt 0-No mask for vnn_ack fall interrupt.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**Interrupt Status For Vnn_ack Fall Interrupt (VNN_ACK_FALLING_EDGE_INTERRUPT_):** Vnn_ack fall interrupt status. 1-vnn_ack fall interrupt 0-No vnn_ack fall interrupt.
2	0h RW/1C	**Interrupt Status For Vnn_ack Rise Interrupt (VNN_ACK_RISING_EDGE_INTERRUPT_):** Vnn_ack rise interrupt status. 1-vnn_ack rise interrupt 0-No vnn_ack rise interrupt.
1	0h RO	**Vnn_ack Live Status (VNN_ACK_STATUS):** Vnn_ack live status. 1-vnn_ack set 0-vnn_ack cleared.
0	0h RO	**Vnn_req_ack Status (VNN_REQ_ACK_STATUS):** Vnn_req & vnn_ack Status 1- vnn_req & vnn_ack Set 0-vnn_req OR vnn_ack RESET.

14.5.1.13 Wake Mask-2 (PMU_ISH_MASK_EVENT2) — Offset 4050004Ch

This register is used for masking a wake event to ensure clock gate exit.

Type	Size	Offset	Default
MMIO	32 bit	4050004Ch	000FFC00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**PMU I2C7 Mask 1-Mask Wake From I2C7 Event 0-No Mask For Wake From I2C7 Event (PMU_I2C7_WK_MASK):** Masks I2C7 wake interrupts 1-Mask Wake from I2C7 event 0-No mask for wake from I2C7 event.
29	0h RW	**PMU I2C6 Mask 1-Mask Wake From I2C6 Event 0-No Mask For Wake From I2C6 Event (PMU_I2C6_WK_MASK):** Masks I2C6 wake interrupts 1-Mask Wake from I2C6 event 0-No mask for wake from I2C6 event.
28	0h RW	**I3C Wake Mask 1-Mask Wake From I3C Event 0-No Mask For Wake From I3C Event (MASK_I3C_WAKE_INTERRUPTS):** Masks I3C wake interrupts 1-Mask Wake from I3C event 0-No mask for wake from I3C event.
27	0h RW	**DMA2 Wake Mask 1-Mask Wake From DMA2 Event 0-No Mask For Wake From DMA2 Event (MASK_DMA2_WAKE_INTERRUPTS):** Masks DMA2 wake interrupts 1-Mask Wake from DMA2 event 0-No mask for wake from DMA2 event.
26	0h RW	**DMA1 Wake Mask 1-Mask Wake From DMA1 Event 0-No Mask For Wake From DMA1 Event (MASK_DMA1_WAKE_INTERRUPTS):** Masks DMA1 wake interrupts 1-Mask Wake from DMA1 event 0-No mask for wake from DMA1 event.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**SPI3 Wake Interrupts 1-Mask Wake From SPI3 Event 0-No Mask For Wake From SPI3 Event (MASK_SPI3_WAKE_INTERUPTS):** Masks SPI3 wake interrupts 1-Mask Wake from SPI3 event 0-No mask for wake from SPI3 event.
24	0h RW	**SPI2 Wake Interrupts 1-Mask Wake From SPI2 Event 0-No Mask For Wake From SPI2 Event (MASK_SPI2_WAKE_INTERUPTS):** Masks SPI2 wake interrupts 1-Mask Wake from SPI2 event 0-No mask for wake from SPI2 event.
23	0h RW	**I2C1 Wake Mask (MASK_I2C5_WAKE_INTERRUPTS):** Masks I2C1 wake interrupts 1-Mask Wake from I2C1 event 0-No mask for wake from I2C1 event.
22	0h RW	**I2C1 Wake Mask (MASK_I2C4_WAKE_INTERRUPTS):** Masks I2C1 wake interrupts 1-Mask Wake from I2C1 event 0-No mask for wake from I2C1 event.
21	0h RW	**I2C3 Wake Mask (MASK_I2C3_WAKE_INTERRUPTS):** Masks I2C3 wake interrupts 1-Mask Wake from I2C3 event 0-No mask for wake from I2C3 event.
20	0h RW	**Reset Warn Rise Wake Mask (RST_WARN_RISE_WK_MASK):** When set this bit will mask wake from spcu_ish_reset_warn rise event.
19	1h RW	**PME_STATUS_CLR_INTR Wake Mask Bit (PMU_PME_STATUS_CLR_INTR_WK_MSK):** When set this bit will mask wake from PME_STATUS_CLR_INTR.
18	1h RW	**PCE_CHG_DETECT_INTR Wake Mask Bit (PMU_PCE_CHG_DETECT_INTR_WK_MSK):** When set this bit will mask wake from PCE_CHG_DETECT_INTR.
17	1h RW	**HOST_RSTB_WIRE_FALL Wake Mask Bit (PMU_HOST_RSTB_WIRE_FALL_WK_MSK):** When set this bit will mask wake from HOST_RSTB_WIRE_FALL interrupt.
16	1h RW	**HOST_RSTB_WIRE_RISE Wake Mask Bit (PMU_HOST_RSTB_WIRE_RISE_WK_MSK):** When set this bit will mask wake from HOST_RSTB_WIRE_RISE.
15	1h RW	**BR_ISOL_ACK_FALL Wake Mask Bit (PMU_BR_ISOL_ACK_FALL_WK_MSK):** When set this bit will mask wake from BR_ISOL_ACK_FALL interrupt.
14	1h RW	**BR_ISOL_ACK_RISE Wake Mask Bit (PMU_BR_ISOL_ACK_RISE_WK_MSK):** When set this bit will mask wake from BR_ISOL_ACK_RISE interrupt.
13	1h RW	**PMC_PG_WAKE_FALL Wake Mask Bit (PMU_PG_WAKE_FALL_WK_MSK):** When set this bit will mask wake from PMC_PG_WAKE_FALL interrupt.
12	1h RW	**PMC_PG_WAKE_RISE Wake Mask Bit (PMU_PG_WAKE_RISE_WK_MSK):** When set this bit will mask wake from PMC_PG_WAKE_RISE interrupt.
11	1h RW	**PG_REQ_B_FALL Wake Mask Bit (PMU_SW_PG_REQ_B_FALL_WK_MSK):** When set this bit will mask wake from SW_PG_REQ_B_FALL interrupt.
10	1h RW	**PG_REQ_B_RISE Wake Mask Bit (PMU_SW_PG_REQ_B_RISE_WK_MSK):** When set this bit will mask wake from SW_PG_REQ_B_RISE interrupt.
9	0h RW	**XPRSN Wake Mask Bit (PMU_XPRSN_WK_MSK___):** When set this bit will mask wake from XPRSN indication.
8:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**RESET Prep Wake Mask (MASK_RESET_PREP_AVAIL_WAKE_INTERRUPT):** Mask reset prep avail interrupts 1-Mask wake from reset prep avail event 0-No mask for wake from reset prep avail event.
4	0h RW	**Sram Erase Wake Mask (MASK_SRAM_ERASE_WAKE_INTERRUPT_0):** Mask sram erase interrupts 1-Mask wake from sram erase event 0-No mask for wake from sram erase event.
3:0	0h RO	**Reserved**

14.5.1.14 PGCB Clock Gating Control (PMU_PGCB_CLK_GATE_CTRL) — Offset 40500054h

This register is used by FW to program the IP-accessible clock gating disable as well as the count value for the T_CLKGATE hysterisis timer for the PGCB clock.

Type	Size	Offset	Default
MMIO	32 bit	40500054h	00000100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	1h RW	**Accessible Clock Gate Disable Bit For PGCB Clock (ACC_CLKGATE_DISABLED):** This bit is a disable for clock gating PGCB clock during IP-accessible flow. 1-ClkGating disabled for Acc. flow 0-ClkGating enabled for Acc. Flow.
7:4	0h RO	**Reserved**
3:0	0h RW	**T_CLKGATE Count Value (T_CLKGATE_TIMER_VALUE):** Count value for T_CLKGATE state 0-16. This is used to load the hysterisis timer in the PCGU.

14.5.1.15 Vnnaon Reduction Enable (PMU_VNNAON_RED_EN) — Offset 40500058h

This register is used to enable the vnnaon reduction handshake by the AON clock gate FSM.

Type	Size	Offset	Default
MMIO	32 bit	40500058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/AC	**VNNAON Reduction Enable (VNNAON_RED_EN):** This bit is used to enable VNNAON reduction feature. 1-VNNAON reduction enable 0-VNNAON reduction disable.

14.5.1.16 Reset Prep (PMU_RESET_PREP_REG) — Offset 4050005Ch

This register records the Reset Prep avail and the other associated messages for Reset Prep.

Type	Size	Offset	Default
MMIO	32 bit	4050005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Prep Avail Mask 1- Mask Reset Prep Avail Interrupt 0-Reset Prep Avail Interrupt Not Masked. (RESET_PREP_AVAIL_MASK):** Reset Prep Avail Mask 1- mask reset prep avail interrupt 0-reset prep avail interrupt not masked.
30:18	0000h RO	**RSV:** Reserved
17:10	00h RO	**PREP_TYPE:** Prep Type.
9:2	00h RO	**RESET_TYPE:** Reset Type.
1	0h RO	**RESET_PREP_AVAIL:** Reset Prep Avail status.
0	0h RW/AC	**Prep Get 1- Reset Prep Message Read 0-Reset Prep Message Not Read (RESET_PREP_GET):** Reset Prep Get 1- reset prep message read 0-reset prep message not read.

14.5.1.17 Fabric Idle Time Out Snapshot (PMU_FABRIC_SNAPSHOT_REG) — Offset 40500060h

This register indicates the snap shot of the idle indications when the fabric time out counter expires. This register indicates the cause for the ISH HW to fail enter D0ix state. Note that this is an interrupt cause vector for a PMU wake. This means that PMU Wake Handler must read this register on every wake event. This is used for debug purposes only, as this is to be never set, in good operational conditions.

Type	Size	Offset	Default
MMIO	32 bit	40500060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C	**HPET Write InProgress Snapshot (PMU_HPET_WR_INPROGRESS_SNAPSHOT):** This bit tis the snap shot of the HPET_REG_WR_InProgress signal from the HPET when Fabric time out counter expires.
4	0h RW/1C	**UART HSU Active Snapshot (PMU_HSU_ACTIVE_SNAPSHOT):** This bit tis the snap shot of !hsu_idle signal when Fabric time out counter expires.
3	0h RW/1C	**OCP Fabric Active Snapshot (PMU_FABRIC_ACTIVE_SNAPSHOT):** This bit tis the snap shot of the OR of all the pm_active_o inications from the OCP fabric when Fabric time out counter expires.
2	0h RW/1C	**Bridge OCP Active Snapshot (PMU_BR_OCP_ACTIVE_SNAPSHOT):** This bit tis the snap shot of !iosf2ocp_idle signal when Fabric time out counter expires.
1	0h RW/1C	**Bridge Side Active Snapshot (PMU_BR_SIDE_ACTIVE_SNAPSHOT):** This bit tis the snap shot of !iosf2ocp_sb_idle_funcclk_sync signal when Fabric time out counter expires.
0	0h RW/1C	**Bridge Prim Active Snapshot (PMU_BR_PRIM_ACTIVE_SNAPSHOT):** This bit tis the snap shot of PwrActive_funcclk_sync (!iosf2ocp_pr_idle_funcclk_sync in chassis compliant SOCs) signal when Fabric time out counter expires.

14.5.1.18 Context Propagation Enable (PMU_CP_EN_REG) — Offset 40500064h

Context Propagation Enable Register. This register can be programmed by ISH FW to enable forcing the clock for context propagation during IP accessible exit.

Type	Size	Offset	Default
MMIO	32 bit	40500064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**RSV:** Reserved
0	0h RW	**Force Clock For Context Propagation Enable (PMU_CP_EN):** This bit is routed to the SHIM module for forcing clocks to allow for context propagation during IP accessible PG exit. When this bit is set, the force clocks for context propagation will be enabled.

14.5.1.19 Clock Gating And Power Gating Status (PMU_CG_PG_STATUS_REG) — Offset 40500068h

This register indicates the clock gating and power gating progress and status (PCR 1503884648). This can be used by FW to ensure that the clock gating and the power gating has happened as expected and specific states have been reached during the clock gating and power gating entry. FW is expected to clear this register after every exit to ensure the correct status is getting recorded during the next clock gate/power gate entry.

Type	Size	Offset	Default
MMIO	32 bit	40500068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	00000h RO	**RSV:** Reserved
12	0h RW/1C	**Successful AON Clk Gating Entry Achieved (PMU_AONCG_ENTRY_STATUS):** This bit is set as soon as the AON clkreq fsm enters clk_deassert state. Note: This bit will get set only after the exit happens as the functional clock is not running at the time the aon clk gating happens.
11	0h RW/1C	**Successful PowerGate Entry Achieved (PMU_PG_ENTRY_STATUS):** This bit is set as soon as the pg_ack from the PMC is asserted. Note: This bit will get set only after the exit happens as the functional clock is not running at the time the pg_ack from PMC gets asserted. Note: When this bit is set, both the logic and the memories (RF cache and ROM) are guaranteed to be power gated during IP accessible PG.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**Successful PowerGate Ready Achieved For SBEP Side Clock Domain (PMU_PGREADY_SBEP_ENTRY_STATUS):** This bit is set as soon as CDC for Prim domain was able to enter assert the pwrgate_ready indication to the PGCB. Note: This bit may get set only after the exit happens as the functional clock is not running at the time the Prim CDC is asserting the PwrgateReady.
9	0h RW/1C	**Successful PowerGate Ready Achieved For Bridge Side Clock Domain (PMU_PGREADY_BRSIDE_ENTRY_STATUS):** This bit is set as soon as CDC for bridge side clock domain was able to enter assert the pwrgate_ready indication to the PGCB. Note: This bit may get set only after the exit happens as the functional clock may not be running at the time the bridge side CDC is asserting the PwrgateReady.
8	0h RW/1C	**Successful PowerGate Ready Achieved For Bridge Primary Clock Domain (PMU_PGREADY_BRPRIM_ENTRY_STATUS):** This bit is set as soon as CDC for bridge primary clock domain was able to enter assert the pwrgate_ready indication to the PGCB. Note: This bit may get set only after the exit happens as the functional clock may not be running at the time the Primary domain CDC is asserting the PwrgateReady.
7	0h RW/1C	**Successful PowerGate Ready Achieved For Functional Clock Domain (PMU_PGREADY_FUNC_ENTRY_STATUS):** This bit is set as soon as CDC for functional clock domain was able to enter assert the pwrgate_ready indication to the PGCB. Note: This bit will get set only after the exit happens as the functional clock is not running at the time the functional CDC is asserting the PwrgateReady.
6	0h RW/1C	**Successful PowerGate Ready Achieved For MIA Clock Domain (PMU_PGREADY_MIA_ENTRY_STATUS):** This bit is set as soon as CDC for MIA clock domain was able to enter assert the pwrgate_ready indication to the PGCB. Note: This bit will get set only after the exit happens as the MIA clock is not running at the time the MIA CDC is asserting the PwrgateReady.
5	0h RW/1C	**Successful PowerGate Ready Achieved For Xtal Clock Domain (PMU_PGREADY_XTAL_ENTRY_STATUS):** This bit is set as soon as CDC for xtal clock domain was able to enter assert the pwrgate_ready indication to the PGCB. Note: This bit will get set only after the exit happens as the xtal clock is not running at the time the xtal CDC is asserting the PwrgateReady.
4	0h RW/1C	**Successful Vnnaon Active Deassertion Entry Achieved (PMU_VNNAON_ACT_DEASRT_ENTRY_STATUS):** This bit is set as soon as FSM2 was able to enter Vnnaon_Deassert state. Note: This bit will get set only after the exit happens as the functional clock is not running when the FSM2 enters Vnnaon_Deassert state.
3	0h RW/1C	**Successful Trunk Clock Gate Entry Achieved (PMU_TCG_ENTRY_STATUS):** This bit is set as soon as FSM2 was able to enter Clkreq_Deassert state. Note: This bit will get set only after the exit happens as the functional clock is not running when the FSM2 enters clkreq_Deassert state.
2	0h RW/1C	**Successful RF And ROM ONLY Power Gate Entry Achieved (PMU_RF_ROM_PG_ENTRY_STATUS):** This bit is set as soon as FSM1 was able to enter PowerGate state and hence when the RF and ROM only are power gated by FSM1. Note: This big does not get set when the RF and ROM are power gated by the SHIM during IP accessible PG entry.
1	0h RW/1C	**Clock Gating Abort Condition (PMU_CG_ABORT_STATUS):** This bit is set only when FSM 1 moved from WAIT => IDLE state.
0	0h RW/1C	**Successful Minute IA CG ONLY State Entry Achieved (PMU_MIA_CG_ENTRY_STATUS):** This bit indicates that the FSM 1 was able to enter Minute IA CG state and hence when Minute IA alone is clock gated. Note: This bit does not get set during TCG entry and IP accessible PG even though the Minute IA clock is expected to be gated during these states.

14.5.1.20 VNN Req Assert (PMU_VNN_REQ_63_32) — Offset 4050006Ch

This register is used by ISH FW to assert ish_pmc_vnn_req indication towards PMC.

Type	Size	Offset	Default
MMIO	32 bit	4050006Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 63 (VNN_REQ_63_32_31):** Vnn_req bit63. 1-vnn_req set 0-vnn_req reset.
30	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 62 (VNN_REQ_63_32_30):** Vnn_req bit62. 1-vnn_req set 0-vnn_req reset.
29	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 61 (VNN_REQ_63_32_29):** Vnn_req bit61. 1-vnn_req set 0-vnn_req reset.
28	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 60 (VNN_REQ_63_32_28):** Vnn_req bit60. 1-vnn_req set 0-vnn_req reset.
27	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 59 (VNN_REQ_63_32_27):** Vnn_req bit59. 1-vnn_req set 0-vnn_req reset.
26	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 58 (VNN_REQ_63_32_26):** Vnn_req bit58. 1-vnn_req set 0-vnn_req reset.
25	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 57 (VNN_REQ_63_32_25):** Vnn_req bit57. 1-vnn_req set 0-vnn_req reset.
24	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 56 (VNN_REQ_63_32_24):** Vnn_req bit56. 1-vnn_req set 0-vnn_req reset.
23	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 55 (VNN_REQ_63_32_23):** Vnn_req bit55. 1-vnn_req set 0-vnn_req reset.
22	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 54 (VNN_REQ_63_32_22):** Vnn_req bit54. 1-vnn_req set 0-vnn_req reset.
21	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 53 (VNN_REQ_63_32_21):** Vnn_req bit53. 1-vnn_req set 0-vnn_req reset.
20	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 52 (VNN_REQ_63_32_20):** Vnn_req bit52. 1-vnn_req set 0-vnn_req reset.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 51 (VNN_REQ_63_32_19):** Vnn_req bit51. 1-vnn_req set 0-vnn_req reset.
18	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 50 (VNN_REQ_63_32_18):** Vnn_req bit50. 1-vnn_req set 0-vnn_req reset.
17	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 49 (VNN_REQ_63_32_17):** Vnn_req bit49. 1-vnn_req set 0-vnn_req reset.
16	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 48 (VNN_REQ_63_32_16):** Vnn_req bit48. 1-vnn_req set 0-vnn_req reset.
15	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 47 (VNN_REQ_63_32_15):** Vnn_req bit47. 1-vnn_req set 0-vnn_req reset.
14	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 46 (VNN_REQ_63_32_14):** Vnn_req bit46. 1-vnn_req set 0-vnn_req reset.
13	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 45 (VNN_REQ_63_32_13):** Vnn_req bit45. 1-vnn_req set 0-vnn_req reset.
12	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 44 (VNN_REQ_63_32_12):** Vnn_req bit44. 1-vnn_req set 0-vnn_req reset.
11	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 43 (VNN_REQ_63_32_11):** Vnn_req bit43. 1-vnn_req set 0-vnn_req reset.
10	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 42 (VNN_REQ_63_32_10):** Vnn_req bit42. 1-vnn_req set 0-vnn_req reset.
9	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 41 (VNN_REQ_63_32_9):** Vnn_req bit41. 1-vnn_req set 0-vnn_req reset.
8	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 40 (VNN_REQ_63_32_8):** Vnn_req bit 40. 1-vnn_req set 0-vnn_req reset.
7	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 39 (VNN_REQ_63_32_7):** Vnn_req bit39. 1-vnn_req set 0-vnn_req reset.
6	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 38 (VNN_REQ_63_32_6):** Vnn_req bit38. 1-vnn_req set 0-vnn_req reset.
5	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 37 (VNN_REQ_63_32_5):** Vnn_req bit37. 1-vnn_req set 0-vnn_req reset.
4	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 36 (VNN_REQ_63_32_4):** Vnn_req bit36. 1-vnn_req set 0-vnn_req reset.
3	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 35 (VNN_REQ_63_32_3):** Vnn_req bit35. 1-vnn_req set 0-vnn_req reset.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 34 (VNN_REQ_63_32_2):** Vnn_req bit34. 1-vnn_req set 0-vnn_req reset.
1	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 33 (VNN_REQ_63_32_1):** Vnn_req bit33. 1-vnn_req set 0-vnn_req reset.
0	0h RW/1S/ 1C/V	**Vnn_req Assert Bit 32 (VNN_REQ_63_32_0):** Vnn_req bit 32. 1-vnn_req set 0-vnn_req reset.

14.5.1.21 Host Wake (PMU_HOST_WAKEUP_0) — Offset 40500070h

This register us used for PME assertion.

Type	Size	Offset	Default
MMIO	32 bit	40500070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**OOB_PME Assert Bit (OOB_PME_0):** Used to assert the oob PME signal. 1-Assert oob_pme_b signal 0-De-assert oob_pme_b signal.

14.5.1.22 Host Wake (PMU_HOST_WAKEUP_1) — Offset 40500074h

This register us used for PME assertion.

Type	Size	Offset	Default
MMIO	32 bit	40500074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/V	**OOB_PME Assert Bit (OOB_PME_1):** Used to assert the oob PME signal. 1-Assert oob_pme_b signal 0-De-assert oob_pme_b signal.

14.5.1.23 PME Status Clear Interrupt Mask (PMU_STATUS_CLR_INTR_MSK_0) — Offset 40500078h

This register is used for recording the PME status interrupt mask.

Type	Size	Offset	Default
MMIO	32 bit	40500078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PME Status Clear Interrupt Mask Register (PMU_PME_STATUS_CLR_INTR_MSK_0):** This is the mask bit for PME status clear interrupt. 1- Mask the PME Status clear interrupt, 0 - Unmask PME status clear interrupt.

14.5.1.24 PME Status Clear Interrupt Mask (PMU_STATUS_CLR_INTR_MSK_1) — Offset 4050007Ch

This register is used for recording the PME status interrupt mask.

Type	Size	Offset	Default
MMIO	32 bit	4050007Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**PME Status Clear Interrupt Mask Register (PMU_PME_STATUS_CLR_INTR_MSK_1):** This is the mask bit for PME status clear interrupt. 1- Mask the PME Status clear interrupt, 0 - Unmask PME status clear interrupt.

14.5.1.25 PME Status Clear Interrupt Status (PMU_PME_STATUS_CLR_INTR_STS_0) — Offset 40500080h

This register is used for recording the PMEinterrupt status.

Type	Size	Offset	Default
MMIO	32 bit	40500080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**PME Status Clear Interrupt Status Register (PMU_PME_STATUS_CLR_INTR_STS_0):** This is the interrupt status bit for PME status clear interrupt. 1- PME status clear interrupt is set. 0 - PME status clear interrupt is cleared.

14.5.1.26 PME Status Clear Interrupt Status (PMU_PME_STATUS_CLR_INTR_STS_1) — Offset 40500084h

This register is used for recording the PMEinterrupt status.

Type	Size	Offset	Default
MMIO	32 bit	40500084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**PME Status Clear Interrupt Status Register (PMU_PME_STATUS_CLR_INTR_STS_1):** This is the interrupt status bit for PME status clear interrupt. 1- PME status clear interrupt is set. 0 - PME status clear interrupt is cleared.

14.5.1.27 PME Live Status (PMC_STS_SHADOW_0) — Offset 40500088h

This register is used to record the lie status of PME.

Type	Size	Offset	Default
MMIO	32 bit	40500088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**PME_STS Live Status Bit (PMC_STS_SHADOW_0):** This is the live status of the PME_STS bit in PCI configuration register in IOSF2OCP Bridge.

14.5.1.28 PME Live Status (PMC_STS_SHADOW_1) — Offset 4050008Ch

This register is used to record the lie status of PME.

Type	Size	Offset	Default
MMIO	32 bit	4050008Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**PME_STS Live Status Bit (PMC_STS_SHADOW_1):** This is the live status of the PME_STS bit in PCI configuration register in IOSF2OCP Bridge.

14.5.1.29 PCE ShadowFor PCI Function 0 (PCE_STATUS_0) — Offset 40500100h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.30 PCE ShadowFor PCI Function 1 (PCE_STATUS_1) — Offset 40500104h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_1):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_1):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_1):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_1):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_1):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_1):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_1):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_1):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_1):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_1):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_1):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_1):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_1):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_1):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_1):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_1):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_1):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_1):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_1):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_1):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_1):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_1):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_1):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.31 PCE ShadowFor PCI Function 2 (PCE_STATUS_2) — Offset 40500108h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_2):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_2):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_2):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_2):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_2):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_2):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_2):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_2):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_2):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_2):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_2):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_2):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_2):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_2):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_2):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_2):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_2):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_2):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_2):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_2):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_2):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_2):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_2):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.32 PCE ShadowFor PCI Function 3 (PCE_STATUS_3) — Offset 4050010Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050010Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_3):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_3):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_3):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_3):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_3):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_3):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_3):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_3):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_3):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_3):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_3):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_3):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_3):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_3):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_3):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_3):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_3):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_3):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_3):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_3):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_3):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_3):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_3):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.33 PCE ShadowFor PCI Function 4 (PCE_STATUS_4) — Offset 40500110h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_4):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_4):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_4):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_4):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_4):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_4):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_4):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_4):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_4):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_4):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_4):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_4):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_4):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_4):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_4):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_4):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_4):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_4):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_4):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_4):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_4):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_4):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_4):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.34 PCE ShadowFor PCI Function 5 (PCE_STATUS_5) — Offset 40500114h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_5):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_5):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_5):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_5):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_5):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_5):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_5):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_5):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_5):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_5):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_5):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_5):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_5):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_5):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_5):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_5):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_5):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_5):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_5):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_5):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_5):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_5):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_5):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.35 PCE ShadowFor PCI Function 6 (PCE_STATUS_6) — Offset 40500118h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_6):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_6):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_6):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_6):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_6):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_6):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_6):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_6):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_6):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_6):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_6):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_6):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_6):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_6):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_6):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_6):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_6):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_6):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_6):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_6):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_6):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_6):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_6):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.36 PCE ShadowFor PCI Function 7 (PCE_STATUS_7) — Offset 4050011Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050011Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_7):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_7):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_7):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_7):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_7):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_7):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_7):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_7):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_7):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_7):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_7):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_7):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_7):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_7):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_7):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_7):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_7):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_7):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_7):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_7):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_7):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_7):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_7):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.37 PCE ShadowFor PCI Function 8 (PCE_STATUS_8) — Offset 40500120h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_8):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_8):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_8):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_8):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_8):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_8):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_8):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_8):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_8):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_8):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_8):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_8):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_8):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_8):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_8):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_8):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_8):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_8):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_8):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_8):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_8):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_8):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_8):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.38 PCE ShadowFor PCI Function 9 (PCE_STATUS_9) — Offset 40500124h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_9):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_9):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_9):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_9):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_9):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_9):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_9):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_9):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_9):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_9):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_9):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_9):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_9):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_9):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_9):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_9):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_9):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_9):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_9):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_9):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_9):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_9):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_9):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.39 PCE ShadowFor PCI Function 10 (PCE_STATUS_10) — Offset 40500128h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_10):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_10):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_10):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_10):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_10):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_10):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_10):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_10):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_10):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_10):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_10):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_10):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_10):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_10):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_10):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_10):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_10):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_10):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_10):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_10):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_10):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_10):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_10):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.40 PCE ShadowFor PCI Function 11 (PCE_STATUS_11) — Offset 4050012Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050012Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_11):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_11):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_11):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_11):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_11):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_11):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_11):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_11):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_11):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_11):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_11):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_11):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_11):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_11):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_11):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_11):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_11):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_11):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_11):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_11):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_11):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_11):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_11):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.41 PCE ShadowFor PCI Function 12 (PCE_STATUS_12) — Offset 40500130h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_12):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_12):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_12):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_12):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_12):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_12):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_12):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_12):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_12):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_12):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_12):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_12):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_12):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_12):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_12):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_12):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_12):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_12):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_12):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_12):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_12):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_12):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_12):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.42 PCE ShadowFor PCI Function 13 (PCE_STATUS_13) — Offset 40500134h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_13):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_13):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_13):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_13):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_13):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_13):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_13):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_13):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_13):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_13):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_13):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_13):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_13):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_13):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_13):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_13):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_13):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_13):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_13):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_13):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_13):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_13):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_13):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.43 PCE ShadowFor PCI Function 14 (PCE_STATUS_14) — Offset 40500138h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500138h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_14):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_14):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_14):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_14):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_14):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_14):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_14):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_14):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_14):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_14):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_14):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_14):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_14):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_14):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_14):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_14):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_14):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_14):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_14):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_14):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_14):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_14):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_14):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.44 PCE ShadowFor PCI Function 15 (PCE_STATUS_15) — Offset 4050013Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050013Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_15):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_15):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_15):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_15):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_15):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_15):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_15):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_15):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_15):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_15):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_15):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_15):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_15):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_15):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_15):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_15):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_15):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_15):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_15):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_15):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_15):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_15):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_15):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.45 PCE ShadowFor PCI Function 16 (PCE_STATUS_16) — Offset 40500140h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_16):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_16):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_16):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_16):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_16):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_16):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_16):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_16):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_16):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_16):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_16):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_16):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_16):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_16):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_16):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_16):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_16):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_16):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_16):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_16):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_16):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_16):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_16):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.46 PCE ShadowFor PCI Function 17 (PCE_STATUS_17) — Offset 40500144h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_17):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_17):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_17):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_17):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_17):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_17):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_17):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_17):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_17):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_17):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_17):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_17):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_17):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_17):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_17):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_17):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_17):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_17):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_17):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_17):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_17):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_17):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_17):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.47 PCE ShadowFor PCI Function 18 (PCE_STATUS_18) — Offset 40500148h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_18):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_18):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_18):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_18):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_18):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_18):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_18):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_18):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_18):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_18):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_18):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_18):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_18):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_18):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_18):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_18):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_18):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_18):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_18):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_18):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_18):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_18):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_18):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.48 PCE ShadowFor PCI Function 19 (PCE_STATUS_19) — Offset 4050014Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050014Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_19):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_19):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_19):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_19):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_19):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_19):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_19):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_19):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_19):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_19):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_19):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_19):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_19):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_19):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_19):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_19):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_19):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_19):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_19):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_19):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_19):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_19):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_19):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.49 PCE ShadowFor PCI Function 20 (PCE_STATUS_20) — Offset 40500150h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_20):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_20):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_20):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_20):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_20):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_20):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_20):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_20):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_20):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_20):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_20):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_20):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_20):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_20):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_20):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_20):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_20):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_20):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_20):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_20):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_20):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_20):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_20):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.50 PCE ShadowFor PCI Function 21 (PCE_STATUS_21) — Offset 40500154h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500154h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_21):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_21):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_21):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_21):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_21):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_21):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_21):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_21):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_21):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_21):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_21):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_21):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_21):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_21):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_21):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_21):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_21):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_21):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_21):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_21):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_21):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_21):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_21):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.51 PCE ShadowFor PCI Function 22 (PCE_STATUS_22) — Offset 40500158h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_22):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_22):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_22):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_22):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_22):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_22):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_22):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_22):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_22):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_22):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_22):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_22):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_22):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_22):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_22):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_22):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_22):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_22):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_22):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_22):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_22):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_22):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_22):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.52 PCE ShadowFor PCI Function 23 (PCE_STATUS_23) — Offset 4050015Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050015Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_23):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_23):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_23):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_23):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_23):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_23):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_23):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_23):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_23):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_23):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_23):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_23):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_23):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_23):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_23):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_23):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_23):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_23):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_23):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_23):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_23):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_23):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_23):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.53 PCE ShadowFor PCI Function 24 (PCE_STATUS_24) — Offset 40500160h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_24):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_24):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_24):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_24):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_24):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_24):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_24):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_24):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_24):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_24):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_24):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_24):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_24):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_24):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_24):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_24):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_24):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_24):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_24):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_24):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_24):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_24):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_24):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.54 PCE ShadowFor PCI Function 25 (PCE_STATUS_25) — Offset 40500164h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_25):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_25):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_25):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_25):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_25):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_25):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_25):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_25):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_25):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_25):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_25):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_25):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_25):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_25):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_25):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_25):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_25):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_25):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_25):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_25):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_25):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_25):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_25):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.55 PCE ShadowFor PCI Function 26 (PCE_STATUS_26) — Offset 40500168h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_26):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_26):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_26):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_26):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_26):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_26):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_26):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_26):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_26):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_26):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_26):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_26):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_26):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_26):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_26):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_26):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_26):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_26):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_26):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_26):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_26):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_26):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_26):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.56 PCE ShadowFor PCI Function 27 (PCE_STATUS_27) — Offset 4050016Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050016Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_27):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_27):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_27):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_27):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_27):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_27):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_27):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_27):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_27):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_27):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_27):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_27):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_27):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_27):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_27):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_27):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_27):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_27):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_27):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_27):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_27):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_27):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_27):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.57 PCE ShadowFor PCI Function 28 (PCE_STATUS_28) — Offset 40500170h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500170h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_28):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_28):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_28):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_28):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_28):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_28):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_28):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_28):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_28):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_28):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_28):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_28):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_28):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_28):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_28):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_28):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_28):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_28):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_28):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_28):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_28):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_28):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_28):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.58 PCE ShadowFor PCI Function 29 (PCE_STATUS_29) — Offset 40500174h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500174h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_29):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_29):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_29):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_29):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_29):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_29):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_29):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_29):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_29):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_29):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_29):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_29):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_29):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_29):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_29):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_29):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_29):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_29):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_29):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_29):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_29):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_29):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_29):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.59 PCE ShadowFor PCI Function 30 (PCE_STATUS_30) — Offset 40500178h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500178h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_30):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_30):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_30):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_30):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_30):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_30):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_30):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_30):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_30):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_30):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_30):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_30):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_30):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_30):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_30):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_30):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_30):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_30):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_30):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_30):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_30):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_30):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_30):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.60 PCE ShadowFor PCI Function 31 (PCE_STATUS_31) — Offset 4050017Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050017Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_31):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_31):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_31):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_31):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_31):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_31):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_31):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_31):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_31):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_31):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_31):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_31):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_31):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_31):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_31):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_31):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_31):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_31):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_31):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_31):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_31):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_31):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_31):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.61 PCE ShadowFor PCI Function 32 (PCE_STATUS_32) — Offset 40500180h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500180h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_32):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_32):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_32):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_32):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_32):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_32):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_32):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_32):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_32):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_32):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_32):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_32):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_32):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_32):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_32):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_32):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_32):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_32):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_32):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_32):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_32):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_32):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_32):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.62 PCE ShadowFor PCI Function 33 (PCE_STATUS_33) — Offset 40500184h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500184h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_33):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_33):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_33):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_33):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_33):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_33):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_33):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_33):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_33):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_33):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_33):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_33):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_33):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_33):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_33):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_33):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_33):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_33):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_33):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_33):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_33):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_33):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_33):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.63 PCE ShadowFor PCI Function 34 (PCE_STATUS_34) — Offset 40500188h

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	40500188h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_34):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_34):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_34):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_34):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_34):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_34):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_34):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_34):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_34):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_34):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_34):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_34):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_34):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_34):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_34):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_34):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_34):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_34):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_34):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_34):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_34):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_34):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_34):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.64 PCE ShadowFor PCI Function 35 (PCE_STATUS_35) — Offset 4050018Ch

This register is a shadow register for the 'Power Control Enable' Register in IOSF2OCP bridge. Register to record the live status of D3 and BME along with the rising edge and falling edge interrupts and masks.

Type	Size	Offset	Default
MMIO	32 bit	4050018Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**BME Fall Edge INTR Mask (BME_FALL_EDGE_INTR_MASK_35):** Reflect BME bit falling edge interrupt mask. 1-BME falling interrupt mask set 0-BME falling interrupt mask reset.
27	0h RW	**BME Rise Edge INTR Mask (BME_RISE_EDGE_INTR_MASK_35):** Reflect BME bit rising edge interrupt mask. 1-BME rising interrupt mask set 0-BME rising interrupt mask reset.
26	0h RW/1C	**BME Fall Edge INTR Status (BME_FALL_EDGE_INTR_STATUS_35):** Reflect BME bit falling edge interrupt. 1-BME falling interrupt set 0-BME falling interrupt reset.
25	0h RW/1C	**BME Rise Edge INTR Status (BME_RISE_EDGE_INTR_STATUS_35):** Reflect BME bit rising edge interrupt. 1-BME rising interrupt set 0-BME rising interrupt reset.
24	0h RO	**BME Live Status Bit (BME_LIVE_STATUS_35):** Reflect BME register bit in the bridge. 1-BME set 0-BME reset.
23	0h RW	**D0i3 Enable Mask (D0I3_MASK_35):** Mask for D0i3; if set D0i3 indication is ignored for PG entry.
22	0h RO/V	**D0i3 Live Status (D0I3_LIVE_STATUS_35):** Reflects D0i3 register bit (Bit 2).
21	0h RO	**D0i3 CIP Live Status (D0I3_CIP_LIVE_STATUS_35):** Reflects D0i3 CIP register bit (Bit 0).
20	0h RW	**D3 Fall Edge INTR Mask (D3_FALLING_EDGE_INTR_MASK_35):** Reflect D3 bit falling edge interrupt mask. 1-D3 falling interrupt mask set 0-D3 falling interrupt mask reset.
19	0h RW	**D3 Rise Edge INTR Mask (D3_RISING_EDGE_INTR_MASK_35):** Reflect D3 bit rising edge interrupt mask. 1-D3 rising interrupt mask set 0-D3 rising interrupt mask reset.
18	0h RW/1C	**D3 Fall Edge INTR Status (D3_FALLING_EDGE_INTR_STATUS_35):** Reflect D3 bit falling edge interrupt. 1-D3 falling interrupt set 0-D3 falling interrupt reset.
17	0h RW/1C	**D3 Rise Edge INTR Status (D3_RISING_EDGE_INTR_STATUS_35):** Reflect D3 bit rising edge interrupt. 1-D3 rising interrupt set 0-D3 rising interrupt reset.
16	0h RO/V	**D3 Live Status Bit (D3_LIVE_STATUS_35):** Reflect D3 register bit in the bridge. 1-D3 set 0-D3 reset.
15:13	0h RO	**Reserved**
12	0h RW	**Hardware Autonomous Enable Mask (HAE) (HAE_MASK_35):** Mask bit for HAE; if set PCE changes for HAE will not be detected.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Sleep Enable Mask (SE) (SE_MASK_35):** Mask bit for SE; if set PCE changes for SE will not be detected.
10	0h RW	**D3Hot Enable Mask (D3HEN) (D3HEN_MASK_35):** Mask bit for D3HEN; if set PCE changes for D3HEN will not be detected.
9	0h RW	**IDLE Enable Mask (IDLEN) (IDLEN_MASK_35):** Mask bit for IDLEN; if set PCE changes for IDLEN will not be detected.
8	0h RW	**PMC Request Enable Mask (PMCRE) (PMCRE_MASK_35):** Mask bit for PMCRE; if set PCE changes for PMCRE will not be detected.
7:5	0h RO	**Reserved**
4	0h RO	**Hardware Autonomous Enable (HAE) (HAE_35):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .
3	0h RO	**Sleep Enable (SE) (SE_35):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RO	**D3Hot Enable (D3HEN) (D3HEN_35):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RO	**IDLE Enable (IDLEN) (IDLEN_35):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RO	**PMC Request Enable (PMCRE) (PMCRE_35):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.65 Bridge D3 Rise Interrupt Wake Mask 0 (D3_RISE_INTR_MASK_REG_0) — Offset 40500200h

This register is used to mask D3 rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**D3 Rise Wake Mask For PCI Function 31 (D3_RISE_INTR_MASK_31):** If set D3 rise wake interrupt will be mask for PCI Function 31.
30	0h RW	**D3 Rise Wake Mask For PCI Function 30 (D3_RISE_INTR_MASK_30):** If set D3 rise wake interrupt will be mask for PCI Function 30.
29	0h RW	**D3 Rise Wake Mask For PCI Function 29 (D3_RISE_INTR_MASK_29):** If set D3 rise wake interrupt will be mask for PCI Function 29.
28	0h RW	**D3 Rise Wake Mask For PCI Function 28 (D3_RISE_INTR_MASK_28):** If set D3 rise wake interrupt will be mask for PCI Function 28.
27	0h RW	**D3 Rise Wake Mask For PCI Function 27 (D3_RISE_INTR_MASK_27):** If set D3 rise wake interrupt will be mask for PCI Function 27.
26	0h RW	**D3 Rise Wake Mask For PCI Function 26 (D3_RISE_INTR_MASK_26):** If set D3 rise wake interrupt will be mask for PCI Function 26.
25	0h RW	**D3 Rise Wake Mask For PCI Function 25 (D3_RISE_INTR_MASK_25):** If set D3 rise wake interrupt will be mask for PCI Function 25.
24	0h RW	**D3 Rise Wake Mask For PCI Function 24 (D3_RISE_INTR_MASK_24):** If set D3 rise wake interrupt will be mask for PCI Function 24.
23	0h RW	**D3 Rise Wake Mask For PCI Function 23 (D3_RISE_INTR_MASK_23):** If set D3 rise wake interrupt will be mask for PCI Function 23.
22	0h RW	**D3 Rise Wake Mask For PCI Function 22 (D3_RISE_INTR_MASK_22):** If set D3 rise wake interrupt will be mask for PCI Function 22.
21	0h RW	**D3 Rise Wake Mask For PCI Function 21 (D3_RISE_INTR_MASK_21):** If set D3 rise wake interrupt will be mask for PCI Function 21.
20	0h RW	**D3 Rise Wake Mask For PCI Function 20 (D3_RISE_INTR_MASK_20):** If set D3 rise wake interrupt will be mask for PCI Function 20.
19	0h RW	**D3 Rise Wake Mask For PCI Function 19 (D3_RISE_INTR_MASK_19):** If set D3 rise wake interrupt will be mask for PCI Function 19.
18	0h RW	**D3 Rise Wake Mask For PCI Function 18 (D3_RISE_INTR_MASK_18):** If set D3 rise wake interrupt will be mask for PCI Function 18.
17	0h RW	**D3 Rise Wake Mask For PCI Function 17 (D3_RISE_INTR_MASK_17):** If set D3 rise wake interrupt will be mask for PCI Function 17.
16	0h RW	**D3 Rise Wake Mask For PCI Function 16 (D3_RISE_INTR_MASK_16):** If set D3 rise wake interrupt will be mask for PCI Function 16.
15	0h RW	**D3 Rise Wake Mask For PCI Function 15 (D3_RISE_INTR_MASK_15):** If set D3 rise wake interrupt will be mask for PCI Function 15.
14	0h RW	**D3 Rise Wake Mask For PCI Function 14 (D3_RISE_INTR_MASK_14):** If set D3 rise wake interrupt will be mask for PCI Function 14.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**D3 Rise Wake Mask For PCI Function 13 (D3_RISE_INTR_MASK_13):** If set D3 rise wake interrupt will be mask for PCI Function 13.
12	0h RW	**D3 Rise Wake Mask For PCI Function 12 (D3_RISE_INTR_MASK_12):** If set D3 rise wake interrupt will be mask for PCI Function 12.
11	0h RW	**D3 Rise Wake Mask For PCI Function 11 (D3_RISE_INTR_MASK_11):** If set D3 rise wake interrupt will be mask for PCI Function 11.
10	0h RW	**D3 Rise Wake Mask For PCI Function 10 (D3_RISE_INTR_MASK_10):** If set D3 rise wake interrupt will be mask for PCI Function 10.
9	0h RW	**D3 Rise Wake Mask For PCI Function 9 (D3_RISE_INTR_MASK_9):** If set D3 rise wake interrupt will be mask for PCI Function 9.
8	0h RW	**D3 Rise Wake Mask For PCI Function 8 (D3_RISE_INTR_MASK_8):** If set D3 rise wake interrupt will be mask for PCI Function 8.
7	0h RW	**D3 Rise Wake Mask For PCI Function 7 (D3_RISE_INTR_MASK_7):** If set D3 rise wake interrupt will be mask for PCI Function 7.
6	0h RW	**D3 Rise Wake Mask For PCI Function 6 (D3_RISE_INTR_MASK_6):** If set D3 rise wake interrupt will be mask for PCI Function 6.
5	0h RW	**D3 Rise Wake Mask For PCI Function 5 (D3_RISE_INTR_MASK_5):** If set D3 rise wake interrupt will be mask for PCI Function 5.
4	0h RW	**D3 Rise Wake Mask For PCI Function 4 (D3_RISE_INTR_MASK_4):** If set D3 rise wake interrupt will be mask for PCI Function 4.
3	0h RW	**D3 Rise Wake Mask For PCI Function 3 (D3_RISE_INTR_MASK_3):** If set D3 rise wake interrupt will be mask for PCI Function 3.
2	0h RW	**D3 Rise Wake Mask For PCI Function 2 (D3_RISE_INTR_MASK_2):** If set D3 rise wake interrupt will be mask for PCI Function 2.
1	0h RW	**D3 Rise Wake Mask For PCI Function 1 (D3_RISE_INTR_MASK_1):** If set D3 rise wake interrupt will be mask for PCI Function 1.
0	0h RW	**D3 Rise Wake Mask For PCI Function 0 (D3_RISE_INTR_MASK_0):** If set D3 rise wake interrupt will be mask for PCI Function 0.

14.5.1.66 Bridge D3 Rise Interrupt Wake Mask 1 (D3_RISE_INTR_MASK_REG_1) — Offset 40500204h

This register is used to mask D3 rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**D3 Rise Wake Mask For PCI Function 35 (D3_RISE_INTR_MASK_35):** If set D3 rise wake interrupt will be mask for PCI Function 35.
2	0h RW	**D3 Rise Wake Mask For PCI Function 34 (D3_RISE_INTR_MASK_34):** If set D3 rise wake interrupt will be mask for PCI Function 34.
1	0h RW	**D3 Rise Wake Mask For PCI Function 33 (D3_RISE_INTR_MASK_33):** If set D3 rise wake interrupt will be mask for PCI Function 33.
0	0h RW	**D3 Rise Wake Mask For PCI Function 32 (D3_RISE_INTR_MASK_32):** If set D3 rise wake interrt will be mask for PCI Function 32.

14.5.1.67 Bridge D3 Fall Interrupt Wake Mask 0 (D3_FALL_INTR_MASK_REG_0) — Offset 40500208h

This register is used to mask D3 fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**D3 Fall Wake Mask For PCI Function 31 (D3_FALL_INTR_MASK_31):** If set D3 fall wake interrupt will be mask for PCI Function 31.
30	0h RW	**D3 Fall Wake Mask For PCI Function 30 (D3_FALL_INTR_MASK_30):** If set D3 fall wake interrupt will be mask for PCI Function 30.
29	0h RW	**D3 Fall Wake Mask For PCI Function 29 (D3_FALL_INTR_MASK_29):** If set D3 fall wake interrupt will be mask for PCI Function 29.
28	0h RW	**D3 Fall Wake Mask For PCI Function 28 (D3_FALL_INTR_MASK_28):** If set D3 fall wake interrupt will be mask for PCI Function 28.
27	0h RW	**D3 Fall Wake Mask For PCI Function 27 (D3_FALL_INTR_MASK_27):** If set D3 fall wake interrupt will be mask for PCI Function 27.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**D3 Fall Wake Mask For PCI Function 26 (D3_FALL_INTR_MASK_26):** If set D3 fall wake interrupt will be mask for PCI Function 26.
25	0h RW	**D3 Fall Wake Mask For PCI Function 25 (D3_FALL_INTR_MASK_25):** If set D3 fall wake interrupt will be mask for PCI Function 25.
24	0h RW	**D3 Fall Wake Mask For PCI Function 24 (D3_FALL_INTR_MASK_24):** If set D3 fall wake interrupt will be mask for PCI Function 24.
23	0h RW	**D3 Fall Wake Mask For PCI Function 23 (D3_FALL_INTR_MASK_23):** If set D3 fall wake interrupt will be mask for PCI Function 23.
22	0h RW	**D3 Fall Wake Mask For PCI Function 22 (D3_FALL_INTR_MASK_22):** If set D3 fall wake interrupt will be mask for PCI Function 22.
21	0h RW	**D3 Fall Wake Mask For PCI Function 21 (D3_FALL_INTR_MASK_21):** If set D3 fall wake interrupt will be mask for PCI Function 21.
20	0h RW	**D3 Fall Wake Mask For PCI Function 20 (D3_FALL_INTR_MASK_20):** If set D3 fall wake interrupt will be mask for PCI Function 20.
19	0h RW	**D3 Fall Wake Mask For PCI Function 19 (D3_FALL_INTR_MASK_19):** If set D3 fall wake interrupt will be mask for PCI Function 19.
18	0h RW	**D3 Fall Wake Mask For PCI Function 18 (D3_FALL_INTR_MASK_18):** If set D3 fall wake interrupt will be mask for PCI Function 18.
17	0h RW	**D3 Fall Wake Mask For PCI Function 17 (D3_FALL_INTR_MASK_17):** If set D3 fall wake interrupt will be mask for PCI Function 17.
16	0h RW	**D3 Fall Wake Mask For PCI Function 16 (D3_FALL_INTR_MASK_16):** If set D3 fall wake interrupt will be mask for PCI Function 16.
15	0h RW	**D3 Fall Wake Mask For PCI Function 15 (D3_FALL_INTR_MASK_15):** If set D3 fall wake interrupt will be mask for PCI Function 15.
14	0h RW	**D3 Fall Wake Mask For PCI Function 14 (D3_FALL_INTR_MASK_14):** If set D3 fall wake interrupt will be mask for PCI Function 14.
13	0h RW	**D3 Fall Wake Mask For PCI Function 13 (D3_FALL_INTR_MASK_13):** If set D3 fall wake interrupt will be mask for PCI Function 13.
12	0h RW	**D3 Fall Wake Mask For PCI Function 12 (D3_FALL_INTR_MASK_12):** If set D3 fall wake interrupt will be mask for PCI Function 12.
11	0h RW	**D3 Fall Wake Mask For PCI Function 11 (D3_FALL_INTR_MASK_11):** If set D3 fall wake interrupt will be mask for PCI Function 11.
10	0h RW	**D3 Fall Wake Mask For PCI Function 10 (D3_FALL_INTR_MASK_10):** If set D3 fall wake interrupt will be mask for PCI Function 10.
9	0h RW	**D3 Fall Wake Mask For PCI Function 9 (D3_FALL_INTR_MASK_9):** If set D3 fall wake interrupt will be mask for PCI Function 9.
8	0h RW	**D3 Fall Wake Mask For PCI Function 8 (D3_FALL_INTR_MASK_8):** If set D3 fall wake interrupt will be mask for PCI Function 8.
7	0h RW	**D3 Fall Wake Mask For PCI Function 7 (D3_FALL_INTR_MASK_7):** If set D3 fall wake interrupt will be mask for PCI Function 7.
6	0h RW	**D3 Fall Wake Mask For PCI Function 6 (D3_FALL_INTR_MASK_6):** If set D3 fall wake interrupt will be mask for PCI Function 6.
5	0h RW	**D3 Fall Wake Mask For PCI Function 5 (D3_FALL_INTR_MASK_5):** If set D3 fall wake interrupt will be mask for PCI Function 5.
4	0h RW	**D3 Fall Wake Mask For PCI Function 4 (D3_FALL_INTR_MASK_4):** If set D3 fall wake interrupt will be mask for PCI Function 4.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**D3 Fall Wake Mask For PCI Function 3 (D3_FALL_INTR_MASK_3):** If set D3 fall wake interrupt will be mask for PCI Function 3.
2	0h RW	**D3 Fall Wake Mask For PCI Function 2 (D3_FALL_INTR_MASK_2):** If set D3 fall wake interrupt will be mask for PCI Function 2.
1	0h RW	**D3 Fall Wake Mask For PCI Function 1 (D3_FALL_INTR_MASK_1):** If set D3 fall wake interrupt will be mask for PCI Function 1.
0	0h RW	**D3 Fall Wake Mask For PCI Function 0 (D3_FALL_INTR_MASK_0):** If set D3 fall wake interrupt will be mask for PCI Function 0.

14.5.1.68 Bridge D3 Fall Interrupt Wake Mask 1 (D3_FALL_INTR_MASK_REG_1) — Offset 4050020Ch

This register is used to mask D3 fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	4050020Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**D3 Fall Wake Mask For PCI Function 35 (D3_FALL_INTR_MASK_35):** If set D3 fall wake interrupt will be mask for PCI Function 35.
2	0h RW	**D3 Fall Wake Mask For PCI Function 34 (D3_FALL_INTR_MASK_34):** If set D3 fall wake interrupt will be mask for PCI Function 34.
1	0h RW	**D3 Fall Wake Mask For PCI Function 33 (D3_FALL_INTR_MASK_33):** If set D3 fall wake interrupt will be mask for PCI Function 33.
0	0h RW	**D3 Fall Wake Mask For PCI Function 32 (D3_FALL_INTR_MASK_32):** If set D3 fall wake interrupt will be mask for PCI Function 32.

14.5.1.69 Bridge D3 Rise Interrupt Wake0 (D3_RISE_INTR_REG_31_0) — Offset 40500210h

This register is used to record D3 rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**D3 Rise Wake Record For PCI Function 31 To 0 (D3_RISE_INTR_31_0):** D3 rise wake interrupt record for PCI Function 31 to 0.

14.5.1.70 Bridge D3 Rise Interrupt Wake1 (D3_RISE_INTR_REG_35_32) — Offset 40500214h

This register is used to record D3 rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500214h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/1C	**D3 Rise Wake Record For PCI Function 35 To 32 (D3_RISE_INTR_35_32):** D3 rise wake interrupt record for PCI Function 35 to 32.

14.5.1.71 Bridge D3 Fall Interrupt Wake0 (D3_FALL_INTR_REG_31_0) — Offset 40500218h

This register is used to record D3 fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500218h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**D3 Fall Wake Record For PCI Function 31 To 0 (D3_FALL_INTR_31_0):** D3 fall wake interrupt record for PCI Function 31 to 0.

14.5.1.72 Bridge D3 Fall Interrupt Wake1 (D3_FALL_INTR_REG_35_32) — Offset 4050021Ch

This register is used to record D3 fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	4050021Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/1C	**D3 Fall Wake Record For PCI Function 35 To 32 (D3_FALL_INTR_35_32):** D3 fall wake interrupt record for PCI Function 35 to 32.

14.5.1.73 BME Rise Interrupt Wake Mask 0 (BME_RISE_INTR_MASK_REG_0) — Offset 40500220h

This register is used to mask BME rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BME Rise Wake Mask For PCI Function 31 (BME_RISE_INTR_MASK_31):** If set BME rise wake interrupt will be mask for PCI Function 31.
30	0h RW	**BME Rise Wake Mask For PCI Function 30 (BME_RISE_INTR_MASK_30):** If set BME rise wake interrupt will be mask for PCI Function 30.
29	0h RW	**BME Rise Wake Mask For PCI Function 29 (BME_RISE_INTR_MASK_29):** If set BME rise wake interrupt will be mask for PCI Function 29.
28	0h RW	**BME Rise Wake Mask For PCI Function 28 (BME_RISE_INTR_MASK_28):** If set BME rise wake interrupt will be mask for PCI Function 28.
27	0h RW	**BME Rise Wake Mask For PCI Function 27 (BME_RISE_INTR_MASK_27):** If set BME rise wake interrupt will be mask for PCI Function 27.
26	0h RW	**BME Rise Wake Mask For PCI Function 26 (BME_RISE_INTR_MASK_26):** If set BME rise wake interrupt will be mask for PCI Function 26.
25	0h RW	**BME Rise Wake Mask For PCI Function 25 (BME_RISE_INTR_MASK_25):** If set BME rise wake interrupt will be mask for PCI Function 25.
24	0h RW	**BME Rise Wake Mask For PCI Function 24 (BME_RISE_INTR_MASK_24):** If set BME rise wake interrupt will be mask for PCI Function 24.
23	0h RW	**BME Rise Wake Mask For PCI Function 23 (BME_RISE_INTR_MASK_23):** If set BME rise wake interrupt will be mask for PCI Function 23.
22	0h RW	**BME Rise Wake Mask For PCI Function 22 (BME_RISE_INTR_MASK_22):** If set BME rise wake interrupt will be mask for PCI Function 22.
21	0h RW	**BME Rise Wake Mask For PCI Function 21 (BME_RISE_INTR_MASK_21):** If set BME rise wake interrupt will be mask for PCI Function 21.
20	0h RW	**BME Rise Wake Mask For PCI Function 20 (BME_RISE_INTR_MASK_20):** If set BME rise wake interrupt will be mask for PCI Function 20.
19	0h RW	**BME Rise Wake Mask For PCI Function 19 (BME_RISE_INTR_MASK_19):** If set BME rise wake interrupt will be mask for PCI Function 19.
18	0h RW	**BME Rise Wake Mask For PCI Function 18 (BME_RISE_INTR_MASK_18):** If set BME rise wake interrupt will be mask for PCI Function 18.
17	0h RW	**BME Rise Wake Mask For PCI Function 17 (BME_RISE_INTR_MASK_17):** If set BME rise wake interrupt will be mask for PCI Function 17.
16	0h RW	**BME Rise Wake Mask For PCI Function 16 (BME_RISE_INTR_MASK_16):** If set BME rise wake interrupt will be mask for PCI Function 16.
15	0h RW	**BME Rise Wake Mask For PCI Function 15 (BME_RISE_INTR_MASK_15):** If set BME rise wake interrupt will be mask for PCI Function 15.
14	0h RW	**BME Rise Wake Mask For PCI Function 14 (BME_RISE_INTR_MASK_14):** If set BME rise wake interrupt will be mask for PCI Function 14.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**BME Rise Wake Mask For PCI Function 13 (BME_RISE_INTR_MASK_13):** If set BME rise wake interrupt will be mask for PCI Function 13.
12	0h RW	**BME Rise Wake Mask For PCI Function 12 (BME_RISE_INTR_MASK_12):** If set BME rise wake interrupt will be mask for PCI Function 12.
11	0h RW	**BME Rise Wake Mask For PCI Function 11 (BME_RISE_INTR_MASK_11):** If set BME rise wake interrupt will be mask for PCI Function 11.
10	0h RW	**BME Rise Wake Mask For PCI Function 10 (BME_RISE_INTR_MASK_10):** If set BME rise wake interrupt will be mask for PCI Function 10.
9	0h RW	**BME Rise Wake Mask For PCI Function 9 (BME_RISE_INTR_MASK_9):** If set BME rise wake interrupt will be mask for PCI Function 9.
8	0h RW	**BME Rise Wake Mask For PCI Function 8 (BME_RISE_INTR_MASK_8):** If set BME rise wake interrupt will be mask for PCI Function 8.
7	0h RW	**BME Rise Wake Mask For PCI Function 7 (BME_RISE_INTR_MASK_7):** If set BME rise wake interrupt will be mask for PCI Function 7.
6	0h RW	**BME Rise Wake Mask For PCI Function 6 (BME_RISE_INTR_MASK_6):** If set BME rise wake interrupt will be mask for PCI Function 6.
5	0h RW	**BME Rise Wake Mask For PCI Function 5 (BME_RISE_INTR_MASK_5):** If set BME rise wake interrupt will be mask for PCI Function 5.
4	0h RW	**BME Rise Wake Mask For PCI Function 4 (BME_RISE_INTR_MASK_4):** If set BME rise wake interrupt will be mask for PCI Function 4.
3	0h RW	**BME Rise Wake Mask For PCI Function 3 (BME_RISE_INTR_MASK_3):** If set BME rise wake interrupt will be mask for PCI Function 3.
2	0h RW	**BME Rise Wake Mask For PCI Function 2 (BME_RISE_INTR_MASK_2):** If set BME rise wake interrupt will be mask for PCI Function 2.
1	0h RW	**BME Rise Wake Mask For PCI Function 1 (BME_RISE_INTR_MASK_1):** If set BME rise wake interrupt will be mask for PCI Function 1.
0	0h RW	**BME Rise Wake Mask For PCI Function 0 (BME_RISE_INTR_MASK_0):** If set BME rise wake interrupt will be mask for PCI Function 0.

14.5.1.74 BME Rise Interrupt Wake Mask 1 (BME_RISE_INTR_MASK_REG_1) — Offset 40500224h

This register is used to mask BME rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500224h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**BME Rise Wake Mask For PCI Function 35 To 32 (BME_RISE_INTR_MASK_35_32):** If set BME rise wake interrupt will be mask for PCI Function 35 to 32.

14.5.1.75 BME Fall Interrupt Wake Mask 0 (BME_FALL_INTR_MASK_REG_0) — Offset 40500228h

This register is used to mask BME fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BME Fall Wake Mask For PCI Function 31 (BME_FALL_INTR_MASK_31):** If set BME fall wake interrupt will be mask for PCI Function 31.
30	0h RW	**BME Fall Wake Mask For PCI Function 30 (BME_FALL_INTR_MASK_30):** If set BME fall wake interrupt will be mask for PCI Function 30.
29	0h RW	**BME Fall Wake Mask For PCI Function 29 (BME_FALL_INTR_MASK_29):** If set BME fall wake interrupt will be mask for PCI Function 29.
28	0h RW	**BME Fall Wake Mask For PCI Function 28 (BME_FALL_INTR_MASK_28):** If set BME fall wake interrupt will be mask for PCI Function 28.
27	0h RW	**BME Fall Wake Mask For PCI Function 27 (BME_FALL_INTR_MASK_27):** If set BME fall wake interrupt will be mask for PCI Function 27.
26	0h RW	**BME Fall Wake Mask For PCI Function 26 (BME_FALL_INTR_MASK_26):** If set BME fall wake interrupt will be mask for PCI Function 26.
25	0h RW	**BME Fall Wake Mask For PCI Function 25 (BME_FALL_INTR_MASK_25):** If set BME fall wake interrupt will be mask for PCI Function 25.
24	0h RW	**BME Fall Wake Mask For PCI Function 24 (BME_FALL_INTR_MASK_24):** If set BME fall wake interrupt will be mask for PCI Function 24.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**BME Fall Wake Mask For PCI Function 23 (BME_FALL_INTR_MASK_23):** If set BME fall wake interrupt will be mask for PCI Function 23.
22	0h RW	**BME Fall Wake Mask For PCI Function 22 (BME_FALL_INTR_MASK_22):** If set BME fall wake interrupt will be mask for PCI Function 22.
21	0h RW	**BME Fall Wake Mask For PCI Function 21 (BME_FALL_INTR_MASK_21):** If set BME fall wake interrupt will be mask for PCI Function 21.
20	0h RW	**BME Fall Wake Mask For PCI Function 20 (BME_FALL_INTR_MASK_20):** If set BME fall wake interrupt will be mask for PCI Function 20.
19	0h RW	**BME Fall Wake Mask For PCI Function 19 (BME_FALL_INTR_MASK_19):** If set BME fall wake interrupt will be mask for PCI Function 19.
18	0h RW	**BME Fall Wake Mask For PCI Function 18 (BME_FALL_INTR_MASK_18):** If set BME fall wake interrupt will be mask for PCI Function 18.
17	0h RW	**BME Fall Wake Mask For PCI Function 17 (BME_FALL_INTR_MASK_17):** If set BME fall wake interrupt will be mask for PCI Function 17.
16	0h RW	**BME Fall Wake Mask For PCI Function 16 (BME_FALL_INTR_MASK_16):** If set BME fall wake interrupt will be mask for PCI Function 16.
15	0h RW	**BME Fall Wake Mask For PCI Function 15 (BME_FALL_INTR_MASK_15):** If set BME fall wake interrupt will be mask for PCI Function 15.
14	0h RW	**BME Fall Wake Mask For PCI Function 14 (BME_FALL_INTR_MASK_14):** If set BME fall wake interrupt will be mask for PCI Function 14.
13	0h RW	**BME Fall Wake Mask For PCI Function 13 (BME_FALL_INTR_MASK_13):** If set BME fall wake interrupt will be mask for PCI Function 13.
12	0h RW	**BME Fall Wake Mask For PCI Function 12 (BME_FALL_INTR_MASK_12):** If set BME fall wake interrupt will be mask for PCI Function 12.
11	0h RW	**BME Fall Wake Mask For PCI Function 11 (BME_FALL_INTR_MASK_11):** If set BME fall wake interrupt will be mask for PCI Function 11.
10	0h RW	**BME Fall Wake Mask For PCI Function 10 (BME_FALL_INTR_MASK_10):** If set BME fall wake interrupt will be mask for PCI Function 10.
9	0h RW	**BME Fall Wake Mask For PCI Function 9 (BME_FALL_INTR_MASK_9):** If set BME fall wake interrupt will be mask for PCI Function 9.
8	0h RW	**BME Fall Wake Mask For PCI Function 8 (BME_FALL_INTR_MASK_8):** If set BME fall wake interrupt will be mask for PCI Function 8.
7	0h RW	**BME Fall Wake Mask For PCI Function 7 (BME_FALL_INTR_MASK_7):** If set BME fall wake interrupt will be mask for PCI Function 7.
6	0h RW	**BME Fall Wake Mask For PCI Function 6 (BME_FALL_INTR_MASK_6):** If set BME fall wake interrupt will be mask for PCI Function 6.
5	0h RW	**BME Fall Wake Mask For PCI Function 5 (BME_FALL_INTR_MASK_5):** If set BME fall wake interrupt will be mask for PCI Function 5.
4	0h RW	**BME Fall Wake Mask For PCI Function 4 (BME_FALL_INTR_MASK_4):** If set BME fall wake interrupt will be mask for PCI Function 4.
3	0h RW	**BME Fall Wake Mask For PCI Function 3 (BME_FALL_INTR_MASK_3):** If set BME fall wake interrupt will be mask for PCI Function 3.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**BME Fall Wake Mask For PCI Function 2 (BME_FALL_INTR_MASK_2):** If set BME fall wake interrupt will be mask for PCI Function 2.
1	0h RW	**BME Fall Wake Mask For PCI Function 1 (BME_FALL_INTR_MASK_1):** If set BME fall wake interrupt will be mask for PCI Function 1.
0	0h RW	**BME Fall Wake Mask For PCI Function 0 (BME_FALL_INTR_MASK_0):** If set BME fall wake interrupt will be mask for PCI Function 0.

14.5.1.76 BME Fall Interrupt Wake Mask 1 (BME_FALL_INTR_MASK_REG_1) — Offset 4050022Ch

This register is used to mask BME fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	4050022Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**BME Fall Wake Mask For PCI Function 35 To 32 (BME_FALL_INTR_MASK_35_32):** If set BME fall wake interrupt will be mask for PCI Function 35 to 32.

14.5.1.77 BME Rise Interrupt Wake0 (BME_RISE_INTR_REG_0) — Offset 40500230h

This register is used to record BME rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**BME Rise Wake Record For PCI Function 31 To 0 (BME_RISE_INTR_31_0):** BME rise wake interrupt record for PCI Function 31 to 0.

14.5.1.78 BME Rise Interrupt Wake1 (BME_RISE_INTR_REG_1) — Offset 40500234h

This register is used to record BME rise interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500234h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/1C	**BME Rise Wake Record For PCI Function 35 To 32 (BME_RISE_INTR_35_32):** BME rise wake interrupt record for PCI Function 35 to 32.

14.5.1.79 BME Fall Interrupt Wake0 (BME_FALL_INTR_REG_0) — Offset 40500238h

This register is used to record BME fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500238h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**BME Fall Wake Record For PCI Function 31 To 0 (BME_FALL_INTR_31_0):** BME fall wake interrupt record for PCI Function 31 to 0.

14.5.1.80 BME Fall Interrupt Wake1 (BME_FALL_INTR_REG_1) — Offset 4050023Ch

This register is used to record BME fall interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	4050023Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/1C	**BME Fall Wake Record For PCI Function 35 To 32 (BME_FALL_INTR_35_32):** BME fall wake interrupt record for PCI Function 35 to 32.

14.5.1.81 Bridge D3 Interrupt Wake Mask 0 (D3_INTR_MASK_REG_0) — Offset 40500240h

This register is used to mask D3 interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500240h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**D3 Wake Mask For PCI Function 31 (D3_INTR_MASK_31):** If set D3 wake interrupt will be mask for PCI Function 31.
30	0h RW	**D3 Wake Mask For PCI Function 30 (D3_INTR_MASK_30):** If set D3 wake interrupt will be mask for PCI Function 30.
29	0h RW	**D3 Wake Mask For PCI Function 29 (D3_INTR_MASK_29):** If set D3 wake interrupt will be mask for PCI Function 29.
28	0h RW	**D3 Wake Mask For PCI Function 28 (D3_INTR_MASK_28):** If set D3 wake interrupt will be mask for PCI Function 28.
27	0h RW	**D3 Wake Mask For PCI Function 27 (D3_INTR_MASK_27):** If set D3 wake interrupt will be mask for PCI Function 27.
26	0h RW	**D3 Wake Mask For PCI Function 26 (D3_INTR_MASK_26):** If set D3 wake interrupt will be mask for PCI Function 26.
25	0h RW	**D3 Wake Mask For PCI Function 25 (D3_INTR_MASK_25):** If set D3 wake interrupt will be mask for PCI Function 25.
24	0h RW	**D3 Wake Mask For PCI Function 24 (D3_INTR_MASK_24):** If set D3 wake interrupt will be mask for PCI Function 24.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**D3 Wake Mask For PCI Function 23 (D3_INTR_MASK_23):** If set D3 wake interrupt will be mask for PCI Function 23.
22	0h RW	**D3 Wake Mask For PCI Function 22 (D3_INTR_MASK_22):** If set D3 wake interrupt will be mask for PCI Function 22.
21	0h RW	**D3 Wake Mask For PCI Function 21 (D3_INTR_MASK_21):** If set D3 wake interrupt will be mask for PCI Function 21.
20	0h RW	**D3 Wake Mask For PCI Function 20 (D3_INTR_MASK_20):** If set D3 wake interrupt will be mask for PCI Function 20.
19	0h RW	**D3 Wake Mask For PCI Function 19 (D3_INTR_MASK_19):** If set D3 wake interrupt will be mask for PCI Function 19.
18	0h RW	**D3 Wake Mask For PCI Function 18 (D3_INTR_MASK_18):** If set D3 wake interrupt will be mask for PCI Function 18.
17	0h RW	**D3 Wake Mask For PCI Function 17 (D3_INTR_MASK_17):** If set D3 wake interrupt will be mask for PCI Function 17.
16	0h RW	**D3 Wake Mask For PCI Function 16 (D3_INTR_MASK_16):** If set D3 wake interrupt will be mask for PCI Function 16.
15	0h RW	**D3 Wake Mask For PCI Function 15 (D3_INTR_MASK_15):** If set D3 wake interrupt will be mask for PCI Function 15.
14	0h RW	**D3 Wake Mask For PCI Function 14 (D3_INTR_MASK_14):** If set D3 wake interrupt will be mask for PCI Function 14.
13	0h RW	**D3 Wake Mask For PCI Function 13 (D3_INTR_MASK_13):** If set D3 wake interrupt will be mask for PCI Function 13.
12	0h RW	**D3 Wake Mask For PCI Function 12 (D3_INTR_MASK_12):** If set D3 wake interrupt will be mask for PCI Function 12.
11	0h RW	**D3 Wake Mask For PCI Function 11 (D3_INTR_MASK_11):** If set D3 wake interrupt will be mask for PCI Function 11.
10	0h RW	**D3 Wake Mask For PCI Function 10 (D3_INTR_MASK_10):** If set D3 wake interrupt will be mask for PCI Function 10.
9	0h RW	**D3 Wake Mask For PCI Function 9 (D3_INTR_MASK_9):** If set D3 wake interrupt will be mask for PCI Function 9.
8	0h RW	**D3 Wake Mask For PCI Function 8 (D3_INTR_MASK_8):** If set D3 wake interrupt will be mask for PCI Function 8.
7	0h RW	**D3 Wake Mask For PCI Function 7 (D3_INTR_MASK_7):** If set D3 wake interrupt will be mask for PCI Function 7.
6	0h RW	**D3 Wake Mask For PCI Function 6 (D3_INTR_MASK_6):** If set D3 wake interrupt will be mask for PCI Function 6.
5	0h RW	**D3 Wake Mask For PCI Function 5 (D3_INTR_MASK_5):** If set D3 wake interrupt will be mask for PCI Function 5.
4	0h RW	**D3 Wake Mask For PCI Function 4 (D3_INTR_MASK_4):** If set D3 wake interrupt will be mask for PCI Function 4.
3	0h RW	**D3 Wake Mask For PCI Function 3 (D3_INTR_MASK_3):** If set D3 wake interrupt will be mask for PCI Function 3.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**D3 Wake Mask For PCI Function 2 (D3_INTR_MASK_2):** If set D3 wake interrupt will be mask for PCI Function 2.
1	0h RW	**D3 Wake Mask For PCI Function 1 (D3_INTR_MASK_1):** If set D3 wake interrupt will be mask for PCI Function 1.
0	0h RW	**D3 Wake Mask For PCI Function 0 (D3_INTR_MASK_0):** If set D3 wake interrupt will be mask for PCI Function 0.

14.5.1.82 Bridge D3 Interrupt Wake Mask 1 (D3_INTR_MASK_REG_1) — Offset 40500244h

This register is used to mask D3 interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500244h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**D3 Wake Mask For PCI Function 35 To 32 (D3_INTR_MASK_35_32):** If set D3 wake interrupt will be mask for PCI Function 35 to 32.

14.5.1.83 Bridge D3 Interrupt Wake0 (D3_INTR_REG_0) — Offset 40500248h

This register is used to record D3 interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	40500248h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**D3 Wake Record For PCI Function 31 To 0 (D3_INTR_31_0):** D3 wake interrupt record for PCI Function 1.

14.5.1.84 Bridge D3 Interrupt Wake1 (D3_INTR_REG_1) — Offset 4050024Ch

This register is used to record D3 interrupt for each PCI function.

Type	Size	Offset	Default
MMIO	32 bit	4050024Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/1C	**D3 Wake Record For PCI Function 35 To 32 (D3_INTR_35_32):** D3 wake interrupt record for PCI Function 35 to 32.

14.5.1.85 GPIO Wake Mask0 (GPIO_INTR_WK_MASK_REG_0) — Offset 40500250h

This register is used for masking the wakes from gpio pins [31:0].

Type	Size	Offset	Default
MMIO	32 bit	40500250h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPIO Wake Mask For Register 0 (GPIO_WK_MSK_0_REG):** Setting this bit masks wake from the corresponding gpio_pin.

14.5.1.86 GPIO Wake Mask1 (GPIO_INTR_WK_MASK_REG_1) — Offset 40500254h

This register is used for masking the wakes from gpio pins [63:32].

Type	Size	Offset	Default
MMIO	32 bit	40500254h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPIO Wake Mask For Register 1 (GPIO_WK_MSK_1_REG):** Setting this bit masks wake from the corresponding gpio_pin.

14.5.1.87 GPIO Wake Mask2 (GPIO_INTR_WK_MASK_REG_2) — Offset 40500258h

This register is used for masking the wakes from gpio pins [95:64].

Type	Size	Offset	Default
MMIO	32 bit	40500258h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPIO Wake Mask For Register 2 (GPIO_WK_MSK_2_REG):** Setting this bit masks wake from the corresponding gpio_pin.

14.5.1.88 GPIO Wake Mask3 (GPIO_INTR_WK_MASK_REG_3) — Offset 4050025Ch

This register is used for masking the wakes from gpio pins [127:96].

Type	Size	Offset	Default
MMIO	32 bit	4050025Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPIO Wake Mask For Register 3 (GPIO_WK_MSK_3_REG):** Setting this bit masks wake from the corresponding gpio_pin.

14.5.1.89 GPIO Wake Interrupt Record 0 (GPIO_INTR_REG_0) — Offset 40500270h

This register is used to record wake from GPIO.

Type	Size	Offset	Default
MMIO	32 bit	40500270h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**GPIO Wake Record For GPIO_31 (GPIO_INTR_31):** GPIO wake interrupt record for GPIO_31.
30	0h RW/1C	**GPIO Wake Record For GPIO_30 (GPIO_INTR_30):** GPIO wake interrupt record for GPIO_30.
29	0h RW/1C	**GPIO Wake Record For GPIO_29 (GPIO_INTR_29):** GPIO wake interrupt record for GPIO_29.
28	0h RW/1C	**GPIO Wake Record For GPIO_28 (GPIO_INTR_28):** GPIO wake interrupt record for GPIO_28.
27	0h RW/1C	**GPIO Wake Record For GPIO_27 (GPIO_INTR_27):** GPIO wake interrupt record for GPIO_27.
26	0h RW/1C	**GPIO Wake Record For GPIO_26 (GPIO_INTR_26):** GPIO wake interrupt record for GPIO_26.
25	0h RW/1C	**GPIO Wake Record For GPIO_25 (GPIO_INTR_25):** GPIO wake interrupt record for GPIO_25.
24	0h RW/1C	**GPIO Wake Record For GPIO_24 (GPIO_INTR_24):** GPIO wake interrupt record for GPIO_24.
23	0h RW/1C	**GPIO Wake Record For GPIO_23 (GPIO_INTR_23):** GPIO wake interrupt record for GPIO_23.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW/1C	**GPIO Wake Record For GPIO_22 (GPIO_INTR_22):** GPIO wake interrupt record for GPIO_22.
21	0h RW/1C	**GPIO Wake Record For GPIO_21 (GPIO_INTR_21):** GPIO wake interrupt record for GPIO_21.
20	0h RW/1C	**GPIO Wake Record For GPIO_20 (GPIO_INTR_20):** GPIO wake interrupt record for GPIO_20.
19	0h RW/1C	**GPIO Wake Record For GPIO_19 (GPIO_INTR_19):** GPIO wake interrupt record for GPIO_19.
18	0h RW/1C	**GPIO Wake Record For GPIO_18 (GPIO_INTR_18):** GPIO wake interrupt record for GPIO_18.
17	0h RW/1C	**GPIO Wake Record For GPIO_17 (GPIO_INTR_17):** GPIO wake interrupt record for GPIO_17.
16	0h RW/1C	**GPIO Wake Record For GPIO_16 (GPIO_INTR_16):** GPIO wake interrupt record for GPIO_16.
15	0h RW/1C	**GPIO Wake Record For GPIO_15 (GPIO_INTR_15):** GPIO wake interrupt record for GPIO_15.
14	0h RW/1C	**GPIO Wake Record For GPIO_14 (GPIO_INTR_14):** GPIO wake interrupt record for GPIO_14.
13	0h RW/1C	**GPIO Wake Record For GPIO_13 (GPIO_INTR_13):** GPIO wake interrupt record for GPIO_13.
12	0h RW/1C	**GPIO Wake Record For GPIO_12 (GPIO_INTR_12):** GPIO wake interrupt record for GPIO_12.
11	0h RW/1C	**GPIO Wake Record For GPIO_11 (GPIO_INTR_11):** GPIO wake interrupt record for GPIO_11.
10	0h RW/1C	**GPIO Wake Record For GPIO_10 (GPIO_INTR_10):** GPIO wake interrupt record for GPIO_10.
9	0h RW/1C	**GPIO Wake Record For GPIO_9 (GPIO_INTR_9):** GPIO wake interrupt record for GPIO_9.
8	0h RW/1C	**GPIO Wake Record For GPIO_8 (GPIO_INTR_8):** GPIO wake interrupt record for GPIO_8.
7	0h RW/1C	**GPIO Wake Record For GPIO_7 (GPIO_INTR_7):** GPIO wake interrupt record for GPIO_7.
6	0h RW/1C	**GPIO Wake Record For GPIO_6 (GPIO_INTR_6):** GPIO wake interrupt record for GPIO_6.
5	0h RW/1C	**GPIO Wake Record For GPIO_5 (GPIO_INTR_5):** GPIO wake interrupt record for GPIO_5.
4	0h RW/1C	**GPIO Wake Record For GPIO_4 (GPIO_INTR_4):** GPIO wake interrupt record for GPIO_4.
3	0h RW/1C	**GPIO Wake Record For GPIO_3 (GPIO_INTR_3):** GPIO wake interrupt record for GPIO_3.
2	0h RW/1C	**GPIO Wake Record For GPIO_2 (GPIO_INTR_2):** GPIO wake interrupt record for GPIO_2.
1	0h RW/1C	**GPIO Wake Record For GPIO_1 (GPIO_INTR_1):** GPIO wake interrupt record for GPIO_1.
0	0h RW/1C	**GPIO Wake Record For GPIO_0 (GPIO_INTR_0):** GPIO wake interrupt record for GPIO_0.

14.5.1.90 GPIO Wake Interrupt Record 1 (GPIO_INTR_REG_1) — Offset 40500274h

This register is used to record wake from GPIO.

Type	Size	Offset	Default
MMIO	32 bit	40500274h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW/1C	**GPIO Wake Record For GPIO_63 To 36 (GPIO_INTR_63_36):** GPIO wake interrupt record for GPIO_63_36.
3	0h RW/1C	**GPIO Wake Record For GPIO_35 (I3C IBI Wake) (GPIO_INTR_35):** GPIO wake interrupt record for GPIO_35.
2	0h RW/1C	**GPIO Wake Record For GPIO_34 (UART2 CTS) (GPIO_INTR_34):** GPIO wake interrupt record for GPIO_34.
1	0h RW/1C	**GPIO Wake Record For GPIO_33 (UART1 CTS) (GPIO_INTR_33):** GPIO wake interrupt record for GPIO_33.
0	0h RW/1C	**GPIO Wake Record For GPIO_32 (UART0 CTS) (GPIO_INTR_32):** GPIO wake interrupt record for GPIO_32.

14.5.1.91 GPIO Wake Interrupt Record 2 (GPIO_INTR_REG_2) — Offset 40500278h

This register is used to record wake from GPIO.

Type	Size	Offset	Default
MMIO	32 bit	40500278h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GPIO Wake Record For GPIO_ 95 To 64 (GPIO_INTR_95_64):** GPIO wake interrupt record for GPIO_95_64.

14.5.1.92 GPIO Wake Interrupt Record 3 (GPIO_INTR_REG_3) — Offset 4050027Ch

This register is used to record wake from GPIO.

Type	Size	Offset	Default
MMIO	32 bit	4050027Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**GPIO Wake Record For GPIO_ 127 To 96 (GPIO_INTR_127_96):** GPIO wake interrupt record for GPIO_127_96.

14.5.1.93 PWM And I2S Wake Interrupt (I2S_INTR_REG) — Offset 40500290h

This register is used to record wake from I2S.

Type	Size	Offset	Default
MMIO	32 bit	40500290h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW/1C	**Wake Record Register For PWM_0 (PWM_INTR_0):** This will record wake interrupt from PWM_0.
7:0	0h RO	**Reserved**

14.5.1.94 I2S Interrupt Mask (I2S_INTR_MASK_REG) — Offset 40500294h

This register is used to mask wake from I2S.

Type	Size	Offset	Default
MMIO	32 bit	40500294h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Wake Mask For PWM_0 (PWM_INTR_MASK_0):** If set wake interrupt for PWM_0 will be masked.
7:0	0h RO	**Reserved**

14.5.1.95 IETHERNET Wake Interrupt (ETHER_INTR_REG) — Offset 40500298h

This register is used to record wake from Ethernet.

Type	Size	Offset	Default
MMIO	32 bit	40500298h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/1C	**Wake Record Register For Canbus_1 (CANBUS_INTR_1):** This will record wake interrupt from Canbus_1.
16	0h RW/1C	**Wake Record Register For Canbus_0 (CANBUS_INTR_0):** This will record wake interrupt from Canbus_0.
15:0	0h RO	**Reserved**

14.5.1.96 ETHERNET Interrupt Mask (ETHERNET_INTR_MASK_REG) — Offset 4050029Ch

This register is used to mask wake from ETHERNET.

Type	Size	Offset	Default
MMIO	32 bit	4050029Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Wake Mask For CANBUS_1 (CANBUS_INTR_MASK_1):** If set wake interrupt for CANBUS_1 will be masked.
16	0h RW	**Wake Mask For CANBUS_0 (CANBUS_INTR_MASK_0):** If set wake interrupt for CANBUS_0 will be masked.
15:9	00h RO	**ETHERNET_INTR_MASK_12_15:** Reserved
8:0	0h RO	**Reserved**

14.5.1.97 QEP Wake Interrupt (QEP_INTR_REG) — Offset 405002A0h

This register is used to record wake from QEP.

Type	Size	Offset	Default
MMIO	32 bit	405002A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/1C	**Wake Record Register For QEP_3 (QEP_INTR_3):** This will record wake interrupt from QEP_3.
2	0h RW/1C	**Wake Record Register For QEP_2 (QEP_INTR_2):** This will record wake interrupt from QEP_2.
1	0h RW/1C	**Wake Record Register For QEP_1 (QEP_INTR_1):** This will record wake interrupt from QEP_1.
0	0h RW/1C	**Wake Record Register For QEP_0 (QEP_INTR_0):** This will record wake interrupt from QEP_0.

14.5.1.98 QEP Interrupt Mask (QEP_INTR_MASK_REG) — Offset 405002A4h

This register is used to mask wake from QEP.

Type	Size	Offset	Default
MMIO	32 bit	405002A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Reserved**
7:4	0h RO	**Reserved**
3	0h RW	**Wake Mask For QEP_3 (QEP_INTR_MASK_3):** If set wake interrupt for QEP_3 will be masked.
2	0h RW	**Wake Mask For QEP_2 (QEP_INTR_MASK_2):** If set wake interrupt for QEP_2 will be masked.
1	0h RW	**Wake Mask For QEP_1 (QEP_INTR_MASK_1):** If set wake interrupt for QEP_1 will be masked.
0	0h RW	**Wake Mask For QEP_0 (QEP_INTR_MASK_0):** If set wake interrupt for QEP_0 will be masked.

14.5.1.99 PMU LART Update (ADR_LART_UPD_REG) — Offset 405002A8h

This register enables the Local ART update as part of HH flow.

Type	Size	Offset	Default
MMIO	32 bit	405002A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RO	**PMU_LART_UPD_RSVD1:** Reserved
9	0h RW	**PMU LART Update Interrupt Mask (PMU_LART_UPD_INT_MASK):** The interrupt mask is set by FW to mask the LART update interrupt.
8	0h RW/1C	**PMU LART Update Interrupt Status (PMU_LART_UPD_INT):** The interrupt status is set when LART update is completed.
7:1	00h RO	**PMU_LART_UPD_RSVD0:** Reserved
0	0h RW	**PMU LART Update Enable (PMU_LART_UPD_EN):** When set , initiates the Local ART value update for LMT.

14.5.1.100 ISH HOST DEV Interrupt (HOST_DEV_REG) — Offset 405002ACh

This register is used to record interrupt from host device.

Type	Size	Offset	Default
MMIO	32 bit	405002ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**HOST DEV Interrupt Mask (PMU_HOST_DEV_INT_MASK):** If set wake interrupt for HOST DEV will be masked.
0	0h RW/1C	**HOST DEV Interrupt (PMU_HOST_DEV_INT):** This will record interrupt from HOST DEV.

14.5.1.101 PCI Interrupt0 (PCE_INTR_REG_0) — Offset 405002B0h

Combined interrupt status for each PCI functiion. This register is RO for the FW to identify the function where the interrupt status is set.

Type	Size	Offset	Default
MMIO	32 bit	405002B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**PCI Interrupt Record For PCI_31_0 (PCE_INTR_31_0):** Combined PCI interrupt record for PCI_31_0.

14.5.1.102 PCI Interrupt1 (PCE_INTR_REG_1) — Offset 405002B4h

Combined interrupt status for each PCI functiion. This register is RO for the FW to identify the function where the interrupt status is set.

Type	Size	Offset	Default
MMIO	32 bit	405002B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO	**PCI Interrupt Record For PCI_36_32 (PCE_INTR_36_32):** Combined PCI interrupt record for PCI_36_32.

14.5.1.103 D0I3 Interrupt0 (ADR_D0I3_INTR_0_REG) — Offset 405002B8h

Status for individual D0i3 cip for each function.

Type	Size	Offset	Default
MMIO	32 bit	405002B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**D0i3 CIP Interrupt Status For PCI Function_31_0 (D0I3_INTR_0_STATUS):** D0i3 CIP interrupt status for PCI Function_31_0.

14.5.1.104 D0I3 Interrupt1 (ADR_D0I3_INTR_1_REG) — Offset 405002BCh

Status for individual D0i3 cip for each function.

Type	Size	Offset	Default
MMIO	32 bit	405002BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/V	**D0i3 CIP Interrupt Status For PCI Function_35_32 (D0I3_INTR_1_STATUS):** D0i3 CIP interrupt status for PCI Function_35_32.

14.5.1.105 XTAL Clk Reg (PMU_XTAL_CLK_REQ_REG) — Offset 405002C0h

This register has the config bit for controlling ISH gclkreq for XTAL clk. This gclkreq goes to XTAL CDC to generate final XTAL clkreq. This register also contains Live status of gclkack for XTAL clk.

Type	Size	Offset	Default
MMIO	32 bit	405002C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**PMU_XTAL_CLK_REQ_RSVD0:** Reserved
1	0h RO	**Live Status Of XTAL Gclkack (PMU_XTAL_CLK_ACK):** Live status of XTAL gclkack.
0	0h RW	**Config Bit For XTAL Gclkreq (PMU_XTAL_CLK_REQ):** Controls gclkreq for XTAL clk.

14.5.1.106 PMU CLKOCK SWITCH INTR (PMU_CLK_SWITCH_INTR) — Offset 405002C4h

This register is an intrupt to ARM to wakes it up after clock switching.

Type	Size	Offset	Default
MMIO	32 bit	405002C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**INTR_PMU_SWITCH_MASK:** Interrupt mask for clock switch interrupt.
0	0h RW/1C	**INTR_PMU_SWITCH:** This interrupt is set when clock switching is done. This wakes up ARM from WFI after clock switching.

14.5.1.107 PMU VNNAON Metastability Fix Enable (PMU_VNNAON_METAFIX_EN_REG) — Offset 405002CCh

This register can be used to enable the fix for meta-stability issue found in the vnnaon_reduction feature. By default the fix will be enabled and can be disabled only if there are any issues found with the fix.

Type	Size	Offset	Default
MMIO	32 bit	405002CCh	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Reserved**
1	0h RO	**Reserved**
0	1h RW	**Vnnaon Meta-Stabiility Fix Enable (PMU_VNNAON_METAFIX_EN):** When set, this bit will enable the meta-stability fix in vnnaon reduction logic.

14.5.1.108 PLL Power Up Sequence (PLL_PUSEQ_REG) — Offset 405002D0h

This register can be used to enable the PLL (6GHz) clock.

Type	Size	Offset	Default
MMIO	32 bit	405002D0h	00020000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	000h RO	**PLL_PUSEQ_RSVD1:** Reserved
21	0h RO/V	**AFC Done Status (PMUREG_AFC_DONE):** Asserted high when Auto-Frequency calibration (AFC) of the VCO coarse-tuning capacitor bank is complete. Prior to lock, AFC must be completed, or afcovrden must be asserted.
20	0h RO/V	**Suspend Acknowledgment (PMUREG_SUSPEND_ACK):** 1: PLLcore can be put in suspend state 0: PLLcore is not ready to be put in suspend state.
19:18	0h RO	**PLL_PUSEQ_RSVD2:** Reserved
17	1h RW	**PLL Isolation Enable (FWEN_B):** Active Low. To Control PLL Isoation.
16	0h RW	**CRI Version (CRI_VERSION):** CRI master handshaking config 0: Gen1 1: Gen2.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**CRI Mode (CRI_MODE):** Non-CRI or CRI mode config signal 0 - Non CRI 1 - CRI.
14	0h RW	**125MHz Clock Divider Enable (CK125_EN):** If sets enable clock divider to generate the 125MHz clock from 6GHz PLL clock.
13	0h RW	**200MHz Clock Divider Enable (CK200_EN):** If sets enable clock divider to generate the 200MHz clock from 6GHz PLL clock.
12	0h RW	**400MHz Clock Divider Enable (CK400_EN):** If sets enable clock divider to generate the 400MHz clock from 6GHz PLL clock.
11	0h RW	**500MHz Clock Divider Enable (CK500_EN):** If sets enable clock divider to generate the 500MHz clock from 6GHz PLL clock.
10:5	00h RW	**Register Compensation Code (RCOMP):** Resistor compensation code, which by default is used to calibrate the internal CPR based bias generator. 0x28 nominal. The value corresponds to the number of 2022 Ohm CPR resistors required in parallel to equal 50 Ohms.
4	0h RW	**PLL Enable (PLL_EN):** If sets it enable the PLL.
3	0h RW	**Full Calibration Reset (FULL_CAL_RESET):** TDC calibration and AFC calilbration reset signal, PLL will perform a full calibration after PLL is enabled if i_fullcalreset_l has transitioned from low to high since previous PLL calibration.
2	0h RW	**Suspend Request (SUSPEND_REQ):** Sleep enable for retention latches. When this bit is enabled, retention latches are configured to retain it's state. Upon acknowledgement (pmureg_suspend_ack) from PLLcore, core power is shut down. Refclk will be available, until pmureg_suspend_ack status is sent back to common logic.
1	0h RW	**CRI Reset (CRI_RESET):** Rest for all of the registers in CRI slave unit. Active low.
0	0h RW	**DIV Reset (PLLDIV_RESET):** Divider reset. Active low.

14.5.1.109 PLL INTR (PLL_INT_REG) — Offset 405002D4h

This register captures the live status, fall edge,rise edge interrupt status and mask bits for the pll lock and divided clocks valid indication from the PLL.

Type	Size	Offset	Default
MMIO	32 bit	405002D4h	098C6318h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	1h RW	**PLL Unlock Rise Interrupt Mask (PMU_PLL_UNLOCK_RISE_INTR_MSK):** Set this bit is to mask the interrupt generation when PLL unlock flag is asserted.
26	0h RW/V	**PLL Unlock Rise Interrupt (PMU_PLL_UNLOCK_RISE_INTR):** This is interrupt to indicate that PLL Unlock flag is asserted.
25	0h RO/V	**PLL Unlock Live Status (PMU_PLL_UNLOCK_LIVE):** This bit captures the live status of PLL Unlock flag.
24	1h RW	**500MHz Clock Valid Fall Interrupt Mask (PMU_PLL_CK500_VALID_FALL_INTR_MSK):** Set this bit to mask the interrupt generation when 500MHz clock valid is de-asserted.
23	1h RW	**500MHz Clock Valid Rise Interrupt Mask (PMU_PLL_CK500_VALID_RISE_INTR_MSK):** Set this bit to mask the interrupt generation when 500MHz clock valid is asserted.
22	0h RW/V	**500MHz Clock Valid Fall Interrupt (PMU_PLL_CK500_VALID_FALL_INTR):** This is interrupt to indicate that 500MHz clock valid is de-asserted.
21	0h RW/V	**500MHz Clock Valid Rise Interrupt (PMU_PLL_CK500_VALID_RISE_INTR):** This is interrupt to indicate that 500MHz clock valid is asserted.
20	0h RO/V	**500MHz Clock Valid Live Status (PMU_PLL_CK500_VALID_LIVE):** This bit captures the live status of 500MHz clock valid signal.
19	1h RW	**400MHz Clock Valid Fall Interrupt Mask (PMU_PLL_CK400_VALID_FALL_INTR_MSK):** Set this bit to mask the interrupt generation when 400MHz clock valid is de-asserted.
18	1h RW	**400MHz Clock Valid Rise Interrupt Mask (PMU_PLL_CK400_VALID_RISE_INTR_MSK):** Set this bit to mask the interrupt generation when 400MHz clock valid is asserted.
17	0h RW/V	**400MHz Clock Valid Fall Interrupt (PMU_PLL_CK400_VALID_FALL_INTR):** This is interrupt to indicate that 400MHz clock valid is de-asserted.
16	0h RW/V	**400MHz Clock Valid Rise Interrupt (PMU_PLL_CK400_VALID_RISE_INTR):** This is interrupt to indicate that 400MHz clock valid is asserted.
15	0h RW/V	**400MHz Clock Valid Live Status (PMU_PLL_CK400_VALID_LIVE):** This bit captures the live status of 400MHz clock valid signal.
14	1h RW	**200MHz Clock Valid Fall Interrupt Mask (PMU_PLL_CK200_VALID_FALL_INTR_MSK):** Set this bit to mask the interrupt generation when 200MHz clock valid is de-asserted.
13	1h RW	**200MHz Clock Valid Rise Interrupt Mask (PMU_PLL_CK200_VALID_RISE_INTR_MSK):** Set this bit to mask the interrupt generation when 200MHz clock valid is asserted.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/V	**200MHz Clock Valid Fall Interrupt (PMU_PLL_CK200_VALID_FALL_INTR):** This is interrupt to indicate that 200MHz clock valid is de-asserted.
11	0h RW/V	**200MHz Clock Valid Rise Interrupt (PMU_PLL_CK200_VALID_RISE_INTR):** This is interrupt to indicate that 200MHz clock valid is asserted.
10	0h RO/V	**200MHz Clock Valid Live Status (PMU_PLL_CK200_VALID_LIVE):** This bit captures the live status of 200MHz clock valid signal.
9	1h RW	**125MHz Clock Valid Fall Interrupt Mask (PMU_PLL_CK125_VALID_FALL_INTR_MSK):** Set this bit to mask the interrupt generation when 125MHx clock valid is de-asserted.
8	1h RW	**125MHz Clock Valid Rise Interrupt Mask (PMU_PLL_CK125_VALID_RISE_INTR_MSK):** Set this bit to mask the interrupt generation when 125MHz clock valid is asserted.
7	0h RW/V	**125MHz Clock Valid Fall Interrupt (PMU_PLL_CK125_VALID_FALL_INTR):** This is interrupt to indicate that 125MHz clock valid is de-asserted.
6	0h RW/V	**125MHz Clock Valid Rise Interrupt (PMU_PLL_CK125_VALID_RISE_INTR):** This is interrupt to indicate that 125MHz clock valid is asserted.
5	0h RO/V	**125MHz Clock Valid Live Status (PMU_PLL_CK125_VALID_LIVE):** This bit captures the live status of 125MHz clock valid signal.
4	1h RW	**PLL Lock Fall Interrupt Mask (PMU_PLL_LOCK_FALL_INTR_MSK):** Set this bit to mask the interrupt generation when PLL lock is de-asserted.
3	1h RW	**PLL Lock Rise Interrupt Mask (PMU_PLL_LOCK_RISE_INTR_MSK):** Set this bit to mask the interrupt generation when PLL lock is asserted.
2	0h RW/V	**PLL Lock Fall Interrupt (PMU_PLL_LOCK_FALL_INTR):** This is interrupt to indicate that PLL Lock is de-asserted.
1	0h RW/V	**PLL Lock Rise Interrupt (PMU_PLL_LOCK_RISE_INTR):** This is interrupt to indicate that PLL Lock is asserted.
0	0h RO/V	**PLL Lock Live Status (PMU_PLL_LOCK_LIVE):** This bit captures the live status of PLL Lock.

14.5.1.110 ISH UART IDLE Mask (ADR_PMU_UART_IDLE_MASK_REG) — Offset 405002D8h

When set PMU does not look for uart idle condition to initiate low power flow.

Type	Size	Offset	Default
MMIO	32 bit	405002D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**UART Mask Idle (PMU_UART_IDLE_MASK):** If set enable the mask for UART idle interrupt.

14.5.1.111 PMU_TCG_EXIT_INTR_REG — Offset 405002DCh

PMU TCG EXIT Interrupt register.

Type	Size	Offset	Default
MMIO	32 bit	405002DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**PMU TCG Exit Interrupt Exit Mask (PMU_TCG_EXIT_INTR_MASK):** If set enable the mask for PMU TCG exit interrupt.
0	0h RW/1C	**TCG Exit Interrupt (PMU_TCG_EXIT_INTR):** It records PMU the TCG exit interrupt.

14.5.1.112 Address D3 Live Status0 (ADR_D3_STATUS_0_REG) — Offset 405002E0h

D3 live status for all 36 PCI functions.

Type	Size	Offset	Default
MMIO	32 bit	405002E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**D3 Status (ADR_D3_STATUS_0):** D3 status register for PCI functions 31 to 0.

14.5.1.113 Address D3 Live Status1 (ADR_D3_STATUS_1_REG) — Offset 405002E4h

D3 live status for all 36 PCI functions.

Type	Size	Offset	Default
MMIO	32 bit	405002E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO/V	**D3 Status (ADR_D3_STATUS_1):** D3 status register for PCI functions 36 to 32.

14.5.1.114 D0i3 Bit2 Status0 (ADR_D0I3_BIT2_STATUS_0_REG) — Offset 405002E8h

D0i3 live value from D0i3 MMIO block for all PCI functions.

Type	Size	Offset	Default
MMIO	32 bit	405002E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**D0I3_BIT2_STATUS_0:** D0i3 BIT2 Status register for PCI functions 31 to 0.

14.5.1.115 D0i3 Bit2 Status1 (ADR_D0I3_BIT2_STATUS_1_REG) — Offset 405002ECh

D0i3 live value from D0i3 MMIO block for all PCI functions.

Type	Size	Offset	Default
MMIO	32 bit	405002ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO/V	**D0i3 Bit2 Status (D0I3_BIT2_STATUS_1):** D0i3 BIT2 Status register for PCI functions 36 to 32.

14.5.1.116 D0i3 Bit0 Status0 (ADR_D0I3_BIT0_STATUS_0_REG) — Offset 405002F0h

When CIP bits per function(or it could be the live CIP value of that function) get sets, corresponding bits per function in this register also gets set to 1. FM will clear that bit by writing 1 to that particular function bit number. On clearing of this bit number PMU HW will assert the D0i3_req for that particular function number.

Type	Size	Offset	Default
MMIO	32 bit	405002F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**D0I3_BIT0_STATUS_0:** D0i3 BIT0 Status register for PCI functions 31 to 0.

14.5.1.117 D0i3 Bit0 Status1 (ADR_D0I3_BIT0_STATUS_1_REG) — Offset 405002F4h

When CIP bits per function(or it could be the live CIP value of that function) get sets, corresponding bits per function in this register also gets set to 1. FM will clear that bit by writing 1 to that particular function bit number. On clearing of this bit number PMU HW will assert the D0i3_req for that particular function number.

Type	Size	Offset	Default
MMIO	32 bit	405002F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/V	**D0i3 Bit0 Status (D0I3_BIT0_STATUS_1):** D0i3 BIT0 Status register for PCI functions 36 to 32.

14.5.1.118 D0i3 Interrupt Mask 0 (ADR_D0I3C_INTR_STATUS_CLR_MSK_0_REG) — Offset 405002F8h

Mask register for ADR_D0I3_INTR_0_REG.

Type	Size	Offset	Default
MMIO	32 bit	405002F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**D0I3_MASK_0:** If sets enable the mask for D0i3 Interrupt for PCI functions 31 to 0.

14.5.1.119 D0i3 Interrupt Mask 1 (ADR_D0I3C_INTR_STATUS_CLR_MSK_1_REG) — Offset 405002FCh

Mask register for ADR_D0I3_INTR_1_REG.

Type	Size	Offset	Default
MMIO	32 bit	405002FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/V	**D0i3 Interrupt Mask 1 (D0I3_MASK_1):** If sets enable the mask for D0i3 Interrupt for PCI functions 36 to 32.

14.5.1.120 Power Status (PMU_PWR_ST_REG) — Offset 40500F00h

This register will give indication of whether it is a cold boot/Sx exit, or IP accessible PG exit with ISH in D0i2 or D0i3, with platform in S0 or Sx. ISH ROM FW is expected to read this register, during boot.

Type	Size	Offset	Default
MMIO	32 bit	40500F00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000000h RW	**FW Status/Track (PWR_ST_FW_ST_TRACK):** This field is reserved for ISH FW to place any information which aids in the exit flow.
4	0h RW	**IP Accessible PG (PWR_ST_IPAPG):** This field indicates if ISH was in an IP accessible PG state prior to this wake. 1: Yes 0: No.
3:2	0h RW	**S State (PWR_ST_S_STATE):** This field indicates the state in which platform was, prior to this wake. 00: S0/s0ix 01: Sx.
1:0	0h RW	**D0ix State (PWR_ST_D0IX_STATE):** This field indicates the state in which the ISH was in, prior to this wake. 00: D0i0-Uninitialized 01: D0i1 10: D0i2 11: D0i3.

14.5.1.121 IPAPG Scrath-Pad0 (IPAPG_SC_PAD0) — Offset 40500F04h

This register will give additional register bits for FW to store information which could make FW implementation easier and cleaner otherwise. e.g. it could store a NONCE value in AON and this scratchpad before entering IPAPG state and upon exit could compare for match to ensure that there were no exceptions.

Type	Size	Offset	Default
MMIO	32 bit	40500F04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FW Scratch Pad Register0 (IPAPG_SC_PAD0):** Scratch pad for the FW.

14.5.1.122 IPAPG Scratch-Pad1 (IPAPG_SC_PAD1) — Offset 40500F08h

This register will give additional register bits for FW to store information which could make FW implementation easier and cleaner otherwise. e.g. it could store a NONCE value in AON and this scratchpad before entering IPAPG state and upon exit could compare for match to ensure that there were no exceptions.

Type	Size	Offset	Default
MMIO	32 bit	40500F08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FW Scratch Pad Register1 (IPAPG_SC_PAD1):** Scratch pad for the FW.

14.5.1.123 IP Accessible PG Enable (IPAPG_EN_REG) — Offset 40500F10h

Before executing HALT, ISH FW is expected to set this bit to indicate to PMU if IP accessible PG needs to be enabled while entering D0i2 / D0i3 (along with RF_ROM_PG_EN, 0x30h).

Type	Size	Offset	Default
MMIO	32 bit	40500F10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW/1C	**IPAPG Exit Completed (IPAPG_EXIT_INDICATION):** This bit, when set by ISH HW, indicates that ISH HW has completed IPAPG exit sequence. Note that ISH FW/ROM could be out of reset prior to completion of the IPAPG sequence. This bit is to be polled by ISH ROM, if exiting IPAPG state, before boot sequence can be initiated. ISH FW will write 1 to clear this status bit.
7:1	0h RO	**Reserved**
0	0h RW	**IP Accessible PG Enable (IPAPG_EN):** This bit, when set indicates that ISH FW should enter into IP accessible PG state, while entering D0ix state (which is controlled by other PMU registers for TCG, RF_ROM PG, etc.).

14.5.1.124 SW PG REQ Interrupt (SW_PG_REQ_INTR) — Offset 40500F14h

This register captures the live status, fall edge,rise edge interrupt status and mask bits for the pmc_ish_sw_pg_req_b indication from the PMC.

Type	Size	Offset	Default
MMIO	32 bit	40500F14h	00000018h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	1h RW	**Sw_pg_req_b_falledge' INTR Mask Bit. (SW_PG_REQ_FALL_INTR_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable sw_pg_req_b_falledge interrupt to ILB 1 - disable sw_pg_req_b_falledge interrupt to ILB.
3	1h RW	**Sw_pg_req_b_riseedge' INTR Mask Bit (SW_PG_REQ_RISE_INTR_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable sw_pg_req_b_riseedge interrupt to ILB 1 - disable sw_pg_req_b_riseedge interrupt to ILB.
2	0h RW/1C	**Sw_pg_req_b_falledge' INTR Status Bit (SW_PG_REQ_FALL_INTR_STATUS):** This is bit is set by HW whenever a fall edge is detected in the 'pmc_ish_sw_pg_req_b' signal. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every fall edge to receive an interrupt on the next fall edge. Note to ISH FW: This bit indicates that PMC is allowing entry into IPAPG state. Note that this bit will be set irrespective of which D0ix state ISH is in. ISH FW needs to keep this interrupt masked by setting bit[4] of this register to 1, if this event notification is not needed.
1	0h RW/1C	**Sw_pg_req_b_riseedge' INTR Status Bit (SW_PG_REQ_RISE_INTR_STATUS):** This is bit is set by HW whenever a rise edge is detected in the 'pmc_ish_sw_pg_req_b' signal. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every rise edge to receive an interrupt on the next rise edge. Note to ISH FW: This bit indicates that PMC wants ISH to get out of IPAPG state. Note that this bit will be set irrespective of whether ISH is in IPAPG state or not. ISH FW needs to keep this interrupt masked by setting bit[3] of this register to 1.
0	0h RO	**Pmc_ish_sw_pg_req_b Live Status (SW_PG_REQ_B_ASSERTED):** Reflects the live value of pmc_ish_sw_pg_req_b. 1- pmc_ish_sw_pg_req_b is de-asserted. 0- pmc_ish_sw_pg_req_b is asserted.

14.5.1.125 ISH PMC WAKE INTR (PMC_WAKE_INT_REG) — Offset 40500F18h

This register captures the live status, fall edge,rise edge interrupt status and mask bits for the pmc_ish_pg_wake indication from the PMC.

Type	Size	Offset	Default
MMIO	32 bit	40500F18h	00000018h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	1h RW	**Pmc_wake_falledge' INTR Mask Bit (PMU_PMC_WAKE_FALL_INT_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable pmc_wake_falledge interrupt to ILB 1 - disable pmc_wake_falledge interrupt to ILB.
3	1h RW	**Pmc_wake_riseedge' INTR Mask Bit (PMU_PMC_WAKE_RISE_INT_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable pmc_wake_riseedge interrupt to ILB 1 - disable pmc_wake_riseedge interrupt to ILB.
2	0h RW/1C	**Pmc_wake_falledge' INTR Status Bit (PMU_PMC_WAKE_FALL_INT):** This is bit is set by HW whenever a fall edge is detected in the 'pmc_ish_pg_wake' signal. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every fall edge to receive an interrupt on the next fall edge. Note to ISH FW: This bit indicates that PMC is allowing ISH to get into IPAPG state. Note that this bit will be set irrespective of whether ISH is in IPAPG state or not. ISH FW needs to keep this interrupt masked by setting bit[4] of this register to 1.
1	0h RW/1C	**Pmc_wake_riseedge' INTR Status Bit (PMU_PMC_WAKE_RISE_INT):** This is bit is set by HW whenever a rise edge is detected in the 'pmc_ish_pg_wake' signal. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every rise edge to receive an interrupt on the next rise edge. Note to ISH FW: This bit indicates that PMC wants ISH to get out of IPAPG state. Note that this bit will be set irrespective of whether ISH is in IPAPG state or not. ISH FW needs to keep this interrupt masked by setting bit[3] of this register to 1.
0	0h RO	**Pmc_ish_pg_wake' Live Status Register (PMU_PMC_WAKE_LIVE):** Reflects the live value of pmc_ish_pg_wake. 1- pmc_ish_pg_wake is asserted. 0- pmc_ish_pg_wake is de-asserted.

14.5.1.126 ISH BRIDGEISOL CTL(Supported Only When There Is Sx Usage) (PMU_BRISOLCTL_REG) — Offset 40500F24h

This register captures the live status, fall edge,rise edge interrupt status and mask bits for the rst_isol_ack signal from IOSF2OCP bridge along with the bit to drive the br_isol_req to the IOSF2OCP bridge.

Type	Size	Offset	Default
MMIO	32 bit	40500F24h	00000030h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RO	**RSV:** Reserved
5	1h RW	**Br_rst_isol_ack_fall' INTR Mask Bit (PMU_BR_ISOL_ACK_FALL_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable br_rst_isol_ack_fall interrupt to ILB 1 - disable br_rst_isol_ack_fall interrupt to ILB.
4	1h RW	**Br_rst_isol_ack_rise' INTR Mask Bit (PMU_BR_ISOL_ACK_RISE_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable br_rst_isol_ack_rise interrupt to ILB 1 - disable br_rst_isol_ack_rise interrupt to ILB.
3	0h RW/1C	**Br_rst_isol_ack_fall' INTR Status Bit (PMU_BR_ISOL_ACK_FALL):** This bit is set by HW whenever a fall edge is detected in the 'br_rst_isol_ack' signal. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every fall edge to receive an interrupt on the next fall edge. Note to ISH FW: This bit indicates that the br_rst_isol_ack has been de-asserted.
2	0h RW/1C	**Br_rst_isol_ack_rise' INTR Status Bit (PMU_BR_ISOL_ACK_RISE):** This bit is set by HW whenever a rise edge is detected in the 'br_rst_isol_ack' signal. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every rise edge to receive an interrupt on the next rise edge. Note to ISH FW: This bit indicates that the br_rst_isol_ack has been asserted and the reset isolation in the bridge is completed.
1	0h RO	**Bridge Host Reset Isolation Acknowledge (BR_ISOL_ACK) (PMU_BR_ISOL_ACK):** This bit provides ISH FW visibility onto the state of the internal signal from the IOSF2OCP bridge which acts as an acknowledge to the signal from the BR_ISOL_REQ bit below. Behavior: 1: signal is active - Bridge is acknowledging having entered Host reset isolation mode 0 (default): signal is inactive.
0	0h RW/1S	**Bridge Host Reset Isolation Request (BR_ISOL_REQ) (PMU_BR_ISOL_REQ):** This bit drives an internal ISH signal to the IOSF2OCP Bridge which acts as a request for the Bridge to enter its Host partition reset regime, thereby isolating it in preparation of host_prim_rst_b assertion. Note that ISH HW will auto-clear this bit upon the assertion of host_rst_b signal. ISH HW also ensures that this bit is cleared at least 3 clocks AFTER the assertion event of host_rst_b. Behavior: 1: signal is active - Bridge is requested to enter Host reset isolation mode 0 (default): signal is inactive no change in Bridge state requested.

14.5.1.127 CDC Config Clock Gate Disable(Required Only During Sx Usage) (PMU_CDCCGDIS_REG) — Offset 40500F28h

The clock gate disable register is required for Sx support in CNL SOC. The FW is expected to program bit 0 of this register before bootprep ack is sent until the hostprim reset is de-asserted.

Type	Size	Offset	Default
MMIO	32 bit	40500F28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:0	00000h RW	**ISH CDC Config Clkgate Disable Register (CDCCGDIS):** The clock gate disable register is required for Sx support in CNL SOC. The FW is expected to program bit 0 of this register before bootprep ack is sent until the hostprim reset is de-asserted.

14.5.1.128 PCE ISH FW Local (PMU_PCE_LOCAL_REG) — Offset 40500F30h

This register is the local version of PCI.PCE register. It is the responsibility of ISH FW to keep this register contents coherent to PCI. PCE register (as indicated by PCE SHADOW register). ISH HW will use the contents of this register for all IPAPG decisions.

Type	Size	Offset	Default
MMIO	32 bit	40500F30h	00000200h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	1h RW	**PCE Change Detect Interrupt Mask (PMU_PCE_CHG_DETECT_INTR_MASK):** This is set by FW when FW doesn t want to generate interrupt to ILB. 0 - enable PCE Change Detected interrupt to ILB 1 - disable PCE Change Detected interrupt to ILB.
8	0h RW/1C	**PCE Change Detect Interrupt Status (PMU_PCE_CHG_DETECT_INTR):** This is bit is set by HW whenever any change in value of PCE SHADOW REGISTER is detected. This bit will also be tied to the IOAPIC RTE entry in iLB as interrupt source to Minute IA. FW needs to clear this bit after every receiving an interrupt.
7:5	0h RO	**Reserved**
4	0h RW	**Hardware Autonomous Enable (HAE) (PMU_PCE_HAE_LOCAL):** If set, then the PGCB may request a PG whenever it is idle. NOTE: If this bit is set, then bits [2:0] must be 000 .

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Sleep Enable (SE) (PMU_PCE_SLEN_LOCAL):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
2	0h RW	**D3Hot Enable (D3HEN) (PMU_PCE_D3HEN_LOCAL):** If 1 , then function will request power gating when idle and the PMCSR[1:0] register in the function = 11 (D3).
1	0h RW	**IDLE Enable (IDLEN) (PMU_PCE_IDLEEN_LOCAL):** If 1 , then the function will request power gating when idle and the DEVIDLEC register (DEVIDLEC[DEVIDLE] = 1) is set. This bit should be RO if DEVIDLEC capability is not implemented. .
0	0h RW	**PMC Request Enable (PMCRE) (PMU_PCE_PMCRE_LOCAL):** If this bit is set to 1 , the function will request power gating when idle and pmc_ip_sw_pg_req_b = 0 . NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific. .

14.5.1.129 ISH SRAM Bitline Float Enable (ADR_SRAM_SLEEPB) — Offset 40500F34h

SRAM_SLEEPB.

Type	Size	Offset	Default
MMIO	32 bit	40500F34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:0	0000000h RW	**PMU SRAM B Sleep (PMU_SRAM_SLEEPB):** Register for PMU sram B Sleep. Active low.

14.5.1.130 ISH SRAM Array Sleep Enable (ADR_SRAM_ARSLEEP) — Offset 40500F38h

SRAM_ARSLEEP.

Type	Size	Offset	Default
MMIO	32 bit	40500F38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:0	0000000h RW	**PMU Sram AR Sleep (PMU_SRAM_ARSLEEP):** Register for PMU sram AR Sleep . Active low.

14.5.1.131 IP In-Accessible PG Exit Status (IPIAPG_EN_REG) — Offset 40500F40h

This register indicates IP In-Accessible exit status for RTSS. This is used as RTSS ready indication.

Type	Size	Offset	Default
MMIO	32 bit	40500F40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**IPIAPG Exit Complete (IPIAPG_EXIT_INDICATION):** When set this bit indicates RTSS ip-inaccessible PG exit completion, which will be used as RTSS ready indication.

14.6 CCU Registers

CCU Registers	Address Offset	Table
CCU	40600000h - 406000DCh	Table 14-16

14.6.1 CCU Registers Summary

Table 14-16. Summary of CCU Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40600000h	4	Trunk Clock Gate (TRUNK_CG)	0000FFFEh
40600004h	4	Block Level Clock Gate (BLK_CG)	00000000h
40600008h	4	Block Level Clock Gate- UART (UART_BLK_CG)	00000000h
4060000Ch	4	Block Level Clock Gate- I2C (I2C_BLK_CG)	00000000h
40600010h	4	Block Level Clock Gate- SPI (SPI_BLK_CG)	00000000h
40600014h	4	Block Level Clock Gate- GPIO (GPIO_BLK_CG)	00000000h
40600018h	4	Block Level Clock Gate- I2S (I2S_BLK_CG)	00000000h
40600020h	4	Block Level Clock Gate- SRAM (SRAM_BLK_CG)	00000000h
40600024h	4	Block Level Clock Gate- QEP (QEP_BLK_CG)	00000000h
40600028h	4	Block Level Clock Gate- DMA (DMA_BLK_CG)	00000000h
4060002Ch	4	Block Level Clock Gate- PWM (PWM_BLK_CG)	00000000h
40600034h	4	Block Level Clock Gate- CANBUS (CANBUS_BLK_CG)	00000000h
4060003Ch	4	Reset History (RST_HIS)	00000000h
40600040h	4	Trunk Gate Disable (TRUNK_CG_DIS)	00000001h
40600044h	4	Block Gate Disable (BLK_CG_DIS)	00000001h
40600048h	4	Soft Reset (SOFT_RST)	00000000h
4060004Ch	4	Soft Reset- UART (UART_SOFT_RST)	00000000h
40600050h	4	Soft Reset- I2C (I2C_SOFT_RST)	00000000h
40600054h	4	Soft Reset- SPI (SPI_SOFT_RST)	00000000h
40600058h	4	Soft Reset- GPIO (GPIO_SOFT_RST)	00000000h
4060005Ch	4	Soft Reset- I2S (I2S_SOFT_RST)	00000000h
40600064h	4	Soft Reset- SRAM (SRAM_SOFT_RST)	00000000h
40600068h	4	Soft Reset- QEP (QEP_SOFT_RST)	00000000h
4060006Ch	4	Soft Reset- PWM (PWM_SOFT_RST)	00000000h
40600074h	4	Soft Reset- CANBUS (CANBUS_SOFT_RST)	00000000h
4060007Ch	4	Clock Divider WD (CKDIV_WD)	00000001h
40600080h	4	Clock Divider LDO (CKDIV_LDO)	00000005h
40600084h	4	Global Reset (GLBL_RST_EN)	00000000h
40600088h	4	Trunk Clock Gate Status (TCG_STS_REG)	00000000h
4060008Ch	4	Soft Reset- DMA (DMA_SOFT_RST)	00000000h
40600090h	4	Block Level Clock Gate- GBE (GBE_BLK_CG)	00000000h
40600094h	4	Soft Reset GBE (GBE_SOFT_RST)	00000000h
40600098h	4	Trunk Clock Gate Rise Interrupt Mask (TCG_CLKACK_RISE_INTR_MASK)	00000000h
4060009Ch	4	Trunk Clock Gate Fall Interrupt Mask (TCG_CLKACK_FALL_INTR_MASK)	00000000h
406000A8h	4	HBW_CLK_SEL Reg (HBW_CLK_SEL)	00000000h
406000B0h	4	M Value M/N Divide- I2S0 (I2S0_MNDIV_M_VALUE)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
406000B4h	4	N Value M/N Divide- I2S0 (I2S0_MNDIV_N_VALUE)	00000000h
406000B8h	4	Enable - M/N Divide- I2S0 (I2S0_MNDIV_ENABLE)	00000000h
406000BCh	4	M Value M/N Divide- I2S1 (I2S1_MNDIV_M_VALUE)	00000000h
406000C0h	4	N Value M/N Divide- I2S1 (I2S1_MNDIV_N_VALUE)	00000000h
406000C4h	4	Enable - M/N Divide- I2S1 (I2S1_MNDIV_ENABLE)	00000000h
406000C8h	4	Soft Reset TGPIO (TGPIO_SOFT_RST)	00000000h
406000CCh	4	Block Level Clock Gate TGPIO (TGPIO_BLK_OCPCG)	00000000h
406000D0h	4	Trunk Clock Gate Rise Interrupt Status (TCG_CLKACK_RISE_INTR_STS)	00000000h
406000D4h	4	Trunk Clock Gate Fall Interrupt Status (TCG_CLKACK_FALL_INTR_STS)	00000000h
406000D8h	4	CORE_CLK_SEL Reg (CORE_CLK_SEL)	00000000h
406000DCh	4	AON Clock Gate Enable (AON_CG_EN)	00000100h

14.6.1.1 Trunk Clock Gate (TRUNK_CG) — Offset 40600000h

Register for enabling trunk clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600000h	0000FFFEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW	**TCG_GBE2_RGMII_PHY_RX:** 1 initiates trunk clock gating, 0 no clock gating for GBE2_RGMII_PHY_RX clock.
14	1h RW	**TCG_GBE1_RGMII_PHY_RX:** 1 initiates trunk clock gating, 0 no clock gating for GBE1_RGMII_PHY_RX clock.
13	1h RW	**TCG_GBE2_SGMII_PHY_RX:** 1 - initiates trunk clock gating, 0 no clock gating for GBE2_SGMII_PHY_RX clock.
12	1h RW	**TCG_GBE1_SGMII_PHY_RX:** 1 - initiates trunk clock gating, 0 no clock gating for GBE1_SGMII_PHY_RX clock.
11	1h RW	**TCG_GBE2_SGMII_REF:** 1 - initiates trunk clock gating, 0 no clock gating for GBE2_SGMII_REF clock.
10	1h RW	**TCG_GBE1_SGMII_REF:** 1 - initiates trunk clock gating, 0 no clock gating for GBE1_SGMII_REF clock.
9	1h RW	**TCG_GBE2_RGMII_TX:** 1 - initiates trunk clock gating, 0 no clock gating for GBE2_RGMII_TX clock.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**TCG_GBE1_RGMII_TX:** 1 - initiates trunk clock gating, 0 no clock gating for GBE1_RGMII_TX clock.
7	1h RW	**TCG_GBE_PTP:** 1 - initiates trunk clock gating, 0 no clock gating for GBE_PTP clock.
6	1h RW	**TCG_PLL_PTP:** 1 - initiates trunk clock gating, 0 no clock gating for PLL_PTP clock.
5	1h RW	**Reserved**
4	1h RW	**Reserved**
3	1h RW	**TCG_LCPLL_REF:** 1 initiates trunk clock gating, 0 no clock gating for LCPLL_REF clock.
2	1h RW	**TCG_MAIN:** 1 initiates trunk clock gating, 0 no clock gating for MAIN clock.
1	1h RW	**TCG_CPU_FAST:** 1 initiates trunk clock gating, 0 no clock gating for CPU_FAST clock.
0	0h RW	**TCG_S0IX_XTAL:** 1 initiates trunk clock gating, 0 no clock gating for S0IX_XTAL clock.

14.6.1.2 Block Level Clock Gate (BLK_CG) — Offset 40600004h

Register for enabling block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**HPET Clock Gate Register (CCU_HPET_CG):** ILB-HPET clock gating register. 1-Clock gate ILB-HPET 0-No ILB-HPET clock gating.
0	0h RO	**Reserved**

14.6.1.3 Block Level Clock Gate- UART (UART_BLK_CG) — Offset 40600008h

Register for enabling UART block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**Block Levell Gate Enable - UART (CCUREG_UART_CG):** UART Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.4 Block Level Clock Gate- I2C (I2C_BLK_CG) — Offset 4060000Ch

Register for enabling I2C block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	4060000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Block Levell Gate Enable - I2C (CCUREG_I2C_CG_INT):** I2C Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.5 Block Level Clock Gate- SPI (SPI_BLK_CG) — Offset 40600010h

Register for enabling SPI block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**Block Levell Gate Enable - SPI (CCUREG_SPI_CG):** SPI Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.6 Block Level Clock Gate- GPIO (GPIO_BLK_CG) — Offset 40600014h

Register for enabling GPIO block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Block Levell Gate Enable - GPIO (CCUREG_GPIO_CG):** GPIO clock gating register. 1-Clock gate GPIO 0-No GPIO clock gating.

14.6.1.7 Block Level Clock Gate- I2S (I2S_BLK_CG) — Offset 40600018h

Register for enabling I2S block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Block Levell Gate Enable - I2S (CCUREG_I2S_CG):** Reserved

14.6.1.8 Block Level Clock Gate- SRAM (SRAM_BLK_CG) — Offset 40600020h

Register for enabling SRAM block level clock gating for L2 Bank.

Type	Size	Offset	Default
MMIO	32 bit	40600020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Block Levell Gate Enable - SRAM (CCUREG_SRAM_CG):** SRAM Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.9 Block Level Clock Gate- QEP (QEP_BLK_CG) — Offset 40600024h

Register for enabling QEP block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**Block Levell Gate Enable - QEP (CCUREG_QEP_CG):** QEP Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.10 Block Level Clock Gate- DMA (DMA_BLK_CG) — Offset 40600028h

Register for enabling DMA block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**Block Level Clock Gating Register - DMA (CCUREG_DMA_CG):** DMA clock gating register. 1-Clock gate DMA 0-No DMA clock gating.

14.6.1.11 Block Level Clock Gate- PWM (PWM_BLK_CG) — Offset 4060002Ch

Register for enabling PWM block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	4060002Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Block Levell Gate Enable - PWM (CCUREG_PWM_CG):** PWM Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.12 Block Level Clock Gate- CANBUS (CANBUS_BLK_CG) — Offset 40600034h

Register for enabling CANBUS block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Block Levell Gate Enable - CANBUS (CCUREG_CANBUS_CG):** CANBUS Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.13 Reset History (RST_HIS) — Offset 4060003Ch

Reset history register.

Type	Size	Offset	Default
MMIO	32 bit	4060003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/1C	**Reset History For SRECC (CCUREG_SRAMECC_RST_HIST):** Used to indicate SRECC reset 1-indicates SRECC reset 0-No SRECC reset.
2	0h RW/1C	**Reset History For MIASS (CCUREG_MIASS_RST_HIST):** Used to indicate MIASS reset 1-indicates MIASS reset 0-No MIASS reset.
1	0h RW/1C	**Reset History For WD (CCUREG_WD_RESET_HIST):** Used to indicate WD reset 1-indicates WD reset 0-No WD reset.
0	0h RW/1C	**Reset History For SW (CCUREG_SW_RESET_HIST):** Used to indicate SW reset 1-indicates SW reset 0-No SW reset.

14.6.1.14 Trunk Gate Disable (TRUNK_CG_DIS) — Offset 40600040h

Register for disabling the trunk clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600040h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RW	**Trunk Clock Gate Disable (CCUREG_TRUNK_CG_DIS):** Used to disable ISH trunk level clock gating. Note- (Ref. Sighting 4796578) When this bit is set, this will disable only the toggling of clk_req/clk_ack signals. Clock gating of internal blocks are disabled only by the Block Gate Disable register (0x3C). 1-disable ISH trunk level clock gating (keep clk_req always on) 0-enable trunk level clock gating.

14.6.1.15 Block Gate Disable (BLK_CG_DIS) — Offset 40600044h

Register for disabling the block gate gating.

Type	Size	Offset	Default
MMIO	32 bit	40600044h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Checker Bit Choosing Async Path (ASYNC_PATH):** Choosing async path during 400/200 clk mode.
7:2	0h RO	**Reserved**
1	0h RW	**Wdt Clk Gating Disable (WDT_CG_DIS):** Setting this bit to 1 - disables wdt clk gating when CORE is halted, 0 enables wdt clk gating.
0	1h RW	**Block Level Clock Gate Disable (CCU_REG_INT_CG_DIS):** Used to disable ISH internal clock gating 1-Disable ISH clock block clock gating0-Enable ISH block clock gating.

14.6.1.16 Soft Reset (SOFT_RST) — Offset 40600048h

Register for enabling the soft reset.

Type	Size	Offset	Default
MMIO	32 bit	40600048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**Soft Reset Enable - ILB (CCUREG_ILB_RST):** ILB soft reset bit. 1-Reset asserted 0-Reset de-asserted.
1	0h RW	**Soft Reset Enable - OCP Bridge (CCUREG_OCP_BRIDGE_RST):** OCP_BRIDGE soft reset bit. 1-Reset asserted 0-Reset de-asserted.
0	0h RW	**Soft Reset Enable - WD (CCUREG_WD_RST):** WD soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.17 Soft Reset- UART (UART_SOFT_RST) — Offset 4060004Ch

Register for Soft Reset of UART.

Type	Size	Offset	Default
MMIO	32 bit	4060004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**Soft Reset Enable - UART (CCUREG_UART_RST):** Soft reset bit for UART. 1-Reset asserted 0-Reset de-asserted.

14.6.1.18 Soft Reset- I2C (I2C_SOFT_RST) — Offset 40600050h

Register for Soft Reset of I2C.

Type	Size	Offset	Default
MMIO	32 bit	40600050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Soft Reset Enable - I2C (CCUREG_I2C_RST_INT):** I2C soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.19 Soft Reset- SPI (SPI_SOFT_RST) — Offset 40600054h

Register for Soft Reset of SPI.

Type	Size	Offset	Default
MMIO	32 bit	40600054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**Soft Reset Enable - SPI (CCUREG_SPI_RST):** SPI soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.20 Soft Reset- GPIO (GPIO_SOFT_RST) — Offset 40600058h

Register for Soft Reset of GPIO.

Type	Size	Offset	Default
MMIO	32 bit	40600058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Soft Reset Enable - GPIO (CCUREG_GPIO_RST):** GPIO soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.21 Soft Reset- I2S (I2S_SOFT_RST) — Offset 4060005Ch

Register for Soft Reset of I2S.

Type	Size	Offset	Default
MMIO	32 bit	4060005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Soft Reset Enable - I2S (CCUREG_I2S_RST):** Reserved

14.6.1.22 Soft Reset- SRAM (SRAM_SOFT_RST) — Offset 40600064h

Register for Soft Reset of SRAM.

Type	Size	Offset	Default
MMIO	32 bit	40600064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Soft Reset Enable - SRAM (CCUREG_SRAM_RST):** Sram soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.23 Soft Reset- QEP (QEP_SOFT_RST) — Offset 40600068h

Register for Soft Reset of QEP.

Type	Size	Offset	Default
MMIO	32 bit	40600068h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**Soft Reset Enable - QEP (CCUREG_QEP_RST):** QEP soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.24 Soft Reset- PWM (PWM_SOFT_RST) — Offset 4060006Ch

Register for Soft Reset of PWM.

Type	Size	Offset	Default
MMIO	32 bit	4060006Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Soft Reset Enable - PWM (CCUREG_PWM_RST):** PWM soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.25 Soft Reset- CANBUS (CANBUS_SOFT_RST) — Offset 40600074h

Register for Soft Reset of CANBUS.

Type	Size	Offset	Default
MMIO	32 bit	40600074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Soft Reset Enable - CANBUS (CCUREG_CANBUS_RST):** CANBUS soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.26 Clock Divider WD (CKDIV_WD) — Offset 4060007Ch

Register for enabling the clock divider - WD.

Type	Size	Offset	Default
MMIO	32 bit	4060007Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RW	**Div Ratio For WDT Clock (CCUREG_CLKDIV_WD):** Divide ratio to generate WDT clock from PERI clock.

14.6.1.27 Clock Divider LDO (CKDIV_LDO) — Offset 40600080h

Register for enabling the clock divider - LDO.

Type	Size	Offset	Default
MMIO	32 bit	40600080h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	5h RW	**Div Ratio For LDO (CCUREG_CLKDIV_LDO):** Divide ratio for LDO.

14.6.1.28 Global Reset (GLBL_RST_EN) — Offset 40600084h

Register for enabling the global reset.

Type	Size	Offset	Default
MMIO	32 bit	40600084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**Global Reset Enable (CCUREG_GLBL_RST_EN):** Unused in GLV. Global reset enable register These bits enable (when set) and disable (when cleared) the indication to PMC for initiating global reset on the following conditions: Bit[0] Enable for IPC/SW reset assertion. Bit[1] Enable for MIA sub system shutdown. Bit[2] Enable for fabric interrupt. Bit[3] Enable for fabric UR. .

14.6.1.29 Trunk Clock Gate Status (TCG_STS_REG) — Offset 40600088h

TCG Status bits for various clocks. If set to 1, clk is gated. The status is cleared when clkack for respective clks are high. Each bit is for the clks related to the respective bit in TCG register.

Type	Size	Offset	Default
MMIO	32 bit	40600088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**TCG_STS_GBE2_RGMII_PHY_RX:** TCG_STS_GBE2_RGMII_PHY_RX field.
14	0h RO/V	**TCG_STS_GBE1_RGMII_PHY_RX:** TCG_STS_GBE1_RGMII_PHY_RX field.
13	0h RO/V	**TCG_STS_GBE2_SGMII_PHY_RX:** TCG_STS_GBE2_SGMII_PHY_RX field.
12	0h RO/V	**TCG_STS_GBE1_SGMII_PHY_RX:** TCG_STS_GBE1_SGMII_PHY_RX field.
11	0h RO/V	**TCG_STS_GBE2_SGMII_REF:** TCG_STS_GBE2_SGMII_REF field.
10	0h RO/V	**TCG_STS_GBE1_SGMII_REF:** TCG_STS_GBE1_SGMII_REF field.
9	0h RO/V	**TCG_STS_GBE2_RGMII_TX:** TCG_STS_GBE2_RGMII_TX field.
8	0h RO/V	**TCG_STS_GBE1_RGMII_TX:** TCG_STS_GBE1_RGMII_TX field.
7	0h RO/V	**TCG_STS_GBE_PTP:** TCG_STS_GBE_PTP field.
6	0h RO/V	**TCG_STS_PLL_PTP:** TCG_STS_PLL_PTP field.
5	0h RO/V	**Reserved**
4	0h RO/V	**Reserved**
3	0h RO/V	**TCG_STS_LCPLL_REF:** TCG_STS_LCPLL_REF field.
2	0h RO/V	**TCG_STS_MAIN:** TCG_STS_MAIN field.
1	0h RO/V	**TCG_STS_CPU_FAST:** TCG_STS_CPU_FAST field.
0	0h RO/V	**TCG_STS_S0IX_XTAL:** TCG_STS_S0IX_XTAL field.

14.6.1.30 Soft Reset- DMA (DMA_SOFT_RST) — Offset 4060008Ch

Register for Soft Reset of DMA.

Type	Size	Offset	Default
MMIO	32 bit	4060008Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**Soft Reset Enable - DMA (CCUREG_DMA_RST):** DMA soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.31 Block Level Clock Gate- GBE (GBE_BLK_CG) — Offset 40600090h

Register for enabling GBE block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	40600090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Block Levell Gate Enable GBE (CCUREG_GBE_CG):** CANBUS Clock gating register. 1-Clock gate 0-No clock gating.

14.6.1.32 Soft Reset GBE (GBE_SOFT_RST) — Offset 40600094h

Register for Soft Reset of GBE.

Type	Size	Offset	Default
MMIO	32 bit	40600094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Soft Reset Enable GBE (CCUREG_GBE_RST):** CANBUS soft reset bit. 1-Reset asserted 0-Reset de-asserted.

14.6.1.33 Trunk Clock Gate Rise Interrupt Mask (TCG_CLKACK_RISE_INTR_MASK) — Offset 40600098h

RISE Interrupt mask bits for each TCG clk. When bit is set, the interrupt due to the respective clk is disabled.

Type	Size	Offset	Default
MMIO	32 bit	40600098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**TCG_RISE_INTR_MASK_GBE2_RGMII_PHY_RX:** TCG_RISE_INTR_MASK_GBE2_RGMII_PHY_RX field.
14	0h RW	**TCG_RISE_INTR_MASK_GBE1_RGMII_PHY_RX:** TCG_RISE_INTR_MASK_GBE1_RGMII_PHY_RX field.
13	0h RW	**TCG_RISE_INTR_MASK_GBE2_SGMII_PHY_RX:** TCG_RISE_INTR_MASK_GBE2_SGMII_PHY_RX field.
12	0h RW	**TCG_RISE_INTR_MASK_GBE1_SGMII_PHY_RX:** TCG_RISE_INTR_MASK_GBE1_SGMII_PHY_RX field.
11	0h RW	**TCG_RISE_INTR_MASK_GBE2_SGMII_REF:** TCG_RISE_INTR_MASK_GBE2_SGMII_REF field.
10	0h RW	**TCG_RISE_INTR_MASK_GBE1_SGMII_REF:** TCG_RISE_INTR_MASK_GBE1_SGMII_REF field.
9	0h RW	**TCG_RISE_INTR_MASK_GBE2_RGMII_TX:** TCG_RISE_INTR_MASK_GBE2_RGMII_TX field.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**TCG_RISE_INTR_MASK_GBE1_RGMII_TX:** TCG_RISE_INTR_MASK_GBE1_RGMII_TX field.
7	0h RW	**TCG_RISE_INTR_MASK_GBE_PTP:** TCG_RISE_INTR_MASK_GBE_PTP field.
6	0h RW	**TCG_RISE_INTR_MASK_PLL_PTP:** TCG_RISE_INTR_MASK_PLL_PTP field.
5	0h RW	**Reserved**
4	0h RW	**Reserved**
3	0h RW	**TCG_RISE_INTR_MASK_LCPLL_REF:** TCG_RISE_INTR_MASK_LCPLL_REF field.
2	0h RW	**TCG_RISE_INTR_MASK_MAIN:** TCG_RISE_INTR_MASK_MAIN field.
1	0h RW	**TCG_RISE_INTR_MASK_CPU_FAST:** TCG_RISE_INTR_MASK_CPU_FAST field.
0	0h RW	**TCG_RISE_INTR_MASK_S0IX_XTAL:** TCG_RISE_INTR_MASK_S0IX_XTAL field.

14.6.1.34 Trunk Clock Gate Fall Interrupt Mask (TCG_CLKACK_FALL_INTR_MASK) — Offset 4060009Ch

FALL Interrupt mask bits for each TCG clk. When bit is set, the interrupt due to the respective clk is disabled.

Type	Size	Offset	Default
MMIO	32 bit	4060009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**TCG_FALL_INTR_MASK_GBE2_RGMII_PHY_RX:** TCG_FALL_INTR_MASK_GBE2_RGMII_PHY_RX field.
14	0h RW	**TCG_FALL_INTR_MASK_GBE1_RGMII_PHY_RX:** TCG_FALL_INTR_MASK_GBE1_RGMII_PHY_RX field.
13	0h RW	**TCG_FALL_INTR_MASK_GBE2_SGMII_PHY_RX:** TCG_FALL_INTR_MASK_GBE2_SGMII_PHY_RX field.
12	0h RW	**TCG_FALL_INTR_MASK_GBE1_SGMII_PHY_RX:** TCG_FALL_INTR_MASK_GBE1_SGMII_PHY_RX field.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**TCG_FALL_INTR_MASK_GBE2_SGMII_REF:** TCG_FALL_INTR_MASK_GBE2_SGMII_REF field.
10	0h RW	**TCG_FALL_INTR_MASK_GBE1_SGMII_REF:** TCG_FALL_INTR_MASK_GBE1_SGMII_REF field.
9	0h RW	**TCG_FALL_INTR_MASK_GBE2_RGMII_TX:** TCG_FALL_INTR_MASK_GBE2_RGMII_TX field.
8	0h RW	**TCG_FALL_INTR_MASK_GBE1_RGMII_TX:** TCG_FALL_INTR_MASK_GBE1_RGMII_TX field.
7	0h RW	**TCG_FALL_INTR_MASK_GBE_PTP:** TCG_FALL_INTR_MASK_GBE_PTP field.
6	0h RW	**TCG_FALL_INTR_MASK_PLL_PTP:** TCG_FALL_INTR_MASK_PLL_PTP field.
5	0h RW	**Reserved**
4	0h RW	**Reserved**
3	0h RW	**TCG_FALL_INTR_MASK_LCPLL_REF:** TCG_FALL_INTR_MASK_LCPLL_REF field.
2	0h RW	**TCG_FALL_INTR_MASK_MAIN:** TCG_FALL_INTR_MASK_MAIN field.
1	0h RW	**TCG_FALL_INTR_MASK_CPU_FAST:** TCG_FALL_INTR_MASK_CPU_FAST field.
0	0h RW	**TCG_FALL_INTR_MASK_S0IX_XTAL:** TCG_FALL_INTR_MASK_S0IX_XTALfield.

14.6.1.35 HBW_CLK_SEL Reg (HBW_CLK_SEL) — Offset 406000A8h

Clock hbw switch control bits. Clock switching is done after HBW is halted. Switch enable is auto cleared by hardware after switching is complete.PMU intr is generated when switching is complete.

Type	Size	Offset	Default
MMIO	32 bit	406000A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Clkswitch En (CLK_SW_EN):** FW write 1 and HW auto clear.
7:1	0h RO	**Reserved**
0	0h RW	**Clk Sel Value (CLK_SELECT):** Bit[0] - Selection control for HBW clk. 0 - S0ix_clk - 100MHz 1 - Main_clk_div2 - 200MHz bit[8] - HBW clk switch Enable Clock switching is done after CORE is halted. Switch enable is auto-cleared by hardware after switching is complete. PMU intr is generated when switching is complete. .

14.6.1.36 M Value M/N Divide- I2S0 (I2S0_MNDIV_M_VALUE) — Offset 406000B0h

M/N Divide Register for M Value - I2S0.

Type	Size	Offset	Default
MMIO	32 bit	406000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.6.1.37 N Value M/N Divide- I2S0 (I2S0_MNDIV_N_VALUE) — Offset 406000B4h

M/N Divide Register for N Value - I2S0.

Note: Bit definitions are the same as I2S0_MNDIV_M_VALUE, offset 406000B0h.

14.6.1.38 Enable - M/N Divide- I2S0 (I2S0_MNDIV_ENABLE) — Offset 406000B8h

M/N Divide Enable Register - I2S0.

Note: Bit definitions are the same as I2S0_MNDIV_M_VALUE, offset 406000B0h.

14.6.1.39 M Value M/N Divide- I2S1 (I2S1_MNDIV_M_VALUE) — Offset 406000BCh

M/N Divide Register for M Value - I2S1.

Note: Bit definitions are the same as I2S0_MNDIV_M_VALUE, offset 406000B0h.

14.6.1.40 N Value M/N Divide- I2S1 (I2S1_MNDIV_N_VALUE) — Offset 406000C0h

M/N Divide Register for N Value - I2S1.

Note: Bit definitions are the same as I2S0_MNDIV_M_VALUE, offset 406000B0h.

14.6.1.41 Enable - M/N Divide- I2S1 (I2S1_MNDIV_ENABLE) — Offset 406000C4h

M/N Divide Enable Register - I2S1.

Note: Bit definitions are the same as I2S0_MNDIV_M_VALUE, offset 406000B0h.

14.6.1.42 Soft Reset TGPIO (TGPIO_SOFT_RST) — Offset 406000C8h

Register for Soft Reset of TGPIO.

Type	Size	Offset	Default
MMIO	32 bit	406000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Soft Reset Enable TGPIO (CCUREG_TGPIO_RST):** Reserved

14.6.1.43 Block Level Clock Gate TGPIO (TGPIO_BLK_OCPCG) — Offset 406000CCh

Register for enabling TGPIO block level clock gating.

Type	Size	Offset	Default
MMIO	32 bit	406000CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Block Levell Gate Enable TGPIO OCPCLK (CCUREG_TGPIO_OCPCG):** Reserved

14.6.1.44 Trunk Clock Gate Rise Interrupt Status (TCG_CLKACK_RISE_INTR_STS) — Offset 406000D0h

RISE Interrupt status bits for each TCG clk. The sts bit is set on rise-edge of clkack. Each bit is for the clks related to the respective bit in TCG register. .

Type	Size	Offset	Default
MMIO	32 bit	406000D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**TCG_RISE_INTR_STS_GBE2_RGMII_PHY_RX:** TCG_RISE_INTR_STS_GBE2_RGMII_PHY_RX field.
14	0h RW/1C	**TCG_RISE_INTR_STS_GBE1_RGMII_PHY_RX:** TCG_RISE_INTR_STS_GBE1_RGMII_PHY_RX field.
13	0h RW/1C	**TCG_RISE_INTR_STS_GBE2_SGMII_PHY_RX:** TCG_RISE_INTR_STS_GBE2_SGMII_PHY_RX field.
12	0h RW/1C	**TCG_RISE_INTR_STS_GBE1_SGMII_PHY_RX:** TCG_RISE_INTR_STS_GBE1_SGMII_PHY_RX field.
11	0h RW/1C	**TCG_RISE_INTR_STS_GBE2_SGMII_REF:** TCG_RISE_INTR_STS_GBE2_SGMII_REF field.
10	0h RW/1C	**TCG_RISE_INTR_STS_GBE1_SGMII_REF:** TCG_RISE_INTR_STS_GBE1_SGMII_REF field.
9	0h RW/1C	**TCG_RISE_INTR_STS_GBE2_RGMII_TX:** TCG_RISE_INTR_STS_GBE2_SGMII_TX field.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**TCG_RISE_INTR_STS_GBE1_RGMII_TX:** TCG_RISE_INTR_STS_GBE1_SGMII_TX field.
7	0h RW/1C	**TCG_RISE_INTR_STS_GBE_PTP:** TCG_RISE_INTR_STS_GBE_PTP field.
6	0h RW/1C	**TCG_RISE_INTR_STS_PLL_PTP:** TCG_RISE_INTR_STS_PLL_PTP field.
5	0h RW/1C	**Reserved**
4	0h RW/1C	**Reserved**
3	0h RW/1C	**TCG_RISE_INTR_STS_LCPLL_REF:** TCG_RISE_INTR_STS_LCPLL_REF field.
2	0h RW/1C	**TCG_RISE_INTR_STS_MAIN:** TCG_RISE_INTR_STS_MAIN field.
1	0h RW/1C	**TCG_RISE_INTR_STS_CPU_FAST:** TCG_RISE_INTR_STS_CPU_FAST field.
0	0h RW/1C	**TCG_RISE_INTR_STS_S0IX_XTAL:** TCG_RISE_INTR_STS_S0IX_XTAL field.

14.6.1.45 Trunk Clock Gate Fall Interrupt Status (TCG_CLKACK_FALL_INTR_STS) — Offset 406000D4h

FALL Interrupt status bits for each TCG clk. The sts bit is set on fall-edge of clkack. Each bit is for the clks related to the respective bit in TCG register.

Type	Size	Offset	Default
MMIO	32 bit	406000D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**TCG_FALL_INTR_STS_GBE2_RGMII_PHY_RX:** TCG_FALL_INTR_STS_GBE2_RGMII_PHY_RX field.
14	0h RW/1C	**TCG_FALL_INTR_STS_GBE1_RGMII_PHY_RX:** TCG_FALL_INTR_STS_GBE1_RGMII_PHY_RX field.
13	0h RW/1C	**TCG_FALL_INTR_STS_GBE2_SGMII_PHY_RX:** TCG_FALL_INTR_STS_GBE2_SGMII_PHY_RX field.
12	0h RW/1C	**TCG_FALL_INTR_STS_GBE1_SGMII_PHY_RX:** TCG_FALL_INTR_STS_GBE1_SGMII_PHY_RX field.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**TCG_FALL_INTR_STS_GBE2_SGMII_REF:** TCG_FALL_INTR_STS_GBE2_SGMII_REF field.
10	0h RW/1C	**TCG_FALL_INTR_STS_GBE1_SGMII_REF:** TCG_FALL_INTR_STS_GBE1_SGMII_REF field.
9	0h RW/1C	**TCG_FALL_INTR_STS_GBE2_RGMII_TX:** TCG_FALL_INTR_STS_GBE2_RGMII_TX field.
8	0h RW/1C	**TCG_FALL_INTR_STS_GBE1_RGMII_TX:** TCG_FALL_INTR_STS_GBE1_RGMII_TX field.
7	0h RW/1C	**TCG_FALL_INTR_STS_GBE_PTP:** TCG_FALL_INTR_STS_GBE_PTP field.
6	0h RW/1C	**TCG_FALL_INTR_STS_PLL_PTP:** TCG_FALL_INTR_STS_PLL_PTP field.
5	0h RW/1C	**Reserved**
4	0h RW/1C	**Reserved**
3	0h RW/1C	**TCG_FALL_INTR_STS_LCPLL_REF:** TCG_FALL_INTR_STS_LCPLL_REF field.
2	0h RW/1C	**TCG_FALL_INTR_STS_MAIN:** TCG_FALL_INTR_STS_MAIN field.
1	0h RW/1C	**TCG_FALL_INTR_STS_CPU_FAST:** TCG_FALL_INTR_STS_CPU_FAST field.
0	0h RW/1C	**TCG_FALL_INTR_STS_S0IX_XTAL:** TCG_FALL_INTR_STS_S0IX_XTAL field.

14.6.1.46 CORE_CLK_SEL Reg (CORE_CLK_SEL) — Offset 406000D8h

Clock core switch control bits. Clock switching is done after CORE is halted. Switch enable is auto cleared by hardware after switching is complete.PMU intr is generated when switching is complete.

Type	Size	Offset	Default
MMIO	32 bit	406000D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/V	**Clk Switch En (CLK_SW_EN):** FW write 1 and HW auto clear.
7:2	0h RO	**Reserved**
1:0	0h RW	**Clk Sel Value (CLK_SELECT):** Bit[1:0] - Selection control for core clk. 00 - S0ix_clk - 100MHz 01 - Main_clk_div2 - 200MHz 10 - Main_clk - 400MHz 11 - Cpu_fast_clk - 500MHz bit[8] - Core clk switch Enable Clock switching is done after CORE is halted. Switch enable is auto-cleared by hardware after switching is complete. PMU intr is generated when switching is complete. .

14.6.1.47 AON Clock Gate Enable (AON_CG_EN) — Offset 406000DCh

Register for enabling clock gating of ish_aon_clk (2.5 MHz Clock). This will allow the SOC to shutoff the ring oscillator and hence enable S0i3.4 entry.

Type	Size	Offset	Default
MMIO	32 bit	406000DCh	00000100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	1h RW	**Isolation Control For PLL And DLL Power Domain. (PLL_DLL_ISO_CTRL):** Bit 1 - Disable isolation Bit 0 Enable isolation.
7:1	0h RO	**Reserved**
0	0h RW	**Aon Clock Gate Enable Bit (CCUREG_AON_CG_EN):** AON clock gate enable bit. 1-Enable clock gating of ish_aon_clk 0-Do not enable clock gating of ish_aon_clk.

14.7 MISC Registers

MISC Registers	Address Offset	Table
MISC	40700090h - 40700908h	Table 14-17

14.7.1 Misc Registers Summary

Table 14-17. Summary of Misc Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40700090h	4	DFX VISA Milestone (DFX_VISA_MILESTONE)	00000000h
40700094h	4	ISH RTC Counter LSB Value (ISH_RTC_COUNTER0)	00000000h
40700098h	4	ISH RTC Counter MSB Value (ISH_RTC_COUNTER1)	00000000h
407000ACh	4	ISH_MISC_UART_CKN	00000000h
407000B0h	4	ISH_MISC_VMID	00000000h
407000B4h	4	ISH_LMTHH_DEFEATURE	00000000h
407000B8h	4	NMI Enable (ISH_NMI_EN)	00000000h
407000C0h	4	HH ART Timestamp Control (HH_ART_TS_CTRL)	00000000h
407000C4h	4	[31:0] Of HH FW Value Low (HH_ART_TB_STAMP_LOW)	00000000h
407000C8h	4	[63:32] Of HH FW Value High (HH_ART_TB_STAMP_HIGH)	00000000h
407000CCh	4	HH Saturation Staus (HH_SATURATION)	00000000h
407000D0h	4	[31:0[] Of Local Art Sync Counter (HH_ART_RD_TS_SNAPSHOT_LOW)	00000000h
407000D4h	4	[63:32] OfLocal Art Sync Counter (HH_ART_RD_TS_SNAPSHOT_HIGH)	00000000h
40700100h	4	Revision ID (ISH_MISC_REVISION_ID)	00000001h
40700200h	4	This Is Spare ROFor ECO. (ISH_MISC_ECO_RO)	00000000h
40700204h	4	This Is Spare RWFor ECO. (ISH_MISC_ECO_RW)	00000000h
40700208h	4	This Is Spare RW1CFor ECO (ISH_MISC_ECO_RW1C)	00000000h
4070020Ch	4	This Is Spare Retention RWFor ECO. (ISH_MISC_ECO_RET_RW)	00000000h
40700210h	4	This Is Spare Retention RW1CFor ECO. (ISH_MISC_ECO_RET_RW1C)	00000000h
40700220h	4	AON Timestamp Control0 (ISH_AON_TIMESTAMP_CTRL0)	00000000h
40700224h	4	AON Timestamp Capture LOWregister0 (ISH_AON_TIMESTAMP_LOW0)	00000000h
40700228h	4	AON Timestamp Control HIGH0 (ISH_AON_TIMESTAMP_HIGH0)	00000000h
4070022Ch	4	AON Timestamp Control STATUS0 (ISH_AON_TIMESTAMP_STATUS0)	00000000h
40700230h	4	AON Timestamp Control1 (ISH_AON_TIMESTAMP_CTRL1)	00000000h
40700234h	4	AON Timestamp Capture LOWregister1 (ISH_AON_TIMESTAMP_LOW1)	00000000h
40700238h	4	AON Timestamp Control HIGH1 (ISH_AON_TIMESTAMP_HIGH1)	00000000h
4070023Ch	4	AON Timestamp Control STATUS1 (ISH_AON_TIMESTAMP_STATUS1)	00000000h
40700240h	4	AON Timestamp Control2 (ISH_AON_TIMESTAMP_CTRL2)	00000000h
40700244h	4	AON Timestamp Capture LOWregister2 (ISH_AON_TIMESTAMP_LOW2)	00000000h
40700248h	4	AON Timestamp Control HIGH2 (ISH_AON_TIMESTAMP_HIGH2)	00000000h
4070024Ch	4	AON Timestamp Control STATUS2 (ISH_AON_TIMESTAMP_STATUS2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40700250h	4	AON Timestamp Control3 (ISH_AON_TIMESTAMP_CTRL3)	00000000h
40700254h	4	AON Timestamp Capture LOWregister3 (ISH_AON_TIMESTAMP_LOW3)	00000000h
40700258h	4	AON Timestamp Control HIGH3 (ISH_AON_TIMESTAMP_HIGH3)	00000000h
4070025Ch	4	AON Timestamp Control STATUS3 (ISH_AON_TIMESTAMP_STATUS3)	00000000h
40700260h	4	RTC Timestamp Control0 (ISH_RTC_TIMESTAMP_CTRL0)	00000000h
40700264h	4	RTC Timestamp Capture LOWregister0 (ISH_RTC_TIMESTAMP_LOW0)	00000000h
40700268h	4	RTC Timestamp Control HIGH0 (ISH_RTC_TIMESTAMP_HIGH0)	00000000h
4070026Ch	4	RTC Timestamp Control STATUS0 (ISH_RTC_TIMESTAMP_STATUS0)	00000000h
40700270h	4	RTC Timestamp Control1 (ISH_RTC_TIMESTAMP_CTRL1)	00000000h
40700274h	4	RTC Timestamp Capture LOWregister1 (ISH_RTC_TIMESTAMP_LOW1)	00000000h
40700278h	4	RTC Timestamp Control HIGH1 (ISH_RTC_TIMESTAMP_HIGH1)	00000000h
4070027Ch	4	RTC Timestamp Control STATUS1 (ISH_RTC_TIMESTAMP_STATUS1)	00000000h
40700280h	4	RTC Timestamp Control2 (ISH_RTC_TIMESTAMP_CTRL2)	00000000h
40700284h	4	RTC Timestamp Capture LOWregister2 (ISH_RTC_TIMESTAMP_LOW2)	00000000h
40700288h	4	RTC Timestamp Control HIGH2 (ISH_RTC_TIMESTAMP_HIGH2)	00000000h
4070028Ch	4	RTC Timestamp Control STATUS2 (ISH_RTC_TIMESTAMP_STATUS2)	00000000h
40700290h	4	RTC Timestamp Control3 (ISH_RTC_TIMESTAMP_CTRL3)	00000000h
40700294h	4	RTC Timestamp Capture LOWregister3 (ISH_RTC_TIMESTAMP_LOW3)	00000000h
40700298h	4	RTC Timestamp Control HIGH3 (ISH_RTC_TIMESTAMP_HIGH3)	00000000h
4070029Ch	4	RTC Timestamp Control STATUS3 (ISH_RTC_TIMESTAMP_STATUS3)	00000000h
407002A0h	4	XTAL Timestamp Control0 (ISH_XTAL_TIMESTAMP_CTRL0)	00000000h
407002A4h	4	XTAL Timestamp Capture LOWregister0 (ISH_XTAL_TIMESTAMP_LOW0)	00000000h
407002A8h	4	XTAL Timestamp Control HIGH0 (ISH_XTAL_TIMESTAMP_HIGH0)	00000000h
407002ACh	4	XTAL Timestamp Control STATUS0 (ISH_XTAL_TIMESTAMP_STATUS0)	00000000h
407002B0h	4	XTAL Timestamp Control1 (ISH_XTAL_TIMESTAMP_CTRL1)	00000000h
407002B4h	4	XTAL Timestamp Capture LOWregister1 (ISH_XTAL_TIMESTAMP_LOW1)	00000000h
407002B8h	4	XTAL Timestamp Control HIGH1 (ISH_XTAL_TIMESTAMP_HIGH1)	00000000h
407002BCh	4	XTAL Timestamp Control STATUS1 (ISH_XTAL_TIMESTAMP_STATUS1)	00000000h
407002C0h	4	XTAL Timestamp Control2 (ISH_XTAL_TIMESTAMP_CTRL2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
407002C4h	4	XTAL Timestamp Capture LOWregister2 (ISH_XTAL_TIMESTAMP_LOW2)	00000000h
407002C8h	4	XTAL Timestamp Control HIGH2 (ISH_XTAL_TIMESTAMP_HIGH2)	00000000h
407002CCh	4	XTAL Timestamp Control STATUS2 (ISH_XTAL_TIMESTAMP_STATUS2)	00000000h
407002D0h	4	XTAL Timestamp Control2 (ISH_XTAL_TIMESTAMP_CTRL3)	00000000h
407002D4h	4	XTAL Timestamp Capture LOWregister3 (ISH_XTAL_TIMESTAMP_LOW3)	00000000h
407002D8h	4	XTAL Timestamp Control HIGH3 (ISH_XTAL_TIMESTAMP_HIGH3)	00000000h
407002DCh	4	XTAL Timestamp Control STATUS3 (ISH_XTAL_TIMESTAMP_STATUS3)	00000000h
40700300h	4	N Value For M/N Of XTAL Timer (HH_ART_TIMER0_N_VAL)	00000001h
40700304h	4	N Value For M/N Of AON Timer (HH_ART_TIMER1_N_VAL)	00000019h
40700308h	4	N Value For M/N Of RTC Timer (HH_ART_TIMER2_N_VAL)	00008000h
40700310h	4	Quotient For M/N Of XTAL Timer (HH_ART_TIMER0_MN_QUOTIENT)	00000001h
40700314h	4	Quotient For M/N Of AON Timer (HH_ART_TIMER1_MN_QUOTIENT)	00000007h
40700318h	4	Quotient For M/N Of RTC Timer (HH_ART_TIMER2_MN_QUOTIENT)	00000249h
40700320h	4	Remainder For M/N Of XTAL Timer (HH_ART_TIMER0_MN_REMAINDER)	00000000h
40700324h	4	Remainder For M/N Of AON Timer (HH_ART_TIMER1_MN_REMAINDER)	00000011h
40700328h	4	Remainder For M/N Of RTC Timer (HH_ART_TIMER2_MN_REMAINDER)	00007800h
40700330h	4	MISC_PROXYMODE_REG_GBE1	00000000h
40700334h	4	MISC_PROXYMODE_REG_GBE2	00000000h
40700338h	4	MISC_PROXYMODE_ENTRY_INT_STS	00000000h
4070033Ch	4	ARM DFX Secure Feature Status (OSE_ARM_DFX_SECURE_STS)	00000000h
40700340h	4	ARM AHBS Select (OSE_ARM_AHBS_SEL_ADDR)	00000000h
40700400h	4	Reg Ose_sram_region1_base (SRAM_REGION_1_BASE)	60000000h
40700404h	4	Reg Ose_sram_region1_size (SRAM_REGION_1_SIZE)	00000000h
40700408h	4	Reg Ose_sram_region2_base (SRAM_REGION_2_BASE)	60000000h
4070040Ch	4	Reg Ose_sram_region2_size (SRAM_REGION_2_SIZE)	00000000h
40700410h	4	Reg Ose_sram_region3_base (SRAM_REGION_3_BASE)	60000000h
40700414h	4	Reg Ose_sram_region3_size (SRAM_REGION_3_SIZE)	00000000h
40700418h	4	Reg Ose_sram_region4_base (SRAM_REGION_4_BASE)	60000000h
4070041Ch	4	Reg Ose_sram_region4_size (SRAM_REGION_4_SIZE)	00000000h
40700800h	4	FUSA_HBW_FABRIC_PARITY_LOG	00000000h
40700804h	4	FUSA_PER0 FABRIC PARITY_LOG (FUSA_PER0_FABRIC_PARITY_LOG)	00000000h
40700808h	4	FUSA_PER1 FABRIC PARITY_LOG (FUSA_PER1_FABRIC_PARITY_LOG)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4070080Ch	4	FUSA_MEM PARITY_LOG (FUSA_MEM_PARITY_LOG)	00000000h
40700810h	4	FUSA_ARM DC ERROR_LOG (FUSA_ARM_DC_ERROR_LOG)	00000000h
40700814h	4	FUSA_ARM IC ERROR_LOG (FUSA_ARM_IC_ERROR_LOG)	00000000h
40700818h	4	FUSA BRIDGE_PARTY_LOG0 (FUSA_BRIDGE_PARTY_LOG0)	00000000h
4070081Ch	4	FUSA BRIDGE_PARTY_LOG1 (FUSA_BRIDGE_PARTY_LOG1)	00000000h
40700820h	4	FUSA CONTROL (FUSA_CTRL)	00000000h
40700900h	4	ISH_FW_ALIVE	00000000h
40700904h	4	ISH_FW_TIMEOUT	000186A0h
40700908h	4	ISH_NMI_STATUS	00000000h

14.7.1.1 DFX VISA Milestone (DFX_VISA_MILESTONE) — Offset 40700090h

DFX VISA Milestone.

Type	Size	Offset	Default
MMIO	32 bit	40700090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DFX_VISA_MILESTONE_BIT31TO0:** Software code execution milestone indication This will be used in VISA observe ability for getting performance metrics of code execution Usage will be to have this observed on a Logic Analyzer.

14.7.1.2 ISH RTC Counter LSB Value (ISH_RTC_COUNTER0) — Offset 40700094h

ISH RTC Counter LSB Value Register.

Type	Size	Offset	Default
MMIO	32 bit	40700094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**ISH_RTC_COUNTER0:** ISH_RTC_COUNTER0: ISH RTC counter LSB value Register.

14.7.1.3 ISH RTC Counter MSB Value (ISH_RTC_COUNTER1) — Offset 40700098h

ISH RTC Counter MSB Value Register.

Type	Size	Offset	Default
MMIO	32 bit	40700098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**ISH_RTC_COUNTER1:** ISH_RTC_COUNTER1 : ISH RTC counter MSB value Register.

14.7.1.4 ISH_MISC_UART_CKN — Offset 407000ACh

Reserved

Type	Size	Offset	Default
MMIO	32 bit	407000ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.7.1.5 ISH_MISC_VMID — Offset 407000B0h

Reserved

Note: Bit definitions are the same as ISH_MISC_UART_CKN, offset 407000ACh.

14.7.1.6 ISH_LMTHH_DEFEATURE — Offset 407000B4h

Reserved

Note: Bit definitions are the same as ISH_MISC_UART_CKN, offset 407000ACh.

14.7.1.7 NMI Enable (ISH_NMI_EN) — Offset 407000B8h

Reserved

Note: Bit definitions are the same as ISH_MISC_UART_CKN, offset 407000ACh.

14.7.1.8 HH ART Timestamp Control (HH_ART_TS_CTRL) — Offset 407000C0h

HH ART Timestamp Control Register.

Type	Size	Offset	Default
MMIO	32 bit	407000C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW	**HH_ART_TIMER_SEL:** TIMER__SEL[1:0] selects the timer from which FW wants to read the timestamp 00 - XTAL_CLK timer 01 - AON_CLK timer 10 - RTC_CLK timer .
3:2	0h RO	**Reserved**
1	0h RW/AC	**HH_FWUPD:** The FWUpd Bit will be asserted Fw when the RTSS SB EPHW will receive LocalSync packet and interrupt RTSS FW to write the received ART timer value when asserted indicated that the new FW_VALUE . HH block will update the Free running Local ART with the new calculated FW_VALUE on FwUpd Re pulse and will set the FWUpd_done pulse for clearing this Bit. FW set and auto clear on Hardware intervention(pulse) .
0	0h RW	**HH_TIMESTAMP_EN:** 1: HH_time_stamp_en would be provided and asserted for all valid the syncCntr pulse are generated 0: HH_time_stamp_en deasserted incated that no valid the synccntr pulse for HH block and can be ignored .

14.7.1.9 [31:0] Of HH FW Value Low (HH_ART_TB_STAMP_LOW) — Offset 407000C4h

[31:0] of HH FW Value Low.

Type	Size	Offset	Default
MMIO	32 bit	407000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HH_FW_VALUE_LOW:** RTSS SB EPHW will receive LocalSync packet and interrupt RTSS FW to write the NEW received ART timer value in FW_VALUE. Free running Local ART will be updated with this FW_VALUE on FwUpd .

14.7.1.10 [63:32] Of HH FW Value High (HH_ART_TB_STAMP_HIGH) — Offset 407000C8h

[63:32] of HH FW Value High.

Type	Size	Offset	Default
MMIO	32 bit	407000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HH_FW_VALUE_HIGH:** RTSS SB EPHW will receive LocalSync packet and interrupt RTSS FW to write the NEW received ART timer value in FW_VALUE. Free running Local ART will be updated with this FW_VALUE on FwUpd .

14.7.1.11 HH Saturation Staus (HH_SATURATION) — Offset 407000CCh

HH Saturation Staus Register.

Type	Size	Offset	Default
MMIO	32 bit	407000CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**HH_UPD_IN_PROG:** 1: xtal_clk timer update is in progress 0: xtal_clk timer is ready to be read by FW. FW needs to make sure that xtal_clkack status is high before reading this bit.
0	0h RW/1C	**HH_SAT_STAT:** 1: stauration has occured . 0: No stauration occurred FW needs to ensure that there is no Saturation Event status set for the Delay Counter. The 17bit counter will saturate at max programmable value will set a status bit SAT_STAT in Saturation register on MSB bit being 1 to indicate saturation event has occurred . If SAT_STAT is set,asserted by delaycounter logic in Hh Block , the RTSS. FW is expected to restart the LOCAL ART SYNC Update flow and clear this bit on read .

14.7.1.12 [31:0[] Of Local Art Sync Counter (HH_ART_RD_TS_SNAPSHOT_LOW) — Offset 407000D0h

[31:0[] of Local Art Sync Counter.

Type	Size	Offset	Default
MMIO	32 bit	407000D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**ISH_HH_ART_RD_TS_SNAPSHOT:** FW Will Read this Locally Updated HH Time stamp Value to verify whether the correct HH Time stamp is written into the IP.

14.7.1.13 [63:32] OfLocal Art Sync Counter (HH_ART_RD_TS_SNAPSHOT_HIGH) — Offset 407000D4h

[63:32] of Local Art Sync Counter.

Note: Bit definitions are the same as HH_ART_RD_TS_SNAPSHOT_LOW, offset 407000D0h.

14.7.1.14 Revision ID (ISH_MISC_REVISION_ID) — Offset 40700100h

This register provides information to ISH FW (Not accessible by any other entity) on the current ISH generation-revision.

Type	Size	Offset	Default
MMIO	32 bit	40700100h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RO	**ISH_MISC_REVISION_ID:** This register provides information to ISH FW (Not accessible by any other entity) on the current ISH generation-revision.

14.7.1.15 This Is Spare RO for ECO. (ISH_MISC_ECO_RO) — Offset 40700200h

This is spare RO register for ECO.

Type	Size	Offset	Default
MMIO	32 bit	40700200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**ISH_MISC_ECO_RO:** This is spare RO register for ECO.

14.7.1.16 This Is Spare RW for ECO. (ISH_MISC_ECO_RW) — Offset 40700204h

This is spare RW register for ECO.

Type	Size	Offset	Default
MMIO	32 bit	40700204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RW	**ISH_MISC_ECO_RW1:** This is spare RW register for ECO.
0	0h RW	**ISH_MISC_ECO_RW2:** 1: Disable adsnn fix

14.7.1.17 This Is Spare RW1C for ECO (ISH_MISC_ECO_RW1C) — Offset 40700208h

This is spare RW1C register for ECO.

Type	Size	Offset	Default
MMIO	32 bit	40700208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**ISH_MISC_ECO_RW1C:** This is spare RW1C register for ECO.

14.7.1.18 This Is Spare Retention RW for ECO. (ISH_MISC_ECO_RET_RW) — Offset 4070020Ch

This is spare Retention RW register for ECO. Bit 0 is used for enabling NMI on SRAM DED error.

Type	Size	Offset	Default
MMIO	32 bit	4070020Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RW	**ISH_MISC_ECO_RET_RW:** This is spare Retention RW register for ECO.
0	0h RW	**NMI Enable On SRAM DED Error (ISH_SRAM_DED_NMI_EN):** Bit 0: When 1, enables the NMI status generation in ISH_NMI_STATUS bit 0 on SRAM DED error . When 0, disables the NMI status generation in ISH_NMI_STATUS bit 0 on SRAM DED error.

14.7.1.19 This Is Spare Retention RW1C for ECO. (ISH_MISC_ECO_RET_RW1C) — Offset 40700210h

This is spare Retention RW1C register for ECO.

Type	Size	Offset	Default
MMIO	32 bit	40700210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**ISH_MISC_ECO_RET_RW1C:** This is spare Retention RW1C register for ECO.

14.7.1.20 AON Timestamp Control0 (ISH_AON_TIMESTAMP_CTRL0) — Offset 40700220h

Control Register for AON Timestamp 0.

Type	Size	Offset	Default
MMIO	32 bit	40700220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BUSY:** Indicates Enable signal has been receive by timestamp module. FW should wait for busy to match enable before changing enable.
30:13	0h RO	**Reserved**
12:8	00h RW	**GPIO Select (ISH_TIMESTAMP_GPIO_SEL_REG):** Selcts GPIO pin to be timestamped.
7:2	0h RO	**Reserved**
1	0h RW	**Edge Detect (ISH_TIMESTAMP_EDGE_DETECT_REG):** GPIO Edge for capturing tiemstamp. 0: Falling edge,1 : Rising Edge.
0	0h RW	**Timestamp Enable (ISH_TIMESTAMP_EN):** Setting this bit enables the timestamp.

14.7.1.21 AON Timestamp Capture LOWregister0 (ISH_AON_TIMESTAMP_LOW0) — Offset 40700224h

AON Timestamp capture low for AON Timestamp 0.

Type	Size	Offset	Default
MMIO	32 bit	40700224h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Timestamp Low (ISH_TIMESTAMP_LOW):** LSB 32bits of timestamp capture value. Valid when Timestamp status is 1.

14.7.1.22 AON Timestamp Control HIGH0 (ISH_AON_TIMESTAMP_HIGH0) — Offset 40700228h

AON Timestamp capture high for AON Timestamp 0.

Type	Size	Offset	Default
MMIO	32 bit	40700228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Timestamp High (ISH_TIMESTAMP_HIGH):** MSB 32bits of timestamp capture value. Valid when Timestamp status is 1.

14.7.1.23 AON Timestamp Control STATUS0 (ISH_AON_TIMESTAMP_STATUS0) — Offset 4070022Ch

Status Register for AON Timestamp 0.

Type	Size	Offset	Default
MMIO	32 bit	4070022Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**ISH_TIMESTAMP_STATUS:** Timestamp status being 1 indicates an GPIO edge has been timestamped.

14.7.1.24 AON Timestamp Control1 (ISH_AON_TIMESTAMP_CTRL1) — Offset 40700230h

Control Register for AON Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.25 AON Timestamp Capture LOWregister1 (ISH_AON_TIMESTAMP_LOW1) — Offset 40700234h

AON Timestamp capture low for AON Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.26 AON Timestamp Control HIGH1 (ISH_AON_TIMESTAMP_HIGH1) — Offset 40700238h

AON Timestamp capture high for AON Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.27 AON Timestamp Control STATUS1 (ISH_AON_TIMESTAMP_STATUS1) — Offset 4070023Ch

Status Register for AON Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.28 AON Timestamp Control2 (ISH_AON_TIMESTAMP_CTRL2) — Offset 40700240h

Control Register for AON Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.29 AON Timestamp Capture LOWregister2 (ISH_AON_TIMESTAMP_LOW2) — Offset 40700244h

AON Timestamp capture low for AON Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.30 AON Timestamp Control HIGH2 (ISH_AON_TIMESTAMP_HIGH2) — Offset 40700248h

AON Timestamp capture high for AON Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.31 AON Timestamp Control STATUS2 (ISH_AON_TIMESTAMP_STATUS2) — Offset 4070024Ch

Status Register for AON Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.32 AON Timestamp Control3 (ISH_AON_TIMESTAMP_CTRL3) — Offset 40700250h

Control Register for AON Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.33 AON Timestamp Capture LOWregister3 (ISH_AON_TIMESTAMP_LOW3) — Offset 40700254h

AON Timestamp capture low for AON Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.34 AON Timestamp Control HIGH3 (ISH_AON_TIMESTAMP_HIGH3) — Offset 40700258h

AON Timestamp capture high for AON Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.35 AON Timestamp Control STATUS3 (ISH_AON_TIMESTAMP_STATUS3) — Offset 4070025Ch

Status Register for AON Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.36 RTC Timestamp Control0 (ISH_RTC_TIMESTAMP_CTRL0) — Offset 40700260h

Control Register for RTC Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.37 RTC Timestamp Capture LOWregister0 (ISH_RTC_TIMESTAMP_LOW0) — Offset 40700264h

RTC Timestamp capture low for RTC Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.38 RTC Timestamp Control HIGH0 (ISH_RTC_TIMESTAMP_HIGH0) — Offset 40700268h

RTC Timestamp capture high for RTC Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.39 RTC Timestamp Control STATUS0 (ISH_RTC_TIMESTAMP_STATUS0) — Offset 4070026Ch

Status Register for RTC Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.40 RTC Timestamp Control1 (ISH_RTC_TIMESTAMP_CTRL1) — Offset 40700270h

Control Register for RTC Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.41 RTC Timestamp Capture LOWregister1 (ISH_RTC_TIMESTAMP_LOW1) — Offset 40700274h

RTC Timestamp capture low for RTC Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.42 RTC Timestamp Control HIGH1 (ISH_RTC_TIMESTAMP_HIGH1) — Offset 40700278h

RTC Timestamp capture high for RTC Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.43 RTC Timestamp Control STATUS1 (ISH_RTC_TIMESTAMP_STATUS1) — Offset 4070027Ch

Status Register for RTC Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.44 RTC Timestamp Control2 (ISH_RTC_TIMESTAMP_CTRL2) — Offset 40700280h

Control Register for RTC Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.45 RTC Timestamp Capture LOWregister2 (ISH_RTC_TIMESTAMP_LOW2) — Offset 40700284h

RTC Timestamp capture low for RTC Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.46 RTC Timestamp Control HIGH2 (ISH_RTC_TIMESTAMP_HIGH2) — Offset 40700288h

RTC Timestamp capture high for RTC Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.47 RTC Timestamp Control STATUS2 (ISH_RTC_TIMESTAMP_STATUS2) — Offset 4070028Ch

Status Register for RTC Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.48 RTC Timestamp Control3 (ISH_RTC_TIMESTAMP_CTRL3) — Offset 40700290h

Control Register for RTC Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.49 RTC Timestamp Capture LOWregister3 (ISH_RTC_TIMESTAMP_LOW3) — Offset 40700294h

RTC Timestamp capture low for RTC Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.50 RTC Timestamp Control HIGH3 (ISH_RTC_TIMESTAMP_HIGH3) — Offset 40700298h

RTC Timestamp capture high for RTC Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.51 RTC Timestamp Control STATUS3 (ISH_RTC_TIMESTAMP_STATUS3) — Offset 4070029Ch

Status Register for RTC Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.52 XTAL Timestamp Control0 (ISH_XTAL_TIMESTAMP_CTRL0) — Offset 407002A0h

Control Register for XTAL Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.53 XTAL Timestamp Capture LOWregister0 (ISH_XTAL_TIMESTAMP_LOW0) — Offset 407002A4h

XTAL Timestamp capture low for XTAL Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.54 XTAL Timestamp Control HIGH0 (ISH_XTAL_TIMESTAMP_HIGH0) — Offset 407002A8h

XTAL Timestamp capture high for XTAL Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.55 XTAL Timestamp Control STATUS0 (ISH_XTAL_TIMESTAMP_STATUS0) — Offset 407002ACh

Status Register for XTAL Timestamp 0.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.56 XTAL Timestamp Control1 (ISH_XTAL_TIMESTAMP_CTRL1) — Offset 407002B0h

Control Register for XTAL Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.57 XTAL Timestamp Capture LOWregister1 (ISH_XTAL_TIMESTAMP_LOW1) — Offset 407002B4h

XTAL Timestamp capture low for XTAL Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.58 XTAL Timestamp Control HIGH1 (ISH_XTAL_TIMESTAMP_HIGH1) — Offset 407002B8h

XTAL Timestamp capture high for XTAL Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.59 XTAL Timestamp Control STATUS1 (ISH_XTAL_TIMESTAMP_STATUS1) — Offset 407002BCh

Status Register for XTAL Timestamp 1.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.60 XTAL Timestamp Control2 (ISH_XTAL_TIMESTAMP_CTRL2) — Offset 407002C0h

Control Register for XTAL Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.61 XTAL Timestamp Capture LOWregister2 (ISH_XTAL_TIMESTAMP_LOW2) — Offset 407002C4h

XTAL Timestamp capture low for XTAL Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.62 XTAL Timestamp Control HIGH2 (ISH_XTAL_TIMESTAMP_HIGH2) — Offset 407002C8h

XTAL Timestamp capture high for XTAL Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.63 XTAL Timestamp Control STATUS2 (ISH_XTAL_TIMESTAMP_STATUS2) — Offset 407002CCh

Status Register for XTAL Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.64 XTAL Timestamp Control2 (ISH_XTAL_TIMESTAMP_CTRL3) — Offset 407002D0h

Control Register for XTAL Timestamp 2.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_CTRL0, offset 40700220h.

14.7.1.65 XTAL Timestamp Capture LOWregister3 (ISH_XTAL_TIMESTAMP_LOW3) — Offset 407002D4h

XTAL Timestamp capture low for XTAL Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_LOW0, offset 40700224h.

14.7.1.66 XTAL Timestamp Control HIGH3 (ISH_XTAL_TIMESTAMP_HIGH3) — Offset 407002D8h

XTAL Timestamp capture high for XTAL Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_HIGH0, offset 40700228h.

14.7.1.67 XTAL Timestamp Control STATUS3 (ISH_XTAL_TIMESTAMP_STATUS3) — Offset 407002DCh

Status Register for XTAL Timestamp 3.

Note: Bit definitions are the same as ISH_AON_TIMESTAMP_STATUS0, offset 4070022Ch.

14.7.1.68 N Value For M/N Of XTAL Timer (HH_ART_TIMER0_N_VAL) — Offset 40700300h

N value for M/N of XTAL Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700300h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RW	**HH_ART_TIMER0_N_VAL:** FW needs to configure the N value of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.69 N Value For M/N Of AON Timer (HH_ART_TIMER1_N_VAL) — Offset 40700304h

N value for M/N of AON Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700304h	00000019h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000019h RW	**HH_ART_TIMER1_N_VAL:** FW needs to configure the N value of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.70 N Value For M/N Of RTC Timer (HH_ART_TIMER2_N_VAL) — Offset 40700308h

N value for M/N of RTC Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700308h	00008000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00008000h RW	**HH_ART_TIMER2_N_VAL:** FW needs to configure the N value of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.71 Quotient For M/N Of XTAL Timer (HH_ART_TIMER0_MN_QUOTIENT) — Offset 40700310h

Quotient for M/N of XTAL Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700310h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RW	**HH_ART_TIMER0_MN_QUOTIENT:** FW needs to configure the Quotient of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.72 Quotient For M/N Of AON Timer (HH_ART_TIMER1_MN_QUOTIENT) — Offset 40700314h

Quotient for M/N of AON Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700314h	00000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000007h RW	**HH_ART_TIMER1_MN_QUOTIENT:** FW needs to configure the Quotient of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.73 Quotient For M/N Of RTC Timer (HH_ART_TIMER2_MN_QUOTIENT) — Offset 40700318h

Quotient for M/N of RTC Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700318h	00000249h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000249h RW	**HH_ART_TIMER2_MN_QUOTIENT:** FW needs to configure the Quotient of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.74 Remainder For M/N Of XTAL Timer (HH_ART_TIMER0_MN_REMAINDER) — Offset 40700320h

Remainder for M/N of XTAL Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700320h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HH_ART_TIMER0_MN_REMAINDER:** FW needs to configure the Remainder of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.75 Remainder For M/N Of AON Timer (HH_ART_TIMER1_MN_REMAINDER) — Offset 40700324h

Remainder for M/N of AON Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700324h	00000011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000011h RW	**HH_ART_TIMER1_MN_REMAINDER:** FW needs to configure the Remainder of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.76 Remainder For M/N Of RTC Timer (HH_ART_TIMER2_MN_REMAINDER) — Offset 40700328h

Remainder for M/N of RTC Timer.

Type	Size	Offset	Default
MMIO	32 bit	40700328h	00007800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00007800h RW	**HH_ART_TIMER2_MN_REMAINDER:** FW needs to configure the Remainder of the M/N ratio which specifies the timer clock rate relative to the 19.2M PMC art clock.

14.7.1.77 MISC_PROXYMODE_REG_GBE1 — Offset 40700330h

Proxy mode reg for GBE1.

Type	Size	Offset	Default
MMIO	32 bit	40700330h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**PROXY_MODE_BIT:** Proxymode reg for GBE 1, set when entering network proxy. HW set from mirror reg in GBE misc. Cleared by FW.

14.7.1.78 MISC_PROXYMODE_REG_GBE2 — Offset 40700334h

Proxy mode reg for GBE2.

Type	Size	Offset	Default
MMIO	32 bit	40700334h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**PROXY_MODE_BIT:** Proxymode reg for GBE 2, set when entering network proxy. HW set from mirror reg in GBE misc. Cleared by FW.

14.7.1.79 MISC_PROXYMODE_ENTRY_INT_STS — Offset 40700338h

Proxy mode intr reg for both GBE1 & GB2.

Type	Size	Offset	Default
MMIO	32 bit	40700338h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**PROXY_MODE_ENTRY_STS_MASK2:** Entry sts reg interrupt mask.
2	0h RW	**PROXY_MODE_ENTRY_STS_MASK1:** Entry sts reg interrupt mask.
1	0h RW/1C	**PROXY_MODE_ENTRY_STS_2:** Entry sts reg of proxymode, it when posedge is seen in GBE_proxy_mode reg. Cleared by FW.
0	0h RW/1C	**PROXY_MODE_ENTRY_STS_1:** Entry sts reg of proxymode, it when posedge is seen in GBE_proxy_mode reg. Cleared by FW.

14.7.1.80 ARM DFX Secure Feature Status (OSE_ARM_DFX_SECURE_STS) — Offset 4070033Ch

ARM DFX Secure Feature status for FW read.

Type	Size	Offset	Default
MMIO	32 bit	4070033Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO	**OSE_ARM_DFX_SECURE_STATUS:** This bit is set, when either of the policy selected: Policy 2 (Security Unlocked), Policy 4 (Intel Unlocked), Policy 5 (OEM Unlocked).

14.7.1.81 ARM AHBS Select (OSE_ARM_AHBS_SEL_ADDR) — Offset 40700340h

AHBS Select.

Type	Size	Offset	Default
MMIO	32 bit	40700340h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO/V	**AHBSRDY:** AHBSRDYOutput Indicates when the AHBS is ready to accept transactions.
0	0h RW	**AHBSPRI:** Input Indicates that the AHBS or software access takes priority LOW -Software access takes priority over AHBS access, HIGHAHBS access takes priority over software access.

14.7.1.82 Reg Ose_sram_region1_base (SRAM_REGION_1_BASE) — Offset 40700400h

This register has to be programmed by firmware to configure region 1 start address/ base address in SRAM l2 that can be accessed by host.

Type	Size	Offset	Default
MMIO	32 bit	40700400h	60000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	60h RW	**Ose_sram_region1_base 24 To 31 (SRAM_RGN1_BASE_PRG2):** This can be programmed.
23:16	00h RW	**Ose_sram_region1_base 16 To 23 (SRAM_RGN1_BASE_PRG1):** This can be programmed.
15:10	00h RW	**Ose_sram_region1_base 10 To 15 (SRAM_RGN1_BASE_PRG0):** This can be programmed.
9:0	000h RO	**Non Accessable Bits 9 To 0 (SRAM_RGN1_BASE_NON):** These are non accessable bits.

14.7.1.83 Reg Ose_sram_region1_size (SRAM_REGION_1_SIZE) — Offset 40700404h

This register needs to be programmed by firmware to configure the offset/size for the region 1 in SRAM l2 that can be accessed by HOST. The protection region is not present when SIZE=0. When SIZE>0, the size of the protection region is calculated as ((2^(SIZE-1))*(2^10)).

Type	Size	Offset	Default
MMIO	32 bit	40700404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	00h RW	**Ose_sram_region1_size 3 To 7 (SRAM_RGN1_SIZE_PRG):** This can be programmed.
2:0	0h RO	**Ose_sram_region1_size 0 To 2 (SRAM_RGN1_SIZE_NON):** These are non accessable bits.

14.7.1.84 Reg Ose_sram_region2_base (SRAM_REGION_2_BASE) — Offset 40700408h

This register has to be programmed by firmware to configure region 2 start address/ base address in SRAM l2 that can be accessed by host.

Type	Size	Offset	Default
MMIO	32 bit	40700408h	60000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	60h RW	**Ose_sram_region2_base 24 To 31 (SRAM_RGN2_BASE_PRG2):** This can be programmed.
23:16	00h RW	**Ose_sram_region2_base 16 To 23 (SRAM_RGN2_BASE_PRG1):** This can be programmed.
15:10	00h RW	**Ose_sram_region2_base 10 To 15 (SRAM_RGN2_BASE_PRG0):** This can be programmed.
9:0	000h RO	**Non Accessable Bits 9 To 0 (SRAM_RGN2_BASE_NON):** These are non accessable bits.

14.7.1.85 Reg Ose_sram_region2_size (SRAM_REGION_2_SIZE) — Offset 4070040Ch

This register needs to be programmed by firmware to configure the offset/size for the region 2 in SRAM l2 that can be accessed by HOST. The protection region is not present when SIZE=0. When SIZE>0, the size of the protection region is calculated as ((2^(SIZE-1))*(2^10)).

Type	Size	Offset	Default
MMIO	32 bit	4070040Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	00h RW	**Ose_sram_region2_size 3 To 7 (SRAM_RGN2_SIZE_PRG):** This can be programmed.
2:0	0h RO	**Ose_sram_region2_size 0 To 2 (SRAM_RGN2_SIZE_NON):** These are non accessable bits.

14.7.1.86 Reg Ose_sram_region3_base (SRAM_REGION_3_BASE) — Offset 40700410h

This register has to be programmed by firmware to configure region 3 start address/ base address in SRAM I2 that can be accessed by host.

Type	Size	Offset	Default
MMIO	32 bit	40700410h	60000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	60h RW	**Ose_sram_region3_base 24 To 31 (SRAM_RGN3_BASE_PRG2):** This can be programmed.
23:16	00h RW	**Ose_sram_region3_base 16 To 23 (SRAM_RGN3_BASE_PRG1):** This can be programmed.
15:10	00h RW	**Ose_sram_region3_base 10 To 15 (SRAM_RGN3_BASE_PRG0):** This can be programmed.
9:0	000h RO	**Non Accessable Bits 9 To 0 (SRAM_RGN3_BASE_NON):** These are non accessable bits.

14.7.1.87 Reg Ose_sram_region3_size (SRAM_REGION_3_SIZE) — Offset 40700414h

This register needs to be programmed by firmware to configure the offset/size for the region 2 in SRAM l2 that can be accessed by HOST. The protection region is not present when SIZE=0. When SIZE>0, the size of the protection region is calculated as ((2^(SIZE-1))*(2^10)).

Type	Size	Offset	Default
MMIO	32 bit	40700414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	00h RW	**Ose_sram_region3_base 3 To 7 (SRAM_RGN3_SIZE_PRG):** This can be programmed.
2:0	0h RO	**Ose_sram_region3_base 0 To 2 (SRAM_RGN3_SIZE_NON):** These are non accessable bits.

14.7.1.88 Reg Ose_sram_region4_base (SRAM_REGION_4_BASE) — Offset 40700418h

This register has to be programmed by firmware to configure region 4 start address/ base address in SRAM l2 that can be accessed by host.

Type	Size	Offset	Default
MMIO	32 bit	40700418h	60000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	60h RW	**Ose_sram_region4_base 24 To 31 (SRAM_RGN4_BASE_PRG2):** This can be programmed.

Bit Range	Default & Access	Field Name (ID): Description
23:16	00h RW	**Ose_sram_region4_base 16 To 23 (SRAM_RGN4_BASE_PRG1):** This can be programmed.
15:10	00h RW	**Ose_sram_region4_base 10 To 15 (SRAM_RGN4_BASE_PRG0):** This can be programmed.
9:0	000h RO	**Non Accessable Bits 9 To 0 (SRAM_RGN4_BASE_NON):** These are non accessable bits.

14.7.1.89 Reg Ose_sram_region4_size (SRAM_REGION_4_SIZE) — Offset 4070041Ch

This register needs to be programmed by firmware to configure the offset/size for the region 2 in SRAM l2 that can be accessed by HOST. The protection region is not present when SIZE=0. When SIZE>0, the size of the protection region is calculated as ((2^(SIZE-1))*(2^10)).

Type	Size	Offset	Default
MMIO	32 bit	4070041Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:3	00h RW	**Ose_sram_region4_base 3 To 7 (SRAM_RGN4_SIZE_PRG):** This can be programmed.
2:0	0h RO	**Ose_sram_region4_base 0 To 2 (SRAM_RGN4_SIZE_NON):** These are non accessable bits.

14.7.1.90 FUSA_HBW_FABRIC_PARITY_LOG — Offset 40700800h

Parity error for HBW fabric.

Type	Size	Offset	Default
MMIO	32 bit	40700800h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RO	**ETHNET1_IAXI_IPRG:** Parity log for ethnet1_iaxi_iprg.
29	0h RO	**ETHNET0_IAXI_IPRG:** Parity log for ethnet0_iaxi_iprg.
28	0h RO	**IOSF2AXI_VC1_TAXI_TPWG:** Parity log for iosf2axi_vc1_taxi_tpwg.
27	0h RO	**IOSF2AXI_VC0_TAXI_TPWG:** Parity log for iosf2axi_vc0_taxi_tpwg.
26	0h RO	**IOSF2AXI_IAXI_IPRG:** Parity log for iosf2axi_iaxi_iprg.
25	0h RO	**ETHNET1_MISC_REG_TOCP_TPMDATA:** Parity log for ethnet1_misc_reg_tocp_tpMData.
24	0h RO	**ETHNET1_REG_TAHB_TPHWDATA:** Parity log for ethnet1_reg_tahb_tphwdata.
23	0h RO	**ETHNET0_MISC_REG_TOCP_TPMDATA:** Parity log for ethnet0_misc_reg_tocp_tpMData.
22	0h RO	**ETHNET0_REG_TAHB_TPHWDATA:** Parity log for ethnet0_reg_tahb_tphwdata.
21	0h RO	**CAN1_REG_TAHB_TPHWDATA:** Parity log for can1_reg_tahb_tphwdata.
20	0h RO	**CAN0_REG_TAHB_TPHWDATA:** Parity log for can0_reg_tahb_tphwdata.
19	0h RO	**PER1_FABRIC_TOCP_TPMDATA:** Parity log for per1_fabric_tocp_tpMData.
18	0h RO	**PER0_FABRIC_TOCP_TPMDATA:** Parity log for per0_fabric_tocp_tpMData.
17	0h RO	**TAP2OCP_IOCP_IPSDATA:** Parity log for tap2ocp_iocp_ipSData.
16	0h RO	**SRAM1_MEM_TOCP_TPMDATA:** Parity log for sram1_mem_tocp_tpMData.
15	0h RO	**SRAM0_MEM_TOCP_TPMDATA:** Parity log for sram0_mem_tocp_tpMData.
14	0h RO	**SRAM0_REG_TOCP_TPMDATA:** Parity log for sram0_reg_tocp_tpMData.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**ARM_AXIM_IOCP_IPSDATA:** Parity log for arm_axim_iocp_ipSData.
12	0h RO	**LMT_IOCP_IPSDATA:** Parity log for lmt_iocp_ipSData.
11	0h RO	**DMA2_RD_IOCP_IPSDATA:** Parity log for dma2_rd_iocp_ipSData.
10	0h RO	**DMA2_MISC_REG_TOCP_TPMDATA:** Parity log for dma2_misc_reg_tocp_tpMData.
9	0h RO	**DMA2_REG_TOCP_TPMDATA:** Parity log for dma2_reg_tocp_tpMData.
8	0h RO	**DMA1_RD_IOCP_IPSDATA:** Parity log for dma1_rd_iocp_ipSData.
7	0h RO	**DMA1_MISC_REG_TOCP_TPMDATA:** Parity log for dma1_misc_reg_tocp_tpMData.
6	0h RO	**DMA1_REG_TOCP_TPMDATA:** Parity log for dma1_reg_tocp_tpMData.
5	0h RO	**DMA0_RD_IOCP_IPSDATA:** Parity log for dma0_rd_iocp_ipSData.
4	0h RO	**DMA0_MISC_REG_TOCP_TPMDATA:** Parity log for dma0_misc_reg_tocp_tpMData.
3	0h RO	**DMA0_REG_TOCP_TPMDATA:** Parity log for dma0_reg_tocp_tpMData.
2	0h RO	**Reserved**
1	0h RO	**AONRF_MEM_TOCP_TPMDATA:** Parity log for aonrf_mem_tocp_tpMData.
0	0h RO	**DEVICE_IDLE_REG_TOCP_TPMDATA:** Parity log for device_idle_reg_tocp_tpMData.

14.7.1.91 FUSA_PER0 FABRIC PARITY_LOG (FUSA_PER0_FABRIC_PARITY_LOG) — Offset 40700804h

Parity error for PER0 fabric.

Type	Size	Offset	Default
MMIO	32 bit	40700804h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**PER0_FABRIC_IOCP_IPSDATA:** Parity log for wdt_reg_tocp_tpMData.
24	0h RO	**WDT_REG_TOCP_TPMDATA:** Parity log for sbep_reg_tocp_tpMData.
23	0h RO	**SBEP_REG_TOCP_TPMDATA:** Parity log for pmu_reg_tocp_tpMData.
22	0h RO	**PMU_REG_TOCP_TPMDATA:** Parity log for sec_reg_tocp_tpMData.
21	0h RO	**SEC_REG_TOCP_TPMDATA:** Parity log for att_reg_tocp_tpMData.
20	0h RO	**ATT_REG_TOCP_TPMDATA:** Parity log for misc_reg_tocp_tpMData.
19	0h RO	**MISC_REG_TOCP_TPMDATA:** Parity log for ip_dashboard_reg_tocp_tpMData.
18	0h RO	**IP_DASHBOARD_REG_TOCP_TPMDATA:** Parity log for ipc_reg_tocp_tpMData.
17	0h RO	**IPC_REG_TOCP_TPMDATA:** Parity log for i2c7_per_tapb_tppwdata.
16	0h RO	**I2C7_PER_TAPB_TPPWDATA:** Parity log for i2c6_per_tapb_tppwdata.
15	0h RO	**I2C6_PER_TAPB_TPPWDATA:** Parity log for i2c5_per_tapb_tppwdata.
14	0h RO	**I2C5_PER_TAPB_TPPWDATA:** Parity log for i2c4_per_tapb_tppwdata.
13	0h RO	**I2C4_PER_TAPB_TPPWDATA:** Parity log for i2c3_per_tapb_tppwdata.
12	0h RO	**I2C3_PER_TAPB_TPPWDATA:** Parity log for i2c2_per_tapb_tppwdata.
11	0h RO	**I2C2_PER_TAPB_TPPWDATA:** Parity log for i2c1_per_tapb_tppwdata.
10	0h RO	**I2C1_PER_TAPB_TPPWDATA:** Parity log for i2c0_per_tapb_tppwdata.
9	0h RO	**I2C0_PER_TAPB_TPPWDATA:** Parity log for pll_reg_tapb_tppwdata.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**PLL_REG_TAPB_TPPWDATA:** Parity log for hpet_reg_tocp_tpMData.
7	0h RO	**HPET_REG_TOCP_TPMDATA:** Parity log for tgpio1_per_tocp_tpMData.
6	0h RO	**TGPIO1_PER_TOCP_TPMDATA:** Parity log for tgpio0_per_tocp_tpMData.
5	0h RO	**TGPIO0_PER_TOCP_TPMDATA:** Parity log for gpio1_per_tapb_tppwdata.
4	0h RO	**GPIO1_PER_TAPB_TPPWDATA:** Parity log for gpio0_per_tapb_tppwdata.
3	0h RO	**GPIO0_PER_TAPB_TPPWDATA:** Parity log for dtf_reg_tocp_tpMData.
2	0h RO	**DTF_REG_TOCP_TPMDATA:** Parity log for ccu_reg_tocp_tpMData.
1	0h RO	**CCU_REG_TOCP_TPMDATA:** Parity log for device_idle_reg_tocp_tpMData.
0	0h RO	**DEVICE_IDLE_REG_TOCP_TPMDATA:** Parity log for device_idle_reg_tocp_tpMData.

14.7.1.92 FUSA_PER1 FABRIC PARITY_LOG (FUSA_PER1_FABRIC_PARITY_LOG) — Offset 40700808h

Parity error for PER1 fabric.

Type	Size	Offset	Default
MMIO	32 bit	40700808h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**QEP3_PER_TAPB_TPPWDATA:** Parity log for qep3_per_tapb_tppwdata.
19	0h RO	**QEP2_PER_TAPB_TPPWDATA:** Parity log for qep2_per_tapb_tppwdata.
18	0h RO	**QEP1_PER_TAPB_TPPWDATA:** Parity log for qep1_per_tapb_tppwdata.
17	0h RO	**QEP0_PER_TAPB_TPPWDATA:** Parity log for qep0_per_tapb_tppwdata.
16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PWM1_PER_TAPB_TPPWDATA:** Parity log for pwm1_per_tapb_tppwdata.
14	0h RO	**PWM0_PER_TAPB_TPPWDATA:** Parity log for pwm0_per_tapb_tppwdata.
13	0h RO	**I2S1_PER_TAPB_TPPWDATA:** Parity log for i2s1_per_tapb_tppwdata.
12	0h RO	**I2S0_PER_TAPB_TPPWDATA:** Parity log for i2s0_per_tapb_tppwdata.
11	0h RO	**SPI3_PER_TAPB_TPPWDATA:** Parity log for spi3_per_tapb_tppwdata.
10	0h RO	**SPI2_PER_TAPB_TPPWDATA:** Parity log for spi2_per_tapb_tppwdata.
9	0h RO	**SPI1_PER_TAPB_TPPWDATA:** Parity log for spi1_per_tapb_tppwdata.
8	0h RO	**SPI0_PER_TAPB_TPPWDATA:** Parity log for spi0_per_tapb_tppwdata.
7	0h RO	**UART5_PER_TAPB_TPPWDATA:** Parity log for uart5_per_tapb_tppwdata.
6	0h RO	**UART4_PER_TAPB_TPPWDATA:** Parity log for uart4_per_tapb_tppwdata.
5	0h RO	**UART3_PER_TAPB_TPPWDATA:** Parity log for uart3_per_tapb_tppwdata.
4	0h RO	**UART2_PER_TAPB_TPPWDATA:** Parity log for uart2_per_tapb_tppwdata.
3	0h RO	**UART1_PER_TAPB_TPPWDATA:** Parity log for uart1_per_tapb_tppwdata.
2	0h RO	**UART0_PER_TAPB_TPPWDATA:** Parity log for uart0_per_tapb_tppwdata.
1	0h RO	**PER1_FABRIC_IOCP_IPSDATA:** Parity log for per1_fabric_iocp_ipSData.
0	0h RO	**DEVICE_IDLE_0_REG_TOCP_TPMDATA:** Parity log for device_idle_0_reg_tocp_tpMData.

14.7.1.93 FUSA_MEM PARITY_LOG (FUSA_MEM_PARITY_LOG) — Offset 4070080Ch

Parity error for different memories fabric.

Type	Size	Offset	Default
MMIO	32 bit	4070080Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**ERROR_LOG_DATA_READ_DATA_CACHE:** Fatal error on data read for Data Cache.
6	0h RO	**ERROR_LOG_TAG_READ_DATA_CACHE:** Fatal error on tag read for Data Cache.
5	0h RO	**ERROR_LOG_DATA_READ_INSTRUCTION_CACHE:** Fatal error on data read for Instruction Cache.
4	0h RO	**ERROR_LOG_TAG_READ_INSTRUCTION_CACHE:** Fatal error on tag read for Instruction Cache.
3	0h RO	**Reserved**
2	0h RO	**BOOT_ROM_PARITY:** Boot ROM parity odd Error bit.
1	0h RO	**AON_RF_PARITY:** AON RF parity odd Error bit.
0	0h RO	**SRAM_DED_ERROR:** SRAM DED error bit.

14.7.1.94 FUSA_ARM DC ERROR_LOG (FUSA_ARM_DC_ERROR_LOG) — Offset 40700810h

This register reports information about the current status of the Data cache Error Bank Registers(DEBR), which of these Error Bank Registers have been allocated to this cycle, and information about any allocation that has occurred.

Type	Size	Offset	Default
MMIO	32 bit	40700810h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**DEBR1 Locked (DEBR1_LOCKED):** Indicates whether DEBR1 is locked.
20	0h RO	**DEBR1 Valid (DEBR1_VALID):** Indicates whether DEBR1 is valid.
19	0h RO	**DEBR0 Locked. (DEBR0_LOCKED):** Indicates whether DEBR0 is loked . 0 - Not Loked , 1 -Locked. No hardware allocations.
18	0h RO	**DEBR0 Valid. (DEBR0_VALID):** Indicates whether DEBR0 is valid.
17:2	0000h RO	**Data Allocation (DATA_ALLOCATION):** Data to be allocated. Corresponds to bits [17:2] of data to be written to Error Bank Register. Only valid when DCERR[1:0] is not b00.
1:0	0h RO	**Allocation Status (ALLOCATION_STATUS):** Allocation status. 00 - No allocation,10 Allocation into DEBR0,11 - Allocation into DEBR1,01 - attempted allocation but both entries are locked. Will not allocate.

14.7.1.95 FUSA_ARM IC ERROR_LOG (FUSA_ARM_IC_ERROR_LOG) — Offset 40700814h

This register reports information about the current status of the instruction cache Error Bank Registers(IEBR), which of these Error Bank Registers have been allocated to this cycle, and information about any allocation that has occurred.

Type	Size	Offset	Default
MMIO	32 bit	40700814h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**IEBR1 Locked (IEBR1_LOCKED):** Indicates whether IEBR1 is locked.
20	0h RO	**IEBR1 Valid (IEBR1_VALID):** Indicates whether IEBR1 is valid.
19	0h RO	**IEBR0 Locked. (IEBR0_LOCKED):** Indicates whether IEBR0 is loked . 0 - Not Loked , 1 -Locked. No hardware allocations.
18	0h RO	**IEBR0 Valid. (IEBR0_VALID):** Indicates whether IEBR0 is valid.
17:2	0000h RO	**Data Allocation (DATA_ALLOCATION):** Data to be allocated. Corresponds to bits [17:2] of data to be written to Error Bank Register. Only valid when ICERR[1:0] is not b00.
1:0	0h RO	**Allocation Status (ALLOCATION_STATUS):** Allocation status. 00 - No allocation,10 Allocation into IEBR0,11 - Allocation into IEBR1,01 - attempted allocation but both entries are locked. Will not allocate.

14.7.1.96 FUSA BRIDGE_PARTY_LOG0 (FUSA_BRIDGE_PARTY_LOG0) — Offset 40700818h

This register is clear when FUSA_CTRL.LOG_CLR is set to 1.Set when there is a data parity error for PCI function [31:0].

Type	Size	Offset	Default
MMIO	32 bit	40700818h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**FUSA_BRIDGE_PARTY_LOG0:** This register is clear when FUSA_CTRL.LOG_CLR is set to 1.Set when there is a data parity error for PCI function [31:0].

14.7.1.97 FUSA BRIDGE_PARTY_LOG1 (FUSA_BRIDGE_PARTY_LOG1) — Offset 4070081Ch

This register is clear when FUSA_CTRL.LOG_CLR is set to 1.Set when there is a data parity error for PCI function [36:32].

Type	Size	Offset	Default
MMIO	32 bit	4070081Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO	**FUSA_BRIDGE_PARTY_LOG1:** This register is clear when FUSA_CTRL.LOG_CLR is set to 1.Set when there is a data parity error for PCI function [36:32].

14.7.1.98 FUSA CONTROL (FUSA_CTRL) — Offset 40700820h

Fusa control register.

Type	Size	Offset	Default
MMIO	32 bit	40700820h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**FABRIC_PARITY_DISABLE:** Disables Fabric parity check. Also clear fabric parity log registers. It may take upto 5 clks to clear. Check FUSA_*_FABRIC_PARITY_LOG registers to confirm when it is cleared.
0	0h RW	**LOG_CLR:** Clears log other than fabric fusa parity.

14.7.1.99 ISH_FW_ALIVE — Offset 40700900h

On raising NMI, FW needs to write pattern 0xDEADBEEF into this register before ish_fw_timer expires. If FW is not alive and timer expires, global reset is issued.

Type	Size	Offset	Default
MMIO	32 bit	40700900h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ISH_FW_ALIVE:** On raising NMI, FW needs to write pattern 0xDEADBEEF into this register before ish_fw_timer expires. If FW is not alive and timer expires, global reset is issued.

14.7.1.100 ISH_FW_TIMEOUT — Offset 40700904h

On raising NMI, down counter starts with ish_fw_timeout value. FW needs to write pattern before counter expires.

Type	Size	Offset	Default
MMIO	32 bit	40700904h	000186A0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	000186A0h RW	**ISH_FW_TIMEOUT:** On raising NMI, down counter starts with ish_fw_timeout value. FW needs to write pattern before counter expires.

14.7.1.101 ISH_NMI_STATUS — Offset 40700908h

Indicates NMI to ARM.

Type	Size	Offset	Default
MMIO	32 bit	40700908h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW/1C	**DMA UR From Psf (DMA_UR_INTR):** DMA resp error from PSF in ARM owend mode. In host owned mode, this bit internally tied to '0'.
3	0h RW/1C	**Cpu Exception Intr (CPU_EXCEPTION_INTR):** ARM lockup, fpixc, fpidc, fpofc, fpufc, fpdzc, fpioc errors.
2	0h RO	**Reserved**
1	0h RW/1C	**Wdt Expiry Intr (WDT_EXP_INTR):** Sram ecc, fabric parity, aon_rf parity , brom parity errors.
0	0h RW/1C	**Ecc Parity Intr (ECC_PARITY_INTR):** Bridge parity error.

14.8 SBEP Registers

SBEP Registers	Address Offset	Table
SBEP	40800000h - 40800084h	Table 14-18

14.8.1 SBEP Registers Summary

Table 14-18. Summary of SBEP Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40800000h	4	Attribute Reg (DS_ATTRIBUTES)	00000000h
40800004h	4	Address Reg LO (DS_ADDRESS_LSB)	00000000h
40800008h	4	Address Reg HI (DS_ADDRESS_MSB)	00000000h
4080000Ch	4	Extended Header (SAIRS) (DS_SAI)	00000000h
40800010h	4	Received Data (DS_DATA_IN)	00000000h
40800014h	4	Control And Status (DS_CONTROL_STATUS)	00000000h
40800018h	4	ISH Source Port ID (DS_SOURCEPORTID)	00000000h
40800020h	4	Completion Data (DS_CMP_DATA)	00000000h
40800024h	4	Completion SAI (DS_CMP_SAI)	00000000h
40800028h	4	Completion Status And Control (DS_CMP_STATUS)	00000000h
40800040h	4	Status Reg (US_STATUS)	00000000h
40800044h	4	Command Reg (US_COMMAND)	00000000h
40800048h	4	Target AddressLO (US_TARGET_LO)	00000000h
4080004Ch	4	Target AddressHI (US_TARGET_HIGH)	00000000h
40800050h	4	Target Out Data (US_TARGET_DATA)	00000000h
40800054h	4	Upstream Attribute (US_ATTRIBUTES)	00000000h
40800058h	4	Upstream Request SAIRS (US_SAIR)	80000000h
4080005Ch	4	Upstream Completion Data (US_CMP_DATA)	00000000h
40800060h	4	Upstream Completion Status And Control (US_CMP_STATUS_CONTROL)	00000000h
40800064h	4	Upstream Completion SAI (US_CMP_SAIR)	00000034h
40800068h	4	SAI_WIDTH Reg (SAI_WIDTH)	00000007h
4080006Ch	4	Side Clk Gate Enable (SIDE_CLK_GATE_EN)	00000000h
40800074h	4	Received Data (DS_DATA_IN_DW2)	00000000h
40800080h	4	DN Access Valid Enable (DS_ACCESS_VALID_EN)	00000000h
40800084h	4	Boot Prep Control (BOOT_PREP_CONTROL_REG)	00000000h

14.8.1.1 Attribute Reg (DS_ATTRIBUTES) — Offset 40800000h

Attribute Register.

Type	Size	Offset	Default
MMIO	32 bit	40800000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:24	0h WO	**BYTE_ENABLE_OF_THE_DWORD:** Byte enables. First byte enables.
23:16	00h WO	**OPCODE_OF_MESSAGE:** Opcode of messages.
15:8	00h WO	**SOURCE_PORT_ID:** Source Port ID.
7:0	00h WO	**DESTINATION_PORT_ID:** Destination Port ID.

14.8.1.2 Address Reg LO (DS_ADDRESS_LSB) — Offset 40800004h

Downstream Address Register LO.

Type	Size	Offset	Default
MMIO	32 bit	40800004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**ADDRESS_LSB:** Address[31:0].

14.8.1.3 Address Reg HI (DS_ADDRESS_MSB) — Offset 40800008h

Downstream Address Register HI.

Type	Size	Offset	Default
MMIO	32 bit	40800008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Address Length (ADDRESS_LENGTH):** Indicates the length of the address field as follows: 0: 16-bit address 1: 48-bit address .
30:16	0h RO	**Reserved**
15:0	0000h WO	**ADDRESS_MSB:** Address[47:32].

14.8.1.4 Extended Header (SAIRS) (DS_SAI) — Offset 4080000Ch

Downstream Extended Header (SAIRS) Register.

Type	Size	Offset	Default
MMIO	32 bit	4080000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**VALID:** EH Present SAI preset- when 1, 23:0 bits are valid.
30:20	0h RO	**Reserved**
19:16	0h WO	**ROOT_SPACE:** Root Space field received in message.
15:0	0000h WO	**SAI:** SAI Security attribute indicator.

14.8.1.5 Received Data (DS_DATA_IN) — Offset 40800010h

Downstream Received Data Register.

Type	Size	Offset	Default
MMIO	32 bit	40800010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**DATA_RECEIVED:** Data received in message.

14.8.1.6 Control And Status (DS_CONTROL_STATUS) — Offset 40800014h

Downstream Control and status Register.

Type	Size	Offset	Default
MMIO	32 bit	40800014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**MSG_RX_STATUS:** Message received interrupt - Message received interrupt status register. Written by HW and cleared HW itself when MinuteIA writes to upstream completion control register indicating completion is available. When cleared interrupt going to MinuteIA goes low.
30	0h RW	**INTERRUPT_MASK:** Interrupt mask register for message received interrupt. When set to 1 interrupt is not generated to MinuteIA. Mask does not affect interrupt status bit.
29:2	0h RO	**Reserved**
1:0	0h RO	**TYPE_OF_TRANSACTION:** Type of transaction: indicates type of transaction received as follows: 2 b001 : Posted message 2 b010 : Non-posted message 2 b1011: Completion message.

14.8.1.7 ISH Source Port ID (DS_SOURCEPORTID) — Offset 40800018h

Downstream Source Port ID.

Type	Size	Offset	Default
MMIO	32 bit	40800018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**SOURCE_PORT_ID:** (Reset value is 0, straps will get loaded runtime) Source ID of ISH. Default value is coming from top level straps.

14.8.1.8 Completion Data (DS_CMP_DATA) — Offset 40800020h

Downstream completion Data Register.

Type	Size	Offset	Default
MMIO	32 bit	40800020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**COMPLETION_DATA:** Completion data received for upstream non-posted read.

14.8.1.9 Completion SAI (DS_CMP_SAI) — Offset 40800024h

Downstream Completion SAI Registers.

Type	Size	Offset	Default
MMIO	32 bit	40800024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**COMPLETION_SAI:** Completion SAI received for upstream non-posted read.

14.8.1.10 Completion Status And Control (DS_CMP_STATUS) — Offset 40800028h

Downstream Completion status and control Register.

Type	Size	Offset	Default
MMIO	32 bit	40800028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**COMPLETION_RECEIVED:** Completion received status register. Set by HW and cleared by FW by writing 1 to it.
30	0h RW	**INTERRUPT_MASK:** Interrupt mask register for completion received interrupt. When set to 1 interrupt is not generated to MinuteIA. Mask does not affect interrupt status bit.
29:9	0h RO	**Reserved**
8	0h RO	**DN_CMPL_EHPRESENT:** EH present for Downstream completion (ISH4 Only).
7:3	0h RO	**Reserved**
2:0	0h RO	**Completion Status (COMPLETION_STATUS):** 000: Successful Completion (SC) 001: Unsupported Request (UR).

14.8.1.11 Status Reg (US_STATUS) — Offset 40800040h

Upstream status register.

Type	Size	Offset	Default
MMIO	32 bit	40800040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW/1C	**Message Sent (MSG_SENT):** Upstream message sent interrupt status 1, Upstream message has been sent out. This is cleared FW by writing 1 to it.
0	0h RO	**SM Status (STATE_MACHINE_STATUS):** 1 = The Endpoint State Machine is busy. 0 = The Endpoint Status Machine is idle. This is OR of posted SM and NP SM busy signals.

14.8.1.12 Command Reg (US_COMMAND) — Offset 40800044h

Upstream Command Register.

Type	Size	Offset	Default
MMIO	32 bit	40800044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Interrupt Enable (ENABLE_INTERRUPT):** 1 = Cause an interrupt when the transaction completes.
2	0h RW	**Message Type (TYPE_OF_MSG):** 1 = Transaction will be Posted 0 = Transaction will be non-posted will be hardcoded to 0 indicating NP message For posted message register (new) this field would be hardcoded to 1. .
1	0h RW	**Transaction Command Type (TRANSACTION_TYPE):** 1 = Transaction will be a Read 0 = Transaction will be a Write For posted message register (new) this bit will be hardcoded to 0 as reads cannot be P .
0	0h RW	**SEND_IOSF_SB_TRANSACTION:** MinuteIA writes a 1 to this bit to cause an IOSF SB Transaction. The type of transaction is determined by Bit 1 in this register. *This bit will always be read as 0 but FW can write it to 1 to start the upstream transaction. In that way it won't be readable as 1 after writing to.

14.8.1.13 Target AddressLO (US_TARGET_LO) — Offset 40800048h

Target Address Register LO.

Type	Size	Offset	Default
MMIO	32 bit	40800048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Address Low (ADDRESS_LOW):** Address of message. Offset within the Target s IOSF SB Port.

14.8.1.14 Target AddressHI (US_TARGET_HIGH) — Offset 4080004Ch

Target Address Register HI.

Type	Size	Offset	Default
MMIO	32 bit	4080004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Length (ADDRESS_LENGTH):** Indicates the length of the address field as follows: 0: 16-bit address 1: 48-bit address.
30:16	0h RO	**Reserved**
15:0	0000h RW	**Address MSB (ADDRESS_HIGH):** MSB 16 address bits, valid only when bit 31 is set to 1.

14.8.1.15 Target Out Data (US_TARGET_DATA) — Offset 40800050h

Target Out data Register.

Type	Size	Offset	Default
MMIO	32 bit	40800050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA_SENT:** The MinuteIA writes the data value that will be sent on the next write IOSF SB Transaction.

14.8.1.16 Upstream Attribute (US_ATTRIBUTES) — Offset 40800054h

Upstream Attribute Register.

Type	Size	Offset	Default
MMIO	32 bit	40800054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**FID:** FID.
23:20	0h RW	**BAR:** BAR for upstream register access.
19:16	0h RW	**BYTE_ENABLE_FOR_THE_MSG:** Upstream byte enables. 19:16 FBE.
15:8	00h RW	**OPCODE:** Message Opcode. This Opcode will go as Opcode for upstream message.
7:0	00h RW	**DESTINATION_PORT_ID:** Destination ID of upstream message. For ex. Ifwhen the upstream message is targeted to PMC then.FW writes to this register with destination ID of PMC.

14.8.1.17 Upstream Request SAIRS (US_SAIR) — Offset 40800058h

Upstream request SAIRS Register.

Type	Size	Offset	Default
MMIO	32 bit	40800058h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**EH Present (EH_PRESET):** Extended header present indication. When set to 1 indicates extended header is present. Currently tied to 1 in RTL as ISH supports only EH=1 transactions.
30:20	0h RO	**Reserved**
19:16	0h RW	**ROOT_SPACE:** Root space..
15:11	0h RO	**Reserved**
10:8	0h RW	**TAG:** Tag.
7:0	00h RO	**SAI_OF_IOSF_SBEP:** ISH SAI to be inserted in all upstream messages with if EH_present bit is set to 1. Reset value is 0, straps will get loaded runtime .

14.8.1.18 Upstream Completion Data (US_CMP_DATA) — Offset 4080005Ch

Upstream Completion Data Register.

Type	Size	Offset	Default
MMIO	32 bit	4080005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**COMPLETION_DATA:** Completion data to be used for upstream completion as a result of downstream read request. This field is valid only downstream when type of transfer register indicates non-posted type of transaction.

14.8.1.19 Upstream Completion Status And Control (US_CMP_STATUS_CONTROL) — Offset 40800060h

Upstream Completion status and control Register.

Type	Size	Offset	Default
MMIO	32 bit	40800060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/AC	**IOSF_SB_COMPLETION:** Upstream completion for Downstream request. MinuteIA writes a 1 to this bit to indicate downstream message received is consumed. This internally causes an IOSF SB completion Transaction if original downstream request is non-posted. If original message is posted then upstream completion is not generated by HW. to it. This bit cleared by HW.
30:3	0h RO	**Reserved**
2:0	0h RW	**COMPLETION_STATUS:** Completion Status 000: Successful Completion (SC) 001: Unsupported Request (UR).

14.8.1.20 Upstream Completion SAI (US_CMP_SAIR) — Offset 40800064h

Upstream completion SAI Register.

Type	Size	Offset	Default
MMIO	32 bit	40800064h	00000034h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	34h RO	**SAI_STRAP_FOR_COMPLETION:** SAI for ISH which will be inserted in upstream completion. Reset value is 0, straps will get loaded runtime .

14.8.1.21 SAI_WIDTH Reg (SAI_WIDTH) — Offset 40800068h

Register for SAI_WIDTH.

Type	Size	Offset	Default
MMIO	32 bit	40800068h	00000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	7h RO	**SAI_WIDTH:** Specifies the SAI Width value.

14.8.1.22 Side Clk Gate Enable (SIDE_CLK_GATE_EN) — Offset 4080006Ch

Register for Side clk gate enable.

Type	Size	Offset	Default
MMIO	32 bit	4080006Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Trunk Clk Gate (JTAG_FORCE_CLKREQ):** 0: Clk request enable 1: Clk is gated.
0	0h RW	**Local Clk Gate (CG_CTRL_CLKGATEDEF):** 0: Clk is un-gated 1: Clk is gated.

14.8.1.23 Received Data (DS_DATA_IN_DW2) — Offset 40800074h

Downstream Received Data Register DW2.

Type	Size	Offset	Default
MMIO	32 bit	40800074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**Data Received (DATA_RECEIVED):** Data received in message. DW2.

14.8.1.24 DN Access Valid Enable (DS_ACCESS_VALID_EN) — Offset 40800080h

Downstream access valid enable.

Type	Size	Offset	Default
MMIO	32 bit	40800080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**DS_ACCESS_VALID_EN_RSVD:** Reserved
0	0h RW	**Access Valid Enable For DS (ACCESS_VALID_ENABLE):** Downstream messages PMC access valid Enable: This bit is set by ISH FW to enable SBEP HW to accept downstream cycles from PMC, Hammock Harbor ART agent, Audio, ISP, CSME, GPIO, DFX Trusted0 Red2, DFX Trusted1 Red4, DFX Trusted2 Orange and interrupt ISH upon such an event. Note that ISH HW chooses the SAI value corresponding to this agent. NOTE: If a BOOTPREP message is received, ISH FW is interrupted unconditionally, i.e. irrespective of this bit being 1 or 0. .

14.8.1.25 Boot Prep Control (BOOT_PREP_CONTROL_REG) — Offset 40800084h

BOOT PREP CONTROL register.

Type	Size	Offset	Default
MMIO	32 bit	40800084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**Boot Prep Received Status (BOOT_PREP_RECEIVED_STATUS):** This bit is set by SBEP HW upon the reception of Boot Prep message. ISH FW is required to clear this status bit by writing 0, upon issuing Boot Prep Ack message on the upstream path of SBEP HW. SBEP HW will clear this bit, upon auto ack ing of Boot Prep due to timeout condition.

14.9 DTF Registers

DTF Registers	Address Offset	Table
DTF	40900000h - 4090000Ch	Table 14-19

14.9.1 DTF Registers Summary

Table 14-19. Summary of DTF Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40900000h	4	DTF Packetizer Source Configuration (PCKTZR_DTF_SRC_CONFIG)	00000000h
40900004h	4	DTF Packetizer Source Status (PCKTZR_DTF_SRC_STATUS)	00000000h
40900008h	4	DTF Encoder Source Config (ENCDR_DTF_SRC_CONFIG)	00000000h
4090000Ch	4	DTF Encoder Source Status (ENCDR_DTF_SRC_STATUS)	00000000h

14.9.1.1 DTF Packetizer Source Configuration (PCKTZR_DTF_SRC_CONFIG) — Offset 40900000h

This register allow software enabling of the individual source, as well as software specification of the trace aggregator destination.

Type	Size	Offset	Default
MMIO	32 bit	40900000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**Encoder Clock Gating Override (ENC_CG_OVRD):** Encoder clock gating override.
1	0h RW	**Destination ID (DEST_ID):** This bit specifies which trace aggregator to use.
0	0h RW	**Source Enable (SRC_EN):** Enable for source packetizer.

14.9.1.2 DTF Packetizer Source Status (PCKTZR_DTF_SRC_STATUS) — Offset 40900004h

This register allow software discovery and debug of the master and channel ID produced by this source packetizer.

Type	Size	Offset	Default
MMIO	32 bit	40900004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BUSY:** If set, encoder is not in a state to accept data from packetiser.
30	0h RO	**Encoder FIFO Empty (ENC_FIFO_EMPTY):** This bit is set when encoder indicates FIFO empty.
29	0h RO	**Arbiter Empty (ARBITER_EMPTY):** This bit is set when the empty signal from arbiter is asserted.
28	0h RO	**Encoder Active (ENC_ACTIVE):** This bit is set when the active signal from encoder is asserted.
27:18	0h RO	**Reserved**
17:16	0h RO	**Timestamp Bit Shift Value (TS_BIT_SHFT_VAL):** Bit shift value for FW inserted TS driven by SOC.
15:8	00h RO	**Channel ID (CHNL_ID):** Channel ID.
7:0	00h RO	**Master ID (MSTR_ID):** Master ID.

14.9.1.3 DTF Encoder Source Config (ENCDR_DTF_SRC_CONFIG) — Offset 40900008h

This register to allow some survivability and debug-ability if there is an issue in the DTF.

Type	Size	Offset	Default
MMIO	32 bit	40900008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:3	0h RW	**Pattern Selected (PATT_SEL):** Select pattern for Debug.
2	0h RW	**Pattern Enable (PATT_EN):** Pattern generation enabled.
1	0h RW	**EOF Control Enable (EOF_EN):** EOF Control Enable.
0	0h RW	**Credit Control Enable (IGNORE_CR):** Credit Control Enable.

14.9.1.4 DTF Encoder Source Status (ENCDR_DTF_SRC_STATUS) — Offset 4090000Ch

This register is to provides information on states of the different FSMs and signals that are critical to the encoder functionality.

Type	Size	Offset	Default
MMIO	32 bit	4090000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:13	0h RO	**Count Valid Out (CNT_VALID_OUT):** Cnt_valid_out signal.
12:10	0h RO	**Valid Count (VALID_CNT):** Valid_cnt signal.
9	0h RO	**D_FIFO_S:** D_FIFO_s signal.
8	0h RO	**DTFE_UPSTREAM_CREDIT:** Dtfe_upstream_credit signal.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**DRAIN:** Drain signal.
6	0h RO	**Fifo Valid (FIFO_VALID):** Fifo_valid signal.
5	0h RO	**TS:** Ts signal.
4	0h RO	**FIFO_WR_INT:** Fifo_wr_int signal.
3	0h RO	**FIFO_RD_INT:** Fifo_rd_int signal.
2	0h RO	**EOF:** EOF signal.
1	0h RO	**TXID_UCI:** Txid signal.
0	0h RO	**CREDIT_OK:** Credit_ok signal can send ds data.

14.10 HPET Registers

HPET Registers	Address Offset	Table
HPET	40A00000h - 40A00160h	Table 14-20

14.10.1 HPET Registers Summary

Table 14-20. Summary of HPET Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40A00000h	4	General Capabilities And ID (GCID_LOW)	8086A201h
40A00004h	4	General Capabilities And ID (GCID_HIGH)	01D1A94Ah
40A00010h	4	General Configuration (GCFG_LOW)	00000000h
40A00014h	4	General Configuration (GCFG_HIGH)	00000000h
40A00020h	4	General Interrupt Status (GIS_LOW)	00000000h
40A00024h	4	General Interrupt Status (GIS_HIGH)	00000000h
40A000F0h	4	Main Counter Value (MCV_LOW)	00000000h
40A000F4h	4	Main Counter Value (MCV_HIGH)	00000000h
40A00100h	4	Timer N Config And Capabilities (T0C_LOW)	00000030h
40A00104h	4	Timer N Config And Capabilities (T0C_HIGH)	00F00000h
40A00108h	4	Timer N Comparator Value (T0CV_LOW)	FFFFFFFFh
40A0010Ch	4	Timer N Comparator Value (T0CV_HIGH)	FFFFFFFFh
40A00120h	4	Timer N Config And Capabilities (T1C_LOW)	00000000h
40A00124h	4	Timer N Config And Capabilities (T1C_HIGH)	00F00000h
40A00128h	4	Timer N Comparator Value (T1CV_LOW)	FFFFFFFFh
40A00140h	4	Timer N Config And Capabilities (T2C_LOW)	00000000h
40A00144h	4	Timer N Config And Capabilities (T2C_HIGH)	00F00800h
40A00148h	4	Timer N Comparator Value (T2CV_LOW)	FFFFFFFFh
40A00160h	4	HPET Control And Status (HPET_CTRL_STS)	80000000h

14.10.1.1 General Capabilities And ID (GCID_LOW) — Offset 40A00000h

HPET_GCID : Vendor ID (VID): Value of 8086h indicates Intel.

Type	Size	Offset	Default
MMIO	32 bit	40A00000h	8086A201h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	8086h RO	**Vendor ID (VID):** Value of 8086h indicates Intel.
15	1h RO	**Legacy Rout Capable (LRC):** Indicates support for Legacy Interrupt Rout.
14	0h RO	**Reserved**
13	1h RO	**Counter Size (CS):** Indicates support for Legacy Interrupt Rout.
12:8	02h RO	**Number Of Timers (NT):** Indicates that 3 timers are supported.
7:0	01h RO	**Revision ID (RID):** Indicates that revision 1.0 of the specification is implemented.

14.10.1.2 General Capabilities And ID (GCID_HIGH) — Offset 40A00004h

HPET_GCID : Counter Tick Period (CTP): Indicates the clock period.

Type	Size	Offset	Default
MMIO	32 bit	40A00004h	01D1A94Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	01D1A94Ah RO	**Counter Tick Period (CTP):** ISH2: Specified in picoseconds. Indicates a period of 1000000 ps, (1 MHz clock period) ISH3: Specified in picoseconds. Indicates a period of 83333 ps, (12 MHz clock period) ISH4: Specified in picoseconds. Indicates a period of 30517578 ps (32.768 KHz clock period) .

14.10.1.3 General Configuration (GCFG_LOW) — Offset 40A00010h

HPET_GCFG : Reserved.

Type	Size	Offset	Default
MMIO	32 bit	40A00010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW/V	**Overall Enable (EN) (LRE):** When set, interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC . Timer 1 will be routed to IRQ8 in 8259 and I/O APIC. Timer 2 will be routed as per the routing in T2C When set, the TNC.IR will have no impact for timers 0 and 1. For ISH, this bit needs to be set for routing HPET1 interrupt.
0	0h RW/V	**Overall Enable (EN):** When set, the timers can generate interrupts. When cleared, the main counter will halt and no interrupts will be caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx will not be cleared.

14.10.1.4 General Configuration (GCFG_HIGH) — Offset 40A00014h

HPET_GCFG : Reserved.

Type	Size	Offset	Default
MMIO	32 bit	40A00014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.10.1.5 General Interrupt Status (GIS_LOW) — Offset 40A00020h

HPET_GIS.

Type	Size	Offset	Default
MMIO	32 bit	40A00020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW/V	**Timer 2 Status (T2) (T2):** Same functionality as T0, for timer 2.
1	0h RW/V	**Timer 1 Status (T1) (T1):** Same functionality as T0, for timer 1.
0	0h RW/V	**Timer 0 Status (T0) (T0):** In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

14.10.1.6 General Interrupt Status (GIS_HIGH) — Offset 40A00024h

HPET_GIS.

Note: Bit definitions are the same as GCFG_HIGH, offset 40A00014h.

14.10.1.7 Main Counter Value (MCV_LOW) — Offset 40A000F0h

HPET_MCV : Counter Value (CV): Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

Type	Size	Offset	Default
MMIO	32 bit	40A000F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Counter Value (CV (MCV_LOW):** Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

14.10.1.8 Main Counter Value (MCV_HIGH) — Offset 40A000F4h

HPET_MCV : Counter Value (CV): Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

Type	Size	Offset	Default
MMIO	32 bit	40A000F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**Counter Value (CV (MCV_HIGH):** Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

14.10.1.9 Timer N Config And Capabilities (T0C_LOW) — Offset 40A00100h

HPET_T0C : reserved.

Type	Size	Offset	Default
MMIO	32 bit	40A00100h	00000030h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**FSB Interrupt Delivery (FID) (FID):** Not supported.
14	0h RO	**FSB Enable (FE) (FE):** Not supported, since FID is not supported.
13:9	00h RW/V	**Interrupt Rout (IR) (IR):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum value of 32 interrupts is supported. Default is 00h Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timer s interrupt. If the value is not supported by this particular timer, then the value read back will not match what is written. The software must only write valid values.. If GC.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect. For ISH, Timer 2 interrupt need to be routed only through IRQ 11. This field needs to be 0bh. .

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/V	**Timer 32-Bit Mode (T32M) (T32M):** When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only 0 .
7	0h RO	**Reserved**
6	0h RW/V	**Timer Value Set (TVS) (TVS):** This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	1h RO	**Timer Size (TS) (TS):** 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	1h RO	**Periodic Interrupt Capable (PIC) (PIC):** When set, hardware supports a periodic mode for this timer s interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0h RW/V	**Timer Type (TYP) (TYP):** If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0h RW/V	**Interrupt Enable (IE) (IE):** When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0h RW/V	**Timer Interrupt Type (IT) (IT):** When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active. For ISH, this bit needs to be 0 always to generate edge-sensitive interrupts from all 3 HEPT Timers.
0	0h RO	**Reserved**

14.10.1.10 Timer N Config And Capabilities (T0C_HIGH) — Offset 40A00104h

HPET_T0C : Interrupt Rout Capability (IRC): Indicates IOxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11.

Type	Size	Offset	Default
MMIO	32 bit	40A00104h	00F00000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00F00000h RO	**Interrupt Rout Capability (IRC) (IRC):** Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23. Timer 2: 00f00800h. Indicates support for IRQ11, IRQ20, 21, 22, 23 .

14.10.1.11 Timer N Comparator Value (T0CV_LOW) — Offset 40A00108h

HPET_T0CV Reads to this register return the current value of the comparator. The default value for each timer is all 1s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide.

Type	Size	Offset	Default
MMIO	32 bit	40A00108h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**T0CV_LOW:** Reads to this register return the current value of the comparator. The default value for each timer is all 1 s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide. Due to Hardware latencies, it is recommended to use a comparator value greater than 25 for Timer 0 in periodic mode in ISH.

14.10.1.12 Timer N Comparator Value (T0CV_HIGH) — Offset 40A0010Ch

HPET_T0CV Reads to this register return the current value of the comparator. The default value for each timer is all 1s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide.

Type	Size	Offset	Default
MMIO	32 bit	40A0010Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**T0CV_HIGH:** Reads to this register return the current value of the comparator. The default value for each timer is all 1 s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide. Due to Hardware latencies, it is recommended to use a comparator value greater than 25 for Timer 0 in periodic mode in ISH.

14.10.1.13 Timer N Config And Capabilities (T1C_LOW) — Offset 40A00120h

HPET_T1C : reserved.

Note: Bit definitions are the same as T0C_LOW, offset 40A00100h.

14.10.1.14 Timer N Config And Capabilities (T1C_HIGH) — Offset 40A00124h

HPET_T1C : Interrupt Rout Capability (IRC): Indicates IOxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11.

Note: Bit definitions are the same as T0C_HIGH, offset 40A00104h.

14.10.1.15 Timer N Comparator Value (T1CV_LOW) — Offset 40A00128h

HPET_T1CV Reads to this register return the current value of the comparator. The default value for each timer is all 1s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide.

Type	Size	Offset	Default
MMIO	32 bit	40A00128h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**T1CV:** Reads to this register return the current value of the comparator. The default value for each timer is all 1 s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide. Due to Hardware latencies, it is recommended to use a comparator value greater than 25 for Timer 0 in periodic mode in ISH.

14.10.1.16 Timer N Config And Capabilities (T2C_LOW) — Offset 40A00140h

HPET_T2C : reserved.

Note: Bit definitions are the same as T0C_LOW, offset 40A00100h.

14.10.1.17 Timer N Config And Capabilities (T2C_HIGH) — Offset 40A00144h

HPET_T1C : Interrupt Rout Capability (IRC): Indicates IOxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11.

Note: Bit definitions are the same as T0C_HIGH, offset 40A00104h.

14.10.1.18 Timer N Comparator Value (T2CV_LOW) — Offset 40A00148h

HPET_T2CV Reads to this register return the current value of the comparator. The default value for each timer is all 1s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide.

Type	Size	Offset	Default
MMIO	32 bit	40A00148h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**T2CV:** Reads to this register return the current value of the comparator. The default value for each timer is all 1 s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide. Due to Hardware latencies, it is recommended to use a comparator value greater than 25 for Timer 0 in periodic mode in ISH.

14.10.1.19 HPET Control And Status (HPET_CTRL_STS) — Offset 40A00160h

Enable HPET Latency Fix : 1 b1 :HPET Latency fix is enabled (Enabled by default where the shadow registers in fast clock domain allow faster read/write access to this register) 1 b0: HPET Latency fix is disabled (Disables the latency fix and switches to legacy mode where each register read/write takes more than 130 us).

Type	Size	Offset	Default
MMIO	32 bit	40A00160h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/V	**Enbale HPET Latency Fix : (HPET_CTRL_STS31):** 1 b1 :HPET Latency fix is enabled (Enabled by default where the shadow registers in fast clock domain allow faster read/write access to this register) 1 b0: HPET Latency fix is disabled (Disables the latency fix and switches to legacy mode where each register read/write takes more than 130 us) .
30	0h RW	**Write In Progress Status Bit Disable (HPET_CTRL_STS30):** 1 b1 :Disable the write in progress status indication to PMU. Ie. The write in progress status bit to PMU will be set to 0. 1 b0: Write in progress status indication is enabled. The status bit will be sent to PMU and PMU will monitor this bit before entering TCG. .
29:14	0000h RO	**HPET_CTRL_STS16_29:** Reserved
13	0h RO	**HPET_CTRL_STS13:** 1 b1 : HPET Main Counter value is Invalid 1 b0 : HPET Main Counter value is Valid This bit is set and cleared during TCG exit condition by the h/w.
12	0h RO	**HPET_CTRL_STS12:** 1 b1 : HPET Timer0 Accumulator is Invalid 1 b0 : HPET Timer0 Accumulator is Valid This bit is set and cleared during TCG exit condition by the h/w.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**HPET_CTRL_STS11:** 1 b1 : HPET Control and Status LO : Shadow to Primary Register Write is in progress 1 b0 : HPET Control and Status LO : Shadow to Primary Register Write is done .
10	0h RO	**HPET_CTRL_STS10:** 1 b1 : Timer 2 Comparator Value LO : Shadow to Primary Register Write is in progress 1 b0 : Timer 2 Comparator Value LO : Shadow to Primary Register Write is done .
9	0h RO	**HPET_CTRL_STS9:** 1 b1 : Timer 1 Comparator Value LO : Shadow to Primary Register Write is in progress 1 b0 : Timer 1 Comparator Value LO : Shadow to Primary Register Write is done .
8	0h RO	**HPET_CTRL_STS8:** 1 b1 : Timer 0 Comparator Value HI : Shadow to Primary Register Write is in progress 1 b0 : Timer 0 Comparator Value HI : Shadow to Primary Register Write is done .
7	0h RO	**HPET_CTRL_STS7:** 1 b1 : Timer 0 Comparator Value LO : Shadow to Primary Register Write is in progress 1 b0 : Timer 0 Comparator Value LO : Shadow to Primary Register Write is done .
6	0h RO	**HPET_CTRL_STS6:** 1 b1 : Timer 2 Config & Capabilities LO : Shadow to Primary Register Write is in progress 1 b0 : Timer 2 Config & Capabilities LO : Shadow to Primary Register Write is done .
5	0h RO	**HPET_CTRL_STS5:** 1 b1 : Timer 1 Config & Capabilities LO : Shadow to Primary Register Write is in progress 1 b0 : Timer 1 Config & Capabilities LO : Shadow to Primary Register Write is done .
4	0h RO	**HPET_CTRL_STS4:** 1 b1 : Timer 0 Config & Capabilities LO : Shadow to Primary Register Write is in progress 1 b0 : Timer 0 Config & Capabilities LO : Shadow to Primary Register Write is done .
3	0h RO	**HPET_CTRL_STS3:** 1 b1 : Main Counter Value HI : Shadow to Primary Register Write is in progress 1 b0 : Main Counter Value HI : Shadow to Primary Register Write is done .
2	0h RO	**HPET_CTRL_STS2:** 1 b1 : Main Counter Value LO : Shadow to Primary Register Write is in progress 1 b0 : Main Counter Value LO : Shadow to Primary Register Write is done .
1	0h RO	**HPET_CTRL_STS1:** 1 b1 : General Interrupt Status LO : Shadow to Primary Register Write is in progress 1 b0 : General Interrupt Status LO : Shadow to Primary Register Write is done .
0	0h RO	**HPET_CTRL_STS0:** 1 b1 : General Config Regiser LO : Shadow to Primary Register Write is in progress 1 b0 : General Config Regiser LO : Shadow to Primary Register Write is done .

14.11 WDT Registers

WDT Registers	Address Offset	Table
WDT	40B00000h - 40B00008h	Table 14-21

14.11.1 WDT Registers Summary

Table 14-21. Summary of WDT Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40B00000h	4	WDT Control (WDTC)	0000A0A0h
40B00004h	4	WDT Reload (WDTR)	00000000h
40B00008h	4	WDT Values (WDTV)	0000A0A0h

14.11.1.1 WDT Control (WDTC) — Offset 40B00000h

WDT control register. Used for Enabling the WDT and Loading timeout values.

Type	Size	Offset	Default
MMIO	32 bit	40B00000h	0000A0A0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**WDT_EN:** Enables the watchdog timer.
16	0h RO	**Reserved**
15:8	A0h RW	**Load Value For T2 Counter (WDT_T2):** The value loaded at the beginning of the T2 state.
7:0	A0h RW	**Load Value For T1 Counter (WDT_T1):** The value loaded at the beginning of the T1 state.

14.11.1.2 WDT Reload (WDTR) — Offset 40B00004h

WDT Reload register. When reload is set to 1, the hardware reloads the counters to the values in WDT_T1 and WDT_T2 fields.

Type	Size	Offset	Default
MMIO	32 bit	40B00004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**WDT_RL:** Reload. When firmware writes a 1 to this bit, the hardware reloads the counters to the values in WDT_T1 and WDT_T2 fields. The hardware will auto-clear this bit, so it will always read as a 0.

14.11.1.3 WDT Values (WDTV) — Offset 40B00008h

WDT Values register. Current values of T1 and T2 counter can be read from this register.

Type	Size	Offset	Default
MMIO	32 bit	40B00008h	0000A0A0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	A0h RO	**Current Value Of T2 Counter (WDT_T2_VAL):** Current values of the T2 counter (The actual timer, counting down).
7:0	A0h RO	**Current Value Of T1 Counter (WDT_T1_VAL):** Current values of the T1 counter (The actual timer, counting down).

14.12 ATT Registers

ATT Registers	Address Offset	Table
ATT	40E00000h - 40E0001FCh	Table 14-22

14.12.1 ATT Registers Summary

Table 14-22. Summary of ATT Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40E00000h	4	MMIO BASE VALUE For Entry 0 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0)	80000001h
40E00004h	4	MMIO BASE VALUE For Entry 0 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0)	80001000h
40E00008h	4	OCP Translate Offset For Entry 0 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0)	40400000h
40E0000Ch	4	OCP Translate Mask For Entry 0 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0)	FFFF0000h
40E00010h	4	MMIO BASE VALUE For Entry 1 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_1)	80004001h
40E00014h	4	MMIO BASE VALUE For Entry 1 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_1)	80006000h
40E00018h	4	OCP Translate Offset For Entry 1 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_1)	40F00000h
40E0001Ch	4	OCP Translate Mask For Entry 1 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_1)	FFFFE000h
40E00020h	4	MMIO BASE VALUE For Entry 2 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_2)	80006001h
40E00024h	4	MMIO BASE VALUE For Entry 2 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_2)	80007000h
40E00028h	4	OCP Translate Offset For Entry 2 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_2)	40C00000h
40E0002Ch	4	OCP Translate Mask For Entry 2 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_2)	FFFFE000h
40E00030h	4	MMIO BASE VALUE For Entry 3 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_3)	80010001h
40E00034h	4	MMIO BASE VALUE For Entry 3 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_3)	80014000h
40E00038h	4	OCP Translate Offset For Entry 3 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_3)	40410000h
40E0003Ch	4	OCP Translate Mask For Entry 3 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_3)	FFFF0000h
40E00040h	4	MMIO BASE VALUE For Entry 4 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_4)	80100000h
40E00044h	4	MMIO BASE VALUE For Entry 4 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_4)	80104000h
40E00048h	4	OCP Translate Offset For Entry 4 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_4)	60000000h
40E0004Ch	4	OCP Translate Mask For Entry 4 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_4)	FFFF0000h
40E00050h	4	MMIO BASE VALUE For Entry 5 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_5)	80200001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40E00054h	4	MMIO BASE VALUE For Entry 5 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_5)	80220000h
40E00058h	4	OCP Translate Offset For Entry 5 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_5)	50200000h
40E0005Ch	4	OCP Translate Mask For Entry 5 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_5)	FFFE0000h
40E00060h	4	MMIO BASE VALUE For Entry 6 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_6)	80220000h
40E00064h	4	MMIO BASE VALUE For Entry 6 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_6)	80240000h
40E00068h	4	OCP Translate Offset For Entry 6 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_6)	60000000h
40E0006Ch	4	OCP Translate Mask For Entry 6 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_6)	FFFE0000h
40E00070h	4	MMIO BASE VALUE For Entry 7 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_7)	80400001h
40E00074h	4	MMIO BASE VALUE For Entry 7 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_7)	80420000h
40E00078h	4	OCP Translate Offset For Entry 7 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_7)	50220000h
40E0007Ch	4	OCP Translate Mask For Entry 7 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_7)	FFFE0000h
40E00080h	4	MMIO BASE VALUE For Entry 8 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_8)	80420000h
40E00084h	4	MMIO BASE VALUE For Entry 8 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_8)	80440000h
40E00088h	4	OCP Translate Offset For Entry 8 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_8)	60000000h
40E0008Ch	4	OCP Translate Mask For Entry 8 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_8)	FFFE0000h
40E00090h	4	MMIO BASE VALUE For Entry 9 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_9)	00000000h
40E00094h	4	MMIO BASE VALUE For Entry 9 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_9)	00000000h
40E00098h	4	OCP Translate Offset For Entry 9 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_9)	00000000h
40E0009Ch	4	OCP Translate Mask For Entry 9 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_9)	00000000h
40E000A0h	4	MMIO BASE VALUE For Entry 10 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_10)	00000000h
40E000A4h	4	MMIO BASE VALUE For Entry 10 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_10)	00000000h
40E000A8h	4	OCP Translate Offset For Entry 10 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_10)	00000000h
40E000ACh	4	OCP Translate Mask For Entry 10 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_10)	00000000h
40E000B0h	4	MMIO BASE VALUE For Entry 11 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_11)	00000000h
40E000B4h	4	MMIO BASE VALUE For Entry 11 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_11)	00000000h
40E000B8h	4	OCP Translate Offset For Entry 11 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_11)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40E000BCh	4	OCP Translate Mask For Entry 11 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_11)	00000000h
40E000C0h	4	MMIO BASE VALUE For Entry 12 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_12)	00000000h
40E000C4h	4	MMIO BASE VALUE For Entry 12 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_12)	00000000h
40E000C8h	4	OCP Translate Offset For Entry 12 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_12)	00000000h
40E000CCh	4	OCP Translate Mask For Entry 12 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_12)	00000000h
40E000D0h	4	MMIO BASE VALUE For Entry 13 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_13)	00000000h
40E000D4h	4	MMIO BASE VALUE For Entry 13 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_13)	00000000h
40E000D8h	4	OCP Translate Offset For Entry 13 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_13)	00000000h
40E000DCh	4	OCP Translate Mask For Entry 13 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_13)	00000000h
40E000E0h	4	MMIO BASE VALUE For Entry 14 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_14)	00000000h
40E000E4h	4	MMIO BASE VALUE For Entry 14 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_14)	00000000h
40E000E8h	4	OCP Translate Offset For Entry 14 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_14)	00000000h
40E000ECh	4	OCP Translate Mask For Entry 14 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_14)	00000000h
40E000F0h	4	MMIO BASE VALUE For Entry 15 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_15)	00000000h
40E000F4h	4	MMIO BASE VALUE For Entry 15 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_15)	00000000h
40E000F8h	4	OCP Translate Offset For Entry 15 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_15)	00000000h
40E000FCh	4	OCP Translate Mask For Entry 15 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_15)	00000000h
40E00100h	4	MMIO BASE VALUE For Entry 16 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_16)	00000000h
40E00104h	4	MMIO BASE VALUE For Entry 16 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_16)	00000000h
40E00108h	4	OCP Translate Offset For Entry 16 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_16)	00000000h
40E0010Ch	4	OCP Translate Mask For Entry 16 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_16)	00000000h
40E00110h	4	MMIO BASE VALUE For Entry 17 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_17)	00000000h
40E00114h	4	MMIO BASE VALUE For Entry 17 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_17)	00000000h
40E00118h	4	OCP Translate Offset For Entry 17 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_17)	00000000h
40E0011Ch	4	OCP Translate Mask For Entry 17 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_17)	00000000h
40E00120h	4	MMIO BASE VALUE For Entry 18 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_18)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40E00124h	4	MMIO BASE VALUE For Entry 18 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_18)	00000000h
40E00128h	4	OCP Translate Offset For Entry 18 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_18)	00000000h
40E0012Ch	4	OCP Translate Mask For Entry 18 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_18)	00000000h
40E00130h	4	MMIO BASE VALUE For Entry 19 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_19)	00000000h
40E00134h	4	MMIO BASE VALUE For Entry 19 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_19)	00000000h
40E00138h	4	OCP Translate Offset For Entry 19 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_19)	00000000h
40E0013Ch	4	OCP Translate Mask For Entry 19 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_19)	00000000h
40E00140h	4	MMIO BASE VALUE For Entry 20 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_20)	00000000h
40E00144h	4	MMIO BASE VALUE For Entry 20 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_20)	00000000h
40E00148h	4	OCP Translate Offset For Entry 20 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_20)	00000000h
40E0014Ch	4	OCP Translate Mask For Entry 20 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_20)	00000000h
40E00150h	4	MMIO BASE VALUE For Entry 21 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_21)	00000000h
40E00154h	4	MMIO BASE VALUE For Entry 21 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_21)	00000000h
40E00158h	4	OCP Translate Offset For Entry 21 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_21)	00000000h
40E0015Ch	4	OCP Translate Mask For Entry 21 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_21)	00000000h
40E00160h	4	MMIO BASE VALUE For Entry 22 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_22)	00000000h
40E00164h	4	MMIO BASE VALUE For Entry 22 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_22)	00000000h
40E00168h	4	OCP Translate Offset For Entry 22 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_22)	00000000h
40E0016Ch	4	OCP Translate Mask For Entry 22 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_22)	00000000h
40E00170h	4	MMIO BASE VALUE For Entry 23 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_23)	00000000h
40E00174h	4	MMIO BASE VALUE For Entry 23 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_23)	00000000h
40E00178h	4	OCP Translate Offset For Entry 23 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_23)	00000000h
40E0017Ch	4	OCP Translate Mask For Entry 23 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_23)	00000000h
40E00180h	4	MMIO BASE VALUE For Entry 24 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_24)	00000000h
40E00184h	4	MMIO BASE VALUE For Entry 24 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_24)	00000000h
40E00188h	4	OCP Translate Offset For Entry 24 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_24)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40E0018Ch	4	OCP Translate Mask For Entry 24 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_24)	00000000h
40E00190h	4	MMIO BASE VALUE For Entry 25 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_25)	00000000h
40E00194h	4	MMIO BASE VALUE For Entry 25 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_25)	00000000h
40E00198h	4	OCP Translate Offset For Entry 25 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_25)	00000000h
40E0019Ch	4	OCP Translate Mask For Entry 25 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_25)	00000000h
40E001A0h	4	MMIO BASE VALUE For Entry 26 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_26)	00000000h
40E001A4h	4	MMIO BASE VALUE For Entry 26 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_26)	00000000h
40E001A8h	4	OCP Translate Offset For Entry 26 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_26)	00000000h
40E001ACh	4	OCP Translate Mask For Entry 26 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_26)	00000000h
40E001B0h	4	MMIO BASE VALUE For Entry 27 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_27)	00000000h
40E001B4h	4	MMIO BASE VALUE For Entry 27 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_27)	00000000h
40E001B8h	4	OCP Translate Offset For Entry 27 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_27)	00000000h
40E001BCh	4	OCP Translate Mask For Entry 27 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_27)	00000000h
40E001C0h	4	MMIO BASE VALUE For Entry 28 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_28)	00000000h
40E001C4h	4	MMIO BASE VALUE For Entry 28 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_28)	00000000h
40E001C8h	4	OCP Translate Offset For Entry 28 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_28)	00000000h
40E001CCh	4	OCP Translate Mask For Entry 28 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_28)	00000000h
40E001D0h	4	MMIO BASE VALUE For Entry 29 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_29)	00000000h
40E001D4h	4	MMIO BASE VALUE For Entry 29 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_29)	00000000h
40E001D8h	4	OCP Translate Offset For Entry 29 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_29)	00000000h
40E001DCh	4	OCP Translate Mask For Entry 29 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_29)	00000000h
40E001E0h	4	MMIO BASE VALUE For Entry 30 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_30)	00000000h
40E001E4h	4	MMIO BASE VALUE For Entry 30 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_30)	00000000h
40E001E8h	4	OCP Translate Offset For Entry 30 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_30)	00000000h
40E001ECh	4	OCP Translate Mask For Entry 30 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_30)	00000000h
40E001F0h	4	MMIO BASE VALUE For Entry 31 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_31)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40E001F4h	4	MMIO BASE VALUE For Entry 31 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_31)	00000000h
40E001F8h	4	OCP Translate Offset For Entry 31 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_31)	00000000h
40E001FCh	4	OCP Translate Mask For Entry 31 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_31)	00000000h

14.12.1.1 MMIO BASE VALUE For Entry 0 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0) — Offset 40E00000h

MMIO BASE VALUE for entry 0.

Type	Size	Offset	Default
MMIO	32 bit	40E00000h	80000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	80000h RW	**MMIO_BASE_VALUE:** This defines the MMIO Base (4K aligned address offset) value.
11:1	0h RO	**Reserved**
0	1h RW	**VALID:** Valid: This defines that this entry is valid.

14.12.1.2 MMIO BASE VALUE For Entry 0 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0) — Offset 40E00004h

MMIO BASE VALUE for entry 0.

Type	Size	Offset	Default
MMIO	32 bit	40E00004h	80001000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	80001h RW	**MMIO_LIMIT_VALUE:** MMIO Limit VALUE for entry K: This defines the MMIO Limit (4K aligned address offset) value.
11:0	0h RO	**Reserved**

14.12.1.3 OCP Translate Offset For Entry 0 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0) — Offset 40E00008h

OCP Translate Offset for entry 0.

Type	Size	Offset	Default
MMIO	32 bit	40E00008h	40400000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	40400h RW	**OCP_XLATE_OFFSET:** OCP Translate Offset for entry K: This defines the OCP translate offset to be substituted instead of the incoming MMIO address to derive the upper OCP target address. The number of bits for offset and pass-through is defined in mask field.
11:0	0h RO	**Reserved**

14.12.1.4 OCP Translate Mask For Entry 0 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0) — Offset 40E0000Ch

OCP Translate Mask for entry 0.

Type	Size	Offset	Default
MMIO	32 bit	40E0000Ch	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	FFFF0h RW	**OCP_XLATE_MASK:** OCP Translate Mask for entry K: This defines the OCP translate mask bits for the incoming MMIO address to pass through onto OCP fabric. 0 : MMIO Address Pass through to OCP Fabric 1 : MMIO Address substituted by Translate Offset field.
11:0	0h RO	**Reserved**

14.12.1.5 MMIO BASE VALUE For Entry 1 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_1) — Offset 40E00010h

MMIO BASE VALUE for entry 1.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.6 MMIO BASE VALUE For Entry 1 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_1) — Offset 40E00014h

MMIO BASE VALUE for entry 1.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.7 OCP Translate Offset For Entry 1 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_1) — Offset 40E00018h

OCP Translate Offset for entry 1.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.8 OCP Translate Mask For Entry 1 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_1) — Offset 40E0001Ch

OCP Translate Mask for entry 1.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.9 MMIO BASE VALUE For Entry 2 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_2) — Offset 40E00020h

MMIO BASE VALUE for entry 2.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.10 MMIO BASE VALUE For Entry 2 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_2) — Offset 40E00024h

MMIO BASE VALUE for entry 2.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.11 OCP Translate Offset For Entry 2 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_2) — Offset 40E00028h

OCP Translate Offset for entry 2.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.12 OCP Translate Mask For Entry 2 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_2) — Offset 40E0002Ch

OCP Translate Mask for entry 2.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.13 MMIO BASE VALUE For Entry 3 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_3) — Offset 40E00030h

MMIO BASE VALUE for entry 3.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.14 MMIO BASE VALUE For Entry 3 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_3) — Offset 40E00034h

MMIO BASE VALUE for entry 3.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.15 OCP Translate Offset For Entry 3 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_3) — Offset 40E00038h

OCP Translate Offset for entry 3.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.16 OCP Translate Mask For Entry 3 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_3) — Offset 40E0003Ch

OCP Translate Mask for entry 3.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.17 MMIO BASE VALUE For Entry 4 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_4) — Offset 40E00040h

MMIO BASE VALUE for entry 4.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.18 MMIO BASE VALUE For Entry 4 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_4) — Offset 40E00044h

MMIO BASE VALUE for entry 4.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.19 OCP Translate Offset For Entry 4 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_4) — Offset 40E00048h

OCP Translate Offset for entry 4.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.20 OCP Translate Mask For Entry 4 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_4) — Offset 40E0004Ch

OCP Translate Mask for entry 4.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.21 MMIO BASE VALUE For Entry 5 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_5) — Offset 40E00050h

MMIO BASE VALUE for entry 5.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.22 MMIO BASE VALUE For Entry 5 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_5) — Offset 40E00054h

MMIO BASE VALUE for entry 5.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.23 OCP Translate Offset For Entry 5 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_5) — Offset 40E00058h

OCP Translate Offset for entry 5.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.24 OCP Translate Mask For Entry 5 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_5) — Offset 40E0005Ch

OCP Translate Mask for entry 5.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.25 MMIO BASE VALUE For Entry 6 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_6) — Offset 40E00060h

MMIO BASE VALUE for entry 6.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.26 MMIO BASE VALUE For Entry 6 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_6) — Offset 40E00064h

MMIO BASE VALUE for entry 6.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.27 OCP Translate Offset For Entry 6 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_6) — Offset 40E00068h

OCP Translate Offset for entry 6.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.28 OCP Translate Mask For Entry 6 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_6) — Offset 40E0006Ch

OCP Translate Mask for entry 6.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.29 MMIO BASE VALUE For Entry 7 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_7) — Offset 40E00070h

MMIO BASE VALUE for entry 7.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.30 MMIO BASE VALUE For Entry 7 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_7) — Offset 40E00074h

MMIO BASE VALUE for entry 7.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.31 OCP Translate Offset For Entry 7 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_7) — Offset 40E00078h

OCP Translate Offset for entry 7.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.32 OCP Translate Mask For Entry 7 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_7) — Offset 40E0007Ch

OCP Translate Mask for entry 7.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.33 MMIO BASE VALUE For Entry 8 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_8) — Offset 40E00080h

MMIO BASE VALUE for entry 8.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.34 MMIO BASE VALUE For Entry 8 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_8) — Offset 40E00084h

MMIO BASE VALUE for entry 8.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.35 OCP Translate Offset For Entry 8 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_8) — Offset 40E00088h

OCP Translate Offset for entry 8.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.36 OCP Translate Mask For Entry 8 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_8) — Offset 40E0008Ch

OCP Translate Mask for entry 8.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.37 MMIO BASE VALUE For Entry 9 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_9) — Offset 40E00090h

MMIO BASE VALUE for entry 9.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.38 MMIO BASE VALUE For Entry 9 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_9) — Offset 40E00094h

MMIO BASE VALUE for entry 9.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.39 OCP Translate Offset For Entry 9 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_9) — Offset 40E00098h

OCP Translate Offset for entry 9.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.40 OCP Translate Mask For Entry 9 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_9) — Offset 40E0009Ch

OCP Translate Mask for entry 9.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.41 MMIO BASE VALUE For Entry 10 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_10) — Offset 40E000A0h

MMIO BASE VALUE for entry 10.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.42 MMIO BASE VALUE For Entry 10 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_10) — Offset 40E000A4h

MMIO BASE VALUE for entry 10.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.43 OCP Translate Offset For Entry 10 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_10) — Offset 40E000A8h

OCP Translate Offset for entry 10.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.44 OCP Translate Mask For Entry 10 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_10) — Offset 40E000ACh

OCP Translate Mask for entry 10.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.45 MMIO BASE VALUE For Entry 11 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_11) — Offset 40E000B0h

MMIO BASE VALUE for entry 11.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.46 MMIO BASE VALUE For Entry 11 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_11) — Offset 40E000B4h

MMIO BASE VALUE for entry 11.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.47 OCP Translate Offset For Entry 11 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_11) — Offset 40E000B8h

OCP Translate Offset for entry 11.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.48 OCP Translate Mask For Entry 11 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_11) — Offset 40E000BCh

OCP Translate Mask for entry 11.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.49 MMIO BASE VALUE For Entry 12 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_12) — Offset 40E000C0h

MMIO BASE VALUE for entry 12.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.50 MMIO BASE VALUE For Entry 12 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_12) — Offset 40E000C4h

MMIO BASE VALUE for entry 12.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.51 OCP Translate Offset For Entry 12 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_12) — Offset 40E000C8h

OCP Translate Offset for entry 12.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.52 OCP Translate Mask For Entry 12 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_12) — Offset 40E000CCh

OCP Translate Mask for entry 12.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.53 MMIO BASE VALUE For Entry 13 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_13) — Offset 40E000D0h

MMIO BASE VALUE for entry 13.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.54 MMIO BASE VALUE For Entry 13 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_13) — Offset 40E000D4h

MMIO BASE VALUE for entry 13.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.55 OCP Translate Offset For Entry 13 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_13) — Offset 40E000D8h

OCP Translate Offset for entry 13.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.56 OCP Translate Mask For Entry 13 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_13) — Offset 40E000DCh

OCP Translate Mask for entry 13.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.57 MMIO BASE VALUE For Entry 14 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_14) — Offset 40E000E0h

MMIO BASE VALUE for entry 14.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.58 MMIO BASE VALUE For Entry 14 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_14) — Offset 40E000E4h

MMIO BASE VALUE for entry 14.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.59 OCP Translate Offset For Entry 14 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_14) — Offset 40E000E8h

OCP Translate Offset for entry 14.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.60 OCP Translate Mask For Entry 14 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_14) — Offset 40E000ECh

OCP Translate Mask for entry 14.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.61 MMIO BASE VALUE For Entry 15 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_15) — Offset 40E000F0h

MMIO BASE VALUE for entry 15.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.62 MMIO BASE VALUE For Entry 15 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_15) — Offset 40E000F4h

MMIO BASE VALUE for entry 15.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.63 OCP Translate Offset For Entry 15 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_15) — Offset 40E000F8h

OCP Translate Offset for entry 15.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.64 OCP Translate Mask For Entry 15 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_15) — Offset 40E000FCh

OCP Translate Mask for entry 15.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.65 MMIO BASE VALUE For Entry 16 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_16) — Offset 40E00100h

MMIO BASE VALUE for entry 16.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.66 MMIO BASE VALUE For Entry 16 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_16) — Offset 40E00104h

MMIO BASE VALUE for entry 16.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.67 OCP Translate Offset For Entry 16 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_16) — Offset 40E00108h

OCP Translate Offset for entry 16.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.68 OCP Translate Mask For Entry 16 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_16) — Offset 40E0010Ch

OCP Translate Mask for entry 16.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.69 MMIO BASE VALUE For Entry 17 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_17) — Offset 40E00110h

MMIO BASE VALUE for entry 17.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.70 MMIO BASE VALUE For Entry 17 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_17) — Offset 40E00114h

MMIO BASE VALUE for entry 17.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.71 OCP Translate Offset For Entry 17 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_17) — Offset 40E00118h

OCP Translate Offset for entry 17.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.72 OCP Translate Mask For Entry 17 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_17) — Offset 40E0011Ch

OCP Translate Mask for entry 17.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.73 MMIO BASE VALUE For Entry 18 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_18) — Offset 40E00120h

MMIO BASE VALUE for entry 18.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.74 MMIO BASE VALUE For Entry 18 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_18) — Offset 40E00124h

MMIO BASE VALUE for entry 18.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.75 OCP Translate Offset For Entry 18 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_18) — Offset 40E00128h

OCP Translate Offset for entry 18.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.76 OCP Translate Mask For Entry 18 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_18) — Offset 40E0012Ch

OCP Translate Mask for entry 18.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.77 MMIO BASE VALUE For Entry 19 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_19) — Offset 40E00130h

MMIO BASE VALUE for entry 19.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.78 MMIO BASE VALUE For Entry 19 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_19) — Offset 40E00134h

MMIO BASE VALUE for entry 19.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.79 OCP Translate Offset For Entry 19 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_19) — Offset 40E00138h

OCP Translate Offset for entry 19.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.80 OCP Translate Mask For Entry 19 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_19) — Offset 40E0013Ch

OCP Translate Mask for entry 19.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.81 MMIO BASE VALUE For Entry 20 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_20) — Offset 40E00140h

MMIO BASE VALUE for entry 20.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.82 MMIO BASE VALUE For Entry 20 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_20) — Offset 40E00144h

MMIO BASE VALUE for entry 20.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.83 OCP Translate Offset For Entry 20 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_20) — Offset 40E00148h

OCP Translate Offset for entry 20.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.84 OCP Translate Mask For Entry 20 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_20) — Offset 40E0014Ch

OCP Translate Mask for entry 20.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.85 MMIO BASE VALUE For Entry 21 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_21) — Offset 40E00150h

MMIO BASE VALUE for entry 21.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.86 MMIO BASE VALUE For Entry 21 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_21) — Offset 40E00154h

MMIO BASE VALUE for entry 21.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.87 OCP Translate Offset For Entry 21 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_21) — Offset 40E00158h

OCP Translate Offset for entry 21.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.88 OCP Translate Mask For Entry 21 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_21) — Offset 40E0015Ch

OCP Translate Mask for entry 21.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.89 MMIO BASE VALUE For Entry 22 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_22) — Offset 40E00160h

MMIO BASE VALUE for entry 22.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.90 MMIO BASE VALUE For Entry 22 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_22) — Offset 40E00164h

MMIO BASE VALUE for entry 22.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.91 OCP Translate Offset For Entry 22 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_22) — Offset 40E00168h

OCP Translate Offset for entry 22.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.92 OCP Translate Mask For Entry 22 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_22) — Offset 40E0016Ch

OCP Translate Mask for entry 22.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.93 MMIO BASE VALUE For Entry 23 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_23) — Offset 40E00170h

MMIO BASE VALUE for entry 23.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.94 MMIO BASE VALUE For Entry 23 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_23) — Offset 40E00174h

MMIO BASE VALUE for entry 23.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.95 OCP Translate Offset For Entry 23 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_23) — Offset 40E00178h

OCP Translate Offset for entry 23.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.96 OCP Translate Mask For Entry 23 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_23) — Offset 40E0017Ch

OCP Translate Mask for entry 23.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.97 MMIO BASE VALUE For Entry 24 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_24) — Offset 40E00180h

MMIO BASE VALUE for entry 24.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.98 MMIO BASE VALUE For Entry 24 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_24) — Offset 40E00184h

MMIO BASE VALUE for entry 24.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.99 OCP Translate Offset For Entry 24 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_24) — Offset 40E00188h

OCP Translate Offset for entry 24.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.100 OCP Translate Mask For Entry 24 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_24) — Offset 40E0018Ch

OCP Translate Mask for entry 24.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.101 MMIO BASE VALUE For Entry 25 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_25) — Offset 40E00190h

MMIO BASE VALUE for entry 25.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.102 MMIO BASE VALUE For Entry 25 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_25) — Offset 40E00194h

MMIO BASE VALUE for entry 25.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.103 OCP Translate Offset For Entry 25 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_25) — Offset 40E00198h

OCP Translate Offset for entry 25.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.104 OCP Translate Mask For Entry 25 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_25) — Offset 40E0019Ch

OCP Translate Mask for entry 25.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.105 MMIO BASE VALUE For Entry 26 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_26) — Offset 40E001A0h

MMIO BASE VALUE for entry 26.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.106 MMIO BASE VALUE For Entry 26 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_26) — Offset 40E001A4h

MMIO BASE VALUE for entry 26.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.107 OCP Translate Offset For Entry 26 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_26) — Offset 40E001A8h

OCP Translate Offset for entry 26.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.108 OCP Translate Mask For Entry 26 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_26) — Offset 40E001ACh

OCP Translate Mask for entry 26.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.109 MMIO BASE VALUE For Entry 27 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_27) — Offset 40E001B0h

MMIO BASE VALUE for entry 27.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.110 MMIO BASE VALUE For Entry 27 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_27) — Offset 40E001B4h

MMIO BASE VALUE for entry 27.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.111 OCP Translate Offset For Entry 27 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_27) — Offset 40E001B8h

OCP Translate Offset for entry 27.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.112 OCP Translate Mask For Entry 27 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_27) — Offset 40E001BCh

OCP Translate Mask for entry 27.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.113 MMIO BASE VALUE For Entry 28 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_28) — Offset 40E001C0h

MMIO BASE VALUE for entry 28.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.114 MMIO BASE VALUE For Entry 28 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_28) — Offset 40E001C4h

MMIO BASE VALUE for entry 28.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.115 OCP Translate Offset For Entry 28 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_28) — Offset 40E001C8h

OCP Translate Offset for entry 28.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.116 OCP Translate Mask For Entry 28 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_28) — Offset 40E001CCh

OCP Translate Mask for entry 28.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.117 MMIO BASE VALUE For Entry 29 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_29) — Offset 40E001D0h

MMIO BASE VALUE for entry 29.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.118 MMIO BASE VALUE For Entry 29 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_29) — Offset 40E001D4h

MMIO BASE VALUE for entry 29.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.119OCP Translate Offset For Entry 29 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_29) — Offset 40E001D8h

OCP Translate Offset for entry 29.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.120OCP Translate Mask For Entry 29 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_29) — Offset 40E001DCh

OCP Translate Mask for entry 29.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.121MMIO BASE VALUE For Entry 30 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_30) — Offset 40E001E0h

MMIO BASE VALUE for entry 30.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.122MMIO BASE VALUE For Entry 30 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_30) — Offset 40E001E4h

MMIO BASE VALUE for entry 30.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.123OCP Translate Offset For Entry 30 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_30) — Offset 40E001E8h

OCP Translate Offset for entry 30.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.124OCP Translate Mask For Entry 30 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_30) — Offset 40E001ECh

OCP Translate Mask for entry 30.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.12.1.125 MMIO BASE VALUE For Entry 31 (ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_31) — Offset 40E001F0h

MMIO BASE VALUE for entry 31.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_BASE_REG_ENTRY_0, offset 40E00000h.

14.12.1.126 MMIO BASE VALUE For Entry 31 (ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_31) — Offset 40E001F4h

MMIO BASE VALUE for entry 31.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_MMIO_LIMIT_REG_ENTRY_0, offset 40E00004h.

14.12.1.127 OCP Translate Offset For Entry 31 (ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_31) — Offset 40E001F8h

OCP Translate Offset for entry 31.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_OFFSET_REG_ENTRY_0, offset 40E00008h.

14.12.1.128 OCP Translate Mask For Entry 31 (ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_31) — Offset 40E001FCh

OCP Translate Mask for entry 31.

Note: Bit definitions are the same as ISH_DS_OCP_ATT_OCP_XLATE_MASK_REG_ENTRY_0, offset 40E0000Ch.

14.13 PLL Registers

PLL Registers	Address Offset	Table
PLL	41000000h - 4100007Ch	Table 14-23

14.13.1 PLL Registers Summary

Table 14-23. Summary of PLL Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41000000h	4	Reg LCPLL_DIV0 (LCPLL_DIV0)	4800004Eh
41000004h	4	Reg LCPLL_CFG0 (LCPLL_CFG0)	00000000h
41000008h	4	Reg LCPLL_SSC0 (LCPLL_SSC0)	00000139h
4100000Ch	4	Reg LCPLL_CFG1 (LCPLL_CFG1)	00000000h
41000010h	4	Reg LCPLL_LF0 (LCPLL_LF0)	0A010804h
41000014h	4	Reg LCPLL_CFG2 (LCPLL_CFG2)	00000000h
41000018h	4	Reg LCPLL_DIV1 (LCPLL_DIV1)	00020000h
4100001Ch	4	Reg LCPLL_RCOMP (LCPLL_RCOMP)	002A0003h
41000020h	4	Reg LCPLL_SSC1 (LCPLL_SSC1)	00000000h
41000024h	4	Reg LCPLL_LF1 (LCPLL_LF1)	00000000h
41000028h	4	Reg LCPLL_TDC0 (LCPLL_TDC0)	000F0011h
4100002Ch	4	Reg LCPLL_LF2 (LCPLL_LF2)	0000030Ah
41000030h	4	Reg LCPLL_DFT0 (LCPLL_DFT0)	78003C00h
41000034h	4	Reg LCPLL_DFT1 (LCPLL_DFT1)	00000000h
41000038h	4	Reg LCPLL_DFT2Reg (LCPLL_DFT2)	00000000h
4100003Ch	4	Reg LCPLL_VISA_EN (LCPLL_VISA_EN)	00000000h
41000040h	4	Reg LCPLL_VISA_LANE0 (LCPLL_VISA_LANE0)	00000000h
41000044h	4	Reg LCPLL_VISA_LANE1 (LCPLL_VISA_LANE1)	00000000h
41000048h	4	Reg LCPLL_BONUS (LCPLL_BONUS)	00000000h
4100004Ch	4	Reg LCPLL_EBB0 (LCPLL_EBB0)	0C000900h
41000050h	4	Reg LCPLL_EBB1 (LCPLL_EBB1)	2D001B00h
41000054h	4	Reg Reserved_0 (RESERVED_0)	00000000h
41000058h	4	Reg Reserved_1 (RESERVED_1)	00000000h
4100005Ch	4	Reg LCPLL_CRIOP0 (LCPLL_CRIOP0)	0000004Eh
41000060h	4	Reg LCPLL_CRIOP1 (LCPLL_CRIOP1)	00000000h
41000064h	4	Reg LCPLL_CRIOP2 (LCPLL_CRIOP2)	00000000h
41000068h	4	Reg LCPLL_CRIOP3 (LCPLL_CRIOP3)	01FF0000h
4100006Ch	4	Reg LCPLL_CRIOP4 (LCPLL_CRIOP4)	00000000h
41000070h	4	Reg LCPLL_CRIOP5 (LCPLL_CRIOP5)	00400000h
41000074h	4	Reg LCPLL_CRIOP6 (LCPLL_CRIOP6)	7F303C4Bh
41000078h	4	Reg LCPLL_CRIOP7 (LCPLL_CRIOP7)	00000000h
4100007Ch	4	Reg LCPLL_CRIOP8 (LCPLL_CRIOP8)	2000000Fh

14.13.1.1 Reg LCPLL_DIV0 (LCPLL_DIV0) — Offset 41000000h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000000h	4800004Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	1h RW	**I_FRACNEN_H:** RET Enables fractional modulator. For overclocking case, this bit need to be set to '1', even though it starts with integer division ratio .
29:24	08h RW	**I_FRACDIV_2:** RET Fractional Modulator settings Effected by i_fbdiv_propagate_h.
23:16	00h RW	**I_FRACDIV_1:** RET Fractional Modulator settings Effected by i_fbdiv_propagate_h.
15:8	00h RW	**I_FRACDIV_0:** RET Fractional Modulator settings Effected by i_fbdiv_propagate_h.
7:0	4Eh RW	**I_FBDIVRATIO:** RET Feedback divider post division (M2) Effected by i_fbdiv_propagate_h.

14.13.1.2 Reg LCPLL_CFG0 (LCPLL_CFG0) — Offset 41000004h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/1C	**I_OVC_SNAPSHOT_H:** RETCLR This bit enables for LCPLL to take snapshot of PLL calibration states and integral component.
23:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**I_FBDIV_PROPAGATE_H:** RETCLR Propagate bit for LCPLL to capture feedback divider ratio settings and feedfwrd gain. This bit is automatically cleared after divratio ratio settings captured. (hw clear).
7:1	0h RO	**Reserved**
0	0h RW	**I_PLLRAMPEN_H:** RET This need to be asserted for dynamically updating AFC (coarse DCO code). In normal POR mode, AFC is not updated. For supporting over clocking through PLL and memACT (-1.6125%), this bit need to be asserted so that AFC can be dynamically updated.

14.13.1.3 Reg LCPLL_SSC0 (LCPLL_SSC0) — Offset 41000008h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000008h	00000139h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	0h RW	**I_SSCSTEPSIZE_1:** RET Fractional value for one SSC frequency step. effected by i_ssc_propagate_h.
23:16	00h RW	**I_SSCSTEPSIZE_0:** RET Fractional value for one SSC frequency step. effected by i_ssc_propagate_h.
15:11	0h RO	**Reserved**
10	0h RW	**I_SSCEN_H:** RET Enables SSC modulator. Used for dynamically controlling SSC modulator. SSC profile shuts off after reaching neutral point.
9	0h RW	**I_FEEDFWRDCAL_PAUSE_H:** RET This bit is for dynamically turning on and off feed forward gain calibration, when i_feedfwrdcal_en_h is enabled to take care of dynamic feedfwrdgain calculation during SSC mode.
8	1h RW	**I_FEEDFWRDCAL_EN_H:** RET Background feedfward gain calibration enable signal This is meant for PVT coverage. During PLL ramping this need to be disabled. It is taken care by dynamically changing i_feedfwrdcal_pause_h.
7:0	39h RW	**I_FEEDFWRDGAIN:** RET Feedforwad gain for fractional mode/SSC mode PLL This setting is needed whenever PLL is configured in fractional mode or configured for SSC clock generation. Effected by i_fbdiv_propagate_h.

14.13.1.4 Reg LCPLL_CFG1 (LCPLL_CFG1) — Offset 4100000Ch

RET.

Type	Size	Offset	Default
MMIO	32 bit	4100000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**I_FRACDIV_TOGGLE:** RET Not used.
15:9	0h RO	**Reserved**
8	0h RW	**I_RAMPAFC_SSCEN_H:** RET 0: Disables changing of AFC during SSC 1: Enables AFC changes during SSC to take care PLL ramping and SSC simulataneously This need to be high only for 2-3% SSC spread cases. For BCLK PLL case, default is 1'b0 as 0.5% can be covered with out AFC changes.
7:1	0h RO	**Reserved**
0	0h RW/1C	**I_SSC_PROPAGATE_H:** RETCLR Propagate bit for LCPLL to capture SSC stepsize This bit is automatically cleared after sscstepsize settings captured. (hw clear).

14.13.1.5 Reg LCPLL_LF0 (LCPLL_LF0) — Offset 41000010h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000010h	0A010804h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	1h RW	**I_NDIVRATIO:** RET Refclk input divider control, which sets the divide ratio for the PLL input reference clock 0000 divide by 1 0001 divide by 1 (default) 0010 divide by 2 0011 divide by 3 0100 divide by 4 0101 divide by 5 0110 divide by 6 0111 divide by 7 1000 - 1111 reserved values, do not use.
26:24	2h RW	**I_FBPREDIVRATIO:** RET predivider ratio 000 : /1 (default) 001: reserved 010: /2 011: /2 + (i_fbdivratio + 0.5) 100: /4 101 - 111: reserved.
23:19	0h RO	**Reserved**
18:16	1h RW	**I_GAINCTRL:** RET Adjustable gain for loop filter. Both gains << gainctrl if plllockout=0.
15:13	0h RO	**Reserved**
12:8	08h RW	**I_INT_COEFF:** RET integral coeff. = 2^(-int_coeff), tageting up to 2^-16.
7:4	0h RO	**Reserved**
3:0	4h RW	**I_PROP_COEFF:** RET proportional coeff. = 2^(-prop_coeff+1) .

14.13.1.6 Reg LCPLL_CFG2 (LCPLL_CFG2) — Offset 41000014h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	00h RW	**I_PLLLOCK_CNT_1:** RET target count value for counter based plllock in terms of reference clock.
23:16	00h RW	**I_PLLLOCK_CNT_0:** RET target count value for counter based plllock in terms of reference clock.
15:9	0h RO	**Reserved**
8	0h RW	**I_PLLLOCK_SEL:** RET select between lockdetect-based plllock or counter based plllock, 1 for counter-based one, 0 for lock detection logic.
7:1	0h RO	**Reserved**
0	0h RW	**I_LF_PROPAGATE_H:** RET Not used.

14.13.1.7 Reg LCPLL_DIV1 (LCPLL_DIV1) — Offset 41000018h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000018h	00020000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**I_FRACMODORDER:** RET Not Used.
23:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17	1h RW	**I_DIVRETIMEREN:** RET 0 no retiming of feedback clock (default) 1 feedback clock output is retimed to vco clock .
16	0h RW	**I_FBDIVDUTYCYCSEL:** RET Not Used.
15:0	0h RO	**Reserved**

14.13.1.8 Reg LCPLL_RCOMP (LCPLL_RCOMP) — Offset 4100001Ch

RET.

Type	Size	Offset	Default
MMIO	32 bit	4100001Ch	002A0003h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:16	2Ah RW	**I_RCOMPOV:** RET Repurposed to set frequency scalar for rcomp calculation.
15:9	0h RO	**Reserved**
8	0h RW	**I_RCOMPOV_EN_H:** RET Not Used.
7:2	0h RO	**Reserved**
1	1h RW	**I_BIASFILTER_EN_H:** RET Bypass R in the bias filter.
0	1h RW	**I_BIASCALEN_H:** RET self calibrating bias using digital control enable.

14.13.1.9 Reg LCPLL_SSC1 (LCPLL_SSC1) — Offset 41000020h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	0h RW	**I_SSCSTEPLENGTH_1:** RET Num of refclk cycles of one SSC step.
23:16	00h RW	**I_SSCSTEPLENGTH_0:** RET Num of refclk cycles of one SSC step.
15:10	0h RO	**Reserved**
9:8	0h RW	**I_SSCTYPE:** RET 00 - UP Spread 01 - Center Spread 10 - DN Spread (default) 11 - Reserved.
7:3	0h RO	**Reserved**
2:0	0h RW	**I_SSCSTEPNUM:** RET Num of SSC steps = 2^(sscsetpnum).

14.13.1.10 Reg LCPLL_LF1 (LCPLL_LF1) — Offset 41000024h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW	**I_DUTYCYCCORR_EN_H:** RET Feedback divider duty cycle corrector enable for odd division ratio. When this is asserted, i_divretimeren should be set to '0'.
25	0h RW	**I_BBINLOCK_H:** RET Forces bang-bang mode after the PLL is locked regardless of TDC count when '1', default is '0'.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**I_BBTHRESHSEL:** RET Select bit between coarse threshold and fine threshold 1:coarse 0: fine.
23:21	0h RO	**Reserved**
20:16	00h RW	**I_INT2_COEFF:** RET Not Used.
15:11	0h RO	**Reserved**
10:8	0h RW	**I_BBTHRESH:** RET Digital loop filter goes into BB mode if TDC output is less than bbthresh.
7:3	0h RO	**Reserved**
2:0	0h RW	**I_BB_GAIN:** RET If TDC is less than lockthreshold, diglf input is assumed bb_gain/2^3. .

14.13.1.11 Reg LCPLL_TDC0 (LCPLL_TDC0) — Offset 41000028h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000028h	000F0011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**I_TDCDC_EN_H:** RET TDC gain dynamic change enable.
23:22	0h RO	**Reserved**
21:19	1h RW	**I_PLLWAIT_CNTR:** RET iref vco bias low pass filter settling time. Sets delay before AFC calibration & TDC calibration begins. 0: no delay other values: delay = 25*2^(pllwait_cntr - 1) * refclk cycles.
18	1h RW	**I_TDCCALSETUPDETEN_H:** RET TDC setup time detect enable (used for adjusting TDC output with measured TDC overlap value for -ve setup time).
17:16	3h RW	**I_TDCSEL:** RET selects tdc resolution 00:turn off both tdc 01: turn on only fine 10: turn on only coarse 11: turn on both.

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9:8	0h RW	**I_TDCTARGETCNT_1:** RET TDC tristate buffer calibration counter value. Delay line loop oscillation is counted over two refclk cycles.
7:0	11h RW	**I_TDCTARGETCNT_0:** RET TDC tristate buffer calibration counter value. Delay line loop oscillation is counted over two refclk cycles.

14.13.1.12 Reg LCPLL_LF2 (LCPLL_LF2) — Offset 4100002Ch

RET.

Type	Size	Offset	Default
MMIO	32 bit	4100002Ch	0000030Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**I_USEIDVDATA_H:** RET NOT USED.Enable i_idvnmon to be used by DCO amplitude logic to adjust DCO tail current amplitude with idvnmon bits, where slow corner will be set to highest current, and fast corner set to lowest current.
9	1h RW	**I_DCODITHEREN_H:** RET DCO dithering enable signal (1st order dithering).
8	1h RW	**I_AFCCNTSEL:** RET AFC counter target, 0: 256 (0.4% tolerance) 1:512 (0.2% tolerance).
7:4	0h RO	**Reserved**
3:1	5h RW	**I_LOCKTHRESH:** RET Digital lock detect threshold, the PLL will generate plllockout when the phase error detected by TDC is within lockthresh number of TDC counts for 64 consecutive cycles.
0	0h RW	**I_LOCKTHRESHSEL:** RET Select bit between coarse threshold and fine threshold 1:coarse 0: fine.

14.13.1.13 Reg LCPLL_DFT0 (LCPLL_DFT0) — Offset 41000030h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000030h	78003C00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	7h RW	**I_PLLPWRMODE:** RET dcoen : pllpwrmode[0] cml2cmosenp : pllpwrmode[1] cml2cmosenn: pllpwrmode[2] irefout_en: pllpwrmode[3].
27	1h RW	**I_DCOAMPOVRDEN_H:** RET DCO amplitude override enable: 0 DCO amplitude set internally (default) 1 DCO amplitude is set by i_dcoamp<3:0> (DFT mode).
26	0h RW	**I_DCOCOARSE_OVRD_H:** RET DCO coarse frequency override signal: 0: DCO coarse tuning is set by AFC state machine (default) 1: DCO coarse frequency value is set by i_dcocoarse<7:0> .
25:24	0h RW	**I_DCOFINEDFTSEL:** RET DCO fine frequency and dco dither override: 00 DCO fine tuning is set by PLL closed loop (default) 01 DCO fine frequency value is set by i_dcofine<9:0>, and DCO dither value is set by i_dco_ditherext (DFT, open loop mode) 10 Internal SAW tooth pattern 11 Resvd.
23:16	00h RW	**I_DCOCOARSE:** RET DCO coarse tune frequency value, when dcocoarse_ovrd_h is '1', this input is used to override the value calculated from the Automatic Frequency Calibration (AFC) block.
15:14	0h RO	**Reserved**
13:10	Fh RW	**I_DCOAMP_2:** RET Amplitude override value for DCO, 0000 is min amplitude, 1111 is max amplitude, applied when i_dcoampovrden_h is high. .
9:8	0h RW	**I_DCOFINE_1:** RET DCO Fine tune bits override. (DCO DFT).
7:0	00h RW	**I_DCOFINE_0:** RET DCO Fine tune bits override. (DCO DFT).

14.13.1.14 Reg LCPLL_DFT1 (LCPLL_DFT1) — Offset 41000034h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**I_FBCLK_EXTSEL:** RET select for feedback clock mux 0 fbclk from pll core (default) 1 extfbclk (DFT mode).
28	0h RW	**I_FBDIVEXTEN_H:** RET External stimulus of 'reset', fbdivratio, fbdivselext(n-2,n-1,n,n+1,n+2 mux select), bindivexten applied to feedback divider, when this signal is asserted.
27	0h RW	**I_BINDIVEXTEN_H:** RET External binary divider enable signal. .
26:24	0h RW	**I_FBDIVSELEXT:** RET Not Used.
23:17	0h RO	**Reserved**
16	0h RW	**I_RCOMP_EN_H_RESVD:** RET NOT USED.Enable i_rcomp<7:0> to tune the reference resistor based current generator when asserted high.
15:10	0h RO	**Reserved**
9:8	0h RW	**I_ANA_OBSV_MUX_CTRL_1:** RET Analog o/p signals mux select.
7:4	0h RO	**Reserved**
3:0	0h RW	**I_DIG_OBSV_MUX_CTRL_0:** RET CMOS o/p signals mux select.

14.13.1.15 Reg LCPLL_DFT2Reg (LCPLL_DFT2) — Offset 41000038h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**I_TDCCALEXTEN_H:** RET TDC calibration values override enable.
29	0h RW	**I_BWMEASEN_H:** RET Bandwidth measurement enable signal.
28:24	00h RW	**I_BWPHASE:** RET Phase amplitude for bandwidth measurement.
23:21	0h RO	**Reserved**
20:16	00h RW	**I_CLOADCTRLHEXT_2:** RET cload control override for H Vernier line.
15:13	0h RO	**Reserved**
12:8	00h RW	**I_CLOADCTRLLEXT_1:** RET cload control override for L Vernier line.
7:5	0h RO	**Reserved**
4:0	00h RW	**I_TRIBUFCTRLEXT_0:** RET Tribufctrl control override .

14.13.1.16 Reg LCPLL_VISA_EN (LCPLL_VISA_EN) — Offset 4100003Ch

RET.

Type	Size	Offset	Default
MMIO	32 bit	4100003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**IDFX_VISAEN:** RET Visa enable.

14.13.1.17 Reg LCPLL_VISA_LANE0 (LCPLL_VISA_LANE0) — Offset 41000040h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**IDFX_VISA_BYPASS0:** RET Bypass bit for control lane 0.
15:8	00h RW	**IDFX_VISA_CONTROL_LANE0_1:** RET NOT USED : visa_control_lane0[15:11] visa_clk_sel_lane0 : visa_control_lane0[10:8] (clock mux select) visa_sel_lane0: visa_control_lane0[7:0] (lane0 mux select).
7:0	00h RW	**IDFX_VISA_CONTROL_LANE0_0:** RET NOT USED : visa_control_lane0[15:11] visa_clk_sel_lane0 : visa_control_lane0[10:8] (clock mux select) visa_sel_lane0: visa_control_lane0[7:0] (lane0 mux select).

14.13.1.18 Reg LCPLL_VISA_LANE1 (LCPLL_VISA_LANE1) — Offset 41000044h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**IDFX_VISA_BYPASS1:** RET Bypass bit for control lane 1.
15:8	00h RW	**IDFX_VISA_CONTROL_LANE1_1:** RET NOT USED : visa_control_lane1[15:11] visa_clk_sel_lane1 : visa_control_lane1[10:8] (clock mux select) visa_sel_lane1: visa_control_lane1[7:0] (lane0 mux select).
7:0	00h RW	**IDFX_VISA_CONTROL_LANE1_0:** RET NOT USED : visa_control_lane1[15:11] visa_clk_sel_lane1 : visa_control_lane1[10:8] (clock mux select) visa_sel_lane1: visa_control_lane1[7:0] (lane0 mux select).

14.13.1.19 Reg LCPLL_BONUS (LCPLL_BONUS) — Offset 41000048h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**I_PLL_BONUS_3:** RET BONUS.
23:16	00h RW	**I_PLL_BONUS_2:** RET BONUS.
15:8	00h RW	**I_PLL_BONUS_1:** RET BONUS.
7:0	00h RW	**I_PLL_BONUS_0:** RET BONUS.

14.13.1.20 Reg LCPLL_EBB0 (LCPLL_EBB0) — Offset 4100004Ch

RET.

Type	Size	Offset	Default
MMIO	32 bit	4100004Ch	0C000900h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ch RW	**I_PLLEBB_BONUS3_3:** RET BONUS.
23:16	00h RW	**I_PLLEBB_BONUS2_2:** RET BONUS.
15:8	09h RW	**I_PLLEBB_BONUS1_1:** RET BONUS.
7:0	00h RW	**I_PLLEBB_BONUS0_0:** RET BONUS.

14.13.1.21 Reg LCPLL_EBB1 (LCPLL_EBB1) — Offset 41000050h

RET.

Type	Size	Offset	Default
MMIO	32 bit	41000050h	2D001B00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	2Dh RW	**I_PLLEBB_BONUS7_7:** RET BONUS.
23:16	00h RW	**I_PLLEBB_BONUS6_6:** RET BONUS.
15:8	1Bh RW	**I_PLLEBB_BONUS5_5:** RET BONUS.
7:0	00h RW	**I_PLLEBB_BONUS4_4:** RET BONUS.

14.13.1.22 Reg Reserved_0 (RESERVED_0) — Offset 41000054h

Reserved

Type	Size	Offset	Default
MMIO	32 bit	41000054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.13.1.23 Reg Reserved_1 (RESERVED_1) — Offset 41000058h

Reserved

Note: Bit definitions are the same as RESERVED_0, offset 41000054h.

14.13.1.24 Reg LCPLL_CRIOP0 (LCPLL_CRIOP0) — Offset 4100005Ch

RO.

Type	Size	Offset	Default
MMIO	32 bit	4100005Ch	0000004Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	00h RO/V	**FRACDIV_SYNC_CRI_3:** RO Double buffered fractional divider ratio .
23:16	00h RO	**FRACDIV_SYNC_CRI_2:** RO Double buffered fractional divider ratio .
15:8	00h RO	**FRACDIV_SYNC_CRI_1:** RO Double buffered fractional divider ratio .
7:0	4Eh RO/V	**FBDIVRATIO_SYNC_CRI_0:** RO Double buffered feedback divider ratio .

14.13.1.25 Reg LCPLL_CRIOP1 (LCPLL_CRIOP1) — Offset 41000060h

RO.

Type	Size	Offset	Default
MMIO	32 bit	41000060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RO	**SSCSTEPSIZE_SYNC_CRI_2:** RO Double buffered SSC step size.
15:8	00h RO	**SSCSTEPSIZE_SYNC_CRI_1:** RO Double buffered SSC step size.
7:0	00h RO/V	**FEEDFWRDGAIN_SYNC_CRI_0:** RO Double buffered feedforward gain.

14.13.1.26 Reg LCPLL_CRIOP2 (LCPLL_CRIOP2) — Offset 41000064h

RO.

Type	Size	Offset	Default
MMIO	32 bit	41000064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RO/V	**FBDIV_UPDATE_ALLOWED_H_CRI:** RO Fbdivratio update allowed indicator.
12	0h RO/V	**SSC_UPDATE_ALLOWED_H_CRI:** RO SSC update allowed indicator.
11	0h RO	**SSCON_CRI:** RO SSC on; asserted when sscen is high, and PLL is locked.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**SSCSTATE_CRI:** RO SSC status; stays high until triangle shape is complete.
9:8	0h RO	**FRACSSC_CRI_1:** RO Fractional value from SSC.
7:0	00h RO	**FRACSSC_CRI_0:** RO Fractional value from SSC.

14.13.1.27 Reg LCPLL_CRIOP3 (LCPLL_CRIOP3) — Offset 41000068h

RO.

Type	Size	Offset	Default
MMIO	32 bit	41000068h	01FF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	1h RO/V	**CSELFINE_CRI_1:** RO Fine DCO control code.
23:16	FFh RO/V	**CSELFINE_CRI_0:** RO Fine DCO control code.
15	0h RO	**Reserved**
14	0h RO	**BWMEASDONE_CRI:** RO BWMEAS done status.
13:9	00h RO	**BANDWIDTH_CRI:** RO Bandwidth from BWMEAS.
8	0h RO	**DCGAIN_CRI_1:** RO DC gain from BWMEAS.
7:0	00h RO	**DCGAIN_CRI_0:** RO DC gain from BWMEAS.

14.13.1.28 Reg LCPLL_CRIOP4 (LCPLL_CRIOP4) — Offset 4100006Ch

RO.

Type	Size	Offset	Default
MMIO	32 bit	4100006Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**PEAKFREQ_CRI:** RO Peaking frequency index from BWMEAS.
24	0h RO	**PEAK_CRI_1:** RO Peaking from BWMEAS.
23:16	00h RO	**PEAK_CRI_0:** RO Peaking from BWMEAS.
15:9	00h RO	**SETTLETIME_CRI_2:** RO Settle Time from BWMEAS.
8	0h RO	**NOISEFLOOR_CRI_1:** RO Noise floor from BWMEAS.
7:0	00h RO	**NOISEFLOOR_CRI_0:** RO Noise floor from BWMEAS.

14.13.1.29 Reg LCPLL_CRIOP5 (LCPLL_CRIOP5) — Offset 41000070h

RO.

Type	Size	Offset	Default
MMIO	32 bit	41000070h	00400000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RO/V	**PLLLOCKOUT_CRI:** RO Mux between freqlock and phaselock based on fractional enable bit.
29	0h RO	**PLLUNLOCK_FLAG_CRI:** RO Sticky PLL unlock event indicator.
28	0h RO	**PHASELOCK_CRI:** RO Phase lock indicator; monitoring TDC output .

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO/V	**PLLLOCKMONITOR_CRI:** RO Non-stickly PLL lock indicator; continuously monitoring lock condition.
26	0h RO/V	**FREQLOCKOUT_CRI:** RO Freqency lock indicator; monitoring integral value in loop filter.
25	0h RO/V	**TDCDIR_CRI:** RO TDC dir from PLLDIG.
24	0h RO/V	**TDCDIR_BB_CRI:** RO TDC dir from TDC Sch.
23:21	2h RO/V	**PLLVERSION_CRI:** RO PLL Version.
20:17	0h RO	**OVERLAP_CRI:** RO Overlap between VernierL and VernierH thermometer codes.
16	0h RO	**TDCOUT_CRI_1:** RO TDC binary output code.
15:8	00h RO/V	**TDCOUT_CRI_0:** RO TDC binary output code.
7:0	00h RO/V	**FEEDFWRDGAIN_CAL_CRI:** RO Feedfwrdgain to Loop filter.

14.13.1.30 Reg LCPLL_CRIOP6 (LCPLL_CRIOP6) — Offset 41000074h

RO.

Type	Size	Offset	Default
MMIO	32 bit	41000074h	7F303C4Bh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	7Fh RO/V	**CSELAFC_CRI:** RO AFC code to DCO.
23	0h RO/V	**BIASCALDONE_CRI:** RO Bias calibration done status.
22	0h RO/V	**BIASOUTOFRANGE_CRI:** RO Asserted when input rcomp is out of range compared to bias calibration.
21:16	30h RO/V	**RCOMPCALIBOUT_CRI:** RO Rcomp value during bias calibration.
15	0h RO/V	**TDCDPMDONE_CRI:** RO TDC DPM done status.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**TDCDPMERROR_CRI:** RO TDC DPM error status.
13:8	3Ch RO/V	**RCOMPOUT_CRI:** RO Rcomp code to DCO.
7:0	4Bh RO/V	**M2FBDIVMOD_CRI:** RO Feedback divider ratio.

14.13.1.31 Reg LCPLL_CRIOP7 (LCPLL_CRIOP7) — Offset 41000078h

RO.

Type	Size	Offset	Default
MMIO	32 bit	41000078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	0h RO/V	**AFCCNTHIGH_CRI_1:** RO AFC binary search high count.
23:16	00h RO/V	**AFCCNTHIGH_CRI_0:** RO AFC binary search high count.
15:10	0h RO	**Reserved**
9:8	0h RO/V	**AFCCNTLOW_CRI_1:** RO AFC binary search low count.
7:0	00h RO/V	**AFCCNTLOW_CRI_0:** RO AFC binary search low count.

14.13.1.32 Reg LCPLL_CRIOP8 (LCPLL_CRIOP8) — Offset 4100007Ch

RO.

Type	Size	Offset	Default
MMIO	32 bit	4100007Ch	2000000Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	2h RO/V	**FBPREDIVRATIO_CRI:** RO Feedback divider prediv ratio.
27	0h RO/V	**TDCCALDONE_CRI:** RO TDC calibration done status.
26	0h RO/V	**AFCDONE_CRI:** RO AFC done status.
25	0h RO	**AFCERR_CRI:** RO AFC error status .
24	0h RO/V	**CALIBRESETB_CRI:** RO Internally generated calibration reset.
23:21	0h RO	**Reserved**
20:16	00h RO/V	**CLOADCTRLH_CRI_1:** RO TDC fine control code for H Vernier line.
15:13	0h RO	**Reserved**
12:8	00h RO/V	**CLOADCTRLL_CRI_0:** RO TDC fine control code for L Vernier line.
7	0h RO	**HALFTDCGAIN_CRI:** RO TDC dynamic gain control indicator.
6:5	0h RO/V	**TDCMODE_CRI_1:** RO TDC mode.
4:0	0Fh RO/V	**TRIBUFCTRL_CRI_0:** RO TDC coarse control code.

14.14 SPI Interface Registers

There are four SPI Interface registers:-

- SPI_0 Registers
- SPI_1 Registers
- SPI_2 Registers
- SPI_3 Registers

SPI Interface Registers	Address Offset	Table
SPI_0	48100000h - 481000FCh	Table 14-24
SPI_1	48102000h - 481020FCh	Table 14-25
SPI_2	48104000h - 481040FCh	Table 14-26
SPI_3	48106000h - 481060FCh	Table 14-27

14.14.1 SPI_0 Registers Summary

Table 14-24. Summary of SPI_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48100000h	4	CTRLR0	01000007h
48100004h	4	CTRLR1	00000000h
48100008h	4	SSIENR	00000000h
4810000Ch	4	MWCR	00000000h
48100010h	4	SER	00000000h
48100014h	4	BAUDR	00000000h
48100018h	4	TXFTLR	00000000h
4810001Ch	4	RXFTLR	00000000h
48100020h	4	TXFLR	00000000h
48100024h	4	RXFLR	00000000h
48100028h	4	SR	00000006h
4810002Ch	4	IMR	0000003Fh
48100030h	4	ISR	00000000h
48100034h	4	RISR	00000000h
48100038h	4	TXOICR	00000000h
4810003Ch	4	RXOICR	00000000h
48100040h	4	RXUICR	00000000h
48100044h	4	MSTICR	00000000h
48100048h	4	ICR	00000000h
4810004Ch	4	DMACR	00000000h
48100050h	4	DMATDLR	00000000h
48100054h	4	DMARDLR	00000000h
48100058h	4	IDR	FFFFFFFFh
4810005Ch	4	SSI_VERSION_ID	3430322Ah
48100060h	4	DR0	00000000h
48100064h	4	DR1	00000000h
48100068h	4	DR2	00000000h
4810006Ch	4	DR3	00000000h
48100070h	4	DR4	00000000h
48100074h	4	DR5	00000000h
48100078h	4	DR6	00000000h
4810007Ch	4	DR7	00000000h
48100080h	4	DR8	00000000h
48100084h	4	DR9	00000000h
48100088h	4	DR10	00000000h
4810008Ch	4	DR11	00000000h
48100090h	4	DR12	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48100094h	4	DR13	00000000h
48100098h	4	DR14	00000000h
4810009Ch	4	DR15	00000000h
481000A0h	4	DR16	00000000h
481000A4h	4	DR17	00000000h
481000A8h	4	DR18	00000000h
481000ACh	4	DR19	00000000h
481000B0h	4	DR20	00000000h
481000B4h	4	DR21	00000000h
481000B8h	4	DR22	00000000h
481000BCh	4	DR23	00000000h
481000C0h	4	DR24	00000000h
481000C4h	4	DR25	00000000h
481000C8h	4	DR26	00000000h
481000CCh	4	DR27	00000000h
481000D0h	4	DR28	00000000h
481000D4h	4	DR29	00000000h
481000D8h	4	DR30	00000000h
481000DCh	4	DR31	00000000h
481000E0h	4	DR32	00000000h
481000E4h	4	DR33	00000000h
481000E8h	4	DR34	00000000h
481000ECh	4	DR35	00000000h
481000F0h	4	RX_SAMPLE_DLY	00000000h
481000FCh	4	RSVD	00000000h

14.14.1.1 CTRLR0 — Offset 48100000h

Control Register 0 - This register controls the serial data transfer. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: SSI_CTRLR0_RST

Type	Size	Offset	Default
MMIO	32 bit	48100000h	01000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RW	**SSTE:** Slave Select Toggle Enable. When operating in SPI mode with clock phase (SCPH) set to 0, this register controls the behavior of the slave select line (ss_*_n) between data frames. If this register field is set to 1 the ss_*_n line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while ss_*_n is high; if this register field is set to 0 the ss_*_n will stay low and sclk will run continuously for the duration of the transfer. Note: This register is only valid when SSI_SCPH0_SSTOGGLE is set to 1.
23	0h RO	**Reserved**
22:21	0h RO/V	**SPI_FRF:** SPI Frame Format: Selects data frame format for Transmitting/Receiving the data Bits only valid when SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode. When SSI_SPI_MODE is configured for "Dual Mode", 10/11 combination is reserved. When SSI_SPI_MODE is configured for "Quad Mode", 11 combination is reserved.
20:16	00h RO/V	**DFS_32:** Data Frame Size in 32-bit transfer size mode. Used to select the data frame size in 32-bit transfer mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You are responsible for making sure that transmit data is right-justified before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 0x01, - DFS value should be multiple of 4 if SPI_FRF = 0x10, - DFS value should be multiple of 8 if SPI_FRF = 0x11.
15:12	0h RW	**CFS:** Control Frame Size. Selects the length of the control word for the Microwire frame format.
11	0h RW	**SRL:** Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the DW_apb_ssi is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back
10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**TMOD:** Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the DW_apb_ssi is configured as master device. 00 - Transmit & Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. There are only two valid combinations: 10 - Read 01 - Write
7	0h RW	**SCPOL:** Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the DW_apb_ssi master is not actively transferring data on the serial bus.
6	0h RW	**SCPH:** Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.
5:4	0h RW	**FRF:** Frame Format. Selects which serial protocol transfers the data.
3:0	7h RW	**DFS:** Data Frame Size. This register field is only valid when SSI_MAX_XFER_SIZE is configured to 16. If SSI_MAX_XFER_SIZE is configured to 32, then writing to this field will not have any effect. Selects the data frame length. When the data frame size is programmed to be less than 16 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 01, - DFS value should be multiple of 4 if SPI_FRF = 10, - DFS value should be multiple of 8 if SPI_FRF = 11.

14.14.1.2 CTRLR1 — Offset 48100004h

Control Register 1 - This register exists only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**NDF:** Number of Data Frames. When TMOD = 10 or TMOD = 11 , this register field sets the number of data frames to be continuously received by the DW_apb_ssi. The DW_apb_ssi continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When the DW_apb_ssi is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the DW_apb_ssi is configured as a serial slave.

14.14.1.3 SSIENR — Offset 48100008h

SSI Enable Register - This register enables and disables the DW_apb_ssi. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SSI_EN:** SSI Enable. Enables and disables all DW_apb_ssi operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the DW_apb_ssi control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

14.14.1.4 MWCR — Offset 4810000Ch

Microwire Control Register - This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**MHS:** Microwire Handshaking. Relevant only when the DW_apb_ssi is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the DW_apb_ssi checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register.
1	0h RW	**MDD:** Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the DW_apb_ssi MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the DW_apb_ssi MacroCell to the external serial device.
0	0h RW	**MWMOD:** Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

14.14.1.5 SER — Offset 48100010h

Slave Enable Register - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the DW_apb_ssi master. Up to 16 slave-select output pins are available on the DW_apb_ssi master. Register bits can be set or cleared when SSI_EN=0. If SSI_EN=1, then register bits can be set (to delay the slave select assertion while TX FIFO is getting filled) but cannot be cleared. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**SER:** Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (ss_x_n) from the DW_apb_ssi master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

14.14.1.6 BAUDR — Offset 48100014h

Baud Rate Select - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**SCKDV:** SSI Clock Divider. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fssi_clk/SCKDV where SCKDV is any even value between 2 and 65534. For example: for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz

14.14.1.7 TXFTLR — Offset 48100018h

Transmit FIFO Threshold Level - This register controls the threshold value for the transmit FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**TFT:** Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

14.14.1.8 RXFTLR — Offset 4810001Ch

Receive FIFO Threshold Level - This register controls the threshold value for the receive FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RFT:** Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

14.14.1.9 TXFLR — Offset 48100020h

Transmit FIFO Level Register - This register contains the number of valid data entries in the transmit FIFO memory. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXTFL:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.14.1.10 RXFLR — Offset 48100024h

Receive FIFO Level Register - This register contains the number of valid data entries in the receive FIFO memory. This register can be ready at any time. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXTFL:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.14.1.11 SR — Offset 48100028h

Status Register - This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt. Reset Value: 0x6

Type	Size	Offset	Default
MMIO	32 bit	48100028h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**DCOL:** Data Collision Error. Relevant only when the DW_apb_ssi is configured as a master device. This bit will be set if ss_in_n input is asserted by other master, when the DW_apb_ssi master is in the middle of the transfer. This informs the processor that the last data transfer was halted before completion. This bit is cleared when read.
5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.
2	1h RO/V	**TFE:** Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO/V	**BUSY:** SSI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the DW_apb_ssi is idle or disabled.

14.14.1.12 IMR — Offset 4810002Ch

Interrupt Mask Register - This read/write reigster masks or enables all interrupts generated by the DW_apb_ssi. When the DW_apb_ssi is configured as a slave device, the MSTIM bit field is not present. This changes the reset value from 0x3F for serial-master configurations to 0x1F for serial-slave configurations. Reset Value: (SSI_IS_MASTER == 1) ? 0x3F : 0x1F

Type	Size	Offset	Default
MMIO	32 bit	4810002Ch	0000003Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW	**MSTIM:** Multi-Master Contention Interrupt Mask. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	1h RW	**RXFIM:** Receive FIFO Full Interrupt Mask
3	1h RW	**RXOIM:** Receive FIFO Overflow Interrupt Mask
2	1h RW	**RXUIM:** Receive FIFO Underflow Interrupt Mask
1	1h RW	**TXOIM:** Transmit FIFO Overflow Interrupt Mask
0	1h RW	**TXEIM:** Transmit FIFO Empty Interrupt Mask

14.14.1.13 ISR — Offset 48100030h

Interrupt Status Register - This register reports the status of the DW_apb_ssi interrupts after they have been masked. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIS:** Multi-Master Contention Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIS:** Receive FIFO Full Interrupt Status
3	0h RO/V	**RXOIS:** Receive FIFO Overflow Interrupt Status
2	0h RO/V	**RXUIS:** Receive FIFO Underflow Interrupt Status
1	0h RO/V	**TXOIS:** Transmit FIFO Overflow Interrupt Status
0	0h RO/V	**TXEIS:** Transmit FIFO Empty Interrupt Status

14.14.1.14 RISR — Offset 48100034h

Raw Interrupt Status Register - This read-only register reports the status of the DW_apb_ssi interrupts prior to masking. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIR:** Multi-Master Contention Raw Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIR:** Receive FIFO Full Raw Interrupt Status
3	0h RO/V	**RXOIR:** Receive FIFO Overflow Raw Interrupt Status
2	0h RO/V	**RXUIR:** Receive FIFO Underflow Raw Interrupt Status
1	0h RO/V	**TXOIR:** Transmit FIFO Overflow Raw Interrupt Status
0	0h RO/V	**TXEIR:** Transmit FIFO Empty Raw Interrupt Status

14.14.1.15 TXOICR — Offset 48100038h

Transmit FIFO Overflow Interrupt Clear Register Register - Transmit FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TXOICR:** Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

14.14.1.16 RXOICR — Offset 4810003Ch

Receive FIFO Overflow Interrupt Clear Register - Receive FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXOICR:** Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

14.14.1.17 RXUICR — Offset 48100040h

Receive FIFO Underflow Interrupt Clear Register - Receive FIFO Underflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXUICR:** Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

14.14.1.18 MSTICR — Offset 48100044h

Multi-Master Interrupt Clear Register - Multi-Master Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**MSTICR:** Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_mst_intr interrupt; writing has no effect.

14.14.1.19 ICR — Offset 48100048h

Interrupt Clear Register - Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**ICR:** Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

14.14.1.20 DMACR — Offset 4810004Ch

DMA Control Register - This register is only valid when DW_apb_ssi is configured with a set of DMA Controller interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel

14.14.1.21 DMATDLR — Offset 48100050h

DMA Transmit Data Level - This register is only valid when the DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.14.1.22 DMARDLR — Offset 48100054h

DMA Receive Data Level - This register is only valid when DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.

14.14.1.23 IDR — Offset 48100058h

Identification Register - This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant. Reset Value: SSI_ID

Type	Size	Offset	Default
MMIO	32 bit	48100058h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**IDCODE:** Identification code. The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant.

14.14.1.24 SSI_VERSION_ID — Offset 4810005Ch

coreKit version ID Register - This read-only register stores the specific DW_apb_ssi component version. Reset Value: SSI_VERSION_ID

Type	Size	Offset	Default
MMIO	32 bit	4810005Ch	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**SSI_COMP_VERSION:** Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*.

14.14.1.25 DR0 — Offset 48100060h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48100060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

14.14.1.26 DR1 — Offset 48100064h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.27 DR2 — Offset 48100068h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.28 DR3 — Offset 4810006Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.29 DR4 — Offset 48100070h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.30 DR5 — Offset 48100074h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.31 DR6 — Offset 48100078h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.32 DR7 — Offset 4810007Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.33 DR8 — Offset 48100080h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.34 DR9 — Offset 48100084h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.35 DR10 — Offset 48100088h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.36 DR11 — Offset 4810008Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.37 DR12 — Offset 48100090h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.38 DR13 — Offset 48100094h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.39 DR14 — Offset 48100098h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.40 DR15 — Offset 4810009Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.41 DR16 — Offset 481000A0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.42 DR17 — Offset 481000A4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.43 DR18 — Offset 481000A8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.44 DR19 — Offset 481000ACh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.45 DR20 — Offset 481000B0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.46 DR21 — Offset 481000B4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.47 DR22 — Offset 481000B8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.48 DR23 — Offset 481000BCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.49 DR24 — Offset 481000C0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.50 DR25 — Offset 481000C4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.51 DR26 — Offset 481000C8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.52 DR27 — Offset 481000CCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.53 DR28 — Offset 481000D0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.54 DR29 — Offset 481000D4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.55 DR30 — Offset 481000D8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.56 DR31 — Offset 481000DCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.57 DR32 — Offset 481000E0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.58 DR33 — Offset 481000E4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.59 DR34 — Offset 481000E8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.60 DR35 — Offset 481000ECh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48100060h.

14.14.1.61 RX_SAMPLE_DLY — Offset 481000F0h

RX Sample Delay Register - This register is only valid when the DW_apb_ssi is configured with rxd sample delay logic (SSI_HAS_RX_SAMPLE_DELAY==1). When the DW_apb_ssi is not configured with rxd sample delay logic, this register will not exist and writing to its address location will have no effect; reading from its address will return zero. This register control the number of ssi_clk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	481000F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RSD:** Rxd Sample Delay. This register is used to delay the sample of the rxd input port. Each value represents a single ssi_clk delay on the sample of rxd. Note: If this register is programmed with a value that exceeds the depth of the internal shift registers (SSI_RX_DLY_SR_DEPTH) zero delay will be applied to the rxd sample.

14.14.1.62 RSVD — Offset 481000FCh

Reserved

Type	Size	Offset	Default
MMIO	32 bit	481000FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.14.2 SPI_1 Registers Summary

Table 14-25. Summary of SPI_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48102000h	4	CTRLR0	01000007h
48102004h	4	CTRLR1	00000000h
48102008h	4	SSIENR	00000000h
4810200Ch	4	MWCR	00000000h
48102010h	4	SER	00000000h
48102014h	4	BAUDR	00000000h
48102018h	4	TXFTLR	00000000h
4810201Ch	4	RXFTLR	00000000h
48102020h	4	TXFLR	00000000h
48102024h	4	RXFLR	00000000h
48102028h	4	SR	00000006h
4810202Ch	4	IMR	0000003Fh
48102030h	4	ISR	00000000h
48102034h	4	RISR	00000000h
48102038h	4	TXOICR	00000000h
4810203Ch	4	RXOICR	00000000h
48102040h	4	RXUICR	00000000h
48102044h	4	MSTICR	00000000h
48102048h	4	ICR	00000000h
4810204Ch	4	DMACR	00000000h
48102050h	4	DMATDLR	00000000h
48102054h	4	DMARDLR	00000000h
48102058h	4	IDR	FFFFFFFFh
4810205Ch	4	SSI_VERSION_ID	3430322Ah
48102060h	4	DR0	00000000h
48102064h	4	DR1	00000000h
48102068h	4	DR2	00000000h
4810206Ch	4	DR3	00000000h
48102070h	4	DR4	00000000h
48102074h	4	DR5	00000000h
48102078h	4	DR6	00000000h
4810207Ch	4	DR7	00000000h
48102080h	4	DR8	00000000h
48102084h	4	DR9	00000000h
48102088h	4	DR10	00000000h
4810208Ch	4	DR11	00000000h
48102090h	4	DR12	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48102094h	4	DR13	00000000h
48102098h	4	DR14	00000000h
4810209Ch	4	DR15	00000000h
481020A0h	4	DR16	00000000h
481020A4h	4	DR17	00000000h
481020A8h	4	DR18	00000000h
481020ACh	4	DR19	00000000h
481020B0h	4	DR20	00000000h
481020B4h	4	DR21	00000000h
481020B8h	4	DR22	00000000h
481020BCh	4	DR23	00000000h
481020C0h	4	DR24	00000000h
481020C4h	4	DR25	00000000h
481020C8h	4	DR26	00000000h
481020CCh	4	DR27	00000000h
481020D0h	4	DR28	00000000h
481020D4h	4	DR29	00000000h
481020D8h	4	DR30	00000000h
481020DCh	4	DR31	00000000h
481020E0h	4	DR32	00000000h
481020E4h	4	DR33	00000000h
481020E8h	4	DR34	00000000h
481020ECh	4	DR35	00000000h
481020F0h	4	RX_SAMPLE_DLY	00000000h
481020FCh	4	RSVD	00000000h

14.14.2.1 CTRLR0 — Offset 48102000h

Control Register 0 - This register controls the serial data transfer. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: SSI_CTRLR0_RST

Type	Size	Offset	Default
MMIO	32 bit	48102000h	01000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RW	**SSTE:** Slave Select Toggle Enable. When operating in SPI mode with clock phase (SCPH) set to 0, this register controls the behavior of the slave select line (ss_*_n) between data frames. If this register field is set to 1 the ss_*_n line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while ss_*_n is high; if this register field is set to 0 the ss_*_n will stay low and sclk will run continuously for the duration of the transfer. Note: This register is only valid when SSI_SCPH0_SSTOGGLE is set to 1.
23	0h RO	**Reserved**
22:21	0h RO/V	**SPI_FRF:** SPI Frame Format: Selects data frame format for Transmitting/Receiving the data Bits only valid when SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode. When SSI_SPI_MODE is configured for "Dual Mode", 10/11 combination is reserved. When SSI_SPI_MODE is configured for "Quad Mode", 11 combination is reserved.
20:16	00h RO/V	**DFS_32:** Data Frame Size in 32-bit transfer size mode. Used to select the data frame size in 32-bit transfer mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You are responsible for making sure that transmit data is right-justified before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 0x01, - DFS value should be multiple of 4 if SPI_FRF = 0x10, - DFS value should be multiple of 8 if SPI_FRF = 0x11.
15:12	0h RW	**CFS:** Control Frame Size. Selects the length of the control word for the Microwire frame format.
11	0h RW	**SRL:** Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the DW_apb_ssi is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back
10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**TMOD:** Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the DW_apb_ssi is configured as master device. 00 - Transmit & Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. There are only two valid combinations: 10 - Read 01 - Write
7	0h RW	**SCPOL:** Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the DW_apb_ssi master is not actively transferring data on the serial bus.
6	0h RW	**SCPH:** Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.
5:4	0h RW	**FRF:** Frame Format. Selects which serial protocol transfers the data.
3:0	7h RW	**DFS:** Data Frame Size. This register field is only valid when SSI_MAX_XFER_SIZE is configured to 16. If SSI_MAX_XFER_SIZE is configured to 32, then writing to this field will not have any effect. Selects the data frame length. When the data frame size is programmed to be less than 16 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 01, - DFS value should be multiple of 4 if SPI_FRF = 10, - DFS value should be multiple of 8 if SPI_FRF = 11.

14.14.2.2 CTRLR1 — Offset 48102004h

Control Register 1 - This register exists only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**NDF:** Number of Data Frames. When TMOD = 10 or TMOD = 11 , this register field sets the number of data frames to be continuously received by the DW_apb_ssi. The DW_apb_ssi continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When the DW_apb_ssi is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the DW_apb_ssi is configured as a serial slave.

14.14.2.3 SSIENR — Offset 48102008h

SSI Enable Register - This register enables and disables the DW_apb_ssi. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SSI_EN:** SSI Enable. Enables and disables all DW_apb_ssi operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the DW_apb_ssi control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

14.14.2.4 MWCR — Offset 4810200Ch

Microwire Control Register - This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810200Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**MHS:** Microwire Handshaking. Relevant only when the DW_apb_ssi is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the DW_apb_ssi checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register.
1	0h RW	**MDD:** Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the DW_apb_ssi MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the DW_apb_ssi MacroCell to the external serial device.
0	0h RW	**MWMOD:** Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

14.14.2.5 SER — Offset 48102010h

Slave Enable Register - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the DW_apb_ssi master. Up to 16 slave-select output pins are available on the DW_apb_ssi master. Register bits can be set or cleared when SSI_EN=0. If SSI_EN=1, then register bits can be set (to delay the slave select assertion while TX FIFO is getting filled) but cannot be cleared. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**SER:** Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (ss_x_n) from the DW_apb_ssi master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

14.14.2.6 BAUDR — Offset 48102014h

Baud Rate Select - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**SCKDV:** SSI Clock Divider. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fssi_clk/SCKDV where SCKDV is any even value between 2 and 65534. For example: for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz

14.14.2.7 TXFTLR — Offset 48102018h

Transmit FIFO Threshold Level - This register controls the threshold value for the transmit FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**TFT:** Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

14.14.2.8 RXFTLR — Offset 4810201Ch

Receive FIFO Threshold Level - This register controls the threshold value for the receive FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810201Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RFT:** Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

14.14.2.9 TXFLR — Offset 48102020h

Transmit FIFO Level Register - This register contains the number of valid data entries in the transmit FIFO memory. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXTFL:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.14.2.10 RXFLR — Offset 48102024h

Receive FIFO Level Register - This register contains the number of valid data entries in the receive FIFO memory. This register can be ready at any time. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXTFL:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.14.2.11 SR — Offset 48102028h

Status Register - This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt. Reset Value: 0x6

Type	Size	Offset	Default
MMIO	32 bit	48102028h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**DCOL:** Data Collision Error. Relevant only when the DW_apb_ssi is configured as a master device. This bit will be set if ss_in_n input is asserted by other master, when the DW_apb_ssi master is in the middle of the transfer. This informs the processor that the last data transfer was halted before completion. This bit is cleared when read.
5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.
2	1h RO/V	**TFE:** Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO/V	**BUSY:** SSI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the DW_apb_ssi is idle or disabled.

14.14.2.12 IMR — Offset 4810202Ch

Interrupt Mask Register - This read/write reigster masks or enables all interrupts generated by the DW_apb_ssi. When the DW_apb_ssi is configured as a slave device, the MSTIM bit field is not present. This changes the reset value from 0x3F for serial-master configurations to 0x1F for serial-slave configurations. Reset Value: (SSI_IS_MASTER == 1) ? 0x3F : 0x1F

Type	Size	Offset	Default
MMIO	32 bit	4810202Ch	0000003Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW	**MSTIM:** Multi-Master Contention Interrupt Mask. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	1h RW	**RXFIM:** Receive FIFO Full Interrupt Mask
3	1h RW	**RXOIM:** Receive FIFO Overflow Interrupt Mask
2	1h RW	**RXUIM:** Receive FIFO Underflow Interrupt Mask
1	1h RW	**TXOIM:** Transmit FIFO Overflow Interrupt Mask
0	1h RW	**TXEIM:** Transmit FIFO Empty Interrupt Mask

14.14.2.13 ISR — Offset 48102030h

Interrupt Status Register - This register reports the status of the DW_apb_ssi interrupts after they have been masked. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIS:** Multi-Master Contention Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIS:** Receive FIFO Full Interrupt Status
3	0h RO/V	**RXOIS:** Receive FIFO Overflow Interrupt Status
2	0h RO/V	**RXUIS:** Receive FIFO Underflow Interrupt Status
1	0h RO/V	**TXOIS:** Transmit FIFO Overflow Interrupt Status
0	0h RO/V	**TXEIS:** Transmit FIFO Empty Interrupt Status

14.14.2.14 RISR — Offset 48102034h

Raw Interrupt Status Register - This read-only register reports the status of the DW_apb_ssi interrupts prior to masking. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIR:** Multi-Master Contention Raw Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIR:** Receive FIFO Full Raw Interrupt Status
3	0h RO/V	**RXOIR:** Receive FIFO Overflow Raw Interrupt Status
2	0h RO/V	**RXUIR:** Receive FIFO Underflow Raw Interrupt Status
1	0h RO/V	**TXOIR:** Transmit FIFO Overflow Raw Interrupt Status
0	0h RO/V	**TXEIR:** Transmit FIFO Empty Raw Interrupt Status

14.14.2.15 TXOICR — Offset 48102038h

Transmit FIFO Overflow Interrupt Clear Register Register - Transmit FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TXOICR:** Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

14.14.2.16 RXOICR — Offset 4810203Ch

Receive FIFO Overflow Interrupt Clear Register - Receive FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810203Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXOICR:** Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

14.14.2.17 RXUICR — Offset 48102040h

Receive FIFO Underflow Interrupt Clear Register - Receive FIFO Underflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXUICR:** Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

14.14.2.18 MSTICR — Offset 48102044h

Multi-Master Interrupt Clear Register - Multi-Master Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**MSTICR:** Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_mst_intr interrupt; writing has no effect.

14.14.2.19 ICR — Offset 48102048h

Interrupt Clear Register - Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**ICR:** Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

14.14.2.20 DMACR — Offset 4810204Ch

DMA Control Register - This register is only valid when DW_apb_ssi is configured with a set of DMA Controller interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810204Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel

14.14.2.21 DMATDLR — Offset 48102050h

DMA Transmit Data Level - This register is only valid when the DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.14.2.22 DMARDLR — Offset 48102054h

DMA Receive Data Level - This register is only valid when DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.

14.14.2.23 IDR — Offset 48102058h

Identification Register - This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant. Reset Value: SSI_ID

Type	Size	Offset	Default
MMIO	32 bit	48102058h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**IDCODE:** Identification code. The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant.

14.14.2.24 SSI_VERSION_ID — Offset 4810205Ch

coreKit version ID Register - This read-only register stores the specific DW_apb_ssi component version. Reset Value: SSI_VERSION_ID

Type	Size	Offset	Default
MMIO	32 bit	4810205Ch	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**SSI_COMP_VERSION:** Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*.

14.14.2.25 DR0 — Offset 48102060h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48102060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

14.14.2.26 DR1 — Offset 48102064h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.27 DR2 — Offset 48102068h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.28 DR3 — Offset 4810206Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.29 DR4 — Offset 48102070h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.30 DR5 — Offset 48102074h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.31 DR6 — Offset 48102078h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.32 DR7 — Offset 4810207Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.33 DR8 — Offset 48102080h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.34 DR9 — Offset 48102084h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.35 DR10 — Offset 48102088h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.36 DR11 — Offset 4810208Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.37 DR12 — Offset 48102090h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.38 DR13 — Offset 48102094h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.39 DR14 — Offset 48102098h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.40 DR15 — Offset 4810209Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.41 DR16 — Offset 481020A0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.42 DR17 — Offset 481020A4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.43 DR18 — Offset 481020A8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.44 DR19 — Offset 481020ACh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.45 DR20 — Offset 481020B0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.46 DR21 — Offset 481020B4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.47 DR22 — Offset 481020B8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.48 DR23 — Offset 481020BCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.49 DR24 — Offset 481020C0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.50 DR25 — Offset 481020C4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.51 DR26 — Offset 481020C8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.52 DR27 — Offset 481020CCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.53 DR28 — Offset 481020D0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.54 DR29 — Offset 481020D4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.55 DR30 — Offset 481020D8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.56 DR31 — Offset 481020DCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.57 DR32 — Offset 481020E0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.58 DR33 — Offset 481020E4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.59 DR34 — Offset 481020E8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.60 DR35 — Offset 481020ECh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48102060h.

14.14.2.61 RX_SAMPLE_DLY — Offset 481020F0h

RX Sample Delay Register - This register is only valid when the DW_apb_ssi is configured with rxd sample delay logic (SSI_HAS_RX_SAMPLE_DELAY==1). When the DW_apb_ssi is not configured with rxd sample delay logic, this register will not exist and writing to its address location will have no effect; reading from its address will return zero. This register control the number of ssi_clk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	481020F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RSD:** Rxd Sample Delay. This register is used to delay the sample of the rxd input port. Each value represents a single ssi_clk delay on the sample of rxd. Note: If this register is programmed with a value that exceeds the depth of the internal shift registers (SSI_RX_DLY_SR_DEPTH) zero delay will be applied to the rxd sample.

14.14.2.62 RSVD — Offset 481020FCh

Reserved

Type	Size	Offset	Default
MMIO	32 bit	481020FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.14.3 SPI_2 Registers Summary

Table 14-26. Summary of SPI_2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48104000h	4	CTRLR0	01000007h
48104004h	4	CTRLR1	00000000h
48104008h	4	SSIENR	00000000h
4810400Ch	4	MWCR	00000000h
48104010h	4	SER	00000000h
48104014h	4	BAUDR	00000000h
48104018h	4	TXFTLR	00000000h
4810401Ch	4	RXFTLR	00000000h
48104020h	4	TXFLR	00000000h
48104024h	4	RXFLR	00000000h
48104028h	4	SR	00000006h
4810402Ch	4	IMR	0000003Fh
48104030h	4	ISR	00000000h
48104034h	4	RISR	00000000h
48104038h	4	TXOICR	00000000h
4810403Ch	4	RXOICR	00000000h
48104040h	4	RXUICR	00000000h
48104044h	4	MSTICR	00000000h
48104048h	4	ICR	00000000h
4810404Ch	4	DMACR	00000000h
48104050h	4	DMATDLR	00000000h
48104054h	4	DMARDLR	00000000h
48104058h	4	IDR	FFFFFFFFh
4810405Ch	4	SSI_VERSION_ID	3430322Ah
48104060h	4	DR0	00000000h
48104064h	4	DR1	00000000h
48104068h	4	DR2	00000000h
4810406Ch	4	DR3	00000000h
48104070h	4	DR4	00000000h
48104074h	4	DR5	00000000h
48104078h	4	DR6	00000000h
4810407Ch	4	DR7	00000000h
48104080h	4	DR8	00000000h
48104084h	4	DR9	00000000h
48104088h	4	DR10	00000000h
4810408Ch	4	DR11	00000000h
48104090h	4	DR12	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48104094h	4	DR13	00000000h
48104098h	4	DR14	00000000h
4810409Ch	4	DR15	00000000h
481040A0h	4	DR16	00000000h
481040A4h	4	DR17	00000000h
481040A8h	4	DR18	00000000h
481040ACh	4	DR19	00000000h
481040B0h	4	DR20	00000000h
481040B4h	4	DR21	00000000h
481040B8h	4	DR22	00000000h
481040BCh	4	DR23	00000000h
481040C0h	4	DR24	00000000h
481040C4h	4	DR25	00000000h
481040C8h	4	DR26	00000000h
481040CCh	4	DR27	00000000h
481040D0h	4	DR28	00000000h
481040D4h	4	DR29	00000000h
481040D8h	4	DR30	00000000h
481040DCh	4	DR31	00000000h
481040E0h	4	DR32	00000000h
481040E4h	4	DR33	00000000h
481040E8h	4	DR34	00000000h
481040ECh	4	DR35	00000000h
481040F0h	4	RX_SAMPLE_DLY	00000000h
481040FCh	4	RSVD	00000000h

14.14.3.1 CTRLR0 — Offset 48104000h

Control Register 0 - This register controls the serial data transfer. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: SSI_CTRLR0_RST

Type	Size	Offset	Default
MMIO	32 bit	48104000h	01000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RW	**SSTE:** Slave Select Toggle Enable. When operating in SPI mode with clock phase (SCPH) set to 0, this register controls the behavior of the slave select line (ss_*_n) between data frames. If this register field is set to 1 the ss_*_n line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while ss_*_n is high; if this register field is set to 0 the ss_*_n will stay low and sclk will run continuously for the duration of the transfer. Note: This register is only valid when SSI_SCPH0_SSTOGGLE is set to 1.
23	0h RO	**Reserved**
22:21	0h RO/V	**SPI_FRF:** SPI Frame Format: Selects data frame format for Transmitting/Receiving the data Bits only valid when SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode. When SSI_SPI_MODE is configured for "Dual Mode", 10/11 combination is reserved. When SSI_SPI_MODE is configured for "Quad Mode", 11 combination is reserved.
20:16	00h RO/V	**DFS_32:** Data Frame Size in 32-bit transfer size mode. Used to select the data frame size in 32-bit transfer mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You are responsible for making sure that transmit data is right-justified before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 0x01, - DFS value should be multiple of 4 if SPI_FRF = 0x10, - DFS value should be multiple of 8 if SPI_FRF = 0x11.
15:12	0h RW	**CFS:** Control Frame Size. Selects the length of the control word for the Microwire frame format.
11	0h RW	**SRL:** Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the DW_apb_ssi is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back
10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**TMOD:** Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the DW_apb_ssi is configured as master device. 00 - Transmit & Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. There are only two valid combinations: 10 - Read 01 - Write
7	0h RW	**SCPOL:** Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the DW_apb_ssi master is not actively transferring data on the serial bus.
6	0h RW	**SCPH:** Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.
5:4	0h RW	**FRF:** Frame Format. Selects which serial protocol transfers the data.
3:0	7h RW	**DFS:** Data Frame Size. This register field is only valid when SSI_MAX_XFER_SIZE is configured to 16. If SSI_MAX_XFER_SIZE is configured to 32, then writing to this field will not have any effect. Selects the data frame length. When the data frame size is programmed to be less than 16 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 01, - DFS value should be multiple of 4 if SPI_FRF = 10, - DFS value should be multiple of 8 if SPI_FRF = 11.

14.14.3.2 CTRLR1 — Offset 48104004h

Control Register 1 - This register exists only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**NDF:** Number of Data Frames. When TMOD = 10 or TMOD = 11 , this register field sets the number of data frames to be continuously received by the DW_apb_ssi. The DW_apb_ssi continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When the DW_apb_ssi is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the DW_apb_ssi is configured as a serial slave.

14.14.3.3 SSIENR — Offset 48104008h

SSI Enable Register - This register enables and disables the DW_apb_ssi. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SSI_EN:** SSI Enable. Enables and disables all DW_apb_ssi operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the DW_apb_ssi control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

14.14.3.4 MWCR — Offset 4810400Ch

Microwire Control Register - This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810400Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**MHS:** Microwire Handshaking. Relevant only when the DW_apb_ssi is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the DW_apb_ssi checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register.
1	0h RW	**MDD:** Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the DW_apb_ssi MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the DW_apb_ssi MacroCell to the external serial device.
0	0h RW	**MWMOD:** Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

14.14.3.5 SER — Offset 48104010h

Slave Enable Register - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the DW_apb_ssi master. Up to 16 slave-select output pins are available on the DW_apb_ssi master. Register bits can be set or cleared when SSI_EN=0. If SSI_EN=1, then register bits can be set (to delay the slave select assertion while TX FIFO is getting filled) but cannot be cleared. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**SER:** Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (ss_x_n) from the DW_apb_ssi master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

14.14.3.6 BAUDR — Offset 48104014h

Baud Rate Select - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**SCKDV:** SSI Clock Divider. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fssi_clk/SCKDV where SCKDV is any even value between 2 and 65534. For example: for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz

14.14.3.7 TXFTLR — Offset 48104018h

Transmit FIFO Threshold Level - This register controls the threshold value for the transmit FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**TFT:** Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

14.14.3.8 RXFTLR — Offset 4810401Ch

Receive FIFO Threshold Level - This register controls the threshold value for the receive FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810401Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RFT:** Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

14.14.3.9 TXFLR — Offset 48104020h

Transmit FIFO Level Register - This register contains the number of valid data entries in the transmit FIFO memory. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXTFL:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.14.3.10 RXFLR — Offset 48104024h

Receive FIFO Level Register - This register contains the number of valid data entries in the receive FIFO memory. This register can be ready at any time. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXTFL:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.14.3.11 SR — Offset 48104028h

Status Register - This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt. Reset Value: 0x6

Type	Size	Offset	Default
MMIO	32 bit	48104028h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**DCOL:** Data Collision Error. Relevant only when the DW_apb_ssi is configured as a master device. This bit will be set if ss_in_n input is asserted by other master, when the DW_apb_ssi master is in the middle of the transfer. This informs the processor that the last data transfer was halted before completion. This bit is cleared when read.
5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.
2	1h RO/V	**TFE:** Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO/V	**BUSY:** SSI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the DW_apb_ssi is idle or disabled.

14.14.3.12 IMR — Offset 4810402Ch

Interrupt Mask Register - This read/write reigster masks or enables all interrupts generated by the DW_apb_ssi. When the DW_apb_ssi is configured as a slave device, the MSTIM bit field is not present. This changes the reset value from 0x3F for serial-master configurations to 0x1F for serial-slave configurations. Reset Value: (SSI_IS_MASTER == 1) ? 0x3F : 0x1F

Type	Size	Offset	Default
MMIO	32 bit	4810402Ch	0000003Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW	**MSTIM:** Multi-Master Contention Interrupt Mask. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	1h RW	**RXFIM:** Receive FIFO Full Interrupt Mask
3	1h RW	**RXOIM:** Receive FIFO Overflow Interrupt Mask
2	1h RW	**RXUIM:** Receive FIFO Underflow Interrupt Mask
1	1h RW	**TXOIM:** Transmit FIFO Overflow Interrupt Mask
0	1h RW	**TXEIM:** Transmit FIFO Empty Interrupt Mask

14.14.3.13 ISR — Offset 48104030h

Interrupt Status Register - This register reports the status of the DW_apb_ssi interrupts after they have been masked. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIS:** Multi-Master Contention Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIS:** Receive FIFO Full Interrupt Status
3	0h RO/V	**RXOIS:** Receive FIFO Overflow Interrupt Status
2	0h RO/V	**RXUIS:** Receive FIFO Underflow Interrupt Status
1	0h RO/V	**TXOIS:** Transmit FIFO Overflow Interrupt Status
0	0h RO/V	**TXEIS:** Transmit FIFO Empty Interrupt Status

14.14.3.14 RISR — Offset 48104034h

Raw Interrupt Status Register - This read-only register reports the status of the DW_apb_ssi interrupts prior to masking. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIR:** Multi-Master Contention Raw Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIR:** Receive FIFO Full Raw Interrupt Status
3	0h RO/V	**RXOIR:** Receive FIFO Overflow Raw Interrupt Status
2	0h RO/V	**RXUIR:** Receive FIFO Underflow Raw Interrupt Status
1	0h RO/V	**TXOIR:** Transmit FIFO Overflow Raw Interrupt Status
0	0h RO/V	**TXEIR:** Transmit FIFO Empty Raw Interrupt Status

14.14.3.15 TXOICR — Offset 48104038h

Transmit FIFO Overflow Interrupt Clear Register Register - Transmit FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TXOICR:** Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

14.14.3.16 RXOICR — Offset 4810403Ch

Receive FIFO Overflow Interrupt Clear Register - Receive FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810403Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXOICR:** Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

14.14.3.17 RXUICR — Offset 48104040h

Receive FIFO Underflow Interrupt Clear Register - Receive FIFO Underflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXUICR:** Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

14.14.3.18 MSTICR — Offset 48104044h

Multi-Master Interrupt Clear Register - Multi-Master Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**MSTICR:** Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_mst_intr interrupt; writing has no effect.

14.14.3.19 ICR — Offset 48104048h

Interrupt Clear Register - Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**ICR:** Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

14.14.3.20 DMACR — Offset 4810404Ch

DMA Control Register - This register is only valid when DW_apb_ssi is configured with a set of DMA Controller interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810404Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel

14.14.3.21 DMATDLR — Offset 48104050h

DMA Transmit Data Level - This register is only valid when the DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.14.3.22 DMARDLR — Offset 48104054h

DMA Receive Data Level - This register is only valid when DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.

14.14.3.23 IDR — Offset 48104058h

Identification Register - This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant. Reset Value: SSI_ID

Type	Size	Offset	Default
MMIO	32 bit	48104058h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**IDCODE:** Identification code. The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant.

14.14.3.24 SSI_VERSION_ID — Offset 4810405Ch

coreKit version ID Register - This read-only register stores the specific DW_apb_ssi component version. Reset Value: SSI_VERSION_ID

Type	Size	Offset	Default
MMIO	32 bit	4810405Ch	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**SSI_COMP_VERSION:** Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*.

14.14.3.25 DR0 — Offset 48104060h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48104060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

14.14.3.26 DR1 — Offset 48104064h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.27 DR2 — Offset 48104068h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.28 DR3 — Offset 4810406Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.29 DR4 — Offset 48104070h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.30 DR5 — Offset 48104074h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.31 DR6 — Offset 48104078h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.32 DR7 — Offset 4810407Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.33 DR8 — Offset 48104080h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.34 DR9 — Offset 48104084h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.35 DR10 — Offset 48104088h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.36 DR11 — Offset 4810408Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.37 DR12 — Offset 48104090h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.38 DR13 — Offset 48104094h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.39 DR14 — Offset 48104098h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.40 DR15 — Offset 4810409Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.41 DR16 — Offset 481040A0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.42 DR17 — Offset 481040A4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.43 DR18 — Offset 481040A8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.44 DR19 — Offset 481040ACh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.45 DR20 — Offset 481040B0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.46 DR21 — Offset 481040B4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.47 DR22 — Offset 481040B8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.48 DR23 — Offset 481040BCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.49 DR24 — Offset 481040C0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.50 DR25 — Offset 481040C4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.51 DR26 — Offset 481040C8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.52 DR27 — Offset 481040CCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.53 DR28 — Offset 481040D0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.54 DR29 — Offset 481040D4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.55 DR30 — Offset 481040D8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.56 DR31 — Offset 481040DCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.57 DR32 — Offset 481040E0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.58 DR33 — Offset 481040E4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.59 DR34 — Offset 481040E8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.60 DR35 — Offset 481040ECh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48104060h.

14.14.3.61 RX_SAMPLE_DLY — Offset 481040F0h

RX Sample Delay Register - This register is only valid when the DW_apb_ssi is configured with rxd sample delay logic (SSI_HAS_RX_SAMPLE_DELAY==1). When the DW_apb_ssi is not configured with rxd sample delay logic, this register will not exist and writing to its address location will have no effect; reading from its address will return zero. This register control the number of ssi_clk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	481040F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RSD:** Rxd Sample Delay. This register is used to delay the sample of the rxd input port. Each value represents a single ssi_clk delay on the sample of rxd. Note: If this register is programmed with a value that exceeds the depth of the internal shift registers (SSI_RX_DLY_SR_DEPTH) zero delay will be applied to the rxd sample.

14.14.3.62 RSVD — Offset 481040FCh

Reserved

Type	Size	Offset	Default
MMIO	32 bit	481040FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.14.4 SPI_3 Registers Summary

Table 14-27. Summary of SPI_3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48106000h	4	CTRLR0	01000007h
48106004h	4	CTRLR1	00000000h
48106008h	4	SSIENR	00000000h
4810600Ch	4	MWCR	00000000h
48106010h	4	SER	00000000h
48106014h	4	BAUDR	00000000h
48106018h	4	TXFTLR	00000000h
4810601Ch	4	RXFTLR	00000000h
48106020h	4	TXFLR	00000000h
48106024h	4	RXFLR	00000000h
48106028h	4	SR	00000006h
4810602Ch	4	IMR	0000003Fh
48106030h	4	ISR	00000000h
48106034h	4	RISR	00000000h
48106038h	4	TXOICR	00000000h
4810603Ch	4	RXOICR	00000000h
48106040h	4	RXUICR	00000000h
48106044h	4	MSTICR	00000000h
48106048h	4	ICR	00000000h
4810604Ch	4	DMACR	00000000h
48106050h	4	DMATDLR	00000000h
48106054h	4	DMARDLR	00000000h
48106058h	4	IDR	FFFFFFFFh
4810605Ch	4	SSI_VERSION_ID	3430322Ah
48106060h	4	DR0	00000000h
48106064h	4	DR1	00000000h
48106068h	4	DR2	00000000h
4810606Ch	4	DR3	00000000h
48106070h	4	DR4	00000000h
48106074h	4	DR5	00000000h
48106078h	4	DR6	00000000h
4810607Ch	4	DR7	00000000h
48106080h	4	DR8	00000000h
48106084h	4	DR9	00000000h
48106088h	4	DR10	00000000h
4810608Ch	4	DR11	00000000h
48106090h	4	DR12	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48106094h	4	DR13	00000000h
48106098h	4	DR14	00000000h
4810609Ch	4	DR15	00000000h
481060A0h	4	DR16	00000000h
481060A4h	4	DR17	00000000h
481060A8h	4	DR18	00000000h
481060ACh	4	DR19	00000000h
481060B0h	4	DR20	00000000h
481060B4h	4	DR21	00000000h
481060B8h	4	DR22	00000000h
481060BCh	4	DR23	00000000h
481060C0h	4	DR24	00000000h
481060C4h	4	DR25	00000000h
481060C8h	4	DR26	00000000h
481060CCh	4	DR27	00000000h
481060D0h	4	DR28	00000000h
481060D4h	4	DR29	00000000h
481060D8h	4	DR30	00000000h
481060DCh	4	DR31	00000000h
481060E0h	4	DR32	00000000h
481060E4h	4	DR33	00000000h
481060E8h	4	DR34	00000000h
481060ECh	4	DR35	00000000h
481060F0h	4	RX_SAMPLE_DLY	00000000h
481060FCh	4	RSVD	00000000h

14.14.4.1 CTRLR0 — Offset 48106000h

Control Register 0 - This register controls the serial data transfer. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: SSI_CTRLR0_RST

Type	Size	Offset	Default
MMIO	32 bit	48106000h	01000007h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RW	**SSTE:** Slave Select Toggle Enable. When operating in SPI mode with clock phase (SCPH) set to 0, this register controls the behavior of the slave select line (ss_*_n) between data frames. If this register field is set to 1 the ss_*_n line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while ss_*_n is high; if this register field is set to 0 the ss_*_n will stay low and sclk will run continuously for the duration of the transfer. Note: This register is only valid when SSI_SCPH0_SSTOGGLE is set to 1.
23	0h RO	**Reserved**
22:21	0h RO/V	**SPI_FRF:** SPI Frame Format: Selects data frame format for Transmitting/Receiving the data Bits only valid when SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode. When SSI_SPI_MODE is configured for "Dual Mode", 10/11 combination is reserved. When SSI_SPI_MODE is configured for "Quad Mode", 11 combination is reserved.
20:16	00h RO/V	**DFS_32:** Data Frame Size in 32-bit transfer size mode. Used to select the data frame size in 32-bit transfer mode. These bits are only valid when SSI_MAX_XFER_SIZE is configured to 32. When the data frame size is programmed to be less than 32 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You are responsible for making sure that transmit data is right-justified before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 0x01, - DFS value should be multiple of 4 if SPI_FRF = 0x10, - DFS value should be multiple of 8 if SPI_FRF = 0x11.
15:12	0h RW	**CFS:** Control Frame Size. Selects the length of the control word for the Microwire frame format.
11	0h RW	**SRL:** Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the DW_apb_ssi is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back
10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**TMOD:** Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode. This transfer mode is only valid when the DW_apb_ssi is configured as master device. 00 - Transmit & Receive 01 - Transmit Only 10 - Receive Only 11 - EEPROM Read When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. There are only two valid combinations: 10 - Read 01 - Write
7	0h RW	**SCPOL:** Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the DW_apb_ssi master is not actively transferring data on the serial bus.
6	0h RW	**SCPH:** Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.
5:4	0h RW	**FRF:** Frame Format. Selects which serial protocol transfers the data.
3:0	7h RW	**DFS:** Data Frame Size. This register field is only valid when SSI_MAX_XFER_SIZE is configured to 16. If SSI_MAX_XFER_SIZE is configured to 32, then writing to this field will not have any effect. Selects the data frame length. When the data frame size is programmed to be less than 16 bits, the receive data are automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data Note: When SSI_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00. - DFS value should be multiple of 2 if SPI_FRF = 01, - DFS value should be multiple of 4 if SPI_FRF = 10, - DFS value should be multiple of 8 if SPI_FRF = 11.

14.14.4.2 CTRLR1 — Offset 48106004h

Control Register 1 - This register exists only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**NDF:** Number of Data Frames. When TMOD = 10 or TMOD = 11 , this register field sets the number of data frames to be continuously received by the DW_apb_ssi. The DW_apb_ssi continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When the DW_apb_ssi is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the DW_apb_ssi is configured as a serial slave.

14.14.4.3 SSIENR — Offset 48106008h

SSI Enable Register - This register enables and disables the DW_apb_ssi. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**SSI_EN:** SSI Enable. Enables and disables all DW_apb_ssi operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the DW_apb_ssi control registers when enabled. When disabled, the ssi_sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

14.14.4.4 MWCR — Offset 4810600Ch

Microwire Control Register - This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810600Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**MHS:** Microwire Handshaking. Relevant only when the DW_apb_ssi is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the DW_apb_ssi checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register.
1	0h RW	**MDD:** Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the DW_apb_ssi MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the DW_apb_ssi MacroCell to the external serial device.
0	0h RW	**MWMOD:** Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

14.14.4.5 SER — Offset 48106010h

Slave Enable Register - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the DW_apb_ssi master. Up to 16 slave-select output pins are available on the DW_apb_ssi master. Register bits can be set or cleared when SSI_EN=0. If SSI_EN=1, then register bits can be set (to delay the slave select assertion while TX FIFO is getting filled) but cannot be cleared. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**SER:** Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (ss_x_n) from the DW_apb_ssi master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

14.14.4.6 BAUDR — Offset 48106014h

Baud Rate Select - This register is valid only when the DW_apb_ssi is configured as a master device. When the DW_apb_ssi is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**SCKDV:** SSI Clock Divider. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fssi_clk/SCKDV where SCKDV is any even value between 2 and 65534. For example: for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz

14.14.4.7 TXFTLR — Offset 48106018h

Transmit FIFO Threshold Level - This register controls the threshold value for the transmit FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**TFT:** Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

14.14.4.8 RXFTLR — Offset 4810601Ch

Receive FIFO Threshold Level - This register controls the threshold value for the receive FIFO memory. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810601Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RFT:** Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

14.14.4.9 TXFLR — Offset 48106020h

Transmit FIFO Level Register - This register contains the number of valid data entries in the transmit FIFO memory. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TXTFL:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

14.14.4.10 RXFLR — Offset 48106024h

Receive FIFO Level Register - This register contains the number of valid data entries in the receive FIFO memory. This register can be ready at any time. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RXTFL:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

14.14.4.11 SR — Offset 48106028h

Status Register - This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt. Reset Value: 0x6

Type	Size	Offset	Default
MMIO	32 bit	48106028h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**DCOL:** Data Collision Error. Relevant only when the DW_apb_ssi is configured as a master device. This bit will be set if ss_in_n input is asserted by other master, when the DW_apb_ssi master is in the middle of the transfer. This informs the processor that the last data transfer was halted before completion. This bit is cleared when read.
5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.
2	1h RO/V	**TFE:** Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO/V	**BUSY:** SSI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the DW_apb_ssi is idle or disabled.

14.14.4.12 IMR — Offset 4810602Ch

Interrupt Mask Register - This read/write reigster masks or enables all interrupts generated by the DW_apb_ssi. When the DW_apb_ssi is configured as a slave device, the MSTIM bit field is not present. This changes the reset value from 0x3F for serial-master configurations to 0x1F for serial-slave configurations. Reset Value: (SSI_IS_MASTER == 1) ? 0x3F : 0x1F

Type	Size	Offset	Default
MMIO	32 bit	4810602Ch	0000003Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	1h RW	**MSTIM:** Multi-Master Contention Interrupt Mask. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	1h RW	**RXFIM:** Receive FIFO Full Interrupt Mask
3	1h RW	**RXOIM:** Receive FIFO Overflow Interrupt Mask
2	1h RW	**RXUIM:** Receive FIFO Underflow Interrupt Mask
1	1h RW	**TXOIM:** Transmit FIFO Overflow Interrupt Mask
0	1h RW	**TXEIM:** Transmit FIFO Empty Interrupt Mask

14.14.4.13 ISR — Offset 48106030h

Interrupt Status Register - This register reports the status of the DW_apb_ssi interrupts after they have been masked. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIS:** Multi-Master Contention Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIS:** Receive FIFO Full Interrupt Status
3	0h RO/V	**RXOIS:** Receive FIFO Overflow Interrupt Status
2	0h RO/V	**RXUIS:** Receive FIFO Underflow Interrupt Status
1	0h RO/V	**TXOIS:** Transmit FIFO Overflow Interrupt Status
0	0h RO/V	**TXEIS:** Transmit FIFO Empty Interrupt Status

14.14.4.14 RISR — Offset 48106034h

Raw Interrupt Status Register - This read-only register reports the status of the DW_apb_ssi interrupts prior to masking. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RO/V	**MSTIR:** Multi-Master Contention Raw Interrupt Status. This bit field is not present if the DW_apb_ssi is configured as a serial-slave device.
4	0h RO/V	**RXFIR:** Receive FIFO Full Raw Interrupt Status
3	0h RO/V	**RXOIR:** Receive FIFO Overflow Raw Interrupt Status
2	0h RO/V	**RXUIR:** Receive FIFO Underflow Raw Interrupt Status
1	0h RO/V	**TXOIR:** Transmit FIFO Overflow Raw Interrupt Status
0	0h RO/V	**TXEIR:** Transmit FIFO Empty Raw Interrupt Status

14.14.4.15 TXOICR — Offset 48106038h

Transmit FIFO Overflow Interrupt Clear Register Register - Transmit FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TXOICR:** Clear Transmit FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

14.14.4.16 RXOICR — Offset 4810603Ch

Receive FIFO Overflow Interrupt Clear Register - Receive FIFO Overflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810603Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXOICR:** Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

14.14.4.17 RXUICR — Offset 48106040h

Receive FIFO Underflow Interrupt Clear Register - Receive FIFO Underflow Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**RXUICR:** Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

14.14.4.18 MSTICR — Offset 48106044h

Multi-Master Interrupt Clear Register - Multi-Master Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**MSTICR:** Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_mst_intr interrupt; writing has no effect.

14.14.4.19 ICR — Offset 48106048h

Interrupt Clear Register - Interrupt Clear Register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**ICR:** Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

14.14.4.20 DMACR — Offset 4810604Ch

DMA Control Register - This register is only valid when DW_apb_ssi is configured with a set of DMA Controller interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	4810604Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel.
0	0h RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel

14.14.4.21 DMATDLR — Offset 48106050h

DMA Transmit Data Level - This register is only valid when the DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

14.14.4.22 DMARDLR — Offset 48106054h

DMA Receive Data Level - This register is only valid when DW_apb_ssi is configured with a set of DMA interface signals (SSI_HAS_DMA = 1). When DW_apb_ssi is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.

14.14.4.23 IDR — Offset 48106058h

Identification Register - This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant. Reset Value: SSI_ID

Type	Size	Offset	Default
MMIO	32 bit	48106058h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**IDCODE:** Identification code. The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant.

14.14.4.24 SSI_VERSION_ID — Offset 4810605Ch

coreKit version ID Register - This read-only register stores the specific DW_apb_ssi component version. Reset Value: SSI_VERSION_ID

Type	Size	Offset	Default
MMIO	32 bit	4810605Ch	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**SSI_COMP_VERSION:** Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*.

14.14.4.25 DR0 — Offset 48106060h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	48106060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/V	**DR:** Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. If SSI_MAX_XFER_SIZE configuration parameter is set to 32, all 32 bits are valid. Otherwise, only 16 bits ([15:0]) of the register are valid. Read = Receive FIFO buffer Write = Transmit FIFO buffer.

14.14.4.26 DR1 — Offset 48106064h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.27 DR2 — Offset 48106068h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.28 DR3 — Offset 4810606Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.29 DR4 — Offset 48106070h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.30 DR5 — Offset 48106074h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.31 DR6 — Offset 48106078h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.32 DR7 — Offset 4810607Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.33 DR8 — Offset 48106080h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.34 DR9 — Offset 48106084h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.35 DR10 — Offset 48106088h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.36 DR11 — Offset 4810608Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.37 DR12 — Offset 48106090h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.38 DR13 — Offset 48106094h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.39 DR14 — Offset 48106098h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.40 DR15 — Offset 4810609Ch

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.41 DR16 — Offset 481060A0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.42 DR17 — Offset 481060A4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.43 DR18 — Offset 481060A8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.44 DR19 — Offset 481060ACh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.45 DR20 — Offset 481060B0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.46 DR21 — Offset 481060B4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.47 DR22 — Offset 481060B8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.48 DR23 — Offset 481060BCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.49 DR24 — Offset 481060C0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.50 DR25 — Offset 481060C4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.51 DR26 — Offset 481060C8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.52 DR27 — Offset 481060CCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus

into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.53 DR28 — Offset 481060D0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.54 DR29 — Offset 481060D4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.55 DR30 — Offset 481060D8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.56 DR31 — Offset 481060DCh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.57 DR32 — Offset 481060E0h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.58 DR33 — Offset 481060E4h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.59 DR34 — Offset 481060E8h

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read,

data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.60 DR35 — Offset 481060ECh

Data Register x - The DW_apb_ssi data register is a 16/32-bit (depending on SSI_MAX_XFER_SIZE) read/write buffer for the transmit/receive FIFOs. If the configuration parameter SSI_MAX_XFER_SIZE is set to 32, then all 32 bits are valid, otherwise, only 16 bits ([15:0]) of the register are valid. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0. NOTE: The DR register in the DW_apb_ssi occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the prdata bus. The FIFO buffers on the DW_apb_ssi are not addressable. Reset Value: 0x0

Note: Bit definitions are the same as DR0, offset 48106060h.

14.14.4.61 RX_SAMPLE_DLY — Offset 481060F0h

RX Sample Delay Register - This register is only valid when the DW_apb_ssi is configured with rxd sample delay logic (SSI_HAS_RX_SAMPLE_DELAY==1). When the DW_apb_ssi is not configured with rxd sample delay logic, this register will not exist and writing to its address location will have no effect; reading from its address will return zero. This register control the number of ssi_clk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the DW_apb_ssi is enabled. The DW_apb_ssi is enabled and disabled by writing to the SSIENR register. Reset Value: 0x0

Type	Size	Offset	Default
MMIO	32 bit	481060F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RSD:** Rxd Sample Delay. This register is used to delay the sample of the rxd input port. Each value represents a single ssi_clk delay on the sample of rxd. Note: If this register is programmed with a value that exceeds the depth of the internal shift registers (SSI_RX_DLY_SR_DEPTH) zero delay will be applied to the rxd sample.

14.14.4.62 RSVD — Offset 481060FCh

Reserved

Type	Size	Offset	Default
MMIO	32 bit	481060FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.15 UART Interface Registers

There are six UART Interface registers:-

- UART_0 Registers
- UART_1 Registers
- UART_2 Registers
- UART_3 Registers
- UART_4 Registers
- UART_5 Registers

UART Interface Registers	Address Offset	Table
UART_0	48200000h - 482000FCh	Table 14-28
UART_1	48202000h - 482020FCh	Table 14-29
UART_2	48204000h - 482040FCh	Table 14-30
UART_3	48206000h - 482060FCh	Table 14-31
UART_4	48208000h - 482080FCh	Table 14-32
UART_5	4820A000h - 4820A0FCh	Table 14-33

14.15.1 UART_0 Registers Summary

Table 14-28. Summary of UART_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48200000h	4	RBR	00000000h
48200004h	4	IER	00000000h
48200008h	4	IIR	00000001h
4820000Ch	4	LCR	00000000h
48200010h	4	MCR	00000000h
48200014h	4	LSR	00000060h
48200018h	4	MSR	00000000h
4820001Ch	4	SCR	00000000h
48200070h	4	FAR	00000000h
4820007Ch	4	USR	00000006h
48200080h	4	TFL	00000000h
48200084h	4	RFL	00000000h
482000A4h	4	HTX	00000000h
482000A8h	4	DMASA	00000000h
482000ACh	4	TCR	00000006h
482000B0h	4	DE_EN	00000000h
482000B4h	4	RE_EN	00000000h
482000B8h	4	DET	00000000h
482000BCh	4	TAT	00000000h
482000C0h	4	DLF	00000000h
482000C4h	4	RAR	00000000h
482000C8h	4	TAR	00000000h
482000CCh	4	LCR_EXT	00000000h
482000F4h	4	CPR	00043532h
482000F8h	4	UCV	3430322Ah
482000FCh	4	CTR	44570110h

14.15.1.1 RBR — Offset 48200000h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48200000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. Note: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

14.15.1.2 IER — Offset 48200004h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48200004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

14.15.1.3 IIR — Offset 48200008h

Interrupt Identification Register - Interrupt Identification Register

Type	Size	Offset	Default
MMIO	32 bit	48200008h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h RO/V	**FIFOSE:** FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.
5:4	0h RO	**Reserved**
3:0	1h RO/V	**IID:** Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. **Note:** an interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

14.15.1.4 LCR — Offset 4820000Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Note: NOTE: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

14.15.1.5 MCR — Offset 48200010h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	48200010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable . Writeable only when SIR_MODE == Enabled, always readable. **Note:** To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable . Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**LOOPBACK:** LoopBack Bit . This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2 . This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1 . This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

14.15.1.6 LSR — Offset 48200014h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	48200014h	00000060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

14.15.1.7 MSR — Offset 48200018h

Modem Status Register - Whenever bits 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	48200018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

14.15.1.8 SCR — Offset 4820001Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	4820001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

14.15.1.9 FAR — Offset 48200070h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	48200070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

14.15.1.10 USR — Offset 4820007Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	4820007Ch	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

14.15.1.11 TFL — Offset 48200080h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48200080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

14.15.1.12 RFL — Offset 48200084h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48200084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

14.15.1.13 HTX — Offset 482000A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	482000A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

14.15.1.14 DMASA — Offset 482000A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	482000A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

14.15.1.15 TCR — Offset 482000ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	482000ACh	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

14.15.1.16 DE_EN — Offset 482000B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

14.15.1.17 RE_EN — Offset 482000B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482000B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

14.15.1.18 DET — Offset 482000B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482000B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

14.15.1.19 TAT — Offset 482000BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482000BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. Note: - If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. Note: The actual time is the programmed value + 1.

14.15.1.20 DLF — Offset 482000C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482000C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

14.15.1.21 RAR — Offset 482000C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	482000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

14.15.1.22 TAR — Offset 482000C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	482000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

14.15.1.23 LCR_EXT — Offset 482000CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	482000CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: - 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then subsequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

14.15.1.24 CPR — Offset 482000F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482000F4h	00043532h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

14.15.1.25 UCV — Offset 482000F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482000F8h	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

14.15.1.26 CTR — Offset 482000FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482000FCh	44570110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

14.15.2 UART_1 Registers Summary

Table 14-29. Summary of UART_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48202000h	4	RBR	00000000h
48202004h	4	IER	00000000h
48202008h	4	IIR	00000001h
4820200Ch	4	LCR	00000000h
48202010h	4	MCR	00000000h
48202014h	4	LSR	00000060h
48202018h	4	MSR	00000000h
4820201Ch	4	SCR	00000000h
48202070h	4	FAR	00000000h
4820207Ch	4	USR	00000006h
48202080h	4	TFL	00000000h
48202084h	4	RFL	00000000h
482020A4h	4	HTX	00000000h
482020A8h	4	DMASA	00000000h
482020ACh	4	TCR	00000006h
482020B0h	4	DE_EN	00000000h
482020B4h	4	RE_EN	00000000h
482020B8h	4	DET	00000000h
482020BCh	4	TAT	00000000h
482020C0h	4	DLF	00000000h
482020C4h	4	RAR	00000000h
482020C8h	4	TAR	00000000h
482020CCh	4	LCR_EXT	00000000h
482020F4h	4	CPR	00043532h
482020F8h	4	UCV	3430322Ah
482020FCh	4	CTR	44570110h

14.15.2.1 RBR — Offset 48202000h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48202000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. Note: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

14.15.2.2 IER — Offset 48202004h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48202004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

14.15.2.3 IIR — Offset 48202008h

Interrupt Identification Register - Interrupt Identification Register

Type	Size	Offset	Default
MMIO	32 bit	48202008h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h RO/V	**FIFOSE:** FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.
5:4	0h RO	**Reserved**
3:0	1h RO/V	**IID:** Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. **Note:** an interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

14.15.2.4 LCR — Offset 4820200Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820200Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Note: NOTE: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

14.15.2.5 MCR — Offset 48202010h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	48202010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable . Writeable only when SIR_MODE == Enabled, always readable. **Note:** To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable . Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**LOOPBACK:** LoopBack Bit . This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2 . This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1 . This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

14.15.2.6 LSR — Offset 48202014h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	48202014h	00000060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

14.15.2.7 MSR — Offset 48202018h

Modem Status Register - Whenever bits 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	48202018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

14.15.2.8 SCR — Offset 4820201Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	4820201Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

14.15.2.9 FAR — Offset 48202070h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	48202070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

14.15.2.10 USR — Offset 4820207Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	4820207Ch	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

14.15.2.11 TFL — Offset 48202080h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48202080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

14.15.2.12 RFL — Offset 48202084h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48202084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

14.15.2.13 HTX — Offset 482020A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	482020A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

14.15.2.14 DMASA — Offset 482020A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	482020A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

14.15.2.15 TCR — Offset 482020ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	482020ACh	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

14.15.2.16 DE_EN — Offset 482020B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482020B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

14.15.2.17 RE_EN — Offset 482020B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482020B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

14.15.2.18 DET — Offset 482020B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482020B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

14.15.2.19 TAT — Offset 482020BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482020BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. Note: - If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. Note: The actual time is the programmed value + 1.

14.15.2.20 DLF — Offset 482020C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482020C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

14.15.2.21 RAR — Offset 482020C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	482020C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

14.15.2.22 TAR — Offset 482020C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	482020C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

14.15.2.23 LCR_EXT — Offset 482020CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	482020CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: - 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then sub-sequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

14.15.2.24 CPR — Offset 482020F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482020F4h	00043532h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

14.15.2.25 UCV — Offset 482020F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482020F8h	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

14.15.2.26 CTR — Offset 482020FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482020FCh	44570110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

14.15.3 UART_2 Registers Summary

Table 14-30. Summary of UART_2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48204000h	4	RBR	00000000h
48204004h	4	IER	00000000h
48204008h	4	IIR	00000001h
4820400Ch	4	LCR	00000000h
48204010h	4	MCR	00000000h
48204014h	4	LSR	00000060h
48204018h	4	MSR	00000000h
4820401Ch	4	SCR	00000000h
48204070h	4	FAR	00000000h
4820407Ch	4	USR	00000006h
48204080h	4	TFL	00000000h
48204084h	4	RFL	00000000h
482040A4h	4	HTX	00000000h
482040A8h	4	DMASA	00000000h
482040ACh	4	TCR	00000006h
482040B0h	4	DE_EN	00000000h
482040B4h	4	RE_EN	00000000h
482040B8h	4	DET	00000000h
482040BCh	4	TAT	00000000h
482040C0h	4	DLF	00000000h
482040C4h	4	RAR	00000000h
482040C8h	4	TAR	00000000h
482040CCh	4	LCR_EXT	00000000h
482040F4h	4	CPR	00043532h
482040F8h	4	UCV	3430322Ah
482040FCh	4	CTR	44570110h

14.15.3.1 RBR — Offset 48204000h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48204000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. Note: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

14.15.3.2 IER — Offset 48204004h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48204004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

14.15.3.3 IIR — Offset 48204008h

Interrupt Identification Register - Interrupt Identification Register

Type	Size	Offset	Default
MMIO	32 bit	48204008h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h RO/V	**FIFOSE:** FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.
5:4	0h RO	**Reserved**
3:0	1h RO/V	**IID:** Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. **Note:** an interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

14.15.3.4 LCR — Offset 4820400Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820400Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Note: NOTE: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

14.15.3.5 MCR — Offset 48204010h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	48204010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable . Writeable only when SIR_MODE == Enabled, always readable. **Note:** To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable . Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**LOOPBACK:** LoopBack Bit . This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2 . This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1 . This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

14.15.3.6 LSR — Offset 48204014h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	48204014h	00000060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

14.15.3.7 MSR — Offset 48204018h

Modem Status Register - Whenever bits 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	48204018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

14.15.3.8 SCR — Offset 4820401Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	4820401Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

14.15.3.9 FAR — Offset 48204070h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	48204070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

14.15.3.10 USR — Offset 4820407Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	4820407Ch	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

14.15.3.11 TFL — Offset 48204080h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48204080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

14.15.3.12 RFL — Offset 48204084h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48204084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

14.15.3.13 HTX — Offset 482040A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	482040A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

14.15.3.14 DMASA — Offset 482040A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	482040A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

14.15.3.15 TCR — Offset 482040ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	482040ACh	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

14.15.3.16 DE_EN — Offset 482040B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482040B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

14.15.3.17 RE_EN — Offset 482040B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482040B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

14.15.3.18 DET — Offset 482040B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482040B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

14.15.3.19 TAT — Offset 482040BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482040BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. Note: - If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. Note: The actual time is the programmed value + 1.

14.15.3.20 DLF — Offset 482040C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482040C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

14.15.3.21 RAR — Offset 482040C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	482040C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

14.15.3.22 TAR — Offset 482040C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	482040C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

14.15.3.23 LCR_EXT — Offset 482040CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	482040CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: - 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then sub-sequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

14.15.3.24 CPR — Offset 482040F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482040F4h	00043532h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

14.15.3.25 UCV — Offset 482040F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482040F8h	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

14.15.3.26 CTR — Offset 482040FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482040FCh	44570110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

14.15.4 UART_3 Registers Summary

Table 14-31. Summary of UART_3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48206000h	4	RBR	00000000h
48206004h	4	IER	00000000h
48206008h	4	IIR	00000001h
4820600Ch	4	LCR	00000000h
48206010h	4	MCR	00000000h
48206014h	4	LSR	00000060h
48206018h	4	MSR	00000000h
4820601Ch	4	SCR	00000000h
48206070h	4	FAR	00000000h
4820607Ch	4	USR	00000006h
48206080h	4	TFL	00000000h
48206084h	4	RFL	00000000h
482060A4h	4	HTX	00000000h
482060A8h	4	DMASA	00000000h
482060ACh	4	TCR	00000006h
482060B0h	4	DE_EN	00000000h
482060B4h	4	RE_EN	00000000h
482060B8h	4	DET	00000000h
482060BCh	4	TAT	00000000h
482060C0h	4	DLF	00000000h
482060C4h	4	RAR	00000000h
482060C8h	4	TAR	00000000h
482060CCh	4	LCR_EXT	00000000h
482060F4h	4	CPR	00043532h
482060F8h	4	UCV	3430322Ah
482060FCh	4	CTR	44570110h

14.15.4.1 RBR — Offset 48206000h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48206000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. Note: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

14.15.4.2 IER — Offset 48206004h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48206004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

14.15.4.3 IIR — Offset 48206008h

Interrupt Identification Register - Interrupt Identification Register

Type	Size	Offset	Default
MMIO	32 bit	48206008h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h RO/V	**FIFOSE:** FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.
5:4	0h RO	**Reserved**
3:0	1h RO/V	**IID:** Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. **Note:** An interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

14.15.4.4 LCR — Offset 4820600Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820600Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Note: NOTE: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

14.15.4.5 MCR — Offset 48206010h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	48206010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable . Writeable only when SIR_MODE == Enabled, always readable. **Note:** To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable . Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**LOOPBACK:** LoopBack Bit . This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2 . This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1 . This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

14.15.4.6 LSR — Offset 48206014h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	48206014h	00000060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

14.15.4.7 MSR — Offset 48206018h

Modem Status Register - Whenever bits 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	48206018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

14.15.4.8 SCR — Offset 4820601Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	4820601Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

14.15.4.9 FAR — Offset 48206070h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	48206070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

14.15.4.10 USR — Offset 4820607Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	4820607Ch	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

14.15.4.11 TFL — Offset 48206080h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48206080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

14.15.4.12 RFL — Offset 48206084h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48206084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

14.15.4.13 HTX — Offset 482060A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	482060A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

14.15.4.14 DMASA — Offset 482060A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	482060A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

14.15.4.15 TCR — Offset 482060ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	482060ACh	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

14.15.4.16 DE_EN — Offset 482060B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482060B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

14.15.4.17 RE_EN — Offset 482060B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482060B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

14.15.4.18 DET — Offset 482060B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482060B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

14.15.4.19 TAT — Offset 482060BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482060BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. Note: - If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. Note: The actual time is the programmed value + 1.

14.15.4.20 DLF — Offset 482060C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482060C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

14.15.4.21 RAR — Offset 482060C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	482060C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

14.15.4.22 TAR — Offset 482060C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	482060C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

14.15.4.23 LCR_EXT — Offset 482060CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	482060CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: - 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then sub-sequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

14.15.4.24 CPR — Offset 482060F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482060F4h	00043532h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

14.15.4.25 UCV — Offset 482060F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482060F8h	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

14.15.4.26 CTR — Offset 482060FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482060FCh	44570110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

14.15.5 UART_4 Registers Summary

Table 14-32. Summary of UART_4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48208000h	4	RBR	00000000h
48208004h	4	IER	00000000h
48208008h	4	IIR	00000001h
4820800Ch	4	LCR	00000000h
48208010h	4	MCR	00000000h
48208014h	4	LSR	00000060h
48208018h	4	MSR	00000000h
4820801Ch	4	SCR	00000000h
48208070h	4	FAR	00000000h
4820807Ch	4	USR	00000006h
48208080h	4	TFL	00000000h
48208084h	4	RFL	00000000h
482080A4h	4	HTX	00000000h
482080A8h	4	DMASA	00000000h
482080ACh	4	TCR	00000006h
482080B0h	4	DE_EN	00000000h
482080B4h	4	RE_EN	00000000h
482080B8h	4	DET	00000000h
482080BCh	4	TAT	00000000h
482080C0h	4	DLF	00000000h
482080C4h	4	RAR	00000000h
482080C8h	4	TAR	00000000h
482080CCh	4	LCR_EXT	00000000h
482080F4h	4	CPR	00043532h
482080F8h	4	UCV	3430322Ah
482080FCh	4	CTR	44570110h

14.15.5.1 RBR — Offset 48208000h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48208000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. Note: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

14.15.5.2 IER — Offset 48208004h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	48208004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

14.15.5.3 IIR — Offset 48208008h

Interrupt Identification Register - Interrupt Identification Register

Type	Size	Offset	Default
MMIO	32 bit	48208008h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h RO/V	**FIFOSE:** FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.
5:4	0h RO	**Reserved**
3:0	1h RO/V	**IID:** Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. **Note:** an interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

14.15.5.4 LCR — Offset 4820800Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820800Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Note: NOTE: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

14.15.5.5 MCR — Offset 48208010h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	48208010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable . Writeable only when SIR_MODE == Enabled, always readable. **Note:** To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable . Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**LOOPBACK:** LoopBack Bit . This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2 . This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1 . This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

14.15.5.6 LSR — Offset 48208014h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	48208014h	00000060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

14.15.5.7 MSR — Offset 48208018h

Modem Status Register - Whenever bits 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	48208018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

14.15.5.8 SCR — Offset 4820801Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	4820801Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

14.15.5.9 FAR — Offset 48208070h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	48208070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

14.15.5.10 USR — Offset 4820807Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	4820807Ch	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

14.15.5.11 TFL — Offset 48208080h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48208080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

14.15.5.12 RFL — Offset 48208084h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	48208084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

14.15.5.13 HTX — Offset 482080A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	482080A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

14.15.5.14 DMASA — Offset 482080A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	482080A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

14.15.5.15 TCR — Offset 482080ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	482080ACh	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

14.15.5.16 DE_EN — Offset 482080B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482080B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

14.15.5.17 RE_EN — Offset 482080B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482080B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

14.15.5.18 DET — Offset 482080B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482080B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

14.15.5.19 TAT — Offset 482080BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482080BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. Note: - If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. Note: The actual time is the programmed value + 1.

14.15.5.20 DLF — Offset 482080C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	482080C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

14.15.5.21 RAR — Offset 482080C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	482080C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

14.15.5.22 TAR — Offset 482080C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	482080C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

14.15.5.23 LCR_EXT — Offset 482080CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	482080CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: - 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then subsequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

14.15.5.24 CPR — Offset 482080F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482080F4h	00043532h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

14.15.5.25 UCV — Offset 482080F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482080F8h	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

14.15.5.26 CTR — Offset 482080FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	482080FCh	44570110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

14.15.6 UART_5 Registers Summary

Table 14-33. Summary of UART_5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4820A000h	4	RBR	00000000h
4820A004h	4	IER	00000000h
4820A008h	4	IIR	00000001h
4820A00Ch	4	LCR	00000000h
4820A010h	4	MCR	00000000h
4820A014h	4	LSR	00000060h
4820A018h	4	MSR	00000000h
4820A01Ch	4	SCR	00000000h
4820A070h	4	FAR	00000000h
4820A07Ch	4	USR	00000006h
4820A080h	4	TFL	00000000h
4820A084h	4	RFL	00000000h
4820A0A4h	4	HTX	00000000h
4820A0A8h	4	DMASA	00000000h
4820A0ACh	4	TCR	00000006h
4820A0B0h	4	DE_EN	00000000h
4820A0B4h	4	RE_EN	00000000h
4820A0B8h	4	DET	00000000h
4820A0BCh	4	TAT	00000000h
4820A0C0h	4	DLF	00000000h
4820A0C4h	4	RAR	00000000h
4820A0C8h	4	TAR	00000000h
4820A0CCh	4	LCR_EXT	00000000h
4820A0F4h	4	CPR	00043532h
4820A0F8h	4	UCV	3430322Ah
4820A0FCh	4	CTR	44570110h

14.15.6.1 RBR — Offset 4820A000h

Receive Buffer Register - Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	4820A000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8:0	000h RO/V	**RBR:** Receive Buffer Register. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs. Note: When UART_9BIT_DATA_EN=0, this field width is 8. When UART_9BIT_DATA_EN=1, this field width is 9.

14.15.6.2 IER — Offset 4820A004h

Interrupt Enable Register - Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.

Type	Size	Offset	Default
MMIO	32 bit	4820A004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**PTIME:** Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.
6:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**ELCOLR:** Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable.
3	0h RW	**EDSSI:** Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.
2	0h RW	**ELSI:** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.
1	0h RW	**ETBEI:** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.
0	0h RW	**ERBFI:** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.

14.15.6.3 IIR — Offset 4820A008h

Interrupt Identification Register - Interrupt Identification Register

Type	Size	Offset	Default
MMIO	32 bit	4820A008h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:6	0h RO/V	**FIFOSE:** FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.
5:4	0h RO	**Reserved**
3:0	1h RO/V	**IID:** Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. **Note:** an interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

14.15.6.4 LCR — Offset 4820A00Ch

Line Control Register - Line Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820A00Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**BC:** Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RW	**SP:** Stick Parity. If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	0h RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PEN:** Parity Enable . If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.
2	0h RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Note: NOTE: The STOP bit duration implemented by DW_apb_uart may appear longer due to idle time inserted between characters for some configurations and baud clock divisor values in the transmit direction.
1:0	0h RW	**DLS:** Data Length Select (or CLS as used in legacy). If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.

14.15.6.5 MCR — Offset 4820A010h

Modem Control Register - Modem Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820A010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6	0h RO/V	**SIRE:** SIR Mode Enable . Writeable only when SIR_MODE == Enabled, always readable. **Note:** To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.
5	0h RW	**AFCE:** Auto Flow Control Enable . Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**LOOPBACK:** LoopBack Bit . This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0h RW	**OUT2:** OUT2 . This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0h RW	**OUT1:** OUT1 . This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0h RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

14.15.6.6 LSR — Offset 4820A014h

Line Status Register - Line Status Register

Type	Size	Offset	Default
MMIO	32 bit	4820A014h	00000060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**ADDR_RCVD:** Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. - 1 = Indicates the character is address. - 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt.
7	0h RO/V	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1h RO/V	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RO/V	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0h RO/V	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).
2	0h RO/V	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).
1	0h RO/V	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).
0	0h RO/V	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.

14.15.6.7 MSR — Offset 4820A018h

Modem Status Register - Whenever bits 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.

Type	Size	Offset	Default
MMIO	32 bit	4820A018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	0h RO/V	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	0h RO/V	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	0h RO/V	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).
3	0h RO/V	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	0h RO/V	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.
0	0h RO/V	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.

14.15.6.8 SCR — Offset 4820A01Ch

Scratchpad Register - Scratchpad Register

Type	Size	Offset	Default
MMIO	32 bit	4820A01Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**SCR:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

14.15.6.9 FAR — Offset 4820A070h

FIFO Access Register - FIFO Access Register

Type	Size	Offset	Default
MMIO	32 bit	4820A070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**FAR:** Writes will have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.

14.15.6.10 USR — Offset 4820A07Ch

UART Status register - UART Status register.

Type	Size	Offset	Default
MMIO	32 bit	4820A07Ch	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO/V	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full.
3	0h RO/V	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.
1	1h RO/V	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

14.15.6.11 TFL — Offset 4820A080h

Transmit FIFO Level - TFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	4820A080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**TFL:** Transmit FIFO Level. This indicates the number of data entries in the transmit FIFO.

14.15.6.12 RFL — Offset 4820A084h

Receive FIFO Level - RFL register is valid only when the DW_apb_uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES). If status registers are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	4820A084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	00h RO/V	**RFL:** Receive FIFO Level. This indicates the number of data entries in the receive FIFO.

14.15.6.13 HTX — Offset 4820A0A4h

Halt TX - Halt TX

Type	Size	Offset	Default
MMIO	32 bit	4820A0A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HTX:** Halt TX. Writes will have no effect when FIFO_MODE == NONE, always readable. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.

14.15.6.14 DMASA — Offset 4820A0A8h

DMA Software Acknowledge Register - DMA Software Acknowledge Register

Type	Size	Offset	Default
MMIO	32 bit	4820A0A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h WO	**DMASA:** DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.

14.15.6.15 TCR — Offset 4820A0ACh

Transceiver Control Register - This register is used to enable or disable RS485 mode and also control the polarity values for Driven enable (de) and Receiver Enable (re) signals. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address returns zero.

Type	Size	Offset	Default
MMIO	32 bit	4820A0ACh	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:3	0h RW	**XFER_MODE:** Transfer Mode. - 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. - 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission Hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. - 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and DW_apb_uart controller will be ready to receive. If the user programs the TX FIFO with the data then DW_apb_uart, after ensuring no receive is in progress, disable 're' and enable 'de' signal. Once the TX FIFO becomes empty, 're' signal gets enabled and 'de' signal will be disabled. In this mode of operation hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other.
2	1h RW	**DE_POL:** Driver Enable Polarity. - 1: DE signal is active high - 0: DE signal is active low
1	1h RW	**RE_POL:** Receiver Enable Polarity. - 1: RE signal is active high - 0: RE signal is active low
0	0h RW	**RS485_EN:** RS485 Transfer Enable. - 0 : In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and register DE_EN/RE_EN/TAT are also reserved. - 1 : In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable.

14.15.6.16 DE_EN — Offset 4820A0B0h

Driver Output Enable Register - The Driver Output Enable Register (DE_EN) is used to control the assertion and de-assertion of the DE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	4820A0B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DE_ENABLE:** DE Enable control. The 'DE Enable' register bit is used to control assertion and de-assertion of 'de' signal. - 0: De-assert 'de' signal - 1: Assert 'de' signal

14.15.6.17 RE_EN — Offset 4820A0B4h

Receiver Output Enable Register - The Receiver Output Enable Register (RE_EN) is used to control the assertion and de-assertion of the RE signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If the RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	4820A0B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**RE_ENABLE:** RE Enable control. The 'RE Enable' register bit is used to control assertion and de-assertion of 're' signal. - 0: De-assert 're' signal - 1: Assert 're' signal

14.15.6.18 DET — Offset 4820A0B8h

Driver Output Enable Timing Register - The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of 'de' signal. This register is only valid when the DW_apb_uart is configured to have RS485 interface implemented (UART_RS485_INTERFACE = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	4820A0B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**DE_DE_ASSERTION_TIME:** Driver Enable de-assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal.
15:8	0h RO	**Reserved**
7:0	00h RW	**DE_ASSERTION_TIME:** Driver Enable assertion time. This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable.

14.15.6.19 TAT — Offset 4820A0BCh

TurnAround Timing Register - The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of 're' and 'de' signals. This register is only valid when the DW_apb_uart is configured to have the RS485 interface implemented (UART_RS485_INTERFACE_EN = ENABLED). If RS485 interface is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	4820A0BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RE_TO_DE:** Receiver Enable to Driver Enable TurnAround time. Turnaround time (in terms of serial clock) for RE De-assertion to DE assertion. Note: - If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. - If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. - If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.
15:0	0000h RW	**DE_TO_RE:** Driver Enable to Receiver Enable TurnAround time. Turnaround time (in terms of serial clock) for DE De-assertion to RE assertion. Note: The actual time is the programmed value + 1.

14.15.6.20 DLF — Offset 4820A0C0h

Divisor Latch Fraction Register - This register is only valid when the DW_apb_uart is configured to have Fractional Baud rate Divisor implemented (FRACTIONAL_BAUD_DIVISOR_EN = ENABLED). If Fractional Baud rate divisor is not implemented, this register does not exist and reading from this register address will return zero.

Type	Size	Offset	Default
MMIO	32 bit	4820A0C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**DLF:** Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE).

14.15.6.21 RAR — Offset 4820A0C4h

Receive Address Register - Receive Address Register

Type	Size	Offset	Default
MMIO	32 bit	4820A0C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RAR:** This is an address matching register during receive mode. If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then sub-sequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received. Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.

14.15.6.22 TAR — Offset 4820A0C8h

Transmit Address Register - Transmit Address Register

Type	Size	Offset	Default
MMIO	32 bit	4820A0C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TAR:** This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then DW_apb_uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the DW_apb_uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.

14.15.6.23 LCR_EXT — Offset 4820A0CCh

Line Extended Control Register - Line Extended Control Register

Type	Size	Offset	Default
MMIO	32 bit	4820A0CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/V	**TRANSMIT_MODE:** Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers. - 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data : 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. - 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the DW_apb_uart on when to send the address.
2	0h RW/V	**SEND_ADDR:** Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. - 1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. - 0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register. Note: - 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. - 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0.
1	0h RW/V	**ADDR_MATCH:** Address Match Mode.This bit is used to enable the address match feature during receive. - 1 = Address match mode; DW_apb_uart will wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then subsequent characters will be treated as valid data and DW_apb_uart starts receiving data. - 0 = Normal mode; DW_apb_uart will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1.
0	0h RW/V	**DLS_E:** Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers.

14.15.6.24 CPR — Offset 4820A0F4h

Component Parameter Register - Component Parameter Register.This register is valid only when UART_ADD_ENCODED_PARAMS = 1. If the UART_ADD_ENCODED_PARAMS parameter is not set, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	4820A0F4h	00043532h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	04h RO/V	**FIFO_MODE:** Encoding of FIFO_MODE configuration parameter value.
15:14	0h RO	**Reserved**
13	1h RO/V	**DMA_EXTRA:** Encoding of DMA_EXTRA configuration parameter value.
12	1h RO/V	**UART_ADD_ENCODED_PARAMS:** Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value.
11	0h RO/V	**SHADOW:** Encoding of SHADOW configuration parameter value.
10	1h RO/V	**FIFO_STAT:** Encoding of FIFO_STAT configuration parameter value.
9	0h RO/V	**FIFO_ACCESS:** Encoding of FIFO_ACCESS configuration parameter value.
8	1h RO/V	**ADDITIONAL_FEAT:** Encoding of ADDITIONAL_FEATURES configuration parameter value.
7	0h RO/V	**SIR_LP_MODE:** Encoding of SIR_LP_MODE configuration parameter value.
6	0h RO/V	**SIR_MODE:** Encoding of SIR_MODE configuration parameter value.
5	1h RO/V	**THRE_MODE:** Encoding of THRE_MODE configuration parameter value.
4	1h RO/V	**AFCE_MODE:** Encoding of AFCE_MODE configuration parameter value.
3:2	0h RO	**Reserved**
1:0	2h RO/V	**APB_DATA_WIDTH:** Encoding of APB_DATA_WIDTH configuration parameter value.

14.15.6.25 UCV — Offset 4820A0F8h

UART Component Version - UCV register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	4820A0F8h	3430322Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3430322Ah RO/V	**UART_COMPONENT_VERSION:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*

14.15.6.26 CTR — Offset 4820A0FCh

Component Type Register - CTR is register is valid only when the DW_apb_uart is configured to have additional features implemented (ADDITIONAL_FEATURES = YES). If additional features are not implemented, this register does not exist and reading from this register address returns 0.

Type	Size	Offset	Default
MMIO	32 bit	4820A0FCh	44570110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO/V	**PERIPHERAL_ID:** This register contains the peripherals identification code.

14.16 I2S Interface Registers

There are two I2S Interface registers:-

- I2S_0 Registers
- I2S_1 Registers

I2S Interface Registers	Address Offset	Table
I2S_0	48300000h - 48300040h	Table 14-34
I2S_1	48302000h - 48302040h	Table 14-35

14.16.1 I2S_0 Registers Summary

Table 14-34. Summary of I2S_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48300000h	4	I2S-SC Control (I2S_CTRL)	000001B8h
48300004h	4	I2S Full Duplex Mode Receiver Control (I2S_CTRL_FDR)	00000010h
48300008h	4	Transceiver Sample Resolution (I2S_SRES)	00000000h
4830000Ch	4	Full Duplex Mode Receive Samples Resolution (I2S_SRES_FDR)	00000000h
48300010h	4	Transceiver Sample Rate (I2S_SRATE)	00000000h
48300014h	4	I2S-SC Status Flags (I2S_STAT)	0003000Ch
48300018h	4	FIFO Using Level(Read Only) (FIFO_LEVEL)	00000000h
4830001Ch	4	FIFO Almost Empty Level (FIFO_AEMPTY)	00000000h
48300020h	4	FIFO Almost Full Level (FIFO_AFULL)	0000001Fh
48300024h	4	Full Duplex Mode Receiver FIFO Using Level(Read Only) (FIFO_LEVEL_FDR)	00000000h
48300028h	4	Full Duplex Mode Receiver FIFO Almost Empty Level (FIFO_AEMPTY_FDR)	00000000h
4830002Ch	4	Full Duplex Mode Receiver FIFO Almost Full Level (FIFO_AFULL_FDR)	0000001Fh
48300030h	4	Time Division Multiplexing Control (TDM_CTRL)	FFFF0000h
48300034h	4	Time Division Multiplexing Full Duplex Mode Channels Direction (TDM_FD_DIR)	0000FFFFh
48300040h	4	TX/RX FIFo (FIFO)	00000000h

14.16.1.1 I2S-SC Control (I2S_CTRL) — Offset 48300000h

I2S-SC Control Register After end of reset bit sfr_rst triggers to 1 and bit fifo_rst triggers to 1. Therefore register value after end of reset is 000001B8.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300000h	000001B8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Full-Duplex Mode Receiver Samples Resolution (FULL_DUPLEX):** Full-duplex mode enable bit. If HIGH transmitter and receiver data units work simultaneously, otherwise only transmitter or receiver is enable in dependent to dir_cfg bit (I2S_CTRL[1]).
30	0h RW	**FIFO Almost Full Mask Register (FIFO_AFULL_MASK):** Bit masking interrupt request generation after FIFO becomes almost full. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
29	0h RW	**FIFO Full Mask Register (FIFO_FULL_MASK):** Bit masking interrupt request generation after FIFO becomes full. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
28	0h RW	**FIFO Almost Empty Mask Register (FIFO_AEMPTY_MASK):** Bit masking interrupt request generation after FIFO becomes almost empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition. Sampled on the rising edge of the clock.
27	0h RW	**FIFO Empty Mask Register (FIFO_EMPTY_MASK):** Bit masking interrupt request generation after FIFO becomes empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition. Sampled on the rising edge of the clock.
26	0h RW	**I2s Mask Register (I2S_MASK):** Bit masking interrupt request generation after underrun/overrun condition occurrence in I2S-SC transceiver. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for underrun event interrupt. Sampled on the rising edge of the clock.
25	0h RW	**Interupt Mask Register (INTREQ_MASK):** Bit masking all interrupt requests. When LOW all interrupts are masked, when HIGH interrupts use individual masks. Sampled on the rising edge of the clock.
24	0h RW	**Transceiver Clock Enable. (I2S_STB):** Transceiver clock enable. When LOW the clk_i2s clock is enabled, else clock is disabled. Sampled on the rising edge of the clock.
23	0h RW	**Audio Data Sample Alignment At Host Data Bus. (HOST_DATA_ALIGN):** Audio data sample alignment at host data bus. When LOW the audio sample data is aligned to the LSB at the host data bus. When HIGH the audio sample data is aligned to the MSB at host data bus.Sampled on the rising edge of the clock.
22	0h RW	**Audio Data Sample Arrangement In Audio Data Slot (DATA_ORDER):** Bit masking interrupt request generation after FIFO becomes almost empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
21	0h RW	**Audio Sample Alignment In Audio Data Time Slot (DATA_ALIGN):** Bit masking interrupt request generation after FIFO becomes empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.

Bit Range	Default & Access	Field Name (ID): Description
20:16	00h RW	**Audio Data Delay After WS Signal (DATA_WS_DEL):** Bit masking interrupt request generation after underrun/overrun condition occurrence in I2S-SC transceiver. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for underrun event interrupt.
15	0h RW	**The Word Select Signal Polarity Selection. (WS_POLAR):** Bit masking all interrupt requests. When LOW all interrupts are masked, when HIGH interrupts use individual masks.
14	0h RW	**The Continuous Serial Clock Active Edge. (SCK_POLAR):** Transceiver clock enable. When LOW the clk_i2s clock is enabled, else clock is disabled.
13	0h RW	**Mono/Stereo Audio Mode Selection (AUDIO_MODE):** Audio data sample alignment at host data bus. When LOW the audio sample data is aligned to the LSB at the host data bus. When HIGH the audio sample data is aligned to the MSB at host data bus.
12	0h RW	**Active Audio Channel In Mono Mode (MONO_MODE):** Active audio channel in mono mode. When LOW left audio channel is active. When HIGH right audio channel is active.
11:8	1h RW	**Word Select Signal (WS) Format. (WS_MODE):** Word select signal (WS) format. TDM mode is not active: Only bit 8 is relevant. If it is set to LOW (even value of ws_mode) WS signal have DSP audio interface specification format. If it is set to HIGH (odd value of ws_mode) WS signal have standard I2S audio interface specification format. TDM mode is active: When field equals 0 WS signal has DSP audio interface specification format, otherwise (ws_mode field equals the value from range 1 &CHN_NO-1) WS.
7:5	5h RW	**Audio Channel Time Slot Width (CHN_WIDTH):** Audio channel time slot width in I2S master or DSP/TDM master and slave modes. 0 8 SCK cycles per audio channel 1 12 SCK cycles per audio channel 2 16 SCK cycles per audio channel 3 18 SCK cycles per audio channel 4 20 SCK cycles per audio channel 5 24 SCK cycles per audio channel 6 28 SCK cycles per audio channel 7 32 SCK cycles per audio channel.
4	1h RW	**FIFO Reset (FIFO_RST):** FIFO reset. When LOW, FIFO pointer is reset to zero. Threshold levels for FIFO are unchanged. This bit is automatically set to HIGH after one clock cycle. In full-duplex mode this bit resets only transmitter FIFO.
3	1h RW	**SFR Block Synchronous Reset (SFR_RST):** SFR block synchronous reset. When LOW, all bits in SFR registers are reset to default values. This bit is automatically set to HIGH after one clock cycle.
2	0h RW	**Configuration Bit For Transceiver Synchronizing Unit (MS_CFG):** Configuration bit for transceiver synchronizing unit: 1 Master 0 Slave.
1	0h RW	**Direction Of Transmission (DIR_CFG):** 1 Transmitter 0 Receiver.
0	0h RW	**Enable Bit For I2S Transceiver (I2S_EN):** 1 enables transceiver 0 disables transceiver, causes synchronous reset signal, configuration SFR bits are unchanged .

14.16.1.2 I2S Full Duplex Mode Receiver Control (I2S_CTRL_FDR) — Offset 48300004h

I2S Full Duplex Mode Receiver Control Register After end of reset bit FIFO_rst triggers to 1. Therefore register value after end of reset is 00000010.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300004h	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**Full Duplex Almost FIFO Full Mask Register (RFIFO_AFULL_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes almost full. When LOW, masks generation of interrupt request.
29	0h RW	**Full Duplex FIFO Full Mask Register (RFIFO_FULL_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes full. When LOW, masks generation of interrupt request.
28	0h RW	**Full Duplex Almost FIFO Empty Mask Register (RFIFO_AEMPTY_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes almost empty. When LOW, masks generation of interrupt request.
27	0h RW	**Full Duplex FIFO Empty Mask Register (RFIFO_EMPTY_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes empty. When LOW, masks generation of interrupt request.
26	0h RW	**Full Duplex I2s_mask Register (RI2S_MASK):** Bit masking interrupt request generation after overrun condition occurrence in I2S-SC full-duplex mode receiver. When LOW, masks generation of interrupt request.
25:5	0h RO	**Reserved**
4	1h RW	**Full-Duplex Mode Receiver FIFO Reset. (FIFO_RST):** Full-duplex mode receiver FIFO reset. Active only in full-duplex mode. When '0', RFIFO pointer is reset to zero. Threshold levels for RFIFO are unchanged. The bit is automatically set to '1' after one clock cycle.
3:0	0h RO	**Reserved**

14.16.1.3 Transceiver Sample Resolution (I2S_SRES) — Offset 48300008h

Transceiver Sample Resolution.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Samples Resolution. (RESOLUTION):** Samples resolution. When full-duplex mode is active, this value specifies resolution only for transmitted samples. Sampled on the rising edge of the clock. It simply should be assigned the value equal to the number of valid bits minus one, for example: 00000B sample resolution = 1 bit 11111B sample resolution = 32 bits.

14.16.1.4 Full Duplex Mode Receive Samples Resolution (I2S_SRES_FDR) — Offset 4830000Ch

Full Duplex Mode Receive Samples Resolution.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4830000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**I2s_sres Register - Samples Resolution (RESOLUTION):** Full-duplex mode receive samples resolution. When half-duplex mode is active this value is ignored. It simply should be assigned the value equal to the number of valid bits minus one, for example: 00000B sample resolution = 1 bit 11111B sample resolution = 32 bits.

14.16.1.5 Transceiver Sample Rate (I2S_SRATE) — Offset 48300010h

Transceiver Sample Rate.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:0	00000h RW	**SAMPLE_RATE:** In general value of sample rate is the quotient of clk frequency and I2S rate [bit/s]. The value of sample rate is the higher the clk frequency is greater than I2S rate.

14.16.1.6 I2S-SC Status Flags (I2S_STAT) — Offset 48300014h

I2S-SC Status Flags Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300014h	0003000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Receive FIFO Almost Full Flag In Full-Duplex Mode (RFIFO_AFULL):** Receive FIFO almost full flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO becomes almost full (rising edge of almost full condition).
18	0h RW	**Receive FIFO Full Flag In Full-Duplex Mode (RFIFO_FULL):** Receive FIFO full flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO is full.
17	1h RW	**Receive FIFO Almost Empty Flag In Full-Duplex Mode (RFIFO_AEMPTY):** Receive FIFO almost empty flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO becomes almost empty (rising edge of almost empty condition).
16	1h RW	**Receive FIFO Empty Flag In Full-Duplex Mode (RFIFO_EMPTY):** Receive FIFO empty flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO is empty.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**FIFO Almost Full Flag (FIFO_AFULL):** FIFO almost full flag. Active HIGH. This flag is set to HIGH when FIFO becomes almost full (rising edge of almost full condition). When full-duplex mode is active, this bit is a flag only for transmitter FIFO almost full condition.
4	0h RW	**FIFO Full Flag (FIFO_FULL):** FIFO full flag. Active HIGH. This flag is set to HIGH when FIFO is full. When full-duplex mode is active, this bit is a flag only for transmitter FIFO full condition.
3	1h RW	**FIFO Almost Empty Flag (FIFO_AEMPTY):** FIFO almost empty flag. Active HIGH. This flag is set to HIGH when FIFO becomes almost empty (rising edge of almost empty condition). When full-duplex mode is active, this bit is a flag only for transmitter FIFO almost empty condition.
2	1h RW	**FIFO Empty Flag (FIFO_EMPTY):** FIFO empty flag. Active HIGH. This flag is set to HIGH when FIFO is empty. When full-duplex mode is active, this bit is a flag only for transmitter FIFO empty condition.
1	0h RW	**RDATA_OVRERR:** Indicates data overrun error for transceiver in receiver mode, active HIGH. Sampled and updated on the rising edge of the clock. Writing LOW value to this bit resets the transceiver and the FIFO. The transceiver configuration is preserved.
0	0h RW	**Full Duplex Mode Samples Resolution Register (TDATA_UNDERR):** Indicates data underrun event, active HIGH. This flag is set to HIGH when TX underrun arises (rising edge of underrun condition).

14.16.1.7 FIFO Using Level(Read Only) (FIFO_LEVEL) — Offset 48300018h

FIFO Using Level Register (read only).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RO	**FIFO Level Register (FIFO_LEVEL):** Indicates FIFO level. Updated on the rising edge of the clock. When full-duplex mode is active, this register holds value of the transmitter FIFO level. When half-duplex mode is active, this register holds value of the transmitter or receiver FIFO level in dependent to the transmit/receive direction mode.

14.16.1.8 FIFO Almost Empty Level (FIFO_AEMPTY) — Offset 4830001Ch

FIFO Almost Empty Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4830001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**FIFO Almost Empty Threshold Level (AEMPTY_THRESHOLD):** Determines threshold for almost empty flag in the FIFO. When full-duplex mode is active, this register specifies an almost empty level of the transmitter FIFO level.

14.16.1.9 FIFO Almost Full Level (FIFO_AFULL) — Offset 48300020h

FIFO Almost Full Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300020h	0000001Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	1Fh RW	**FIFO Aempty Threshold Level (AFULL_THRESHOLD):** Determines threshold for almost full flag in the FIFO. When full-duplex mode is active, this register specifies an almost full level of the transmitter FIFO level.

14.16.1.10 Full Duplex Mode Receiver FIFO Using Level(Read Only) (FIFO_LEVEL_FDR) — Offset 48300024h

Full Duplex Mode Receiver FIFO Using Level Register (read only).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RO	**Full Duplex FIFO Level (RX_FIFO_LEVEL):** Full-duplex mode receive FIFO level.

14.16.1.11 Full Duplex Mode Receiver FIFO Almost Empty Level (FIFO_AEMPTY_FDR) — Offset 48300028h

Full Duplex Mode Receiver FIFO Almost Empty Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Full Duples FIFO Almost Empty Level (AEMPTY_THRESHOLD):** Determines almost empty level in the receive FIFO in full-duplex mode.

14.16.1.12 Full Duplex Mode Receiver FIFO Almost Full Level (FIFO_AFULL_FDR) — Offset 4830002Ch

Full Duplex Mode Receiver FIFO Almost Full Level.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4830002Ch	0000001Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	1Fh RW	**Full Duplex FIFO Almost Full Level (AFULL_THRESHOLD):** Determines almost full level in the receive FIFO in full-duplex mode.

14.16.1.13 Time Division Multiplexing Control (TDM_CTRL) — Offset 48300030h

Time Division Multiplexing Control Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300030h	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**TDM Channel Enable 15 (CH15_EN):** TDM interface channel 15 activating bit. When HIGH 15th time slot sample is transmitted and/or received depending on transceiver mode.
30	1h RW	**TDM Channel Enable 14 (CH14_EN):** TDM interface channel 14 activating bit. When HIGH 14th time slot sample is transmitted and/or received depending on transceiver mode.
29	1h RW	**TDM Channel Enable 13 (CH13_EN):** TDM interface channel 13 activating bit. When HIGH 13th time slot sample is transmitted and/or received depending on transceiver mode.
28	1h RW	**TDM Channel Enable 12 (CH12_EN):** TDM interface channel 12 activating bit. When HIGH 12th time slot sample is transmitted and/or received depending on transceiver mode.
27	1h RW	**TDM Channel Enable 11 (CH11_EN):** TDM interface channel 11 activating bit. When HIGH 11th time slot sample is transmitted and/or received depending on transceiver mode.
26	1h RW	**TDM Channel Enable 10 (CH10_EN):** TDM interface channel 10 activating bit. When HIGH 10th time slot sample is transmitted and/or received depending on transceiver mode.

Bit Range	Default & Access	Field Name (ID): Description
25	1h RW	**TDM Channel Enable 9 (CH9_EN):** TDM interface channel 9 activating bit. When HIGH 9th time slot sample is transmitted and/or received depending on transceiver mode.
24	1h RW	**TDM Channel Enable 8 (CH8_EN):** TDM interface channel 8 activating bit. When HIGH 8th time slot sample is transmitted and/or received depending on transceiver mode.
23	1h RW	**TDM Channel Enable 7 (CH7_EN):** TDM interface channel 7 activating bit. When HIGH 7th time slot sample is transmitted and/or received depending on transceiver mode.
22	1h RW	**TDM Channel Enable 6 (CH6_EN):** TDM interface channel 6 activating bit. When HIGH 6th time slot sample is transmitted and/or received depending on transceiver mode.
21	1h RW	**TDM Channel Enable 5 (CH5_EN):** TDM interface channel 5 activating bit. When HIGH 5th time slot sample is transmitted and/or received depending on transceiver mode.
20	1h RW	**TDM Channel Enable 4 (CH4_EN):** TDM interface channel 4 activating bit. When HIGH 4th time slot sample is transmitted and/or received depending on transceiver mode.
19	1h RW	**TDM Channel Enable 3 (CH3_EN):** TDM interface channel 3 activating bit. When HIGH 3rd time slot sample is transmitted and/or received depending on transceiver mode.
18	1h RW	**TDM Channel Enable 2 (CH2_EN):** TDM interface channel 2 activating bit. When HIGH 2nd time slot sample is transmitted and/or received depending on transceiver mode.
17	1h RW	**TDM Channel Enable 1 (CH1_EN):** TDM interface channel 1 activating bit. When HIGH 1st time slot sample is transmitted and/or received depending on transceiver mode.
16	1h RW	**TDM Channel Enable 0 (CH0_EN):** TDM interface channel 0 activating bit. When HIGH zero time slot sample is transmitted and/or received depending on transceiver mode.
15:5	0h RO	**Reserved**
4:1	0h RW	**Tdm Register For Number Of Channels Per Frame (CHN_NO):** Number of supported audio channels in TDM compatible interface mode. Written value equals channels number minus 1.
0	0h RW	**Time Division Multiplexing Audio Interface Enable (TDM_EN):** Time Division Multiplexing audio interface enable. When HIGH audio interface works in TDM compatible mode determined by this register value. When LOW audio interface works in standard stereo I2S mode.

14.16.1.14 Time Division Multiplexing Full Duplex Mode Channels Direction (TDM_FD_DIR) — Offset 48300034h

Time Division Multiplexing Full Duplex Mode Channels Direction Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300034h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Full Duplex Rx Channel Enable 15 (CH15_RXEN):** TDM interface channel 15 receive enable bit. Active only in full-duplex mode. When HIGH and ch15_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 15 time slot.
30	0h RW	**Full Duplex Rx Channel Enable 14 (CH14_RXEN):** TDM interface channel 14 receive enable bit. Active only in full-duplex mode. When HIGH and ch14_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 14 time slot.
29	0h RW	**Full Duplex Rx Channel Enable 13 (CH13_RXEN):** TDM interface channel 13 receive enable bit. Active only in full-duplex mode. When HIGH and ch13_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 13 time slot.
28	0h RW	**Full Duplex Rx Channel Enable 12 (CH12_RXEN):** TDM interface channel 12 receive enable bit. Active only in full-duplex mode. When HIGH and ch12_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 12 time slot.
27	0h RW	**Full Duplex Rx Channel Enable 11 (CH11_RXEN):** TDM interface channel 11 receive enable bit. Active only in full-duplex mode. When HIGH and ch11_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 11 time slot.
26	0h RW	**Full Duplex Rx Channel Enable 10 (CH10_RXEN):** TDM interface channel 10 receive enable bit. Active only in full-duplex mode. When HIGH and ch10_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 10 time slot.
25	0h RW	**Full Duplex Rx Channel Enable 9 (CH9_RXEN):** TDM interface channel 9 receive enable bit. Active only in full-duplex mode. When HIGH and ch9_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 9 time slot.
24	0h RW	**Full Duplex Rx Channel Enable 8 (CH8_RXEN):** TDM interface channel 8 receive enable bit. Active only in full-duplex mode. When HIGH and ch8_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 8 time slot.
23	0h RW	**Full Duplex Rx Channel Enable 7 (CH7_RXEN):** TDM interface channel 7 receive enable bit. Active only in full-duplex mode. When HIGH and ch7_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 7 time slot.
22	0h RW	**Full Duplex Rx Channel Enable 6 (CH6_RXEN):** TDM interface channel 6 receive enable bit. Active only in full-duplex mode. When HIGH and ch6_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 6 time slot.
21	0h RW	**Full Duplex Rx Channel Enable 5 (CH5_RXEN):** TDM interface channel 5 receive enable bit. Active only in full-duplex mode. When HIGH and ch5_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 5 time slot.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Full Duplex Rx Channel Enable 4 (CH4_RXEN):** TDM interface channel 4 receive enable bit. Active only in full-duplex mode. When HIGH and ch4_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 4 time slot.
19	0h RW	**Full Duplex Rx Channel Enable 3 (CH3_RXEN):** TDM interface channel 3 receive enable bit. Active only in full-duplex mode. When HIGH and ch3_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 3 time slot.
18	0h RW	**Full Duplex Rx Channel Enable 2 (CH2_RXEN):** TDM interface channel 2 receive enable bit. Active only in full-duplex mode. When HIGH and ch2_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 2 time slot.
17	0h RW	**Full Duplex Rx Channel Enable 1 (CH1_RXEN):** TDM interface channel 1 receive enable bit. Active only in full-duplex mode. When HIGH and ch1_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 1 time slot.
16	0h RW	**Full Duplex Tx Channel Enable 0 (CH0_TXEN):** TDM interface channel 0 receive enable bit. Active only in full-duplex mode. When HIGH and ch0_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 0 time slot.
15	1h RW	**Full Duplex Tx Channel Enable 15 (CH15_TXEN):** TDM interface channel 15 transmit enable bit. Active only in full-duplex mode. When HIGH and ch15_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 15 time slot through sdo line.
14	1h RW	**Full Duplex Tx Channel Enable 14 (CH14_TXEN):** TDM interface channel 14 transmit enable bit. Active only in full-duplex mode. When HIGH and ch14_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 14 time slot through sdo line.
13	1h RW	**Full Duplex Tx Channel Enable 13 (CH13_TXEN):** TDM interface channel 13 transmit enable bit. Active only in full-duplex mode. When HIGH and ch13_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 13 time slot through sdo line.
12	1h RW	**Full Duplex Tx Channel Enable 12 (CH12_TXEN):** TDM interface channel 12 transmit enable bit. Active only in full-duplex mode. When HIGH and ch12_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 12 time slot through sdo line.
11	1h RW	**Full Duplex Tx Channel Enable 11 (CH11_TXEN):** TDM interface channel 11 transmit enable bit. Active only in full-duplex mode. When HIGH and ch11_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 11 time slot through sdo line.
10	1h RW	**Full Duplex Tx Channel Enable 10 (CH10_TXEN):** TDM interface channel 10 transmit enable bit. Active only in full-duplex mode. When HIGH and ch10_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 10 time slot through sdo line.
9	1h RW	**Full Duplex Tx Channel Enable 9 (CH9_TXEN):** TDM interface channel 9 transmit enable bit. Active only in full-duplex mode. When HIGH and ch9_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 9 time slot through sdo line.
8	1h RW	**Full Duplex Tx Channel Enable 8 (CH8_TXEN):** TDM interface channel 8 transmit enable bit. Active only in full-duplex mode. When HIGH and ch8_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 8th time slot through sdo line.
7	1h RW	**Full Duplex Tx Channel Enable 7 (CH7_TXEN):** TDM interface channel 7 transmit enable bit. Active only in full-duplex mode. When HIGH and ch7_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 7 time slot through sdo line.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RW	**Full Duplex Tx Channel Enable 6 (CH6_TXEN):** TDM interface channel 6 transmit enable bit. Active only in full-duplex mode. When HIGH and ch6_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 6 time slot through sdo line.
5	1h RW	**Full Duplex Tx Channel Enable 5 (CH5_TXEN):** TDM interface channel 5 transmit enable bit. Active only in full-duplex mode. When HIGH and ch5_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 5 time slot through sdo line.
4	1h RW	**Full Duplex Tx Channel Enable 4 (CH4_TXEN):** TDM interface channel 4 transmit enable bit. Active only in full-duplex mode. When HIGH and ch4_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 4 time slot through sdo line.
3	1h RW	**Full Duplex Tx Channel Enable 3 (CH3_TXEN):** TDM interface channel 3 transmit enable bit. Active only in full-duplex mode. When HIGH and ch3_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 3 time slot through sdo line.
2	1h RW	**Full Duplex Tx Channel Enable 2 (CH2_TXEN):** TDM interface channel 2 transmit enable bit. Active only in full-duplex mode. When HIGH and ch2_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 2 time slot through sdo line.
1	1h RW	**Full Duplex Tx Channel Enable 1 (CH1_TXEN):** TDM interface channel 1 transmit enable bit. Active only in full-duplex mode. When HIGH and ch1_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 1 time slot through sdo line.
0	1h RW	**Full Duplex Rx Channel Enable 0 (CH0_RXEN):** TDM interface channel 0 transmit enable bit. Active only in full-duplex mode. When HIGH and ch0_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 0 time slot through sdo line.

14.16.1.15 TX/RX FIFO (FIFO) — Offset 48300040h

TX/RX FIFO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 48300040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SFR:** Registers for TX and RX FIFO.

14.16.2 I2S_1 Registers Summary

Table 14-35. Summary of I2S_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48302000h	4	I2S-SC Control (I2S_CTRL)	000001B8h
48302004h	4	I2S Full Duplex Mode Receiver Control (I2S_CTRL_FDR)	00000010h
48302008h	4	Transceiver Sample Resolution (I2S_SRES)	00000000h
4830200Ch	4	Full Duplex Mode Receive Samples Resolution (I2S_SRES_FDR)	00000000h
48302010h	4	Transceiver Sample Rate (I2S_SRATE)	00000000h
48302014h	4	I2S-SC Status Flags (I2S_STAT)	0003000Ch
48302018h	4	FIFO Using Level(Read Only) (FIFO_LEVEL)	00000000h
4830201Ch	4	FIFO Almost Empty Level (FIFO_AEMPTY)	00000000h
48302020h	4	FIFO Almost Full Level (FIFO_AFULL)	0000001Fh
48302024h	4	Full Duplex Mode Receiver FIFO Using Level(Read Only) (FIFO_LEVEL_FDR)	00000000h
48302028h	4	Full Duplex Mode Receiver FIFO Almost Empty Level (FIFO_AEMPTY_FDR)	00000000h
4830202Ch	4	Full Duplex Mode Receiver FIFO Almost Full Level (FIFO_AFULL_FDR)	0000001Fh
48302030h	4	Time Division Multiplexing Control (TDM_CTRL)	FFFF0000h
48302034h	4	Time Division Multiplexing Full Duplex Mode Channels Direction (TDM_FD_DIR)	0000FFFFh
48302040h	4	TX/RX FIFo (FIFO)	00000000h

14.16.2.1 I2S-SC Control (I2S_CTRL) — Offset 48302000h

I2S-SC Control Register After end of reset bit sfr_rst triggers to 1 and bit fifo_rst triggers to 1. Therefore register value after end of reset is 000001B8.

Type	Size	Offset	Default
MMIO	32 bit	48302000h	000001B8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Full-Duplex Mode Receiver Samples Resolution (FULL_DUPLEX):** Full-duplex mode enable bit. If HIGH transmitter and receiver data units work simultaneously, otherwise only transmitter or receiver is enable in dependent to dir_cfg bit (I2S_CTRL[1]).
30	0h RW	**FIFO Almost Full Mask Register (FIFO_AFULL_MASK):** Bit masking interrupt request generation after FIFO becomes almost full. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
29	0h RW	**FIFO Full Mask Register (FIFO_FULL_MASK):** Bit masking interrupt request generation after FIFO becomes full. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
28	0h RW	**FIFO Almost Empty Mask Register (FIFO_AEMPTY_MASK):** Bit masking interrupt request generation after FIFO becomes almost empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition. Sampled on the rising edge of the clock.
27	0h RW	**FIFO Empty Mask Register (FIFO_EMPTY_MASK):** Bit masking interrupt request generation after FIFO becomes empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition. Sampled on the rising edge of the clock.
26	0h RW	**I2s Mask Register (I2S_MASK):** Bit masking interrupt request generation after underrun/overrun condition occurrence in I2S-SC transceiver. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for underrun event interrupt. Sampled on the rising edge of the clock.
25	0h RW	**Interupt Mask Register (INTREQ_MASK):** Bit masking all interrupt requests. When LOW all interrupts are masked, when HIGH interrupts use individual masks. Sampled on the rising edge of the clock.
24	0h RW	**Transceiver Clock Enable. (I2S_STB):** Transceiver clock enable. When LOW the clk_i2s clock is enabled, else clock is disabled. Sampled on the rising edge of the clock.
23	0h RW	**Audio Data Sample Alignment At Host Data Bus. (HOST_DATA_ALIGN):** Audio data sample alignment at host data bus. When LOW the audio sample data is aligned to the LSB at the host data bus. When HIGH the audio sample data is aligned to the MSB at host data bus.Sampled on the rising edge of the clock.
22	0h RW	**Audio Data Sample Arrangement In Audio Data Slot (DATA_ORDER):** Bit masking interrupt request generation after FIFO becomes almost empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.
21	0h RW	**Audio Sample Alignment In Audio Data Time Slot (DATA_ALIGN):** Bit masking interrupt request generation after FIFO becomes empty. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for transmitter FIFO empty condition.

Bit Range	Default & Access	Field Name (ID): Description
20:16	00h RW	**Audio Data Delay After WS Signal (DATA_WS_DEL):** Bit masking interrupt request generation after underrun/overrun condition occurrence in I2S-SC transceiver. When LOW, masks generation of interrupt request. When full-duplex mode is active, this bit is a mask only for underrun event interrupt.
15	0h RW	**The Word Select Signal Polarity Selection. (WS_POLAR):** Bit masking all interrupt requests. When LOW all interrupts are masked, when HIGH interrupts use individual masks.
14	0h RW	**The Continuous Serial Clock Active Edge. (SCK_POLAR):** Transceiver clock enable. When LOW the clk_i2s clock is enabled, else clock is disabled.
13	0h RW	**Mono/Stereo Audio Mode Selection (AUDIO_MODE):** Audio data sample alignment at host data bus. When LOW the audio sample data is aligned to the LSB at the host data bus. When HIGH the audio sample data is aligned to the MSB at host data bus.
12	0h RW	**Active Audio Channel In Mono Mode (MONO_MODE):** Active audio channel in mono mode. When LOW left audio channel is active. When HIGH right audio channel is active.
11:8	1h RW	**Word Select Signal (WS) Format. (WS_MODE):** Word select signal (WS) format. TDM mode is not active: Only bit 8 is relevant. If it is set to LOW (even value of ws_mode) WS signal have DSP audio interface specification format. If it is set to HIGH (odd value of ws_mode) WS signal have standard I2S audio interface specification format. TDM mode is active: When field equals 0 WS signal has DSP audio interface specification format, otherwise (ws_mode field equals the value from range 1 &CHN_NO-1) WS.
7:5	5h RW	**Audio Channel Time Slot Width (CHN_WIDTH):** Audio channel time slot width in I2S master or DSP/TDM master and slave modes. 0 8 SCK cycles per audio channel 1 12 SCK cycles per audio channel 2 16 SCK cycles per audio channel 3 18 SCK cycles per audio channel 4 20 SCK cycles per audio channel 5 24 SCK cycles per audio channel 6 28 SCK cycles per audio channel 7 32 SCK cycles per audio channel.
4	1h RW	**FIFO Reset (FIFO_RST):** FIFO reset. When LOW, FIFO pointer is reset to zero. Threshold levels for FIFO are unchanged. This bit is automatically set to HIGH after one clock cycle. In full-duplex mode this bit resets only transmitter FIFO.
3	1h RW	**SFR Block Synchronous Reset (SFR_RST):** SFR block synchronous reset. When LOW, all bits in SFR registers are reset to default values. This bit is automatically set to HIGH after one clock cycle.
2	0h RW	**Configuration Bit For Transceiver Synchronizing Unit (MS_CFG):** Configuration bit for transceiver synchronizing unit: 1 Master 0 Slave.
1	0h RW	**Direction Of Transmission (DIR_CFG):** 1 Transmitter 0 Receiver.
0	0h RW	**Enable Bit For I2S Transceiver (I2S_EN):** 1 enables transceiver 0 disables transceiver, causes synchronous reset signal, configuration SFR bits are unchanged .

14.16.2.2 I2S Full Duplex Mode Receiver Control (I2S_CTRL_FDR) — Offset 48302004h

I2S Full Duplex Mode Receiver Control Register After end of reset bit FIFO_rst triggers to 1. Therefore register value after end of reset is 00000010.

Type	Size	Offset	Default
MMIO	32 bit	48302004h	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**Full Duplex Almost FIFO Full Mask Register (RFIFO_AFULL_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes almost full. When LOW, masks generation of interrupt request.
29	0h RW	**Full Duplex FIFO Full Mask Register (RFIFO_FULL_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes full. When LOW, masks generation of interrupt request.
28	0h RW	**Full Duplex Almost FIFO Empty Mask Register (RFIFO_AEMPTY_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes almost empty. When LOW, masks generation of interrupt request.
27	0h RW	**Full Duplex FIFO Empty Mask Register (RFIFO_EMPTY_MASK):** Bit masking interrupt request generation after full-duplex mode receive FIFO becomes empty. When LOW, masks generation of interrupt request.
26	0h RW	**Full Duplex I2s_mask Register (RI2S_MASK):** Bit masking interrupt request generation after overrun condition occurrence in I2S-SC full-duplex mode receiver. When LOW, masks generation of interrupt request.
25:5	0h RO	**Reserved**
4	1h RW	**Full-Duplex Mode Receiver FIFO Reset. (FIFO_RST):** Full-duplex mode receiver FIFO reset. Active only in full-duplex mode. When '0', RFIFO pointer is reset to zero. Threshold levels for RFIFO are unchanged. The bit is automatically set to '1' after one clock cycle.
3:0	0h RO	**Reserved**

14.16.2.3 Transceiver Sample Resolution (I2S_SRES) — Offset 48302008h

Transceiver Sample Resolution.

Type	Size	Offset	Default
MMIO	32 bit	48302008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Samples Resolution. (RESOLUTION):** Samples resolution. When full-duplex mode is active, this value specifies resolution only for transmitted samples. Sampled on the rising edge of the clock. It simply should be assigned the value equal to the number of valid bits minus one, for example: 00000B sample resolution = 1 bit 11111B sample resolution = 32 bits.

14.16.2.4 Full Duplex Mode Receive Samples Resolution (I2S_SRES_FDR) — Offset 4830200Ch

Full Duplex Mode Receive Samples Resolution.

Type	Size	Offset	Default
MMIO	32 bit	4830200Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**I2s_sres Register - Samples Resolution (RESOLUTION):** Full-duplex mode receive samples resolution. When half-duplex mode is active this value is ignored. It simply should be assigned the value equal to the number of valid bits minus one, for example: 00000B sample resolution = 1 bit 11111B sample resolution = 32 bits.

14.16.2.5 Transceiver Sample Rate (I2S_SRATE) — Offset 48302010h

Transceiver Sample Rate.

Type	Size	Offset	Default
MMIO	32 bit	48302010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:0	00000h RW	**SAMPLE_RATE:** In general value of sample rate is the quotient of clk frequency and I2S rate [bit/s]. The value of sample rate is the higher the clk frequency is greater than I2S rate.

14.16.2.6 I2S-SC Status Flags (I2S_STAT) — Offset 48302014h

I2S-SC Status Flags Register.

Type	Size	Offset	Default
MMIO	32 bit	48302014h	0003000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Receive FIFO Almost Full Flag In Full-Duplex Mode (RFIFO_AFULL):** Receive FIFO almost full flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO becomes almost full (rising edge of almost full condition).
18	0h RW	**Receive FIFO Full Flag In Full-Duplex Mode (RFIFO_FULL):** Receive FIFO full flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO is full.
17	1h RW	**Receive FIFO Almost Empty Flag In Full-Duplex Mode (RFIFO_AEMPTY):** Receive FIFO almost empty flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO becomes almost empty (rising edge of almost empty condition).
16	1h RW	**Receive FIFO Empty Flag In Full-Duplex Mode (RFIFO_EMPTY):** Receive FIFO empty flag in full-duplex mode. Active HIGH. This flag is set to HIGH when RX FIFO is empty.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**FIFO Almost Full Flag (FIFO_AFULL):** FIFO almost full flag. Active HIGH. This flag is set to HIGH when FIFO becomes almost full (rising edge of almost full condition). When full-duplex mode is active, this bit is a flag only for transmitter FIFO almost full condition.
4	0h RW	**FIFO Full Flag (FIFO_FULL):** FIFO full flag. Active HIGH. This flag is set to HIGH when FIFO is full. When full-duplex mode is active, this bit is a flag only for transmitter FIFO full condition.
3	1h RW	**FIFO Almost Empty Flag (FIFO_AEMPTY):** FIFO almost empty flag. Active HIGH. This flag is set to HIGH when FIFO becomes almost empty (rising edge of almost empty condition). When full-duplex mode is active, this bit is a flag only for transmitter FIFO almost empty condition.
2	1h RW	**FIFO Empty Flag (FIFO_EMPTY):** FIFO empty flag. Active HIGH. This flag is set to HIGH when FIFO is empty. When full-duplex mode is active, this bit is a flag only for transmitter FIFO empty condition.
1	0h RW	**RDATA_OVRERR:** Indicates data overrun error for transceiver in receiver mode, active HIGH. Sampled and updated on the rising edge of the clock. Writing LOW value to this bit resets the transceiver and the FIFO. The transceiver configuration is preserved.
0	0h RW	**Full Duplex Mode Samples Resolution Register (TDATA_UNDERR):** Indicates data underrun event, active HIGH. This flag is set to HIGH when TX underrun arises (rising edge of underrun condition).

14.16.2.7 FIFO Using Level(Read Only) (FIFO_LEVEL) — Offset 48302018h

FIFO Using Level Register (read only).

Type	Size	Offset	Default
MMIO	32 bit	48302018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RO	**FIFO Level Register (FIFO_LEVEL):** Indicates FIFO level. Updated on the rising edge of the clock. When full-duplex mode is active, this register holds value of the transmitter FIFO level. When half-duplex mode is active, this register holds value of the transmitter or receiver FIFO level in dependent to the transmit/receive direction mode.

14.16.2.8 FIFO Almost Empty Level (FIFO_AEMPTY) — Offset 4830201Ch

FIFO Almost Empty Level.

Type	Size	Offset	Default
MMIO	32 bit	4830201Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**FIFO Almost Empty Threshold Level (AEMPTY_THRESHOLD):** Determines threshold for almost empty flag in the FIFO. When full-duplex mode is active, this register specifies an almost empty level of the transmitter FIFO level.

14.16.2.9 FIFO Almost Full Level (FIFO_AFULL) — Offset 48302020h

FIFO Almost Full Level.

Type	Size	Offset	Default
MMIO	32 bit	48302020h	0000001Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	1Fh RW	**FIFO Aempty Threshold Level (AFULL_THRESHOLD):** Determines threshold for almost full flag in the FIFO. When full-duplex mode is active, this register specifies an almost full level of the transmitter FIFO level.

14.16.2.10 Full Duplex Mode Receiver FIFO Using Level(Read Only) (FIFO_LEVEL_FDR) — Offset 48302024h

Full Duplex Mode Receiver FIFO Using Level Register (read only).

Type	Size	Offset	Default
MMIO	32 bit	48302024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RO	**Full Duplex FIFO Level (RX_FIFO_LEVEL):** Full-duplex mode receive FIFO level.

14.16.2.11 Full Duplex Mode Receiver FIFO Almost Empty Level (FIFO_AEMPTY_FDR) — Offset 48302028h

Full Duplex Mode Receiver FIFO Almost Empty Level.

Type	Size	Offset	Default
MMIO	32 bit	48302028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Full Duples FIFO Almost Empty Level (AEMPTY_THRESHOLD):** Determines almost empty level in the receive FIFO in full-duplex mode.

14.16.2.12 Full Duplex Mode Receiver FIFO Almost Full Level (FIFO_AFULL_FDR) — Offset 4830202Ch

Full Duplex Mode Receiver FIFO Almost Full Level.

Type	Size	Offset	Default
MMIO	32 bit	4830202Ch	0000001Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	1Fh RW	**Full Duplex FIFO Almost Full Level (AFULL_THRESHOLD):** Determines almost full level in the receive FIFO in full-duplex mode.

14.16.2.13 Time Division Multiplexing Control (TDM_CTRL) — Offset 48302030h

Time Division Multiplexing Control Register.

Type	Size	Offset	Default
MMIO	32 bit	48302030h	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**TDM Channel Enable 15 (CH15_EN):** TDM interface channel 15 activating bit. When HIGH 15th time slot sample is transmitted and/or received depending on transceiver mode.
30	1h RW	**TDM Channel Enable 14 (CH14_EN):** TDM interface channel 14 activating bit. When HIGH 14th time slot sample is transmitted and/or received depending on transceiver mode.
29	1h RW	**TDM Channel Enable 13 (CH13_EN):** TDM interface channel 13 activating bit. When HIGH 13th time slot sample is transmitted and/or received depending on transceiver mode.
28	1h RW	**TDM Channel Enable 12 (CH12_EN):** TDM interface channel 12 activating bit. When HIGH 12th time slot sample is transmitted and/or received depending on transceiver mode.
27	1h RW	**TDM Channel Enable 11 (CH11_EN):** TDM interface channel 11 activating bit. When HIGH 11th time slot sample is transmitted and/or received depending on transceiver mode.
26	1h RW	**TDM Channel Enable 10 (CH10_EN):** TDM interface channel 10 activating bit. When HIGH 10th time slot sample is transmitted and/or received depending on transceiver mode.

Bit Range	Default & Access	Field Name (ID): Description
25	1h RW	**TDM Channel Enable 9 (CH9_EN):** TDM interface channel 9 activating bit. When HIGH 9th time slot sample is transmitted and/or received depending on transceiver mode.
24	1h RW	**TDM Channel Enable 8 (CH8_EN):** TDM interface channel 8 activating bit. When HIGH 8th time slot sample is transmitted and/or received depending on transceiver mode.
23	1h RW	**TDM Channel Enable 7 (CH7_EN):** TDM interface channel 7 activating bit. When HIGH 7th time slot sample is transmitted and/or received depending on transceiver mode.
22	1h RW	**TDM Channel Enable 6 (CH6_EN):** TDM interface channel 6 activating bit. When HIGH 6th time slot sample is transmitted and/or received depending on transceiver mode.
21	1h RW	**TDM Channel Enable 5 (CH5_EN):** TDM interface channel 5 activating bit. When HIGH 5th time slot sample is transmitted and/or received depending on transceiver mode.
20	1h RW	**TDM Channel Enable 4 (CH4_EN):** TDM interface channel 4 activating bit. When HIGH 4th time slot sample is transmitted and/or received depending on transceiver mode.
19	1h RW	**TDM Channel Enable 3 (CH3_EN):** TDM interface channel 3 activating bit. When HIGH 3rd time slot sample is transmitted and/or received depending on transceiver mode.
18	1h RW	**TDM Channel Enable 2 (CH2_EN):** TDM interface channel 2 activating bit. When HIGH 2nd time slot sample is transmitted and/or received depending on transceiver mode.
17	1h RW	**TDM Channel Enable 1 (CH1_EN):** TDM interface channel 1 activating bit. When HIGH 1st time slot sample is transmitted and/or received depending on transceiver mode.
16	1h RW	**TDM Channel Enable 0 (CH0_EN):** TDM interface channel 0 activating bit. When HIGH zero time slot sample is transmitted and/or received depending on transceiver mode.
15:5	0h RO	**Reserved**
4:1	0h RW	**Tdm Register For Number Of Channels Per Frame (CHN_NO):** Number of supported audio channels in TDM compatible interface mode. Written value equals channels number minus 1.
0	0h RW	**Time Division Multiplexing Audio Interface Enable (TDM_EN):** Time Division Multiplexing audio interface enable. When HIGH audio interface works in TDM compatible mode determined by this register value. When LOW audio interface works in standard stereo I2S mode.

14.16.2.14 Time Division Multiplexing Full Duplex Mode Channels Direction (TDM_FD_DIR) — Offset 48302034h

Time Division Multiplexing Full Duplex Mode Channels Direction Register.

Type	Size	Offset	Default
MMIO	32 bit	48302034h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Full Duplex Rx Channel Enable 15 (CH15_RXEN):** TDM interface channel 15 receive enable bit. Active only in full-duplex mode. When HIGH and ch15_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 15 time slot.
30	0h RW	**Full Duplex Rx Channel Enable 14 (CH14_RXEN):** TDM interface channel 14 receive enable bit. Active only in full-duplex mode. When HIGH and ch14_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 14 time slot.
29	0h RW	**Full Duplex Rx Channel Enable 13 (CH13_RXEN):** TDM interface channel 13 receive enable bit. Active only in full-duplex mode. When HIGH and ch13_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 13 time slot.
28	0h RW	**Full Duplex Rx Channel Enable 12 (CH12_RXEN):** TDM interface channel 12 receive enable bit. Active only in full-duplex mode. When HIGH and ch12_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 12 time slot.
27	0h RW	**Full Duplex Rx Channel Enable 11 (CH11_RXEN):** TDM interface channel 11 receive enable bit. Active only in full-duplex mode. When HIGH and ch11_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 11 time slot.
26	0h RW	**Full Duplex Rx Channel Enable 10 (CH10_RXEN):** TDM interface channel 10 receive enable bit. Active only in full-duplex mode. When HIGH and ch10_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 10 time slot.
25	0h RW	**Full Duplex Rx Channel Enable 9 (CH9_RXEN):** TDM interface channel 9 receive enable bit. Active only in full-duplex mode. When HIGH and ch9_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 9 time slot.
24	0h RW	**Full Duplex Rx Channel Enable 8 (CH8_RXEN):** TDM interface channel 8 receive enable bit. Active only in full-duplex mode. When HIGH and ch8_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 8 time slot.
23	0h RW	**Full Duplex Rx Channel Enable 7 (CH7_RXEN):** TDM interface channel 7 receive enable bit. Active only in full-duplex mode. When HIGH and ch7_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 7 time slot.
22	0h RW	**Full Duplex Rx Channel Enable 6 (CH6_RXEN):** TDM interface channel 6 receive enable bit. Active only in full-duplex mode. When HIGH and ch6_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 6 time slot.
21	0h RW	**Full Duplex Rx Channel Enable 5 (CH5_RXEN):** TDM interface channel 5 receive enable bit. Active only in full-duplex mode. When HIGH and ch5_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 5 time slot.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Full Duplex Rx Channel Enable 4 (CH4_RXEN):** TDM interface channel 4 receive enable bit. Active only in full-duplex mode. When HIGH and ch4_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 4 time slot.
19	0h RW	**Full Duplex Rx Channel Enable 3 (CH3_RXEN):** TDM interface channel 3 receive enable bit. Active only in full-duplex mode. When HIGH and ch3_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 3 time slot.
18	0h RW	**Full Duplex Rx Channel Enable 2 (CH2_RXEN):** TDM interface channel 2 receive enable bit. Active only in full-duplex mode. When HIGH and ch2_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 2 time slot.
17	0h RW	**Full Duplex Rx Channel Enable 1 (CH1_RXEN):** TDM interface channel 1 receive enable bit. Active only in full-duplex mode. When HIGH and ch1_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 1 time slot.
16	0h RW	**Full Duplex Tx Channel Enable 0 (CH0_TXEN):** TDM interface channel 0 receive enable bit. Active only in full-duplex mode. When HIGH and ch0_en bit in TDM_CTRL register is HIGH audio sample is received from sdi line at 0 time slot.
15	1h RW	**Full Duplex Tx Channel Enable 15 (CH15_TXEN):** TDM interface channel 15 transmit enable bit. Active only in full-duplex mode. When HIGH and ch15_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 15 time slot through sdo line.
14	1h RW	**Full Duplex Tx Channel Enable 14 (CH14_TXEN):** TDM interface channel 14 transmit enable bit. Active only in full-duplex mode. When HIGH and ch14_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 14 time slot through sdo line.
13	1h RW	**Full Duplex Tx Channel Enable 13 (CH13_TXEN):** TDM interface channel 13 transmit enable bit. Active only in full-duplex mode. When HIGH and ch13_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 13 time slot through sdo line.
12	1h RW	**Full Duplex Tx Channel Enable 12 (CH12_TXEN):** TDM interface channel 12 transmit enable bit. Active only in full-duplex mode. When HIGH and ch12_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 12 time slot through sdo line.
11	1h RW	**Full Duplex Tx Channel Enable 11 (CH11_TXEN):** TDM interface channel 11 transmit enable bit. Active only in full-duplex mode. When HIGH and ch11_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 11 time slot through sdo line.
10	1h RW	**Full Duplex Tx Channel Enable 10 (CH10_TXEN):** TDM interface channel 10 transmit enable bit. Active only in full-duplex mode. When HIGH and ch10_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 10 time slot through sdo line.
9	1h RW	**Full Duplex Tx Channel Enable 9 (CH9_TXEN):** TDM interface channel 9 transmit enable bit. Active only in full-duplex mode. When HIGH and ch9_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 9 time slot through sdo line.
8	1h RW	**Full Duplex Tx Channel Enable 8 (CH8_TXEN):** TDM interface channel 8 transmit enable bit. Active only in full-duplex mode. When HIGH and ch8_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 8th time slot through sdo line.
7	1h RW	**Full Duplex Tx Channel Enable 7 (CH7_TXEN):** TDM interface channel 7 transmit enable bit. Active only in full-duplex mode. When HIGH and ch7_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 7 time slot through sdo line.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RW	**Full Duplex Tx Channel Enable 6 (CH6_TXEN):** TDM interface channel 6 transmit enable bit. Active only in full-duplex mode. When HIGH and ch6_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 6 time slot through sdo line.
5	1h RW	**Full Duplex Tx Channel Enable 5 (CH5_TXEN):** TDM interface channel 5 transmit enable bit. Active only in full-duplex mode. When HIGH and ch5_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 5 time slot through sdo line.
4	1h RW	**Full Duplex Tx Channel Enable 4 (CH4_TXEN):** TDM interface channel 4 transmit enable bit. Active only in full-duplex mode. When HIGH and ch4_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 4 time slot through sdo line.
3	1h RW	**Full Duplex Tx Channel Enable 3 (CH3_TXEN):** TDM interface channel 3 transmit enable bit. Active only in full-duplex mode. When HIGH and ch3_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 3 time slot through sdo line.
2	1h RW	**Full Duplex Tx Channel Enable 2 (CH2_TXEN):** TDM interface channel 2 transmit enable bit. Active only in full-duplex mode. When HIGH and ch2_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 2 time slot through sdo line.
1	1h RW	**Full Duplex Tx Channel Enable 1 (CH1_TXEN):** TDM interface channel 1 transmit enable bit. Active only in full-duplex mode. When HIGH and ch1_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 1 time slot through sdo line.
0	1h RW	**Full Duplex Rx Channel Enable 0 (CH0_RXEN):** TDM interface channel 0 transmit enable bit. Active only in full-duplex mode. When HIGH and ch0_en bit in TDM_CTRL register is HIGH audio sample is transmitted at 0 time slot through sdo line.

14.16.2.15 TX/RX FIFO (FIFO) — Offset 48302040h

TX/RX FIFO.

Type	Size	Offset	Default
MMIO	32 bit	48302040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SFR:** Registers for TX and RX FIFO.

14.17 Timers Registers

Timers Registers	Address Offset	Table
Timers	48400000h - 484000CCh	Table 14-36

14.17.1 Timers Registers Summary

Table 14-36. Summary of Timers Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48400000h	4	TIMER1LOADCOUNT	00000000h
48400004h	4	TIMER1CURRENTVAL	80000000h
48400008h	4	TIMER1CONTROLREG	00000000h
4840000Ch	4	TIMER1EOI	00000000h
48400010h	4	TIMER1INTSTAT	00000000h
48400014h	4	TIMER2LOADCOUNT	00000000h
48400018h	4	TIMER2CURRENTVAL	80000000h
4840001Ch	4	TIMER2CONTROLREG	00000000h
48400020h	4	TIMER2EOI	00000000h
48400024h	4	TIMER2INTSTAT	00000000h
48400028h	4	TIMER3LOADCOUNT	00000000h
4840002Ch	4	TIMER3CURRENTVAL	80000000h
48400030h	4	TIMER3CONTROLREG	00000000h
48400034h	4	TIMER3EOI	00000000h
48400038h	4	TIMER3INTSTAT	00000000h
4840003Ch	4	TIMER4LOADCOUNT	00000000h
48400040h	4	TIMER4CURRENTVAL	80000000h
48400044h	4	TIMER4CONTROLREG	00000000h
48400048h	4	TIMER4EOI	00000000h
4840004Ch	4	TIMER4INTSTAT	00000000h
48400050h	4	TIMER5LOADCOUNT	00000000h
48400054h	4	TIMER5CURRENTVAL	80000000h
48400058h	4	TIMER5CONTROLREG	00000000h
4840005Ch	4	TIMER5EOI	00000000h
48400060h	4	TIMER5INTSTAT	00000000h
48400064h	4	TIMER6LOADCOUNT	00000000h
48400068h	4	TIMER6CURRENTVAL	80000000h
4840006Ch	4	TIMER6CONTROLREG	00000000h
48400070h	4	TIMER6EOI	00000000h
48400074h	4	TIMER6INTSTAT	00000000h
48400078h	4	TIMER7LOADCOUNT	00000000h
4840007Ch	4	TIMER7CURRENTVAL	80000000h
48400080h	4	TIMER7CONTROLREG	00000000h
48400084h	4	TIMER7EOI	00000000h
48400088h	4	TIMER7INTSTAT	00000000h
4840008Ch	4	TIMER8LOADCOUNT	00000000h
48400090h	4	TIMER8CURRENTVAL	80000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48400094h	4	TIMER8CONTROLREG	00000000h
48400098h	4	TIMER8EOI	00000000h
4840009Ch	4	TIMER8INTSTAT	00000000h
484000A0h	4	TIMERSINTSTAT	00000000h
484000A4h	4	TIMERSEOI	00000000h
484000A8h	4	TIMERSRAWINTSTAT	00000000h
484000ACh	4	TIMERSCOMPVERSION	3231302Ah
484000B0h	4	TIMER1LOADCOUNT2	00000000h
484000B4h	4	TIMER2LOADCOUNT2	00000000h
484000B8h	4	TIMER3LOADCOUNT2	00000000h
484000BCh	4	TIMER4LOADCOUNT2	00000000h
484000C0h	4	TIMER5LOADCOUNT2	00000000h
484000C4h	4	TIMER6LOADCOUNT2	00000000h
484000C8h	4	TIMER7LOADCOUNT2	00000000h
484000CCh	4	TIMER8LOADCOUNT2	00000000h

14.17.1.1 TIMER1LOADCOUNT — Offset 48400000h

Timer1 Load Count Register - Name: Timer1 Load Count Register Size: 8-32 bits Address Offset: 0x00 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	48400000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER1LOADCOUNT:** Value to be loaded into Timer1. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.2 TIMER1CURRENTVAL — Offset 48400004h

Name: Timer1 Current Value Size: 8-32 bits Address Offset: 4 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400004h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER1CURRENTVAL:** Current Value of Timer1. This register is supported only when timer_1_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.3 TIMER1CONTROLREG — Offset 48400008h

Timer1 Control Register - Name: Timer1 Control Register Size: 4 bits Address Offset: 8 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer1. You can program each Timer1ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	48400008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_1_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer1. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer1. 0: free_running mode 1: user_defined count mode NOTE: You must set the Timer1LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer1. 0: disable 1: enable

14.17.1.4 TIMER1EOI — Offset 4840000Ch

Timer1 End-of-Interrupt Register - Name: Timer1 End-of-Interrupt Register Size: 1 bit Address Offset: 12 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	4840000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER1EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer1.

14.17.1.5 TIMER1INTSTAT — Offset 48400010h

Timer1 Interrupt Status Register - Name: Timer1 Interrupt Status Register Size: 1 bit Address Offset: 16 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER1INTSTAT:** Contains the interrupt status for Timer1.

14.17.1.6 TIMER2LOADCOUNT — Offset 48400014h

Timer2 Load Count Register - Name: Timer2 Load Count Register Size: 8-32 bits Address Offset: 20 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	48400014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER2LOADCOUNT:** Value to be loaded into Timer2. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.7 TIMER2CURRENTVAL — Offset 48400018h

Timer2 Current Value - Name: Timer2 Current Value Size: 8-32 bits Address Offset: 24 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400018h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER2CURRENTVAL:** Current Value of Timer2. This register is supported only when timer_2_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.8 TIMER2CONTROLREG — Offset 4840001Ch

Timer2 Control Register - Name: Timer2 Control Register Size: 3 bits Address Offset: 28 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer2. You can program each Timer2ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	4840001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_2_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer2. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer2. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer2LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer2. 0: disable 1: enable

14.17.1.9 TIMER2EOI — Offset 48400020h

Timer2 End-of-Interrupt Register - Name: Timer2 End-of-Interrupt Register Size: 1 bit Address Offset: 32 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER2EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer2.

14.17.1.10 TIMER2INTSTAT — Offset 48400024h

Timer2 Interrupt Status Register - Name: Timer2 Interrupt Status Register Size: 1 bit Address Offset: 36 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER2INTSTAT:** Contains the interrupt status for Timer2.

14.17.1.11 TIMER3LOADCOUNT — Offset 48400028h

Timer1 Load Count Register - Name: Timer3 Load Count Register Size: 8-32 bits Address Offset: 40 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	48400028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER3LOADCOUNT:** Value to be loaded into Timer3. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.12 TIMER3CURRENTVAL — Offset 4840002Ch

Timer3 Current Value - Name: Timer3 Current Value Size: 8-32 bits Address Offset: 44 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	4840002Ch	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER3CURRENTVAL:** Current Value of Timer3. This register is supported only when timer_3_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.13 TIMER3CONTROLREG — Offset 48400030h

Timer3 Control Register - Name: Timer3 Control Register Size: 4 bits Address Offset: 48 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer3. You can program each Timer3ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	48400030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_3_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer3. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer3. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer3LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer3. 0: disable 1: enable

14.17.1.14 TIMER3EOI — Offset 48400034h

Timer3 End-of-Interrupt Register - Name: Timer3 End-of-Interrupt Register Size: 1 bit Address Offset: 52 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER3EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer3.

14.17.1.15 TIMER3INTSTAT — Offset 48400038h

Timer3 Interrupt Status Register - Name: Timer3 Interrupt Status Register Size: 1 bit Address Offset: 56 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER3INTSTAT:** Contains the interrupt status for Timer3.

14.17.1.16 TIMER4LOADCOUNT — Offset 4840003Ch

Timer4 Load Count Register - Name: Timer4 Load Count Register Size: 8-32 bits Address Offset: 60 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	4840003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER4LOADCOUNT:** Value to be loaded into Timer4. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.17 TIMER4CURRENTVAL — Offset 48400040h

Timer4 Current Value Register - Name: Timer4 Current Value Size: 8-32 bits Address Offset: 64 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400040h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER4CURRENTVAL:** Current Value of Timer4. This register is supported only when timer_4_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.18 TIMER4CONTROLREG — Offset 48400044h

Timer4 Control Register - Name: Timer4 Control Register Size: 4 bits Address Offset: 68 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer4. You can program each Timer4ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	48400044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_4_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer4. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer4. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer4LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer4. 0: disable 1: enable

14.17.1.19 TIMER4EOI — Offset 48400048h

Timer4 End-of-Interrupt Register - Name: Timer4 End-of-Interrupt Register Size: 1 bit Address Offset: 72 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER4EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer4.

14.17.1.20 TIMER4INTSTAT — Offset 4840004Ch

Timer4 Interrupt Status Register - Name: Timer4 Interrupt Status Register Size: 1 bit Address Offset: 76 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	4840004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER4INTSTAT:** Contains the interrupt status for Timer4.

14.17.1.21 TIMER5LOADCOUNT — Offset 48400050h

Timer5 Load Count Register - Name: Timer5 Load Count Register Size: 8-32 bits Address Offset: 80 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	48400050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER5LOADCOUNT:** Value to be loaded into Timer5. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.22 TIMER5CURRENTVAL — Offset 48400054h

Timer5 Current Value - Name: Timer5 Current Value Size: 8-32 bits Address Offset: 84 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400054h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER5CURRENTVAL:** Current Value of Timer5. This register is supported only when timer_5_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.23 TIMER5CONTROLREG — Offset 48400058h

Timer5 Control Register - Name: Timer5 Control Register Size: 4 bits Address Offset: 88 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer5. You can program each Timer5ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	48400058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_5_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer5. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer5. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer5LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer5. 0: disable 1: enable

14.17.1.24 TIMER5EOI — Offset 4840005Ch

Timer5 End-of-Interrupt Register - Name: Timer5 End-of-Interrupt Register Size: 1 bit Address Offset: 92 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	4840005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER5EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer5.

14.17.1.25 TIMER5INTSTAT — Offset 48400060h

Timer5 Interrupt Status Register - Name: Timer5 Interrupt Status Register Size: 1 bit Address Offset: 96 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER5INTSTAT:** Contains the interrupt status for Timer5.

14.17.1.26 TIMER6LOADCOUNT — Offset 48400064h

Timer6 Load Count Register - Name: Timer6 Load Count Register Size: 8-32 bits Address Offset: 100 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	48400064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER6LOADCOUNT:** Value to be loaded into Timer6. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.27 TIMER6CURRENTVAL — Offset 48400068h

Timer6 Current Value Register - Name: Timer6 Current Value Size: 8-32 bits Address Offset: 104 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400068h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER6CURRENTVAL:** Current Value of Timer6. This register is supported only when timer_6_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.28 TIMER6CONTROLREG — Offset 4840006Ch

Timer6 Control Register - Name: Timer6 Control Register Size: 4 bits Address Offset: 108 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer6. You can program each Timer6ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	4840006Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_6_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer6. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer6. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer6LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer6. 0: disable 1: enable

14.17.1.29 TIMER6EOI — Offset 48400070h

Timer6 End-of-Interrupt Register - Name: Timer6 End-of-Interrupt Register Size: 1 bit Address Offset: 112 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER6EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer6.

14.17.1.30 TIMER6INTSTAT — Offset 48400074h

Timer6 Interrupt Status Register - Name: Timer6 Interrupt Status Register Size: 1 bit Address Offset: 116 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER6INTSTAT:** Contains the interrupt status for Timer6.

14.17.1.31 TIMER7LOADCOUNT — Offset 48400078h

Timer7 Load Count Register - Name: Timer7 Load Count Register Size: 8-32 bits Address Offset: 120 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	48400078h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER7LOADCOUNT:** Value to be loaded into Timer7. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.32 TIMER7CURRENTVAL — Offset 4840007Ch

Timer7 Current Register - Name: Timer7 Current Value Size: 8-32 bits Address Offset: 124 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	4840007Ch	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER7CURRENTVAL:** Current Value of Timer7. This register is supported only when timer_7_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.33 TIMER7CONTROLREG — Offset 48400080h

Timer7 Control Register - Name: Timer7 Control Register Size: 4 bits Address Offset: 128 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer7. You can program each Timer7ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	48400080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_7_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer7. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer7. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer7LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer7. 0: disable 1: enable

14.17.1.34 TIMER7EOI — Offset 48400084h

Timer7 End-of-Interrupt Register - Name: Timer7 End-of-Interrupt Register Size: 1 bit Address Offset: 132 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER7EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer7.

14.17.1.35 TIMER7INTSTAT — Offset 48400088h

Timer7 Interrupt Status Register - Name: Timer7 Interrupt Status Register Size: 1 bit Address Offset: 136 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER7INTSTAT:** Contains the interrupt status for Timer7.

14.17.1.36 TIMER8LOADCOUNT — Offset 4840008Ch

Timer8 Load Count Register - Name: Timer8 Load Count Register Size: 8-32 bits Address Offset: 140 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	4840008Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER8LOADCOUNT:** Value to be loaded into Timer8. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.

14.17.1.37 TIMER8CURRENTVAL — Offset 48400090h

Timer8 Current Value - Name: Timer8 Current Value Size: 8-32 bits Address Offset: 144 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400090h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	80000000h RO/V	**TIMER8CURRENTVAL:** Current Value of Timer8. This register is supported only when timer_8_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.

14.17.1.38 TIMER8CONTROLREG — Offset 48400094h

Timer8 Control Register - Name: Timer8 Control Register Size: 4 bits Address Offset: 148 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer8. You can program each Timer8ControlReg to enable or disable a specific timer and to control its mode of operation.

Type	Size	Offset	Default
MMIO	32 bit	48400094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**TIMER_PWM:** Pulse Width Modulation of timer_8_toggle output. 0: Disabled 1: Enabled This field is only present when TIM_NEWMODE is enabled
2	0h RW	**TIMER_INTERRUPT_MASK:** Timer interrupt mask for Timer8. 0: not masked 1: masked
1	0h RW	**TIMER_MODE:** Timer mode for Timer8. 0: free-running mode 1: user-defined count mode NOTE: You must set the Timer8LoadCount register to all 1s before enabling the timer in free-running mode.
0	0h RW	**TIMER_ENABLE:** Timer enable bit for Timer8. 0: disable 1: enable

14.17.1.39 TIMER8EOI — Offset 48400098h

Timer8 End-of-Interrupt Register - Name: Timer8 End-of-Interrupt Register Size: 1 bit Address Offset: 152 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	48400098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER8EOI:** Reading from this register returns all zeroes (0) and clears the interrupt from Timer8.

14.17.1.40 TIMER8INTSTAT — Offset 4840009Ch

Timer8 Interrupt Status Register - Name: Timer8 Interrupt Status Register Size: 1 bit Address Offset: 156 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	4840009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**TIMER8INTSTAT:** Contains the interrupt status for Timer8.

14.17.1.41 TIMERSINTSTAT — Offset 484000A0h

Timers Interrupt Status Register - Name: Timers Interrupt Status Register Size: 1-8 bits Address Offset: 0xa0 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	484000A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSINTSTAT:** Contains the interrupt status of all timers in the component. If a bit of this register is 0, then the corresponding timer interrupt is not active and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts: 0 = either timer_intr or timer_intr_n is not active after masking 1 = either timer_intr or timer_intr_n is active after masking.

14.17.1.42 TIMERSEOI — Offset 484000A4h

Timers End-of-Interrupt Register - Name: Timers End-of-Interrupt Register Size: 1-8 bits Address Offset: 0xa4 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	484000A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSEOI:** Reading this register returns all zeroes (0) and clears all active interrupts.

14.17.1.43 TIMERSRAWINTSTAT — Offset 484000A8h

Timers Raw Interrupt Status Register - Name: Timers Raw Interrupt Status Register Size: 1-8 bits Address Offset: 0xa8 Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	484000A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TIMERSRAWINTSTAT:** The register contains the unmasked interrupt status of all timers in the component. 0 = either timer_intr or timer_intr_n is not active prior to masking 1 = either timer_intr or timer_intr_n is active prior to masking.

14.17.1.44 TIMERSCOMPVERSION — Offset 484000ACh

Timers Component Version - Name: Timers Component Version Size: 32 bits Address Offset: 0xac Read/Write Access: Read

Type	Size	Offset	Default
MMIO	32 bit	484000ACh	3231302Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	3231302Ah RO/V	**TIMERSCOMPVERSION:** Current revision number of the DW_apb_timers component.

14.17.1.45 TIMER1LOADCOUNT2 — Offset 484000B0h

Timer1 Load Count2 Register - Name: Timer1 Load Count2 Register Size: 8-32 bits Address Offset: 0xb0 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER1LOADCOUNT2:** Value to be loaded into Timer1 when timer_1_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_1_toggle output.

14.17.1.46 TIMER2LOADCOUNT2 — Offset 484000B4h

Timer2 Load Count2 Register - Name: Timer2 Load Count2 Register Size: 8-32 bits Address Offset: 180 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER2LOADCOUNT2:** Value to be loaded into Timer2 when timer_2_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_2_toggle output.

14.17.1.47 TIMER3LOADCOUNT2 — Offset 484000B8h

Timer3 Load Count2 Register - Name: Timer3 Load Count2 Register Size: 8-32 bits Address Offset: 184 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER3LOADCOUNT2:** Value to be loaded into Timer3 when timer_3_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_3_toggle output.

14.17.1.48 TIMER4LOADCOUNT2 — Offset 484000BCh

Timer4 Load Count2 Register - Name: Timer4 Load Count2 Register Size: 8-32 bits Address Offset: 188 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER4LOADCOUNT2:** Value to be loaded into Timer4 when timer_4_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_4_toggle output.

14.17.1.49 TIMER5LOADCOUNT2 — Offset 484000C0h

Timer5 Load Count2 Register - Name: Timer5 Load Count2 Register Size: 8-32 bits Address Offset: 192 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER5LOADCOUNT2:** Value to be loaded into Timer5 when timer_5_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_5_toggle output.

14.17.1.50 TIMER6LOADCOUNT2 — Offset 484000C4h

Timer6 Load Count2 Register - Name: Timer6 Load Count2 Register Size: 8-32 bits Address Offset: 196 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER6LOADCOUNT2:** Value to be loaded into Timer6 when timer_6_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_6_toggle output.

14.17.1.51 TIMER7LOADCOUNT2 — Offset 484000C8h

Timer7 Load Count2 Register - Name: Timer7 Load Count2 Register Size: 8-32 bits Address Offset: 200 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER7LOADCOUNT2:** Value to be loaded into Timer7 when timer_7_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_7_toggle output.

14.17.1.52 TIMER8LOADCOUNT2 — Offset 484000CCh

Timer8 Load Count2 Register - Name: Timer8 Load Count2 Register Size: 8-32 bits Address Offset: 204 Read/Write Access: Read/Write

Type	Size	Offset	Default
MMIO	32 bit	484000CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TIMER8LOADCOUNT2:** Value to be loaded into Timer8 when timer_8_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_8_toggle output.

14.18 QEP Interface Registers

There are four QEP Interface Registers:-

- QEP_0 Registers
- QEP_1 Registers
- QEP_2 Registers
- QEP_3 Registers

QEP Registers	Address Offset	Table
QEP_0	48600000h - 48600024h	Table 14-37
QEP_1	48602000h - 48602024h	Table 14-38
QEP_2	48604000h - 48604024h	Table 14-39
QEP_3	48606000h - 48606024h	Table 14-40

14.18.1 QEP_0 Registers Summary

Table 14-37. Summary of QEP_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48600000h	4	QEPCON	0000001Ch
48600004h	4	QEPFLT	00000000h
48600008h	4	QEPCOUNT	00000000h
4860000Ch	4	QEPMAX	FFFFFFFFh
48600010h	4	QEPWDT	00000000h
48600014h	4	QEPCAPDIV	00000000h
48600018h	4	QEPCNTR	00000000h
4860001Ch	4	QEPCAPBUF	00000000h
48600020h	4	QEPINT_STAT	00000000h
48600024h	4	QEPINT_MASK	00000000h

14.18.1.1 QEPCON — Offset 48600000h

QEP Control Register. This register controls the QEP operation and provides status flags for the state of the QEP module

Type	Size	Offset	Default
MMIO	32 bit	48600000h	0000001Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**FIFO_EMPTY:** Capture FIFO Empty Status Flag. Set when the FIFO is empty
14:12	0h RW/L	**FIFO_THRE:** Capture FIFO Threshold. It contains the number of valid data entries in the FIFO: NUM_DATA_ENTRIES = FIFO_THRE + 1 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
11	0h RW/L	**CAP_MODE:** Capture Block Mode. It selects the PhaseA event which triggers the FIFO to store the current QEPCNTR value 0 = Single edge 1 = Both edges It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
10:9	0h RW/L	**INDX_GATING:** Index Gating Select. It selects the state of PhaseA and PhaseB signals at which the index pulse will be gated 00 = PhaseA low and PhaseB low 01 = PhaseA low and PhaseB high 10 = PhaseA high and PhaseB low 11 = PhaseA high and PhaseB high It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
8	0h RW/L	**COUNT_RST_MODE:** Position Counter Reset Mode 0 = Position counter reset on index event 1 = Position counter reset on maximum position It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
7	0h RO	**Reserved**
6	0h RW/L	**OP_MODE:** Operating Mode 0 = Quadrature Encoder Peripheral (QEP) 1 = Capture Compare (CC) It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**SWPAB:** Phase A and Phase B Input Swap Select 0 = Phase A and Phase B inputs are not swapped 1 = Phase A and Phase B inputs are swapped It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
4	1h RW/L	**EDGE_INDX:** Edge selection of the Index input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
3	1h RW/L	**EDGE_B:** Edge selection of the PhaseB input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
2	1h RW/L	**EDGE_A:** Edge selection of the PhaseA input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
1	0h RW/L	**FLT_EN:** Noise Filters Enable 0 = Filters disabled 1 = Filters enabled It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
0	0h RW	**EN:** QEP/CC Enable 0 = QEP/CC disabled 1 = QEP/CC enabled

14.18.1.2 QEPFLT — Offset 48600004h

QEP Noise Filter Register

Type	Size	Offset	Default
MMIO	32 bit	48600004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW/L	**MAX_COUNT:** Noise Filter Maximum Count. It selects the maximum glitch width to remove in terms of peripheral clock cycles: PCLK_CYCLES = MAX_COUNT + 2 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.1.3 QEPCOUNT — Offset 48600008h

QEP Position Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48600008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**POS_COUNT:** Position Count Value. It stores the count value currently reached by the position counter. Disabling the peripheral will automatically clear its content.

14.18.1.4 QEPMAX — Offset 4860000Ch

QEP Maximum Position Register

Type	Size	Offset	Default
MMIO	32 bit	4860000Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/L	**MAX_COUNT:** Maximum Position Count. It defines the operating range for the position counter. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.1.5 QEPWDT — Offset 48600010h

QEP Watchdog Timer Register

Type	Size	Offset	Default
MMIO	32 bit	48600010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**TOP:** Watchdog Timer Timeout Period. When the WDT reaches this value, a dedicated interrupt is generated to flag a stall event. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.1.6 QEPCAPDIV — Offset 48600014h

QEP Capture Divider Register

Type	Size	Offset	Default
MMIO	32 bit	48600014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**CLK_DIV:** Clock Divider Value. It allows the clock to be divided as follows: 000 = clock divided by 1 001 = clock divided by 2 010 = clock divided by 4 011 = clock divided by 8 100 = clock divided by 16 101 = clock divided by 32 110 = clock divided by 64 111 = clock divided by 128 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.1.7 QEPCNTR — Offset 48600018h

QEP Capture Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48600018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CAP_COUNT:** Capture Count Value. It stores the count value currently reached by the free-running capture counter. Disabling the peripheral will automatically clear its content.

14.18.1.8 QEPCAPBUF — Offset 4860001Ch

QEP Capture Data Register

Type	Size	Offset	Default
MMIO	32 bit	4860001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** This is the register the processor reads from when retrieving bytes from FIFO

14.18.1.9 QEPINT_STAT — Offset 48600020h

QEP Raw Interrupt Status Register. Each bit in this register has a corresponding mask bit in the QEPINT_MASK register. These bits are cleared by writing '1' to the matching interrupt register field.

Type	Size	Offset	Default
MMIO	32 bit	48600020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C/V	**FIFOCRIT/QEP_PH_ERR_INTR :** In Capture mode, Capture Function Event FIFO Critical Interrupt. The number of entries in the Capture FIFO has reached the configured threshold level. In Encoder mode, this bit is set when phase error has occurred on the QEP inputs.
4	0h RW/1C/V	**FIFOENTRY:** Capture Function Event FIFO Entry Interrupt. An entry has been added to the 'Capture' FIFO.
3	0h RW/1C/V	**QEPDIR:** QEP Function Change Of Direction Detected Interrupt. The Quadrature Decoder has detected that the attached motor (or user dial device) has changed direction.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C/V	**QEPRST_UP:** QEPCOUNT Reset detect with forward count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
1	0h RW/1C/V	**QEPRST_DOWN:** QEPCOUNT Reset detect with reverse count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
0	0h RW/1C/V	**WDT:** Watchdog Timeout Interrupt. The Watchdog Timer value has reached the watchdog comparator value.

14.18.1.10 QEPINT_MASK — Offset 48600024h

QEP Interrupt Mask Register

Type	Size	Offset	Default
MMIO	32 bit	48600024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**FIFOCRIT:** This bit masks the FIFOCRIT interrupt bit from the QEPINT_STAT register
4	0h RW	**FIFOENTRY:** This bit masks the FIFOENTRY interrupt bit from the QEPINT_STAT register
3	0h RW	**QEPDIR:** This bit masks the QEPDIR interrupt bit from the QEPINT_STAT register
2	0h RW	**QEPRST_UP:** This bit masks the QEPRST_UP interrupt bit from the QEPINT_STAT register
1	0h RW	**QEPRST_DOWN:** This bit masks the QEPRST_DOWN interrupt bit from the QEPINT_STAT register
0	0h RW	**WDT:** This bit masks the WDT interrupt bit from the QEPINT_STAT register

14.18.2 QEP_1 Registers Summary

Table 14-38. Summary of QEP_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48602000h	4	QEPCON	0000001Ch
48602004h	4	QEPFLT	00000000h
48602008h	4	QEPCOUNT	00000000h
4860200Ch	4	QEPMAX	FFFFFFFFh
48602010h	4	QEPWDT	00000000h
48602014h	4	QEPCAPDIV	00000000h
48602018h	4	QEPCNTR	00000000h
4860201Ch	4	QEPCAPBUF	00000000h
48602020h	4	QEPINT_STAT	00000000h
48602024h	4	QEPINT_MASK	00000000h

14.18.2.1 QEPCON — Offset 48602000h

QEP Control Register. This register controls the QEP operation and provides status flags for the state of the QEP module

Type	Size	Offset	Default
MMIO	32 bit	48602000h	0000001Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**FIFO_EMPTY:** Capture FIFO Empty Status Flag. Set when the FIFO is empty
14:12	0h RW/L	**FIFO_THRE:** Capture FIFO Threshold. It contains the number of valid data entries in the FIFO: NUM_DATA_ENTRIES = FIFO_THRE + 1 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
11	0h RW/L	**CAP_MODE:** Capture Block Mode. It selects the PhaseA event which triggers the FIFO to store the current QEPCNTR value 0 = Single edge 1 = Both edges It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
10:9	0h RW/L	**INDX_GATING:** Index Gating Select. It selects the state of PhaseA and PhaseB signals at which the index pulse will be gated 00 = PhaseA low and PhaseB low 01 = PhaseA low and PhaseB high 10 = PhaseA high and PhaseB low 11 = PhaseA high and PhaseB high It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
8	0h RW/L	**COUNT_RST_MODE:** Position Counter Reset Mode 0 = Position counter reset on index event 1 = Position counter reset on maximum position It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
7	0h RO	**Reserved**
6	0h RW/L	**OP_MODE:** Operating Mode 0 = Quadrature Encoder Peripheral (QEP) 1 = Capture Compare (CC) It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
5	0h RW/L	**SWPAB:** Phase A and Phase B Input Swap Select 0 = Phase A and Phase B inputs are not swapped 1 = Phase A and Phase B inputs are swapped It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
4	1h RW/L	**EDGE_INDX:** Edge selection of the Index input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
3	1h RW/L	**EDGE_B:** Edge selection of the PhaseB input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**EDGE_A:** Edge selection of the PhaseA input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
1	0h RW/L	**FLT_EN:** Noise Filters Enable 0 = Filters disabled 1 = Filters enabled It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
0	0h RW	**EN:** QEP/CC Enable 0 = QEP/CC disabled 1 = QEP/CC enabled

14.18.2.2 QEPFLT — Offset 48602004h

QEP Noise Filter Register

Type	Size	Offset	Default
MMIO	32 bit	48602004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW/L	**MAX_COUNT:** Noise Filter Maximum Count. It selects the maximum glitch width to remove in terms of peripheral clock cycles: PCLK_CYCLES = MAX_COUNT + 2 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.2.3 QEPCOUNT — Offset 48602008h

QEP Position Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48602008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**POS_COUNT:** Position Count Value. It stores the count value currently reached by the position counter. Disabling the peripheral will automatically clear its content.

14.18.2.4 QEPMAX — Offset 4860200Ch

QEP Maximum Position Register

Type	Size	Offset	Default
MMIO	32 bit	4860200Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/L	**MAX_COUNT:** Maximum Position Count. It defines the operating range for the position counter. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.2.5 QEPWDT — Offset 48602010h

QEP Watchdog Timer Register

Type	Size	Offset	Default
MMIO	32 bit	48602010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**TOP:** Watchdog Timer Timeout Period. When the WDT reaches this value, a dedicated interrupt is generated to flag a stall event. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.2.6 QEPCAPDIV — Offset 48602014h

QEP Capture Divider Register

Type	Size	Offset	Default
MMIO	32 bit	48602014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**CLK_DIV:** Clock Divider Value. It allows the clock to be divided as follows: 000 = clock divided by 1 001 = clock divided by 2 010 = clock divided by 4 011 = clock divided by 8 100 = clock divided by 16 101 = clock divided by 32 110 = clock divided by 64 111 = clock divided by 128 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.2.7 QEPCNTR — Offset 48602018h

QEP Capture Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48602018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CAP_COUNT:** Capture Count Value. It stores the count value currently reached by the free-running capture counter. Disabling the peripheral will automatically clear its content.

14.18.2.8 QEPCAPBUF — Offset 4860201Ch

QEP Capture Data Register

Type	Size	Offset	Default
MMIO	32 bit	4860201Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** This is the register the processor reads from when retrieving bytes from FIFO

14.18.2.9 QEPINT_STAT — Offset 48602020h

QEP Raw Interrupt Status Register. Each bit in this register has a corresponding mask bit in the QEPINT_MASK register. These bits are cleared by writing '1' to the matching interrupt register field.

Type	Size	Offset	Default
MMIO	32 bit	48602020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C/V	**FIFOCRIT/QEP_PH_ERR_INTR:** In Capture mode, Capture Function Event FIFO Critical Interrupt. The number of entries in the Capture FIFO has reached the configured threshold level. In Encoder mode, this bit is set when phase error has occurred on the QEP inputs.
4	0h RW/1C/V	**FIFOENTRY:** Capture Function Event FIFO Entry Interrupt. An entry has been added to the 'Capture' FIFO.
3	0h RW/1C/V	**QEPDIR:** QEP Function Change Of Direction Detected Interrupt. The Quadrature Decoder has detected that the attached motor (or user dial device) has changed direction.
2	0h RW/1C/V	**QEPRST_UP:** QEPCOUNT Reset detect with forward count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
1	0h RW/1C/V	**QEPRST_DOWN:** QEPCOUNT Reset detect with reverse count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
0	0h RW/1C/V	**WDT:** Watchdog Timeout Interrupt. The Watchdog Timer value has reached the watchdog comparator value.

14.18.2.10 QEPINT_MASK — Offset 48602024h

QEP Interrupt Mask Register

Type	Size	Offset	Default
MMIO	32 bit	48602024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**FIFOCRIT:** This bit masks the FIFOCRIT interrupt bit from the QEPINT_STAT register
4	0h RW	**FIFOENTRY:** This bit masks the FIFOENTRY interrupt bit from the QEPINT_STAT register
3	0h RW	**QEPDIR:** This bit masks the QEPDIR interrupt bit from the QEPINT_STAT register
2	0h RW	**QEPRST_UP:** This bit masks the QEPRST_UP interrupt bit from the QEPINT_STAT register
1	0h RW	**QEPRST_DOWN:** This bit masks the QEPRST_DOWN interrupt bit from the QEPINT_STAT register
0	0h RW	**WDT:** This bit masks the WDT interrupt bit from the QEPINT_STAT register

14.18.3 QEP_2 Registers Summary

Table 14-39. Summary of QEP_2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48604000h	4	QEPCON	0000001Ch
48604004h	4	QEPFLT	00000000h
48604008h	4	QEPCOUNT	00000000h
4860400Ch	4	QEPMAX	FFFFFFFFh
48604010h	4	QEPWDT	00000000h
48604014h	4	QEPCAPDIV	00000000h
48604018h	4	QEPCNTR	00000000h
4860401Ch	4	QEPCAPBUF	00000000h
48604020h	4	QEPINT_STAT	00000000h
48604024h	4	QEPINT_MASK	00000000h

14.18.3.1 QEPCON — Offset 48604000h

QEP Control Register. This register controls the QEP operation and provides status flags for the state of the QEP module

Type	Size	Offset	Default
MMIO	32 bit	48604000h	0000001Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**FIFO_EMPTY:** Capture FIFO Empty Status Flag. Set when the FIFO is empty
14:12	0h RW/L	**FIFO_THRE:** Capture FIFO Threshold. It contains the number of valid data entries in the FIFO: NUM_DATA_ENTRIES = FIFO_THRE + 1 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
11	0h RW/L	**CAP_MODE:** Capture Block Mode. It selects the PhaseA event which triggers the FIFO to store the current QEPCNTR value 0 = Single edge 1 = Both edges It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
10:9	0h RW/L	**INDX_GATING:** Index Gating Select. It selects the state of PhaseA and PhaseB signals at which the index pulse will be gated 00 = PhaseA low and PhaseB low 01 = PhaseA low and PhaseB high 10 = PhaseA high and PhaseB low 11 = PhaseA high and PhaseB high It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
8	0h RW/L	**COUNT_RST_MODE:** Position Counter Reset Mode 0 = Position counter reset on index event 1 = Position counter reset on maximum position It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
7	0h RO	**Reserved**
6	0h RW/L	**OP_MODE:** Operating Mode 0 = Quadrature Encoder Peripheral (QEP) 1 = Capture Compare (CC) It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**SWPAB:** Phase A and Phase B Input Swap Select 0 = Phase A and Phase B inputs are not swapped 1 = Phase A and Phase B inputs are swapped It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
4	1h RW/L	**EDGE_INDX:** Edge selection of the Index input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
3	1h RW/L	**EDGE_B:** Edge selection of the PhaseB input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
2	1h RW/L	**EDGE_A:** Edge selection of the PhaseA input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
1	0h RW/L	**FLT_EN:** Noise Filters Enable 0 = Filters disabled 1 = Filters enabled It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
0	0h RW	**EN:** QEP/CC Enable 0 = QEP/CC disabled 1 = QEP/CC enabled

14.18.3.2 QEPFLT — Offset 48604004h

QEP Noise Filter Register

Type	Size	Offset	Default
MMIO	32 bit	48604004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW/L	**MAX_COUNT:** Noise Filter Maximum Count. It selects the maximum glitch width to remove in terms of peripheral clock cycles: PCLK_CYCLES = MAX_COUNT + 2 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.3.3 QEPCOUNT — Offset 48604008h

QEP Position Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48604008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**POS_COUNT:** Position Count Value. It stores the count value currently reached by the position counter. Disabling the peripheral will automatically clear its content.

14.18.3.4 QEPMAX — Offset 4860400Ch

QEP Maximum Position Register

Type	Size	Offset	Default
MMIO	32 bit	4860400Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/L	**MAX_COUNT:** Maximum Position Count. It defines the operating range for the position counter. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.3.5 QEPWDT — Offset 48604010h

QEP Watchdog Timer Register

Type	Size	Offset	Default
MMIO	32 bit	48604010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**TOP:** Watchdog Timer Timeout Period. When the WDT reaches this value, a dedicated interrupt is generated to flag a stall event. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.3.6 QEPCAPDIV — Offset 48604014h

QEP Capture Divider Register

Type	Size	Offset	Default
MMIO	32 bit	48604014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**CLK_DIV:** Clock Divider Value. It allows the clock to be divided as follows: 000 = clock divided by 1 001 = clock divided by 2 010 = clock divided by 4 011 = clock divided by 8 100 = clock divided by 16 101 = clock divided by 32 110 = clock divided by 64 111 = clock divided by 128 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.3.7 QEPCNTR — Offset 48604018h

QEP Capture Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48604018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CAP_COUNT:** Capture Count Value. It stores the count value currently reached by the free-running capture counter. Disabling the peripheral will automatically clear its content.

14.18.3.8 QEPCAPBUF — Offset 4860401Ch

QEP Capture Data Register

Type	Size	Offset	Default
MMIO	32 bit	4860401Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** This is the register the processor reads from when retrieving bytes from FIFO

14.18.3.9 QEPINT_STAT — Offset 48604020h

QEP Raw Interrupt Status Register. Each bit in this register has a corresponding mask bit in the QEPINT_MASK register. These bits are cleared by writing '1' to the matching interrupt register field.

Type	Size	Offset	Default
MMIO	32 bit	48604020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C/V	**FIFOCRIT/QEP_PH_ERR_INTR:** In Capture mode, Capture Function Event FIFO Critical Interrupt. The number of entries in the Capture FIFO has reached the configured threshold level. In Encoder mode, this bit is set when phase error has occurred on the QEP inputs.
4	0h RW/1C/V	**FIFOENTRY:** Capture Function Event FIFO Entry Interrupt. An entry has been added to the 'Capture' FIFO.
3	0h RW/1C/V	**QEPDIR:** QEP Function Change Of Direction Detected Interrupt. The Quadrature Decoder has detected that the attached motor (or user dial device) has changed direction.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C/V	**QEPRST_UP:** QEPCOUNT Reset detect with forward count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
1	0h RW/1C/V	**QEPRST_DOWN:** QEPCOUNT Reset detect with reverse count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
0	0h RW/1C/V	**WDT:** Watchdog Timeout Interrupt. The Watchdog Timer value has reached the watchdog comparator value.

14.18.3.10 QEPINT_MASK — Offset 48604024h

QEP Interrupt Mask Register

Type	Size	Offset	Default
MMIO	32 bit	48604024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**FIFOCRIT:** This bit masks the FIFOCRIT interrupt bit from the QEPINT_STAT register
4	0h RW	**FIFOENTRY:** This bit masks the FIFOENTRY interrupt bit from the QEPINT_STAT register
3	0h RW	**QEPDIR:** This bit masks the QEPDIR interrupt bit from the QEPINT_STAT register
2	0h RW	**QEPRST_UP:** This bit masks the QEPRST_UP interrupt bit from the QEPINT_STAT register
1	0h RW	**QEPRST_DOWN:** This bit masks the QEPRST_DOWN interrupt bit from the QEPINT_STAT register
0	0h RW	**WDT:** This bit masks the WDT interrupt bit from the QEPINT_STAT register

14.18.4 QEP_3 Registers Summary

Table 14-40. Summary of QEP_3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
48606000h	4	QEPCON	0000001Ch
48606004h	4	QEPFLT	00000000h
48606008h	4	QEPCOUNT	00000000h
4860600Ch	4	QEPMAX	FFFFFFFFh
48606010h	4	QEPWDT	00000000h
48606014h	4	QEPCAPDIV	00000000h
48606018h	4	QEPCNTR	00000000h
4860601Ch	4	QEPCAPBUF	00000000h
48606020h	4	QEPINT_STAT	00000000h
48606024h	4	QEPINT_MASK	00000000h

14.18.4.1 QEPCON — Offset 48606000h

QEP Control Register. This register controls the QEP operation and provides status flags for the state of the QEP module

Type	Size	Offset	Default
MMIO	32 bit	48606000h	0000001Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**FIFO_EMPTY:** Capture FIFO Empty Status Flag. Set when the FIFO is empty
14:12	0h RW/L	**FIFO_THRE:** Capture FIFO Threshold. It contains the number of valid data entries in the FIFO: NUM_DATA_ENTRIES = FIFO_THRE + 1 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
11	0h RW/L	**CAP_MODE:** Capture Block Mode. It selects the PhaseA event which triggers the FIFO to store the current QEPCNTR value 0 = Single edge 1 = Both edges It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
10:9	0h RW/L	**INDX_GATING:** Index Gating Select. It selects the state of PhaseA and PhaseB signals at which the index pulse will be gated 00 = PhaseA low and PhaseB low 01 = PhaseA low and PhaseB high 10 = PhaseA high and PhaseB low 11 = PhaseA high and PhaseB high It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
8	0h RW/L	**COUNT_RST_MODE:** Position Counter Reset Mode 0 = Position counter reset on index event 1 = Position counter reset on maximum position It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
7	0h RO	**Reserved**
6	0h RW/L	**OP_MODE:** Operating Mode 0 = Quadrature Encoder Peripheral (QEP) 1 = Capture Compare (CC) It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
5	0h RW/L	**SWPAB:** Phase A and Phase B Input Swap Select 0 = Phase A and Phase B inputs are not swapped 1 = Phase A and Phase B inputs are swapped It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
4	1h RW/L	**EDGE_INDX:** Edge selection of the Index input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
3	1h RW/L	**EDGE_B:** Edge selection of the PhaseB input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**EDGE_A:** Edge selection of the PhaseA input signal 0 = Falling edge 1 = Rising edge It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
1	0h RW/L	**FLT_EN:** Noise Filters Enable 0 = Filters disabled 1 = Filters enabled It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN
0	0h RW	**EN:** QEP/CC Enable 0 = QEP/CC disabled 1 = QEP/CC enabled

14.18.4.2 QEPFLT — Offset 48606004h

QEP Noise Filter Register

Type	Size	Offset	Default
MMIO	32 bit	48606004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW/L	**MAX_COUNT:** Noise Filter Maximum Count. It selects the maximum glitch width to remove in terms of peripheral clock cycles: PCLK_CYCLES = MAX_COUNT + 2 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.4.3 QEPCOUNT — Offset 48606008h

QEP Position Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48606008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**POS_COUNT:** Position Count Value. It stores the count value currently reached by the position counter. Disabling the peripheral will automatically clear its content.

14.18.4.4 QEPMAX — Offset 4860600Ch

QEP Maximum Position Register

Type	Size	Offset	Default
MMIO	32 bit	4860600Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/L	**MAX_COUNT:** Maximum Position Count. It defines the operating range for the position counter. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.4.5 QEPWDT — Offset 48606010h

QEP Watchdog Timer Register

Type	Size	Offset	Default
MMIO	32 bit	48606010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/L	**TOP:** Watchdog Timer Timeout Period. When the WDT reaches this value, a dedicated interrupt is generated to flag a stall event. It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.4.6 QEPCAPDIV — Offset 48606014h

QEP Capture Divider Register

Type	Size	Offset	Default
MMIO	32 bit	48606014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**CLK_DIV:** Clock Divider Value. It allows the clock to be divided as follows: 000 = clock divided by 1 001 = clock divided by 2 010 = clock divided by 4 011 = clock divided by 8 100 = clock divided by 16 101 = clock divided by 32 110 = clock divided by 64 111 = clock divided by 128 It is writeable by the processor only when the peripheral is disabled. **Locked by:** QEPCON.EN

14.18.4.7 QEPCNTR — Offset 48606018h

QEP Capture Counter Register

Type	Size	Offset	Default
MMIO	32 bit	48606018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CAP_COUNT:** Capture Count Value. It stores the count value currently reached by the free-running capture counter. Disabling the peripheral will automatically clear its content.

14.18.4.8 QEPCAPBUF — Offset 4860601Ch

QEP Capture Data Register

Type	Size	Offset	Default
MMIO	32 bit	4860601Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** This is the register the processor reads from when retrieving bytes from FIFO

14.18.4.9 QEPINT_STAT — Offset 48606020h

QEP Raw Interrupt Status Register. Each bit in this register has a corresponding mask bit in the QEPINT_MASK register. These bits are cleared by writing '1' to the matching interrupt register field.

Type	Size	Offset	Default
MMIO	32 bit	48606020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW/1C/V	**FIFOCRIT/QEP_PH_ERR_INTR:** In Capture mode, Capture Function Event FIFO Critical Interrupt. The number of entries in the Capture FIFO has reached the configured threshold level. In Encoder mode, this bit is set when phase error has occurred on the QEP inputs.
4	0h RW/1C/V	**FIFOENTRY:** Capture Function Event FIFO Entry Interrupt. An entry has been added to the 'Capture' FIFO.
3	0h RW/1C/V	**QEPDIR:** QEP Function Change Of Direction Detected Interrupt. The Quadrature Decoder has detected that the attached motor (or user dial device) has changed direction.
2	0h RW/1C/V	**QEPRST_UP:** QEPCOUNT Reset detect with forward count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
1	0h RW/1C/V	**QEPRST_DOWN:** QEPCOUNT Reset detect with reverse count direction Interrupt; The QEPCOUNT can be reset by one of 2 configurable methods: Index Input detect event or comparator match event
0	0h RW/1C/V	**WDT:** Watchdog Timeout Interrupt. The Watchdog Timer value has reached the watchdog comparator value.

14.18.4.10 QEPINT_MASK — Offset 48606024h

QEP Interrupt Mask Register

Type	Size	Offset	Default
MMIO	32 bit	48606024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**FIFOCRIT:** This bit masks the FIFOCRIT interrupt bit from the QEPINT_STAT register
4	0h RW	**FIFOENTRY:** This bit masks the FIFOENTRY interrupt bit from the QEPINT_STAT register
3	0h RW	**QEPDIR:** This bit masks the QEPDIR interrupt bit from the QEPINT_STAT register
2	0h RW	**QEPRST_UP:** This bit masks the QEPRST_UP interrupt bit from the QEPINT_STAT register
1	0h RW	**QEPRST_DOWN:** This bit masks the QEPRST_DOWN interrupt bit from the QEPINT_STAT register
0	0h RW	**WDT:** This bit masks the WDT interrupt bit from the QEPINT_STAT register

14.19 DMA MISC Registers

There are three DMA MISC registers:-

- DMA_0 MISC Registers
- DMA_1 MISC Registers
- DMA_2 MISC Registers

DMA MISC Registers	Address Offset	Table
DMA_0 MISC	50101000h - 50102000h	Table 14-41
DMA_1 MISC	50105000h - 50106000h	Table 14-42
DMA_2 MISC	50109000h - 5010A000h	Table 14-43

14.19.1 DMA_0 MISC Registers Summary

Table 14-41. Summary of DMA_0 MISC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50101000h	4	DMA ControlChannel0 (DMA_CTL_CH0)	00000000h
50101004h	4	DMA ControlChannel1 (DMA_CTL_CH1)	00000000h
50101008h	4	DMA ControlChannel2 (DMA_CTL_CH2)	00000000h
5010100Ch	4	DMA ControlChannel3 (DMA_CTL_CH3)	00000000h
50101010h	4	DMA ControlChannel4 (DMA_CTL_CH4)	00000000h
50101014h	4	DMA ControlChannel5 (DMA_CTL_CH5)	00000000h
50101018h	4	DMA ControlChannel6 (DMA_CTL_CH6)	00000000h
5010101Ch	4	DMA ControlChannel7 (DMA_CTL_CH7)	00000000h
50101100h	4	DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0)	00000000h
50101104h	4	DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1)	00000000h
50101108h	4	DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2)	00000000h
5010110Ch	4	DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3)	00000000h
50101110h	4	DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4)	00000000h
50101114h	4	DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5)	00000000h
50101118h	4	DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6)	00000000h
5010111Ch	4	DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7)	00000000h
50101200h	4	DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0)	00000000h
50101204h	4	DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1)	00000000h
50101208h	4	DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2)	00000000h
5010120Ch	4	DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3)	00000000h
50101210h	4	DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4)	00000000h
50101214h	4	DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5)	00000000h
50101218h	4	DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6)	00000000h
5010121Ch	4	DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7)	00000000h
50101300h	4	DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0)	00000000h
50101304h	4	DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1)	00000000h
50101308h	4	DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5010130Ch	4	DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3)	00000000h
50101310h	4	DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4)	00000000h
50101314h	4	DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5)	00000000h
50101318h	4	DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6)	00000000h
5010131Ch	4	DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7)	00000000h
50101400h	4	DMA Channel Id Config (DMA_REGACCESS_CHID_CFG)	00000000h
50101404h	4	DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP)	00000000h
50101410h	4	D0i3 Control (D0I3C)	00000008h
50101414h	4	Clock Gating And Soft Reset (CGSR)	00000000h
50101418h	4	DMA Interrupt Enable (DMA_INT_EN)	00000000h
50102000h	4	DMA VMM Mask (DMA_VMM_MASK)	00000000h

14.19.1.1 DMA ControlChannel0 (DMA_CTL_CH0) — Offset 50101000h

DMA Control register channel0.

Type	Size	Offset	Default
MMIO	32 bit	50101000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel0 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel0 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.2 DMA ControlChannel1 (DMA_CTL_CH1) — Offset 50101004h

DMA Control register channel1.

Type	Size	Offset	Default
MMIO	32 bit	50101004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port.When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port.When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel1 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel1 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel1. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.3 DMA ControlChannel2 (DMA_CTL_CH2) — Offset 50101008h

DMA Control register channel2.

Type	Size	Offset	Default
MMIO	32 bit	50101008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel2 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel2 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel2. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.4 DMA ControlChannel3 (DMA_CTL_CH3) — Offset 5010100Ch

DMA Control register channel3.

Type	Size	Offset	Default
MMIO	32 bit	5010100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel3 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel3 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel3. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.5 DMA ControlChannel4 (DMA_CTL_CH4) — Offset 50101010h

DMA Control register channel4.

Type	Size	Offset	Default
MMIO	32 bit	50101010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel4 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel4 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel4. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.6 DMA ControlChannel5 (DMA_CTL_CH5) — Offset 50101014h

DMA Control register channel5.

Type	Size	Offset	Default
MMIO	32 bit	50101014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel5 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel5 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel5. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.7 DMA ControlChannel6 (DMA_CTL_CH6) — Offset 50101018h

DMA Control register channel6.

Type	Size	Offset	Default
MMIO	32 bit	50101018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel6 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel6 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel6. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.8 DMA ControlChannel7 (DMA_CTL_CH7) — Offset 5010101Ch

DMA Control register channel7.

Type	Size	Offset	Default
MMIO	32 bit	5010101Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel7 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel7 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel7. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.1.9 DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0) — Offset 50101100h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	50101100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

14.19.1.10 DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1) — Offset 50101104h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.11 DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2) — Offset 50101108h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.12 DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3) — Offset 5010110Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.13 DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4) — Offset 50101110h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.14 DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5) — Offset 50101114h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.15 DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6) — Offset 50101118h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.16 DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7) — Offset 5010111Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.17 DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0) — Offset 50101200h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.18 DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1) — Offset 50101204h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.19 DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2) — Offset 50101208h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.20 DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3) — Offset 5010120Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.21 DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4) — Offset 50101210h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.22 DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5) — Offset 50101214h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.23 DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6) — Offset 50101218h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.24 DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7) — Offset 5010121Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50101100h.

14.19.1.25 DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0) — Offset 50101300h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 0.

Type	Size	Offset	Default
MMIO	32 bit	50101300h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** DeviceId of Peripheral to be selected for HW Handshake.

14.19.1.26 DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1) — Offset 50101304h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 1.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.27 DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2) — Offset 50101308h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 2.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.28 DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3) — Offset 5010130Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 3.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.29 DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4) — Offset 50101310h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 4.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.30 DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5) — Offset 50101314h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 5.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.31 DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6) — Offset 50101318h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 6.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.32 DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7) — Offset 5010131Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 7.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50101300h.

14.19.1.33 DMA Channel Id Config (DMA_REGACCESS_CHID_CFG) — Offset 50101400h

This reg is used to program the Mreqinfo fo the DMA channel to be programmed next by FW.

Type	Size	Offset	Default
MMIO	32 bit	50101400h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**CHID_CFG:** Register access MREQINFO DMA channel id configuration.

14.19.1.34 DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP) — Offset 50101404h

Sresp register for SRAM_base/OCP logic selection at DMA.

Type	Size	Offset	Default
MMIO	32 bit	50101404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:1	000000h RW/1C	**Peripheral BAR Remap Error Status (PER_BAR_REMAP_ERR):** This Error status bit is set on the peripheral BAR remap error and cleared when '1' is written to it. Bit 1-8 of this register indicate BAR remap error for the peripherals I2C0-7, Bits 9-14 indicate for UART0-5, bits 15-18 indicate for SPI0-3, Bits 19-20 inidicate for I2S0-1 resp. and Bit 21 is reserved.
0	0h RW/1C	**Sresp Error Status Bit (ECC_ERR_SRESP):** This Error status bit is set on the Rd/Wr Sresp error on the DMA Rd/Wr ports and cleared when '1' is written to it.

14.19.1.35 D0i3 Control (D0I3C) — Offset 50101410h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit: 1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost. 2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit. 3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW. 4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear). The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following: 1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1. 2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied. 3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	50101410h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RW/1C	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

14.19.1.36 Clock Gating And Soft Reset (CGSR) — Offset 50101414h

This register is used to Clock gate or soft reset an IP by Host/Remote Host.

Type	Size	Offset	Default
MMIO	32 bit	50101414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

14.19.1.37 DMA Interrupt Enable (DMA_INT_EN) — Offset 50101418h

This register is used to enable the DMA combined interrupt for VC0/VC1.

Type	Size	Offset	Default
MMIO	32 bit	50101418h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA Combined Interrupt For VC0/1 (DMA_COMB_INT_EN):** When set, enables the DMA combined interrupt to be generated on VC1 lines to MSI gen. When reset , enables the DMA Combined interrupt to be generated on VC0 lines to MSI gen.

14.19.1.38 DMA VMM Mask (DMA_VMM_MASK) — Offset 50102000h

This register is used to program the VMM Mask for each peripheral.

Type	Size	Offset	Default
MMIO	32 bit	50102000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Peripheral VMM Mask (PER_VMM_MASK):** When set, enables the VMM Mask for the peripheral. When reset, disables the VMM Mask for the peripheral. Bit 0-7 correspond to I2C0-7, Bits 8-13 correspond to UART0-5, bits 14-17 correspond to SPI0-3, Bits 18-19 correspond to I2S0-1 resp. and Bit 20 is reserved.

14.19.2 DMA_1 MISC Registers Summary

Table 14-42. Summary of DMA_1 MISC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50105000h	4	DMA ControlChannel0 (DMA_CTL_CH0)	00000000h
50105004h	4	DMA ControlChannel1 (DMA_CTL_CH1)	00000000h
50105008h	4	DMA ControlChannel2 (DMA_CTL_CH2)	00000000h
5010500Ch	4	DMA ControlChannel3 (DMA_CTL_CH3)	00000000h
50105010h	4	DMA ControlChannel4 (DMA_CTL_CH4)	00000000h
50105014h	4	DMA ControlChannel5 (DMA_CTL_CH5)	00000000h
50105018h	4	DMA ControlChannel6 (DMA_CTL_CH6)	00000000h
5010501Ch	4	DMA ControlChannel7 (DMA_CTL_CH7)	00000000h
50105100h	4	DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0)	00000000h
50105104h	4	DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1)	00000000h
50105108h	4	DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2)	00000000h
5010510Ch	4	DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3)	00000000h
50105110h	4	DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4)	00000000h
50105114h	4	DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5)	00000000h
50105118h	4	DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6)	00000000h
5010511Ch	4	DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7)	00000000h
50105200h	4	DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0)	00000000h
50105204h	4	DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1)	00000000h
50105208h	4	DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2)	00000000h
5010520Ch	4	DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3)	00000000h
50105210h	4	DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4)	00000000h
50105214h	4	DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5)	00000000h
50105218h	4	DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6)	00000000h
5010521Ch	4	DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7)	00000000h
50105300h	4	DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0)	00000000h
50105304h	4	DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1)	00000000h
50105308h	4	DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5010530Ch	4	DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3)	00000000h
50105310h	4	DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4)	00000000h
50105314h	4	DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5)	00000000h
50105318h	4	DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6)	00000000h
5010531Ch	4	DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7)	00000000h
50105400h	4	DMA Channel Id Config (DMA_REGACCESS_CHID_CFG)	00000000h
50105404h	4	DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP)	00000000h
50105410h	4	D0i3 Control (D0I3C)	00000008h
50105414h	4	Clock Gating And Soft Reset (CGSR)	00000000h
50105418h	4	DMA Interrupt Enable (DMA_INT_EN)	00000000h
50106000h	4	DMA VMM Mask (DMA_VMM_MASK)	00000000h

14.19.2.1 DMA ControlChannel0 (DMA_CTL_CH0) — Offset 50105000h

DMA Control register channel0.

Type	Size	Offset	Default
MMIO	32 bit	50105000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel0 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel0 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.2 DMA ControlChannel1 (DMA_CTL_CH1) — Offset 50105004h

DMA Control register channel1.

Type	Size	Offset	Default
MMIO	32 bit	50105004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port.When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port.When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel1 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel1 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel1. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.3 DMA ControlChannel2 (DMA_CTL_CH2) — Offset 50105008h

DMA Control register channel2.

Type	Size	Offset	Default
MMIO	32 bit	50105008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel2 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel2 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel2. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.4 DMA ControlChannel3 (DMA_CTL_CH3) — Offset 5010500Ch

DMA Control register channel3.

Type	Size	Offset	Default
MMIO	32 bit	5010500Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel3 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel3 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel3. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.5 DMA ControlChannel4 (DMA_CTL_CH4) — Offset 50105010h

DMA Control register channel4.

Type	Size	Offset	Default
MMIO	32 bit	50105010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel4 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel4 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel4. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.6 DMA ControlChannel5 (DMA_CTL_CH5) — Offset 50105014h

DMA Control register channel5.

Type	Size	Offset	Default
MMIO	32 bit	50105014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel5 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel5 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel5. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.7 DMA ControlChannel6 (DMA_CTL_CH6) — Offset 50105018h

DMA Control register channel6.

Type	Size	Offset	Default
MMIO	32 bit	50105018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel6 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel6 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel6. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.8 DMA ControlChannel7 (DMA_CTL_CH7) — Offset 5010501Ch

DMA Control register channel7.

Type	Size	Offset	Default
MMIO	32 bit	5010501Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel7 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel7 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel7. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.2.9 DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0) — Offset 50105100h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	50105100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

14.19.2.10 DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1) — Offset 50105104h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.11 DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2) — Offset 50105108h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.12 DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3) — Offset 5010510Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.13 DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4) — Offset 50105110h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.14 DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5) — Offset 50105114h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.15 DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6) — Offset 50105118h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.16 DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7) — Offset 5010511Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.17 DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0) — Offset 50105200h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.18 DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1) — Offset 50105204h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.19 DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2) — Offset 50105208h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.20 DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3) — Offset 5010520Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.21 DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4) — Offset 50105210h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.22 DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5) — Offset 50105214h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.23 DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6) — Offset 50105218h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.24 DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7) — Offset 5010521Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50105100h.

14.19.2.25 DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0) — Offset 50105300h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 0.

Type	Size	Offset	Default
MMIO	32 bit	50105300h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** DeviceId of Peripheral to be selected for HW Handshake.

14.19.2.26 DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1) — Offset 50105304h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 1.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.27 DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2) — Offset 50105308h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 2.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.28 DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3) — Offset 5010530Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 3.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.29 DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4) — Offset 50105310h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 4.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.30 DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5) — Offset 50105314h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 5.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.31 DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6) — Offset 50105318h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 6.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.32 DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7) — Offset 5010531Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 7.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50105300h.

14.19.2.33 DMA Channel Id Config (DMA_REGACCESS_CHID_CFG) — Offset 50105400h

This reg is used to program the Mreqinfo fo the DMA channel to be programmed next by FW.

Type	Size	Offset	Default
MMIO	32 bit	50105400h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**CHID_CFG:** Register access MREQINFO DMA channel id configuration.

14.19.2.34 DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP) — Offset 50105404h

Sresp register for SRAM_base/OCP logic selection at DMA.

Type	Size	Offset	Default
MMIO	32 bit	50105404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:1	000000h RW/1C	**Peripheral BAR Remap Error Status (PER_BAR_REMAP_ERR):** This Error status bit is set on the peripheral BAR remap error and cleared when '1' is written to it. Bit 1-8 of this register indicate BAR remap error for the peripherals I2C0-7, Bits 9-14 indicate for UART0-5, bits 15-18 indicate for SPI0-3, Bits 19-20 inidicate for I2S0-1 resp. and Bit 21 is reserved.
0	0h RW/1C	**Sresp Error Status Bit (ECC_ERR_SRESP):** This Error status bit is set on the Rd/Wr Sresp error on the DMA Rd/Wr ports and cleared when '1' is written to it.

14.19.2.35 D0i3 Control (D0I3C) — Offset 50105410h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit: 1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost. 2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit. 3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW. 4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear). The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following: 1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1. 2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied. 3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	50105410h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RW/1C	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

14.19.2.36 Clock Gating And Soft Reset (CGSR) — Offset 50105414h

This register is used to Clock gate or soft reset an IP by Host/Remote Host.

Type	Size	Offset	Default
MMIO	32 bit	50105414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

14.19.2.37 DMA Interrupt Enable (DMA_INT_EN) — Offset 50105418h

This register is used to enable the DMA combined interrupt for VC0/VC1.

Type	Size	Offset	Default
MMIO	32 bit	50105418h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA Combined Interrupt For VC0/1 (DMA_COMB_INT_EN):** When set, enables the DMA combined interrupt to be generated on VC1 lines to MSI gen. When reset , enables the DMA Combined interrupt to be generated on VC0 lines to MSI gen.

14.19.2.38 DMA VMM Mask (DMA_VMM_MASK) — Offset 50106000h

This register is used to program the VMM Mask for each peripheral.

Type	Size	Offset	Default
MMIO	32 bit	50106000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Peripheral VMM Mask (PER_VMM_MASK):** When set, enables the VMM Mask for the peripheral. When reset, disables the VMM Mask for the peripheral. Bit 0-7 correspond to I2C0-7, Bits 8-13 correspond to UART0-5, bits 14-17 correspond to SPI0-3, Bits 18-19 correspond to I2S0-1 resp. and Bit 20 is reserved.

14.19.3 DMA_2 MISC Registers Summary

Table 14-43. Summary of DMA_2 MISC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50109000h	4	DMA ControlChannel0 (DMA_CTL_CH0)	00000000h
50109004h	4	DMA ControlChannel1 (DMA_CTL_CH1)	00000000h
50109008h	4	DMA ControlChannel2 (DMA_CTL_CH2)	00000000h
5010900Ch	4	DMA ControlChannel3 (DMA_CTL_CH3)	00000000h
50109010h	4	DMA ControlChannel4 (DMA_CTL_CH4)	00000000h
50109014h	4	DMA ControlChannel5 (DMA_CTL_CH5)	00000000h
50109018h	4	DMA ControlChannel6 (DMA_CTL_CH6)	00000000h
5010901Ch	4	DMA ControlChannel7 (DMA_CTL_CH7)	00000000h
50109100h	4	DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0)	00000000h
50109104h	4	DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1)	00000000h
50109108h	4	DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2)	00000000h
5010910Ch	4	DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3)	00000000h
50109110h	4	DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4)	00000000h
50109114h	4	DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5)	00000000h
50109118h	4	DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6)	00000000h
5010911Ch	4	DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7)	00000000h
50109200h	4	DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0)	00000000h
50109204h	4	DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1)	00000000h
50109208h	4	DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2)	00000000h
5010920Ch	4	DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3)	00000000h
50109210h	4	DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4)	00000000h
50109214h	4	DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5)	00000000h
50109218h	4	DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6)	00000000h
5010921Ch	4	DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7)	00000000h
50109300h	4	DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0)	00000000h
50109304h	4	DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1)	00000000h
50109308h	4	DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5010930Ch	4	DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3)	00000000h
50109310h	4	DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4)	00000000h
50109314h	4	DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5)	00000000h
50109318h	4	DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6)	00000000h
5010931Ch	4	DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7)	00000000h
50109400h	4	DMA Channel Id Config (DMA_REGACCESS_CHID_CFG)	00000000h
50109404h	4	DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP)	00000000h
50109410h	4	D0i3 Control (D0I3C)	00000008h
50109414h	4	Clock Gating And Soft Reset (CGSR)	00000000h
50109418h	4	DMA Interrupt Enable (DMA_INT_EN)	00000000h
5010A000h	4	DMA VMM Mask (DMA_VMM_MASK)	00000000h

14.19.3.1 DMA ControlChannel0 (DMA_CTL_CH0) — Offset 50109000h

DMA Control register channel0.

Type	Size	Offset	Default
MMIO	32 bit	50109000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel0 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel0 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.2 DMA ControlChannel1 (DMA_CTL_CH1) — Offset 50109004h

DMA Control register channel1.

Type	Size	Offset	Default
MMIO	32 bit	50109004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel1 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel1 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel1. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.3 DMA ControlChannel2 (DMA_CTL_CH2) — Offset 50109008h

DMA Control register channel2.

Type	Size	Offset	Default
MMIO	32 bit	50109008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel2 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel2 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel2. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.4 DMA ControlChannel3 (DMA_CTL_CH3) — Offset 5010900Ch

DMA Control register channel3.

Type	Size	Offset	Default
MMIO	32 bit	5010900Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel3 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel3 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel3. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.5 DMA ControlChannel4 (DMA_CTL_CH4) — Offset 50109010h

DMA Control register channel4.

Type	Size	Offset	Default
MMIO	32 bit	50109010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel4 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel4 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel4. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.6 DMA ControlChannel5 (DMA_CTL_CH5) — Offset 50109014h

DMA Control register channel5.

Type	Size	Offset	Default
MMIO	32 bit	50109014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel5 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel5 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel5. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.7 DMA ControlChannel6 (DMA_CTL_CH6) — Offset 50109018h

DMA Control register channel6.

Type	Size	Offset	Default
MMIO	32 bit	50109018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel6 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel6 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel6. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.8 DMA ControlChannel7 (DMA_CTL_CH7) — Offset 5010901Ch

DMA Control register channel7.

Type	Size	Offset	Default
MMIO	32 bit	5010901Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RW	**Write Root Space (WR_RS):** Root Space attribute for DMA channel7 writes on IOSF. The read value of these bits will be 00 when the DMA is host owned.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Read Root Space (RD_RS):** Root Space attribute for DMA channel7 reads on IOSF. The read value of these bits will be 00 when the DMA is host owned.
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel7. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM).

14.19.3.9 DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0) — Offset 50109100h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	50109100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

14.19.3.10 DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1) — Offset 50109104h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.11 DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2) — Offset 50109108h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.12 DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3) — Offset 5010910Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.13 DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4) — Offset 50109110h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.14 DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5) — Offset 50109114h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.15 DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6) — Offset 50109118h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.16 DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7) — Offset 5010911Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.17 DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0) — Offset 50109200h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.18 DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1) — Offset 50109204h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.19 DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2) — Offset 50109208h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.20 DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3) — Offset 5010920Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.21 DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4) — Offset 50109210h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.22 DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5) — Offset 50109214h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.23 DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6) — Offset 50109218h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.24 DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7) — Offset 5010921Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50109100h.

14.19.3.25 DMA Crossbar HW Handshake Interface Select Channel 0 (DMA_XBAR_SEL0) — Offset 50109300h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 0.

Type	Size	Offset	Default
MMIO	32 bit	50109300h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**RX TX Mode (RX_TX):** 0 Selects Peripheral RX HW Handshake interface, 1 Selects Peripheral TX HW Handshake interface.
15:0	0000h RW	**Device ID (DEVID):** DeviceId of Peripheral to be selected for HW Handshake.

14.19.3.26 DMA Crossbar HW Handshake Interface Select Channel 1 (DMA_XBAR_SEL1) — Offset 50109304h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 1.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.27 DMA Crossbar HW Handshake Interface Select Channel 2 (DMA_XBAR_SEL2) — Offset 50109308h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 2.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.28 DMA Crossbar HW Handshake Interface Select Channel 3 (DMA_XBAR_SEL3) — Offset 5010930Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 3.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.29 DMA Crossbar HW Handshake Interface Select Channel 4 (DMA_XBAR_SEL4) — Offset 50109310h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 4.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.30 DMA Crossbar HW Handshake Interface Select Channel 5 (DMA_XBAR_SEL5) — Offset 50109314h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 5.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.31 DMA Crossbar HW Handshake Interface Select Channel 6 (DMA_XBAR_SEL6) — Offset 50109318h

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 6.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.32 DMA Crossbar HW Handshake Interface Select Channel 7 (DMA_XBAR_SEL7) — Offset 5010931Ch

This register is used to program the DMA Hardware Handshake crossbar to route the peripheral lines to DMA channel 7.

Note: Bit definitions are the same as DMA_XBAR_SEL0, offset 50109300h.

14.19.3.33 DMA Channel Id Config (DMA_REGACCESS_CHID_CFG) — Offset 50109400h

This reg is used to program the Mreqinfo fo the DMA channel to be programmed next by FW.

Type	Size	Offset	Default
MMIO	32 bit	50109400h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW	**CHID_CFG:** Register access MREQINFO DMA channel id configuration.

14.19.3.34 DMA ECC Error Sresp Error Logging Reg (DMA_ECC_ERR_SRESP) — Offset 50109404h

Sresp register for SRAM_base/OCP logic selection at DMA.

Type	Size	Offset	Default
MMIO	32 bit	50109404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:1	000000h RW/1C	**Peripheral BAR Remap Error Status (PER_BAR_REMAP_ERR):** This Error status bit is set on the peripheral BAR remap error and cleared when '1' is written to it. Bit 1-8 of this register indicate BAR remap error for the peripherals I2C0-7, Bits 9-14 indicate for UART0-5, bits 15-18 indicate for SPI0-3, Bits 19-20 inidicate for I2S0-1 resp. and Bit 21 is reserved.
0	0h RW/1C	**Sresp Error Status Bit (ECC_ERR_SRESP):** This Error status bit is set on the Rd/Wr Sresp error on the DMA Rd/Wr ports and cleared when '1' is written to it.

14.19.3.35 D0i3 Control (D0I3C) — Offset 50109410h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are yet to be done) The description below also includes the type of access expected for the ISH FW for each configuration bit: 1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost. 2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit. 3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW. 4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear). The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following: 1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1. 2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied. 3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	50109410h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RW/1C	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

14.19.3.36 Clock Gating And Soft Reset (CGSR) — Offset 50109414h

This register is used to Clock gate or soft reset an IP by Host/Remote Host.

Type	Size	Offset	Default
MMIO	32 bit	50109414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Idle Indication To Host (IDLE):** IP IDLE indication.
30:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Enable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reset (SR):** Setting this bit to 1 resets the IP.

14.19.3.37 DMA Interrupt Enable (DMA_INT_EN) — Offset 50109418h

This register is used to enable the DMA combined interrupt for VC0/VC1.

Type	Size	Offset	Default
MMIO	32 bit	50109418h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**DMA Combined Interrupt For VC0/1 (DMA_COMB_INT_EN):** When set, enables the DMA combined interrupt to be generated on VC1 lines to MSI gen. When reset , enables the DMA Combined interrupt to be generated on VC0 lines to MSI gen.

14.19.3.38 DMA VMM Mask (DMA_VMM_MASK) — Offset 5010A000h

This register is used to program the VMM Mask for each peripheral.

Type	Size	Offset	Default
MMIO	32 bit	5010A000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Peripheral VMM Mask (PER_VMM_MASK):** When set, enables the VMM Mask for the peripheral. When reset, disables the VMM Mask for the peripheral. Bit 0-7 correspond to I2C0-7, Bits 8-13 correspond to UART0-5, bits 14-17 correspond to SPI0-3, Bits 18-19 correspond to I2S0-1 resp. and Bit 20 is reserved.

14.20 GbE TSN Interface Registers

There are two GbE TSN Interface registers:-

- GbE_0 TSN Registers
- GbE_1 TSN Registers

Each of GbE TSN register will consist of GbE TSN MISC registers.

GbE TSN Registers	Address Offset	Table
GbE_0 TSN	50200000h - 502014ECh	Table 14-44
GbE_0 TSN MISC	50210000h - 50210500h	Table 14-45
GbE_1 TSN	50220000h - 502214ECh	Table 14-46
GbE_1 TSN MISC	50230000h - 50230500h	Table 14-47

14.20.1 GbE_0 TSN Registers Summary

Table 14-44. Summary of GbE_0 TSN Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200000h	4	MAC_CONFIGURATION	00000000h
50200004h	4	MAC_EXT_CONFIGURATION	00000000h
50200008h	4	MAC_PACKET_FILTER	00000000h
5020000Ch	4	MAC_WATCHDOG_TIMEOUT	00000000h
50200010h	4	MAC_HASH_TABLE_REG0	00000000h
50200014h	4	MAC_HASH_TABLE_REG1	00000000h
50200050h	4	MAC_VLAN_TAG_CTRL	00000000h
50200054h	4	MAC_VLAN_TAG_DATA	00000000h
50200058h	4	MAC_VLAN_HASH_TABLE	00000000h
50200060h	4	MAC_VLAN_INCL	00000000h
50200064h	4	MAC_INNER_VLAN_INCL	00000000h
50200070h	4	MAC_Q0_TX_FLOW_CTRL	00000000h
50200074h	4	MAC_Q1_TX_FLOW_CTRL	00000000h
50200078h	4	MAC_Q2_TX_FLOW_CTRL	00000000h
5020007Ch	4	MAC_Q3_TX_FLOW_CTRL	00000000h
50200080h	4	MAC_Q4_TX_FLOW_CTRL	00000000h
50200084h	4	MAC_Q5_TX_FLOW_CTRL	00000000h
50200088h	4	MAC_Q6_TX_FLOW_CTRL	00000000h
5020008Ch	4	MAC_Q7_TX_FLOW_CTRL	00000000h
50200090h	4	MAC_RX_FLOW_CTRL	00000000h
50200094h	4	MAC_RXQ_CTRL4	00000000h
50200098h	4	MAC_TXQ_PRTY_MAP0	00000000h
5020009Ch	4	MAC_TXQ_PRTY_MAP1	00000000h
502000A0h	4	MAC_RXQ_CTRL0	00000000h
502000A4h	4	MAC_RXQ_CTRL1	00000000h
502000A8h	4	MAC_RXQ_CTRL2	00000000h
502000ACh	4	MAC_RXQ_CTRL3	00000000h
502000B0h	4	MAC_INTERRUPT_STATUS	00000000h
502000B4h	4	MAC_INTERRUPT_ENABLE	00000000h
502000B8h	4	MAC_RX_TX_STATUS	00000000h
502000C0h	4	MAC_PMT_CONTROL_STATUS	00000000h
502000C4h	4	MAC_RWK_PACKET_FILTER	00000000h
502000D0h	4	MAC_LPI_CONTROL_STATUS	00000000h
502000D4h	4	MAC_LPI_TIMERS_CONTROL	03E80000h
502000D8h	4	MAC_LPI_ENTRY_TIMER	00000000h
502000DCh	4	MAC_1US_TIC_COUNTER	00000063h
502000F8h	4	MAC_PHYIF_CONTROL_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200110h	4	MAC_VERSION	00005152h
50200114h	4	MAC_DEBUG	00000000h
5020011Ch	4	MAC_HW_FEATURE0	0EFD73F7h
50200120h	4	MAC_HW_FEATURE1	119F7A69h
50200124h	4	MAC_HW_FEATURE2	225D71C7h
50200128h	4	MAC_HW_FEATURE3	2C395632h
50200140h	4	MAC_DPP_FSM_INTERRUPT_STATUS	00000000h
50200148h	4	MAC_FSM_CONTROL	00000000h
5020014Ch	4	MAC_FSM_ACT_TIMER	00000000h
50200150h	4	SNPS_SCS_REG1	00000000h
50200200h	4	MAC_MDIO_ADDRESS	00000000h
50200204h	4	MAC_MDIO_DATA	00000000h
50200208h	4	MAC_GPIO_CONTROL	00000000h
5020020Ch	4	MAC_GPIO_STATUS	00000000h
50200210h	4	MAC_ARP_ADDRESS	00000000h
50200230h	4	MAC_CSR_SW_CTRL	00000000h
50200234h	4	MAC_FPE_CTRL_STS	00000000h
50200238h	4	MAC_EXT_CFG1	00000002h
50200240h	4	MAC_PRESN_TIME_NS	00000000h
50200244h	4	MAC_PRESN_TIME_UPDT	00000000h
50200300h	4	MAC_ADDRESS0_HIGH	8000FFFFh
50200304h	4	MAC_ADDRESS0_LOW	FFFFFFFFh
50200308h	4	MAC_ADDRESS1_HIGH	0000FFFFh
5020030Ch	4	MAC_ADDRESS1_LOW	FFFFFFFFh
50200310h	4	MAC_ADDRESS2_HIGH	0000FFFFh
50200314h	4	MAC_ADDRESS2_LOW	FFFFFFFFh
50200318h	4	MAC_ADDRESS3_HIGH	0000FFFFh
5020031Ch	4	MAC_ADDRESS3_LOW	FFFFFFFFh
50200320h	4	MAC_ADDRESS4_HIGH	0000FFFFh
50200324h	4	MAC_ADDRESS4_LOW	FFFFFFFFh
50200328h	4	MAC_ADDRESS5_HIGH	0000FFFFh
5020032Ch	4	MAC_ADDRESS5_LOW	FFFFFFFFh
50200330h	4	MAC_ADDRESS6_HIGH	0000FFFFh
50200334h	4	MAC_ADDRESS6_LOW	FFFFFFFFh
50200338h	4	MAC_ADDRESS7_HIGH	0000FFFFh
5020033Ch	4	MAC_ADDRESS7_LOW	FFFFFFFFh
50200340h	4	MAC_ADDRESS8_HIGH	0000FFFFh
50200344h	4	MAC_ADDRESS8_LOW	FFFFFFFFh
50200348h	4	MAC_ADDRESS9_HIGH	0000FFFFh
5020034Ch	4	MAC_ADDRESS9_LOW	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200350h	4	MAC_ADDRESS10_HIGH	0000FFFFh
50200354h	4	MAC_ADDRESS10_LOW	FFFFFFFFh
50200358h	4	MAC_ADDRESS11_HIGH	0000FFFFh
5020035Ch	4	MAC_ADDRESS11_LOW	FFFFFFFFh
50200360h	4	MAC_ADDRESS12_HIGH	0000FFFFh
50200364h	4	MAC_ADDRESS12_LOW	FFFFFFFFh
50200368h	4	MAC_ADDRESS13_HIGH	0000FFFFh
5020036Ch	4	MAC_ADDRESS13_LOW	FFFFFFFFh
50200370h	4	MAC_ADDRESS14_HIGH	0000FFFFh
50200374h	4	MAC_ADDRESS14_LOW	FFFFFFFFh
50200378h	4	MAC_ADDRESS15_HIGH	0000FFFFh
5020037Ch	4	MAC_ADDRESS15_LOW	FFFFFFFFh
50200380h	4	MAC_ADDRESS16_HIGH	0000FFFFh
50200384h	4	MAC_ADDRESS16_LOW	FFFFFFFFh
50200388h	4	MAC_ADDRESS17_HIGH	0000FFFFh
5020038Ch	4	MAC_ADDRESS17_LOW	FFFFFFFFh
50200390h	4	MAC_ADDRESS18_HIGH	0000FFFFh
50200394h	4	MAC_ADDRESS18_LOW	FFFFFFFFh
50200398h	4	MAC_ADDRESS19_HIGH	0000FFFFh
5020039Ch	4	MAC_ADDRESS19_LOW	FFFFFFFFh
502003A0h	4	MAC_ADDRESS20_HIGH	0000FFFFh
502003A4h	4	MAC_ADDRESS20_LOW	FFFFFFFFh
502003A8h	4	MAC_ADDRESS21_HIGH	0000FFFFh
502003ACh	4	MAC_ADDRESS21_LOW	FFFFFFFFh
502003B0h	4	MAC_ADDRESS22_HIGH	0000FFFFh
502003B4h	4	MAC_ADDRESS22_LOW	FFFFFFFFh
502003B8h	4	MAC_ADDRESS23_HIGH	0000FFFFh
502003BCh	4	MAC_ADDRESS23_LOW	FFFFFFFFh
502003C0h	4	MAC_ADDRESS24_HIGH	0000FFFFh
502003C4h	4	MAC_ADDRESS24_LOW	FFFFFFFFh
502003C8h	4	MAC_ADDRESS25_HIGH	0000FFFFh
502003CCh	4	MAC_ADDRESS25_LOW	FFFFFFFFh
502003D0h	4	MAC_ADDRESS26_HIGH	0000FFFFh
502003D4h	4	MAC_ADDRESS26_LOW	FFFFFFFFh
502003D8h	4	MAC_ADDRESS27_HIGH	0000FFFFh
502003DCh	4	MAC_ADDRESS27_LOW	FFFFFFFFh
502003E0h	4	MAC_ADDRESS28_HIGH	0000FFFFh
502003E4h	4	MAC_ADDRESS28_LOW	FFFFFFFFh
502003E8h	4	MAC_ADDRESS29_HIGH	0000FFFFh
502003ECh	4	MAC_ADDRESS29_LOW	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502003F0h	4	MAC_ADDRESS30_HIGH	0000FFFFh
502003F4h	4	MAC_ADDRESS30_LOW	FFFFFFFFh
502003F8h	4	MAC_ADDRESS31_HIGH	0000FFFFh
502003FCh	4	MAC_ADDRESS31_LOW	FFFFFFFFh
50200400h	4	MAC_ADDRESS32_HIGH	0000FFFFh
50200404h	4	MAC_ADDRESS32_LOW	FFFFFFFFh
50200408h	4	MAC_ADDRESS33_HIGH	0000FFFFh
5020040Ch	4	MAC_ADDRESS33_LOW	FFFFFFFFh
50200410h	4	MAC_ADDRESS34_HIGH	0000FFFFh
50200414h	4	MAC_ADDRESS34_LOW	FFFFFFFFh
50200418h	4	MAC_ADDRESS35_HIGH	0000FFFFh
5020041Ch	4	MAC_ADDRESS35_LOW	FFFFFFFFh
50200420h	4	MAC_ADDRESS36_HIGH	0000FFFFh
50200424h	4	MAC_ADDRESS36_LOW	FFFFFFFFh
50200428h	4	MAC_ADDRESS37_HIGH	0000FFFFh
5020042Ch	4	MAC_ADDRESS37_LOW	FFFFFFFFh
50200430h	4	MAC_ADDRESS38_HIGH	0000FFFFh
50200434h	4	MAC_ADDRESS38_LOW	FFFFFFFFh
50200438h	4	MAC_ADDRESS39_HIGH	0000FFFFh
5020043Ch	4	MAC_ADDRESS39_LOW	FFFFFFFFh
50200440h	4	MAC_ADDRESS40_HIGH	0000FFFFh
50200444h	4	MAC_ADDRESS40_LOW	FFFFFFFFh
50200448h	4	MAC_ADDRESS41_HIGH	0000FFFFh
5020044Ch	4	MAC_ADDRESS41_LOW	FFFFFFFFh
50200450h	4	MAC_ADDRESS42_HIGH	0000FFFFh
50200454h	4	MAC_ADDRESS42_LOW	FFFFFFFFh
50200458h	4	MAC_ADDRESS43_HIGH	0000FFFFh
5020045Ch	4	MAC_ADDRESS43_LOW	FFFFFFFFh
50200460h	4	MAC_ADDRESS44_HIGH	0000FFFFh
50200464h	4	MAC_ADDRESS44_LOW	FFFFFFFFh
50200468h	4	MAC_ADDRESS45_HIGH	0000FFFFh
5020046Ch	4	MAC_ADDRESS45_LOW	FFFFFFFFh
50200470h	4	MAC_ADDRESS46_HIGH	0000FFFFh
50200474h	4	MAC_ADDRESS46_LOW	FFFFFFFFh
50200478h	4	MAC_ADDRESS47_HIGH	0000FFFFh
5020047Ch	4	MAC_ADDRESS47_LOW	FFFFFFFFh
50200480h	4	MAC_ADDRESS48_HIGH	0000FFFFh
50200484h	4	MAC_ADDRESS48_LOW	FFFFFFFFh
50200488h	4	MAC_ADDRESS49_HIGH	0000FFFFh
5020048Ch	4	MAC_ADDRESS49_LOW	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200490h	4	MAC_ADDRESS50_HIGH	0000FFFFh
50200494h	4	MAC_ADDRESS50_LOW	FFFFFFFFh
50200498h	4	MAC_ADDRESS51_HIGH	0000FFFFh
5020049Ch	4	MAC_ADDRESS51_LOW	FFFFFFFFh
502004A0h	4	MAC_ADDRESS52_HIGH	0000FFFFh
502004A4h	4	MAC_ADDRESS52_LOW	FFFFFFFFh
502004A8h	4	MAC_ADDRESS53_HIGH	0000FFFFh
502004ACh	4	MAC_ADDRESS53_LOW	FFFFFFFFh
502004B0h	4	MAC_ADDRESS54_HIGH	0000FFFFh
502004B4h	4	MAC_ADDRESS54_LOW	FFFFFFFFh
502004B8h	4	MAC_ADDRESS55_HIGH	0000FFFFh
502004BCh	4	MAC_ADDRESS55_LOW	FFFFFFFFh
502004C0h	4	MAC_ADDRESS56_HIGH	0000FFFFh
502004C4h	4	MAC_ADDRESS56_LOW	FFFFFFFFh
502004C8h	4	MAC_ADDRESS57_HIGH	0000FFFFh
502004CCh	4	MAC_ADDRESS57_LOW	FFFFFFFFh
502004D0h	4	MAC_ADDRESS58_HIGH	0000FFFFh
502004D4h	4	MAC_ADDRESS58_LOW	FFFFFFFFh
502004D8h	4	MAC_ADDRESS59_HIGH	0000FFFFh
502004DCh	4	MAC_ADDRESS59_LOW	FFFFFFFFh
502004E0h	4	MAC_ADDRESS60_HIGH	0000FFFFh
502004E4h	4	MAC_ADDRESS60_LOW	FFFFFFFFh
502004E8h	4	MAC_ADDRESS61_HIGH	0000FFFFh
502004ECh	4	MAC_ADDRESS61_LOW	FFFFFFFFh
502004F0h	4	MAC_ADDRESS62_HIGH	0000FFFFh
502004F4h	4	MAC_ADDRESS62_LOW	FFFFFFFFh
502004F8h	4	MAC_ADDRESS63_HIGH	0000FFFFh
502004FCh	4	MAC_ADDRESS63_LOW	FFFFFFFFh
50200700h	4	MMC_CONTROL	00000000h
50200704h	4	MMC_RX_INTERRUPT	00000000h
50200708h	4	MMC_TX_INTERRUPT	00000000h
5020070Ch	4	MMC_RX_INTERRUPT_MASK	00000000h
50200710h	4	MMC_TX_INTERRUPT_MASK	00000000h
50200714h	4	TX_OCTET_COUNT_GOOD_BAD	00000000h
50200718h	4	TX_PACKET_COUNT_GOOD_BAD	00000000h
5020071Ch	4	TX_BROADCAST_PACKETS_GOOD	00000000h
50200720h	4	TX_MULTICAST_PACKETS_GOOD	00000000h
50200724h	4	TX_64OCTETS_PACKETS_GOOD_BAD	00000000h
50200728h	4	TX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
5020072Ch	4	TX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200730h	4	TX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h
50200734h	4	TX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
50200738h	4	TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
5020073Ch	4	TX_UNICAST_PACKETS_GOOD_BAD	00000000h
50200740h	4	TX_MULTICAST_PACKETS_GOOD_BAD	00000000h
50200744h	4	TX_BROADCAST_PACKETS_GOOD_BAD	00000000h
50200748h	4	TX_UNDERFLOW_ERROR_PACKETS	00000000h
5020074Ch	4	TX_SINGLE_COLLISION_GOOD_PACKETS	00000000h
50200750h	4	TX_MULTIPLE_COLLISION_GOOD_PACKETS	00000000h
50200754h	4	TX_DEFERRED_PACKETS	00000000h
50200758h	4	TX_LATE_COLLISION_PACKETS	00000000h
5020075Ch	4	TX_EXCESSIVE_COLLISION_PACKETS	00000000h
50200760h	4	TX_CARRIER_ERROR_PACKETS	00000000h
50200764h	4	TX_OCTET_COUNT_GOOD	00000000h
50200768h	4	TX_PACKET_COUNT_GOOD	00000000h
5020076Ch	4	TX_EXCESSIVE_DEFERRAL_ERROR	00000000h
50200770h	4	TX_PAUSE_PACKETS	00000000h
50200774h	4	TX_VLAN_PACKETS_GOOD	00000000h
50200778h	4	TX_OSIZE_PACKETS_GOOD	00000000h
50200780h	4	RX_PACKETS_COUNT_GOOD_BAD	00000000h
50200784h	4	RX_OCTET_COUNT_GOOD_BAD	00000000h
50200788h	4	RX_OCTET_COUNT_GOOD	00000000h
5020078Ch	4	RX_BROADCAST_PACKETS_GOOD	00000000h
50200790h	4	RX_MULTICAST_PACKETS_GOOD	00000000h
50200794h	4	RX_CRC_ERROR_PACKETS	00000000h
50200798h	4	RX_ALIGNMENT_ERROR_PACKETS	00000000h
5020079Ch	4	RX_RUNT_ERROR_PACKETS	00000000h
502007A0h	4	RX_JABBER_ERROR_PACKETS	00000000h
502007A4h	4	RX_UNDERSIZE_PACKETS_GOOD	00000000h
502007A8h	4	RX_OVERSIZE_PACKETS_GOOD	00000000h
502007ACh	4	RX_64OCTETS_PACKETS_GOOD_BAD	00000000h
502007B0h	4	RX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
502007B4h	4	RX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h
502007B8h	4	RX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h
502007BCh	4	RX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
502007C0h	4	RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
502007C4h	4	RX_UNICAST_PACKETS_GOOD	00000000h
502007C8h	4	RX_LENGTH_ERROR_PACKETS	00000000h
502007CCh	4	RX_OUT_OF_RANGE_TYPE_PACKETS	00000000h
502007D0h	4	RX_PAUSE_PACKETS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502007D4h	4	RX_FIFO_OVERFLOW_PACKETS	00000000h
502007D8h	4	RX_VLAN_PACKETS_GOOD_BAD	00000000h
502007DCh	4	RX_WATCHDOG_ERROR_PACKETS	00000000h
502007E0h	4	RX_RECEIVE_ERROR_PACKETS	00000000h
502007E4h	4	RX_CONTROL_PACKETS_GOOD	00000000h
502007ECh	4	TX_LPI_USEC_CNTR	00000000h
502007F0h	4	TX_LPI_TRAN_CNTR	00000000h
502007F4h	4	RX_LPI_USEC_CNTR	00000000h
502007F8h	4	RX_LPI_TRAN_CNTR	00000000h
50200800h	4	MMC_IPC_RX_INTERRUPT_MASK	00000000h
50200808h	4	MMC_IPC_RX_INTERRUPT	00000000h
50200810h	4	RXIPV4_GOOD_PACKETS	00000000h
50200814h	4	RXIPV4_HEADER_ERROR_PACKETS	00000000h
50200818h	4	RXIPV4_NO_PAYLOAD_PACKETS	00000000h
5020081Ch	4	RXIPV4_FRAGMENTED_PACKETS	00000000h
50200820h	4	RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS	00000000h
50200824h	4	RXIPV6_GOOD_PACKETS	00000000h
50200828h	4	RXIPV6_HEADER_ERROR_PACKETS	00000000h
5020082Ch	4	RXIPV6_NO_PAYLOAD_PACKETS	00000000h
50200830h	4	RXUDP_GOOD_PACKETS	00000000h
50200834h	4	RXUDP_ERROR_PACKETS	00000000h
50200838h	4	RXTCP_GOOD_PACKETS	00000000h
5020083Ch	4	RXTCP_ERROR_PACKETS	00000000h
50200840h	4	RXICMP_GOOD_PACKETS	00000000h
50200844h	4	RXICMP_ERROR_PACKETS	00000000h
50200850h	4	RXIPV4_GOOD_OCTETS	00000000h
50200854h	4	RXIPV4_HEADER_ERROR_OCTETS	00000000h
50200858h	4	RXIPV4_NO_PAYLOAD_OCTETS	00000000h
5020085Ch	4	RXIPV4_FRAGMENTED_OCTETS	00000000h
50200860h	4	RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	00000000h
50200864h	4	RXIPV6_GOOD_OCTETS	00000000h
50200868h	4	RXIPV6_HEADER_ERROR_OCTETS	00000000h
5020086Ch	4	RXIPV6_NO_PAYLOAD_OCTETS	00000000h
50200870h	4	RXUDP_GOOD_OCTETS	00000000h
50200874h	4	RXUDP_ERROR_OCTETS	00000000h
50200878h	4	RXTCP_GOOD_OCTETS	00000000h
5020087Ch	4	RXTCP_ERROR_OCTETS	00000000h
50200880h	4	RXICMP_GOOD_OCTETS	00000000h
50200884h	4	RXICMP_ERROR_OCTETS	00000000h
502008A0h	4	MMC_FPE_TX_INTERRUPT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502008A4h	4	MMC_FPE_TX_INTERRUPT_MASK	00000000h
502008A8h	4	MMC_TX_FPE_FRAGMENT_CNTR	00000000h
502008ACh	4	MMC_TX_HOLD_REQ_CNTR	00000000h
502008C0h	4	MMC_FPE_RX_INTERRUPT	00000000h
502008C4h	4	MMC_FPE_RX_INTERRUPT_MASK	00000000h
502008C8h	4	MMC_RX_PACKET_ASSEMBLY_ERR_CNTR	00000000h
502008CCh	4	MMC_RX_PACKET_SMD_ERR_CNTR	00000000h
502008D0h	4	MMC_RX_PACKET_ASSEMBLY_OK_CNTR	00000000h
502008D4h	4	MMC_RX_FPE_FRAGMENT_CNTR	00000000h
50200900h	4	MAC_L3_L4_CONTROL0	00000000h
50200904h	4	MAC_LAYER4_ADDRESS0	00000000h
50200910h	4	MAC_LAYER3_ADDR0_REG0	00000000h
50200914h	4	MAC_LAYER3_ADDR1_REG0	00000000h
50200918h	4	MAC_LAYER3_ADDR2_REG0	00000000h
5020091Ch	4	MAC_LAYER3_ADDR3_REG0	00000000h
50200930h	4	MAC_L3_L4_CONTROL1	00000000h
50200934h	4	MAC_LAYER4_ADDRESS1	00000000h
50200940h	4	MAC_LAYER3_ADDR0_REG1	00000000h
50200944h	4	MAC_LAYER3_ADDR1_REG1	00000000h
50200948h	4	MAC_LAYER3_ADDR2_REG1	00000000h
5020094Ch	4	MAC_LAYER3_ADDR3_REG1	00000000h
50200B00h	4	MAC_TIMESTAMP_CONTROL	00002000h
50200B04h	4	MAC_SUB_SECOND_INCREMENT	00000000h
50200B08h	4	MAC_SYSTEM_TIME_SECONDS	00000000h
50200B0Ch	4	MAC_SYSTEM_TIME_NANOSECONDS	00000000h
50200B10h	4	MAC_SYSTEM_TIME_SECONDS_UPDATE	00000000h
50200B14h	4	MAC_SYSTEM_TIME_NANOSECONDS_UPDATE	00000000h
50200B18h	4	MAC_TIMESTAMP_ADDEND	00000000h
50200B1Ch	4	MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS	00000000h
50200B20h	4	MAC_TIMESTAMP_STATUS	00000000h
50200B30h	4	MAC_TX_TIMESTAMP_STATUS_NANOSECONDS	00000000h
50200B34h	4	MAC_TX_TIMESTAMP_STATUS_SECONDS	00000000h
50200B40h	4	MAC_AUXILIARY_CONTROL	00000000h
50200B48h	4	MAC_AUXILIARY_TIMESTAMP_NANOSECONDS	00000000h
50200B4Ch	4	MAC_AUXILIARY_TIMESTAMP_SECONDS	00000000h
50200B50h	4	MAC_TIMESTAMP_INGRESS_ASYM_CORR	00000000h
50200B54h	4	MAC_TIMESTAMP_EGRESS_ASYM_CORR	00000000h
50200B58h	4	MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND	00000000h
50200B5Ch	4	MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND	00000000h
50200B60h	4	MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200B64h	4	MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC	00000000h
50200B68h	4	MAC_TIMESTAMP_INGRESS_LATENCY	00000000h
50200B6Ch	4	MAC_TIMESTAMP_EGRESS_LATENCY	00000000h
50200B70h	4	MAC_PPS_CONTROL	00000000h
50200B80h	4	MAC_PPS0_TARGET_TIME_SECONDS	00000000h
50200B84h	4	MAC_PPS0_TARGET_TIME_NANOSECONDS	00000000h
50200B88h	4	MAC_PPS0_INTERVAL	00000000h
50200B8Ch	4	MAC_PPS0_WIDTH	00000000h
50200B90h	4	MAC_PPS1_TARGET_TIME_SECONDS	00000000h
50200B94h	4	MAC_PPS1_TARGET_TIME_NANOSECONDS	00000000h
50200B98h	4	MAC_PPS1_INTERVAL	00000000h
50200B9Ch	4	MAC_PPS1_WIDTH	00000000h
50200BC0h	4	MAC_PTO_CONTROL	00000000h
50200BC4h	4	MAC_SOURCE_PORT_IDENTITY0	00000000h
50200BC8h	4	MAC_SOURCE_PORT_IDENTITY1	00000000h
50200BCCh	4	MAC_SOURCE_PORT_IDENTITY2	00000000h
50200BD0h	4	MAC_LOG_MESSAGE_INTERVAL	00000000h
50200C00h	4	MTL_OPERATION_MODE	00000000h
50200C08h	4	MTL_DBG_CTL	00000000h
50200C0Ch	4	MTL_DBG_STS	00000018h
50200C10h	4	MTL_FIFO_DEBUG_DATA	00000000h
50200C20h	4	MTL_INTERRUPT_STATUS	00000000h
50200C30h	4	MTL_RXQ_DMA_MAP0	00000000h
50200C34h	4	MTL_RXQ_DMA_MAP1	00000000h
50200C40h	4	MTL_TBS_CTRL	00000000h
50200C50h	4	MTL_EST_CONTROL	00000000h
50200C58h	4	MTL_EST_STATUS	00000000h
50200C60h	4	MTL_EST_SCH_ERROR	00000000h
50200C64h	4	MTL_EST_FRM_SIZE_ERROR	00000000h
50200C68h	4	MTL_EST_FRM_SIZE_CAPTURE	00000000h
50200C70h	4	MTL_EST_INTR_ENABLE	00000000h
50200C80h	4	MTL_EST_GCL_CONTROL	00000000h
50200C84h	4	MTL_EST_GCL_DATA	00000000h
50200C90h	4	MTL_FPE_CTRL_STS	00000000h
50200C94h	4	MTL_FPE_ADVANCE	00000000h
50200CA0h	4	MTL_RXP_CONTROL_STATUS	80FF00FFh
50200CA4h	4	MTL_RXP_INTERRUPT_CONTROL_STATUS	00000000h
50200CA8h	4	MTL_RXP_DROP_CNT	00000000h
50200CACh	4	MTL_RXP_ERROR_CNT	00000000h
50200CB0h	4	MTL_RXP_INDIRECT_ACC_CONTROL_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200CB4h	4	MTL_RXP_INDIRECT_ACC_DATA	00000000h
50200CC0h	4	MTL_ECC_CONTROL	00000000h
50200CC4h	4	MTL_SAFETY_INTERRUPT_STATUS	00000000h
50200CC8h	4	MTL_ECC_INTERRUPT_ENABLE	00000000h
50200CCCh	4	MTL_ECC_INTERRUPT_STATUS	00000000h
50200CD0h	4	MTL_ECC_ERR_STS_RCTL	00000000h
50200CD4h	4	MTL_ECC_ERR_ADDR_STATUS	00000000h
50200CD8h	4	MTL_ECC_ERR_CNTR_STATUS	00000000h
50200CE0h	4	MTL_DPP_CONTROL	00000000h
50200D00h	4	MTL_TXQ0_OPERATION_MODE	00000000h
50200D04h	4	MTL_TXQ0_UNDERFLOW	00000000h
50200D08h	4	MTL_TXQ0_DEBUG	00000000h
50200D14h	4	MTL_TXQ0_ETS_STATUS	00000000h
50200D18h	4	MTL_TXQ0_QUANTUM_WEIGHT	00000000h
50200D2Ch	4	MTL_Q0_INTERRUPT_CONTROL_STATUS	00000000h
50200D30h	4	MTL_RXQ0_OPERATION_MODE	00000000h
50200D34h	4	MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200D38h	4	MTL_RXQ0_DEBUG	00000000h
50200D3Ch	4	MTL_RXQ0_CONTROL	00000000h
50200D40h	4	MTL_TXQ1_OPERATION_MODE	00000000h
50200D44h	4	MTL_TXQ1_UNDERFLOW	00000000h
50200D48h	4	MTL_TXQ1_DEBUG	00000000h
50200D50h	4	MTL_TXQ1_ETS_CONTROL	00000000h
50200D54h	4	MTL_TXQ1_ETS_STATUS	00000000h
50200D58h	4	MTL_TXQ1_QUANTUM_WEIGHT	00000000h
50200D5Ch	4	MTL_TXQ1_SENDSLOPECREDIT	00000000h
50200D60h	4	MTL_TXQ1_HICREDIT	00000000h
50200D64h	4	MTL_TXQ1_LOCREDIT	00000000h
50200D6Ch	4	MTL_Q1_INTERRUPT_CONTROL_STATUS	00000000h
50200D70h	4	MTL_RXQ1_OPERATION_MODE	00000000h
50200D74h	4	MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200D78h	4	MTL_RXQ1_DEBUG	00000000h
50200D7Ch	4	MTL_RXQ1_CONTROL	00000000h
50200D80h	4	MTL_TXQ2_OPERATION_MODE	00000000h
50200D84h	4	MTL_TXQ2_UNDERFLOW	00000000h
50200D88h	4	MTL_TXQ2_DEBUG	00000000h
50200D90h	4	MTL_TXQ2_ETS_CONTROL	00000000h
50200D94h	4	MTL_TXQ2_ETS_STATUS	00000000h
50200D98h	4	MTL_TXQ2_QUANTUM_WEIGHT	00000000h
50200D9Ch	4	MTL_TXQ2_SENDSLOPECREDIT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200DA0h	4	MTL_TXQ2_HICREDIT	00000000h
50200DA4h	4	MTL_TXQ2_LOCREDIT	00000000h
50200DACh	4	MTL_Q2_INTERRUPT_CONTROL_STATUS	00000000h
50200DB0h	4	MTL_RXQ2_OPERATION_MODE	00000000h
50200DB4h	4	MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200DB8h	4	MTL_RXQ2_DEBUG	00000000h
50200DBCh	4	MTL_RXQ2_CONTROL	00000000h
50200DC0h	4	MTL_TXQ3_OPERATION_MODE	00000000h
50200DC4h	4	MTL_TXQ3_UNDERFLOW	00000000h
50200DC8h	4	MTL_TXQ3_DEBUG	00000000h
50200DD0h	4	MTL_TXQ3_ETS_CONTROL	00000000h
50200DD4h	4	MTL_TXQ3_ETS_STATUS	00000000h
50200DD8h	4	MTL_TXQ3_QUANTUM_WEIGHT	00000000h
50200DDCh	4	MTL_TXQ3_SENDSLOPECREDIT	00000000h
50200DE0h	4	MTL_TXQ3_HICREDIT	00000000h
50200DE4h	4	MTL_TXQ3_LOCREDIT	00000000h
50200DECh	4	MTL_Q3_INTERRUPT_CONTROL_STATUS	00000000h
50200DF0h	4	MTL_RXQ3_OPERATION_MODE	00000000h
50200DF4h	4	MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200DF8h	4	MTL_RXQ3_DEBUG	00000000h
50200DFCh	4	MTL_RXQ3_CONTROL	00000000h
50200E00h	4	MTL_TXQ4_OPERATION_MODE	00000000h
50200E04h	4	MTL_TXQ4_UNDERFLOW	00000000h
50200E08h	4	MTL_TXQ4_DEBUG	00000000h
50200E10h	4	MTL_TXQ4_ETS_CONTROL	00000000h
50200E14h	4	MTL_TXQ4_ETS_STATUS	00000000h
50200E18h	4	MTL_TXQ4_QUANTUM_WEIGHT	00000000h
50200E1Ch	4	MTL_TXQ4_SENDSLOPECREDIT	00000000h
50200E20h	4	MTL_TXQ4_HICREDIT	00000000h
50200E24h	4	MTL_TXQ4_LOCREDIT	00000000h
50200E2Ch	4	MTL_Q4_INTERRUPT_CONTROL_STATUS	00000000h
50200E30h	4	MTL_RXQ4_OPERATION_MODE	00000000h
50200E34h	4	MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200E38h	4	MTL_RXQ4_DEBUG	00000000h
50200E3Ch	4	MTL_RXQ4_CONTROL	00000000h
50200E40h	4	MTL_TXQ5_OPERATION_MODE	00000000h
50200E44h	4	MTL_TXQ5_UNDERFLOW	00000000h
50200E48h	4	MTL_TXQ5_DEBUG	00000000h
50200E50h	4	MTL_TXQ5_ETS_CONTROL	00000000h
50200E54h	4	MTL_TXQ5_ETS_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50200E58h	4	MTL_TXQ5_QUANTUM_WEIGHT	00000000h
50200E5Ch	4	MTL_TXQ5_SENDSLOPECREDIT	00000000h
50200E60h	4	MTL_TXQ5_HICREDIT	00000000h
50200E64h	4	MTL_TXQ5_LOCREDIT	00000000h
50200E6Ch	4	MTL_Q5_INTERRUPT_CONTROL_STATUS	00000000h
50200E70h	4	MTL_RXQ5_OPERATION_MODE	00000000h
50200E74h	4	MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200E78h	4	MTL_RXQ5_DEBUG	00000000h
50200E7Ch	4	MTL_RXQ5_CONTROL	00000000h
50200E80h	4	MTL_TXQ6_OPERATION_MODE	00000000h
50200E84h	4	MTL_TXQ6_UNDERFLOW	00000000h
50200E88h	4	MTL_TXQ6_DEBUG	00000000h
50200E90h	4	MTL_TXQ6_ETS_CONTROL	00000000h
50200E94h	4	MTL_TXQ6_ETS_STATUS	00000000h
50200E98h	4	MTL_TXQ6_QUANTUM_WEIGHT	00000000h
50200E9Ch	4	MTL_TXQ6_SENDSLOPECREDIT	00000000h
50200EA0h	4	MTL_TXQ6_HICREDIT	00000000h
50200EA4h	4	MTL_TXQ6_LOCREDIT	00000000h
50200EACh	4	MTL_Q6_INTERRUPT_CONTROL_STATUS	00000000h
50200EB0h	4	MTL_RXQ6_OPERATION_MODE	00000000h
50200EB4h	4	MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200EB8h	4	MTL_RXQ6_DEBUG	00000000h
50200EBCh	4	MTL_RXQ6_CONTROL	00000000h
50200EC0h	4	MTL_TXQ7_OPERATION_MODE	00000000h
50200EC4h	4	MTL_TXQ7_UNDERFLOW	00000000h
50200EC8h	4	MTL_TXQ7_DEBUG	00000000h
50200ED0h	4	MTL_TXQ7_ETS_CONTROL	00000000h
50200ED4h	4	MTL_TXQ7_ETS_STATUS	00000000h
50200ED8h	4	MTL_TXQ7_QUANTUM_WEIGHT	00000000h
50200EDCh	4	MTL_TXQ7_SENDSLOPECREDIT	00000000h
50200EE0h	4	MTL_TXQ7_HICREDIT	00000000h
50200EE4h	4	MTL_TXQ7_LOCREDIT	00000000h
50200EECh	4	MTL_Q7_INTERRUPT_CONTROL_STATUS	00000000h
50200EF0h	4	MTL_RXQ7_OPERATION_MODE	00000000h
50200EF4h	4	MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT	00000000h
50200EF8h	4	MTL_RXQ7_DEBUG	00000000h
50200EFCh	4	MTL_RXQ7_CONTROL	00000000h
50201000h	4	DMA_MODE	00000000h
50201004h	4	DMA_SYSBUS_MODE	01010000h
50201008h	4	DMA_INTERRUPT_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5020100Ch	4	DMA_DEBUG_STATUS0	00000000h
50201010h	4	DMA_DEBUG_STATUS1	00000000h
50201014h	4	DMA_DEBUG_STATUS2	00000000h
50201020h	4	AXI4_TX_AR_ACE_CONTROL	00000000h
50201024h	4	AXI4_RX_AW_ACE_CONTROL	00000000h
50201028h	4	AXI4_TXRX_AWAR_ACE_CONTROL	00000000h
50201040h	4	AXI_LPI_ENTRY_INTERVAL	00000000h
50201050h	4	DMA_TBS_CTRL0	00000000h
50201054h	4	DMA_TBS_CTRL1	00000000h
50201058h	4	DMA_TBS_CTRL2	00000000h
5020105Ch	4	DMA_TBS_CTRL3	00000000h
50201080h	4	DMA_SAFETY_INTERRUPT_STATUS	00000000h
50201084h	4	DMA_ECC_INTERRUPT_ENABLE	00000000h
50201088h	4	DMA_ECC_INTERRUPT_STATUS	00000000h
50201100h	4	DMA_CH0_CONTROL	00000000h
50201104h	4	DMA_CH0_TX_CONTROL	00000000h
50201108h	4	DMA_CH0_RX_CONTROL	00000000h
50201110h	4	DMA_CH0_TXDESC_LIST_HADDRESS	00000000h
50201114h	4	DMA_CH0_TXDESC_LIST_ADDRESS	00000000h
50201118h	4	DMA_CH0_RXDESC_LIST_HADDRESS	00000000h
5020111Ch	4	DMA_CH0_RXDESC_LIST_ADDRESS	00000000h
50201120h	4	DMA_CH0_TXDESC_TAIL_POINTER	00000000h
50201128h	4	DMA_CH0_RXDESC_TAIL_POINTER	00000000h
5020112Ch	4	DMA_CH0_TXDESC_RING_LENGTH	00000000h
50201130h	4	DMA_CH0_RXDESC_RING_LENGTH	00000000h
50201134h	4	DMA_CH0_INTERRUPT_ENABLE	00000000h
50201138h	4	DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5020113Ch	4	DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50201144h	4	DMA_CH0_CURRENT_APP_TXDESC	00000000h
5020114Ch	4	DMA_CH0_CURRENT_APP_RXDESC	00000000h
50201150h	4	DMA_CH0_CURRENT_APP_TXBUFFER_H	00000000h
50201154h	4	DMA_CH0_CURRENT_APP_TXBUFFER	00000000h
50201158h	4	DMA_CH0_CURRENT_APP_RXBUFFER_H	00000000h
5020115Ch	4	DMA_CH0_CURRENT_APP_RXBUFFER	00000000h
50201160h	4	DMA_CH0_STATUS	00000000h
50201164h	4	DMA_CH0_MISS_FRAME_CNT	00000000h
50201168h	4	DMA_CH0_RXP_ACCEPT_CNT	00000000h
5020116Ch	4	DMA_CH0_RX_ERI_CNT	00000000h
50201180h	4	DMA_CH1_CONTROL	00000000h
50201184h	4	DMA_CH1_TX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50201188h	4	DMA_CH1_RX_CONTROL	00000000h
50201190h	4	DMA_CH1_TXDESC_LIST_HADDRESS	00000000h
50201194h	4	DMA_CH1_TXDESC_LIST_ADDRESS	00000000h
50201198h	4	DMA_CH1_RXDESC_LIST_HADDRESS	00000000h
5020119Ch	4	DMA_CH1_RXDESC_LIST_ADDRESS	00000000h
502011A0h	4	DMA_CH1_TXDESC_TAIL_POINTER	00000000h
502011A8h	4	DMA_CH1_RXDESC_TAIL_POINTER	00000000h
502011ACh	4	DMA_CH1_TXDESC_RING_LENGTH	00000000h
502011B0h	4	DMA_CH1_RXDESC_RING_LENGTH	00000000h
502011B4h	4	DMA_CH1_INTERRUPT_ENABLE	00000000h
502011B8h	4	DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502011BCh	4	DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502011C4h	4	DMA_CH1_CURRENT_APP_TXDESC	00000000h
502011CCh	4	DMA_CH1_CURRENT_APP_RXDESC	00000000h
502011D0h	4	DMA_CH1_CURRENT_APP_TXBUFFER_H	00000000h
502011D4h	4	DMA_CH1_CURRENT_APP_TXBUFFER	00000000h
502011D8h	4	DMA_CH1_CURRENT_APP_RXBUFFER_H	00000000h
502011DCh	4	DMA_CH1_CURRENT_APP_RXBUFFER	00000000h
502011E0h	4	DMA_CH1_STATUS	00000000h
502011E4h	4	DMA_CH1_MISS_FRAME_CNT	00000000h
502011E8h	4	DMA_CH1_RXP_ACCEPT_CNT	00000000h
502011ECh	4	DMA_CH1_RX_ERI_CNT	00000000h
50201200h	4	DMA_CH2_CONTROL	00000000h
50201204h	4	DMA_CH2_TX_CONTROL	00000000h
50201208h	4	DMA_CH2_RX_CONTROL	00000000h
50201210h	4	DMA_CH2_TXDESC_LIST_HADDRESS	00000000h
50201214h	4	DMA_CH2_TXDESC_LIST_ADDRESS	00000000h
50201218h	4	DMA_CH2_RXDESC_LIST_HADDRESS	00000000h
5020121Ch	4	DMA_CH2_RXDESC_LIST_ADDRESS	00000000h
50201220h	4	DMA_CH2_TXDESC_TAIL_POINTER	00000000h
50201228h	4	DMA_CH2_RXDESC_TAIL_POINTER	00000000h
5020122Ch	4	DMA_CH2_TXDESC_RING_LENGTH	00000000h
50201230h	4	DMA_CH2_RXDESC_RING_LENGTH	00000000h
50201234h	4	DMA_CH2_INTERRUPT_ENABLE	00000000h
50201238h	4	DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5020123Ch	4	DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50201244h	4	DMA_CH2_CURRENT_APP_TXDESC	00000000h
5020124Ch	4	DMA_CH2_CURRENT_APP_RXDESC	00000000h
50201250h	4	DMA_CH2_CURRENT_APP_TXBUFFER_H	00000000h
50201254h	4	DMA_CH2_CURRENT_APP_TXBUFFER	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50201258h	4	DMA_CH2_CURRENT_APP_RXBUFFER_H	00000000h
5020125Ch	4	DMA_CH2_CURRENT_APP_RXBUFFER	00000000h
50201260h	4	DMA_CH2_STATUS	00000000h
50201264h	4	DMA_CH2_MISS_FRAME_CNT	00000000h
50201268h	4	DMA_CH2_RXP_ACCEPT_CNT	00000000h
5020126Ch	4	DMA_CH2_RX_ERI_CNT	00000000h
50201280h	4	DMA_CH3_CONTROL	00000000h
50201284h	4	DMA_CH3_TX_CONTROL	00000000h
50201288h	4	DMA_CH3_RX_CONTROL	00000000h
50201290h	4	DMA_CH3_TXDESC_LIST_HADDRESS	00000000h
50201294h	4	DMA_CH3_TXDESC_LIST_ADDRESS	00000000h
50201298h	4	DMA_CH3_RXDESC_LIST_HADDRESS	00000000h
5020129Ch	4	DMA_CH3_RXDESC_LIST_ADDRESS	00000000h
502012A0h	4	DMA_CH3_TXDESC_TAIL_POINTER	00000000h
502012A8h	4	DMA_CH3_RXDESC_TAIL_POINTER	00000000h
502012ACh	4	DMA_CH3_TXDESC_RING_LENGTH	00000000h
502012B0h	4	DMA_CH3_RXDESC_RING_LENGTH	00000000h
502012B4h	4	DMA_CH3_INTERRUPT_ENABLE	00000000h
502012B8h	4	DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502012BCh	4	DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502012C4h	4	DMA_CH3_CURRENT_APP_TXDESC	00000000h
502012CCh	4	DMA_CH3_CURRENT_APP_RXDESC	00000000h
502012D0h	4	DMA_CH3_CURRENT_APP_TXBUFFER_H	00000000h
502012D4h	4	DMA_CH3_CURRENT_APP_TXBUFFER	00000000h
502012D8h	4	DMA_CH3_CURRENT_APP_RXBUFFER_H	00000000h
502012DCh	4	DMA_CH3_CURRENT_APP_RXBUFFER	00000000h
502012E0h	4	DMA_CH3_STATUS	00000000h
502012E4h	4	DMA_CH3_MISS_FRAME_CNT	00000000h
502012E8h	4	DMA_CH3_RXP_ACCEPT_CNT	00000000h
502012ECh	4	DMA_CH3_RX_ERI_CNT	00000000h
50201300h	4	DMA_CH4_CONTROL	00000000h
50201304h	4	DMA_CH4_TX_CONTROL	00000000h
50201308h	4	DMA_CH4_RX_CONTROL	00000000h
50201310h	4	DMA_CH4_TXDESC_LIST_HADDRESS	00000000h
50201314h	4	DMA_CH4_TXDESC_LIST_ADDRESS	00000000h
50201318h	4	DMA_CH4_RXDESC_LIST_HADDRESS	00000000h
5020131Ch	4	DMA_CH4_RXDESC_LIST_ADDRESS	00000000h
50201320h	4	DMA_CH4_TXDESC_TAIL_POINTER	00000000h
50201328h	4	DMA_CH4_RXDESC_TAIL_POINTER	00000000h
5020132Ch	4	DMA_CH4_TXDESC_RING_LENGTH	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50201330h	4	DMA_CH4_RXDESC_RING_LENGTH	00000000h
50201334h	4	DMA_CH4_INTERRUPT_ENABLE	00000000h
50201338h	4	DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5020133Ch	4	DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50201344h	4	DMA_CH4_CURRENT_APP_TXDESC	00000000h
5020134Ch	4	DMA_CH4_CURRENT_APP_RXDESC	00000000h
50201350h	4	DMA_CH4_CURRENT_APP_TXBUFFER_H	00000000h
50201354h	4	DMA_CH4_CURRENT_APP_TXBUFFER	00000000h
50201358h	4	DMA_CH4_CURRENT_APP_RXBUFFER_H	00000000h
5020135Ch	4	DMA_CH4_CURRENT_APP_RXBUFFER	00000000h
50201360h	4	DMA_CH4_STATUS	00000000h
50201364h	4	DMA_CH4_MISS_FRAME_CNT	00000000h
50201368h	4	DMA_CH4_RXP_ACCEPT_CNT	00000000h
5020136Ch	4	DMA_CH4_RX_ERI_CNT	00000000h
50201380h	4	DMA_CH5_CONTROL	00000000h
50201384h	4	DMA_CH5_TX_CONTROL	00000000h
50201388h	4	DMA_CH5_RX_CONTROL	00000000h
50201390h	4	DMA_CH5_TXDESC_LIST_HADDRESS	00000000h
50201394h	4	DMA_CH5_TXDESC_LIST_ADDRESS	00000000h
50201398h	4	DMA_CH5_RXDESC_LIST_HADDRESS	00000000h
5020139Ch	4	DMA_CH5_RXDESC_LIST_ADDRESS	00000000h
502013A0h	4	DMA_CH5_TXDESC_TAIL_POINTER	00000000h
502013A8h	4	DMA_CH5_RXDESC_TAIL_POINTER	00000000h
502013ACh	4	DMA_CH5_TXDESC_RING_LENGTH	00000000h
502013B0h	4	DMA_CH5_RXDESC_RING_LENGTH	00000000h
502013B4h	4	DMA_CH5_INTERRUPT_ENABLE	00000000h
502013B8h	4	DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502013BCh	4	DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502013C4h	4	DMA_CH5_CURRENT_APP_TXDESC	00000000h
502013CCh	4	DMA_CH5_CURRENT_APP_RXDESC	00000000h
502013D0h	4	DMA_CH5_CURRENT_APP_TXBUFFER_H	00000000h
502013D4h	4	DMA_CH5_CURRENT_APP_TXBUFFER	00000000h
502013D8h	4	DMA_CH5_CURRENT_APP_RXBUFFER_H	00000000h
502013DCh	4	DMA_CH5_CURRENT_APP_RXBUFFER	00000000h
502013E0h	4	DMA_CH5_STATUS	00000000h
502013E4h	4	DMA_CH5_MISS_FRAME_CNT	00000000h
502013E8h	4	DMA_CH5_RXP_ACCEPT_CNT	00000000h
502013ECh	4	DMA_CH5_RX_ERI_CNT	00000000h
50201400h	4	DMA_CH6_CONTROL	00000000h
50201404h	4	DMA_CH6_TX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50201408h	4	DMA_CH6_RX_CONTROL	00000000h
50201410h	4	DMA_CH6_TXDESC_LIST_HADDRESS	00000000h
50201414h	4	DMA_CH6_TXDESC_LIST_ADDRESS	00000000h
50201418h	4	DMA_CH6_RXDESC_LIST_HADDRESS	00000000h
5020141Ch	4	DMA_CH6_RXDESC_LIST_ADDRESS	00000000h
50201420h	4	DMA_CH6_TXDESC_TAIL_POINTER	00000000h
50201428h	4	DMA_CH6_RXDESC_TAIL_POINTER	00000000h
5020142Ch	4	DMA_CH6_TXDESC_RING_LENGTH	00000000h
50201430h	4	DMA_CH6_RXDESC_RING_LENGTH	00000000h
50201434h	4	DMA_CH6_INTERRUPT_ENABLE	00000000h
50201438h	4	DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5020143Ch	4	DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50201444h	4	DMA_CH6_CURRENT_APP_TXDESC	00000000h
5020144Ch	4	DMA_CH6_CURRENT_APP_RXDESC	00000000h
50201450h	4	DMA_CH6_CURRENT_APP_TXBUFFER_H	00000000h
50201454h	4	DMA_CH6_CURRENT_APP_TXBUFFER	00000000h
50201458h	4	DMA_CH6_CURRENT_APP_RXBUFFER_H	00000000h
5020145Ch	4	DMA_CH6_CURRENT_APP_RXBUFFER	00000000h
50201460h	4	DMA_CH6_STATUS	00000000h
50201464h	4	DMA_CH6_MISS_FRAME_CNT	00000000h
50201468h	4	DMA_CH6_RXP_ACCEPT_CNT	00000000h
5020146Ch	4	DMA_CH6_RX_ERI_CNT	00000000h
50201480h	4	DMA_CH7_CONTROL	00000000h
50201484h	4	DMA_CH7_TX_CONTROL	00000000h
50201488h	4	DMA_CH7_RX_CONTROL	00000000h
50201490h	4	DMA_CH7_TXDESC_LIST_HADDRESS	00000000h
50201494h	4	DMA_CH7_TXDESC_LIST_ADDRESS	00000000h
50201498h	4	DMA_CH7_RXDESC_LIST_HADDRESS	00000000h
5020149Ch	4	DMA_CH7_RXDESC_LIST_ADDRESS	00000000h
502014A0h	4	DMA_CH7_TXDESC_TAIL_POINTER	00000000h
502014A8h	4	DMA_CH7_RXDESC_TAIL_POINTER	00000000h
502014ACh	4	DMA_CH7_TXDESC_RING_LENGTH	00000000h
502014B0h	4	DMA_CH7_RXDESC_RING_LENGTH	00000000h
502014B4h	4	DMA_CH7_INTERRUPT_ENABLE	00000000h
502014B8h	4	DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502014BCh	4	DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502014C4h	4	DMA_CH7_CURRENT_APP_TXDESC	00000000h
502014CCh	4	DMA_CH7_CURRENT_APP_RXDESC	00000000h
502014D0h	4	DMA_CH7_CURRENT_APP_TXBUFFER_H	00000000h
502014D4h	4	DMA_CH7_CURRENT_APP_TXBUFFER	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502014D8h	4	DMA_CH7_CURRENT_APP_RXBUFFER_H	00000000h
502014DCh	4	DMA_CH7_CURRENT_APP_RXBUFFER	00000000h
502014E0h	4	DMA_CH7_STATUS	00000000h
502014E4h	4	DMA_CH7_MISS_FRAME_CNT	00000000h
502014E8h	4	DMA_CH7_RXP_ACCEPT_CNT	00000000h
502014ECh	4	DMA_CH7_RX_ERI_CNT	00000000h

14.20.1.1 MAC_CONFIGURATION — Offset 50200000h

The MAC Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50200000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ARP Offload Enable (ARPEN):** When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. 0x0 (DISABLE): ARP Offload is disabled. 0x1 (ENABLE): ARP Offload is enabled.
30:28	0h RW	**Source Address Insertion or Replacement Control (SARC):** This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: - The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: - Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field. 0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field. 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field. 0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field..
27	0h RW	**Checksum Offload (IPC):** When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. 0x0 (DISABLE): IP header/payload checksum checking is disabled. 0x1 (ENABLE): IP header/payload checksum checking is enabled.

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Inter-Packet Gap (IPG):** These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. 0x0 (IPG96): 96 bit times IPG. 0x1 (IPG88): 88 bit times IPG. 0x2 (IPG80): 80 bit times IPG. 0x3 (IPG72): 72 bit times IPG. 0x4 (IPG64): 64 bit times IPG. 0x5 (IPG56): 56 bit times IPG. 0x6 (IPG48): 48 bit times IPG. 0x7 (IPG40): 40 bit times IPG.
23	0h RW	**Giant Packet Size Limit Control Enable (GPSLCE):** When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. 0x0 (DISABLE): Giant Packet Size Limit Control is disabled. 0x1 (ENABLE): Giant Packet Size Limit Control is enabled.
22	0h RW	**IEEE 802.3as Support for 2K Packets (S2KP):** When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. 0x0 (DISABLE): Support upto 2K packet is disabled. 0x1 (ENABLE): Support upto 2K packet is Enabled.
21	0h RW	**CRC stripping for Type packets (CST):** When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. 0x0 (DISABLE): CRC stripping for Type packets is disabled. 0x1 (ENABLE): CRC stripping for Type packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Automatic Pad or CRC Stripping (ACS):** When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. 0x0 (DISABLE): Automatic Pad or CRC Stripping is disabled. 0x1 (ENABLE): Automatic Pad or CRC Stripping is enabled..
19	0h RW	**Watchdog Disable (WD):** When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. 0x0 (ENABLE): Watchdog is enabled. 0x1 (DISABLE): Watchdog is disabled.
18	0h RW	**Packet Burst Enable (BE)**: When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0x0 (DISABLE): Packet Burst is disabled. 0x1 (ENABLE): Packet Burst is enabled..
17	0h RW	**Jabber Disable (JD):** When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. 0x0 (ENABLE): Jabber is enabled. 0x1 (DISABLE): Jabber is disabled.
16	0h RW	**Jumbo Packet Enable (JE):** When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0x0 (DISABLE): Jumbo packet is disabled. 0x1 (ENABLE): Jumbo packet is enabled.
15	0h RW	**Port Select (PS):** This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read/write (R/W). 0x0 (M_1000_2500M): For 1000 or 2500 Mbps operations. 0x1 (M_10_100M): For 10 or 100 Mbps operations.
14	0h RW	**FES:** This bit selects the speed mode. 0x0 (M_10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0. 0x1 (M_100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0.
13	0h RW	**Duplex Mode (DM):** When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the fullduplex-only configurations. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Loopback Mode (LM):** When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. 0x0 (DISABLE): Loopback is disabled. 0x1 (ENABLE): Loopback is enabled.
11	0h RW	**Enable Carrier Sense Before Transmission in Full-Duplex Mode (ECRSFD):** When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal. 0x0 (DISABLE): ECRSFD is disabled. 0x1 (ENABLE): ECRSFD is enabled.
10	0h RW	**Disable Receive Own (DO):** When this bit is set, the MAC disables the reception of packets when the GMII signal TX_EN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode. 0x0 (ENABLE): Enable Receive Own. 0x1 (DISABLE): Disable Receive Own.
9	0h RW	**Disable Carrier Sense During Transmission (DCRS)**: When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. 0x0 (ENABLE): Enable Carrier Sense During Transmission. 0x1 (DISABLE): Disable Carrier Sense During Transmission.
8	0h RW	**Disable Retry (DR):** When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. 0x0 (ENABLE): Enable Retry. 0x1 (DISABLE): Disable Retry.
7	0h RO	**Reserved**
6:5	0h RW	**Back-Off Limit (BL):** The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. 0x0 (MIN_N_10): k = min(n,10). 0x1 (MIN_N_8): k = min(n,8). 0x2 (MIN_N_4): k = min(n,4). 0x3 (MIN_N_1): k = min(n,1).

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Deferral Check (DC):** When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. 0x0 (DISABLE): Deferral check function is disabled. 0x1 (ENABLE): Deferral check function is enabled.
3:2	0h RW	**Preamble Length for Transmit packets (PRELEN):** These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 0x0 (M_7BYTES): 7 bytes of preamble. 0x1 (M_5BYTES): 5 bytes of preamble. 0x2 (M_3BYTES): 3 bytes of preamble. 0x3 (RESERVED): Reserved.
1	0h RW	**Transmitter Enable (TE):** When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. 0x0 (DISABLE): Transmitter is disabled. 0x1 (ENABLE): Transmitter is enabled.
0	0h RW	**Receiver Enable (RE):** When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. 0x0 (DISABLE): Receiver is disabled. 0x1 (ENABLE): Receiver is enabled.

14.20.1.2 MAC_EXT_CONFIGURATION — Offset 50200004h

The MAC Extended Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50200004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**ARP Packet Drop if IP Mismatch (APDIM):** When set, Packet for which Target Protocol Address does not match IPv4 address is dropped in the MTL layer. When reset, when target Protocol Address does not match, packet is forwarded to MTL maintaining backward compatibility. 0x0 (DISABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address disabled. 0x1 (ENABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address enabled.
29:25	00h RW	**Extended Inter-Packet Gap (EIPG):** The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	0h RW	**Extended Inter-Packet Gap Enable (EIPGEN):** When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. 0x0 (DISABLE): Extended Inter-Packet Gap is disabled. 0x1 (ENABLE): Extended Inter-Packet Gap is enabled.
23	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**Maximum Size for Splitting the Header Data (HDSMS):** These bits indicate the maximum header size allowed for splitting the header data in the received packet. 0x0 (M_64BYTES): Maximum Size for Splitting the Header Data is 64 bytes. 0x1 (M_128BYTES): Maximum Size for Splitting the Header Data is 128 bytes. 0x2 (M_256BYTES): Maximum Size for Splitting the Header Data is 256 bytes. 0x3 (M_512BYTES): Maximum Size for Splitting the Header Data is 512 bytes. 0x4 (M_1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes. 0x5 (RSVD): Reserved.
19	0h RW	**Packet Duplication Control (PDC):** When this bit is set, the received packet with Multicast/Broadcast Destination address is routed to multiple Receive DMA Channels. The Receive DMA Channels is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Multicast/Broadcast Destination address in the received packet. The DCS field is interpreted to be a one-hot value, each bit corresponding to the Receive DMA Channel. When this bit is reset, the received packet is routed to single Receive DMA Channel. The Receive DMA Channel is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Destination address in the received packet. The DCS field is interpreted as a binary value. 0x0 (DISABLE): Packet Duplication Control is disabled. 0x1 (ENABLE): Packet Duplication Control is enabled.
18	0h RW	**Unicast Slow Protocol Packet Detect (USP):** When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. 0x0 (DISABLE): Unicast Slow Protocol Packet Detection is disabled. 0x1 (ENABLE): Unicast Slow Protocol Packet Detection is enabled.
17	0h RW	**Slow Protocol Detection Enable (SPEN):** When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. 0x0 (DISABLE): Slow Protocol Detection is disabled. 0x1 (ENABLE): Slow Protocol Detection is enabled.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Disable CRC Checking for Received Packets (DCRCC):** When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. 0x0 (ENABLE): CRC Checking is enabled. 0x1 (DISABLE): CRC Checking is disabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Giant Packet Size Limit (GPSL):** If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

14.20.1.3 MAC_PACKET_FILTER — Offset 50200008h

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.

Type	Size	Offset	Default
MMIO	32 bit	50200008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Receive All (RA):** When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled. 0x1 (ENABLE): Receive All is enabled.
30:22	0h RO	**Reserved**
21	0h RW	**Drop Non-TCP/UDP over IP Packets (DNTU):** When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0 (FWD): Forward Non-TCP/UDP over IP Packets. 0x1 (DROP): Drop Non-TCP/UDP over IP Packets.
20	0h RW	**Layer 3 and Layer 4 Filter Enable (IPFE):** When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled. 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled.
19:17	0h RO	**Reserved**
16	0h RW	**VLAN Tag Filter Enable (VTFE):** When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. 0x0 (DISABLE): VLAN Tag Filter is disabled. 0x1 (ENABLE): VLAN Tag Filter is enabled.
15:11	0h RO	**Reserved**
10	0h RW	**Hash or Perfect Filter (HPF):** When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. 0x0 (DISABLE): Hash or Perfect Filter is disabled. 0x1 (ENABLE): Hash or Perfect Filter is enabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Source Address Filter Enable (SAF):** When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in GbE Controller, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA. 0x0 (DISABLE): SA Filtering is disabled. 0x1 (ENABLE): SA Filtering is enabled.
8	0h RW	**SA Inverse Filtering (SAIF):** When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0 (DISABLE): SA Inverse Filtering is disabled. 0x1 (ENABLE): SA Inverse Filtering is enabled.
7:6	0h RW	**Pass Control Packets (PCF):** These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0x0 (FLTR_ALL): MAC filters all control packets from reaching the application. 0x1 (FW_XCPT_PAU): MAC forwards all control packets except Pause packets to the application even if they fail the Address filter. 0x2 (FW_ALL): MAC forwards all control packets to the application even if they fail the Address filter. 0x3 (FW_PASS): MAC forwards the control packets that pass the Address filter.
5	0h RW	**Disable Broadcast Packets (DBF):** When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. 0x0 (ENABLE): Enable Broadcast Packets. 0x1 (DISABLE): Disable Broadcast Packets.
4	0h RW	**Pass All Multicast (PM):** When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. 0x0 (DISABLE): Pass All Multicast is disabled. 0x1 (ENABLE): Pass All Multicast is enabled.
3	0h RW	**DA Inverse Filtering (DAIF):** When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. 0x0 (DISABLE): DA Inverse Filtering is disabled. 0x1 (ENABLE): DA Inverse Filtering is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Hash Multicast (HMC):** When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Multicast is disabled. 0x1 (ENABLE): Hash Multicast is enabled.
1	0h RW	**Hash Unicast (HUC):** When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Unicast is disabled. 0x1 (ENABLE): Hash Unicast is enabled.
0	0h RW	**Promiscuous Mode (PR):** When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. 0x0 (DISABLE): Promiscuous Mode is disabled. 0x1 (ENABLE): Promiscuous Mode is enabled.

14.20.1.4 MAC_WATCHDOG_TIMEOUT — Offset 5020000Ch

The Watchdog Timeout register controls the watchdog timeout for received packets.

Type	Size	Offset	Default
MMIO	32 bit	5020000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Programmable Watchdog Enable (PWE):** When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. 0x0 (DISABLE): Programmable Watchdog is disabled. 0x1 (ENABLE): Programmable Watchdog is enabled.
7:4	0h RO	**Reserved**
3:0	0h RW	**Watchdog Timeout (WTO):** When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. 0x0 (M_2KBYTES): 2 KB. 0x1 (M_3KBYTES): 3 KB. 0x2 (M_4KBYTES): 4 KB. 0x3 (M_5KBYTES): 5 KB. 0x4 (M_6KBYTES): 6 KB. 0x5 (M_7KBYTES): 7 KB. 0x6 (M_8KBYTES): 8 KB. 0x7 (M_9KBYTES): 9 KB. 0x08 (M_10KBYTES): 10 KB. 0x09 (M_11KBYTES): 11 KB. 0x0A (M_12KBYTES): 12 KB. 0x0B (M_13KBYTES): 13 KB. 0x0C (M_14KBYTES): 14 KB. 0x0D (M_15KBYTES): 15 KB. 0x0E (M_16383BYTES): 16383 Bytes. 0x0F (RESERVED): Reserved.

14.20.1.5 MAC_HASH_TABLE_REG0 — Offset 50200010h

The Hash Table Register 0 contains the first 32 bits of the hash table, when the width of the hash table is 128 or 256 bits.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:
- Calculate the 32-bit CRC for the DA
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the

corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50200010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table First 32 Bits (HT31T0):** This field contains the first 32 Bits [31:0] of the Hash table.

14.20.1.6 MAC_HASH_TABLE_REG1 — Offset 50200014h

The Hash Table Register 1 contains the second 32 bits of the hash table.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:
- Calculate the 32-bit CRC for the DA.
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50200014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table Second 32 Bits (HT63T32):** This field contains the second 32 Bits [63:32] of the Hash table.

14.20.1.7 MAC_VLAN_TAG_CTRL — Offset 50200050h

This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers.

Type	Size	Offset	Default
MMIO	32 bit	50200050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Inner VLAN Tag in Rx Status (EIVLRXS):** When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled. 0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled.
30	0h RO	**Reserved**
29:28	0h RW	**Enable Inner VLAN Tag Stripping on Receive (EIVLS):** This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** When this bit, VTHM bit and the EDVLP field are set, the MAC receiver enables VLAN Hash filtering operation on the inner VLAN Tag (if present). When this bit is reset and VTHM bit is set, the MAC receiver enables VLAN Hash filtering operation on the outer VLAN Tag (if present). The ERSVLM bit and DOVLTC bit determines which VLAN type is enabled for filtering. 0x0 (DISABLE): Inner VLAN tag is disabled. 0x1 (ENABLE): Inner VLAN tag is enabled.
26	0h RW	**Enable Double VLAN Processing (EDVLP):** When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0 (DISABLE): Double VLAN Processing is disabled. 0x1 (ENABLE): Double VLAN Processing is enabled.
25	0h RW	**VLAN Tag Hash Table Match Enable (VTHM):** When this bit is set, the most significant four bits of CRC of VLAN Tag are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled. 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled.
24	0h RW	**Enable VLAN Tag in Rx status (EVLRXS):** When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. 0x0 (DISABLE): VLAN Tag in Rx status is disabled. 0x1 (ENABLE): VLAN Tag in Rx status is enabled.
23	0h RO	**Reserved**
22:21	0h RW	**Enable VLAN Tag Stripping on Receive (EVLS):** This field indicates the stripping operation on the outer VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
20	0h RW	**Disable VLAN Type Check for VLAN Hash Filtering (DOVLTC):** When this bit is set, the MAC VLAN Hash Filter does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC VLAN Hash Filter filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. 0x0 (ENABLE): VLAN Type Check is enabled. 0x1 (DISABLE): VLAN Type Check is disabled.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Enable Receive S-VLAN Match for VLAN Hash Filtering (ERSVLM):** When this bit is set, the MAC receiver enables VLAN Hash filtering or matching for SVLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables VLAN Hash filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for VLAN Hash filtering or matching. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	**Enable S-VLAN (ESVL):** When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. 0x0 (DISABLE): S-VLAN is disabled. 0x1 (ENABLE): S-VLAN is enabled.
17	0h RW	**VLAN Tag Inverse Match Enable (VTIM):** When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. 0x0 (DISABLE): VLAN Tag Inverse Match is disabled. 0x1 (ENABLE): VLAN Tag Inverse Match is enabled.
16	0h RW	**Enable 12-Bit VLAN Tag Comparison for VLAN Hash Filtering (ETV):** When this bit is set, a 12-bit VLAN identifier is used for VLAN Hash filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag in the received VLAN-tagged packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for VLAN hash filtering. 0x0 (DISABLE): 12-Bit VLAN Tag Comparison is disabled. 0x1 (ENABLE): 12-Bit VLAN Tag Comparison is enabled.
15:5	0h RO	**Reserved**
4:2	0h RW	**OFS:** This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	0h RW	**Command Type (CT):** This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation. 0x0 (WRITE): Write operation. 0x1 (READ): Read operation.
0	0h RW	**Operation Busy (OB):** This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset. 0x0 (DISABLE): Operation Busy is disabled. 0x1 (ENABLE): Operation Busy is enabled.

14.20.1.8 MAC_VLAN_TAG_DATA — Offset 50200054h

This register holds the read/write data for Indirect Access of the Per VLAN Tag registers. During the read access, this field contains valid read data only after the OB bit is reset. During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register.

Type	Size	Offset	Default
MMIO	32 bit	50200054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:25	0h RW	**DMA Channel Number (DMACHN):** The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	0h RW	**DMA Channel Number Enable (DMACHEN):** This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing. 0x0 (DISABLE): DMA Channel Number is disabled. 0x1 (ENABLE): DMA Channel Number is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** This bit is valid only when Double VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). 0x0 (DISABLE): Inner VLAN tag comparison is disabled. 0x1 (ENABLE): Inner VLAN tag comparison is enabled.
19	0h RW	**Enable S-VLAN Match for received Frames (ERSVLM):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Disable VLAN Type Comparison (DOVLTC):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit. 0x0 (ENABLE): VLAN type comparison is enabled. 0x1 (DISABLE): VLAN type comparison is disabled.
17	0h RW	**12bits or 16bits VLAN comparison (ETV):** This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. 0x0 (M_16BIT): 16 bit VLAN comparison. 0x1 (M_12BIT): 12 bit VLAN comparison.
16	0h RW	**VLAN Tag Enable (VEN):** This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields. 0x0 (DISABLE): VLAN Tag is disabled. 0x1 (ENABLE): VLAN Tag is enabled.
15:0	0000h RW	**VLAN Tag ID (VID):** This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

14.20.1.9 MAC_VLAN_HASH_TABLE — Offset 50200058h

When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. The upper four bits of the calculated hash value are used to index the contents of the VLAN Hash table. For example, hash value of 4b'1000 selects Bit 8 of the VLAN Hash table.

The hash value of the destination address is calculated in the following way:
- Calculate the 32-bit CRC for the VLAN tag or ID.
- Perform bitwise reversal for the value obtained in step 1.
- Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] of this register are written.
- If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50200058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**VLAN Hash Table (VLHT):** This field contains the 16-bit VLAN Hash Table.

14.20.1.10 MAC_VLAN_INCL — Offset 50200060h

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	50200060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BUSY:** This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register. 0x0 (INACTIVE): Busy status not detected. 0x1 (ACTIVE): Busy status detected.
30	0h RW	**Read write control (RDWR):** This bit controls the read or write operation for indirectly accessing the queue/ channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset. 0x0 (READ): Read operation of indirect access. 0x1 (WRITE): Write operation of indirect access.
29:27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**ADDR:** This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset.
23:22	0h RO	**Reserved**
21	0h RW	**Channel based tag insertion (CBTI):** When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register. 0x0 (DISABLE): Channel based tag insertion is disabled. 0x1 (ENABLE): Channel based tag insertion is enabled.
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted in the 13th and 14th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

14.20.1.11 MAC_INNER_VLAN_INCL — Offset 50200064h

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	50200064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 17th and 18th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 17th and 18th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

14.20.1.12 MAC_Q0_TX_FLOW_CTRL — Offset 50200070h

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The Busy bit remains set until the control packet is transferred onto the cable. The application must make sure that the Busy bit is cleared before writing to the register. When the PFCE bit in the MAC_Rx_Flow_Ctrl register is enabled, this register controls the generation of Priority Flow Control (PFC) frames with priorities mapped according to PSRQ0 in the MAC_RxQ_Ctrl2 register.

Type	Size	Offset	Default
MMIO	32 bit	50200070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy or Backpressure Activate (FCB_BPA):** This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

14.20.1.13 MAC_Q1_TX_FLOW_CTRL — Offset 50200074h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	50200074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

14.20.1.14 MAC_Q2_TX_FLOW_CTRL — Offset 50200078h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50200074h.

14.20.1.15 MAC_Q3_TX_FLOW_CTRL — Offset 5020007Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50200074h.

14.20.1.16 MAC_Q4_TX_FLOW_CTRL — Offset 50200080h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50200074h.

14.20.1.17 MAC_Q5_TX_FLOW_CTRL — Offset 50200084h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50200074h.

14.20.1.18 MAC_Q6_TX_FLOW_CTRL — Offset 50200088h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50200074h.

14.20.1.19 MAC_Q7_TX_FLOW_CTRL — Offset 5020008Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50200074h.

14.20.1.20 MAC_RX_FLOW_CTRL — Offset 50200090h

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

Type	Size	Offset	Default
MMIO	32 bit	50200090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Priority Based Flow Control Enable (PFCE):** When this bit is set, it enables generation and reception of priority-based flow control (PFC) packets. When this bit is reset, it enables generation and reception of 802.3x Pause control packets. 0x0 (DISABLE): Priority Based Flow Control is disabled. 0x1 (ENABLE): Priority Based Flow Control is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Unicast Pause Packet Detect (UP):** A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. 0x0 (DISABLE): Unicast Pause Packet Detect disabled. 0x1 (ENABLE): Unicast Pause Packet Detect enabled.
0	0h RW	**Receive Flow Control Enable (RFE):** When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. 0x0 (DISABLE): Receive Flow Control is disabled. 0x1 (ENABLE): Receive Flow Control is enabled.

14.20.1.21 MAC_RXQ_CTRL4 — Offset 50200094h

The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	50200094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW	**VLAN Tag Filter Fail Packets Queue (VFFQ):** This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	0h RW	**VLAN Tag Filter Fail Packets Queuing Enable (VFFQE):** When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled.
15:12	0h RO	**Reserved**
11:9	0h RW	**Multicast Address Filter Fail Packets Queue. (MFFQ):** This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
8	0h RW	**Multicast Address Filter Fail Packets Queuing Enable. (MFFQE):** When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3:1	0h RW	**Unicast Address Filter Fail Packets Queue. (UFFQ):** This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	0h RW	**Unicast Address Filter Fail Packets Queuing Enable. (UFFQE):** When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled.

14.20.1.22 MAC_TXQ_PRTY_MAP0 — Offset 50200098h

The Transmit Queue Priority Mapping 0 register contains the priority values assigned to Tx Queue 0 through Tx Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	50200098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 3 (PSTQ3):** This bit is similar to the PSTQ0 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 2 (PSTQ2):** This bit is similar to the PSTQ0 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 1 (PSTQ1):** This bit is similar to the PSTQ0 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 0 (PSTQ0):** This field holds the priorities assigned to Tx Queue 0 by the software. This field determines if Tx Queue 0 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

14.20.1.23 MAC_TXQ_PRTY_MAP1 — Offset 5020009Ch

The Transmit Queue Priority Mapping 1 register contains the priority values assigned to Tx Queue 4 through Tx Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	5020009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 7 (PSTQ7):** This bit is similar to the PSTQ4 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 6 (PSTQ6):** This bit is similar to the PSTQ4 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 5 (PSTQ5):** This bit is similar to the PSTQ4 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 4 (PSTQ4):** This field holds the priorities assigned to Tx Queue 4 by the software. This field determines if Tx Queue 4 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

14.20.1.24 MAC_RXQ_CTRL0 — Offset 502000A0h

The Receive Queue Control 0 register controls the queue management in the MAC Receiver.

Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

Type	Size	Offset	Default
MMIO	32 bit	502000A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:14	0h RW	**Receive Queue 7 Enable (RXQ7EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
13:12	0h RW	**Receive Queue 6 Enable (RXQ6EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
11:10	0h RW	**Receive Queue 5 Enable (RXQ5EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
9:8	0h RW	**Receive Queue 4 Enable (RXQ4EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
7:6	0h RW	**Receive Queue 3 Enable (RXQ3EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Receive Queue 2 Enable (RXQ2EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
3:2	0h RW	**Receive Queue 1 Enable (RXQ1EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
1:0	0h RW	**Receive Queue 0 Enable (RXQ0EN):** This field indicates whether Rx Queue 0 is enabled for AV or DCB. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

14.20.1.25 MAC_RXQ_CTRL1 — Offset 502000A4h

The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	502000A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**OMCBCQ:** 0x0 (DISABLE): overriding MCBCQ priority disabled. 0x1 (ENABLE): overriding MCBCQ priority enabled.
27	0h RO	**Reserved**
26:24	0h RW	**Frame Preemption Residue Queue (FPRQ):** This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RW	**Tagged PTP over Ethernet Packets Queuing Control. (TPQC):** This field controls the routing of the VLAN Tagged PTPoE packets. The following programmable options are allowed. - 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). - 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). - 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. - 2'b11: Reserved
21	0h RW	**Tagged AV Control Packets Queuing Enable. (TACPQE):** When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers. 0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled. 0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled.
20	0h RW	**Multicast and Broadcast Queue Enable (MCBCQEN):** This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. 0x0 (DISABLE): Multicast and Broadcast Queue is disabled. 0x1 (ENABLE): Multicast and Broadcast Queue is enabled.
19	0h RO	**Reserved**
18:16	0h RW	**Multicast and Broadcast Queue (MCBCQ):** This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
15	0h RO	**Reserved**
14:12	0h RW	**Untagged Packet Queue (UPQ):** This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**DCB Control Packets Queue (DCBCPQ):** This field specifies the Rx queue on which the received DCB control packets are routed. The DCB data packets are routed based on the PSRQ field of the Transmit Flow Control Register of corresponding queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
7	0h RO	**Reserved**
6:4	0h RW	**PTP Packets Queue (PTPQ):** This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
3	0h RO	**Reserved**
2:0	0h RW	**AV Untagged Control Packets Queue (AVCPQ):** This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.

14.20.1.26 MAC_RXQ_CTRL2 — Offset 502000A8h

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3.

Type	Size	Offset	Default
MMIO	32 bit	502000A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 3 (PSRQ3):** This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 3 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 2 (PSRQ2):** This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 2 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 1 (PSRQ1):** This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 0 (PSRQ0):** This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.

14.20.1.27 MAC_RXQ_CTRL3 — Offset 502000ACh

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 4 to 7.

Type	Size	Offset	Default
MMIO	32 bit	502000ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 7 (PSRQ7):** This field decides the priorities assigned to Rx Queue 7. All packets with priorities that match the values set in this field are routed to Rx Queue 7. For example, if PSRQ7[7, 4] are set, packets with USP field equal to 7 or 4 are routed to Rx Queue 7. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 7 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 6 (PSRQ6):** This field decides the priorities assigned to Rx Queue 6. All packets with priorities that match the values set in this field are routed to Rx Queue 6. For example, if PSRQ6[5] are set, packets with USP field equal to 5 are routed to Rx Queue 6. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 6 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 5 (PSRQ5):** This field decides the priorities assigned to Rx Queue 5. All packets with priorities that match the values set in this field are routed to Rx Queue 5. For example, if PSRQ5[6] is set, packets with USP field equal to 6 are routed to Rx Queue 5. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 5 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 4 (PSRQ4):** This field decides the priorities assigned to Rx Queue 4. All packets with priorities that match the values set in this field are routed to Rx Queue 4. For example, if PSRQ4[7:4] is set, packets with USP field equal to 7, 6, 5, or 4 are routed to Rx Queue 4. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 4 crosses the flow control threshold settings.

14.20.1.28 MAC_INTERRUPT_STATUS — Offset 502000B0h

The Interrupt Status register contains the status of interrupts.

Type	Size	Offset	Default
MMIO	32 bit	502000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**MMC FPE Receive Interrupt Status (MFRIS):** This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active. 0x1 (ACTIVE): MMC FPE Receive Interrupt status active.
19	0h RO	**MMC FPE Transmit Interrupt Status (MFTIS):** This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active. 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active.
18	0h RO	**MDIO Interrupt Status (MDIOIS):** This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): MDIO Interrupt status not active. 0x1 (ACTIVE): MDIO Interrupt status active.
17	0h RO	**Frame Preemption Interrupt Status (FPEIS):** This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt. 0x0 (INACTIVE): Frame Preemption Interrupt status not active. 0x1 (ACTIVE): Frame Preemption Interrupt status active.
16	0h RO	**Reserved**
15	0h RO	**GPI Interrupt Status (GPIIS):** When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field of the MAC_GPIO_Status register and the corresponding GPIE bit is enabled in the MAC_GPIO_Control register. This bit is cleared on reading lane 0 (GPIS) of the MAC_GPIO_Status register. 0x0 (INACTIVE): GPI Interrupt status not active. 0x1 (ACTIVE): GPI Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Receive Status Interrupt (RXSTSIS):** This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Receive Interrupt status not active. 0x1 (ACTIVE): Receive Interrupt status active.
13	0h RO	**Transmit Status Interrupt (TXSTSIS):** This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Transmit Interrupt status not active. 0x1 (ACTIVE): Transmit Interrupt status active.
12	0h RO	**Timestamp Interrupt Status (TSIS):** If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: - The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. - There is an overflow in the Seconds register. - The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. 0x0 (INACTIVE): Timestamp Interrupt status not active. 0x1 (ACTIVE): Timestamp Interrupt status active.
11	0h RO	**MMC Receive Checksum Offload Interrupt Status (MMCRXIPIS):** This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. 0x0 (INACTIVE): MMC Receive Checksum Offload Interrupt status not active. 0x1 (ACTIVE): MMC Receive Checksum Offload Interrupt status active.
10	0h RO	**MMC Transmit Interrupt Status (MMCTXIS):** This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Transmit Interrupt status not active. 0x1 (ACTIVE): MMC Transmit Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**MMC Receive Interrupt Status (MMCRXIS):** This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Receive Interrupt status not active. 0x1 (ACTIVE): MMC Receive Interrupt status active.
8	0h RO	**MMC Interrupt Status (MMCIS):** This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Interrupt status not active. 0x1 (ACTIVE): MMC Interrupt status active.
7:6	0h RO	**Reserved**
5	0h RO	**LPI Interrupt Status (LPIIS):** When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): LPI Interrupt status not active. 0x1 (ACTIVE): LPI Interrupt status active.
4	0h RO	**PMT Interrupt Status (PMTIS):** This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. 0x0 (INACTIVE): PMT Interrupt status not active. 0x1 (ACTIVE): PMT Interrupt status active.
3	0h RO	**PHY Interrupt (PHYIS):** This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): PHY Interrupt not detected. 0x1 (ACTIVE): PHY Interrupt detected.
2:1	0h RO	**Reserved**
0	0h RO	**RGMII or SMII Interrupt Status (RGSMIIIS):** This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active. 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active.

14.20.1.29 MAC_INTERRUPT_ENABLE — Offset 502000B4h

The Interrupt Enable register contains the masks for generating the interrupts.

Type	Size	Offset	Default
MMIO	32 bit	502000B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**MDIO Interrupt Enable (MDIOIE):** When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): MDIO Interrupt is disabled. 0x1 (ENABLE): MDIO Interrupt is enabled.
17	0h RW	**Frame Preemption Interrupt Enable (FPEIE):** When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): Frame Preemption Interrupt is disabled. 0x1 (ENABLE): Frame Preemption Interrupt is enabled.
16:15	0h RO	**Reserved**
14	0h RW	**Receive Status Interrupt Enable (RXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Receive Status Interrupt is disabled. 0x1 (ENABLE): Receive Status Interrupt is enabled.
13	0h RW	**Transmit Status Interrupt Enable (TXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Status Interrupt is disabled. 0x1 (ENABLE): Timestamp Status Interrupt is enabled.
12	0h RW	**Timestamp Interrupt Enable (TSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Interrupt is disabled. 0x1 (ENABLE): Timestamp Interrupt is enabled.
11:6	0h RO	**Reserved**
5	0h RW	**LPI Interrupt Enable (LPIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): LPI Interrupt is disabled. 0x1 (ENABLE): LPI Interrupt is enabled.
4	0h RW	**PMT Interrupt Enable (PMTIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PMT Interrupt is disabled. 0x1 (ENABLE): PMT Interrupt is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PHY Interrupt Enable (PHYIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PHY Interrupt is disabled. 0x1 (ENABLE): PHY Interrupt is enabled.
2:1	0h RO	**Reserved**
0	0h RW	**RGMII or SMII Interrupt Enable (RGSMIIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): RGMII or SMII Interrupt is disabled. 0x1 (ENABLE): RGMII or SMII Interrupt is enabled.

14.20.1.30 MAC_RX_TX_STATUS — Offset 502000B8h

The Receive Transmit Status register contains the Receive and Transmit Error status.

Type	Size	Offset	Default
MMIO	32 bit	502000B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO	**Receive Watchdog Timeout (RWT):** This bit is set when a packet with length greater than 2,048 bytes is received (10,240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No receive watchdog timeout. 0x1 (ACTIVE): Receive watchdog timed out.
7:6	0h RO	**Reserved**
5	0h RO	**Excessive Collisions (EXCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Excessive collision is sensed.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Late Collision (LCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Late collision is sensed.
3	0h RO	**Excessive Deferral (EXDEF):** When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Excessive deferral. 0x1 (ACTIVE): Excessive deferral.
2	0h RO	**Loss of Carrier (LCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): Loss of carrier.
1	0h RO	**No Carrier (NCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): No carrier.
0	0h RO	**Transmit Jabber Timeout (TJT):** This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Transmit Jabber Timeout. 0x1 (ACTIVE): Transmit Jabber Timeout occurred.

14.20.1.31 MAC_PMT_CONTROL_STATUS — Offset 502000C0h

The PMT Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	502000C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Remote Wake-Up Packet Filter Register Pointer Reset (RWKFILTRST):** When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-Up Packet Filter Register Pointer is not Reset. 0x1 (ENABLE): Remote Wake-Up Packet Filter Register Pointer is Reset.
30:29	0h RO	**Reserved**
28:24	00h RO	**Remote Wake-up FIFO Pointer (RWKPTR):** This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	0h RO	**Reserved**
10	0h RW	**Remote Wake-up Packet Forwarding Enable (RWKPFE):** When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-up Packet Forwarding is disabled. 0x1 (ENABLE): Remote Wake-up Packet Forwarding is enabled.
9	0h RW	**Global Unicast (GLBLUCAST):** When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. 0x0 (DISABLE): Global unicast is disabled. 0x1 (ENABLE): Global unicast is enabled.
8:7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Remote Wake-Up Packet Received (RWKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Remote wake-up packet is received. 0x1 (ACTIVE): Remote wake-up packet is received.
5	0h RO	**Magic Packet Received (MGKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Magic packet is received. 0x1 (ACTIVE): Magic packet is received.
4:3	0h RO	**Reserved**
2	0h RW	**Remote Wake-Up Packet Enable (RWKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. 0x0 (DISABLE): Remote wake-up packet is disabled. 0x1 (ENABLE): Remote wake-up packet is enabled.
1	0h RW	**Magic Packet Enable (MGKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a magic packet. 0x0 (DISABLE): Magic Packet is disabled. 0x1 (ENABLE): Magic Packet is enabled.
0	0h RW	**Power Down (PWRDWN):** When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Power down is disabled. 0x1 (ENABLE): Power down is enabled.

14.20.1.32 MAC_RWK_PACKET_FILTER — Offset 502000C4h

The TSN-GbE implements a filter lookup table programmed through the MAC_RWK_Packet_Filter register in which CRC, offset, and byte mask of the pattern embedded in the remote wakeup packet, and the filter-operation commands are programmed.

Type	Size	Offset	Default
MMIO	32 bit	502000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**RWK Packet Filter (WKUPFRMFTR):** This field contains the various controls of RWK Packet filter.

14.20.1.33 MAC_LPI_CONTROL_STATUS — Offset 502000D0h

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

Type	Size	Offset	Default
MMIO	32 bit	502000D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**LPI Tx Clock Stop Enable (LPITCSE):** When this bit is set, the MAC indicates that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not indicate that the Tx clock to MAC can be stopped after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. 0x0 (DISABLE): LPI Tx Clock Stop is disabled. 0x1 (ENABLE): LPI Tx Clock Stop is enabled.
20	0h RW	**LPI Timer Enable (LPIATE):** This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. 0x0 (DISABLE): LPI Timer is disabled. 0x1 (ENABLE): LPI Timer is enabled.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**LPI Tx Automate (LPITXA):** This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. 0x0 (DISABLE): LPI Tx Automate is disabled. 0x1 (ENABLE): LPI Tx Automate is enabled.
18	0h RW	**PHY Link Status Enable (PLSEN):** This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. 0x0 (DISABLE): PHY Link Status is disabled. 0x1 (ENABLE): PHY Link Status is enabled.
17	0h RW	**PHY Link Status (PLS):** This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. 0x0 (DISABLE): link is down. 0x1 (ENABLE): link is okay (UP).
16	0h RW	**LPI Enable (LPIEN):** When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. 0x0 (DISABLE): LPI state is disabled. 0x1 (ENABLE): LPI state is enabled.
15:10	0h RO	**Reserved**
9	0h RO	**Receive LPI State (RLPIST):** When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Receive LPI state not detected. 0x1 (ACTIVE): Receive LPI state detected.
8	0h RO	**Transmit LPI State (TLPIST):** When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Transmit LPI state not detected. 0x1 (ACTIVE): Transmit LPI state detected.
7:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Receive LPI Exit (RLPIEX):** When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI exit not detected. 0x1 (ACTIVE): Receive LPI exit detected.
2	0h RO	**Receive LPI Entry (RLPIEN):** When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI entry not detected. 0x1 (ACTIVE): Receive LPI entry detected.
1	0h RO	**Transmit LPI Exit (TLPIEX):** When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI exit not detected. 0x1 (ACTIVE): Transmit LPI exit detected.
0	0h RO	**Transmit LPI Entry (TLPIEN):** When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI entry not detected. 0x1 (ACTIVE): Transmit LPI entry detected.

14.20.1.34 MAC_LPI_TIMERS_CONTROL — Offset 502000D4h

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

Type	Size	Offset	Default
MMIO	32 bit	502000D4h	03E80000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:16	3E8h RW	**LPI LS Timer (LST):** This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	0000h RW	**LPI TW Timer (TWT):** This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

14.20.1.35 MAC_LPI_ENTRY_TIMER — Offset 502000D8h

This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	502000D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:3	00000h RW	**LPI Entry Timer (LPIET):** This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	0h RO	**Reserved**

14.20.1.36 MAC_1US_TIC_COUNTER — Offset 502000DCh

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.

Type	Size	Offset	Default
MMIO	32 bit	502000DCh	00000063h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	063h RW	**1US TIC Counter (TIC_1US_CNTR):** The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

14.20.1.37 MAC_PHYIF_CONTROL_STATUS — Offset 502000F8h

The PHY Interface Control and Status register indicates the status signals received by the SGMII, RGMII, or SMII interface (selected at reset) from the PHY. This register is optional.

Type	Size	Offset	Default
MMIO	32 bit	502000F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO	**Link Status (LNKSTS):** This bit indicates whether the link is up (1'b1) or down (1'b0). 0x0 (INACTIVE): Link down. 0x1 (ACTIVE): Link up.
18:17	0h RO	**Link Speed (LNKSPEED):** This bit indicates the current speed of the link. 0x0 (M_2500K): 2.5 MHz. 0x1 (M_25M): 25 MHz. 0x2 (M_125M): 125 MHz. 0x3 (RSVD): Reserved.
16	0h RO	**Link Mode (LNKMOD):** This bit indicates the current mode of operation of the link. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.
15:2	0h RO	**Reserved**
1	0h RW	**Link Up or Down (LUD):** This bit indicates whether the link is up or down during transmission of configuration in the RGMII or SGMII interface. 0x0 (LINKDOWN): Link down. 0x1 (LINKUP): Link up.
0	0h RW	**Transmit Configuration in RGMII or SGMII (TC):** When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: - "Reduced Gigabit Media Independent Interface" - "Serial Media Independent Interface" - "Serial Gigabit Media Independent Interface" 0x0 (DISABLE): Disable Transmit Configuration in RGMII or SGMII. 0x1 (ENABLE): Enable Transmit Configuration in RGMII or SGMII.

14.20.1.38 MAC_VERSION — Offset 50200110h

The version register identifies the version of the GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200110h	00005152h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	51h RO	**USERVER:** Version code
7:0	52h RO	**SNPSVER:** Version code

14.20.1.39 MAC_DEBUG — Offset 50200114h

The Debug register provides the debug status of various MAC blocks.

Type	Size	Offset	Default
MMIO	32 bit	50200114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RO	**MAC Transmit Packet Controller Status (TFCSTS):** This field indicates the state of the MAC Transmit Packet Controller module. 0x0 (IDLE): Idle state. 0x1 (WAITING): Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over. 0x2 (GEN_TX_PAU): Generating and transmitting a Pause control packet (in full-duplex mode). 0x3 (TRNSFR): Transferring input packet for transmission.
16	0h RO	**MAC GMII or MII Transmit Protocol Engine Status (TPESTS):** When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Transmit Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Transmit Protocol Engine Status detected.

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:1	0h RO	**MAC Receive Packet Controller FIFO Status (RFCFCSTS):** When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	0h RO	**MAC GMII or MII Receive Protocol Engine Status (RPESTS):** When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected.

14.20.1.40 MAC_HW_FEATURE0 — Offset 5020011Ch

This register indicates the presence of first set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	5020011Ch	0EFD73F7h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	0h RO	**Active PHY Selected (ACTPHYSEL):** When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. 0x0 (GMII_MII): GMII or MII. 0x1 (RGMII): RGMII. 0x2 (SGMII): SGMII. 0x3 (TBI): TBI. 0x4 (RMII): RMII. 0x5 (RTBI): RTBI. 0x6 (SMII): SMII. 0x7 (REVMIII): RevMII.
27	1h RO	**Source Address or VLAN Insertion Enable (SAVLANINS):** This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected 0x0 (INACTIVE): Source Address or VLAN Insertion Enable option is not selected. 0x1 (ACTIVE): Source Address or VLAN Insertion Enable option is selected.

Bit Range	Default & Access	Field Name (ID): Description
26:25	3h RO	**Timestamp System Time Source (TSSTSSEL):** This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INTRNL): Internal. 0x1 (EXTRNL): External. 0x2 (BOTH): Both. 0x3 (RSVD): Reserved.
24	0h RO	**MAC Addresses 64-127 Selected (MACADR64SEL):** This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected 0x0 (INACTIVE): MAC Addresses 64-127 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 64-127 Select option is selected.
23	1h RO	**MAC Addresses 32-63 Selected (MACADR32SEL):** This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected 0x0 (INACTIVE): MAC Addresses 32-63 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 32-63 Select option is selected.
22:18	1Fh RO	**MAC Addresses 1-31 Selected (ADDMACADRSEL):** This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option
17	0h RO	**Reserved**
16	1h RO	**Receive Checksum Offload Enabled (RXCOESEL):** This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected 0x0 (INACTIVE): Receive Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Receive Checksum Offload Enable option is selected.
15	0h RO	**Reserved**
14	1h RO	**Transmit Checksum Offload Enabled (TXCOESEL):** This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected 0x0 (INACTIVE): Transmit Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Transmit Checksum Offload Enable option is selected.
13	1h RO	**Energy Efficient Ethernet Enabled (EEESEL):** This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected 0x0 (INACTIVE): Energy Efficient Ethernet Enable option is not selected. 0x1 (ACTIVE): Energy Efficient Ethernet Enable option is selected.
12	1h RO	**IEEE 1588-2008 Timestamp Enabled (TSSEL):** This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INACTIVE): IEEE 1588-2008 Timestamp Enable option is not selected. 0x1 (ACTIVE): IEEE 1588-2008 Timestamp Enable option is selected.
11:10	0h RO	**Reserved**
9	1h RO	**ARP Offload Enabled (ARPOFFSEL):** This bit is set to 1 when the Enable IPv4 ARP Offload option is selected 0x0 (INACTIVE): ARP Offload Enable option is not selected. 0x1 (ACTIVE): ARP Offload Enable option is selected.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RO	**RMON Module Enable (MMCSEL):** This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected 0x0 (INACTIVE): RMON Module Enable option is not selected. 0x1 (ACTIVE): RMON Module Enable option is selected.
7	1h RO	**PMT Magic Packet Enable (MGKSEL):** This bit is set to 1 when the Enable Magic Packet Detection option is selected 0x0 (INACTIVE): PMT Magic Packet Enable option is not selected. 0x1 (ACTIVE): PMT Magic Packet Enable option is selected.
6	1h RO	**PMT Remote Wake-up Packet Enable (RWKSEL):** This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected 0x0 (INACTIVE): PMT Remote Wake-up Packet Enable option is not selected. 0x1 (ACTIVE): PMT Remote Wake-up Packet Enable option is selected.
5	1h RO	**SMA (MDIO) Interface (SMASEL):** This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected 0x0 (INACTIVE): SMA (MDIO) Interface not selected. 0x1 (ACTIVE): SMA (MDIO) Interface selected.
4	1h RO	**VLAN Hash Filter Selected (VLHASH):** This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected 0x0 (INACTIVE): VLAN Hash Filter not selected. 0x1 (ACTIVE): VLAN Hash Filter selected.
3	0h RO	**PCS Registers (TBI, SGMII, or RTBI PHY interface) (PCSSEL):** This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected 0x0 (INACTIVE): No PCS Registers (TBI, SGMII, or RTBI PHY interface). 0x1 (ACTIVE): PCS Registers (TBI, SGMII, or RTBI PHY interface).
2	1h RO	**Half-duplex Support (HDSEL):** This bit is set to 1 when the half-duplex mode is selected 0x0 (INACTIVE): No Half-duplex support. 0x1 (ACTIVE): Half-duplex support.
1	1h RO	**1000 Mbps Support (GMIISEL):** This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 1000 Mbps support. 0x1 (ACTIVE): 1000 Mbps support.
0	1h RO	**10 or 100 Mbps Support (MIISEL):** This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 10 or 100 Mbps support. 0x1 (ACTIVE): 10 or 100 Mbps support.

14.20.1.41 MAC_HW_FEATURE1 — Offset 50200120h

This register indicates the presence of second set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	50200120h	119F7A69h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	2h RO	**Total number of L3 or L4 Filters (L3L4FNUM):** This field indicates the total number of L3 or L4 filters: 0x0 (NOFILT): No L3 or L4 Filter. 0x1 (M_1FILT): 1 L3 or L4 Filter. 0x2 (M_2FILT): 2 L3 or L4 Filters. 0x3 (M_3FILT): 3 L3 or L4 Filters. 0x4 (M_4FILT): 4 L3 or L4 Filters. 0x5 (M_5FILT): 5 L3 or L4 Filters. 0x6 (M_6FILT): 6 L3 or L4 Filters. 0x7 (M_7FILT): 7 L3 or L4 Filters. 0x08 (M_8FILT): 8 L3 or L4 Filters.
26	0h RO	**Reserved**
25:24	1h RO	**Hash Table Size (HASHTBLSZ):** This field indicates the size of the hash table: 0x0 (NO_HT): No hash table. 0x1 (M_64): 64. 0x2 (M_128): 128. 0x3 (M_256): 256.
23	1h RO	**One Step for PTP over UDP/IP Feature Enable (POUOST):** This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. 0x0 (INACTIVE): One Step for PTP over UDP/IP Feature is not selected. 0x1 (ACTIVE): One Step for PTP over UDP/IP Feature is selected.
22	0h RO	**Reserved**
21	0h RO	**Rx Side Only AV Feature Enable (RAVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. 0x0 (INACTIVE): Rx Side Only AV Feature is not selected. 0x1 (ACTIVE): Rx Side Only AV Feature is selected.
20	1h RO	**AV Feature Enable (AVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option is selected. 0x0 (INACTIVE): AV Feature is not selected. 0x1 (ACTIVE): AV Feature is selected.
19	1h RO	**DMA Debug Registers Enable (DBGMEMA):** This bit is set to 1 when the Debug Mode Enable option is selected 0x0 (INACTIVE): DMA Debug Registers option is not selected. 0x1 (ACTIVE): DMA Debug Registers option is selected.

Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**TCP Segmentation Offload Enable (TSOEN):** This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected 0x0 (INACTIVE): TCP Segmentation Offload Feature is not selected. 0x1 (ACTIVE): TCP Segmentation Offload Feature is selected.
17	1h RO	**Split Header Feature Enable (SPHEN):** This bit is set to 1 when the Enable Split Header Structure option is selected 0x0 (INACTIVE): Split Header Feature is not selected. 0x1 (ACTIVE): Split Header Feature is selected.
16	1h RO	**DCB Feature Enable (DCBEN):** This bit is set to 1 when the Enable Data Center Bridging option is selected 0x0 (INACTIVE): DCB Feature is not selected. 0x1 (ACTIVE): DCB Feature is selected.
15:14	1h RO	**Address Width. (ADDR64):** This field indicates the configured address width: 0x0 (M_32): 32. 0x1 (M_40): 40. 0x2 (M_48): 48. 0x3 (RSVD): Reserved.
13	1h RO	**IEEE 1588 High Word Register Enable (ADVTHWORD):** This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected 0x0 (INACTIVE): IEEE 1588 High Word Register option is not selected. 0x1 (ACTIVE): IEEE 1588 High Word Register option is selected.
12	1h RO	**PTP Offload Enable (PTOEN):** This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. 0x0 (INACTIVE): PTP Offload feature is not selected. 0x1 (ACTIVE): PTP Offload feature is selected.
11	1h RO	**One-Step Timestamping Enable (OSTEN):** This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. 0x0 (INACTIVE): One-Step Timestamping feature is not selected. 0x1 (ACTIVE): One-Step Timestamping feature is selected.

Bit Range	Default & Access	Field Name (ID): Description
10:6	08h RO	**MTL Transmit FIFO Size (TXFIFOSIZE):** This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (RSVD): Reserved.
5	1h RO	**Single Port RAM Enable (SPRAM):** This bit is set to 1 when the Use single port RAM Feature is selected. 0x0 (INACTIVE): Single Port RAM feature is not selected. 0x1 (ACTIVE): Single Port RAM feature is selected.
4:0	08h RO	**MTL Receive FIFO Size (RXFIFOSIZE):** This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (M_256KB): 256 KB. 0x0C (RSVD): Reserved.

14.20.1.42 MAC_HW_FEATURE2 — Offset 50200124h

This register indicates the presence of third set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	50200124h	225D71C7h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	2h RO	**Number of Auxiliary Snapshot Inputs (AUXSNAPNUM):** This field indicates the number of auxiliary snapshot inputs: 0x0 (NO_AUXI): No auxiliary input. 0x1 (M_1_AUXI): 1 auxiliary input. 0x2 (M_2_AUXI): 2 auxiliary input. 0x3 (M_3_AUXI): 3 auxiliary input. 0x4 (M_4_AUXI): 4 auxiliary input. 0x5 (RSVD): Reserved.
27	0h RO	**Reserved**
26:24	2h RO	**Number of PPS Outputs (PPSOUTNUM):** This field indicates the number of PPS outputs: 0x0 (NO_PPSO): No PPS output. 0x1 (M_1_PPSO): 1 PPS output. 0x2 (M_2_PPSO): 2 PPS output. 0x3 (M_3_PPSO): 3 PPS output. 0x4 (M_4_PPSO): 4 PPS output. 0x5 (RSVD): Reserved.
23:22	3h RO	**Tx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (TDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
21:18	7h RO	**Number of DMA Transmit Channels (TXCHCNT):** This field indicates the number of DMA Transmit channels: 0x0 (M_1TXCH): 1 MTL Tx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1TDCSZ): 4. 0x1 (M_2TXCH): 2 MTL Tx Channels. 0x2 (M_2TDCSZ): 8. 0x2 (M_3TXCH): 3 MTL Tx Channels. 0x3 (M_3TDCSZ): 16. 0x3 (M_4TXCH): 4 MTL Tx Channels. 0x4 (M_5TXCH): 5 MTL Tx Channels. 0x5 (M_6TXCH): 6 MTL Tx Channels. 0x6 (M_7TXCH): 7 MTL Tx Channels. 0x7 (M_8TXCH): 8 MTL Tx Channels.

Bit Range	Default & Access	Field Name (ID): Description
17:16	3h RO	**Rx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (RDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
15:12	7h RO	**Number of DMA Receive Channels (RXCHCNT):** This field indicates the number of DMA Receive channels: 0x0 (M_1RXCH): 1 MTL Rx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1RDCSZ): 4. 0x1 (M_2RXCH): 2 MTL Rx Channels. 0x2 (M_2RDCSZ): 8. 0x2 (M_3RXCH): 3 MTL Rx Channels. 0x3 (M_3RDCSZ): 16. 0x3 (M_4RXCH): 4 MTL Rx Channels. 0x4 (M_5RXCH): 5 MTL Rx Channels. 0x5 (M_6RXCH): 6 MTL Rx Channels. 0x6 (M_7RXCH): 7 MTL Rx Channels. 0x7 (M_8RXCH): 8 MTL Rx Channels.
11:10	0h RO	**Reserved**
9:6	7h RO	**Number of MTL Transmit Queues (TXQCNT):** This field indicates the number of MTL Transmit queues: 0x0 (M_1TXQ): 1 MTL Tx Queue. 0x1 (M_2TXQ): 2 MTL Tx Queues. 0x2 (M_3TXQ): 3 MTL Tx Queues. 0x3 (M_4TXQ): 4 MTL Tx Queues. 0x4 (M_5TXQ): 5 MTL Tx Queues. 0x5 (M_6TXQ): 6 MTL Tx Queues. 0x6 (M_7TXQ): 7 MTL Tx Queues. 0x7 (M_8TXQ): 8 MTL Tx Queues.
5:4	0h RO	**Reserved**
3:0	7h RO	**Number of MTL Receive Queues (RXQCNT):** This field indicates the number of MTL Receive queues: 0x0 (M_1RXQ): 1 MTL Rx Queue. 0x1 (M_2RXQ): 2 MTL Rx Queues. 0x2 (M_3RXQ): 3 MTL Rx Queues. 0x3 (M_4RXQ): 4 MTL Rx Queues. 0x4 (M_5RXQ): 5 MTL Rx Queues. 0x5 (M_6RXQ): 6 MTL Rx Queues. 0x6 (M_7RXQ): 7 MTL Rx Queues. 0x7 (M_8RXQ): 8 MTL Rx Queues.

14.20.1.43 MAC_HW_FEATURE3 — Offset 50200128h

This register indicates the presence of fourth set the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	50200128h	2C395632h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	2h RO	**Automotive Safety Package (ASP):** Following are the encoding for the different Safety features 0x0 (NONE): No Safety features selected. 0x1 (ECC_ONLY): Only "ECC protection for external memory" feature is selected. 0x2 (AS_NPPE): All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature. 0x3 (AS_PPE): All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature.
27	1h RO	**Time Based Scheduling Enable (TBSSEL):** This bit is set to 1 when the Time Based Scheduling feature is selected. 0x0 (INACTIVE): Time Based Scheduling Enable feature is not selected. 0x1 (ACTIVE): Time Based Scheduling Enable feature is selected.
26	1h RO	**Frame Preemption Enable (FPESEL):** This bit is set to 1 when the Enable Frame preemption feature is selected. 0x0 (INACTIVE): Frame Preemption Enable feature is not selected. 0x1 (ACTIVE): Frame Preemption Enable feature is selected.
25:22	0h RO	**Reserved**
21:20	3h RO	**Width of the Time Interval field in the Gate Control List (ESTWID):** This field indicates the width of the Configured Time Interval Field 0x0 (NOWIDTH): Width not configured. 0x1 (WIDTH16): 16. 0x2 (WIDTH20): 20. 0x3 (WIDTH24): 24.
19:17	4h RO	**Depth of the Gate Control List (ESTDEP):** This field indicates the depth of Gate Control list expressed as Log2(512)-5 0x0 (NODEPTH): No Depth configured. 0x1 (DEPTH64): 64. 0x2 (DEPTH128): 128. 0x3 (DEPTH256): 256. 0x4 (DEPTH512): 512. 0x5 (DEPTH1024): 1024. 0x6 (RSVD): Reserved.
16	1h RO	**Enhancements to Scheduling Traffic Enable (ESTSEL):** This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. 0x0 (INACTIVE): Enable Enhancements to Scheduling Traffic feature is not selected. 0x1 (ACTIVE): Enable Enhancements to Scheduling Traffic feature is selected.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:13	2h RO	**Flexible Receive Parser Table Entries size (FRPES):** This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. 0x0 (M_64ENTR): 64 Entries. 0x1 (M_128ENTR): 128 Entries. 0x2 (M_256ENTR): 256 Entries. 0x3 (RSVD): Reserved.
12:11	2h RO	**Flexible Receive Parser Buffer size (FRPBS):** This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. 0x0 (M_64BYTES): 64 Bytes. 0x1 (M_128BYTES): 128 Bytes. 0x2 (M_256BYTES): 256 Bytes. 0x3 (RSVD): Reserved.
10	1h RO	**Flexible Receive Parser Selected (FRPSEL):** This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. 0x0 (INACTIVE): Flexible Receive Parser feature is not selected. 0x1 (ACTIVE): Flexible Receive Parser feature is selected.
9	1h RO	**Broadcast/Multicast Packet Duplication (PDUPSEL):** This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. 0x0 (INACTIVE): Broadcast/Multicast Packet Duplication feature is not selected. 0x1 (ACTIVE): Broadcast/Multicast Packet Duplication feature is selected.
8:6	0h RO	**Reserved**
5	1h RO	**Double VLAN Tag Processing Selected (DVLAN):** This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. 0x0 (INACTIVE): Double VLAN option is not selected. 0x1 (ACTIVE): Double VLAN option is selected.
4	1h RO	**Queue/Channel based VLAN tag insertion on Tx Enable (CBTISEL):** This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. 0x0 (INACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected. 0x1 (ACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is selected.
3	0h RO	**Reserved**
2:0	2h RO	**Number of Extended VLAN Tag Filters Enabled (NRVF):** This field indicates the Number of Extended VLAN Tag Filters selected: 0x0 (NO_ERVLAN): No Extended Rx VLAN Filters. 0x1 (M_4_ERVLAN): 4 Extended Rx VLAN Filters. 0x2 (M_8_ERVLAN): 8 Extended Rx VLAN Filters. 0x3 (M_16_ERVLAN): 16 Extended Rx VLAN Filters. 0x4 (M_24_ERVLAN): 24 Extended Rx VLAN Filters. 0x5 (M_32_ERVLAN): 32 Extended Rx VLAN Filters. 0x6 (RSVD): Reserved.

14.20.1.44 MAC_DPP_FSM_INTERRUPT_STATUS — Offset 50200140h

This register contains the status of Automotive Safety related Data Path Parity Errors, Interface Timeout Errors, FSM State Parity Errors and FSM State Timeout Errors. All the non-Reserved bits are cleared on read.

Type	Size	Offset	Default
MMIO	32 bit	50200140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**FSM State Parity Error Status (FSMPES):** This field when set indicates one of the FSMs State registers has a parity error detected. 0x0 (INACTIVE): FSM State Parity Error Status not detected. 0x1 (ACTIVE): FSM State Parity Error Status detected.
23:18	0h RO	**Reserved**
17	0h RW	**Slave Read/Write Timeout Error Status (SLVTES):** This field when set indicates that an Application/CSR Timeout has occurred on the AXI slave interface. 0x0 (INACTIVE): Slave Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Slave Read/Write Timeout Error Status detected.
16	0h RW	**Master Read/Write Timeout Error Status (MSTTES):** This field when set indicates that an Application/CSR Timeout has occurred on the master (AXI/AHB/ARI/ATI) interface. 0x0 (INACTIVE): Master Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Master Read/Write Timeout Error Status detected.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Status (PTES):** This field when set indicates that one of the PTP FSM Timeout has occurred. 0x0 (INACTIVE): PTP FSM Timeout Error Status not detected. 0x1 (ACTIVE): PTP FSM Timeout Error Status detected.
11	0h RW	**APP FSM Timeout Error Status (ATES):** This field when set indicates that one of the APP FSM Timeout has occurred. 0x0 (INACTIVE): APP FSM Timeout Error Status not detected. 0x1 (ACTIVE): APP FSM Timeout Error Status detected.
10	0h RW	**CSR FSM Timeout Error Status (CTES):** This field when set indicates that one of the CSR FSM Timeout has occurred. 0x0 (INACTIVE): CSR FSM Timeout Error Status not detected. 0x1 (ACTIVE): CSR FSM Timeout Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Rx FSM Timeout Error Status (RTES):** This field when set indicates that one of the Rx FSM Timeout has occurred. 0x0 (INACTIVE): Rx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Rx FSM Timeout Error Status detected.
8	0h RW	**Tx FSM Timeout Error Status (TTES):** This field when set indicates that one of the Tx FSM Timeout has occurred. 0x0 (INACTIVE): Tx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Tx FSM Timeout Error Status detected.
7	0h RW	**AXI Slave Read data path Parity checker Error Status (ASRPES):** This bit when set indicates that parity error is detected at the AXI Slave read data interface. 0x0 (INACTIVE): AXI Slave Read data path Parity checker Error Status not detected. 0x1 (ACTIVE): AXI Slave Read data path Parity checker Error Status detected.
6	0h RW	**CSR Write data path Parity checker Error Status (CWPES):** This bit when set indicates that parity error is detected at the CSR write data interface on mci_wdata_i (or at PC8 checker as shown in AXI slave Interface Data path parity protection diagram). When EPSI bit of MTL_DPP_Control register is set and if any parity mis-match is detected on the input slave parity ports (or at PC7 checker in the AXI slave Interface Data path parity protection diagram) sets this bit to one. 0x0 (INACTIVE): CSR Write data path Parity checker Error Status not detected. 0x1 (ACTIVE): CSR Write data path Parity checker Error Status detected.
5	0h RW	**Application Receive interface data path Parity Error Status (ARPES):** This bit when set indicates that a parity error is detected by the hardware internally at the interface with the application. 0x0 (INACTIVE): Application Receive interface data path Parity Error Status not detected. 0x1 (ACTIVE): Application Receive interface data path Parity Error Status detected.
4	0h RW	**MTL TX Status data path Parity checker Error Status (MTSPES):** This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL TX Status data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL TX Status data path Parity checker Error Status detected.
3	0h RW	**MTL data path Parity checker Error Status (MPES):** This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL data path Parity checker Error Status detected.
2	0h RW	**Read Descriptor Parity checker Error Status (RDPES):** This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): Read Descriptor Parity checker Error Status not detected. 0x1 (ACTIVE): Read Descriptor Parity checker Error Status detected.
1	0h RW	**TSO data path Parity checker Error Status (TPES):** This bit when set indicates that a parity error is detected at the DMA TSO parity checker (or at PC2 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): TSO data path Parity checker Error Status not detected. 0x1 (ACTIVE): TSO data path Parity checker Error Status detected.
0	0h R0	**Reserved**

14.20.1.45 MAC_FSM_CONTROL — Offset 50200148h

This register is used to control the FSM State parity and timeout error injection in Debug mode.

Type	Size	Offset	Default
MMIO	32 bit	50200148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**PTP Large/Normal Mode Select (PLGRNML):** This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for PTP domain. 0x1 (ENABLE): large mode tic generation is used for PTP domain.
27	0h RW	**APP Large/Normal Mode Select (ALGRNML):** This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for APP domain. 0x1 (ENABLE): large mode tic generation is used for APP domain.
26	0h RW	**CSR Large/Normal Mode Select (CLGRNML):** This field when set indicates that large mode tic generation is used for CSR domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for CSR domain. 0x1 (ENABLE): large mode tic generation is used for CSR domain.
25	0h RW	**Rx Large/Normal Mode Select (RLGRNML):** This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Rx domain. 0x1 (ENABLE): large mode tic generation is used for Rx domain.
24	0h RW	**Tx Large/Normal Mode Select (TLGRNML):** This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Tx domain. 0x1 (ENABLE): large mode tic generation is used for Tx domain.
23:21	0h RO	**Reserved**
20	0h RW	**PTP FSM Parity Error Injection (PPEIN):** This field when set indicates that Error Injection for PTP FSM Parity is enabled. 0x0 (DISABLE): PTP FSM Parity Error Injection is disabled. 0x1 (ENABLE): PTP FSM Parity Error Injection is enabled.
19	0h RW	**APP FSM Parity Error Injection (APEIN):** This field when set indicates that Error Injection for APP FSM Parity is enabled. 0x0 (DISABLE): APP FSM Parity Error Injection is disabled. 0x1 (ENABLE): APP FSM Parity Error Injection is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**CSR FSM Parity Error Injection (CPEIN):** This field when set indicates that Error Injection for CSR Parity is enabled. 0x0 (DISABLE): CSR FSM Parity Error Injection is disabled. 0x1 (ENABLE): CSR FSM Parity Error Injection is enabled.
17	0h RW	**Rx FSM Parity Error Injection (RPEIN):** This field when set indicates that Error Injection for RX FSM Parity is enabled. 0x0 (DISABLE): Rx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Rx FSM Parity Error Injection is enabled.
16	0h RW	**Tx FSM Parity Error Injection (TPEIN):** This field when set indicates that Error Injection for TX FSM Parity is enabled. 0x0 (DISABLE): Tx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Tx FSM Parity Error Injection is enabled.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Injection (PTEIN):** This field when set indicates that Error Injection for PTP FSM timeout is enabled. 0x0 (DISABLE): PTP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): PTP FSM Timeout Error Injection is enabled.
11	0h RW	**APP FSM Timeout Error Injection (ATEIN):** This field when set indicates that Error Injection for APP FSM timeout is enabled. 0x0 (DISABLE): APP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): APP FSM Timeout Error Injection is enabled.
10	0h RW	**CSR FSM Timeout Error Injection (CTEIN):** This field when set indicates that Error Injection for CSR timeout is enabled. 0x0 (DISABLE): CSR FSM Timeout Error Injection is disabled. 0x1 (ENABLE): CSR FSM Timeout Error Injection is enabled.
9	0h RW	**Rx FSM Timeout Error Injection (RTEIN):** This field when set indicates that Error Injection for RX FSM timeout is enabled. 0x0 (DISABLE): Rx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Rx FSM Timeout Error Injection is enabled.
8	0h RW	**Tx FSM Timeout Error Injection (TTEIN):** This field when set indicates that Error Injection for TX FSM timeout is enabled. 0x0 (DISABLE): Tx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Tx FSM Timeout Error Injection is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**PRTYEN:** This bit when set indicates that the FSM parity feature is enabled. 0x0 (DISABLE): FSM Parity feature is disabled. 0x1 (ENABLE): FSM Parity feature is enabled.
0	0h RW	**TMOUTEN:** This bit when set indicates that the FSM timeout feature is enabled. 0x0 (DISABLE): FSM timeout feature is disabled. 0x1 (ENABLE): FSM timeout feature is enabled.

14.20.1.46 MAC_FSM_ACT_TIMER — Offset 5020014Ch

This register is used to select the FSM and Interface Timeout values.

Type	Size	Offset	Default
MMIO	32 bit	5020014Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**LTMRMD:** This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
19:16	0h RW	**NTMRMD:** This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
15:10	0h RO	**Reserved**
9:0	000h RW	**TMR:** This field indicates the number of CSR clocks required to generate 1us tic.

14.20.1.47 SNPS_SCS_REG1 — Offset 50200150h

Reserved

Type	Size	Offset	Default
MMIO	32 bit	50200150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RO	RO	RO

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Reserved**

14.20.1.48 MAC_MDIO_ADDRESS — Offset 50200200h

The MDIO Address register controls the management cycles to external PHY through a management interface.

Type	Size	Offset	Default
MMIO	32 bit	50200200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**Preamble Suppression Enable (PSE):** When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. 0x0 (DISABLE): Preamble Suppression disabled. 0x1 (ENABLE): Preamble Suppression enabled.
26	0h RW	**Back to Back transactions (BTB):** When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. 0x0 (DISABLE): Back to Back transactions disabled. 0x1 (ENABLE): Back to Back transactions enabled.

Bit Range	Default & Access	Field Name (ID): Description
25:21	00h RW	**Physical Layer Address (PA):** This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	00h RW	**Register/Device Address (RDA):** These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	0h RO	**Reserved**
14:12	0h RW	**Number of Trailing Clocks (NTC):** This field controls the number of trailing clock cycles generated on the MDIO Clock (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	0h RW	**CSR Clock Range (CR):** The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: - 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 - 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 - 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 - 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 - 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 - 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 - 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 - 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: - 1000: CSR clock/4 - 1001: CSR clock/6 - 1010: CSR clock/8 - 1011: CSR clock/10 - 1100: CSR clock/12 - 1101: CSR clock/14 - 1110: CSR clock/16 - 1111: CSR clock/18
7:5	0h RO	**Reserved**
4	0h RW	**Skip Address Packet (SKAP):** When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0x0 (DISABLE): Skip Address Packet is disabled. 0x1 (ENABLE): Skip Address Packet is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GMII Operation Command 1 (GOC_1):** This bit is higher bit of the operation command to the PHY or GOC_1 and GOC_O are encoded as follows: - 00: Reserved - 01: Write - 10: Post Read Increment Address for Clause 45 PHY - 11: Read When Clause 22 PHY is enabled, only Write and Read commands are valid. 0x0 (DISABLE): GMII Operation Command 1 is disabled. 0x1 (ENABLE): GMII Operation Command 1 is enabled.
2	0h RW	**GMII Operation Command 0 (GOC_0):** This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. 0x0 (DISABLE): GMII Operation Command 0 is disabled. 0x1 (ENABLE): GMII Operation Command 0 is enabled.
1	0h RW	**Clause 45 PHY Enable (C45E):** When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0x0 (DISABLE): Clause 45 PHY is disabled. 0x1 (ENABLE): Clause 45 PHY is enabled.
0	0h RW	**GMII Busy (GB):** The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): GMII Busy is disabled. 0x1 (ENABLE): GMII Busy is enabled.

14.20.1.49 MAC_MDIO_DATA — Offset 50200204h

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

Type	Size	Offset	Default
MMIO	32 bit	50200204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Register Address (RA):** This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	0000h RW	**GMII Data (GD):** This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

14.20.1.50 MAC_GPIO_CONTROL — Offset 50200208h

The GPIO Control register controls the GPIO.

Type	Size	Offset	Default
MMIO	32 bit	50200208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RO	RO	RO

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.20.1.51 MAC_GPIO_STATUS — Offset 5020020Ch

The General Purpose IO register provides the control to drive the following: up to 16 bits of output ports (GPO) and status of up to 16 input ports (GPIS).

Type	Size	Offset	Default
MMIO	32 bit	5020020Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW	**Trigger Snapshot (GPO1)**: Active-high signal. The rising edge of this signal triggers snapshot of current PMC ART and System timer values. The system timer value is stored into AUX FIFO. An interrupt is generated upon snapshotting. The PMC ART timer values is stored in 4x 16-bit ART snapshot register and is read through MDIO registers. MAC_GPIO[3] / MAC_GPIO[0] / PTP REF Clock to GbE MAC: 0 / 0 / Reserved 0 / 1 / Reserved 1 / 0 / Reserved 1 / 1 / PSE PLL_PTP = 200MHz 19th bit and 16th bit are used for selecting Precision Time Protocol (PTP). This bits programming are used in GbE Time Synchronization CTS Test. - 19th Bit: MAC_GPIO[3] - 16th Bit: MAC_GPIO[0]
15:4	0h RO	**Reserved**
3:0	0h RW	**GPIS:** General Purpose Input Status. This field gives the status of the signals connected to the gpi_i port. This field is of the following types based on the setting of the corresponding GPIT field of MAC_GPIO_Control register: - Latched-Low (LL): This field is cleared when the corresponding gpi_i input becomes low. This field remains low until the application reads this field after which this field reflects the current value of gpi_i input. - Latched-High (LH): This field is set when the corresponding gpi_i input becomes high. This field remains high until the application reads this field after which this field reflects the current value of gpi_i input. The number of bits available in this field depends on the GP Input Signal Width option. Other bits are not used (reserved and always reset). 0000H

14.20.1.52 MAC_ARP_ADDRESS — Offset 50200210h

The ARP Address register contains the IPv4 Destination Address of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50200210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ARP Protocol Address (ARPPA):** This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

14.20.1.53 MAC_CSR_SW_CTRL — Offset 50200230h

This register contains SW programmable controls for changing the CSR access response and status bits clearing.

Type	Size	Offset	Default
MMIO	32 bit	50200230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Slave Error Response Enable (SEEN):** When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space. 0x0 (DISABLE): Slave Error Response is disabled. 0x1 (ENABLE): Slave Error Response is enabled.
7:1	0h RO	**Reserved**
0	0h RW	**Register Clear on Write 1 Enable (RCWE):** When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. 0x0 (DISABLE): Register Clear on Write 1 is disabled. 0x1 (ENABLE): Register Clear on Write 1 is enabled.

14.20.1.54 MAC_FPE_CTRL_STS — Offset 50200234h

This register controls the operation of Frame Preemption.

Type	Size	Offset	Default
MMIO	32 bit	50200234h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Transmitted Respond Frame (TRSP):** Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Respond Frame. 0x1 (ACTIVE): transmitted Respond Frame.
18	0h RW	**Transmitted Verify Frame (TVER):** Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Verify Frame. 0x1 (ACTIVE): transmitted Verify Frame.
17	0h RW	**Received Respond Frame (RRSP):** Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Respond Frame. 0x1 (ACTIVE): Received Respond Frame.
16	0h RW	**Received Verify Frame (RVER):** Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Verify Frame. 0x1 (ACTIVE): Received Verify Frame.
15:4	0h RO	**Reserved**
3	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Send Respond mPacket (SRSP):** When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Respond mPacket is disabled. 0x1 (ENABLE): Send Respond mPacket is enabled.
1	0h RW	**Send Verify mPacket (SVER):** When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Verify mPacket is disabled. 0x1 (ENABLE): Send Verify mPacket is enabled.
0	0h RW	**Enable Tx Frame Preemption (EFPE):** When set Frame Preemption Tx functionality is enabled. 0x0 (DISABLE): Tx Frame Preemption is disabled. 0x1 (ENABLE): Tx Frame Preemption is enabled.

14.20.1.55 MAC_EXT_CFG1 — Offset 50200238h

This register contains Split mode control field and offset field for Split Header feature.

Type	Size	Offset	Default
MMIO	32 bit	50200238h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h RW	**Split Mode (SPLM):** These bits indicate the mode of splitting the incoming Rx packets. They are 0x0 (L3L4): Split at L3/L4 header. 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame. 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped. 0x3 (RSVD): Reserved.
7	0h RO	**Reserved**
6:0	02h RW	**Split Offset (SPLOFST):** These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

14.20.1.56 MAC_PRESN_TIME_NS — Offset 50200240h

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns. Exists when DWC_EQOS_FLEXI_PPS_OUT_EN is configured.

Type	Size	Offset	Default
MMIO	32 bit	50200240h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MAC 1722 Presentation Time in ns (MPTN):** These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns

14.20.1.57 MAC_PRESN_TIME_UPDT — Offset 50200244h

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). Exists when DWC_EQOS_FLEXI_PPS_OUT_EN is configured.

Type	Size	Offset	Default
MMIO	32 bit	50200244h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC 1722 Presentation Time Update (MPTU):** This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction

14.20.1.58 MAC_ADDRESS0_HIGH — Offset 50200300h

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if

0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] of the MAC Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50200300h	8000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Address Enable (AE):** This bit is always set to 1. 0x0 (DISABLE): INVALID : This bit must be always set to 1. 0x1 (ENABLE): This bit is always set to 1.
30:24	0h RO	**Reserved**
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	FFFFh RW	**MAC Address0[47:32] (ADDRHI):** This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

14.20.1.59 MAC_ADDRESS0_LOW — Offset 50200304h

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	50200304h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address0[31:0] (ADDRLO):** This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

14.20.1.60 MAC_ADDRESS1_HIGH — Offset 50200308h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50200308h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

14.20.1.61 MAC_ADDRESS1_LOW — Offset 5020030Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	5020030Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

14.20.1.62 MAC_ADDRESS2_HIGH — Offset 50200310h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.63 MAC_ADDRESS2_LOW — Offset 50200314h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.64 MAC_ADDRESS3_HIGH — Offset 50200318h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.65 MAC_ADDRESS3_LOW — Offset 5020031Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.66 MAC_ADDRESS4_HIGH — Offset 50200320h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.67 MAC_ADDRESS4_LOW — Offset 50200324h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.68 MAC_ADDRESS5_HIGH — Offset 50200328h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.69 MAC_ADDRESS5_LOW — Offset 5020032Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.70 MAC_ADDRESS6_HIGH — Offset 50200330h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.71 MAC_ADDRESS6_LOW — Offset 50200334h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.72 MAC_ADDRESS7_HIGH — Offset 50200338h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.73 MAC_ADDRESS7_LOW — Offset 5020033Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.74 MAC_ADDRESS8_HIGH — Offset 50200340h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.75 MAC_ADDRESS8_LOW — Offset 50200344h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.76 MAC_ADDRESS9_HIGH — Offset 50200348h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.77 MAC_ADDRESS9_LOW — Offset 5020034Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.78 MAC_ADDRESS10_HIGH — Offset 50200350h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.79 MAC_ADDRESS10_LOW — Offset 50200354h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.80 MAC_ADDRESS11_HIGH — Offset 50200358h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.81 MAC_ADDRESS11_LOW — Offset 5020035Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.82 MAC_ADDRESS12_HIGH — Offset 50200360h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.83 MAC_ADDRESS12_LOW — Offset 50200364h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.84 MAC_ADDRESS13_HIGH — Offset 50200368h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.85 MAC_ADDRESS13_LOW — Offset 5020036Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.86 MAC_ADDRESS14_HIGH — Offset 50200370h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.87 MAC_ADDRESS14_LOW — Offset 50200374h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.88 MAC_ADDRESS15_HIGH — Offset 50200378h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.89 MAC_ADDRESS15_LOW — Offset 5020037Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.90 MAC_ADDRESS16_HIGH — Offset 50200380h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.91 MAC_ADDRESS16_LOW — Offset 50200384h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.92 MAC_ADDRESS17_HIGH — Offset 50200388h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.93 MAC_ADDRESS17_LOW — Offset 5020038Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.94 MAC_ADDRESS18_HIGH — Offset 50200390h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.95 MAC_ADDRESS18_LOW — Offset 50200394h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.96 MAC_ADDRESS19_HIGH — Offset 50200398h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.97 MAC_ADDRESS19_LOW — Offset 5020039Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.98 MAC_ADDRESS20_HIGH — Offset 502003A0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.99 MAC_ADDRESS20_LOW — Offset 502003A4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.100 MAC_ADDRESS21_HIGH — Offset 502003A8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.101 MAC_ADDRESS21_LOW — Offset 502003ACh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.102MAC_ADDRESS22_HIGH — Offset 502003B0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.103MAC_ADDRESS22_LOW — Offset 502003B4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.104MAC_ADDRESS23_HIGH — Offset 502003B8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.105MAC_ADDRESS23_LOW — Offset 502003BCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.106MAC_ADDRESS24_HIGH — Offset 502003C0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.107MAC_ADDRESS24_LOW — Offset 502003C4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.108MAC_ADDRESS25_HIGH — Offset 502003C8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.109MAC_ADDRESS25_LOW — Offset 502003CCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.110MAC_ADDRESS26_HIGH — Offset 502003D0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.111MAC_ADDRESS26_LOW — Offset 502003D4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.112MAC_ADDRESS27_HIGH — Offset 502003D8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.113MAC_ADDRESS27_LOW — Offset 502003DCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.114MAC_ADDRESS28_HIGH — Offset 502003E0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.115MAC_ADDRESS28_LOW — Offset 502003E4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.116MAC_ADDRESS29_HIGH — Offset 502003E8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.117MAC_ADDRESS29_LOW — Offset 502003ECh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.118MAC_ADDRESS30_HIGH — Offset 502003F0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.119MAC_ADDRESS30_LOW — Offset 502003F4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.120MAC_ADDRESS31_HIGH — Offset 502003F8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50200308h.

14.20.1.121MAC_ADDRESS31_LOW — Offset 502003FCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5020030Ch.

14.20.1.122MAC_ADDRESS32_HIGH — Offset 50200400h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	50200400h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

14.20.1.123MAC_ADDRESS32_LOW — Offset 50200404h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	50200404h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

14.20.1.124MAC_ADDRESS33_HIGH — Offset 50200408h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.125MAC_ADDRESS33_LOW — Offset 5020040Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.126MAC_ADDRESS34_HIGH — Offset 50200410h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.127MAC_ADDRESS34_LOW — Offset 50200414h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.128MAC_ADDRESS35_HIGH — Offset 50200418h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.129MAC_ADDRESS35_LOW — Offset 5020041Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.130MAC_ADDRESS36_HIGH — Offset 50200420h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.131MAC_ADDRESS36_LOW — Offset 50200424h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.132MAC_ADDRESS37_HIGH — Offset 50200428h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.133MAC_ADDRESS37_LOW — Offset 5020042Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.134MAC_ADDRESS38_HIGH — Offset 50200430h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.135MAC_ADDRESS38_LOW — Offset 50200434h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.136MAC_ADDRESS39_HIGH — Offset 50200438h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.137MAC_ADDRESS39_LOW — Offset 5020043Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.138MAC_ADDRESS40_HIGH — Offset 50200440h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.139MAC_ADDRESS40_LOW — Offset 50200444h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.140MAC_ADDRESS41_HIGH — Offset 50200448h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.141MAC_ADDRESS41_LOW — Offset 5020044Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.142MAC_ADDRESS42_HIGH — Offset 50200450h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.143MAC_ADDRESS42_LOW — Offset 50200454h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.144MAC_ADDRESS43_HIGH — Offset 50200458h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.145MAC_ADDRESS43_LOW — Offset 5020045Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.146MAC_ADDRESS44_HIGH — Offset 50200460h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.147MAC_ADDRESS44_LOW — Offset 50200464h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.148MAC_ADDRESS45_HIGH — Offset 50200468h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.149MAC_ADDRESS45_LOW — Offset 5020046Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.150MAC_ADDRESS46_HIGH — Offset 50200470h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.151MAC_ADDRESS46_LOW — Offset 50200474h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.152MAC_ADDRESS47_HIGH — Offset 50200478h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.153MAC_ADDRESS47_LOW — Offset 5020047Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.154MAC_ADDRESS48_HIGH — Offset 50200480h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.155MAC_ADDRESS48_LOW — Offset 50200484h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.156MAC_ADDRESS49_HIGH — Offset 50200488h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.157MAC_ADDRESS49_LOW — Offset 5020048Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.158MAC_ADDRESS50_HIGH — Offset 50200490h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.159MAC_ADDRESS50_LOW — Offset 50200494h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.160MAC_ADDRESS51_HIGH — Offset 50200498h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.161MAC_ADDRESS51_LOW — Offset 5020049Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.162MAC_ADDRESS52_HIGH — Offset 502004A0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.163MAC_ADDRESS52_LOW — Offset 502004A4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.164MAC_ADDRESS53_HIGH — Offset 502004A8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.165MAC_ADDRESS53_LOW — Offset 502004ACh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.166MAC_ADDRESS54_HIGH — Offset 502004B0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.167MAC_ADDRESS54_LOW — Offset 502004B4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.168MAC_ADDRESS55_HIGH — Offset 502004B8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.169MAC_ADDRESS55_LOW — Offset 502004BCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.170MAC_ADDRESS56_HIGH — Offset 502004C0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.171MAC_ADDRESS56_LOW — Offset 502004C4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.172MAC_ADDRESS57_HIGH — Offset 502004C8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.173MAC_ADDRESS57_LOW — Offset 502004CCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.174MAC_ADDRESS58_HIGH — Offset 502004D0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.175MAC_ADDRESS58_LOW — Offset 502004D4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.176MAC_ADDRESS59_HIGH — Offset 502004D8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.177MAC_ADDRESS59_LOW — Offset 502004DCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.178MAC_ADDRESS60_HIGH — Offset 502004E0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.179MAC_ADDRESS60_LOW — Offset 502004E4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.180MAC_ADDRESS61_HIGH — Offset 502004E8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.181MAC_ADDRESS61_LOW — Offset 502004ECh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.182MAC_ADDRESS62_HIGH — Offset 502004F0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.183MAC_ADDRESS62_LOW — Offset 502004F4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.184MAC_ADDRESS63_HIGH — Offset 502004F8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50200400h.

14.20.1.185MAC_ADDRESS63_LOW — Offset 502004FCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50200404h.

14.20.1.186MMC_CONTROL — Offset 50200700h

This register establishes the operating mode of MAC Management Counters.

Type	Size	Offset	Default
MMIO	32 bit	50200700h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Update MMC Counters for Dropped Broadcast Packets (UCDBC):** Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. 0x0 (DISABLE): Update MMC Counters for Dropped Broadcast Packets is disabled. 0x1 (ENABLE): Update MMC Counters for Dropped Broadcast Packets is enabled.
7:6	0h RO	**Reserved**
5	0h RW	**Full-Half Preset (CNTPRSTLVL):** When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. 0x0 (DISABLE): Full-Half Preset is disabled. 0x1 (ENABLE): Full-Half Preset is enabled.
4	0h RW	**Counters Preset (CNTPRST):** When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
3	0h RW	**MMC Counter Freeze (CNTFREEZ):** When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. 0x0 (DISABLE): MMC Counter Freeze is disabled. 0x1 (ENABLE): MMC Counter Freeze is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Reset on Read (RSTONRD):** When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. 0x0 (DISABLE): Reset on Read is disabled. 0x1 (ENABLE): Reset on Read is enabled.
1	0h RW	**Counter Stop Rollover (CNTSTOPRO):** When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0x0 (DISABLE): Counter Stop Rollover is disabled. 0x1 (ENABLE): Counter Stop Rollover is enabled.
0	0h RW	**Counters Reset (CNTRST):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.

14.20.1.187MMC_RX_INTERRUPT — Offset 50200704h

This register maintains the interrupts generated from all Receive statistics counters. The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur:

- Receive statistic counters reach half of their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter).

- Receive statistic counters cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter).

When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit. Note: R_SS_RC means that this register bit is set internally, and it is cleared when the Counter register is read.

Type	Size	Offset	Default
MMIO	32 bit	50200704h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Receive LPI transition counter interrupt status (RXLPITRCIS):** This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Receive LPI microsecond counter interrupt status (RXLPIUSCIS):** This bit is set when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Receive Control Packet Counter Interrupt Status (RXCTRLPIS):** This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Control Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Control Packet Counter Interrupt Status detected.
24	0h RO	**MMC Receive Error Packet Counter Interrupt Status (RXRCVERRPIS):** This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Error Packet Counter Interrupt Status detected.
23	0h RO	**MMC Receive Watchdog Error Packet Counter Interrupt Status (RXWDOGPIS):** This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected.
22	0h RO	**MMC Receive VLAN Good Bad Packet Counter Interrupt Status (RXVLANGBPIS):** This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**MMC Receive FIFO Overflow Packet Counter Interrupt Status (RXFOVPIS):** This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status detected.
20	0h RO	**MMC Receive Pause Packet Counter Interrupt Status (RXPAUSPIS):** This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected.
19	0h RO	**MMC Receive Out Of Range Error Packet Counter Interrupt Status. (RXORANGEPIS):** This bit is set when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Receive Length Error Packet Counter Interrupt Status (RXLENERPIS):** This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Length Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Length Error Packet Counter Interrupt Status detected.
17	0h RO	**MMC Receive Unicast Good Packet Counter Interrupt Status (RXUCGPIS):** This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status detected.
16	0h RO	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (RX1024TMAXOCTGBPIS):** This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
15	0h RO	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (RX512T1023OCTGBPIS):** This bit is set when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status (RX256T511OCTGBPIS):** This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
13	0h RO	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status (RX128T255OCTGBPIS):** This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status (RX65T127OCTGBPIS):** This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status (RX64OCTGBPIS):** This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive Oversize Good Packet Counter Interrupt Status (RXOSIZEGPIS):** This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive Undersize Good Packet Counter Interrupt Status (RXUSIZEGPIS):** This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MMC Receive Jabber Error Packet Counter Interrupt Status (RXJABERPIS):** This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status detected.
7	0h RO	**MMC Receive Runt Packet Counter Interrupt Status (RXRUNTPIS):** This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Runt Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Runt Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive Alignment Error Packet Counter Interrupt Status (RXALGNERPIS):** This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive CRC Error Packet Counter Interrupt Status (RXCRCERPIS):** This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive Multicast Good Packet Counter Interrupt Status (RXMCGPIS):** This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive Broadcast Good Packet Counter Interrupt Status (RXBCGPIS):** This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive Good Octet Counter Interrupt Status (RXGOCTIS):** This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Octet Counter Interrupt Status detected.
1	0h RO	**MMC Receive Good Bad Octet Counter Interrupt Status (RXGBOCTIS):** This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status detected.
0	0h RO	**MMC Receive Good Bad Packet Counter Interrupt Status (RXGBPKTIS):** This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status detected.

14.20.1.188MMC_TX_INTERRUPT — Offset 50200708h

This register maintains the interrupts generated from all Transmit statistics counters. The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	50200708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Transmit LPI transition counter interrupt status (TXLPITRCIS):** This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Transmit LPI microsecond counter interrupt status (TXLPIUSCIS):** This bit is set when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Transmit Oversize Good Packet Counter Interrupt Status (TXOSIZEGPIS):** This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status detected.
24	0h RO	**MMC Transmit VLAN Good Packet Counter Interrupt Status (TXVLANGPIS):** This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status detected.
23	0h RO	**MMC Transmit Pause Packet Counter Interrupt Status (TXPAUSPIS):** This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**MMC Transmit Excessive Deferral Packet Counter Interrupt Status (TXEXDEFPIS):** This bit is set when the txexcessdef counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status detected.
21	0h RO	**MMC Transmit Good Packet Counter Interrupt Status (TXGPKTIS):** This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Packet Counter Interrupt Status detected.
20	0h RO	**MMC Transmit Good Octet Counter Interrupt Status (TXGOCTIS):** This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Octet Counter Interrupt Status detected.
19	0h RO	**MMC Transmit Carrier Error Packet Counter Interrupt Status (TXCARERPIS):** This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Transmit Excessive Collision Packet Counter Interrupt Status (TXEXCOLPIS):** This bit is set when the txexesscol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status detected.
17	0h RO	**MMC Transmit Late Collision Packet Counter Interrupt Status (TXLATCOLPIS):** This bit is set when the txlatecol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status detected.
16	0h RO	**MMC Transmit Deferred Packet Counter Interrupt Status (TXDEFPIS):** This bit is set when the txdeferred counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Status (TXMCOLGPIS):** This bit is set when the txmulticol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status detected.
14	0h RO	**MMC Transmit Single Collision Good Packet Counter Interrupt Status (TXSCOLGPIS):** This bit is set when the txsinglecol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status detected.
13	0h RO	**MMC Transmit Underflow Error Packet Counter Interrupt Status (TXUFLOWERPIS):** This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status (TXBCGBPIS):** This bit is set when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Status (TXMCGBPIS):** The bit is set when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Status (TXUCGBPIS):** This bit is set when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (TX1024TMAXOCTGBPIS):** This bit is set when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
8	0h RO	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (TX512T1023OCTGBPIS):** This bit is set when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.
7	0h RO	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status (TX256T511OCTGBPIS):** This bit is set when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
6	0h RO	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status (TX128T255OCTGBPIS):** This bit is set when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
5	0h RO	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status (TX65T127OCTGBPIS):** This bit is set when the tx65to127octets_gb counter reaches half the maximum value, and also when it reaches the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
4	0h RO	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status (TX64OCTGBPIS):** This bit is set when the tx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**MMC Transmit Multicast Good Packet Counter Interrupt Status (TXMCGPIS):** This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status detected.
2	0h RO	**MMC Transmit Broadcast Good Packet Counter Interrupt Status (TXBCGPIS):** This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status detected.
1	0h RO	**MMC Transmit Good Bad Packet Counter Interrupt Status (TXGBPKTIS):** This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status detected.
0	0h RO	**MMC Transmit Good Bad Octet Counter Interrupt Status (TXGBOCTIS):** This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status detected.

14.20.1.189MMC_RX_INTERRUPT_MASK — Offset 5020070Ch

This register maintains the masks for interrupts generated from all Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	5020070Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Receive LPI transition counter interrupt Mask (RXLPITRCIM):** Setting this bit masks the interrupt when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Receive LPI microsecond counter interrupt Mask (RXLPIUSCIM):** Setting this bit masks the interrupt when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI microsecond counter interrupt Mask is enabled.
25	0h RW	**MMC Receive Control Packet Counter Interrupt Mask (RXCTRLPIM):** Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Control Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Control Packet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive Error Packet Counter Interrupt Mask (RXRCVERRPIM):** Setting this bit masks the interrupt when the rxrcverror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Error Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Receive Watchdog Error Packet Counter Interrupt Mask (RXWDOGPIM):** Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Receive VLAN Good Bad Packet Counter Interrupt Mask (RXVLANGBPIM):** Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive FIFO Overflow Packet Counter Interrupt Mask (RXFOVPIM):** Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**MMC Receive Pause Packet Counter Interrupt Mask (RXPAUSPIM):** Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive Out Of Range Error Packet Counter Interrupt Mask (RXORANGEPIM):** Setting this bit masks the interrupt when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive Length Error Packet Counter Interrupt Mask (RXLENERPIM):** Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Length Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Length Error Packet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Receive Unicast Good Packet Counter Interrupt Mask (RXUCGPIM):** Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask. (RX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
15	0h RW	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (RX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (RX256T511OCTGBPIM):** Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (RX128T255OCTGBPIM):** Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (RX65T127OCTGBPIM):** Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask (RX64OCTGBPIM):** Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Receive Oversize Good Packet Counter Interrupt Mask (RXOSIZEGPIM):** Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive Undersize Good Packet Counter Interrupt Mask (RXUSIZEGPIM):** Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive Jabber Error Packet Counter Interrupt Mask (RXJABERPIM):** Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive Runt Packet Counter Interrupt Mask (RXRUNTPIM):** Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Runt Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Runt Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive Alignment Error Packet Counter Interrupt Mask (RXALGNERPIM):** Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive CRC Error Packet Counter Interrupt Mask (RXCRCERPIM):** Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**MMC Receive Multicast Good Packet Counter Interrupt Mask (RXMCGPIM):** Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Receive Broadcast Good Packet Counter Interrupt Mask (RXBCGPIM):** Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Receive Good Octet Counter Interrupt Mask (RXGOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Octet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive Good Bad Octet Counter Interrupt Mask (RXGBOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive Good Bad Packet Counter Interrupt Mask (RXGBPKTIM):** Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is enabled.

14.20.1.190MMC_TX_INTERRUPT_MASK — Offset 50200710h

This register maintains the masks for interrupts generated from all Transmit statistics counters. The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	50200710h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Transmit LPI transition counter interrupt Mask (TXLPITRCIM):** Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Transmit LPI microsecond counter interrupt Mask (TXLPIUSCIM):** Setting this bit masks the interrupt when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI microsecond counter interrupt Mask is enabled.
25	0h RW	**MMC Transmit Oversize Good Packet Counter Interrupt Mask (TXOSIZEGPIM):** Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Transmit VLAN Good Packet Counter Interrupt Mask (TXVLANGPIM):** Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Transmit Pause Packet Counter Interrupt Mask (TXPAUSPIM):** Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Transmit Excessive Deferral Packet Counter Interrupt Mask (TXEXDEFPIM):** Setting this bit masks the interrupt when the txexcessdef counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Transmit Good Packet Counter Interrupt Mask (TXGPKTIM):** Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**MMC Transmit Good Octet Counter Interrupt Mask (TXGOCTIM):** Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Transmit Carrier Error Packet Counter Interrupt Mask (TXCARERPIM):** Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Transmit Excessive Collision Packet Counter Interrupt Mask (TXEXCOLPIM):** Setting this bit masks the interrupt when the txexcesscol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Transmit Late Collision Packet Counter Interrupt Mask (TXLATCOLPIM):** Setting this bit masks the interrupt when the txlatecol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Transmit Deferred Packet Counter Interrupt Mask (TXDEFPIM):** Setting this bit masks the interrupt when the txdeferred counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is enabled.
15	0h RW	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask (TXMCOLGPIM):** Setting this bit masks the interrupt when the txmulticol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Transmit Single Collision Good Packet Counter Interrupt Mask (TXSCOLGPIM):** Setting this bit masks the interrupt when the txsinglecol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Transmit Underflow Error Packet Counter Interrupt Mask (TXUFLOWERPIM):** Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask (TXBCGBPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask (TXMCGBPIM):** Setting this bit masks the interrupt when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask (TXUCGBPIM):** Setting this bit masks the interrupt when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask (TX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (TX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (TX256T511OCTGBPIM):** Setting this bit masks the interrupt when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (TX128T255OCTGBPIM):** Setting this bit masks the interrupt when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (TX65T127OCTGBPIM):** Setting this bit masks the interrupt when the tx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask (TX64OCTGBPIM):** Setting this bit masks the interrupt when the tx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Transmit Multicast Good Packet Counter Interrupt Mask (TXMCGPIM):** Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Transmit Broadcast Good Packet Counter Interrupt Mask (TXBCGPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Transmit Good Bad Packet Counter Interrupt Mask (TXGBPKTIM):** Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Good Bad Octet Counter Interrupt Mask (TXGBOCTIM):** Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled.

14.20.1.191TX_OCTET_COUNT_GOOD_BAD — Offset 50200714h

This register provides the number of bytes transmitted by the GbE Controller, exclusive of preamble and retried bytes, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	50200714h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good Bad (TXOCTGB):** This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

14.20.1.192TX_PACKET_COUNT_GOOD_BAD — Offset 50200718h

This register provides the number of good and bad packets transmitted by GbE Controller, exclusive of retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50200718h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good Bad (TXPKTGB):** This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

14.20.1.193TX_BROADCAST_PACKETS_GOOD — Offset 5020071Ch

This register provides the number of good broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	5020071Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good (TXBCASTG):** This field indicates the number of good broadcast packets transmitted.

14.20.1.194TX_MULTICAST_PACKETS_GOOD — Offset 50200720h

This register provides the number of good multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200720h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good (TXMCASTG):** This field indicates the number of good multicast packets transmitted.

14.20.1.195TX_64OCTETS_PACKETS_GOOD_BAD — Offset 50200724h

This register provides the number of good and bad packets transmitted by GbE Controller with length 64 bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50200724h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 64Octets Packets Good_Bad (TX64OCTGB):** This field indicates the number of good and bad packets transmitted with length 64 bytes, exclusive of preamble and retried packets.

14.20.1.196TX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 50200728h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50200728h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TX65_127OCTGB:** Tx 65To127Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.1.197TX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 5020072Ch

This register provides the number of good and bad packets transmitted by GbE Controller with length between 128 to 255 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	5020072Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 128To255Octets Packets Good Bad (TX128_255OCTGB):** This field indicates the number of good and bad packets transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.1.198TX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 50200730h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 256 to 511 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50200730h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 256To511Octets Packets Good Bad (TX256_511OCTGB):** This field indicates the number of good and bad packets transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.1.199TX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 50200734h

This register provides the number of good and bad packets transmitted by GbE Controller with length 512 to 1023 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50200734h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 512To1023Octets Packets Good Bad (TX512_1023OCTGB):** This field indicates the number of good and bad packets transmitted with length between 512 and 1023 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.1.200TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 50200738h

This register provides the number of good and bad packets transmitted by GbE Controller with length 1024 to maxsize (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50200738h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 1024ToMaxOctets Packets Good Bad (TX1024_MAXOCTGB):** This field indicates the number of good and bad packets transmitted with length between 1024 and maxsize (inclusive) bytes, exclusive of preamble and retried packets.

14.20.1.201TX_UNICAST_PACKETS_GOOD_BAD — Offset 5020073Ch

This register provides the number of good and bad unicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	5020073Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Unicast Packets Good Bad (TXUCASTGB):** This field indicates the number of good and bad unicast packets transmitted.

14.20.1.202TX_MULTICAST_PACKETS_GOOD_BAD — Offset 50200740h

This register provides the number of good and bad multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200740h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good Bad (TXMCASTGB):** This field indicates the number of good and bad multicast packets transmitted.

14.20.1.203TX_BROADCAST_PACKETS_GOOD_BAD — Offset 50200744h

This register provides the number of good and bad broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200744h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good Bad (TXBCASTGB):** This field indicates the number of good and bad broadcast packets transmitted.

14.20.1.204TX_UNDERFLOW_ERROR_PACKETS — Offset 50200748h

This register provides the number of packets aborted by GbE Controller because of packets underflow error.

Type	Size	Offset	Default
MMIO	32 bit	50200748h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Underflow Error Packets (TXUNDRFLW):** This field indicates the number of packets aborted because of packets underflow error.

14.20.1.205TX_SINGLE_COLLISION_GOOD_PACKETS — Offset 5020074Ch

This register provides the number of successfully transmitted packets by GbE Controller after a single collision in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	5020074Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Single Collision Good Packets (TXSNGLCOLG):** This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

14.20.1.206TX_MULTIPLE_COLLISION_GOOD_PACKETS — Offset 50200750h

This register provides the number of successfully transmitted packets by GbE Controller after multiple collisions in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	50200750h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multiple Collision Good Packets (TXMULTCOLG):** This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

14.20.1.207TX_DEFERRED_PACKETS — Offset 50200754h

This register provides the number of successfully transmitted by GbE Controller after a deferral in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	50200754h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Deferred Packets (TXDEFRD):** This field indicates the number of successfully transmitted after a deferral in the half-duplex mode.

14.20.1.208TX_LATE_COLLISION_PACKETS — Offset 50200758h

This register provides the number of packets aborted by GbE Controller because of late collision error.

Type	Size	Offset	Default
MMIO	32 bit	50200758h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Late Collision Packets (TXLATECOL):** This field indicates the number of packets aborted because of late collision error.

14.20.1.209TX_EXCESSIVE_COLLISION_PACKETS — Offset 5020075Ch

This register provides the number of packets aborted by GbE Controller because of excessive (16) collision errors.

Type	Size	Offset	Default
MMIO	32 bit	5020075Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Collision Packets (TXEXSCOL):** This field indicates the number of packets aborted because of excessive (16) collision errors.

14.20.1.210TX_CARRIER_ERROR_PACKETS — Offset 50200760h

This register provides the number of packets aborted by GbE Controller because of carrier sense error (no carrier or loss of carrier).

Type	Size	Offset	Default
MMIO	32 bit	50200760h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Carrier Error Packets (TXCARR):** This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

14.20.1.211TX_OCTET_COUNT_GOOD — Offset 50200764h

This register provides the number of bytes transmitted by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	50200764h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good (TXOCTG):** This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

14.20.1.212TX_PACKET_COUNT_GOOD — Offset 50200768h

This register provides the number of good packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200768h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good (TXPKTG):** This field indicates the number of good packets transmitted.

14.20.1.213TX_EXCESSIVE_DEFERRAL_ERROR — Offset 5020076Ch

This register provides the number of packets aborted by GbE Controller because of excessive deferral error (deferred for more than two max-sized packet times).

Type	Size	Offset	Default
MMIO	32 bit	5020076Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Deferral Error (TXEXSDEF):** This field indicates the number of packets aborted because of excessive deferral error (deferred for more than two max-sized packet times).

14.20.1.214TX_PAUSE_PACKETS — Offset 50200770h

This register provides the number of good Pause packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200770h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Pause Packets (TXPAUSE):** This field indicates the number of good Pause packets transmitted.

14.20.1.215TX_VLAN_PACKETS_GOOD — Offset 50200774h

This register provides the number of good VLAN packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200774h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx VLAN Packets Good (TXVLANG):** This field provides the number of good VLAN packets transmitted.

14.20.1.216TX_OSIZE_PACKETS_GOOD — Offset 50200778h

This register provides the number of packets transmitted by GbE Controller without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	50200778h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx OSize Packets Good (TXOSIZG):** This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

14.20.1.217RX_PACKETS_COUNT_GOOD_BAD — Offset 50200780h

This register provides the number of good and bad packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200780h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packets Count Good Bad (RXPKTGB):** This field indicates the number of good and bad packets received.

14.20.1.218RX_OCTET_COUNT_GOOD_BAD — Offset 50200784h

This register provides the number of bytes received by DWC_ther_qos, exclusive of preamble, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	50200784h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good Bad (RXOCTGB):** This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

14.20.1.219RX_OCTET_COUNT_GOOD — Offset 50200788h

This register provides the number of bytes received by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	50200788h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good (RXOCTG):** This field indicates the number of bytes received, exclusive of preamble, only in good packets.

14.20.1.220RX_BROADCAST_PACKETS_GOOD — Offset 5020078Ch

This register provides the number of good broadcast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	5020078Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Broadcast Packets Good (RXBCASTG):** This field indicates the number of good broadcast packets received.

14.20.1.221RX_MULTICAST_PACKETS_GOOD — Offset 50200790h

This register provides the number of good multicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50200790h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Multicast Packets Good (RXMCASTG):** This field indicates the number of good multicast packets received.

14.20.1.222RX_CRC_ERROR_PACKETS — Offset 50200794h

This register provides the number of packets received by GbE Controller with CRC error.

Type	Size	Offset	Default
MMIO	32 bit	50200794h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx CRC Error Packets (RXCRCERR):** This field indicates the number of packets received with CRC error.

14.20.1.223RX_ALIGNMENT_ERROR_PACKETS — Offset 50200798h

This register provides the number of packets received by GbE Controller with alignment (dribble) error. It is valid only in 10/100 mode.

Type	Size	Offset	Default
MMIO	32 bit	50200798h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Alignment Error Packets (RXALGNERR):** This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode.

14.20.1.224RX_RUNT_ERROR_PACKETS — Offset 5020079Ch

This register provides the number of packets received by GbE Controller with runt (length less than 64 bytes and CRC error) error.

Type	Size	Offset	Default
MMIO	32 bit	5020079Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Runt Error Packets (RXRUNTERR):** This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error.

14.20.1.225RX_JABBER_ERROR_PACKETS — Offset 502007A0h

This register provides the number of giant packets received by GbE Controller with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

Type	Size	Offset	Default
MMIO	32 bit	502007A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Jabber Error Packets (RXJABERR):** This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

14.20.1.226RX_UNDERSIZE_PACKETS_GOOD — Offset 502007A4h

This register provides the number of packets received by GbE Controller with length less than 64 bytes, without any errors.

Type	Size	Offset	Default
MMIO	32 bit	502007A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Undersize Packets Good (RXUNDERSZG):** This field indicates the number of packets received with length less than 64 bytes, without any errors.

14.20.1.227RX_OVERSIZE_PACKETS_GOOD — Offset 502007A8h

This register provides the number of packets received by GbE Controller without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	502007A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Oversize Packets Good (RXOVERSZG):** This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

14.20.1.228RX_64OCTETS_PACKETS_GOOD_BAD — Offset 502007ACh

This register provides the number of good and bad packets received by GbE Controller with length 64 bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502007ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 64 Octets Packets Good Bad (RX64OCTGB):** This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble.

14.20.1.229RX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 502007B0h

This register provides the number of good and bad packets received by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502007B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX128_255OCTGB:** Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

14.20.1.230RX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 502007B4h

This register provides the number of good and bad packets received by GbE Controller with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502007B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX128_255OCTGB:** Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

14.20.1.231RX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 502007B8h

This register provides the number of good and bad packets received by GbE Controller with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502007B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX256_511OCTGB:** Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

14.20.1.232RX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 502007BCh

This register provides the number of good and bad packets received by GbE Controller with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502007BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX 512-1023 Octets Packets Good Bad (RX512_1023OCTGB):** This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

14.20.1.233RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 502007C0h

This register provides the number of good and bad packets received by GbE Controller with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502007C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 1024-Max Octets Good Bad (RX1024_MAXOCTGB):** This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

14.20.1.234RX_UNICAST_PACKETS_GOOD — Offset 502007C4h

This register provides the number of good unicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Unicast Packets Good (RXUCASTG):** This field indicates the number of good unicast packets received.

14.20.1.235RX_LENGTH_ERROR_PACKETS — Offset 502007C8h

This register provides the number of packets received by GbE Controller with length error (Length Type field not equal to packet size), for all packets with valid length field.

Type	Size	Offset	Default
MMIO	32 bit	502007C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Length Error Packets (RXLENERR):** This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

14.20.1.236RX_OUT_OF_RANGE_TYPE_PACKETS — Offset 502007CCh

This register provides the number of packets received by GbE Controller with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

Type	Size	Offset	Default
MMIO	32 bit	502007CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Out of Range Type Packet (RXOUTOFRNG):** This field indicates the number of packets received with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

14.20.1.237RX_PAUSE_PACKETS — Offset 502007D0h

This register provides the number of good and valid Pause packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Pause Packets (RXPAUSEPKT):** This field indicates the number of good and valid Pause packets received.

14.20.1.238RX_FIFO_OVERFLOW_PACKETS — Offset 502007D4h

This register provides the number of missed received packets because of FIFO overflow in GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FIFO Overflow Packets (RXFIFOOVFL):** This field indicates the number of missed received packets because of FIFO overflow.

14.20.1.239RX_VLAN_PACKETS_GOOD_BAD — Offset 502007D8h

This register provides the number of good and bad VLAN packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx VLAN Packets Good Bad (RXVLANPKTGB):** This field indicates the number of good and bad VLAN packets received.

14.20.1.240RX_WATCHDOG_ERROR_PACKETS — Offset 502007DCh

This register provides the number of packets received by GbE Controller with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

Type	Size	Offset	Default
MMIO	32 bit	502007DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Watchdog Error Packets (RXWDGERR):** This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

14.20.1.241RX_RECEIVE_ERROR_PACKETS — Offset 502007E0h

This register provides the number of packets received by GbE Controller with Receive error or Packet Extension error on the GMII or MII interface.

Type	Size	Offset	Default
MMIO	32 bit	502007E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Receive Error Packets (RXRCVERR):** This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface.

14.20.1.242RX_CONTROL_PACKETS_GOOD — Offset 502007E4h

This register provides the number of good control packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Control Packets Good (RXCTRLG):** This field indicates the number of good control packets received.

14.20.1.243TX_LPI_USEC_CNTR — Offset 502007ECh

This register provides the number of microseconds Tx LPI is asserted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Microseconds Counter (TXLPIUSC):** This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

14.20.1.244TX_LPI_TRAN_CNTR — Offset 502007F0h

This register provides the number of times GbE Controller has entered Tx LPI.

Type	Size	Offset	Default
MMIO	32 bit	502007F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Transition counter (TXLPITRC):** This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments.

14.20.1.245RX_LPI_USEC_CNTR — Offset 502007F4h

This register provides the number of microseconds Rx LPI is sampled by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502007F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Microseconds Counter (RXLPIUSC):** This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

14.20.1.246RX_LPI_TRAN_CNTR — Offset 502007F8h

This register provides the number of times GbE Controller has entered Rx LPI.

Type	Size	Offset	Default
MMIO	32 bit	502007F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Transition counter (RXLPITRC):** This field indicates the number of times Rx LPI Entry has occurred.

14.20.1.247MMC_IPC_RX_INTERRUPT_MASK — Offset 50200800h

This register maintains the mask for the interrupt generated from the receive IPC statistic counters. The MMC Receive Checksum Off load Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Off load) statistic counters reach half their maximum value, and when they reach their maximum values. This register is 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	50200800h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**MMC Receive ICMP Error Octet Counter Interrupt Mask (RXICMPEROIM):** Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled.
28	0h RW	**MMC Receive ICMP Good Octet Counter Interrupt Mask (RXICMPGOIM):** Setting this bit masks the interrupt when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is enabled.
27	0h RW	**MMC Receive TCP Error Octet Counter Interrupt Mask (RXTCPEROIM):** Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is enabled.
26	0h RW	**MMC Receive TCP Good Octet Counter Interrupt Mask (RXTCPGOIM):** Setting this bit masks the interrupt when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is enabled.
25	0h RW	**MMC Receive UDP Good Octet Counter Interrupt Mask (RXUDPEROIM):** Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive IPV6 No Payload Octet Counter Interrupt Mask (RXUDPGOIM):** Setting this bit masks the interrupt when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Receive IPV6 Header Error Octet Counter Interrupt Mask (RXIPV6NOPAYOIM):** Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6HEROIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6GOIM):** Setting this bit masks the interrupt when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask (RXIPV4UDSBLOIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask (RXIPV4FRAGOIM):** Setting this bit masks the interrupt when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive IPV4 No Payload Octet Counter Interrupt Mask (RXIPV4NOPAYOIM):** Setting this bit masks the interrupt when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Receive IPV4 Header Error Octet Counter Interrupt Mask (RXIPV4HEROIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive IPV4 Good Octet Counter Interrupt Mask (RXIPV4GOIM):** Setting this bit masks the interrupt when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is enabled.
15:14	0h RO	**Reserved**
13	0h RW	**MMC Receive ICMP Error Packet Counter Interrupt Mask (RXICMPERPIM):** Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**MMC Receive ICMP Good Packet Counter Interrupt Mask (RXICMPGPIM):** Setting this bit masks the interrupt when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive TCP Error Packet Counter Interrupt Mask (RXTCPERPIM):** Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Receive TCP Good Packet Counter Interrupt Mask (RXTCPGPIM):** Setting this bit masks the interrupt when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive UDP Error Packet Counter Interrupt Mask (RXUDPERPIM):** Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive UDP Good Packet Counter Interrupt Mask (RXUDPGPIM):** Setting this bit masks the interrupt when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive IPV6 No Payload Packet Counter Interrupt Mask (RXIPV6NOPAYPIM):** Setting this bit masks the interrupt when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive IPV6 Header Error Packet Counter Interrupt Mask (RXIPV6HERPIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive IPV6 Good Packet Counter Interrupt Mask (RXIPV6GPIM):** Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask (RXIPV4UDSBLPIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask (RXIPV4FRAGPIM):** Setting this bit masks the interrupt when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Receive IPV4 No Payload Packet Counter Interrupt Mask (RXIPV4NOPAYPIM):** Setting this bit masks the interrupt when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive IPV4 Header Error Packet Counter Interrupt Mask (RXIPV4HERPIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive IPV4 Good Packet Counter Interrupt Mask (RXIPV4GPIM):** Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled.

14.20.1.248MMC_IPC_RX_INTERRUPT — Offset 50200808h

This register maintains the interrupt that the receive IPC statistic counters generate. The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits[7:0]) must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	50200808h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RO	**MMC Receive ICMP Error Octet Counter Interrupt Status (RXICMPEROIS):** This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status detected.
28	0h RO	**MMC Receive ICMP Good Octet Counter Interrupt Status (RXICMPGOIS):** This bit is set when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status detected.
27	0h RO	**MMC Receive TCP Error Octet Counter Interrupt Status (RXTCPEROIS):** This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status detected.
26	0h RO	**MMC Receive TCP Good Octet Counter Interrupt Status (RXTCPGOIS):** This bit is set when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status detected.
25	0h RO	**MMC Receive UDP Error Octet Counter Interrupt Status (RXUDPEROIS):** This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status detected.
24	0h RO	**MMC Receive UDP Good Octet Counter Interrupt Status (RXUDPGOIS):** This bit is set when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**MMC Receive IPV6 No Payload Octet Counter Interrupt Status (RXIPV6NOPAYOIS):** This bit is set when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status detected.
22	0h RO	**MMC Receive IPV6 Header Error Octet Counter Interrupt Status (RXIPV6HEROIS):** This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected.
21	0h RO	**MMC Receive IPV6 Good Octet Counter Interrupt Status (RXIPV6GOIS):** This bit is set when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status detected.
20	0h RO	**RXIPV4UDSBLOIS:** MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status This bit is set when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status detected.
19	0h RO	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Status (RXIPV4FRAGOIS):** This bit is set when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status detected.
18	0h RO	**MMC Receive IPV4 No Payload Octet Counter Interrupt Status (RXIPV4NOPAYOIS):** This bit is set when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**MMC Receive IPV4 Header Error Octet Counter Interrupt Status (RXIPV4HEROIS):** This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected.
16	0h RO	**MMC Receive IPV4 Good Octet Counter Interrupt Status (RXIPV4GOIS):** This bit is set when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status detected.
15:14	0h RO	**Reserved**
13	0h RO	**MMC Receive ICMP Error Packet Counter Interrupt Status (RXICMPERPIS):** This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive ICMP Good Packet Counter Interrupt Status (RXICMPGPIS):** This bit is set when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive TCP Error Packet Counter Interrupt Status (RXTCPERPIS):** This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive TCP Good Packet Counter Interrupt Status (RXTCPGPIS):** This bit is set when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive UDP Error Packet Counter Interrupt Status (RXUDPERPIS):** This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MC Receive UDP Good Packet Counter Interrupt Status (RXUDPGPIS):** This bit is set when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status detected.
7	0h RO	**MMC Receive IPV6 No Payload Packet Counter Interrupt Status (RXIPV6NOPAYPIS):** This bit is set when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive IPV6 Header Error Packet Counter Interrupt Status (RXIPV6HERPIS):** This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive IPV6 Good Packet Counter Interrupt Status (RXIPV6GPIS):** This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status (RXIPV4UDSBLPIS):** This bit is set when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Status (RXIPV4FRAGPIS):** This bit is set when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive IPV4 No Payload Packet Counter Interrupt Status (RXIPV4NOPAYPIS):** This bit is set when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status detected.
1	0h RO	**MMC Receive IPV4 Header Error Packet Counter Interrupt Status (RXIPV4HERPIS):** This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected.
0	0h RO	**MMC Receive IPV4 Good Packet Counter Interrupt Status (RXIPV4GPIS):** This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status detected.

14.20.1.249RXIPV4_GOOD_PACKETS — Offset 50200810h

This register provides the number of good IPv4 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50200810h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Packets (RXIPV4GDPKT):** This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

14.20.1.250RXIPV4_HEADER_ERROR_PACKETS — Offset 50200814h

RxIPv4 Header Error Packets This register provides the number of IPv4 datagrams received by GbE Controller with header (checksum, length, or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	50200814h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Packets (RXIPV4HDRERRPKT):** This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

14.20.1.251RXIPV4_NO_PAYLOAD_PACKETS — Offset 50200818h

This register provides the number of IPv4 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50200818h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Packets (RXIPV4NOPAYPKT):** This field indicates the number of IPv4 datagram packets received that did not have a TCP, UDP, or ICMP payload.

14.20.1.252RXIPV4_FRAGMENTED_PACKETS — Offset 5020081Ch

This register provides the number of good IPv4 datagrams received by GbE Controller with fragmentation.

Type	Size	Offset	Default
MMIO	32 bit	5020081Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Packets (RXIPV4FRAGPKT):** This field indicates the number of good IPv4 datagrams received with fragmentation.

14.20.1.253RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS — Offset 50200820h

This register provides the number of good IPv4 datagrams received by GbE Controller that had a UDP payload with checksum disabled.

Type	Size	Offset	Default
MMIO	32 bit	50200820h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disabled Packets (RXIPV4UDSBLPKT):** This field indicates the number of good IPv4 datagrams received that had a UDP payload with checksum disabled.

14.20.1.254RXIPV6_GOOD_PACKETS — Offset 50200824h

This register provides the number of good IPv6 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50200824h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Packets (RXIPV6GDPKT):** This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

14.20.1.255RXIPV6_HEADER_ERROR_PACKETS — Offset 50200828h

This register provides the number of IPv6 datagrams received by GbE Controller with header (length or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	50200828h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Packets (RXIPV6HDRERRPKT):** This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

14.20.1.256RXIPV6_NO_PAYLOAD_PACKETS — Offset 5020082Ch

This register provides the number of IPv6 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

Type	Size	Offset	Default
MMIO	32 bit	5020082Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Packets (RXIPV6NOPAYPKT):** This field indicates the number of IPv6 datagram packets received that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

14.20.1.257RXUDP_GOOD_PACKETS — Offset 50200830h

This register provides the number of good IP datagrams received by GbE Controller with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

Type	Size	Offset	Default
MMIO	32 bit	50200830h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Packets (RXUDPGDPKT):** This field indicates the number of good IP datagrams received with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

14.20.1.258RXUDP_ERROR_PACKETS — Offset 50200834h

This register provides the number of good IP datagrams received by GbE Controller whose UDP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	50200834h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Packets (RXUDPERRPKT):** This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

14.20.1.259RXTCP_GOOD_PACKETS — Offset 50200838h

This register provides the number of good IP datagrams received by GbE Controller with a good TCP payload.

Type	Size	Offset	Default
MMIO	32 bit	50200838h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Packets (RXTCPGDPKT):** This field indicates the number of good IP datagrams received with a good TCP payload.

14.20.1.260RXTCP_ERROR_PACKETS — Offset 5020083Ch

This register provides the number of good IP datagrams received by GbE Controller whose TCP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	5020083Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Packets (RXTCPERRPKT):** This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

14.20.1.261RXICMP_GOOD_PACKETS — Offset 50200840h

This register provides the number of good IP datagrams received by GbE Controller with a good ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50200840h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Packets (RXICMPGDPKT):** This field indicates the number of good IP datagrams received with a good ICMP payload.

14.20.1.262RXICMP_ERROR_PACKETS — Offset 50200844h

This register provides the number of good IP datagrams received by GbE Controller whose ICMP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	50200844h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Packets (RXICMPERRPKT):** This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

14.20.1.263RXIPV4_GOOD_OCTETS — Offset 50200850h

This register provides the number of bytes received by GbE Controller in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50200850h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Octets (RXIPV4GDOCT):** This field indicates the number of bytes received in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.264RXIPV4_HEADER_ERROR_OCTETS — Offset 50200854h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50200854h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Octets (RXIPV4HDRERROCT):** This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.265RXIPV4_NO_PAYLOAD_OCTETS — Offset 50200858h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50200858h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Octets (RXIPV4NOPAYOCT):** This field indicates the number of bytes received in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.266RXIPV4_FRAGMENTED_OCTETS — Offset 5020085Ch

This register provides the number of bytes received by GbE Controller in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	5020085Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Octets (RXIPV4FRAGOCT):** This field indicates the number of bytes received in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.267RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS — Offset 50200860h

This register provides the number of bytes received by GbE Controller in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50200860h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disable Octets (RXIPV4UDSBLOCT):** This field indicates the number of bytes received in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.268RXIPV6_GOOD_OCTETS — Offset 50200864h

This register provides the number of bytes received by GbE Controller in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50200864h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Octets (RXIPV6GDOCT):** This field indicates the number of bytes received in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.269RXIPV6_HEADER_ERROR_OCTETS — Offset 50200868h

This register provides the number of bytes received by GbE Controller in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50200868h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Octets (RXIPV6HDRERROCT):** This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.270RXIPV6_NO_PAYLOAD_OCTETS — Offset 5020086Ch

This register provides the number of bytes received by GbE Controller in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	5020086Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Octets (RXIPV6NOPAYOCT):** This field indicates the number of bytes received in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.1.271RXUDP_GOOD_OCTETS — Offset 50200870h

This register provides the number of bytes received by GbE Controller in a good UDP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50200870h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Octets (RXUDPGDOCT):** This field indicates the number of bytes received in a good UDP segment. This counter does not count IP header bytes.

14.20.1.272RXUDP_ERROR_OCTETS — Offset 50200874h

This register provides the number of bytes received by GbE Controller in a UDP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50200874h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Octets (RXUDPERROCT):** This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

14.20.1.273RXTCP_GOOD_OCTETS — Offset 50200878h

This register provides the number of bytes received by GbE Controller in a good TCP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50200878h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Octets (RXTCPGDOCT):** This field indicates the number of bytes received in a good TCP segment. This counter does not count IP header bytes.

14.20.1.274RXTCP_ERROR_OCTETS — Offset 5020087Ch

This register provides the number of bytes received by GbE Controller in a TCP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	5020087Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Octets (RXTCPERROCT):** This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

14.20.1.275RXICMP_GOOD_OCTETS — Offset 50200880h

This register provides the number of bytes received by GbE Controller in a good ICMP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50200880h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Octets (RXICMPGDOCT):** This field indicates the number of bytes received in a good ICMP segment. This counter does not count IP header bytes.

14.20.1.276RXICMP_ERROR_OCTETS — Offset 50200884h

This register provides the number of bytes received by GbE Controller in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50200884h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Octets (RXICMPERROCT):** This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

14.20.1.277MMC_FPE_TX_INTERRUPT — Offset 502008A0h

This register maintains the interrupts generated from all FPE related Transmit statistics counters. The MMC FPE Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	502008A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MMC Tx Hold Request Counter Interrupt Status (HRCIS):** This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected.
0	0h RO	**MMC Tx FPE Fragment Counter Interrupt status (FCIS):** This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected. 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected.

14.20.1.278MMC_FPE_TX_INTERRUPT_MASK — Offset 502008A4h

This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	502008A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**MMC Transmit Hold Request Counter Interrupt Mask (HRCIM):** Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled.

14.20.1.279MMC_TX_FPE_FRAGMENT_CNTR — Offset 502008A8h

This register provides the number of additional mPackets transmitted due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	502008A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx FPE Fragment counter (TXFFC):** This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.1.280MMC_TX_HOLD_REQ_CNTR — Offset 502008ACh

This register provides the count of number of times a hold request is given to MAC

Type	Size	Offset	Default
MMIO	32 bit	502008ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Hold Request Counter (TXHRC):** This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

14.20.1.281MMC_FPE_RX_INTERRUPT — Offset 502008C0h

This register maintains the interrupts generated from all FPE related Receive statistics counters. The MMC FPE Receive Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	502008C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**MMC Rx FPE Fragment Counter Interrupt Status (FCIS):** This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected.
2	0h RO	**MMC Rx Packet Assembly OK Counter Interrupt Status (PAOCIS):** This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected.
1	0h RO	**MMC Rx Packet SMD Error Counter Interrupt Status (PSECIS):** This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected.
0	0h RO	**MMC Rx Packet Assembly Error Counter Interrupt Status (PAECIS):** This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected.

14.20.1.282MMC_FPE_RX_INTERRUPT_MASK — Offset 502008C4h

This register maintains the masks for interrupts generated from all FPE related Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	502008C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**MMC Rx FPE Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled.
2	0h RW	**MMC Rx Packet Assembly OK Counter Interrupt Mask (PAOCIM):** Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled.
1	0h RW	**MMC Rx Packet SMD Error Counter Interrupt Mask (PSECIM):** Setting this bit masks the interrupt when the R Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled.
0	0h RW	**MMC Rx Packet Assembly Error Counter Interrupt Mask (PAECIM):** Setting this bit masks the interrupt when the R Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled.

14.20.1.283MMC_RX_PACKET_ASSEMBLY_ERR_CNTR — Offset 502008C8h

This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.

Type	Size	Offset	Default
MMIO	32 bit	502008C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly Error Counter (PAEC):** This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.1.284MMC_RX_PACKET_SMD_ERR_CNTR — Offset 502008CCh

This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.

Type	Size	Offset	Default
MMIO	32 bit	502008CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet SMD Error Counter (PSEC):** This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.1.285MMC_RX_PACKET_ASSEMBLY_OK_CNTR — Offset 502008D0h

This register provides the number of MAC frames that were successfully reassembled and delivered to MAC.

Type	Size	Offset	Default
MMIO	32 bit	502008D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly OK Counter (PAOC):** This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.1.286MMC_RX_FPE_FRAGMENT_CNTR — Offset 502008D4h

This register provides the number of additional mPackets received due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	502008D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FPE Fragment Counter (FFC):** This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.1.287MAC_L3_L4_CONTROL0 — Offset 50200900h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	50200900h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN0):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**
26:24	0h RW	**DMA Channel Number (DMCHN0):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM0):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM0):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Reserved**
16	0h RW	**Layer 4 Protocol Enable (L4PEN0):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	**L3HDBM0:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM0:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN0):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

14.20.1.288MAC_LAYER4_ADDRESS0 — Offset 50200904h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core. You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	50200904h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP0):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP0):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

14.20.1.289MAC_LAYER3_ADDR0_REG0 — Offset 50200910h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50200910h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A00):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

14.20.1.290MAC_LAYER3_ADDR1_REG0 — Offset 50200914h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50200914h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A10):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

14.20.1.291MAC_LAYER3_ADDR2_REG0 — Offset 50200918h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50200918h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A20):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.1.292MAC_LAYER3_ADDR3_REG0 — Offset 5020091Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	5020091Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A30):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.1.293MAC_L3_L4_CONTROL1 — Offset 50200930h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	50200930h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN1):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**DMA Channel Number (DMCHN1):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM1):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM1):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	**Reserved**
16	0h RW	**Layer 4 Protocol Enable (L4PEN1):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RW	**L3HDBM1:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM1:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN1):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

14.20.1.294MAC_LAYER4_ADDRESS1 — Offset 50200934h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core. You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	50200934h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP1):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP1):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

14.20.1.295MAC_LAYER3_ADDR0_REG1 — Offset 50200940h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50200940h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A01):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

14.20.1.296MAC_LAYER3_ADDR1_REG1 — Offset 50200944h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50200944h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A11):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

14.20.1.297MAC_LAYER3_ADDR2_REG1 — Offset 50200948h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50200948h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A21):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.1.298MAC_LAYER3_ADDR3_REG1 — Offset 5020094Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	5020094Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A31):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.1.299MAC_TIMESTAMP_CONTROL — Offset 50200B00h

This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver.

Type	Size	Offset	Default
MMIO	32 bit	50200B00h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**AV 802.1AS Mode Enable (AV8021ASMEN):** When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. 0x0 (DISABLE): AV 802.1AS Mode is disabled. 0x1 (ENABLE): AV 802.1AS Mode is enabled.
27:25	0h RO	**Reserved**
24	0h RW	**Transmit Timestamp Status Mode (TXTSSTSM):** When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. 0x0 (DISABLE): Transmit Timestamp Status Mode is disabled. 0x1 (ENABLE): Transmit Timestamp Status Mode is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**External System Time Input (ESTI):** When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: - To take the timestamp provided as status - To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time. 0x0 (DISABLE): External System Time Input is disabled. 0x1 (ENABLE): External System Time Input is enabled.
19	0h RW	**Enable checksum correction during OST for PTP over UDP/IPv4 packets (CSC):** When this bit is set, the last two bytes of PTP message sent over UDP/IPv4 is updated to keep the UDP checksum correct, for changes made to origin timestamp and/or correction field as part of one step timestamp operation. The application shall form the packet with these two dummy bytes. When reset, no updates are done to keep the UDP checksum correct. The application shall form the packet with UDP checksum set to 0. 0x0 (DISABLE): checksum correction during OST for PTP over UDP/IPv4 packets is disabled. 0x1 (ENABLE): checksum correction during OST for PTP over UDP/IPv4 packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Enable MAC Address for PTP Packet Filtering (TSENMACADDR):** When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. 0x0 (DISABLE): MAC Address for PTP Packet Filtering is disabled. 0x1 (ENABLE): MAC Address for PTP Packet Filtering is enabled.
17:16	0h RW	**Select PTP packets for Taking Snapshots (SNAPTYPSEL):** These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	0h RW	**Enable Snapshot for Messages Relevant to Master (TSMSTRENA):** When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. 0x0 (DISABLE): Snapshot for Messages Relevant to Master is disabled. 0x1 (ENABLE): Snapshot for Messages Relevant to Master is enabled.
14	0h RW	**Enable Timestamp Snapshot for Event Messages (TSEVNTENA):** When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. 0x0 (DISABLE): Timestamp Snapshot for Event Messages is disabled. 0x1 (ENABLE): Timestamp Snapshot for Event Messages is enabled.
13	1h RW	**Enable Processing of PTP Packets Sent over IPv4-UDP (TSIPV4ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv4-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv4-UDP is enabled.
12	0h RW	**Enable Processing of PTP Packets Sent over IPv6-UDP (TSIPV6ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv6-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv6-UDP is enabled.
11	0h RW	**Enable Processing of PTP over Ethernet Packets (TSIPENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. 0x0 (DISABLE): Processing of PTP over Ethernet Packets is disabled. 0x1 (ENABLE): Processing of PTP over Ethernet Packets is enabled.
10	0h RW	**Enable PTP Packet Processing for Version 2 Format (TSVER2ENA):** When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. 0x0 (DISABLE): PTP Packet Processing for Version 2 Format is disabled. 0x1 (ENABLE): PTP Packet Processing for Version 2 Format is enabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Timestamp Digital or Binary Rollover Control (TSCTRLSSR):** When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. 0x0 (DISABLE): Timestamp Digital or Binary Rollover Control is disabled. 0x1 (ENABLE): Timestamp Digital or Binary Rollover Control is enabled.
8	0h RW	**Enable Timestamp for All Packets (TSENALL):** When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. 0x0 (DISABLE): Timestamp for All Packets disabled. 0x1 (ENABLE): Timestamp for All Packets enabled.
7	0h RO	**Reserved**
6	0h RW	**Presentation Time Generation Enable (PTGE):** When this bit is set the Presentation Time generation is enabled. 0x0 (DISABLE): Presentation Time Generation is disabled. 0x1 (ENABLE): Presentation Time Generation is enabled.
5	0h RW	**Update Addend Register (TSADDREG):** When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Addend Register is not updated. 0x1 (ENABLE): Addend Register is updated.
4	0h RO	**Reserved**
3	0h RW	**Update Timestamp (TSUPDT):** When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not updated. 0x1 (ENABLE): Timestamp is updated.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Initialize Timestamp (TSINIT):** When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not initialized. 0x1 (ENABLE): Timestamp is initialized.
1	0h RW	**Fine or Coarse Timestamp Update (TSCFUPDT):** When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. 0x0 (COARSE): Coarse method is used to update system timestamp. 0x1 (FINE): Fine method is used to update system timestamp.
0	0h RW	**Enable Timestamp (TSENA):** When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. 0x0 (DISABLE): Timestamp is disabled. 0x1 (ENABLE): Timestamp is enabled.

14.20.1.300MAC_SUB_SECOND_INCREMENT — Offset 50200B04h

This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock.

Type	Size	Offset	Default
MMIO	32 bit	50200B04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**Sub-second Increment Value (SSINC):** The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:8	00h RW	**Sub-nanosecond Increment Value (SNSINC):** This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C.
7:0	0h RO	**Reserved**

14.20.1.301MAC_SYSTEM_TIME_SECONDS — Offset 50200B08h

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

Type	Size	Offset	Default
MMIO	32 bit	50200B08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Timestamp Second (TSS):** The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

14.20.1.302MAC_SYSTEM_TIME_NANOSECONDS — Offset 50200B0Ch

The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50200B0Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Timestamp Sub Seconds (TSSS):** The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

14.20.1.303MAC_SYSTEM_TIME_SECONDS_UPDATE — Offset 50200B10h

The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both registers before setting the TSINIT or TSUPDT bits in MAC_Timestamp_Control register.

Type	Size	Offset	Default
MMIO	32 bit	50200B10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Seconds (TSS):** The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

14.20.1.304MAC_SYSTEM_TIME_NANOSECONDS_UPDATE — Offset 50200B14h

MAC System Time Nanoseconds Update register.

Type	Size	Offset	Default
MMIO	32 bit	50200B14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Add or Subtract Time (ADDSUB):** When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. 0x0 (ADD): Add time. 0x1 (SUB): Subtract time.
30:0	00000000h RW	**Timestamp Sub Seconds (TSSS):** The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

14.20.1.305MAC_TIMESTAMP_ADDEND — Offset 50200B18h

Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register). The content of this register is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Type	Size	Offset	Default
MMIO	32 bit	50200B18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Addend Register (TSAR):** This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

14.20.1.306MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS — Offset 50200B1Ch

System Time - Higher Word Seconds register.

Type	Size	Offset	Default
MMIO	32 bit	50200B1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Timestamp Higher Word Register (TSHWR):** This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.

14.20.1.307MAC_TIMESTAMP_STATUS — Offset 50200B20h

Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register.

Type	Size	Offset	Default
MMIO	32 bit	50200B20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Number of Auxiliary Timestamp Snapshots (ATSNS):** This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	0h RO	**Auxiliary Timestamp Snapshot Trigger Missed (ATSSTM):** This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. 0x0 (INACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status detected.
23:20	0h RO	**Reserved**
19:16	0h RO	**Auxiliary Timestamp Snapshot Trigger Identifier (ATSSTN):** These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: - Bit 16: Auxiliary trigger 0 - Bit 17: Auxiliary trigger 1 - Bit 18: Auxiliary trigger 2 - Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15	0h RO	**Tx Timestamp Status Interrupt Status (TXTSSIS):** In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Tx Timestamp Status Interrupt status not detected. 0x1 (ACTIVE): Tx Timestamp Status Interrupt status detected.
14:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Timestamp Target Time Error (TSTRGTERR1):** This bit is set when the latest target time programmed in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.
4	0h RO	**Timestamp Target Time Reached for Target Time PPS1 (TSTARGT1):** When this bit is set and MCGREN1 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN1 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[1] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
3	0h RO	**Timestamp Target Time Error (TSTRGTERR0):** This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.
2	0h RO	**Auxiliary Timestamp Trigger Snapshot (AUXTSTRIG):** This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Auxiliary Timestamp Trigger Snapshot status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Trigger Snapshot status detected.
1	0h RO	**Timestamp Target Time Reached (TSTARGT0):** When this bit is set and MCGREN0 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN0 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[0] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
0	0h RO	**Timestamp Seconds Overflow (TSSOVF):** When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Seconds Overflow status not detected. 0x1 (ACTIVE): Timestamp Seconds Overflow status detected.

14.20.1.308MAC_TX_TIMESTAMP_STATUS_NANOSECONDS — Offset 50200B30h

This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled.

The MAC_Tx_Timestamp_Status_Nanoseconds register, along with MAC_Tx_Timestamp_Status_Seconds, gives the 64-bit timestamp captured for the PTP packet successfully transmitted by the MAC. This value is considered to be read by the application when the last byte (bits[31:24]) of MAC_Tx_Timestamp_Status_Nanoseconds is read.

If the application does not read these registers and timestamp of another packet is captured, then either the current timestamp is lost (overwritten) or the new timestamp is lost (dropped), depending on the setting of the TXTSSTSM bit of the MAC_Timestamp_Control register. The status bit TXTSC bit [15] in MAC_Timestamp_Status register is set whenever the MAC transmitter captures the timestamp.

Type	Size	Offset	Default
MMIO	32 bit	50200B30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Transmit Timestamp Status Missed (TXTSSMIS):** When this bit is set, it indicates one of the following: - The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset - The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Transmit Timestamp Status Missed status not detected. 0x1 (ACTIVE): Transmit Timestamp Status Missed status detected.
30:0	00000000h RO	**Transmit Timestamp Status Low (TXTSSLO):** This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

14.20.1.309MAC_TX_TIMESTAMP_STATUS_SECONDS — Offset 50200B34h

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.

Type	Size	Offset	Default
MMIO	32 bit	50200B34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmit Timestamp Status High (TXTSSHI):** This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

14.20.1.310MAC_AUXILIARY_CONTROL — Offset 50200B40h

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.

Type	Size	Offset	Default
MMIO	32 bit	50200B40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Auxiliary Snapshot 1 Enable (ATSEN1):** This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
4	0h RW	**Auxiliary Snapshot 0 Enable (ATSEN0):** This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Auxiliary Snapshot FIFO Clear (ATSFC):** When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Auxiliary Snapshot FIFO Clear is disabled. 0x1 (ENABLE): Auxiliary Snapshot FIFO Clear is enabled.

14.20.1.311MAC_AUXILIARY_TIMESTAMP_NANOSECONDS — Offset 50200B48h

The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected while configuring the core.

You can store multiple snapshots in this FIFO. Bits[29:25] in MAC_Timestamp_Status indicate the fill-level of the FIFO. The top of the FIFO is removed only when the last byte (bits[31:24]) MAC_Auxiliary_Timestamp_Seconds register is read.

Type	Size	Offset	Default
MMIO	32 bit	50200B48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Auxiliary Timestamp (AUXTSLO):** Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

14.20.1.312MAC_AUXILIARY_TIMESTAMP_SECONDS — Offset 50200B4Ch

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Type	Size	Offset	Default
MMIO	32 bit	50200B4Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Auxiliary Timestamp (AUXTSHI):** Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

14.20.1.313MAC_TIMESTAMP_INGRESS_ASYM_CORR — Offset 50200B50h

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	50200B50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Ingress Asymmetry Correction (OSTIAC):** This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

14.20.1.314MAC_TIMESTAMP_EGRESS_ASYM_CORR — Offset 50200B54h

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	50200B54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Egress Asymmetry Correction (OSTEAC):** This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000(2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216).

14.20.1.315MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND — Offset 50200B58h

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

Type	Size	Offset	Default
MMIO	32 bit	50200B58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Ingress Correction (TSIC):** This field contains the ingress path correction value as defined by the Ingress Correction expression.

14.20.1.316MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND — Offset 50200B5Ch

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

Type	Size	Offset	Default
MMIO	32 bit	50200B5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Egress Correction (TSEC):** This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

14.20.1.317MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC — Offset 50200B60h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for ingress direction.

Type	Size	Offset	Default
MMIO	32 bit	50200B60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Ingress Correction, sub-nanoseconds (TSICSNS):** This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression.
7:0	0h RO	**Reserved**

14.20.1.318MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC — Offset 50200B64h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for egress direction.

Type	Size	Offset	Default
MMIO	32 bit	50200B64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Egress Correction, sub-nanoseconds (TSECSNS):** This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression.
7:0	0h RO	**Reserved**

14.20.1.319MAC_TIMESTAMP_INGRESS_LATENCY — Offset 50200B68h

This register holds the Ingress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	50200B68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Ingress Timestamp Latency, in sub-nanoseconds (ITLNS):** This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	00h RO	**Ingress Timestamp Latency, in nanoseconds (ITLSNS):** This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	0h RO	**Reserved**

14.20.1.320MAC_TIMESTAMP_EGRESS_LATENCY — Offset 50200B6Ch

This register holds the Egress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	50200B6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Egress Timestamp Latency, in nanoseconds (ETLNS):** This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	00h RO	**Egress Timestamp Latency, in sub-nanoseconds (ETLSNS):** This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	0h RO	**Reserved**

14.20.1.321MAC_PPS_CONTROL — Offset 50200B70h

PPS Control register. Bits[30:24] of this register are valid only when four Flexible PPS outputs are selected. Bits[22:16] are valid only when three or more Flexible PPS outputs are selected. Bits[14:8] are valid only when two or more Flexible PPS outputs are selected. Bits[6:4] are valid only when Flexible PPS feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50200B70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Time Select (TRGTMODSEL1):** When set, 64-bit PTP time is used to capture time at MCGR trigger[0] input. When reset, presentation time is used to capture time at trigger input, maintaining backward compatibility.
27:16	0h RO	**Reserved**
15	0h RW	**MCGR Mode Enable for PPS1 Output (MCGREN1):** This field enables the 1st PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (DISABLE): 1st PPS instance is disabled to operate in PPS or MCGR mode. 0x1 (ENABLE): 1st PPS instance is enabled to operate in PPS or MCGR mode.
14:13	0h RW	**Target Time Register Mode for PPS1 Output (TIMESEL):** This field indicates the Target Time registers (MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds) mode for PPS1 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT1 (MAC_Timestamp_Status[4]). 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
12	0h RO	**Reserved**
11:8	0h RW	**Flexible PPS1 Output Control (PPSCMD1):** This field controls the flexible PPS1 output signal. This field is similar to the PPSCMD0 field. If MCGREN1 is set, then PPSCMD1 indicated by these 4 bits [11:8] are taken as Presentation Time Control bits for media clock generation and recovery for comparator instance 1. This field is similar to the PPSCMD0 Presentation Time Control bits. If MCGREN1 is not set then only 3 bits from [10:8] is used as PPSCMD1 and the 4th bit is to be set as 0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**MCGR Mode Enable for PPS0 Output (MCGREN0):** This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode. 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Target Time Register Mode for PPS0 Output (TRGTMODSEL0):** Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT0 (MAC_Timestamp_Status[1]) 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
4	0h RW	**Flexible PPS Output Mode Enable (PPSEN0):** When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). 0x0 (DISABLE): Flexible PPS Output Mode is disabled. 0x1 (ENABLE): Flexible PPS Output Mode is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**PPS Output Frequency Control (PPSCTRL_PPSCMD):** This field controls the frequency of the PPS0 output signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: - 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. - 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. - 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. - 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. - .. - 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output signal has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: - When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms - When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) - When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high) This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. or Flexible PPS Output Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: - 0000: No Command - 0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. - 0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. - 0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. - 0100: STOP Pulse train at time This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. - 0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). - 110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. - 0111-1111: Reserved or Presentation Time Control If MCGREN0 is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: - 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed - 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0100-1000: Reserved - 1001: Toggle output on compare - 1010: Pulse output low on compare for one PTP-clock cycle - 1011: Pulse output high on compare for one PTP-clock cycle

14.20.1.322MAC_PPS0_TARGET_TIME_SECONDS — Offset 50200B80h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	50200B80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH0):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

14.20.1.323MAC_PPS0_TARGET_TIME_NANOSECONDS — Offset 50200B84h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	50200B84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY0):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL0):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

14.20.1.324MAC_PPS0_INTERVAL — Offset 50200B88h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50200B88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT0):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

14.20.1.325MAC_PPS0_WIDTH — Offset 50200B8Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50200B8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH0):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

14.20.1.326MAC_PPS1_TARGET_TIME_SECONDS — Offset 50200B90h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	50200B90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH1):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

14.20.1.327MAC_PPS1_TARGET_TIME_NANOSECONDS — Offset 50200B94h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	50200B94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY1):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL1):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

14.20.1.328MAC_PPS1_INTERVAL — Offset 50200B98h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50200B98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT1):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

14.20.1.329MAC_PPS1_WIDTH — Offset 50200B9Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50200B9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH1):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

14.20.1.330MAC_PTO_CONTROL — Offset 50200BC0h

This register controls the PTP Offload Engine operation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50200BC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Domain Number (DN):** This field indicates the domain Number in which the PTP node is operating.
7	0h RW	**Disable Peer Delay Response response generation (PDRDIS):** When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not be generated for received Peer Delay Request (Pdelay_Req) request packet, as required by the programmed mode. Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in Hardware and/or Pdelay_Resp generation is handled by Software. 0x0 (ENABLE): Peer Delay Response response generation is enabled. 0x1 (DISABLE): Peer Delay Response response generation is disabled.
6	0h RW	**Disable PTO Delay Request/Response response generation (DRRDIS):** When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode. 0x0 (ENABLE): PTO Delay Request/Response response generation is enabled. 0x1 (DISABLE): PTO Delay Request/Response response generation is disabled.
5	0h RW	**Automatic PTP Pdelay_Req message Trigger (APDREQTRIG):** When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP Pdelay_Req message Trigger is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message Trigger is enabled.
4	0h RW	**Automatic PTP SYNC message Trigger (ASYNCTRIG):** When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP SYNC message Trigger is disabled. 0x1 (ENABLE): Automatic PTP SYNC message Trigger is enabled.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Automatic PTP Pdelay_Req message Enable (APDREQEN):** When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode. 0x0 (DISABLE): Automatic PTP Pdelay_Req message is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message is enabled.
1	0h RW	**Automatic PTP SYNC message Enable (ASYNCEN):** When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Master mode. 0x0 (DISABLE): Automatic PTP SYNC message is disabled. 0x1 (ENABLE): Automatic PTP SYNC message is enabled.
0	0h RW	**PTP Offload Enable (PTOEN):** When this bit is set, the PTP Offload feature is enabled. 0x0 (DISABLE): PTP Offload feature is disabled. 0x1 (ENABLE): PTP Offload feature is enabled.

14.20.1.331MAC_SOURCE_PORT_IDENTITY0 — Offset 50200BC4h

This register contains Bits[31:0] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50200BC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 0 (SPI0):** This field indicates bits [31:0] of sourcePortIdentity of PTP node.

14.20.1.332MAC_SOURCE_PORT_IDENTITY1 — Offset 50200BC8h

This register contains Bits[63:32] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50200BC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 1 (SPI1):** This field indicates bits [63:32] of sourcePortIdentity of PTP node.

14.20.1.333MAC_SOURCE_PORT_IDENTITY2 — Offset 50200BCCh

This register contains Bits[79:64] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50200BCCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Source Port Identity 2 (SPI2):** This field indicates bits [79:64] of sourcePortIdentity of PTP node.

14.20.1.334MAC_LOG_MESSAGE_INTERVAL — Offset 50200BD0h

This register contains the periodic intervals for automatic PTP packet generation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50200BD0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Log Min Pdelay_Req Interval (LMPDRI):** This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15.Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	0h RO	**Reserved**
10:8	0h RW	**DRSYNCR:** Delay_Req to SYNC Ratio In Slave mode, it is used for controlling frequency of Delay_Req messages transmitted. - 0: DelayReq generated for every received SYNC - 1: DelayReq generated every alternate reception of SYNC - 2: for every 4 SYNC messages - 3: for every 8 SYNC messages - 4: for every 16 SYNC messages - 5: for every 32 SYNC messages - 6-7: Reserved The master sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the slave. The GbE Controller Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Slave mode, the host must not write/update this register unless it has to override the received value. In Master mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. 0x0 (SYNC1): DelayReq generated for every received SYNC. 0x1 (SYNC2): DelayReq generated every alternate reception of SYNC. 0x2 (SYNC4): for every 4 SYNC messages. 0x3 (SYNC8): for every 8 SYNC messages. 0x4 (SYNC16): for every 16 SYNC messages. 0x5 (SYNC32): for every 32 SYNC messages. 0x6 (RSVD): Reserved.
7:0	00h RW	**LSI:** Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Master. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.

14.20.1.335MTL_OPERATION_MODE — Offset 50200C00h

The Operation Mode register establishes the Transmit and Receive operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	50200C00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Flexible Rx parser Enable (FRPE):** When this bit is set to 1, the Programmable Rx Parser functionality is enabled. When the Rx parser is disabled and if the Rx parser is in the middle of the parsing then it gets disabled only after completing the current packet parsing. When the Rx parser is enabled from disabled state then the Rx parser gets activated for the next immediate packet. 0x0 (DISABLE): Flexible Rx parser is disabled. 0x1 (ENABLE): Flexible Rx parser is enabled.
14	0h RW	**RxParser Software Error/Incomplete Parsing Packet Drop Enable (RXPED):** When set to 0, packets encountering software programming errors (NPE/NVE/frame offset overflow errors) or incomplete parsing are forwarded to application with the corresponding RxParser status. When set to 1, backward compatibility is maintained where all above mentioned packets are dropped (when RA is not set). 0x0 (DISABLE): Flexible Rx parser, packet drop in case software error is disabled. 0x1 (ENABLE): Flexible Rx parser, packet drop in case software error is enabled.
13:10	0h RO	**Reserved**
9	0h RW	**Counters Reset (CNTCLR):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.
8	0h RW	**Counters Preset (CNTPRST):** When this bit is set, - MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
7	0h RO	**Reserved**
6:5	0h RW	**Tx Scheduling Algorithm (SCHALG):** This field indicates the algorithm for Tx scheduling: 0x0 (WRR): WRR algorithm. 0x1 (WFQ): WFQ algorithm when DCB feature is selected.Otherwise, Reserved. 0x2 (DWRR): DWRR algorithm when DCB feature is selected.Otherwise, Reserved. 0x3 (SP): Strict priority algorithm.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RO	**Reserved**
2	0h RW	**Receive Arbitration Algorithm (RAA):** This field is used to select the arbitration algorithm for the Rx side. - 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. - 1: Weighted Strict Priority (WSP) 0x0 (SP): Strict priority (SP). 0x1 (WSP): Weighted Strict Priority (WSP).
1	0h RW	**Drop Transmit Status (DTXSTS):** When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. 0x0 (DISABLE): Drop Transmit Status is disabled. 0x1 (ENABLE): Drop Transmit Status is enabled.
0	0h RO	**Reserved**

14.20.1.336MTL_DBG_CTL — Offset 50200C08h

The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	50200C08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RW	**ECC Inject Error Control for Tx, Rx and TSO memories (EIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
16	0h RW	**ECC Inject Error Enable for Tx, Rx and TSO memories (EIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Tx, Rx and TSO memories is disabled. 0x1 (ENABLE): ECC Inject Error for Tx, Rx and TSO memories is enabled.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Transmit Status Available Interrupt Status Enable (STSIE):** When this bit is set, an interrupt is generated when Transmit status is available in slave mode. 0x0 (DISABLE): Transmit Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Transmit Packet Available Interrupt Status is enabled.
14	0h RW	**Receive Packet Available Interrupt Status Enable (PKTIE):** When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. 0x0 (DISABLE): Receive Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Receive Packet Available Interrupt Status is enabled.
13:12	0h RW	**FIFO Selected for Access (FIFOSEL):** This field indicates the FIFO selected for debug access: 0x0 (TXFIFO): Tx FIFO. 0x1 (TXSTSFIFO): Tx Status FIFO (only read access when SLVMOD is set). 0x2 (TSOFIFO): TSO FIFO (cannot be accessed when SLVMOD is set). 0x3 (RXFIFO): Rx FIFO.
11	0h RW	**FIFO Write Enable (FIFOWREN):** When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Write is disabled. 0x1 (ENABLE): FIFO Write is enabled.
10	0h RW	**FIFO Read Enable (FIFORDEN):** When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Read is disabled. 0x1 (ENABLE): FIFO Read is enabled.
9	0h RW	**Reset Pointers of Selected FIFO (RSTSEL):** When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset Pointers of Selected FIFO is disabled. 0x1 (ENABLE): Reset Pointers of Selected FIFO is enabled.
8	0h RW	**Reset All Pointers (RSTALL):** When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset All Pointers is disabled. 0x1 (ENABLE): Reset All Pointers is enabled.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Encoded Packet State (PKTSTATE):** This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
4	0h RO	**Reserved**
3:2	0h RW	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
1	0h RW	**Debug Mode Access to FIFO (DBGMOD):** When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: - Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO - Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: - Write access to the Tx FIFO - Read access to the Rx FIFO and Tx Status FIFO 0x0 (DISABLE): Debug Mode Access to FIFO is disabled. 0x1 (ENABLE): Debug Mode Access to FIFO is enabled.
0	0h RW	**FIFO Debug Access Enable (FDBGEN):** When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. 0x0 (DISABLE): FIFO Debug Access is disabled. 0x1 (ENABLE): FIFO Debug Access is enabled.

14.20.1.337MTL_DBG_STS — Offset 50200C0Ch

The FIFO Debug Status register contains the status of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	50200C0Ch	00000018h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RO	**Remaining Locations in the FIFO (LOCR):** Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively.
14:10	0h RO	**Reserved**
9	0h RW	**Transmit Status Available Interrupt Status (STSI):** When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Transmit Status Available Interrupt Status not detected. 0x1 (ACTIVE): Transmit Status Available Interrupt Status detected.
8	0h RW	**Receive Packet Available Interrupt Status (PKTI):** When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Receive Packet Available Interrupt Status not detected. 0x1 (ACTIVE): Receive Packet Available Interrupt Status detected.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:3	3h RO	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
2:1	0h RO	**Encoded Packet State (PKTSTATE):** This field is used to get the control or status information of the selected FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
0	0h RO	**FIFO Busy (FIFOBUSY):** When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: - All other fields of this register - All fields of the MTL_FIFO_Debug_Data register 0x0 (INACTIVE): FIFO Busy not detected. 0x1 (ACTIVE): FIFO Busy detected.

14.20.1.338MTL_FIFO_DEBUG_DATA — Offset 50200C10h

The FIFO Debug Data register contains the data to be written to or read from the FIFOs.

Type	Size	Offset	Default
MMIO	32 bit	50200C10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FIFO Debug Data (FDBGDATA):** During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

14.20.1.339MTL_INTERRUPT_STATUS — Offset 50200C20h

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50200C20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MTL Rx Parser Interrupt Status (MTLPIS):** This bit indicates that there is an interrupt from Rx Parser Block. To reset this bit, the application must read the MTL_ Rxp_Interrupt_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Rx Parser Interrupt status not detected. 0x1 (ACTIVE): MTL Rx Parser Interrupt status detected.
22:19	0h RO	**Reserved**
18	0h RO	**EST (TAS- 802.1Qbv) Interrupt Status (ESTIS):** This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt. 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected. 0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Debug Interrupt status (DBGIS):** This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Debug Interrupt status not detected. 0x1 (ACTIVE): Debug Interrupt status detected.
16:8	0h RO	**Reserved**
7	0h RO	**Queue 7 Interrupt status (Q7IS):** This bit indicates that there is an interrupt from Queue 7. To reset this bit, the application must read the MTL_Q7_Interrupt_Control_Status Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 7 Interrupt status not detected. 0x1 (ACTIVE): Queue 7 Interrupt status detected.
6	0h RO	**Queue 6 Interrupt status (Q6IS):** This bit indicates that there is an interrupt from Queue 6. To reset this bit, the application must read the MTL_Q6_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 6 Interrupt status not detected. 0x1 (ACTIVE): Queue 6 Interrupt status detected.
5	0h RO	**Queue 5 Interrupt status (Q5IS):** This bit indicates that there is an interrupt from Queue 5. To reset this bit, the application must read the MTL_Q5_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 5 Interrupt status not detected. 0x1 (ACTIVE): Queue 5 Interrupt status detected.
4	0h RO	**Queue 4 Interrupt status (Q4IS):** This bit indicates that there is an interrupt from Queue 4. To reset this bit, the application must read the MTL_Q4_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 4 Interrupt status not detected. 0x1 (ACTIVE): Queue 4 Interrupt status detected.
3	0h RO	**Queue 3 Interrupt status (Q3IS):** This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 3 Interrupt status not detected. 0x1 (ACTIVE): Queue 3 Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Queue 2 Interrupt status (Q2IS):** This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 2 Interrupt status not detected. 0x1 (ACTIVE): Queue 2 Interrupt status detected.
1	0h RO	**Queue 1 Interrupt status (Q1IS):** This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 1 Interrupt status not detected. 0x1 (ACTIVE): Queue 1 Interrupt status detected.
0	0h RO	**Queue 0 Interrupt status (Q0IS):** This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 0 Interrupt status not detected. 0x1 (ACTIVE): Queue 0 Interrupt status detected.

14.20.1.340MTL_RXQ_DMA_MAP0 — Offset 50200C30h

The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	50200C30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection (Q3DDMACH):** When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]). 0x0 (DISABLE): Queue 3 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 3 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Queue 3 Mapped to DMA Channel (Q3MDMACH):** This field controls the routing of the received packet in Queue 3 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. Note: The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved
23:21	0h RO	**Reserved**
20	0h RW	**Queue 2 Enabled for DA-based DMA Channel Selection (Q2DDMACH):** When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]). 0x0 (DISABLE): Queue 2 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 2 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**
18:16	0h RW	**Queue 2 Mapped to DMA Channel (Q2MDMACH):** This field controls the routing of the received packet in Queue 2 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 1 Enabled for DA-based DMA Channel Selection (Q1DDMACH):** When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]). 0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Queue 1 Mapped to DMA Channel (Q1MDMACH):** This field controls the routing of the received packet in Queue 1 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**
4	0h RW	**Queue 0 Enabled for DA-based DMA Channel Selection (Q0DDMACH):** When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field. 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 0 Mapped to DMA Channel (Q0MDMACH):** This field controls the routing of the packet received in Queue 0 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

14.20.1.341MTL_RXQ_DMA_MAP1 — Offset 50200C34h

The Receive Queue and DMA Channel Mapping 1 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	50200C34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 7 Enabled for DA-based DMA Channel Selection (Q7DDMACH):** When set, this bit indicates that the packets received in Queue 7 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 7 are routed to the DMA Channel programmed in the Q7MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**
26:24	0h RW	**Queue 7 Mapped to DMA Channel (Q7MDMACH):** This field controls the routing of the packet received in Queue 7 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q7DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
23:21	0h RO	**Reserved**
20	0h RW	**Queue 6 Enabled for DA-based DMA Channel Selection (Q6DDMACH):** When set, this bit indicates that the packets received in Queue 6 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 6 are routed to the DMA Channel programmed in the Q6MDMACH field. 0x0 (DISABLE): Queue 6 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 6 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RW	**Queue 6 Mapped to DMA Channel (Q6MDMACH):** This field controls the routing of the packet received in Queue 6 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q6DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 5 Enabled for DA-based DMA Channel Selection (Q5DDMACH):** When set, this bit indicates that the packets received in Queue 5 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 5 are routed to the DMA Channel programmed in the Q5MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**
10:8	0h RW	**Queue 5 Mapped to DMA Channel (Q5MDMACH):** This field controls the routing of the packets received in Queue 5 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q5DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Queue 4 Enabled for DA-based DMA Channel Selection (Q4DDMACH):** When set, this bit indicates that the packets received in Queue 4 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 4 are routed to the DMA Channel programmed in the Q4MDMACH field. 0x0 (DISABLE): Queue 4 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 4 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 4 Mapped to DMA Channel (Q4MDMACH):** This field controls the routing of the packet received in Queue 4 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q4DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

14.20.1.342MTL_TBS_CTRL — Offset 50200C40h

This register controls the operation of Time Based Scheduling.

Type	Size	Offset	Default
MMIO	32 bit	50200C40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**Launch Expiry Offset (LEOS):** The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Launch Expiry GSN Offset (LEGOS):** The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Launch Expiry Offset Valid (LEOV):** When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time. 0x0 (INVALID): LEOS field is invalid. 0x1 (VALID): LEOS field is valid.
0	0h RW	**EST offset Mode (ESTM):** When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8]. 0x0 (DISABLE): EST offset Mode is disabled. 0x1 (ENABLE): EST offset Mode is enabled.

14.20.1.343MTL_EST_CONTROL — Offset 50200C50h

This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	50200C50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PTP Time Offset Value (PTOV):** The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23:12	000h RW	**Current Time Offset Value (CTOV):** Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Time Interval Left Shift Amount (TILS):** This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. - 000: No left shift needed (equal to x1ns) - 001: Left shift TI by 1 bit (equal to x2ns) - 010: Left shift TI by 2 bits (equal to x4ns) - . - . - 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.
7:6	0h RW	**Loop Count to report Scheduling Error (LCSE):** Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register. 0x0 (M_4_ITERNS): 4 iterations. 0x1 (M_8_ITERNS): 8 iterations. 0x2 (M_16_ITERNS): 16 iterations. 0x3 (M_32_ITERNS): 32 iterations.
5	0h RW	**Drop Frames causing Scheduling Error (DFBS):** When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped. 0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error. 0x1 (DROP): Drop Frames causing Scheduling Error.
4	0h RW	**Do not Drop frames during Frame Size Error (DDBF):** When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register). 0x0 (DROP): Drop frames during Frame Size Error. 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error.
3:2	0h RO	**Reserved**
1	0h RW	**Switch to S/W owned list (SSWL):** When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Switch to S/W owned list is disabled. 0x1 (ENABLE): Switch to S/W owned list is enabled.
0	0h RW	**Enable EST (EEST):** When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. If any uncorrectable error is detected in the EST memory the hardware resets this bit and disables the EST function. 0x0 (DISABLE): EST is disabled. 0x1 (ENABLE): EST is enabled.

14.20.1.344MTL_EST_STATUS — Offset 50200C58h

This register provides Status related to Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	50200C58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Current GCL Slot Number (CGSN):** Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:8	00h RO	**BTR Error Loop Count (BTRL):** Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "11111111" indicates the iterations exceeded the value of 128 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	0h RO	**S/W owned list (SWOL):** When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default. 0x0 (INACTIVE): Gate control list number "0" is owned by software. 0x1 (ACTIVE): Gate control list number "1" is owned by software.
6:5	0h RO	**Reserved**
4	0h RW	**Constant Gate Control Error (CGCE):** This error occurs when the list length (LLR) is 1 and the Cycle Time (CTR) is less than or equal to the programmed Time Interval (TI) value after the optional Left Shifting. The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Constant Gate Control Error not detected. 0x1 (ACTIVE): Constant Gate Control Error detected.
3	0h RO	**Head-Of-Line Blocking due to Scheduling (HLBS):** Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Head-Of-Line Blocking due to Frame Size (HLBF):** Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected.
1	0h RW	**BTR Error (BTRE):** When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "11111111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "11111111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): BTR Error not detected. 0x1 (ACTIVE): BTR Error detected.
0	0h RW	**Switch to S/W owned list Complete (SWLC):** When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Switch to S/W owned list Complete not detected. 0x1 (ACTIVE): Switch to S/W owned list Complete detected.

14.20.1.345MTL_EST_SCH_ERROR — Offset 50200C60h

This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout).

Type	Size	Offset	Default
MMIO	32 bit	50200C60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Schedule Error Queue Number (SEQN):** The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

14.20.1.346MTL_EST_FRM_SIZE_ERROR — Offset 50200C64h

This register provides the One Hot encoded Queue Numbers that are having the Frame Size related error.

Type	Size	Offset	Default
MMIO	32 bit	50200C64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Frame Size Error Queue Number (FEQN):** The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

14.20.1.347MTL_EST_FRM_SIZE_CAPTURE — Offset 50200C68h

This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error.

Type	Size	Offset	Default
MMIO	32 bit	50200C68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO	**Queue Number of HLBF (HBFQ):** Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	0h RO	**Reserved**
14:0	0000h RO	**Frame Size of HLBF (HBFS):** Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

14.20.1.348MTL_EST_INTR_ENABLE — Offset 50200C70h

This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status register.

Type	Size	Offset	Default
MMIO	32 bit	50200C70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Interrupt Enable for CGCE (CGCE):** When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt 0x0 (DISABLE): Interrupt for CGCE is disabled. 0x1 (ENABLE): Interrupt for CGCE is enabled.
3	0h RW	**Interrupt Enable for HLBS (IEHS):** When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBS is disabled. 0x1 (ENABLE): Interrupt for HLBS is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt Enable for HLBF (IEHF):** When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBF is disabled. 0x1 (ENABLE): Interrupt for HLBF is enabled.
1	0h RW	**Interrupt Enable for BTR Error (IEBE):** When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for BTR Error is disabled. 0x1 (ENABLE): Interrupt for BTR Error is enabled.
0	0h RW	**Interrupt Enable for Switch List (IECC):** When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for Switch List is disabled. 0x1 (ENABLE): Interrupt for Switch List is enabled.

14.20.1.349MTL_EST_GCL_CONTROL — Offset 50200C80h

This register provides the control information for reading/writing to the Gate Control lists.

Type	Size	Offset	Default
MMIO	32 bit	50200C80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**ECC Inject Error Control for EST Memory (ESTEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
21	0h RW	**EST ECC Inject Error Enable (ESTEIEE):** When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): EST ECC Inject Error is disabled. 0x1 (ENABLE): EST ECC Inject Error is enabled.
20:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16:8	000h RW	**Gate Control List Address: (GCLA when GCRR is "0"). (ADDR):** Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. - 000: BTR Low (31:0) - 001: BTR High (63:31) - 010: CTR Low (31:0) - 011: CTR High (39:32) - 100: TER (31:0) - 101: LLR (n:0) (where n is (log{512} / log2)) - Others: Reserved
7:6	0h RO	**Reserved**
5	0h RW	**Debug Mode Bank Select (DBGB):** When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used. 0x0 (BANK0): R/W in debug mode should be directed to Bank 0. 0x1 (BANK1): R/W in debug mode should be directed to Bank 1.
4	0h RW	**Debug Mode (DBGM):** When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use. 0x0 (DISABLE): Debug Mode is disabled. 0x1 (ENABLE): Debug Mode is enabled.
3	0h RO	**Reserved**
2	0h RW	**Gate Control Related Registers (GCRR):** When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA. 0x0 (DISABLE): Gate Control Related Registers are disabled. 0x1 (ENABLE): Gate Control Related Registers are enabled.
1	0h RW	**Read '1', Write '0': (R1W0):** When set to '1': Read Operation When set to '0': Write Operation. 0x0 (WRITE): Write Operation. 0x1 (READ): Read Operation.
0	0h RW	**Start Read/Write Op (SRWO):** When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Start Read/Write Op disabled. 0x1 (ENABLE): Start Read/Write Op enabled.

14.20.1.350MTL_EST_GCL_DATA — Offset 50200C84h

This register holds the read data or write data in case of reads and writes respectively.

Type	Size	Offset	Default
MMIO	32 bit	50200C84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Gate Control Data (GCD):** The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

14.20.1.351MTL_FPE_CTRL_STS — Offset 50200C90h

This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br).

Type	Size	Offset	Default
MMIO	32 bit	50200C90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**HRS:** Hold/Release Status - 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. - 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State.
27:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**Preemption Classification (PEC):** When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	0h RO	**Reserved**
1:0	0h RW	**Additional Fragment Size (AFSZ):** used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes

14.20.1.352MTL_FPE_ADVANCE — Offset 50200C94h

This register holds the Hold and Release Advance time.

Type	Size	Offset	Default
MMIO	32 bit	50200C94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Release Advance (RADV):** The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.
15:0	0000h RW	**Hold Advance (HADV):** The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

14.20.1.353MTL_RXP_CONTROL_STATUS — Offset 50200CA0h

The MTL_RXP_Control_Status register establishes the operating mode of Rx Parser and provides some status.

Type	Size	Offset	Default
MMIO	32 bit	50200CA0h	80FF00FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**RX Parser in Idle state (RXPI):** This status bit is set to 1 when the Rx parser is in Idle State and waiting for a new packet for processing. This bit is used as a handshake with software when parser gets disables. After disabling, when bit is set then software can update the Rx parser instruction table. 0x0 (INACTIVE): RX Parser not in Idle state. 0x1 (ACTIVE): RX Parser in Idle state.
30:24	0h RO	**Reserved**
23:16	FFh RW	**Number of parsable entries in the Instruction table (NPE):** This control indicates the number of parsable entries in the Instruction Memory. This is used in Rx parser logic to detect programming Error. In case number of parsed entries for a packet is more than this entry then NPEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set.
15:8	0h RO	**Reserved**
7:0	FFh RW	**Number of valid entry address/index in the Instruction table (NVE):** This control indicates the number of valid entries address/index in the Instruction Memory (i.e. when NVE field in register=31, the maximum valid entry address is NVE+1 i.e. addresses/indices=0 to 32, or 33 entries). This is used in Rx parser logic to detect any programming Error. In case while parsing Table address (memory address) found to be more than this maximum valid entry address then NVEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set. Note: The minimum value of this should be 2.

14.20.1.354MTL_RXP_INTERRUPT_CONTROL_STATUS — Offset 50200CA4h

The MTL_RXP_Interrupt_Control_Status registers provides enable control for the interrupts and provides interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	50200CA4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Packet Drop due to RF Interrupt Enable (PDRFIE):** When this bit is set, the PDRFIS interrupt is enabled. When this bit is reset, the PDRFIS interrupt is disabled. 0x0 (DISABLE): Packet Drop due to RF Interrupt is disabled. 0x1 (ENABLE): Packet Drop due to RF Interrupt is enabled.
18	0h RW	**Frame Offset Overflow Interrupt Enable (FOOVIE):** When this bit is set, the FOOVIS interrupt is enabled. When this bit is reset, the FOOVIS interrupt is disabled. 0x0 (DISABLE): Frame Offset Overflow Interrupt is disabled. 0x1 (ENABLE): Frame Offset Overflow Interrupt is enabled.
17	0h RW	**Number of Parsable Entries Overflow Interrupt Enable (NPEOVIE):** When this bit is set, the NPEOVIS interrupt is enabled. When this bit is reset, the NPEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Parsable Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Parsable Entries Overflow Interrupt is enabled.
16	0h RW	**Number of Valid Entries Overflow Interrupt Enable (NVEOVIE):** When this bit is set, the NVEOVIS interrupt is enabled. When this bit is reset, the NVEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Valid Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Valid Entries Overflow Interrupt is enabled.
15:4	0h RO	**Reserved**
3	0h RW	**Packet Dropped due to RF Interrupt Status (PDRFIS):** If the Rx Parser result says to drop the packet by setting RF=1 in the instruction memory, then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Packet Dropped due to RF Interrupt Status not detected. 0x1 (ACTIVE): Packet Dropped due to RF Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Frame Offset Overflow Interrupt Status (FOOVIS):** While parsing if the Instruction table entry's 'Frame Offset' found to be more than EOF offset, then then this bit is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Frame Offset Overflow Interrupt Status not detected. 0x1 (ACTIVE): Frame Offset Overflow Interrupt Status detected.
1	0h RW	**Number of Parsable Entries Overflow Interrupt Status (NPEOVIS):** While parsing a packet if the number of parsed entries found to be more than NPE[] (Number of Parseable Entries in MTL_RXP_Control register),then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Parsable Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Parsable Entries Overflow Interrupt Status detected.
0	0h RW	**Number of Valid Entry Address/Index Overflow Interrupt Status (NVEOVIS):** While parsing if the Instruction address found to be more than NVE (Number of Valid Entry Address/index in MTL_RXP_Control register), then this bit is set to 1. For example, when NVE field in register=31, the maximum valid entry address/index is NVE+1 i.e. 32 (addresses/indices=0 to 32, or 33 entries), so NVEOVIS is set when currently processed entry indicates next address is 33 or more i.e. 34th or later entries. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Valid Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Valid Entries Overflow Interrupt Status detected.

14.20.1.355MTL_RXP_DROP_CNT — Offset 50200CA8h

The MTL_RXP_Drop_Cnt register provides the drop count of Rx Parser initiated drops.

Type	Size	Offset	Default
MMIO	32 bit	50200CA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Drop Counter Overflow Bit (RXPDCOVF):** When set, this bit indicates that the MTL_RXP_Drop_cnt (RXPDC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Drop count overflow not occurred. 0x1 (ACTIVE): Rx Parser Drop count overflow occurred.
30:0	00000000h RO	**Rx Parser Drop count (RXPDC):** This 31-bit counter is implemented whenever a Rx Parser Drops a packet due to RF =1. The counter is cleared when the register is read.

14.20.1.356MTL_RXP_ERROR_CNT — Offset 50200CACh

The MTL_RXP_Error_Cnt register provides the Rx Parser related error occurrence count.

Type	Size	Offset	Default
MMIO	32 bit	50200CACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Error Counter Overflow Bit (RXPECOVF):** When set, this bit indicates that the MTL_RXP_Error_cnt (RXPEC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Error count overflow not occurred. 0x1 (ACTIVE): Rx Parser Error count overflow occurred.
30:0	00000000h RO	**Rx Parser Error count (RXPEC):** This 31-bit counter is implemented whenever a Rx Parser encounters following Error scenarios - Entry address >= NVE[] - Number Parsed Entries >= NPE[] - Entry address > EOF data entry address The counter is cleared when the register is read.

14.20.1.357MTL_RXP_INDIRECT_ACC_CONTROL_STATUS — Offset 50200CB0h

The MTL_RXP_Indirect_Acc_Control_Status register provides the Indirect Access control and status for Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	50200CB0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**FRP Instruction Table Access Busy (STARTBUSY):** When this bit is set to 1 by the software then it indicates to start the Read/Write operation from/to the Rx Parser Memory. Software should read this bit as 0 before issuing read or write request to access the Parser Memory Instructions. This bit when set to 1 indicates that hardware is busy until its gets cleared by hardware and software should not issue any read or write operation. 0x0 (INACTIVE): hardware not busy. 0x1 (ACTIVE): hardware is busy (Read/Write operation from/to the Rx Parser Memory).
30:23	0h RO	**Reserved**
22:21	0h RW	**ECC Inject Error Control for Rx Parser Memory (RXPEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
20	0h RW	**ECC Inject Error Enable for Rx Parser Memory (RXPEIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Rx Parser Memory is disabled. 0x1 (ENABLE): ECC Inject Error for Rx Parser Memory is enabled.
19:17	0h RO	**Reserved**
16	0h RW	**Read Write Control (WRRDN):** When this bit is set to 1 indicates the write operation to the Rx Parser Memory. When this bit is set to 0 indicates the read operation to the Rx Parser Memory. 0x0 (READ): Read operation to the Rx Parser Memory. 0x1 (WRITE): Write operation to the Rx Parser Memory.
15:10	0h RO	**Reserved**
9:0	000h RW	**FRP Instruction Table Offset Address (ADDR):** This field indicates the ADDR of the 32-bit entry in Rx parser instruction table. Each entry has 128-bit (4x32-bit words). There are 256 FRP entries. This must be written by the software before issuing any Read/Write command. The hardware does not support auto-increment of ADDR.

14.20.1.358MTL_RXP_INDIRECT_ACC_DATA — Offset 50200CB4h

The MTL_RXP_Indirect_Acc_Data registers holds the data associated to Indirect Access to Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	50200CB4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**FRP Instruction Table Write/Read Data (DATA):** Software should write this register before issuing any write command. The hardware provides the read data from the Rx Parser Memory for read operation when STARTBUSY =0 after read command.

14.20.1.359MTL_ECC_CONTROL — Offset 50200CC0h

The MTL_ECC_Control register establishes the operating mode of ECC related to MTL memories.

Type	Size	Offset	Default
MMIO	32 bit	50200CC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**MTL ECC Error Address Status Over-ride (MEEAO):** When set, the following error address fields hold the last valid address where the error is detected. When reset, the following error address fields hold the first address where the error is detected. EUEAS/ECEAS of MTL_ECC_Err_Addr_Status register. 0x0 (DISABLE): MTL ECC Error Address Status Over-ride is disabled. 0x1 (ENABLE): MTL ECC Error Address Status Over-ride is enabled.
7:5	0h RO	**Reserved**
4	0h RW	**TSO memory ECC Enable (TSOEE):** When set to 1, enables the ECC feature for TSO memory in DMA. When set to zero, disables the ECC feature for TSO memory in DMA. 0x0 (DISABLE): TSO memory ECC is disabled. 0x1 (ENABLE): TSO memory ECC is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**MTL Rx Parser ECC Enable (MRXPEE):** When set to 1, enables the ECC feature for Rx Parser memory. When set to zero, disables the ECC feature for Rx Parser memory. 0x0 (DISABLE): MTL Rx Parser ECC is disabled. 0x1 (ENABLE): MTL Rx Parser ECC is enabled.
2	0h RW	**MTL EST ECC Enable (MESTEE):** When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory. 0x0 (DISABLE): MTL EST ECC is disabled. 0x1 (ENABLE): MTL EST ECC is enabled.
1	0h RW	**MTL Rx FIFO ECC Enable (MRXEE):** When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory. 0x0 (DISABLE): MTL Rx FIFO ECC is disabled. 0x1 (ENABLE): MTL Rx FIFO ECC is enabled.
0	0h RW	**MTL Tx FIFO ECC Enable (MTXEE):** When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory. 0x0 (DISABLE): MTL Tx FIFO ECC is disabled. 0x1 (ENABLE): MTL Tx FIFO ECC is enabled.

14.20.1.360MTL_SAFETY_INTERRUPT_STATUS — Offset 50200CC4h

The MTL_Safety_Interrupt_Status registers provides Safety interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	50200CC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MTL ECC Uncorrectable error Interrupt Status (MEUIS):** This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**MTL ECC Correctable error Interrupt Status (MECIS):** This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Correctable error Interrupt Status detected.

14.20.1.361MTL_ECC_INTERRUPT_ENABLE — Offset 50200CC8h

The MTL_ECC_Interrupt_Enable register provides enable bits for the ECC interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50200CC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Rx Parser memory Correctable Error Interrupt Enable (RPCEIE):** When set, generates an interrupt when an uncorrectable error is detected at the Rx Parser memory interface. It is indicated in RPCES status bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx Parser memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx Parser memory Correctable Error Interrupt is enabled.
11:9	0h RO	**Reserved**
8	0h RW	**EST memory Correctable Error Interrupt Enable (ECEIE):** When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): EST memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): EST memory Correctable Error Interrupt is enabled.
7:5	0h RO	**Reserved**
4	0h RW	**Rx memory Correctable Error Interrupt Enable (RXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx memory Correctable Error Interrupt is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Tx memory Correctable Error Interrupt Enable (TXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Tx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Tx memory Correctable Error Interrupt is enabled.

14.20.1.362MTL_ECC_INTERRUPT_STATUS — Offset 50200CCCh

The MTL_ECC_Interrupt_Status register provides MTL ECC Interrupt Status.

Type	Size	Offset	Default
MMIO	32 bit	50200CCCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**Rx Parser memory Uncorrectable Error Status (RPUES):** When set, indicates that an uncorrectable error is detected at Rx Parser memory interface. 0x0 (INACTIVE): Rx Parser memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): Rx Parser memory Uncorrectable Error Status detected.
13	0h RW	**MTL Rx Parser memory Address Mismatch Status (RPAMS):** This bit when set indicates that address mismatch is found for address bus of Rx Parser memory. 0x0 (INACTIVE): MTL Rx Parser memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Address Mismatch Status detected.
12	0h RW	**MTL Rx Parser memory Correctable Error Status (RPCES):** This bit when set indicates that correctable error is detected at RX Parser memory interface. 0x0 (INACTIVE): MTL Rx Parser memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Correctable Error Status detected.
11	0h RO	**Reserved**
10	0h RW	**MTL EST memory Uncorrectable Error Status (EUES):** When set, indicates that an uncorrectable error is detected at MTL EST memory interface. 0x0 (INACTIVE): MTL EST memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Uncorrectable Error Status detected.
9	0h RW	**MTL EST memory Address Mismatch Status (EAMS):** This bit when set indicates that address mismatch is found for address bus of MTL EST memory. 0x0 (INACTIVE): MTL EST memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL EST memory Address Mismatch Status detected.
8	0h RW	**MTL EST memory Correctable Error Status (ECES):** This bit when set indicates that correctable error is detected at the MTL EST memory. 0x0 (INACTIVE): MTL EST memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Correctable Error Status detected.
7	0h RO	**Reserved**
6	0h RW	**MTL Rx memory Uncorrectable Error Status (RXUES):** When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface. 0x0 (INACTIVE): MTL Rx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory Uncorrectable Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**MTL Rx memory Address Mismatch Status (RXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx memory Address Mismatch Status detected.
4	0h RW	**MTL Rx memory Correctable Error Status (RXCES):** This bit when set indicates that correctable error is detected at the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory correctable Error Status detected.
3	0h RO	**Reserved**
2	0h RW	**MTL Tx memory Uncorrectable Error Status (TXUES):** When set, indicates that an uncorrectable error is detected at the MTL TX memory interface. 0x0 (INACTIVE): MTL Tx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Uncorrectable Error Status detected.
1	0h RW	**MTL Tx memory Address Mismatch Status (TXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Tx memory Address Mismatch Status detected.
0	0h RW	**MTL Tx memory Correctable Error Status (TXCES):** This bit when set indicates that a correctable error is detected at the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Correctable Error Status detected.

14.20.1.363MTL_ECC_ERR_STS_RCTL — Offset 50200CD0h

The MTL_ECC_Err_Sts_Rctl register establishes the control for ECC Error status capture.

Type	Size	Offset	Default
MMIO	32 bit	50200CD0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Clear Uncorrectable Error Status (CUES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Uncorrectable Error Status not detected. 0x1 (ACTIVE): Clear Uncorrectable Error Status detected.
4	0h RW	**Clear Correctable Error Status (CCES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Correctable Error Status not detected. 0x1 (ACTIVE): Clear Correctable Error Status detected.
3:1	0h RW	**MTL ECC Memory Selection (EMS):** When EESRE bit of this register is set, this field indicates which memory's error status value to be read. The memory selection encoding is as described below. 0x0 (TX_MEM): MTL Tx memory. 0x1 (RX_MEM): MTL Rx memory. 0x2 (EST_MEM): MTL EST memory. 0x3 (RXP_MEM): MTL Rx Parser memory. 0x4 (TSO_MEM): DMA TSO memory.
0	0h RW	**MTL ECC Error Status Read Enable (EESRE):** When this bit is set, based on the EMS field of this register, the respective memory's error status values are captured as described: - The correctable and uncorrectable error count values are captured into MTL_ECC_Err_Cnt_Status register - The address location's of correctable and uncorrectable errors are captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers. 0x0 (DISABLE): MTL ECC Error Status Read is disabled. 0x1 (ENABLE): MTL ECC Error Status Read is enabled.

14.20.1.364MTL_ECC_ERR_ADDR_STATUS — Offset 50200CD4h

The MTL_ECC_Err_Addr_Status register provides the memory addresses for the correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	50200CD4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**MTL ECC Uncorrectable Error Address Status (EUEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected.
15:0	0000h RO	**MTL ECC Correctable Error Address Status (ECEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected.

14.20.1.365MTL_ECC_ERR_CNTR_STATUS — Offset 50200CD8h

The MTL_ECC_Err_Cntr_Status register provides ECC Error count for Correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	50200CD8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO	**MTL ECC Uncorrectable Error Counter Status (EUECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's uncorrectable error count value.
15:8	0h RO	**Reserved**
7:0	00h RO	**MTL ECC Correctable Error Counter Status (ECECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value.

14.20.1.366MTL_DPP_CONTROL — Offset 50200CE0h

The MTL_DPP_Control establishes the operating mode of Data Parity protection and error injection.

Type	Size	Offset	Default
MMIO	32 bit	50200CE0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**Insert Parity error in CSR Read data parity generator (IPECW):** When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in AXI slave Interface Data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in CSR Read data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in CSR Read data parity generator is enabled.
12	0h RW	**Insert Parity error in AXI Slave Write data parity generator (IPEASW):** When set to 1, parity bit of first valid data generated by the AXI parity generator is (or at PG9 as shown in AXI slave Interface Data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in AXI Slave Write data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in AXI Slave Write data parity generator is enabled.
11	0h RW	**Insert Parity error in Rx write-back Descriptor parity generator (IPERD):** When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Receive data path parity protection diagram) is flipped. 0x0 (DISABLE): Insert Parity error in Rx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Rx write-back Descriptor parity generator is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Insert Parity error in Tx write-back Descriptor parity generator (IPETD):** When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in Tx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Tx write-back Descriptor parity generator is enabled.
9	0h RW	**Insert Parity Error in DMA TSO parity generator (IPETSO):** When set to 1, parity bit of first valid data generated by the DMA TSO parity generator is (or at PG3 as shown in Transmit data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA TSO parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA TSO parity generator is enabled.
8	0h RW	**Insert Parity Error in DMA DTX Control word parity generator (IPEDDC):** When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA DTX Control word parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA DTX Control word parity generator is enabled.
7	0h RW	**Insert Parity Error in MTL Rx FIFO read control parity generator (IPEMRF):** When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Receive data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is enabled.
6	0h RW	**Insert Parity Error in MTL Tx Status parity generator (IPEMTS):** When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Tx Status parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Tx Status parity generator is enabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Insert Parity Error in MTL checksum parity generator (IPEMC):** When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL checksum parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL checksum parity generator is enabled.
4	0h RW	**Insert Parity Error in Interface Data parity generator (IPEID):** When set to 1, parity bit of first valid input data generated by the Interface data parity generator (or at PG1 as shown in Transmit data path parity protection diagram) is flipped. Following are the input data bus on which parity bits are generated based on configuration selected In AHB Config, hrdata_i In AXI config, rdata_m_i In DMA Config, mdc_rdata_i In MTL Config, ati_data_i Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in Interface Data parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in Interface Data parity generator is enabled.
3:2	0h RO	**Reserved**

14.20.1.367MTL_TXQ0_OPERATION_MODE — Offset 50200D00h

The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	50200D00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Reserved - 2'b10: Enabled - 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

14.20.1.368MTL_TXQ0_UNDERFLOW — Offset 50200D04h

The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	50200D04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

14.20.1.369MTL_TXQ0_DEBUG — Offset 50200D08h

The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	50200D08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

14.20.1.370MTL_TXQ0_ETS_STATUS — Offset 50200D14h

The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	50200D14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

14.20.1.371MTL_TXQ0_QUANTUM_WEIGHT — Offset 50200D18h

The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	50200D18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Quantum or Weights (ISCQW):** When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.

14.20.1.372MTL_Q0_INTERRUPT_CONTROL_STATUS — Offset 50200D2Ch

This register contains the interrupt enable and status bits for the queue 0 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50200D2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

14.20.1.373MTL_RXQ0_OPERATION_MODE — Offset 50200D30h

The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	50200D30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

14.20.1.374MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT — Offset 50200D34h

The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	50200D34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

14.20.1.375MTL_RXQ0_DEBUG — Offset 50200D38h

The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	50200D38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

14.20.1.376MTL_RXQ0_CONTROL — Offset 50200D3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	50200D3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

14.20.1.377MTL_TXQ1_OPERATION_MODE — Offset 50200D40h

The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	50200D40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

14.20.1.378MTL_TXQ1_UNDERFLOW — Offset 50200D44h

The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.379MTL_TXQ1_DEBUG — Offset 50200D48h

The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.380MTL_TXQ1_ETS_CONTROL — Offset 50200D50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	50200D50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

14.20.1.381MTL_TXQ1_ETS_STATUS — Offset 50200D54h

The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	50200D54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

14.20.1.382MTL_TXQ1_QUANTUM_WEIGHT — Offset 50200D58h

The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	50200D58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

14.20.1.383MTL_TXQ1_SENDSLOPECREDIT — Offset 50200D5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	50200D5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

14.20.1.384MTL_TXQ1_HICREDIT — Offset 50200D60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	50200D60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

14.20.1.385MTL_TXQ1_LOCREDIT — Offset 50200D64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	50200D64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

14.20.1.386MTL_Q1_INTERRUPT_CONTROL_STATUS — Offset 50200D6Ch

This register contains the interrupt enable and status bits for the queue 1 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.387MTL_RXQ1_OPERATION_MODE — Offset 50200D70h

The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.388MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT — Offset 50200D74h

The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.389MTL_RXQ1_DEBUG — Offset 50200D78h

The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.390MTL_RXQ1_CONTROL — Offset 50200D7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.391MTL_TXQ2_OPERATION_MODE — Offset 50200D80h

The Queue 2 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50200D40h.

14.20.1.392MTL_TXQ2_UNDERFLOW — Offset 50200D84h

The Queue 2 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.393MTL_TXQ2_DEBUG — Offset 50200D88h

The Queue 2 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.394MTL_TXQ2_ETS_CONTROL — Offset 50200D90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50200D50h.

14.20.1.395MTL_TXQ2_ETS_STATUS — Offset 50200D94h

The Queue 2 ETS Status register provides the average traffic transmitted in Queue 2.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50200D54h.

14.20.1.396MTL_TXQ2_QUANTUM_WEIGHT — Offset 50200D98h

The Queue 2 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 2.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50200D58h.

14.20.1.397MTL_TXQ2_SENDSLOPECREDIT — Offset 50200D9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50200D5Ch.

14.20.1.398MTL_TXQ2_HICREDIT — Offset 50200DA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50200D60h.

14.20.1.399MTL_TXQ2_LOCREDIT — Offset 50200DA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50200D64h.

14.20.1.400MTL_Q2_INTERRUPT_CONTROL_STATUS — Offset 50200DACh

This register contains the interrupt enable and status bits for the queue 2 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.401MTL_RXQ2_OPERATION_MODE — Offset 50200DB0h

The Queue 2 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.402MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT — Offset 50200DB4h

The Queue 2 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.403MTL_RXQ2_DEBUG — Offset 50200DB8h

The Queue 2 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.404MTL_RXQ2_CONTROL — Offset 50200DBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.405MTL_TXQ3_OPERATION_MODE — Offset 50200DC0h

The Queue 3 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50200D40h.

14.20.1.406MTL_TXQ3_UNDERFLOW — Offset 50200DC4h

The Queue 3 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.407MTL_TXQ3_DEBUG — Offset 50200DC8h

The Queue 3 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.408MTL_TXQ3_ETS_CONTROL — Offset 50200DD0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50200D50h.

14.20.1.409MTL_TXQ3_ETS_STATUS — Offset 50200DD4h

The Queue 3 ETS Status register provides the average traffic transmitted in Queue 3.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50200D54h.

14.20.1.410MTL_TXQ3_QUANTUM_WEIGHT — Offset 50200DD8h

The Queue 3 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 3.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50200D58h.

14.20.1.411MTL_TXQ3_SENDSLOPECREDIT — Offset 50200DDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50200D5Ch.

14.20.1.412MTL_TXQ3_HICREDIT — Offset 50200DE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50200D60h.

14.20.1.413MTL_TXQ3_LOCREDIT — Offset 50200DE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50200D64h.

14.20.1.414MTL_Q3_INTERRUPT_CONTROL_STATUS — Offset 50200DECh

This register contains the interrupt enable and status bits for the queue 3 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.415MTL_RXQ3_OPERATION_MODE — Offset 50200DF0h

The Queue 3 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.416MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT — Offset 50200DF4h

The Queue 3 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.417MTL_RXQ3_DEBUG — Offset 50200DF8h

The Queue 3 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.418MTL_RXQ3_CONTROL — Offset 50200DFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.419MTL_TXQ4_OPERATION_MODE — Offset 50200E00h

The Queue 4 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50200D40h.

14.20.1.420MTL_TXQ4_UNDERFLOW — Offset 50200E04h

The Queue 4 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.421MTL_TXQ4_DEBUG — Offset 50200E08h

The Queue 4 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.422MTL_TXQ4_ETS_CONTROL — Offset 50200E10h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50200D50h.

14.20.1.423MTL_TXQ4_ETS_STATUS — Offset 50200E14h

The Queue 4 ETS Status register provides the average traffic transmitted in Queue 4.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50200D54h.

14.20.1.424MTL_TXQ4_QUANTUM_WEIGHT — Offset 50200E18h

The Queue 4 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 4.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50200D58h.

14.20.1.425MTL_TXQ4_SENDSLOPECREDIT — Offset 50200E1Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50200D5Ch.

14.20.1.426MTL_TXQ4_HICREDIT — Offset 50200E20h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50200D60h.

14.20.1.427MTL_TXQ4_LOCREDIT — Offset 50200E24h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50200D64h.

14.20.1.428MTL_Q4_INTERRUPT_CONTROL_STATUS — Offset 50200E2Ch

This register contains the interrupt enable and status bits for the queue 4 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.429MTL_RXQ4_OPERATION_MODE — Offset 50200E30h

The Queue 4 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.430MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT — Offset 50200E34h

The Queue 4 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.431MTL_RXQ4_DEBUG — Offset 50200E38h

The Queue 4 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.432MTL_RXQ4_CONTROL — Offset 50200E3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.433MTL_TXQ5_OPERATION_MODE — Offset 50200E40h

The Queue 5 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50200D40h.

14.20.1.434MTL_TXQ5_UNDERFLOW — Offset 50200E44h

The Queue 5 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.435MTL_TXQ5_DEBUG — Offset 50200E48h

The Queue 5 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.436MTL_TXQ5_ETS_CONTROL — Offset 50200E50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50200D50h.

14.20.1.437MTL_TXQ5_ETS_STATUS — Offset 50200E54h

The Queue 5 ETS Status register provides the average traffic transmitted in Queue 5.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50200D54h.

14.20.1.438MTL_TXQ5_QUANTUM_WEIGHT — Offset 50200E58h

The Queue 5 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 5.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50200D58h.

14.20.1.439MTL_TXQ5_SENDSLOPECREDIT — Offset 50200E5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50200D5Ch.

14.20.1.440MTL_TXQ5_HICREDIT — Offset 50200E60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50200D60h.

14.20.1.441MTL_TXQ5_LOCREDIT — Offset 50200E64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50200D64h.

14.20.1.442MTL_Q5_INTERRUPT_CONTROL_STATUS — Offset 50200E6Ch

This register contains the interrupt enable and status bits for the queue 5 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.443MTL_RXQ5_OPERATION_MODE — Offset 50200E70h

The Queue 5 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.444MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT — Offset 50200E74h

The Queue 5 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.445MTL_RXQ5_DEBUG — Offset 50200E78h

The Queue 5 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.446MTL_RXQ5_CONTROL — Offset 50200E7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.447MTL_TXQ6_OPERATION_MODE — Offset 50200E80h

The Queue 6 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50200D40h.

14.20.1.448MTL_TXQ6_UNDERFLOW — Offset 50200E84h

The Queue 6 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.449MTL_TXQ6_DEBUG — Offset 50200E88h

The Queue 6 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.450MTL_TXQ6_ETS_CONTROL — Offset 50200E90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50200D50h.

14.20.1.451MTL_TXQ6_ETS_STATUS — Offset 50200E94h

The Queue 6 ETS Status register provides the average traffic transmitted in Queue 6.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50200D54h.

14.20.1.452MTL_TXQ6_QUANTUM_WEIGHT — Offset 50200E98h

The Queue 6 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 6.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50200D58h.

14.20.1.453MTL_TXQ6_SENDSLOPECREDIT — Offset 50200E9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50200D5Ch.

14.20.1.454MTL_TXQ6_HICREDIT — Offset 50200EA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50200D60h.

14.20.1.455MTL_TXQ6_LOCREDIT — Offset 50200EA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50200D64h.

14.20.1.456MTL_Q6_INTERRUPT_CONTROL_STATUS — Offset 50200EACh

This register contains the interrupt enable and status bits for the queue 6 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.457MTL_RXQ6_OPERATION_MODE — Offset 50200EB0h

The Queue 6 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.458MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT — Offset 50200EB4h

The Queue 6 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.459MTL_RXQ6_DEBUG — Offset 50200EB8h

The Queue 6 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.460MTL_RXQ6_CONTROL — Offset 50200EBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.461MTL_TXQ7_OPERATION_MODE — Offset 50200EC0h

The Queue 7 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50200D40h.

14.20.1.462MTL_TXQ7_UNDERFLOW — Offset 50200EC4h

The Queue 7 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50200D04h.

14.20.1.463MTL_TXQ7_DEBUG — Offset 50200EC8h

The Queue 7 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50200D08h.

14.20.1.464MTL_TXQ7_ETS_CONTROL — Offset 50200ED0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50200D50h.

14.20.1.465MTL_TXQ7_ETS_STATUS — Offset 50200ED4h

The Queue 7 ETS Status register provides the average traffic transmitted in Queue 7.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50200D54h.

14.20.1.466MTL_TXQ7_QUANTUM_WEIGHT — Offset 50200ED8h

The Queue 7 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 7.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50200D58h.

14.20.1.467MTL_TXQ7_SENDSLOPECREDIT — Offset 50200EDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50200D5Ch.

14.20.1.468MTL_TXQ7_HICREDIT — Offset 50200EE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50200D60h.

14.20.1.469MTL_TXQ7_LOCREDIT — Offset 50200EE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50200D64h.

14.20.1.470MTL_Q7_INTERRUPT_CONTROL_STATUS — Offset 50200EECh

This register contains the interrupt enable and status bits for the queue 7 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50200D2Ch.

14.20.1.471MTL_RXQ7_OPERATION_MODE — Offset 50200EF0h

The Queue 7 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50200D30h.

14.20.1.472MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT — Offset 50200EF4h

The Queue 7 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50200D34h.

14.20.1.473MTL_RXQ7_DEBUG — Offset 50200EF8h

The Queue 7 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50200D38h.

14.20.1.474MTL_RXQ7_CONTROL — Offset 50200EFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50200D3Ch.

14.20.1.475DMA_MODE — Offset 50201000h

The Bus Mode register establishes the bus operating modes for the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50201000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**Rx DMA's Maximum Number of Descriptors to be fetched in a burst (RNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2
21:20	0h RW	**Tx DMA's Maximum Number of Descriptors to be fetched in a burst (TNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2
19	0h RW	**Descriptor Cache Enable (DCHE):** When set enables prefetching of descriptors to the Descriptor Cache. When reset descriptor cache feature is disabled. 0x0 (DISABLE): Descriptor Cache Support is disabled. 0x1 (ENABLE): Descriptor Cache Support is enabled.
18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Interrupt Mode (INTM):** This field defines the interrupt mode of GbE Controller. The behavior of the following outputs changes depending on the following settings: - sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) - sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) - sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. - 00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. - 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 11: Reserved 0x0 (MODE0): See above description. 0x1 (MODE1): See above description. 0x2 (MODE2): See above description. 0x3 (RSVD): Reserved.
15:11	0h RO	**Reserved**
10	0h RW	**Reserved**
9	0h RO	**Reserved**
8	0h RW	**Descriptor Posted Write (DSPW):** When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. 0x0 (DISABLE): Descriptor Posted Write is disabled. 0x1 (ENABLE): Descriptor Posted Write is enabled.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:2	0h RW	**Transmit Arbitration Algorithm (TAA):** This field is used to select the arbitration algorithm for the Transmit side when multiple Tx DMAs are selected. 0x0 (FP): Fixed priority (Channel 0 has the lowest priority and the last channel has the highest priority). 0x1 (WSP): Weighted Strict Priority (WSP). 0x2 (WRR): Weighted Round-Robin (WRR). 0x3 (RSVD): Reserved (for 3'b011 to 3'b111).
1	0h RO	**Reserved**
0	0h RW	**Software Reset (SWR):** When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all GbE Controller clock domains. Before reprogramming any GbE Controller register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Software Reset is disabled. 0x1 (ENABLE): Software Reset is enabled.

14.20.1.476DMA_SYSBUS_MODE — Offset 50201004h

The System Bus mode register controls the behavior of the AHB or AXI master. It mainly controls burst splitting and number of outstanding requests.

Type	Size	Offset	Default
MMIO	32 bit	50201004h	01010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Low Power Interface (LPI) (EN_LPI):** When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. 0x0 (DISABLE): Low Power Interface (LPI) is disabled. 0x1 (ENABLE): Low Power Interface (LPI) is enabled.
30	0h RW	**Unlock on Magic Packet or Remote Wake-Up Packet (LPI_XIT_PKT):** When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. 0x0 (DISABLE): Unlock on Magic Packet or Remote Wake-Up Packet is disabled. 0x1 (ENABLE): Unlock on Magic Packet or Remote Wake-Up Packet is enabled.
29:28	0h RO	**Reserved**
27:24	1h RW	**AXI Maximum Write Outstanding Request Limit (WR_OSR_LMT):** This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1
23:20	0h RO	**Reserved**
19:16	1h RW	**AXI Maximum Read Outstanding Request Limit (RD_OSR_LMT):** This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1
15:14	0h RO	**Reserved**
13	0h RW	**1 KB Boundary Crossing Enable for the EQOS-AXI Master (ONEKBBE):** When set, the burst transfers performed by the EQOS-AXI master do not cross 1 KB boundary. When reset, the burst transfers performed by the EQOS-AXI master do not cross 4 KB boundary. 0x0 (DISABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is disabled. 0x1 (ENABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is enabled.
12	0h RW	**Address-Aligned Beats (AAL):** When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. 0x0 (DISABLE): Address-Aligned Beats is disabled. 0x1 (ENABLE): Address-Aligned Beats is enabled.
11	0h RW	**Enhanced Address Mode Enable. (EAME):** When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. 0x0 (DISABLE): Enhanced Address Mode is disabled. 0x1 (ENABLE): Enhanced Address Mode is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Automatic AXI LPI enable (AALE):** When set to 1, enables the AXI master to enter into LPI state when there is no activity in the GbE Controller for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. 0x0 (DISABLE): Automatic AXI LPI is disabled. 0x1 (ENABLE): Automatic AXI LPI is enabled.
9:8	0h RO	**Reserved**
7	0h RW	**AXI Burst Length 256 (BLEN256):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 256 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 256.
6	0h RW	**AXI Burst Length 128 (BLEN128):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 128 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 128.
5	0h RW	**AXI Burst Length 64 (BLEN64):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 64 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 64.
4	0h RW	**AXI Burst Length 32 (BLEN32):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 32 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 32.
3	0h RW	**AXI Burst Length 16 (BLEN16):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 16.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**AXI Burst Length 8 (BLEN8):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 8.
1	0h RW	**AXI Burst Length 4 (BLEN4):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 4.
0	0h RW	**FB:** Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. - Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field - Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. 0x0 (DISABLE): Fixed Burst Length is disabled. 0x1 (ENABLE): Fixed Burst Length is enabled.

14.20.1.477DMA_INTERRUPT_STATUS — Offset 50201008h

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50201008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO	**MAC Interrupt Status (MACIS):** This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MAC Interrupt Status not detected. 0x1 (ACTIVE): MAC Interrupt Status detected.
16	0h RO	**MTL Interrupt Status (MTLIS):** This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Interrupt Status not detected. 0x1 (ACTIVE): MTL Interrupt Status detected.
15:8	0h RO	**Reserved**
7	0h RO	**DMA Channel 7 Interrupt Status (DC7IS):** This bit indicates an interrupt event in DMA Channel 7. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 7 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 7 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 7 Interrupt Status detected.
6	0h RO	**DMA Channel 6 Interrupt Status (DC6IS):** This bit indicates an interrupt event in DMA Channel 6. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 6 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 6 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 6 Interrupt Status detected.
5	0h RO	**DMA Channel 5 Interrupt Status (DC5IS):** This bit indicates an interrupt event in DMA Channel 5. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 5 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 5 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 5 Interrupt Status detected.
4	0h RO	**DMA Channel 4 Interrupt Status (DC4IS):** This bit indicates an interrupt event in DMA Channel 4. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 4 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 4 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 4 Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**DMA Channel 3 Interrupt Status (DC3IS):** This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 3 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 3 Interrupt Status detected.
2	0h RO	**DMA Channel 2 Interrupt Status (DC2IS):** This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 2 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 2 Interrupt Status detected.
1	0h RO	**DMA Channel 1 Interrupt Status (DC1IS):** This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 1 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 1 Interrupt Status detected.
0	0h RO	**DMA Channel 0 Interrupt Status (DC0IS):** This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 0 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 0 Interrupt Status detected.

14.20.1.478DMA_DEBUG_STATUS0 — Offset 5020100Ch

The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose.

Type	Size	Offset	Default
MMIO	32 bit	5020100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 2 Transmit Process State (TPS2):** This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 2 Receive Process State (RPS2):** This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 1 Transmit Process State (TPS1):** This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO	**DMA Channel 1 Receive Process State (RPS1):** This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
15:12	0h RO	**DMA Channel 0 Transmit Process State (TPS0):** This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
11:8	0h RO	**DMA Channel 0 Receive Process State (RPS0):** This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:2	0h RO	**Reserved**
1	0h RO	**AXI Master Read Channel Status (AXRHSTS):** When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. 0x0 (INACTIVE): AXI Master Read Channel Status not detected. 0x1 (ACTIVE): AXI Master Read Channel Status detected.
0	0h RO	**AXI Master Write Channel (AXWHSTS):** When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. 0x0 (INACTIVE): AXI Master Write Channel or AHB Master Status not detected. 0x1 (ACTIVE): AXI Master Write Channel or AHB Master Status detected.

14.20.1.479DMA_DEBUG_STATUS1 — Offset 50201010h

The Debug Status1 register gives the Receive and Transmit process status for DMA Channel 3-Channel 6.

Type	Size	Offset	Default
MMIO	32 bit	50201010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 6 Transmit Process State (TPS6):** This field indicates the Tx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 6 Receive Process State (RPS6):** This field indicates the Rx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 5 Transmit Process State (TPS5):** This field indicates the Tx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO	**DMA Channel 5 Receive Process State (RPS5):** This field indicates the Rx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
15:12	0h RO	**DMA Channel 4 Transmit Process State (TPS4):** This field indicates the Tx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO	**DMA Channel 4 Receive Process State (RPS4):** This field indicates the Rx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:4	0h RO	**DMA Channel 3 Transmit Process State (TPS3):** This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 3 Receive Process State (RPS3):** This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

14.20.1.480DMA_DEBUG_STATUS2 — Offset 50201014h

The Debug Status Register 2 gives the Receive and Transmit process status for DMA Channel 7.

Type	Size	Offset	Default
MMIO	32 bit	502050201014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	0h RO	**DMA Channel 7 Transmit Process State (TPS7):** This field indicates the Tx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 7 Receive Process State (RPS7):** This field indicates the Rx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

14.20.1.481AXI4_TX_AR_ACE_CONTROL — Offset 50201020h

This register is used to control the AXI4 Cache Coherency Signals for read transactions by all the Transmit DMA channels. The following signals of the AXI4 interface are driven with different values as programmed for corresponding type (descriptor, buffer1, buffer2) of access. - arcache_m_o[3:0] - ardomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	50201020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:20	0h RW	**Transmit DMA First Packet Buffer or TSO Header Domain Control (THD):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO Header data.
19:16	0h RW	**Transmit DMA First Packet Buffer or TSO Header Cache Control (THC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO Header data.
15:14	0h RO	**Reserved**
13:12	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Domain Control (TED):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO payload data.
11:8	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Cache Control (TEC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO payload data.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Read Descriptor Domain Control (TDRD):** This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the Descriptor.
3:0	0h RW	**Transmit DMA Read Descriptor Cache Control (TDRC):** This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor.

14.20.1.482AXI4_RX_AW_ACE_CONTROL — Offset 50201024h

This register is used to control the AXI4 Cache Coherency Signals for write transactions by all the Receive DMA channels. The following signals of the AXI4 interface are driven with different values as programmed for corresponding type (descriptor, buffer1, buffer2) of access. - awcache_m_o[3:0] - awdomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	50201024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Receive DMA Buffer Domain Control (RDD):** This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
27:24	0h RW	**Receive DMA Buffer Cache Control (RDC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
23:22	0h RO	**Reserved**
21:20	0h RW	**Receive DMA Header Domain Control (RHD):** This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
19:16	0h RW	**Receive DMA Header Cache Control (RHC):** This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Payload Domain Control (RPD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
11:8	0h RW	**Receive DMA Payload Cache Control (RPC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
7:6	0h RO	**Reserved**
5:4	0h RW	**Receive DMA Write Descriptor Domain Control (RDWD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor.
3:0	0h RW	**Receive DMA Write Descriptor Cache Control (RDWC):** This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor.

14.20.1.483AXI4_TXRX_AWAR_ACE_CONTROL — Offset 50201028h

This register is used to control the AXI4 Cache Coherency Signals for Descriptor write transactions by all the TxDMA channels and Descriptor read transactions by all the RxDMA channels. It also controls the values to be driven on awprot_m_o and arprot_m_o.

Type	Size	Offset	Default
MMIO	32 bit	50201028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RW	**DMA Write Protection control (WRP):** This field is used to drive awprot_m_o[2:0] signal on the AXI Write Channel.
19	0h RO	**Reserved**
18:16	0h RW	**DMA Read Protection control (RDP):** This field is used to drive arprot_m_o[2:0] signal during all read requests.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Read Descriptor Domain control (RDRD):** This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor.
11:8	0h RW	**Receive DMA Read Descriptor Cache control (RDRC):** This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Write Descriptor Domain control (TDWD):** This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor.
3:0	0h RW	**Transmit DMA Write Descriptor Cache control (TDWC):** This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor.

14.20.1.484AXI_LPI_ENTRY_INTERVAL — Offset 50201040h

This register is used to control the AXI LPI entry interval.

Type	Size	Offset	Default
MMIO	32 bit	50201040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**LPI Entry Interval (LPIEI):** Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the GbE Controller to enter into the AXI low power state 0 indicates 64 clock cycles

14.20.1.485DMA_TBS_CTRL0 — Offset 50201050h

Type	Size	Offset	Default
MMIO	32 bit	50201050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

14.20.1.486DMA_TBS_CTRL1 — Offset 50201054h

Note: Bit definitions are the same as DMA_TBS_CTRL0, offset 50201050h.

14.20.1.487DMA_TBS_CTRL2 — Offset 50201058h

Note: Bit definitions are the same as DMA_TBS_CTRL0, offset 50201050h.

14.20.1.488DMA_TBS_CTRL3 — Offset 5020105Ch

Note: Bit definitions are the same as DMA_TBS_CTRL0, offset 50201050h.

14.20.1.489DMA_SAFETY_INTERRUPT_STATUS — Offset 50201080h

This register indicates summary (whether error occured in DMA/MTL/MAC and correctable/uncorrectable) of the Automotive Safety related error interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50201080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**MAC Safety Uncorrectable Interrupt Status (MCSIS):** Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC. 0x0 (INACTIVE): MAC Safety Uncorrectable Interrupt Status not detected. 0x1 (ACTIVE): MAC Safety Uncorrectable Interrupt Status detected.
30	0h RO	**Reserved**
29	0h RO	**MTL Safety Uncorrectable error Interrupt Status (MSUIS):** This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Uncorrectable error Interrupt Status detected.
28	0h RO	**MTL Safety Correctable error Interrupt Status (MSCIS):** This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Correctable error Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
27:2	0h RO	**Reserved**
1	0h RO	**DMA ECC Uncorrectable error Interrupt Status (DEUIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**DMA ECC Correctable error Interrupt Status (DECIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Correctable error Interrupt Status detected.

14.20.1.490DMA_ECC_INTERRUPT_ENABLE — Offset 50201084h

This register is used to enable the Automotive Safety related TSO memory ECC error interrupt.

Type	Size	Offset	Default
MMIO	32 bit	50201084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TSO memory Correctable Error Interrupt Enable (TCEIE):** When set, generates an interrupt when a correctable error is detected at the DMA TSO memory interface. It is indicated in the TCES bit of DMA_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): TSO memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): TSO memory Correctable Error Interrupt is enabled.

14.20.1.491DMA_ECC_INTERRUPT_STATUS — Offset 50201088h

This register indicates the Automotive Safety related TSO memory ECC error interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	50201088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**DMA TSO memory Uncorrectable Error status (TUES):** When set, indicates that an uncorrectable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Uncorrectable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Uncorrectable Error status detected.
1	0h RW	**DMA TSO memory Address Mismatch status (TAMS):** This bit when set indicates that address mismatch is found for address bus of DMA TSO memory. 0x0 (INACTIVE): DMA TSO memory Address Mismatch status not detected. 0x1 (ACTIVE): DMA TSO memory Address Mismatch status detected.
0	0h RW	**DMA TSO memory Correctable Error status (TCES):** This bit when set indicates that correctable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Correctable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Correctable Error status detected.

14.20.1.492DMA_CH0_CONTROL — Offset 50201100h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	50201100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

14.20.1.493DMA_CH0_TX_CONTROL — Offset 50201104h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	50201104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

14.20.1.494DMA_CH0_RX_CONTROL — Offset 50201108h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	50201108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

14.20.1.495DMA_CH0_TXDESC_LIST_HADDRESS — Offset 50201110h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	50201110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

14.20.1.496DMA_CH0_TXDESC_LIST_ADDRESS — Offset 50201114h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	50201114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.1.497DMA_CH0_RXDESC_LIST_HADDRESS — Offset 50201118h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	50201118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

14.20.1.498DMA_CH0_RXDESC_LIST_ADDRESS — Offset 5020111Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	5020111Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.1.499DMA_CH0_TXDESC_TAIL_POINTER — Offset 50201120h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	50201120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.1.500DMA_CH0_RXDESC_TAIL_POINTER — Offset 50201128h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	50201128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.1.501DMA_CH0_TXDESC_RING_LENGTH — Offset 5020112Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	5020112Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

14.20.1.502DMA_CH0_RXDESC_RING_LENGTH — Offset 50201130h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	50201130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

14.20.1.503DMA_CH0_INTERRUPT_ENABLE — Offset 50201134h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	50201134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

14.20.1.504DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50201138h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	50201138h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

14.20.1.505DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS — Offset 5020113Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	5020113Ch	000007C0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

14.20.1.506DMA_CH0_CURRENT_APP_TXDESC — Offset 50201144h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50201144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

14.20.1.507DMA_CH0_CURRENT_APP_RXDESC — Offset 5020114Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	5020114Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

14.20.1.508DMA_CH0_CURRENT_APP_TXBUFFER_H — Offset 50201150h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50201150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

14.20.1.509DMA_CH0_CURRENT_APP_TXBUFFER — Offset 50201154h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50201154h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

14.20.1.510DMA_CH0_CURRENT_APP_RXBUFFER_H — Offset 50201158h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50201158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

14.20.1.511DMA_CH0_CURRENT_APP_RXBUFFER — Offset 5020115Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	5020115Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

14.20.1.512DMA_CH0_STATUS — Offset 50201160h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	50201160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

14.20.1.513DMA_CH0_MISS_FRAME_CNT — Offset 50201164h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	50201164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

14.20.1.514DMA_CH0_RXP_ACCEPT_CNT — Offset 50201168h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	50201168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

14.20.1.515DMA_CH0_RX_ERI_CNT — Offset 5020116Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	5020116Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

14.20.1.516DMA_CH1_CONTROL — Offset 50201180h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 50201100h.

14.20.1.517DMA_CH1_TX_CONTROL — Offset 50201184h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.518DMA_CH1_RX_CONTROL — Offset 50201188h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.519DMA_CH1_TXDESC_LIST_HADDRESS — Offset 50201190h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.520DMA_CH1_TXDESC_LIST_ADDRESS — Offset 50201194h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.521DMA_CH1_RXDESC_LIST_HADDRESS — Offset 50201198h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.522DMA_CH1_RXDESC_LIST_ADDRESS — Offset 5020119Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.523DMA_CH1_TXDESC_TAIL_POINTER — Offset 502011A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.524DMA_CH1_RXDESC_TAIL_POINTER — Offset 502011A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.525DMA_CH1_TXDESC_RING_LENGTH — Offset 502011ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.526DMA_CH1_RXDESC_RING_LENGTH — Offset 502011B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.527DMA_CH1_INTERRUPT_ENABLE — Offset 502011B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.528DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502011B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.529DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS — Offset 502011BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.530DMA_CH1_CURRENT_APP_TXDESC — Offset 502011C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.531DMA_CH1_CURRENT_APP_RXDESC — Offset 502011CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.532DMA_CH1_CURRENT_APP_TXBUFFER_H — Offset 502011D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.533DMA_CH1_CURRENT_APP_TXBUFFER — Offset 502011D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.534DMA_CH1_CURRENT_APP_RXBUFFER_H — Offset 502011D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.535DMA_CH1_CURRENT_APP_RXBUFFER — Offset 502011DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.536DMA_CH1_STATUS — Offset 502011E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.537DMA_CH1_MISS_FRAME_CNT — Offset 502011E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.538DMA_CH1_RXP_ACCEPT_CNT — Offset 502011E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.539DMA_CH1_RX_ERI_CNT — Offset 502011ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.1.540DMA_CH2_CONTROL — Offset 50201200h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 50201100h.

14.20.1.541DMA_CH2_TX_CONTROL — Offset 50201204h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.542DMA_CH2_RX_CONTROL — Offset 50201208h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.543DMA_CH2_TXDESC_LIST_HADDRESS — Offset 50201210h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.544DMA_CH2_TXDESC_LIST_ADDRESS — Offset 50201214h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.545DMA_CH2_RXDESC_LIST_HADDRESS — Offset 50201218h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.546DMA_CH2_RXDESC_LIST_ADDRESS — Offset 5020121Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.547DMA_CH2_TXDESC_TAIL_POINTER — Offset 50201220h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.548DMA_CH2_RXDESC_TAIL_POINTER — Offset 50201228h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.549DMA_CH2_TXDESC_RING_LENGTH — Offset 5020122Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.550DMA_CH2_RXDESC_RING_LENGTH — Offset 50201230h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.551DMA_CH2_INTERRUPT_ENABLE — Offset 50201234h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.552DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50201238h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.553DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS — Offset 5020123Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.554DMA_CH2_CURRENT_APP_TXDESC — Offset 50201244h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.555DMA_CH2_CURRENT_APP_RXDESC — Offset 5020124Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.556DMA_CH2_CURRENT_APP_TXBUFFER_H — Offset 50201250h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.557DMA_CH2_CURRENT_APP_TXBUFFER — Offset 50201254h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.558DMA_CH2_CURRENT_APP_RXBUFFER_H — Offset 50201258h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.559DMA_CH2_CURRENT_APP_RXBUFFER — Offset 5020125Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.560DMA_CH2_STATUS — Offset 50201260h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.561DMA_CH2_MISS_FRAME_CNT — Offset 50201264h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.562DMA_CH2_RXP_ACCEPT_CNT — Offset 50201268h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.563DMA_CH2_RX_ERI_CNT — Offset 5020126Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.1.564DMA_CH3_CONTROL — Offset 50201280h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 50201100h.

14.20.1.565DMA_CH3_TX_CONTROL — Offset 50201284h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.566DMA_CH3_RX_CONTROL — Offset 50201288h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.567DMA_CH3_TXDESC_LIST_HADDRESS — Offset 50201290h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.568DMA_CH3_TXDESC_LIST_ADDRESS — Offset 50201294h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the

corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.569DMA_CH3_RXDESC_LIST_HADDRESS — Offset 50201298h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.570DMA_CH3_RXDESC_LIST_ADDRESS — Offset 5020129Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.571DMA_CH3_TXDESC_TAIL_POINTER — Offset 502012A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.572DMA_CH3_RXDESC_TAIL_POINTER — Offset 502012A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.573DMA_CH3_TXDESC_RING_LENGTH — Offset 502012ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.574DMA_CH3_RXDESC_RING_LENGTH — Offset 502012B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.575DMA_CH3_INTERRUPT_ENABLE — Offset 502012B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.576DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502012B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.577DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS — Offset 502012BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.578DMA_CH3_CURRENT_APP_TXDESC — Offset 502012C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.579DMA_CH3_CURRENT_APP_RXDESC — Offset 502012CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.580DMA_CH3_CURRENT_APP_TXBUFFER_H — Offset 502012D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.581DMA_CH3_CURRENT_APP_TXBUFFER — Offset 502012D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.582DMA_CH3_CURRENT_APP_RXBUFFER_H — Offset 502012D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.583DMA_CH3_CURRENT_APP_RXBUFFER — Offset 502012DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.584DMA_CH3_STATUS — Offset 502012E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.585DMA_CH3_MISS_FRAME_CNT — Offset 502012E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.586DMA_CH3_RXP_ACCEPT_CNT — Offset 502012E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.587DMA_CH3_RX_ERI_CNT — Offset 502012ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.1.588DMA_CH4_CONTROL — Offset 50201300h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	50201300h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

14.20.1.589DMA_CH4_TX_CONTROL — Offset 50201304h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.590DMA_CH4_RX_CONTROL — Offset 50201308h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.591DMA_CH4_TXDESC_LIST_HADDRESS — Offset 50201310h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.592DMA_CH4_TXDESC_LIST_ADDRESS — Offset 50201314h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.593DMA_CH4_RXDESC_LIST_HADDRESS — Offset 50201318h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.594DMA_CH4_RXDESC_LIST_ADDRESS — Offset 5020131Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped,

this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.595DMA_CH4_TXDESC_TAIL_POINTER — Offset 50201320h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.596DMA_CH4_RXDESC_TAIL_POINTER — Offset 50201328h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.597DMA_CH4_TXDESC_RING_LENGTH — Offset 5020132Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.598DMA_CH4_RXDESC_RING_LENGTH — Offset 50201330h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.599DMA_CH4_INTERRUPT_ENABLE — Offset 50201334h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.600DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50201338h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.601DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS — Offset 5020133Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.602DMA_CH4_CURRENT_APP_TXDESC — Offset 50201344h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.603DMA_CH4_CURRENT_APP_RXDESC — Offset 5020134Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.604DMA_CH4_CURRENT_APP_TXBUFFER_H — Offset 50201350h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.605DMA_CH4_CURRENT_APP_TXBUFFER — Offset 50201354h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.606DMA_CH4_CURRENT_APP_RXBUFFER_H — Offset 50201358h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.607DMA_CH4_CURRENT_APP_RXBUFFER — Offset 5020135Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.608DMA_CH4_STATUS — Offset 50201360h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.609DMA_CH4_MISS_FRAME_CNT — Offset 50201364h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.610DMA_CH4_RXP_ACCEPT_CNT — Offset 50201368h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.611DMA_CH4_RX_ERI_CNT — Offset 5020136Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.1.612DMA_CH5_CONTROL — Offset 50201380h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 50201300h.

14.20.1.613DMA_CH5_TX_CONTROL — Offset 50201384h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.614DMA_CH5_RX_CONTROL — Offset 50201388h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.615DMA_CH5_TXDESC_LIST_HADDRESS — Offset 50201390h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.616DMA_CH5_TXDESC_LIST_ADDRESS — Offset 50201394h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.617DMA_CH5_RXDESC_LIST_HADDRESS — Offset 50201398h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.618DMA_CH5_RXDESC_LIST_ADDRESS — Offset 5020139Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.619DMA_CH5_TXDESC_TAIL_POINTER — Offset 502013A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.620DMA_CH5_RXDESC_TAIL_POINTER — Offset 502013A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.621DMA_CH5_TXDESC_RING_LENGTH — Offset 502013ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.622DMA_CH5_RXDESC_RING_LENGTH — Offset 502013B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.623DMA_CH5_INTERRUPT_ENABLE — Offset 502013B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.624DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502013B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.625DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS — Offset 502013BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.626DMA_CH5_CURRENT_APP_TXDESC — Offset 502013C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.627DMA_CH5_CURRENT_APP_RXDESC — Offset 502013CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.628DMA_CH5_CURRENT_APP_TXBUFFER_H — Offset 502013D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.629DMA_CH5_CURRENT_APP_TXBUFFER — Offset 502013D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.630DMA_CH5_CURRENT_APP_RXBUFFER_H — Offset 502013D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.631DMA_CH5_CURRENT_APP_RXBUFFER — Offset 502013DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.632DMA_CH5_STATUS — Offset 502013E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.633DMA_CH5_MISS_FRAME_CNT — Offset 502013E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.634DMA_CH5_RXP_ACCEPT_CNT — Offset 502013E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.635DMA_CH5_RX_ERI_CNT — Offset 502013ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.1.636DMA_CH6_CONTROL — Offset 50201400h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 50201300h.

14.20.1.637DMA_CH6_TX_CONTROL — Offset 50201404h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.638DMA_CH6_RX_CONTROL — Offset 50201408h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.639DMA_CH6_TXDESC_LIST_HADDRESS — Offset 50201410h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.640DMA_CH6_TXDESC_LIST_ADDRESS — Offset 50201414h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.641DMA_CH6_RXDESC_LIST_HADDRESS — Offset 50201418h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.642DMA_CH6_RXDESC_LIST_ADDRESS — Offset 5020141Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.643DMA_CH6_TXDESC_TAIL_POINTER — Offset 50201420h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.644DMA_CH6_RXDESC_TAIL_POINTER — Offset 50201428h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.645DMA_CH6_TXDESC_RING_LENGTH — Offset 5020142Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.646DMA_CH6_RXDESC_RING_LENGTH — Offset 50201430h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.647DMA_CH6_INTERRUPT_ENABLE — Offset 50201434h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.648DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50201438h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.649DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS — Offset 5020143Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.650DMA_CH6_CURRENT_APP_TXDESC — Offset 50201444h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.651DMA_CH6_CURRENT_APP_RXDESC — Offset 5020144Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.652DMA_CH6_CURRENT_APP_TXBUFFER_H — Offset 50201450h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.653DMA_CH6_CURRENT_APP_TXBUFFER — Offset 50201454h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.654DMA_CH6_CURRENT_APP_RXBUFFER_H — Offset 50201458h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.655DMA_CH6_CURRENT_APP_RXBUFFER — Offset 5020145Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.656DMA_CH6_STATUS — Offset 50201460h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.657DMA_CH6_MISS_FRAME_CNT — Offset 50201464h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.658DMA_CH6_RXP_ACCEPT_CNT — Offset 50201468h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.659DMA_CH6_RX_ERI_CNT — Offset 5020146Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.1.660DMA_CH7_CONTROL — Offset 50201480h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 50201300h.

14.20.1.661DMA_CH7_TX_CONTROL — Offset 50201484h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50201104h.

14.20.1.662DMA_CH7_RX_CONTROL — Offset 50201488h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50201108h.

14.20.1.663DMA_CH7_TXDESC_LIST_HADDRESS — Offset 50201490h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50201110h.

14.20.1.664DMA_CH7_TXDESC_LIST_ADDRESS — Offset 50201494h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50201114h.

14.20.1.665DMA_CH7_RXDESC_LIST_HADDRESS — Offset 50201498h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50201118h.

14.20.1.666DMA_CH7_RXDESC_LIST_ADDRESS — Offset 5020149Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5020111Ch.

14.20.1.667DMA_CH7_TXDESC_TAIL_POINTER — Offset 502014A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50201120h.

14.20.1.668DMA_CH7_RXDESC_TAIL_POINTER — Offset 502014A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50201128h.

14.20.1.669DMA_CH7_TXDESC_RING_LENGTH — Offset 502014ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5020112Ch.

14.20.1.670DMA_CH7_RXDESC_RING_LENGTH — Offset 502014B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50201130h.

14.20.1.671DMA_CH7_INTERRUPT_ENABLE — Offset 502014B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50201134h.

14.20.1.672DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502014B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50201138h.

14.20.1.673DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS — Offset 502014BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5020113Ch.

14.20.1.674DMA_CH7_CURRENT_APP_TXDESC — Offset 502014C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50201144h.

14.20.1.675DMA_CH7_CURRENT_APP_RXDESC — Offset 502014CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5020114Ch.

14.20.1.676DMA_CH7_CURRENT_APP_TXBUFFER_H — Offset 502014D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50201150h.

14.20.1.677DMA_CH7_CURRENT_APP_TXBUFFER — Offset 502014D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50201154h.

14.20.1.678DMA_CH7_CURRENT_APP_RXBUFFER_H — Offset 502014D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50201158h.

14.20.1.679DMA_CH7_CURRENT_APP_RXBUFFER — Offset 502014DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5020115Ch.

14.20.1.680DMA_CH7_STATUS — Offset 502014E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50201160h.

14.20.1.681DMA_CH7_MISS_FRAME_CNT — Offset 502014E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50201164h.

14.20.1.682DMA_CH7_RXP_ACCEPT_CNT — Offset 502014E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50201168h.

14.20.1.683DMA_CH7_RX_ERI_CNT — Offset 502014ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5020116Ch.

14.20.2 GbE_0 TSN MISC Registers Summary

Table 14-45. Summary of GbE_0 TSN MISC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50210000h	4	DMA ControlChannel0 (DMA_CTL_CH0)	00000000h
50210004h	4	DMA ControlChannel1 (DMA_CTL_CH1)	00000000h
50210008h	4	DMA ControlChannel2 (DMA_CTL_CH2)	00000000h
5021000Ch	4	DMA ControlChannel3 (DMA_CTL_CH3)	00000000h
50210010h	4	DMA ControlChannel4 (DMA_CTL_CH4)	00000000h
50210014h	4	DMA ControlChannel5 (DMA_CTL_CH5)	00000000h
50210018h	4	DMA ControlChannel6 (DMA_CTL_CH6)	00000000h
5021001Ch	4	DMA ControlChannel7 (DMA_CTL_CH7)	00000000h
50210020h	4	DMA ControlChannel8 (DMA_CTL_CH8)	00000000h
50210024h	4	DMA ControlChannel9 (DMA_CTL_CH9)	00000000h
50210028h	4	DMA ControlChannel10 (DMA_CTL_CH10)	00000000h
5021002Ch	4	DMA ControlChannel11 (DMA_CTL_CH11)	00000000h
50210030h	4	DMA ControlChannel12 (DMA_CTL_CH12)	00000000h
50210034h	4	DMA ControlChannel13 (DMA_CTL_CH13)	00000000h
50210038h	4	DMA ControlChannel14 (DMA_CTL_CH14)	00000000h
5021003Ch	4	DMA ControlChannel15 (DMA_CTL_CH15)	00000000h
50210100h	4	DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0)	00000000h
50210104h	4	DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1)	00000000h
50210108h	4	DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2)	00000000h
5021010Ch	4	DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3)	00000000h
50210110h	4	DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4)	00000000h
50210114h	4	DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5)	00000000h
50210118h	4	DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6)	00000000h
5021011Ch	4	DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7)	00000000h
50210120h	4	DMA CH8 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH8)	00000000h
50210124h	4	DMA CH9 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH9)	00000000h
50210128h	4	DMA CH10 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH10)	00000000h
5021012Ch	4	DMA CH11 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH11)	00000000h
50210130h	4	DMA CH12 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH12)	00000000h
50210134h	4	DMA CH13 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH13)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50210138h	4	DMA CH14 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH14)	00000000h
5021013Ch	4	DMA CH15 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH15)	00000000h
50210200h	4	DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0)	00000000h
50210204h	4	DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1)	00000000h
50210208h	4	DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2)	00000000h
5021020Ch	4	DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3)	00000000h
50210210h	4	DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4)	00000000h
50210214h	4	DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5)	00000000h
50210218h	4	DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6)	00000000h
5021021Ch	4	DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7)	00000000h
50210220h	4	DMA CH8 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH8)	00000000h
50210224h	4	DMA CH9 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH9)	00000000h
50210228h	4	DMA CH10 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH10)	00000000h
5021022Ch	4	DMA CH11 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH11)	00000000h
50210230h	4	DMA CH12 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH12)	00000000h
50210234h	4	DMA CH13 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH13)	00000000h
50210238h	4	DMA CH14 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH14)	00000000h
5021023Ch	4	DMA CH15 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH15)	00000000h
50210410h	4	D0i3 Control (D0I3C)	00000008h
50210414h	4	Clock Gating And Soft Rset (CSGR)	00000000h
50210418h	4	GBE DMA Interrupt Enable (DMA_INT_EN)	0000FFFFh
50210500h	4	DLL Configuration (DLL_CFG)	00000010h

14.20.2.1 DMA ControlChannel0 (DMA_CTL_CH0) — Offset 50210000h

DMA Control register channel0.

Type	Size	Offset	Default
MMIO	32 bit	50210000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface. When RT_Disable fuse is active, this bit is internally tied to '0'.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel0 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel0 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.2 DMA ControlChannel1 (DMA_CTL_CH1) — Offset 50210004h

DMA Control register channel1.

Type	Size	Offset	Default
MMIO	32 bit	50210004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel1 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel1 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.3 DMA ControlChannel2 (DMA_CTL_CH2) — Offset 50210008h

DMA Control register channel2.

Type	Size	Offset	Default
MMIO	32 bit	50210008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel2 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel2 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.4 DMA ControlChannel3 (DMA_CTL_CH3) — Offset 5021000Ch

DMA Control register channel3.

Type	Size	Offset	Default
MMIO	32 bit	5021000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel3 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel3 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.5 DMA ControlChannel4 (DMA_CTL_CH4) — Offset 50210010h

DMA Control register channel4.

Type	Size	Offset	Default
MMIO	32 bit	50210010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel4 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel4 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.6 DMA ControlChannel5 (DMA_CTL_CH5) — Offset 50210014h

DMA Control register channel5.

Type	Size	Offset	Default
MMIO	32 bit	50210014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel5 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel5 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.7 DMA ControlChannel6 (DMA_CTL_CH6) — Offset 50210018h

DMA Control register channel6.

Type	Size	Offset	Default
MMIO	32 bit	50210018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel6 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel6 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.8 DMA ControlChannel7 (DMA_CTL_CH7) — Offset 5021001Ch

DMA Control register channel7.

Type	Size	Offset	Default
MMIO	32 bit	5021001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel7 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel7 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.9 DMA ControlChannel8 (DMA_CTL_CH8) — Offset 50210020h

DMA Control register channel8.

Type	Size	Offset	Default
MMIO	32 bit	50210020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel8 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel8 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.10 DMA ControlChannel9 (DMA_CTL_CH9) — Offset 50210024h

DMA Control register channel9.

Type	Size	Offset	Default
MMIO	32 bit	50210024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel9 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel9 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.11 DMA ControlChannel10 (DMA_CTL_CH10) — Offset 50210028h

DMA Control register channel10.

Type	Size	Offset	Default
MMIO	32 bit	50210028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel10 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel10 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.12 DMA ControlChannel11 (DMA_CTL_CH11) — Offset 5021002Ch

DMA Control register channel11.

Type	Size	Offset	Default
MMIO	32 bit	5021002Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel11 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel11 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.13 DMA ControlChannel12 (DMA_CTL_CH12) — Offset 50210030h

DMA Control register channel12.

Type	Size	Offset	Default
MMIO	32 bit	50210030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel12 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel12 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.14 DMA ControlChannel13 (DMA_CTL_CH13) — Offset 50210034h

DMA Control register channel13.

Type	Size	Offset	Default
MMIO	32 bit	50210034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel13 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel13 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.15 DMA ControlChannel14 (DMA_CTL_CH14) — Offset 50210038h

DMA Control register channel14.

Type	Size	Offset	Default
MMIO	32 bit	50210038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channe14 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel14 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.16 DMA ControlChannel15 (DMA_CTL_CH15) — Offset 5021003Ch

DMA Control register channel15.

Type	Size	Offset	Default
MMIO	32 bit	5021003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel15 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel15 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.2.17 DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0) — Offset 50210100h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	50210100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

14.20.2.18 DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1) — Offset 50210104h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.19 DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2) — Offset 50210108h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.20 DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3) — Offset 5021010Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.21 DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4) — Offset 50210110h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.22 DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5) — Offset 50210114h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.23 DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6) — Offset 50210118h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.24 DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7) — Offset 5021011Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.25 DMA CH8 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH8) — Offset 50210120h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.26 DMA CH9 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH9) — Offset 50210124h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.27 DMA CH10 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH10) — Offset 50210128h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.28 DMA CH11 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH11) — Offset 5021012Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.29 DMA CH12 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH12) — Offset 50210130h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.30 DMA CH13 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH13) — Offset 50210134h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.31 DMA CH14 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH14) — Offset 50210138h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.32 DMA CH15 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH15) — Offset 5021013Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.33 DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0) — Offset 50210200h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.34 DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1) — Offset 50210204h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.35 DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2) — Offset 50210208h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.36 DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3) — Offset 5021020Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.37 DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4) — Offset 50210210h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.38 DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5) — Offset 50210214h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.39 DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6) — Offset 50210218h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.40 DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7) — Offset 5021021Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.41 DMA CH8 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH8) — Offset 50210220h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.42 DMA CH9 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH9) — Offset 50210224h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.43 DMA CH10 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH10) — Offset 50210228h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.44 DMA CH11 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH11) — Offset 5021022Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.45 DMA CH12 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH12) — Offset 50210230h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.46 DMA CH13 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH13) — Offset 50210234h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.47 DMA CH14 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH14) — Offset 50210238h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.48 DMA CH15 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH15) — Offset 5021023Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50210100h.

14.20.2.49 D0i3 Control (D0I3C) — Offset 50210410h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are To be done) The description below also includes the type of access expected for the ISH FW for each configuration bit: 1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost. 2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit. 3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW. 4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear). The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following: 1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1. 2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied. 3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	50210410h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RW/1C	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

14.20.2.50 Clock Gating And Soft Rset (CSGR) — Offset 50210414h

This register is used to clock gate or soft reset an IP by Host/Remote Host.

Type	Size	Offset	Default
MMIO	32 bit	50210414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Nable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reest (SR):** Setting this bit to 1 resets the IP.

14.20.2.51 GBE DMA Interrupt Enable (DMA_INT_EN) — Offset 50210418h

This register is used to program the interrupt enables for GBE Tx/Rx Interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50210418h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW	**Rx Ch 7 Interrupt Enable (INT_EN_RX_CH7):** When Bit 15 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 7. When Bit 15 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 7.
14	1h RW	**Rx Ch 6 Interrupt Enable (INT_EN_RX_CH6):** When Bit 14 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 6. When Bit 14 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 6.
13	1h RW	**Rx Ch 5 Interrupt Enable (INT_EN_RX_CH5):** When Bit 13 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 5. When Bit 13 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 5.
12	1h RW	**Rx Ch 4 Interrupt Enable (INT_EN_RX_CH4):** When Bit 12 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 4. When Bit 12 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 4.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Rx Ch 3 Interrupt Enable (INT_EN_RX_CH3):** When Bit 11 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 3. When Bit 11 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 3.
10	1h RW	**Rx Ch 2 Interrupt Enable (INT_EN_RX_CH2):** When Bit 10 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 2. When Bit 10 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 2.
9	1h RW	**Rx Ch 1 Interrupt Enable (INT_EN_RX_CH1):** When Bit 9 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 1. When Bit 9 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 1.
8	1h RW	**Rx Ch 0 Interrupt Enable (INT_EN_RX_CH0):** When Bit 8 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 0. When Bit 8 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 0.
7	1h RW	**Tx Ch 7 Interrupt Enable (INT_EN_TX_CH7):** When Bit 7 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 7. When Bit 7 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 7.
6	1h RW	**Tx Ch 6 Interrupt Enable (INT_EN_TX_CH6):** When Bit 6 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 6. When Bit 6 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 6.
5	1h RW	**Tx Ch 5 Interrupt Enable (INT_EN_TX_CH5):** When Bit 5 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 5. When Bit 5 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 5.
4	1h RW	**Tx Ch 4 Interrupt Enable (INT_EN_TX_CH4):** When Bit 4 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 4. When Bit 4 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 4.
3	1h RW	**Tx Ch 3 Interrupt Enable (INT_EN_TX_CH3):** When Bit 3 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 3. When Bit 3 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 3.
2	1h RW	**Tx Ch 2 Interrupt Enable (INT_EN_TX_CH2):** When Bit 2 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 2. When Bit 2 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 2.
1	1h RW	**Tx Ch 1 Interrupt Enable (INT_EN_TX_CH1):** When Bit 1 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 1. When Bit 1 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 1.
0	1h RW	**Tx Ch 0 Interrupt Enable (INT_EN_TX_CH0):** When Bit 0 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 0. When Bit 0 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 0.

14.20.2.52 DLL Configuration (DLL_CFG) — Offset 50210500h

This register is used to configure DLL slave delay elements, to bypass the DLL slave and to read to DLL master lock live status.

Type	Size	Offset	Default
MMIO	32 bit	50210500h	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DLL Master Lock (DLL_LOCK):** When 1 indicated DLL master is locked.
6	0h RW	**DLL Slave Bypass (DLL_BYPASS):** Setting this bit to 1 bypass the DLL slave.
5:0	10h RW	**DLL Slave Delay Elements (TX_DELAY):** Configure total number of delay elements in DLL slave. Resolution is 125ps.

14.20.3 GbE_1 TSN Registers Summary

Table 14-46. Summary of GbE_1 TSN Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220000h	4	MAC_CONFIGURATION	00000000h
50220004h	4	MAC_EXT_CONFIGURATION	00000000h
50220008h	4	MAC_PACKET_FILTER	00000000h
5022000Ch	4	MAC_WATCHDOG_TIMEOUT	00000000h
50220010h	4	MAC_HASH_TABLE_REG0	00000000h
50220014h	4	MAC_HASH_TABLE_REG1	00000000h
50220050h	4	MAC_VLAN_TAG_CTRL	00000000h
50220054h	4	MAC_VLAN_TAG_DATA	00000000h
50220058h	4	MAC_VLAN_HASH_TABLE	00000000h
50220060h	4	MAC_VLAN_INCL	00000000h
50220064h	4	MAC_INNER_VLAN_INCL	00000000h
50220070h	4	MAC_Q0_TX_FLOW_CTRL	00000000h
50220074h	4	MAC_Q1_TX_FLOW_CTRL	00000000h
50220078h	4	MAC_Q2_TX_FLOW_CTRL	00000000h
5022007Ch	4	MAC_Q3_TX_FLOW_CTRL	00000000h
50220080h	4	MAC_Q4_TX_FLOW_CTRL	00000000h
50220084h	4	MAC_Q5_TX_FLOW_CTRL	00000000h
50220088h	4	MAC_Q6_TX_FLOW_CTRL	00000000h
5022008Ch	4	MAC_Q7_TX_FLOW_CTRL	00000000h
50220090h	4	MAC_RX_FLOW_CTRL	00000000h
50220094h	4	MAC_RXQ_CTRL4	00000000h
50220098h	4	MAC_TXQ_PRTY_MAP0	00000000h
5022009Ch	4	MAC_TXQ_PRTY_MAP1	00000000h
502200A0h	4	MAC_RXQ_CTRL0	00000000h
502200A4h	4	MAC_RXQ_CTRL1	00000000h
502200A8h	4	MAC_RXQ_CTRL2	00000000h
502200ACh	4	MAC_RXQ_CTRL3	00000000h
502200B0h	4	MAC_INTERRUPT_STATUS	00000000h
502200B4h	4	MAC_INTERRUPT_ENABLE	00000000h
502200B8h	4	MAC_RX_TX_STATUS	00000000h
502200C0h	4	MAC_PMT_CONTROL_STATUS	00000000h
502200C4h	4	MAC_RWK_PACKET_FILTER	00000000h
502200D0h	4	MAC_LPI_CONTROL_STATUS	00000000h
502200D4h	4	MAC_LPI_TIMERS_CONTROL	03E80000h
502200D8h	4	MAC_LPI_ENTRY_TIMER	00000000h
502200DCh	4	MAC_1US_TIC_COUNTER	00000063h
502200F8h	4	MAC_PHYIF_CONTROL_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220110h	4	MAC_VERSION	00005152h
50220114h	4	MAC_DEBUG	00000000h
5022011Ch	4	MAC_HW_FEATURE0	0EFD73F7h
50220120h	4	MAC_HW_FEATURE1	119F7A69h
50220124h	4	MAC_HW_FEATURE2	225D71C7h
50220128h	4	MAC_HW_FEATURE3	2C395632h
50220140h	4	MAC_DPP_FSM_INTERRUPT_STATUS	00000000h
50220148h	4	MAC_FSM_CONTROL	00000000h
5022014Ch	4	MAC_FSM_ACT_TIMER	00000000h
50220150h	4	SNPS_SCS_REG1	00000000h
50220200h	4	MAC_MDIO_ADDRESS	00000000h
50220204h	4	MAC_MDIO_DATA	00000000h
50220208h	4	MAC_GPIO_CONTROL	00000000h
5022020Ch	4	MAC_GPIO_STATUS	00000000h
50220210h	4	MAC_ARP_ADDRESS	00000000h
50220230h	4	MAC_CSR_SW_CTRL	00000000h
50220234h	4	MAC_FPE_CTRL_STS	00000000h
50220238h	4	MAC_EXT_CFG1	00000002h
50220240h	4	MAC_PRESN_TIME_NS	00000000h
50220244h	4	MAC_PRESN_TIME_UPDT	00000000h
50220300h	4	MAC_ADDRESS0_HIGH	8000FFFFh
50220304h	4	MAC_ADDRESS0_LOW	FFFFFFFFh
50220308h	4	MAC_ADDRESS1_HIGH	0000FFFFh
5022030Ch	4	MAC_ADDRESS1_LOW	FFFFFFFFh
50220310h	4	MAC_ADDRESS2_HIGH	0000FFFFh
50220314h	4	MAC_ADDRESS2_LOW	FFFFFFFFh
50220318h	4	MAC_ADDRESS3_HIGH	0000FFFFh
5022031Ch	4	MAC_ADDRESS3_LOW	FFFFFFFFh
50220320h	4	MAC_ADDRESS4_HIGH	0000FFFFh
50220324h	4	MAC_ADDRESS4_LOW	FFFFFFFFh
50220328h	4	MAC_ADDRESS5_HIGH	0000FFFFh
5022032Ch	4	MAC_ADDRESS5_LOW	FFFFFFFFh
50220330h	4	MAC_ADDRESS6_HIGH	0000FFFFh
50220334h	4	MAC_ADDRESS6_LOW	FFFFFFFFh
50220338h	4	MAC_ADDRESS7_HIGH	0000FFFFh
5022033Ch	4	MAC_ADDRESS7_LOW	FFFFFFFFh
50220340h	4	MAC_ADDRESS8_HIGH	0000FFFFh
50220344h	4	MAC_ADDRESS8_LOW	FFFFFFFFh
50220348h	4	MAC_ADDRESS9_HIGH	0000FFFFh
5022034Ch	4	MAC_ADDRESS9_LOW	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220350h	4	MAC_ADDRESS10_HIGH	0000FFFFh
50220354h	4	MAC_ADDRESS10_LOW	FFFFFFFFh
50220358h	4	MAC_ADDRESS11_HIGH	0000FFFFh
5022035Ch	4	MAC_ADDRESS11_LOW	FFFFFFFFh
50220360h	4	MAC_ADDRESS12_HIGH	0000FFFFh
50220364h	4	MAC_ADDRESS12_LOW	FFFFFFFFh
50220368h	4	MAC_ADDRESS13_HIGH	0000FFFFh
5022036Ch	4	MAC_ADDRESS13_LOW	FFFFFFFFh
50220370h	4	MAC_ADDRESS14_HIGH	0000FFFFh
50220374h	4	MAC_ADDRESS14_LOW	FFFFFFFFh
50220378h	4	MAC_ADDRESS15_HIGH	0000FFFFh
5022037Ch	4	MAC_ADDRESS15_LOW	FFFFFFFFh
50220380h	4	MAC_ADDRESS16_HIGH	0000FFFFh
50220384h	4	MAC_ADDRESS16_LOW	FFFFFFFFh
50220388h	4	MAC_ADDRESS17_HIGH	0000FFFFh
5022038Ch	4	MAC_ADDRESS17_LOW	FFFFFFFFh
50220390h	4	MAC_ADDRESS18_HIGH	0000FFFFh
50220394h	4	MAC_ADDRESS18_LOW	FFFFFFFFh
50220398h	4	MAC_ADDRESS19_HIGH	0000FFFFh
5022039Ch	4	MAC_ADDRESS19_LOW	FFFFFFFFh
502203A0h	4	MAC_ADDRESS20_HIGH	0000FFFFh
502203A4h	4	MAC_ADDRESS20_LOW	FFFFFFFFh
502203A8h	4	MAC_ADDRESS21_HIGH	0000FFFFh
502203ACh	4	MAC_ADDRESS21_LOW	FFFFFFFFh
502203B0h	4	MAC_ADDRESS22_HIGH	0000FFFFh
502203B4h	4	MAC_ADDRESS22_LOW	FFFFFFFFh
502203B8h	4	MAC_ADDRESS23_HIGH	0000FFFFh
502203BCh	4	MAC_ADDRESS23_LOW	FFFFFFFFh
502203C0h	4	MAC_ADDRESS24_HIGH	0000FFFFh
502203C4h	4	MAC_ADDRESS24_LOW	FFFFFFFFh
502203C8h	4	MAC_ADDRESS25_HIGH	0000FFFFh
502203CCh	4	MAC_ADDRESS25_LOW	FFFFFFFFh
502203D0h	4	MAC_ADDRESS26_HIGH	0000FFFFh
502203D4h	4	MAC_ADDRESS26_LOW	FFFFFFFFh
502203D8h	4	MAC_ADDRESS27_HIGH	0000FFFFh
502203DCh	4	MAC_ADDRESS27_LOW	FFFFFFFFh
502203E0h	4	MAC_ADDRESS28_HIGH	0000FFFFh
502203E4h	4	MAC_ADDRESS28_LOW	FFFFFFFFh
502203E8h	4	MAC_ADDRESS29_HIGH	0000FFFFh
502203ECh	4	MAC_ADDRESS29_LOW	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502203F0h	4	MAC_ADDRESS30_HIGH	0000FFFFh
502203F4h	4	MAC_ADDRESS30_LOW	FFFFFFFFh
502203F8h	4	MAC_ADDRESS31_HIGH	0000FFFFh
502203FCh	4	MAC_ADDRESS31_LOW	FFFFFFFFh
50220400h	4	MAC_ADDRESS32_HIGH	0000FFFFh
50220404h	4	MAC_ADDRESS32_LOW	FFFFFFFFh
50220408h	4	MAC_ADDRESS33_HIGH	0000FFFFh
5022040Ch	4	MAC_ADDRESS33_LOW	FFFFFFFFh
50220410h	4	MAC_ADDRESS34_HIGH	0000FFFFh
50220414h	4	MAC_ADDRESS34_LOW	FFFFFFFFh
50220418h	4	MAC_ADDRESS35_HIGH	0000FFFFh
5022041Ch	4	MAC_ADDRESS35_LOW	FFFFFFFFh
50220420h	4	MAC_ADDRESS36_HIGH	0000FFFFh
50220424h	4	MAC_ADDRESS36_LOW	FFFFFFFFh
50220428h	4	MAC_ADDRESS37_HIGH	0000FFFFh
5022042Ch	4	MAC_ADDRESS37_LOW	FFFFFFFFh
50220430h	4	MAC_ADDRESS38_HIGH	0000FFFFh
50220434h	4	MAC_ADDRESS38_LOW	FFFFFFFFh
50220438h	4	MAC_ADDRESS39_HIGH	0000FFFFh
5022043Ch	4	MAC_ADDRESS39_LOW	FFFFFFFFh
50220440h	4	MAC_ADDRESS40_HIGH	0000FFFFh
50220444h	4	MAC_ADDRESS40_LOW	FFFFFFFFh
50220448h	4	MAC_ADDRESS41_HIGH	0000FFFFh
5022044Ch	4	MAC_ADDRESS41_LOW	FFFFFFFFh
50220450h	4	MAC_ADDRESS42_HIGH	0000FFFFh
50220454h	4	MAC_ADDRESS42_LOW	FFFFFFFFh
50220458h	4	MAC_ADDRESS43_HIGH	0000FFFFh
5022045Ch	4	MAC_ADDRESS43_LOW	FFFFFFFFh
50220460h	4	MAC_ADDRESS44_HIGH	0000FFFFh
50220464h	4	MAC_ADDRESS44_LOW	FFFFFFFFh
50220468h	4	MAC_ADDRESS45_HIGH	0000FFFFh
5022046Ch	4	MAC_ADDRESS45_LOW	FFFFFFFFh
50220470h	4	MAC_ADDRESS46_HIGH	0000FFFFh
50220474h	4	MAC_ADDRESS46_LOW	FFFFFFFFh
50220478h	4	MAC_ADDRESS47_HIGH	0000FFFFh
5022047Ch	4	MAC_ADDRESS47_LOW	FFFFFFFFh
50220480h	4	MAC_ADDRESS48_HIGH	0000FFFFh
50220484h	4	MAC_ADDRESS48_LOW	FFFFFFFFh
50220488h	4	MAC_ADDRESS49_HIGH	0000FFFFh
5022048Ch	4	MAC_ADDRESS49_LOW	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220490h	4	MAC_ADDRESS50_HIGH	0000FFFFh
50220494h	4	MAC_ADDRESS50_LOW	FFFFFFFFh
50220498h	4	MAC_ADDRESS51_HIGH	0000FFFFh
5022049Ch	4	MAC_ADDRESS51_LOW	FFFFFFFFh
502204A0h	4	MAC_ADDRESS52_HIGH	0000FFFFh
502204A4h	4	MAC_ADDRESS52_LOW	FFFFFFFFh
502204A8h	4	MAC_ADDRESS53_HIGH	0000FFFFh
502204ACh	4	MAC_ADDRESS53_LOW	FFFFFFFFh
502204B0h	4	MAC_ADDRESS54_HIGH	0000FFFFh
502204B4h	4	MAC_ADDRESS54_LOW	FFFFFFFFh
502204B8h	4	MAC_ADDRESS55_HIGH	0000FFFFh
502204BCh	4	MAC_ADDRESS55_LOW	FFFFFFFFh
502204C0h	4	MAC_ADDRESS56_HIGH	0000FFFFh
502204C4h	4	MAC_ADDRESS56_LOW	FFFFFFFFh
502204C8h	4	MAC_ADDRESS57_HIGH	0000FFFFh
502204CCh	4	MAC_ADDRESS57_LOW	FFFFFFFFh
502204D0h	4	MAC_ADDRESS58_HIGH	0000FFFFh
502204D4h	4	MAC_ADDRESS58_LOW	FFFFFFFFh
502204D8h	4	MAC_ADDRESS59_HIGH	0000FFFFh
502204DCh	4	MAC_ADDRESS59_LOW	FFFFFFFFh
502204E0h	4	MAC_ADDRESS60_HIGH	0000FFFFh
502204E4h	4	MAC_ADDRESS60_LOW	FFFFFFFFh
502204E8h	4	MAC_ADDRESS61_HIGH	0000FFFFh
502204ECh	4	MAC_ADDRESS61_LOW	FFFFFFFFh
502204F0h	4	MAC_ADDRESS62_HIGH	0000FFFFh
502204F4h	4	MAC_ADDRESS62_LOW	FFFFFFFFh
502204F8h	4	MAC_ADDRESS63_HIGH	0000FFFFh
502204FCh	4	MAC_ADDRESS63_LOW	FFFFFFFFh
50220700h	4	MMC_CONTROL	00000000h
50220704h	4	MMC_RX_INTERRUPT	00000000h
50220708h	4	MMC_TX_INTERRUPT	00000000h
5022070Ch	4	MMC_RX_INTERRUPT_MASK	00000000h
50220710h	4	MMC_TX_INTERRUPT_MASK	00000000h
50220714h	4	TX_OCTET_COUNT_GOOD_BAD	00000000h
50220718h	4	TX_PACKET_COUNT_GOOD_BAD	00000000h
5022071Ch	4	TX_BROADCAST_PACKETS_GOOD	00000000h
50220720h	4	TX_MULTICAST_PACKETS_GOOD	00000000h
50220724h	4	TX_64OCTETS_PACKETS_GOOD_BAD	00000000h
50220728h	4	TX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
5022072Ch	4	TX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220730h	4	TX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h
50220734h	4	TX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
50220738h	4	TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
5022073Ch	4	TX_UNICAST_PACKETS_GOOD_BAD	00000000h
50220740h	4	TX_MULTICAST_PACKETS_GOOD_BAD	00000000h
50220744h	4	TX_BROADCAST_PACKETS_GOOD_BAD	00000000h
50220748h	4	TX_UNDERFLOW_ERROR_PACKETS	00000000h
5022074Ch	4	TX_SINGLE_COLLISION_GOOD_PACKETS	00000000h
50220750h	4	TX_MULTIPLE_COLLISION_GOOD_PACKETS	00000000h
50220754h	4	TX_DEFERRED_PACKETS	00000000h
50220758h	4	TX_LATE_COLLISION_PACKETS	00000000h
5022075Ch	4	TX_EXCESSIVE_COLLISION_PACKETS	00000000h
50220760h	4	TX_CARRIER_ERROR_PACKETS	00000000h
50220764h	4	TX_OCTET_COUNT_GOOD	00000000h
50220768h	4	TX_PACKET_COUNT_GOOD	00000000h
5022076Ch	4	TX_EXCESSIVE_DEFERRAL_ERROR	00000000h
50220770h	4	TX_PAUSE_PACKETS	00000000h
50220774h	4	TX_VLAN_PACKETS_GOOD	00000000h
50220778h	4	TX_OSIZE_PACKETS_GOOD	00000000h
50220780h	4	RX_PACKETS_COUNT_GOOD_BAD	00000000h
50220784h	4	RX_OCTET_COUNT_GOOD_BAD	00000000h
50220788h	4	RX_OCTET_COUNT_GOOD	00000000h
5022078Ch	4	RX_BROADCAST_PACKETS_GOOD	00000000h
50220790h	4	RX_MULTICAST_PACKETS_GOOD	00000000h
50220794h	4	RX_CRC_ERROR_PACKETS	00000000h
50220798h	4	RX_ALIGNMENT_ERROR_PACKETS	00000000h
5022079Ch	4	RX_RUNT_ERROR_PACKETS	00000000h
502207A0h	4	RX_JABBER_ERROR_PACKETS	00000000h
502207A4h	4	RX_UNDERSIZE_PACKETS_GOOD	00000000h
502207A8h	4	RX_OVERSIZE_PACKETS_GOOD	00000000h
502207ACh	4	RX_64OCTETS_PACKETS_GOOD_BAD	00000000h
502207B0h	4	RX_65TO127OCTETS_PACKETS_GOOD_BAD	00000000h
502207B4h	4	RX_128TO255OCTETS_PACKETS_GOOD_BAD	00000000h
502207B8h	4	RX_256TO511OCTETS_PACKETS_GOOD_BAD	00000000h
502207BCh	4	RX_512TO1023OCTETS_PACKETS_GOOD_BAD	00000000h
502207C0h	4	RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	00000000h
502207C4h	4	RX_UNICAST_PACKETS_GOOD	00000000h
502207C8h	4	RX_LENGTH_ERROR_PACKETS	00000000h
502207CCh	4	RX_OUT_OF_RANGE_TYPE_PACKETS	00000000h
502207D0h	4	RX_PAUSE_PACKETS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502207D4h	4	RX_FIFO_OVERFLOW_PACKETS	00000000h
502207D8h	4	RX_VLAN_PACKETS_GOOD_BAD	00000000h
502207DCh	4	RX_WATCHDOG_ERROR_PACKETS	00000000h
502207E0h	4	RX_RECEIVE_ERROR_PACKETS	00000000h
502207E4h	4	RX_CONTROL_PACKETS_GOOD	00000000h
502207ECh	4	TX_LPI_USEC_CNTR	00000000h
502207F0h	4	TX_LPI_TRAN_CNTR	00000000h
502207F4h	4	RX_LPI_USEC_CNTR	00000000h
502207F8h	4	RX_LPI_TRAN_CNTR	00000000h
50220800h	4	MMC_IPC_RX_INTERRUPT_MASK	00000000h
50220808h	4	MMC_IPC_RX_INTERRUPT	00000000h
50220810h	4	RXIPV4_GOOD_PACKETS	00000000h
50220814h	4	RXIPV4_HEADER_ERROR_PACKETS	00000000h
50220818h	4	RXIPV4_NO_PAYLOAD_PACKETS	00000000h
5022081Ch	4	RXIPV4_FRAGMENTED_PACKETS	00000000h
50220820h	4	RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS	00000000h
50220824h	4	RXIPV6_GOOD_PACKETS	00000000h
50220828h	4	RXIPV6_HEADER_ERROR_PACKETS	00000000h
5022082Ch	4	RXIPV6_NO_PAYLOAD_PACKETS	00000000h
50220830h	4	RXUDP_GOOD_PACKETS	00000000h
50220834h	4	RXUDP_ERROR_PACKETS	00000000h
50220838h	4	RXTCP_GOOD_PACKETS	00000000h
5022083Ch	4	RXTCP_ERROR_PACKETS	00000000h
50220840h	4	RXICMP_GOOD_PACKETS	00000000h
50220844h	4	RXICMP_ERROR_PACKETS	00000000h
50220850h	4	RXIPV4_GOOD_OCTETS	00000000h
50220854h	4	RXIPV4_HEADER_ERROR_OCTETS	00000000h
50220858h	4	RXIPV4_NO_PAYLOAD_OCTETS	00000000h
5022085Ch	4	RXIPV4_FRAGMENTED_OCTETS	00000000h
50220860h	4	RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	00000000h
50220864h	4	RXIPV6_GOOD_OCTETS	00000000h
50220868h	4	RXIPV6_HEADER_ERROR_OCTETS	00000000h
5022086Ch	4	RXIPV6_NO_PAYLOAD_OCTETS	00000000h
50220870h	4	RXUDP_GOOD_OCTETS	00000000h
50220874h	4	RXUDP_ERROR_OCTETS	00000000h
50220878h	4	RXTCP_GOOD_OCTETS	00000000h
5022087Ch	4	RXTCP_ERROR_OCTETS	00000000h
50220880h	4	RXICMP_GOOD_OCTETS	00000000h
50220884h	4	RXICMP_ERROR_OCTETS	00000000h
502208A0h	4	MMC_FPE_TX_INTERRUPT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502208A4h	4	MMC_FPE_TX_INTERRUPT_MASK	00000000h
502208A8h	4	MMC_TX_FPE_FRAGMENT_CNTR	00000000h
502208ACh	4	MMC_TX_HOLD_REQ_CNTR	00000000h
502208C0h	4	MMC_FPE_RX_INTERRUPT	00000000h
502208C4h	4	MMC_FPE_RX_INTERRUPT_MASK	00000000h
502208C8h	4	MMC_RX_PACKET_ASSEMBLY_ERR_CNTR	00000000h
502208CCh	4	MMC_RX_PACKET_SMD_ERR_CNTR	00000000h
502208D0h	4	MMC_RX_PACKET_ASSEMBLY_OK_CNTR	00000000h
502208D4h	4	MMC_RX_FPE_FRAGMENT_CNTR	00000000h
50220900h	4	MAC_L3_L4_CONTROL0	00000000h
50220904h	4	MAC_LAYER4_ADDRESS0	00000000h
50220910h	4	MAC_LAYER3_ADDR0_REG0	00000000h
50220914h	4	MAC_LAYER3_ADDR1_REG0	00000000h
50220918h	4	MAC_LAYER3_ADDR2_REG0	00000000h
5022091Ch	4	MAC_LAYER3_ADDR3_REG0	00000000h
50220930h	4	MAC_L3_L4_CONTROL1	00000000h
50220934h	4	MAC_LAYER4_ADDRESS1	00000000h
50220940h	4	MAC_LAYER3_ADDR0_REG1	00000000h
50220944h	4	MAC_LAYER3_ADDR1_REG1	00000000h
50220948h	4	MAC_LAYER3_ADDR2_REG1	00000000h
5022094Ch	4	MAC_LAYER3_ADDR3_REG1	00000000h
50220B00h	4	MAC_TIMESTAMP_CONTROL	00002000h
50220B04h	4	MAC_SUB_SECOND_INCREMENT	00000000h
50220B08h	4	MAC_SYSTEM_TIME_SECONDS	00000000h
50220B0Ch	4	MAC_SYSTEM_TIME_NANOSECONDS	00000000h
50220B10h	4	MAC_SYSTEM_TIME_SECONDS_UPDATE	00000000h
50220B14h	4	MAC_SYSTEM_TIME_NANOSECONDS_UPDATE	00000000h
50220B18h	4	MAC_TIMESTAMP_ADDEND	00000000h
50220B1Ch	4	MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS	00000000h
50220B20h	4	MAC_TIMESTAMP_STATUS	00000000h
50220B30h	4	MAC_TX_TIMESTAMP_STATUS_NANOSECONDS	00000000h
50220B34h	4	MAC_TX_TIMESTAMP_STATUS_SECONDS	00000000h
50220B40h	4	MAC_AUXILIARY_CONTROL	00000000h
50220B48h	4	MAC_AUXILIARY_TIMESTAMP_NANOSECONDS	00000000h
50220B4Ch	4	MAC_AUXILIARY_TIMESTAMP_SECONDS	00000000h
50220B50h	4	MAC_TIMESTAMP_INGRESS_ASYM_CORR	00000000h
50220B54h	4	MAC_TIMESTAMP_EGRESS_ASYM_CORR	00000000h
50220B58h	4	MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND	00000000h
50220B5Ch	4	MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND	00000000h
50220B60h	4	MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220B64h	4	MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC	00000000h
50220B68h	4	MAC_TIMESTAMP_INGRESS_LATENCY	00000000h
50220B6Ch	4	MAC_TIMESTAMP_EGRESS_LATENCY	00000000h
50220B70h	4	MAC_PPS_CONTROL	00000000h
50220B80h	4	MAC_PPS0_TARGET_TIME_SECONDS	00000000h
50220B84h	4	MAC_PPS0_TARGET_TIME_NANOSECONDS	00000000h
50220B88h	4	MAC_PPS0_INTERVAL	00000000h
50220B8Ch	4	MAC_PPS0_WIDTH	00000000h
50220B90h	4	MAC_PPS1_TARGET_TIME_SECONDS	00000000h
50220B94h	4	MAC_PPS1_TARGET_TIME_NANOSECONDS	00000000h
50220B98h	4	MAC_PPS1_INTERVAL	00000000h
50220B9Ch	4	MAC_PPS1_WIDTH	00000000h
50220BC0h	4	MAC_PTO_CONTROL	00000000h
50220BC4h	4	MAC_SOURCE_PORT_IDENTITY0	00000000h
50220BC8h	4	MAC_SOURCE_PORT_IDENTITY1	00000000h
50220BCCh	4	MAC_SOURCE_PORT_IDENTITY2	00000000h
50220BD0h	4	MAC_LOG_MESSAGE_INTERVAL	00000000h
50220C00h	4	MTL_OPERATION_MODE	00000000h
50220C08h	4	MTL_DBG_CTL	00000000h
50220C0Ch	4	MTL_DBG_STS	00000018h
50220C10h	4	MTL_FIFO_DEBUG_DATA	00000000h
50220C20h	4	MTL_INTERRUPT_STATUS	00000000h
50220C30h	4	MTL_RXQ_DMA_MAP0	00000000h
50220C34h	4	MTL_RXQ_DMA_MAP1	00000000h
50220C40h	4	MTL_TBS_CTRL	00000000h
50220C50h	4	MTL_EST_CONTROL	00000000h
50220C58h	4	MTL_EST_STATUS	00000000h
50220C60h	4	MTL_EST_SCH_ERROR	00000000h
50220C64h	4	MTL_EST_FRM_SIZE_ERROR	00000000h
50220C68h	4	MTL_EST_FRM_SIZE_CAPTURE	00000000h
50220C70h	4	MTL_EST_INTR_ENABLE	00000000h
50220C80h	4	MTL_EST_GCL_CONTROL	00000000h
50220C84h	4	MTL_EST_GCL_DATA	00000000h
50220C90h	4	MTL_FPE_CTRL_STS	00000000h
50220C94h	4	MTL_FPE_ADVANCE	00000000h
50220CA0h	4	MTL_RXP_CONTROL_STATUS	80FF00FFh
50220CA4h	4	MTL_RXP_INTERRUPT_CONTROL_STATUS	00000000h
50220CA8h	4	MTL_RXP_DROP_CNT	00000000h
50220CACh	4	MTL_RXP_ERROR_CNT	00000000h
50220CB0h	4	MTL_RXP_INDIRECT_ACC_CONTROL_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220CB4h	4	MTL_RXP_INDIRECT_ACC_DATA	00000000h
50220CC0h	4	MTL_ECC_CONTROL	00000000h
50220CC4h	4	MTL_SAFETY_INTERRUPT_STATUS	00000000h
50220CC8h	4	MTL_ECC_INTERRUPT_ENABLE	00000000h
50220CCCh	4	MTL_ECC_INTERRUPT_STATUS	00000000h
50220CD0h	4	MTL_ECC_ERR_STS_RCTL	00000000h
50220CD4h	4	MTL_ECC_ERR_ADDR_STATUS	00000000h
50220CD8h	4	MTL_ECC_ERR_CNTR_STATUS	00000000h
50220CE0h	4	MTL_DPP_CONTROL	00000000h
50220D00h	4	MTL_TXQ0_OPERATION_MODE	00000000h
50220D04h	4	MTL_TXQ0_UNDERFLOW	00000000h
50220D08h	4	MTL_TXQ0_DEBUG	00000000h
50220D14h	4	MTL_TXQ0_ETS_STATUS	00000000h
50220D18h	4	MTL_TXQ0_QUANTUM_WEIGHT	00000000h
50220D2Ch	4	MTL_Q0_INTERRUPT_CONTROL_STATUS	00000000h
50220D30h	4	MTL_RXQ0_OPERATION_MODE	00000000h
50220D34h	4	MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220D38h	4	MTL_RXQ0_DEBUG	00000000h
50220D3Ch	4	MTL_RXQ0_CONTROL	00000000h
50220D40h	4	MTL_TXQ1_OPERATION_MODE	00000000h
50220D44h	4	MTL_TXQ1_UNDERFLOW	00000000h
50220D48h	4	MTL_TXQ1_DEBUG	00000000h
50220D50h	4	MTL_TXQ1_ETS_CONTROL	00000000h
50220D54h	4	MTL_TXQ1_ETS_STATUS	00000000h
50220D58h	4	MTL_TXQ1_QUANTUM_WEIGHT	00000000h
50220D5Ch	4	MTL_TXQ1_SENDSLOPECREDIT	00000000h
50220D60h	4	MTL_TXQ1_HICREDIT	00000000h
50220D64h	4	MTL_TXQ1_LOCREDIT	00000000h
50220D6Ch	4	MTL_Q1_INTERRUPT_CONTROL_STATUS	00000000h
50220D70h	4	MTL_RXQ1_OPERATION_MODE	00000000h
50220D74h	4	MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220D78h	4	MTL_RXQ1_DEBUG	00000000h
50220D7Ch	4	MTL_RXQ1_CONTROL	00000000h
50220D80h	4	MTL_TXQ2_OPERATION_MODE	00000000h
50220D84h	4	MTL_TXQ2_UNDERFLOW	00000000h
50220D88h	4	MTL_TXQ2_DEBUG	00000000h
50220D90h	4	MTL_TXQ2_ETS_CONTROL	00000000h
50220D94h	4	MTL_TXQ2_ETS_STATUS	00000000h
50220D98h	4	MTL_TXQ2_QUANTUM_WEIGHT	00000000h
50220D9Ch	4	MTL_TXQ2_SENDSLOPECREDIT	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220DA0h	4	MTL_TXQ2_HICREDIT	00000000h
50220DA4h	4	MTL_TXQ2_LOCREDIT	00000000h
50220DACh	4	MTL_Q2_INTERRUPT_CONTROL_STATUS	00000000h
50220DB0h	4	MTL_RXQ2_OPERATION_MODE	00000000h
50220DB4h	4	MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220DB8h	4	MTL_RXQ2_DEBUG	00000000h
50220DBCh	4	MTL_RXQ2_CONTROL	00000000h
50220DC0h	4	MTL_TXQ3_OPERATION_MODE	00000000h
50220DC4h	4	MTL_TXQ3_UNDERFLOW	00000000h
50220DC8h	4	MTL_TXQ3_DEBUG	00000000h
50220DD0h	4	MTL_TXQ3_ETS_CONTROL	00000000h
50220DD4h	4	MTL_TXQ3_ETS_STATUS	00000000h
50220DD8h	4	MTL_TXQ3_QUANTUM_WEIGHT	00000000h
50220DDCh	4	MTL_TXQ3_SENDSLOPECREDIT	00000000h
50220DE0h	4	MTL_TXQ3_HICREDIT	00000000h
50220DE4h	4	MTL_TXQ3_LOCREDIT	00000000h
50220DECh	4	MTL_Q3_INTERRUPT_CONTROL_STATUS	00000000h
50220DF0h	4	MTL_RXQ3_OPERATION_MODE	00000000h
50220DF4h	4	MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220DF8h	4	MTL_RXQ3_DEBUG	00000000h
50220DFCh	4	MTL_RXQ3_CONTROL	00000000h
50220E00h	4	MTL_TXQ4_OPERATION_MODE	00000000h
50220E04h	4	MTL_TXQ4_UNDERFLOW	00000000h
50220E08h	4	MTL_TXQ4_DEBUG	00000000h
50220E10h	4	MTL_TXQ4_ETS_CONTROL	00000000h
50220E14h	4	MTL_TXQ4_ETS_STATUS	00000000h
50220E18h	4	MTL_TXQ4_QUANTUM_WEIGHT	00000000h
50220E1Ch	4	MTL_TXQ4_SENDSLOPECREDIT	00000000h
50220E20h	4	MTL_TXQ4_HICREDIT	00000000h
50220E24h	4	MTL_TXQ4_LOCREDIT	00000000h
50220E2Ch	4	MTL_Q4_INTERRUPT_CONTROL_STATUS	00000000h
50220E30h	4	MTL_RXQ4_OPERATION_MODE	00000000h
50220E34h	4	MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220E38h	4	MTL_RXQ4_DEBUG	00000000h
50220E3Ch	4	MTL_RXQ4_CONTROL	00000000h
50220E40h	4	MTL_TXQ5_OPERATION_MODE	00000000h
50220E44h	4	MTL_TXQ5_UNDERFLOW	00000000h
50220E48h	4	MTL_TXQ5_DEBUG	00000000h
50220E50h	4	MTL_TXQ5_ETS_CONTROL	00000000h
50220E54h	4	MTL_TXQ5_ETS_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50220E58h	4	MTL_TXQ5_QUANTUM_WEIGHT	00000000h
50220E5Ch	4	MTL_TXQ5_SENDSLOPECREDIT	00000000h
50220E60h	4	MTL_TXQ5_HICREDIT	00000000h
50220E64h	4	MTL_TXQ5_LOCREDIT	00000000h
50220E6Ch	4	MTL_Q5_INTERRUPT_CONTROL_STATUS	00000000h
50220E70h	4	MTL_RXQ5_OPERATION_MODE	00000000h
50220E74h	4	MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220E78h	4	MTL_RXQ5_DEBUG	00000000h
50220E7Ch	4	MTL_RXQ5_CONTROL	00000000h
50220E80h	4	MTL_TXQ6_OPERATION_MODE	00000000h
50220E84h	4	MTL_TXQ6_UNDERFLOW	00000000h
50220E88h	4	MTL_TXQ6_DEBUG	00000000h
50220E90h	4	MTL_TXQ6_ETS_CONTROL	00000000h
50220E94h	4	MTL_TXQ6_ETS_STATUS	00000000h
50220E98h	4	MTL_TXQ6_QUANTUM_WEIGHT	00000000h
50220E9Ch	4	MTL_TXQ6_SENDSLOPECREDIT	00000000h
50220EA0h	4	MTL_TXQ6_HICREDIT	00000000h
50220EA4h	4	MTL_TXQ6_LOCREDIT	00000000h
50220EACh	4	MTL_Q6_INTERRUPT_CONTROL_STATUS	00000000h
50220EB0h	4	MTL_RXQ6_OPERATION_MODE	00000000h
50220EB4h	4	MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220EB8h	4	MTL_RXQ6_DEBUG	00000000h
50220EBCh	4	MTL_RXQ6_CONTROL	00000000h
50220EC0h	4	MTL_TXQ7_OPERATION_MODE	00000000h
50220EC4h	4	MTL_TXQ7_UNDERFLOW	00000000h
50220EC8h	4	MTL_TXQ7_DEBUG	00000000h
50220ED0h	4	MTL_TXQ7_ETS_CONTROL	00000000h
50220ED4h	4	MTL_TXQ7_ETS_STATUS	00000000h
50220ED8h	4	MTL_TXQ7_QUANTUM_WEIGHT	00000000h
50220EDCh	4	MTL_TXQ7_SENDSLOPECREDIT	00000000h
50220EE0h	4	MTL_TXQ7_HICREDIT	00000000h
50220EE4h	4	MTL_TXQ7_LOCREDIT	00000000h
50220EECh	4	MTL_Q7_INTERRUPT_CONTROL_STATUS	00000000h
50220EF0h	4	MTL_RXQ7_OPERATION_MODE	00000000h
50220EF4h	4	MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT	00000000h
50220EF8h	4	MTL_RXQ7_DEBUG	00000000h
50220EFCh	4	MTL_RXQ7_CONTROL	00000000h
50221000h	4	DMA_MODE	00000000h
50221004h	4	DMA_SYSBUS_MODE	01010000h
50221008h	4	DMA_INTERRUPT_STATUS	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5022100Ch	4	DMA_DEBUG_STATUS0	00000000h
50221010h	4	DMA_DEBUG_STATUS1	00000000h
50221014h	4	DMA_DEBUG_STATUS2	00000000h
50221020h	4	AXI4_TX_AR_ACE_CONTROL	00000000h
50221024h	4	AXI4_RX_AW_ACE_CONTROL	00000000h
50221028h	4	AXI4_TXRX_AWAR_ACE_CONTROL	00000000h
50221040h	4	AXI_LPI_ENTRY_INTERVAL	00000000h
50221050h	4	DMA_TBS_CTRL0	00000000h
50221054h	4	DMA_TBS_CTRL1	00000000h
50221058h	4	DMA_TBS_CTRL2	00000000h
5022105Ch	4	DMA_TBS_CTRL3	00000000h
50221080h	4	DMA_SAFETY_INTERRUPT_STATUS	00000000h
50221084h	4	DMA_ECC_INTERRUPT_ENABLE	00000000h
50221088h	4	DMA_ECC_INTERRUPT_STATUS	00000000h
50221100h	4	DMA_CH0_CONTROL	00000000h
50221104h	4	DMA_CH0_TX_CONTROL	00000000h
50221108h	4	DMA_CH0_RX_CONTROL	00000000h
50221110h	4	DMA_CH0_TXDESC_LIST_HADDRESS	00000000h
50221114h	4	DMA_CH0_TXDESC_LIST_ADDRESS	00000000h
50221118h	4	DMA_CH0_RXDESC_LIST_HADDRESS	00000000h
5022111Ch	4	DMA_CH0_RXDESC_LIST_ADDRESS	00000000h
50221120h	4	DMA_CH0_TXDESC_TAIL_POINTER	00000000h
50221128h	4	DMA_CH0_RXDESC_TAIL_POINTER	00000000h
5022112Ch	4	DMA_CH0_TXDESC_RING_LENGTH	00000000h
50221130h	4	DMA_CH0_RXDESC_RING_LENGTH	00000000h
50221134h	4	DMA_CH0_INTERRUPT_ENABLE	00000000h
50221138h	4	DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5022113Ch	4	DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50221144h	4	DMA_CH0_CURRENT_APP_TXDESC	00000000h
5022114Ch	4	DMA_CH0_CURRENT_APP_RXDESC	00000000h
50221150h	4	DMA_CH0_CURRENT_APP_TXBUFFER_H	00000000h
50221154h	4	DMA_CH0_CURRENT_APP_TXBUFFER	00000000h
50221158h	4	DMA_CH0_CURRENT_APP_RXBUFFER_H	00000000h
5022115Ch	4	DMA_CH0_CURRENT_APP_RXBUFFER	00000000h
50221160h	4	DMA_CH0_STATUS	00000000h
50221164h	4	DMA_CH0_MISS_FRAME_CNT	00000000h
50221168h	4	DMA_CH0_RXP_ACCEPT_CNT	00000000h
5022116Ch	4	DMA_CH0_RX_ERI_CNT	00000000h
50221180h	4	DMA_CH1_CONTROL	00000000h
50221184h	4	DMA_CH1_TX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50221188h	4	DMA_CH1_RX_CONTROL	00000000h
50221190h	4	DMA_CH1_TXDESC_LIST_HADDRESS	00000000h
50221194h	4	DMA_CH1_TXDESC_LIST_ADDRESS	00000000h
50221198h	4	DMA_CH1_RXDESC_LIST_HADDRESS	00000000h
5022119Ch	4	DMA_CH1_RXDESC_LIST_ADDRESS	00000000h
502211A0h	4	DMA_CH1_TXDESC_TAIL_POINTER	00000000h
502211A8h	4	DMA_CH1_RXDESC_TAIL_POINTER	00000000h
502211ACh	4	DMA_CH1_TXDESC_RING_LENGTH	00000000h
502211B0h	4	DMA_CH1_RXDESC_RING_LENGTH	00000000h
502211B4h	4	DMA_CH1_INTERRUPT_ENABLE	00000000h
502211B8h	4	DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502211BCh	4	DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502211C4h	4	DMA_CH1_CURRENT_APP_TXDESC	00000000h
502211CCh	4	DMA_CH1_CURRENT_APP_RXDESC	00000000h
502211D0h	4	DMA_CH1_CURRENT_APP_TXBUFFER_H	00000000h
502211D4h	4	DMA_CH1_CURRENT_APP_TXBUFFER	00000000h
502211D8h	4	DMA_CH1_CURRENT_APP_RXBUFFER_H	00000000h
502211DCh	4	DMA_CH1_CURRENT_APP_RXBUFFER	00000000h
502211E0h	4	DMA_CH1_STATUS	00000000h
502211E4h	4	DMA_CH1_MISS_FRAME_CNT	00000000h
502211E8h	4	DMA_CH1_RXP_ACCEPT_CNT	00000000h
502211ECh	4	DMA_CH1_RX_ERI_CNT	00000000h
50221200h	4	DMA_CH2_CONTROL	00000000h
50221204h	4	DMA_CH2_TX_CONTROL	00000000h
50221208h	4	DMA_CH2_RX_CONTROL	00000000h
50221210h	4	DMA_CH2_TXDESC_LIST_HADDRESS	00000000h
50221214h	4	DMA_CH2_TXDESC_LIST_ADDRESS	00000000h
50221218h	4	DMA_CH2_RXDESC_LIST_HADDRESS	00000000h
5022121Ch	4	DMA_CH2_RXDESC_LIST_ADDRESS	00000000h
50221220h	4	DMA_CH2_TXDESC_TAIL_POINTER	00000000h
50221228h	4	DMA_CH2_RXDESC_TAIL_POINTER	00000000h
5022122Ch	4	DMA_CH2_TXDESC_RING_LENGTH	00000000h
50221230h	4	DMA_CH2_RXDESC_RING_LENGTH	00000000h
50221234h	4	DMA_CH2_INTERRUPT_ENABLE	00000000h
50221238h	4	DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5022123Ch	4	DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50221244h	4	DMA_CH2_CURRENT_APP_TXDESC	00000000h
5022124Ch	4	DMA_CH2_CURRENT_APP_RXDESC	00000000h
50221250h	4	DMA_CH2_CURRENT_APP_TXBUFFER_H	00000000h
50221254h	4	DMA_CH2_CURRENT_APP_TXBUFFER	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50221258h	4	DMA_CH2_CURRENT_APP_RXBUFFER_H	00000000h
5022125Ch	4	DMA_CH2_CURRENT_APP_RXBUFFER	00000000h
50221260h	4	DMA_CH2_STATUS	00000000h
50221264h	4	DMA_CH2_MISS_FRAME_CNT	00000000h
50221268h	4	DMA_CH2_RXP_ACCEPT_CNT	00000000h
5022126Ch	4	DMA_CH2_RX_ERI_CNT	00000000h
50221280h	4	DMA_CH3_CONTROL	00000000h
50221284h	4	DMA_CH3_TX_CONTROL	00000000h
50221288h	4	DMA_CH3_RX_CONTROL	00000000h
50221290h	4	DMA_CH3_TXDESC_LIST_HADDRESS	00000000h
50221294h	4	DMA_CH3_TXDESC_LIST_ADDRESS	00000000h
50221298h	4	DMA_CH3_RXDESC_LIST_HADDRESS	00000000h
5022129Ch	4	DMA_CH3_RXDESC_LIST_ADDRESS	00000000h
502212A0h	4	DMA_CH3_TXDESC_TAIL_POINTER	00000000h
502212A8h	4	DMA_CH3_RXDESC_TAIL_POINTER	00000000h
502212ACh	4	DMA_CH3_TXDESC_RING_LENGTH	00000000h
502212B0h	4	DMA_CH3_RXDESC_RING_LENGTH	00000000h
502212B4h	4	DMA_CH3_INTERRUPT_ENABLE	00000000h
502212B8h	4	DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502212BCh	4	DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502212C4h	4	DMA_CH3_CURRENT_APP_TXDESC	00000000h
502212CCh	4	DMA_CH3_CURRENT_APP_RXDESC	00000000h
502212D0h	4	DMA_CH3_CURRENT_APP_TXBUFFER_H	00000000h
502212D4h	4	DMA_CH3_CURRENT_APP_TXBUFFER	00000000h
502212D8h	4	DMA_CH3_CURRENT_APP_RXBUFFER_H	00000000h
502212DCh	4	DMA_CH3_CURRENT_APP_RXBUFFER	00000000h
502212E0h	4	DMA_CH3_STATUS	00000000h
502212E4h	4	DMA_CH3_MISS_FRAME_CNT	00000000h
502212E8h	4	DMA_CH3_RXP_ACCEPT_CNT	00000000h
502212ECh	4	DMA_CH3_RX_ERI_CNT	00000000h
50221300h	4	DMA_CH4_CONTROL	00000000h
50221304h	4	DMA_CH4_TX_CONTROL	00000000h
50221308h	4	DMA_CH4_RX_CONTROL	00000000h
50221310h	4	DMA_CH4_TXDESC_LIST_HADDRESS	00000000h
50221314h	4	DMA_CH4_TXDESC_LIST_ADDRESS	00000000h
50221318h	4	DMA_CH4_RXDESC_LIST_HADDRESS	00000000h
5022131Ch	4	DMA_CH4_RXDESC_LIST_ADDRESS	00000000h
50221320h	4	DMA_CH4_TXDESC_TAIL_POINTER	00000000h
50221328h	4	DMA_CH4_RXDESC_TAIL_POINTER	00000000h
5022132Ch	4	DMA_CH4_TXDESC_RING_LENGTH	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50221330h	4	DMA_CH4_RXDESC_RING_LENGTH	00000000h
50221334h	4	DMA_CH4_INTERRUPT_ENABLE	00000000h
50221338h	4	DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5022133Ch	4	DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50221344h	4	DMA_CH4_CURRENT_APP_TXDESC	00000000h
5022134Ch	4	DMA_CH4_CURRENT_APP_RXDESC	00000000h
50221350h	4	DMA_CH4_CURRENT_APP_TXBUFFER_H	00000000h
50221354h	4	DMA_CH4_CURRENT_APP_TXBUFFER	00000000h
50221358h	4	DMA_CH4_CURRENT_APP_RXBUFFER_H	00000000h
5022135Ch	4	DMA_CH4_CURRENT_APP_RXBUFFER	00000000h
50221360h	4	DMA_CH4_STATUS	00000000h
50221364h	4	DMA_CH4_MISS_FRAME_CNT	00000000h
50221368h	4	DMA_CH4_RXP_ACCEPT_CNT	00000000h
5022136Ch	4	DMA_CH4_RX_ERI_CNT	00000000h
50221380h	4	DMA_CH5_CONTROL	00000000h
50221384h	4	DMA_CH5_TX_CONTROL	00000000h
50221388h	4	DMA_CH5_RX_CONTROL	00000000h
50221390h	4	DMA_CH5_TXDESC_LIST_HADDRESS	00000000h
50221394h	4	DMA_CH5_TXDESC_LIST_ADDRESS	00000000h
50221398h	4	DMA_CH5_RXDESC_LIST_HADDRESS	00000000h
5022139Ch	4	DMA_CH5_RXDESC_LIST_ADDRESS	00000000h
502213A0h	4	DMA_CH5_TXDESC_TAIL_POINTER	00000000h
502213A8h	4	DMA_CH5_RXDESC_TAIL_POINTER	00000000h
502213ACh	4	DMA_CH5_TXDESC_RING_LENGTH	00000000h
502213B0h	4	DMA_CH5_RXDESC_RING_LENGTH	00000000h
502213B4h	4	DMA_CH5_INTERRUPT_ENABLE	00000000h
502213B8h	4	DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502213BCh	4	DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502213C4h	4	DMA_CH5_CURRENT_APP_TXDESC	00000000h
502213CCh	4	DMA_CH5_CURRENT_APP_RXDESC	00000000h
502213D0h	4	DMA_CH5_CURRENT_APP_TXBUFFER_H	00000000h
502213D4h	4	DMA_CH5_CURRENT_APP_TXBUFFER	00000000h
502213D8h	4	DMA_CH5_CURRENT_APP_RXBUFFER_H	00000000h
502213DCh	4	DMA_CH5_CURRENT_APP_RXBUFFER	00000000h
502213E0h	4	DMA_CH5_STATUS	00000000h
502213E4h	4	DMA_CH5_MISS_FRAME_CNT	00000000h
502213E8h	4	DMA_CH5_RXP_ACCEPT_CNT	00000000h
502213ECh	4	DMA_CH5_RX_ERI_CNT	00000000h
50221400h	4	DMA_CH6_CONTROL	00000000h
50221404h	4	DMA_CH6_TX_CONTROL	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50221408h	4	DMA_CH6_RX_CONTROL	00000000h
50221410h	4	DMA_CH6_TXDESC_LIST_HADDRESS	00000000h
50221414h	4	DMA_CH6_TXDESC_LIST_ADDRESS	00000000h
50221418h	4	DMA_CH6_RXDESC_LIST_HADDRESS	00000000h
5022141Ch	4	DMA_CH6_RXDESC_LIST_ADDRESS	00000000h
50221420h	4	DMA_CH6_TXDESC_TAIL_POINTER	00000000h
50221428h	4	DMA_CH6_RXDESC_TAIL_POINTER	00000000h
5022142Ch	4	DMA_CH6_TXDESC_RING_LENGTH	00000000h
50221430h	4	DMA_CH6_RXDESC_RING_LENGTH	00000000h
50221434h	4	DMA_CH6_INTERRUPT_ENABLE	00000000h
50221438h	4	DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
5022143Ch	4	DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
50221444h	4	DMA_CH6_CURRENT_APP_TXDESC	00000000h
5022144Ch	4	DMA_CH6_CURRENT_APP_RXDESC	00000000h
50221450h	4	DMA_CH6_CURRENT_APP_TXBUFFER_H	00000000h
50221454h	4	DMA_CH6_CURRENT_APP_TXBUFFER	00000000h
50221458h	4	DMA_CH6_CURRENT_APP_RXBUFFER_H	00000000h
5022145Ch	4	DMA_CH6_CURRENT_APP_RXBUFFER	00000000h
50221460h	4	DMA_CH6_STATUS	00000000h
50221464h	4	DMA_CH6_MISS_FRAME_CNT	00000000h
50221468h	4	DMA_CH6_RXP_ACCEPT_CNT	00000000h
5022146Ch	4	DMA_CH6_RX_ERI_CNT	00000000h
50221480h	4	DMA_CH7_CONTROL	00000000h
50221484h	4	DMA_CH7_TX_CONTROL	00000000h
50221488h	4	DMA_CH7_RX_CONTROL	00000000h
50221490h	4	DMA_CH7_TXDESC_LIST_HADDRESS	00000000h
50221494h	4	DMA_CH7_TXDESC_LIST_ADDRESS	00000000h
50221498h	4	DMA_CH7_RXDESC_LIST_HADDRESS	00000000h
5022149Ch	4	DMA_CH7_RXDESC_LIST_ADDRESS	00000000h
502214A0h	4	DMA_CH7_TXDESC_TAIL_POINTER	00000000h
502214A8h	4	DMA_CH7_RXDESC_TAIL_POINTER	00000000h
502214ACh	4	DMA_CH7_TXDESC_RING_LENGTH	00000000h
502214B0h	4	DMA_CH7_RXDESC_RING_LENGTH	00000000h
502214B4h	4	DMA_CH7_INTERRUPT_ENABLE	00000000h
502214B8h	4	DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER	00000000h
502214BCh	4	DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS	000007C0h
502214C4h	4	DMA_CH7_CURRENT_APP_TXDESC	00000000h
502214CCh	4	DMA_CH7_CURRENT_APP_RXDESC	00000000h
502214D0h	4	DMA_CH7_CURRENT_APP_TXBUFFER_H	00000000h
502214D4h	4	DMA_CH7_CURRENT_APP_TXBUFFER	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
502214D8h	4	DMA_CH7_CURRENT_APP_RXBUFFER_H	00000000h
502214DCh	4	DMA_CH7_CURRENT_APP_RXBUFFER	00000000h
502214E0h	4	DMA_CH7_STATUS	00000000h
502214E4h	4	DMA_CH7_MISS_FRAME_CNT	00000000h
502214E8h	4	DMA_CH7_RXP_ACCEPT_CNT	00000000h
502214ECh	4	DMA_CH7_RX_ERI_CNT	00000000h

14.20.3.1 MAC_CONFIGURATION — Offset 50220000h

The MAC Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50220000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ARP Offload Enable (ARPEN):** When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. 0x0 (DISABLE): ARP Offload is disabled. 0x1 (ENABLE): ARP Offload is enabled.
30:28	0h RW	**Source Address Insertion or Replacement Control (SARC):** This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: - The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: - Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field. 0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field. 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field. 0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field..
27	0h RW	**Checksum Offload (IPC):** When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. 0x0 (DISABLE): IP header/payload checksum checking is disabled. 0x1 (ENABLE): IP header/payload checksum checking is enabled.

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Inter-Packet Gap (IPG):** These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. 0x0 (IPG96): 96 bit times IPG. 0x1 (IPG88): 88 bit times IPG. 0x2 (IPG80): 80 bit times IPG. 0x3 (IPG72): 72 bit times IPG. 0x4 (IPG64): 64 bit times IPG. 0x5 (IPG56): 56 bit times IPG. 0x6 (IPG48): 48 bit times IPG. 0x7 (IPG40): 40 bit times IPG.
23	0h RW	**Giant Packet Size Limit Control Enable (GPSLCE):** When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. 0x0 (DISABLE): Giant Packet Size Limit Control is disabled. 0x1 (ENABLE): Giant Packet Size Limit Control is enabled.
22	0h RW	**IEEE 802.3as Support for 2K Packets (S2KP):** When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. 0x0 (DISABLE): Support upto 2K packet is disabled. 0x1 (ENABLE): Support upto 2K packet is Enabled.
21	0h RW	**CRC stripping for Type packets (CST):** When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. 0x0 (DISABLE): CRC stripping for Type packets is disabled. 0x1 (ENABLE): CRC stripping for Type packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Automatic Pad or CRC Stripping (ACS):** When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. 0x0 (DISABLE): Automatic Pad or CRC Stripping is disabled. 0x1 (ENABLE): Automatic Pad or CRC Stripping is enabled..
19	0h RW	**Watchdog Disable (WD):** When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. 0x0 (ENABLE): Watchdog is enabled. 0x1 (DISABLE): Watchdog is disabled.
18	0h RW	**Packet Burst Enable (BE)**: When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0x0 (DISABLE): Packet Burst is disabled. 0x1 (ENABLE): Packet Burst is enabled..
17	0h RW	**Jabber Disable (JD):** When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. 0x0 (ENABLE): Jabber is enabled. 0x1 (DISABLE): Jabber is disabled.
16	0h RW	**Jumbo Packet Enable (JE):** When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0x0 (DISABLE): Jumbo packet is disabled. 0x1 (ENABLE): Jumbo packet is enabled.
15	0h RW	**Port Select (PS):** This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is readwrite (R/W). 0x0 (M_1000_2500M): For 1000 or 2500 Mbps operations. 0x1 (M_10_100M): For 10 or 100 Mbps operations.
14	0h RW	**FES:** This bit selects the speed mode. 0x0 (M_10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0. 0x1 (M_100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Duplex Mode (DM):** When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the fullduplex-only configurations. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.
12	0h RW	**Loopback Mode (LM):** When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. 0x0 (DISABLE): Loopback is disabled. 0x1 (ENABLE): Loopback is enabled.
11	0h RW	**Enable Carrier Sense Before Transmission in Full-Duplex Mode (ECRSFD):** When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal. 0x0 (DISABLE): ECRSFD is disabled. 0x1 (ENABLE): ECRSFD is enabled.
10	0h RW	**Disable Receive Own (DO):** When this bit is set, the MAC disables the reception of packets when the GMII signal TX_EN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode. 0x0 (ENABLE): Enable Receive Own. 0x1 (DISABLE): Disable Receive Own.
9	0h RW	**Disable Carrier Sense During Transmission (DCRS)**: When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. 0x0 (ENABLE): Enable Carrier Sense During Transmission. 0x1 (DISABLE): Disable Carrier Sense During Transmission.
8	0h RW	**Disable Retry (DR):** When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. 0x0 (ENABLE): Enable Retry. 0x1 (DISABLE): Disable Retry.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Back-Off Limit (BL):** The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. 0x0 (MIN_N_10): k = min(n,10). 0x1 (MIN_N_8): k = min(n,8). 0x2 (MIN_N_4): k = min(n,4). 0x3 (MIN_N_1): k = min(n,1).
4	0h RW	**Deferral Check (DC):** When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. 0x0 (DISABLE): Deferral check function is disabled. 0x1 (ENABLE): Deferral check function is enabled.
3:2	0h RW	**Preamble Length for Transmit packets (PRELEN):** These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 0x0 (M_7BYTES): 7 bytes of preamble. 0x1 (M_5BYTES): 5 bytes of preamble. 0x2 (M_3BYTES): 3 bytes of preamble. 0x3 (RESERVED): Reserved.
1	0h RW	**Transmitter Enable (TE):** When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. 0x0 (DISABLE): Transmitter is disabled. 0x1 (ENABLE): Transmitter is enabled.
0	0h RW	**Receiver Enable (RE):** When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. 0x0 (DISABLE): Receiver is disabled. 0x1 (ENABLE): Receiver is enabled.

14.20.3.2 MAC_EXT_CONFIGURATION — Offset 50220004h

The MAC Extended Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50220004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**ARP Packet Drop if IP Mismatch (APDIM):** When set, Packet for which Target Protocol Address does not match IPv4 address is dropped in the MTL layer. When reset, when target Protocol Address does not match, packet is forwarded to MTL maintaining backward compatibility. 0x0 (DISABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address disabled. 0x1 (ENABLE): mux select to drop the arp packet if Trgt prot address mismatches IPv4 address enabled.
29:25	00h RW	**Extended Inter-Packet Gap (EIPG):** The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	0h RW	**Extended Inter-Packet Gap Enable (EIPGEN):** When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. 0x0 (DISABLE): Extended Inter-Packet Gap is disabled. 0x1 (ENABLE): Extended Inter-Packet Gap is enabled
23	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**Maximum Size for Splitting the Header Data (HDSMS):** These bits indicate the maximum header size allowed for splitting the header data in the received packet. 0x0 (M_64BYTES): Maximum Size for Splitting the Header Data is 64 bytes. 0x1 (M_128BYTES): Maximum Size for Splitting the Header Data is 128 bytes. 0x2 (M_256BYTES): Maximum Size for Splitting the Header Data is 256 bytes. 0x3 (M_512BYTES): Maximum Size for Splitting the Header Data is 512 bytes. 0x4 (M_1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes. 0x5 (RSVD): Reserved.
19	0h RW	**Packet Duplication Control (PDC):** When this bit is set, the received packet with Multicast/Broadcast Destination address is routed to multiple Receive DMA Channels. The Receive DMA Channels is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Multicast/Broadcast Destination address in the received packet. The DCS field is interpreted to be a one-hot value, each bit corresponding to the Receive DMA Channel. When this bit is reset, the received packet is routed to single Receive DMA Channel. The Receive DMA Channel is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Destination address in the received packet. The DCS field is interpreted as a binary value. 0x0 (DISABLE): Packet Duplication Control is disabled. 0x1 (ENABLE): Packet Duplication Control is enabled.
18	0h RW	**Unicast Slow Protocol Packet Detect (USP):** When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. 0x0 (DISABLE): Unicast Slow Protocol Packet Detection is disabled. 0x1 (ENABLE): Unicast Slow Protocol Packet Detection is enabled.
17	0h RW	**Slow Protocol Detection Enable (SPEN):** When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. 0x0 (DISABLE): Slow Protocol Detection is disabled. 0x1 (ENABLE): Slow Protocol Detection is enabled.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Disable CRC Checking for Received Packets (DCRCC):** When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. 0x0 (ENABLE): CRC Checking is enabled. 0x1 (DISABLE): CRC Checking is disabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Giant Packet Size Limit (GPSL):** If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

14.20.3.3 MAC_PACKET_FILTER — Offset 50220008h

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.

Type	Size	Offset	Default
MMIO	32 bit	50220008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Receive All (RA):** When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled. 0x1 (ENABLE): Receive All is enabled.
30:22	0h RO	**Reserved**
21	0h RW	**Drop Non-TCP/UDP over IP Packets (DNTU):** When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0 (FWD): Forward Non-TCP/UDP over IP Packets. 0x1 (DROP): Drop Non-TCP/UDP over IP Packets.
20	0h RW	**Layer 3 and Layer 4 Filter Enable (IPFE):** When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled. 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled.
19:17	0h RO	**Reserved**
16	0h RW	**VLAN Tag Filter Enable (VTFE):** When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. 0x0 (DISABLE): VLAN Tag Filter is disabled. 0x1 (ENABLE): VLAN Tag Filter is enabled.
15:11	0h RO	**Reserved**
10	0h RW	**Hash or Perfect Filter (HPF):** When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. 0x0 (DISABLE): Hash or Perfect Filter is disabled. 0x1 (ENABLE): Hash or Perfect Filter is enabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Source Address Filter Enable (SAF):** When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in GbE Controller, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA. 0x0 (DISABLE): SA Filtering is disabled. 0x1 (ENABLE): SA Filtering is enabled.
8	0h RW	**SA Inverse Filtering (SAIF):** When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0 (DISABLE): SA Inverse Filtering is disabled. 0x1 (ENABLE): SA Inverse Filtering is enabled.
7:6	0h RW	**Pass Control Packets (PCF):** These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0x0 (FLTR_ALL): MAC filters all control packets from reaching the application. 0x1 (FW_XCPT_PAU): MAC forwards all control packets except Pause packets to the application even if they fail the Address filter. 0x2 (FW_ALL): MAC forwards all control packets to the application even if they fail the Address filter. 0x3 (FW_PASS): MAC forwards the control packets that pass the Address filter.
5	0h RW	**Disable Broadcast Packets (DBF):** When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. 0x0 (ENABLE): Enable Broadcast Packets. 0x1 (DISABLE): Disable Broadcast Packets.
4	0h RW	**Pass All Multicast (PM):** When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. 0x0 (DISABLE): Pass All Multicast is disabled. 0x1 (ENABLE): Pass All Multicast is enabled.
3	0h RW	**DA Inverse Filtering (DAIF):** When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. 0x0 (DISABLE): DA Inverse Filtering is disabled. 0x1 (ENABLE): DA Inverse Filtering is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Hash Multicast (HMC):** When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Multicast is disabled. 0x1 (ENABLE): Hash Multicast is enabled.
1	0h RW	**Hash Unicast (HUC):** When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0 (DISABLE): Hash Unicast is disabled. 0x1 (ENABLE): Hash Unicast is enabled.
0	0h RW	**Promiscuous Mode (PR):** When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. 0x0 (DISABLE): Promiscuous Mode is disabled. 0x1 (ENABLE): Promiscuous Mode is enabled.

14.20.3.4 MAC_WATCHDOG_TIMEOUT — Offset 5022000Ch

The Watchdog Timeout register controls the watchdog timeout for received packets.

Type	Size	Offset	Default
MMIO	32 bit	5022000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Programmable Watchdog Enable (PWE):** When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. 0x0 (DISABLE): Programmable Watchdog is disabled. 0x1 (ENABLE): Programmable Watchdog is enabled.
7:4	0h RO	**Reserved**
3:0	0h RW	**Watchdog Timeout (WTO):** When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. 0x0 (M_2KBYTES): 2 KB. 0x1 (M_3KBYTES): 3 KB. 0x2 (M_4KBYTES): 4 KB. 0x3 (M_5KBYTES): 5 KB. 0x4 (M_6KBYTES): 6 KB. 0x5 (M_7KBYTES): 7 KB. 0x6 (M_8KBYTES): 8 KB. 0x7 (M_9KBYTES): 9 KB. 0x08 (M_10KBYTES): 10 KB. 0x09 (M_11KBYTES): 11 KB. 0x0A (M_12KBYTES): 12 KB. 0x0B (M_13KBYTES): 13 KB. 0x0C (M_14KBYTES): 14 KB. 0x0D (M_15KBYTES): 15 KB. 0x0E (M_16383BYTES): 16383 Bytes. 0x0F (RESERVED): Reserved.

14.20.3.5 MAC_HASH_TABLE_REG0 — Offset 50220010h

The Hash Table Register 0 contains the first 32 bits of the hash table, when the width of the hash table is 128 or 256 bits. You can specify the width of the hash table by using the Hash Table Size option in coreConsultant. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way:
- Calculate the 32-bit CRC for the DA
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted

regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50220010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table First 32 Bits (HT31T0):** This field contains the first 32 Bits [31:0] of the Hash table.

14.20.3.6 MAC_HASH_TABLE_REG1 — Offset 50220014h

The Hash Table Register 1 contains the second 32 bits of the hash table. You can specify the width of the hash table by using the Hash Table Size option in coreConsultant. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way:
- Calculate the 32-bit CRC for the DA.
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50220014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC Hash Table Second 32 Bits (HT63T32):** This field contains the second 32 Bits [63:32] of the Hash table.

14.20.3.7 MAC_VLAN_TAG_CTRL — Offset 50220050h

This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers.

Type	Size	Offset	Default
MMIO	32 bit	50220050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Inner VLAN Tag in Rx Status (EIVLRXS):** When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled. 0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled.
30	0h RO	**Reserved**
29:28	0h RW	**Enable Inner VLAN Tag Stripping on Receive (EIVLS):** This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** When this bit, VTHM bit and the EDVLP field are set, the MAC receiver enables VLAN Hash filtering operation on the inner VLAN Tag (if present). When this bit is reset and VTHM bit is set, the MAC receiver enables VLAN Hash filtering operation on the outer VLAN Tag (if present). The ERSVLM bit and DOVLTC bit determines which VLAN type is enabled for filtering. 0x0 (DISABLE): Inner VLAN tag is disabled. 0x1 (ENABLE): Inner VLAN tag is enabled.
26	0h RW	**Enable Double VLAN Processing (EDVLP):** When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0 (DISABLE): Double VLAN Processing is disabled. 0x1 (ENABLE): Double VLAN Processing is enabled.
25	0h RW	**VLAN Tag Hash Table Match Enable (VTHM):** When this bit is set, the most significant four bits of CRC of VLAN Tag are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled. 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled.
24	0h RW	**Enable VLAN Tag in Rx status (EVLRXS):** When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. 0x0 (DISABLE): VLAN Tag in Rx status is disabled. 0x1 (ENABLE): VLAN Tag in Rx status is enabled.
23	0h RO	**Reserved**
22:21	0h RW	**Enable VLAN Tag Stripping on Receive (EVLS):** This field indicates the stripping operation on the outer VLAN Tag in received packet. 0x0 (DONOT): Do not strip. 0x1 (IFPASS): Strip if VLAN filter passes. 0x2 (IFFAIL): Strip if VLAN filter fails. 0x3 (ALWAYS): Always strip.
20	0h RW	**Disable VLAN Type Check for VLAN Hash Filtering (DOVLTC):** When this bit is set, the MAC VLAN Hash Filter does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC VLAN Hash Filter filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. 0x0 (ENABLE): VLAN Type Check is enabled. 0x1 (DISABLE): VLAN Type Check is disabled.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Enable Receive S-VLAN Match for VLAN Hash Filtering (ERSVLM):** When this bit is set, the MAC receiver enables VLAN Hash filtering or matching for SVLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables VLAN Hash filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for VLAN Hash filtering or matching. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.
18	0h RW	**Enable S-VLAN (ESVL):** When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. 0x0 (DISABLE): S-VLAN is disabled. 0x1 (ENABLE): S-VLAN is enabled.
17	0h RW	**VLAN Tag Inverse Match Enable (VTIM):** When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. 0x0 (DISABLE): VLAN Tag Inverse Match is disabled. 0x1 (ENABLE): VLAN Tag Inverse Match is enabled.
16	0h RW	**Enable 12-Bit VLAN Tag Comparison for VLAN Hash Filtering (ETV):** When this bit is set, a 12-bit VLAN identifier is used for VLAN Hash filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag in the received VLAN-tagged packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for VLAN hash filtering. 0x0 (DISABLE): 12-Bit VLAN Tag Comparison is disabled. 0x1 (ENABLE): 12-Bit VLAN Tag Comparison is enabled.
15:5	0h RO	**Reserved**
4:2	0h RW	**OFS:** This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	0h RW	**Command Type (CT):** This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation. 0x0 (WRITE): Write operation. 0x1 (READ): Read operation.
0	0h RW	**Operation Busy (OB):** This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset. 0x0 (DISABLE): Operation Busy is disabled. 0x1 (ENABLE): Operation Busy is enabled.

14.20.3.8 MAC_VLAN_TAG_DATA — Offset 50220054h

This register holds the read/write data for Indirect Access of the Per VLAN Tag registers. During the read access, this field contains valid read data only after the OB bit is reset. During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register.

Type	Size	Offset	Default
MMIO	32 bit	50220054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:25	0h RW	**DMA Channel Number (DMACHN):** The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	0h RW	**DMA Channel Number Enable (DMACHEN):** This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing. 0x0 (DISABLE): DMA Channel Number is disabled. 0x1 (ENABLE): DMA Channel Number is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**Enable Inner VLAN Tag Comparison (ERIVLT):** This bit is valid only when Double VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). 0x0 (DISABLE): Inner VLAN tag comparison is disabled. 0x1 (ENABLE): Inner VLAN tag comparison is enabled.
19	0h RW	**Enable S-VLAN Match for received Frames (ERSVLM):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. 0x0 (DISABLE): Receive S-VLAN Match is disabled. 0x1 (ENABLE): Receive S-VLAN Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Disable VLAN Type Comparison (DOVLTC):** This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit. 0x0 (ENABLE): VLAN type comparison is enabled. 0x1 (DISABLE): VLAN type comparison is disabled.
17	0h RW	**12bits or 16bits VLAN comparison (ETV):** This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. 0x0 (M_16BIT): 16 bit VLAN comparison. 0x1 (M_12BIT): 12 bit VLAN comparison.
16	0h RW	**VLAN Tag Enable (VEN):** This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields. 0x0 (DISABLE): VLAN Tag is disabled. 0x1 (ENABLE): VLAN Tag is enabled.
15:0	0000h RW	**VLAN Tag ID (VID):** This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

14.20.3.9 MAC_VLAN_HASH_TABLE — Offset 50220058h

When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. The upper four bits of the calculated hash value are used to index the contents of the VLAN Hash table. For example, hash value of 4b'1000 selects Bit 8 of the VLAN Hash table. The hash value of the destination address is calculated in the following way:
- Calculate the 32-bit CRC for the VLAN tag or ID
- Perform bitwise reversal for the value obtained in step 1.
- Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] of this register are written. - If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50220058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**VLAN Hash Table (VLHT):** This field contains the 16-bit VLAN Hash Table.

14.20.3.10 MAC_VLAN_INCL — Offset 50220060h

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	50220060h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BUSY:** This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register. 0x0 (INACTIVE): Busy status not detected. 0x1 (ACTIVE): Busy status detected.
30	0h RW	**Read write control (RDWR):** This bit controls the read or write operation for indirectly accessing the queue/ channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset. 0x0 (READ): Read operation of indirect access. 0x1 (WRITE): Write operation of indirect access.
29:27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**ADDR:** This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset.
23:22	0h RO	**Reserved**
21	0h RW	**Channel based tag insertion (CBTI):** When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register. 0x0 (DISABLE): Channel based tag insertion is disabled. 0x1 (ENABLE): Channel based tag insertion is enabled.
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted in the 13th and 14th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

14.20.3.11 MAC_INNER_VLAN_INCL — Offset 50220064h

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	50220064h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW	**VLAN Tag Input (VLTI):** When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor 0x0 (DISABLE): VLAN Tag Input is disabled. 0x1 (ENABLE): VLAN Tag Input is enabled.
19	0h RW	**C-VLAN or S-VLAN (CSVL):** When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 17th and 18th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 17th and 18th bytes of transmitted packets. 0x0 (C_VLAN): C-VLAN type (0x8100) is inserted. 0x1 (S_VLAN): S-VLAN type (0x88A8) is inserted.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**VLAN Priority Control (VLP):** When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored. 0x0 (DISABLE): VLAN Priority Control is disabled. 0x1 (ENABLE): VLAN Priority Control is enabled.
17:16	0h RW	**VLC:** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. 0x0 (NONE): No VLAN tag deletion, insertion, or replacement. 0x1 (DELETE): VLAN tag deletion. 0x2 (INSERT): VLAN tag insertion. 0x3 (REPLACE): VLAN tag replacement.
15:0	0000h RW	**VLAN Tag for Transmit Packets (VLT):** This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

14.20.3.12 MAC_Q0_TX_FLOW_CTRL — Offset 50220070h

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The Busy bit remains set until the control packet is transferred onto the cable. The application must make sure that the Busy bit is cleared before writing to the register. When the PFCE bit in the MAC_Rx_Flow_Ctrl register is enabled, this register controls the generation of Priority Flow Control (PFC) frames with priorities mapped according to PSRQ0 in the MAC_RxQ_Ctrl2 register.

Type	Size	Offset	Default
MMIO	32 bit	50220070h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy or Backpressure Activate (FCB_BPA):** This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

14.20.3.13 MAC_Q1_TX_FLOW_CTRL — Offset 50220074h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	50220074h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Pause Time (PT):** This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**Disable Zero-Quanta Pause (DZPQ):** When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled. 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled.
6:4	0h RW	**Pause Low Threshold (PLT):** This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4 slot times). 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times). 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times). 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times). 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times). 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times). 0x6 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Transmit Flow Control Enable (TFE):** When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. 0x0 (DISABLE): Transmit Flow Control is disabled. 0x1 (ENABLE): Transmit Flow Control is enabled.
0	0h RW	**Flow Control Busy (FCB_BPA):** This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled. 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled.

14.20.3.14 MAC_Q2_TX_FLOW_CTRL — Offset 50220078h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50220074h.

14.20.3.15 MAC_Q3_TX_FLOW_CTRL — Offset 5022007Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50220074h.

14.20.3.16 MAC_Q4_TX_FLOW_CTRL — Offset 50220080h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50220074h.

14.20.3.17 MAC_Q5_TX_FLOW_CTRL — Offset 50220084h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50220074h.

14.20.3.18 MAC_Q6_TX_FLOW_CTRL — Offset 50220088h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50220074h.

14.20.3.19 MAC_Q7_TX_FLOW_CTRL — Offset 5022008Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 50220074h.

14.20.3.20 MAC_RX_FLOW_CTRL — Offset 50220090h

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

Type	Size	Offset	Default
MMIO	32 bit	50220090h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Priority Based Flow Control Enable (PFCE):** When this bit is set, it enables generation and reception of priority-based flow control (PFC) packets. When this bit is reset, it enables generation and reception of 802.3x Pause control packets. 0x0 (DISABLE): Priority Based Flow Control is disabled. 0x1 (ENABLE): Priority Based Flow Control is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Unicast Pause Packet Detect (UP):** A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. 0x0 (DISABLE): Unicast Pause Packet Detect disabled. 0x1 (ENABLE): Unicast Pause Packet Detect enabled.
0	0h RW	**Receive Flow Control Enable (RFE):** When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. 0x0 (DISABLE): Receive Flow Control is disabled. 0x1 (ENABLE): Receive Flow Control is enabled.

14.20.3.21 MAC_RXQ_CTRL4 — Offset 50220094h

The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	50220094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW	**VLAN Tag Filter Fail Packets Queue (VFFQ):** This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	0h RW	**VLAN Tag Filter Fail Packets Queuing Enable (VFFQE):** When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled.
15:12	0h RO	**Reserved**
11:9	0h RW	**Multicast Address Filter Fail Packets Queue. (MFFQ):** This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
8	0h RW	**Multicast Address Filter Fail Packets Queuing Enable. (MFFQE):** When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3:1	0h RW	**Unicast Address Filter Fail Packets Queue. (UFFQ):** This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	0h RW	**Unicast Address Filter Fail Packets Queuing Enable. (UFFQE):** When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled. 0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled.

14.20.3.22 MAC_TXQ_PRTY_MAP0 — Offset 50220098h

The Transmit Queue Priority Mapping 0 register contains the priority values assigned to Tx Queue 0 through Tx Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	50220098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 3 (PSTQ3):** This bit is similar to the PSTQ0 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 2 (PSTQ2):** This bit is similar to the PSTQ0 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 1 (PSTQ1):** This bit is similar to the PSTQ0 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 0 (PSTQ0):** This field holds the priorities assigned to Tx Queue 0 by the software. This field determines if Tx Queue 0 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

14.20.3.23 MAC_TXQ_PRTY_MAP1 — Offset 5022009Ch

The Transmit Queue Priority Mapping 1 register contains the priority values assigned to Tx Queue 4 through Tx Queue 7.

Type	Size	Offset	Default
MMIO	32 bit	5022009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in Transmit Queue 7 (PSTQ7):** This bit is similar to the PSTQ4 bit.
23:16	00h RW	**Priorities Selected in Transmit Queue 6 (PSTQ6):** This bit is similar to the PSTQ4 bit.
15:8	00h RW	**Priorities Selected in Transmit Queue 5 (PSTQ5):** This bit is similar to the PSTQ4 bit.
7:0	00h RW	**Priorities Selected in Transmit Queue 4 (PSTQ4):** This field holds the priorities assigned to Tx Queue 4 by the software. This field determines if Tx Queue 4 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

14.20.3.24 MAC_RXQ_CTRL0 — Offset 502200A0h

The Receive Queue Control 0 register controls the queue management in the MAC Receiver. Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

Type	Size	Offset	Default
MMIO	32 bit	502200A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:14	0h RW	**Receive Queue 7 Enable (RXQ7EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
13:12	0h RW	**Receive Queue 6 Enable (RXQ6EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
11:10	0h RW	**Receive Queue 5 Enable (RXQ5EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
9:8	0h RW	**Receive Queue 4 Enable (RXQ4EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
7:6	0h RW	**Receive Queue 3 Enable (RXQ3EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Receive Queue 2 Enable (RXQ2EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
3:2	0h RW	**Receive Queue 1 Enable (RXQ1EN):** This field is similar to the RXQ0EN field. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.
1:0	0h RW	**Receive Queue 0 Enable (RXQ0EN):** This field indicates whether Rx Queue 0 is enabled for AV or DCB. 0x0 (DISABLE): Queue not enabled. 0x1 (EN_AV): Queue enabled for AV. 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic. 0x3 (RSVD): Reserved.

14.20.3.25 MAC_RXQ_CTRL1 — Offset 502200A4h

The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	502200A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**OMCBCQ:** 0x0 (DISABLE): overriding MCBCQ priority disabled. 0x1 (ENABLE): overriding MCBCQ priority enabled.
27	0h RO	**Reserved**
26:24	0h RW	**Frame Preemption Residue Queue (FPRQ):** This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RW	**Tagged PTP over Ethernet Packets Queuing Control. (TPQC):** This field controls the routing of the VLAN Tagged PTPoE packets. The following programmable options are allowed. - 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). - 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). - 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. - 2'b11: Reserved
21	0h RW	**Tagged AV Control Packets Queuing Enable. (TACPQE):** When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers. 0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled. 0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled.
20	0h RW	**Multicast and Broadcast Queue Enable (MCBCQEN):** This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. 0x0 (DISABLE): Multicast and Broadcast Queue is disabled. 0x1 (ENABLE): Multicast and Broadcast Queue is enabled.
19	0h RO	**Reserved**
18:16	0h RW	**Multicast and Broadcast Queue (MCBCQ):** This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
15	0h RO	**Reserved**
14:12	0h RW	**Untagged Packet Queue (UPQ):** This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**DCB Control Packets Queue (DCBCPQ):** This field specifies the Rx queue on which the received DCB control packets are routed. The DCB data packets are routed based on the PSRQ field of the Transmit Flow Control Register of corresponding queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
7	0h RO	**Reserved**
6:4	0h RW	**PTP Packets Queue (PTPQ):** This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.
3	0h RO	**Reserved**
2:0	0h RW	**AV Untagged Control Packets Queue (AVCPQ):** This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field. 0x0 (QUEUE0): Receive Queue 0. 0x1 (QUEUE1): Receive Queue 1. 0x2 (QUEUE2): Receive Queue 2. 0x3 (QUEUE3): Receive Queue 3. 0x4 (QUEUE4): Receive Queue 4. 0x5 (QUEUE5): Receive Queue 5. 0x6 (QUEUE6): Receive Queue 6. 0x7 (QUEUE7): Receive Queue 7.

14.20.3.26 MAC_RXQ_CTRL2 — Offset 502200A8h

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3.

Type	Size	Offset	Default
MMIO	32 bit	502200A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 3 (PSRQ3):** This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 3 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 2 (PSRQ2):** This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 2 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 1 (PSRQ1):** This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 0 (PSRQ0):** This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.

14.20.3.27 MAC_RXQ_CTRL3 — Offset 502200ACh

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 4 to 7.

Type	Size	Offset	Default
MMIO	32 bit	502200ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Priorities Selected in the Receive Queue 7 (PSRQ7):** This field decides the priorities assigned to Rx Queue 7. All packets with priorities that match the values set in this field are routed to Rx Queue 7. For example, if PSRQ7[7, 4] are set, packets with USP field equal to 7 or 4 are routed to Rx Queue 7. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 7 crosses the flow control threshold settings.
23:16	00h RW	**Priorities Selected in the Receive Queue 6 (PSRQ6):** This field decides the priorities assigned to Rx Queue 6. All packets with priorities that match the values set in this field are routed to Rx Queue 6. For example, if PSRQ6[5] are set, packets with USP field equal to 5 are routed to Rx Queue 6. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 6 crosses the flow control threshold settings.
15:8	00h RW	**Priorities Selected in the Receive Queue 5 (PSRQ5):** This field decides the priorities assigned to Rx Queue 5. All packets with priorities that match the values set in this field are routed to Rx Queue 5. For example, if PSRQ5[6] is set, packets with USP field equal to 6 are routed to Rx Queue 5. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 5 crosses the flow control threshold settings.
7:0	00h RW	**Priorities Selected in the Receive Queue 4 (PSRQ4):** This field decides the priorities assigned to Rx Queue 4. All packets with priorities that match the values set in this field are routed to Rx Queue 4. For example, if PSRQ4[7:4] is set, packets with USP field equal to 7, 6, 5, or 4 are routed to Rx Queue 4. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 4 crosses the flow control threshold settings.

14.20.3.28 MAC_INTERRUPT_STATUS — Offset 502200B0h

The Interrupt Status register contains the status of interrupts.

Type	Size	Offset	Default
MMIO	32 bit	502200B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**MMC FPE Receive Interrupt Status (MFRIS):** This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active. 0x1 (ACTIVE): MMC FPE Receive Interrupt status active.
19	0h RO	**MMC FPE Transmit Interrupt Status (MFTIS):** This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support. 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active. 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active.
18	0h RO	**MDIO Interrupt Status (MDIOIS):** This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): MDIO Interrupt status not active. 0x1 (ACTIVE): MDIO Interrupt status active.
17	0h RO	**Frame Preemption Interrupt Status (FPEIS):** This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt. 0x0 (INACTIVE): Frame Preemption Interrupt status not active. 0x1 (ACTIVE): Frame Preemption Interrupt status active.
16	0h RO	**Reserved**
15	0h RO	**GPI Interrupt Status (GPIIS):** When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field of the MAC_GPIO_Status register and the corresponding GPIE bit is enabled in the MAC_GPIO_Control register. This bit is cleared on reading lane 0 (GPIS) of the MAC_GPIO_Status register. 0x0 (INACTIVE): GPI Interrupt status not active. 0x1 (ACTIVE): GPI Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Receive Status Interrupt (RXSTSIS):** This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Receive Interrupt status not active. 0x1 (ACTIVE): Receive Interrupt status active.
13	0h RO	**Transmit Status Interrupt (TXSTSIS):** This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. 0x0 (INACTIVE): Transmit Interrupt status not active. 0x1 (ACTIVE): Transmit Interrupt status active.
12	0h RO	**Timestamp Interrupt Status (TSIS):** If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: - The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. - There is an overflow in the Seconds register. - The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. 0x0 (INACTIVE): Timestamp Interrupt status not active. 0x1 (ACTIVE): Timestamp Interrupt status active.
11	0h RO	**MMC Receive Checksum Offload Interrupt Status (MMCRXIPIS):** This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. 0x0 (INACTIVE): MMC Receive Checksum Offload Interrupt status not active. 0x1 (ACTIVE): MMC Receive Checksum Offload Interrupt status active.
10	0h RO	**MMC Transmit Interrupt Status (MMCTXIS):** This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Transmit Interrupt status not active. 0x1 (ACTIVE): MMC Transmit Interrupt status active.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**MMC Receive Interrupt Status (MMCRXIS):** This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Receive Interrupt status not active. 0x1 (ACTIVE): MMC Receive Interrupt status active.
8	0h RO	**MMC Interrupt Status (MMCIS):** This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. 0x0 (INACTIVE): MMC Interrupt status not active. 0x1 (ACTIVE): MMC Interrupt status active.
7:6	0h RO	**Reserved**
5	0h RO	**LPI Interrupt Status (LPIIS):** When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): LPI Interrupt status not active. 0x1 (ACTIVE): LPI Interrupt status active.
4	0h RO	**PMT Interrupt Status (PMTIS):** This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. 0x0 (INACTIVE): PMT Interrupt status not active. 0x1 (ACTIVE): PMT Interrupt status active.
3	0h RO	**PHY Interrupt (PHYIS):** This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): PHY Interrupt not detected. 0x1 (ACTIVE): PHY Interrupt detected.
2:1	0h RO	**Reserved**
0	0h RO	**RGMII or SMII Interrupt Status (RGSMIIIS):** This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active. 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active.

14.20.3.29 MAC_INTERRUPT_ENABLE — Offset 502200B4h

The Interrupt Enable register contains the masks for generating the interrupts.

Type	Size	Offset	Default
MMIO	32 bit	502200B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**MDIO Interrupt Enable (MDIOIE):** When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): MDIO Interrupt is disabled. 0x1 (ENABLE): MDIO Interrupt is enabled.
17	0h RW	**Frame Preemption Interrupt Enable (FPEIE):** When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. 0x0 (DISABLE): Frame Preemption Interrupt is disabled. 0x1 (ENABLE): Frame Preemption Interrupt is enabled.
16:15	0h RO	**Reserved**
14	0h RW	**Receive Status Interrupt Enable (RXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Receive Status Interrupt is disabled. 0x1 (ENABLE): Receive Status Interrupt is enabled.
13	0h RW	**Transmit Status Interrupt Enable (TXSTSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Status Interrupt is disabled. 0x1 (ENABLE): Timestamp Status Interrupt is enabled.
12	0h RW	**Timestamp Interrupt Enable (TSIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): Timestamp Interrupt is disabled. 0x1 (ENABLE): Timestamp Interrupt is enabled.
11:6	0h RO	**Reserved**
5	0h RW	**LPI Interrupt Enable (LPIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): LPI Interrupt is disabled. 0x1 (ENABLE): LPI Interrupt is enabled.
4	0h RW	**PMT Interrupt Enable (PMTIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PMT Interrupt is disabled. 0x1 (ENABLE): PMT Interrupt is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PHY Interrupt Enable (PHYIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): PHY Interrupt is disabled. 0x1 (ENABLE): PHY Interrupt is enabled.
2:1	0h RO	**Reserved**
0	0h RW	**RGMII or SMII Interrupt Enable (RGSMIIIE):** When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. 0x0 (DISABLE): RGMII or SMII Interrupt is disabled. 0x1 (ENABLE): RGMII or SMII Interrupt is enabled.

14.20.3.30 MAC_RX_TX_STATUS — Offset 502200B8h

The Receive Transmit Status register contains the Receive and Transmit Error status.

Type	Size	Offset	Default
MMIO	32 bit	502200B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO	**Receive Watchdog Timeout (RWT):** This bit is set when a packet with length greater than 2,048 bytes is received (10,240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No receive watchdog timeout. 0x1 (ACTIVE): Receive watchdog timed out.
7:6	0h RO	**Reserved**
5	0h RO	**Excessive Collisions (EXCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Excessive collision is sensed.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Late Collision (LCOL):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No collision. 0x1 (ACTIVE): Late collision is sensed.
3	0h RO	**Excessive Deferral (EXDEF):** When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Excessive deferral. 0x1 (ACTIVE): Excessive deferral.
2	0h RO	**Loss of Carrier (LCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): Loss of carrier.
1	0h RO	**No Carrier (NCARR):** When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Carrier is present. 0x1 (ACTIVE): No carrier.
0	0h RO	**Transmit Jabber Timeout (TJT):** This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Transmit Jabber Timeout. 0x1 (ACTIVE): Transmit Jabber Timeout occurred.

14.20.3.31 MAC_PMT_CONTROL_STATUS — Offset 502200C0h

The PMT Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	502200C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Remote Wake-Up Packet Filter Register Pointer Reset (RWKFILTRST):** When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-Up Packet Filter Register Pointer is not Reset. 0x1 (ENABLE): Remote Wake-Up Packet Filter Register Pointer is Reset.
30:29	0h RO	**Reserved**
28:24	00h RO	**Remote Wake-up FIFO Pointer (RWKPTR):** This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	0h RO	**Reserved**
10	0h RW	**Remote Wake-up Packet Forwarding Enable (RWKPFE):** When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Remote Wake-up Packet Forwarding is disabled. 0x1 (ENABLE): Remote Wake-up Packet Forwarding is enabled.
9	0h RW	**Global Unicast (GLBLUCAST):** When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. 0x0 (DISABLE): Global unicast is disabled. 0x1 (ENABLE): Global unicast is enabled.
8:7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Remote Wake-Up Packet Received (RWKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Remote wake-up packet is received. 0x1 (ACTIVE): Remote wake-up packet is received.
5	0h RO	**Magic Packet Received (MGKPRCVD):** When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): No Magic packet is received. 0x1 (ACTIVE): Magic packet is received.
4:3	0h RO	**Reserved**
2	0h RW	**Remote Wake-Up Packet Enable (RWKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. 0x0 (DISABLE): Remote wake-up packet is disabled. 0x1 (ENABLE): Remote wake-up packet is enabled.
1	0h RW	**Magic Packet Enable (MGKPKTEN):** When this bit is set, a power management event is generated when the MAC receives a magic packet. 0x0 (DISABLE): Magic Packet is disabled. 0x1 (ENABLE): Magic Packet is enabled.
0	0h RW	**Power Down (PWRDWN):** When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Power down is disabled. 0x1 (ENABLE): Power down is enabled.

14.20.3.32 MAC_RWK_PACKET_FILTER — Offset 502200C4h

The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight, sixteen or thirty-two register values in MAC_RWK_Packet_Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg31 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC_PMT_Control_Status register. The Remote Wakeup Filters are arranged in blocks of 4 filters each and each such block

have eight 32-bit wide registers, viz. wkuppktfilter_reg0-7, wkuppktfilter_reg8-15, wkuppktfilter_reg16-23 and wkuppktfilter_reg24-31. The fields of Remote Wakeup Filter are described as follows: Filter i Byte Mask: The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3, .., 15) to determine whether or not a packet is a wake-up packet. - The MSB (31st bit) must be zero. - Bit j[30:0] is the byte mask. - If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored. Filter i Command: The 4-bit filter i command controls the filter i operation. - Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. - Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC-16 value. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". - Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. The details are provided below: -- The And_Previous bit setting is applicable within a set of 4 filters. -- Setting of And_Previous bit of filter that is not enabled has no effect, that is setting And_Previous bit of lowest number filter in the set of 4 filters has no effect. For example, setting of And_Previous bit of Filter 0 has no effect. -- If And_Previous bit is set for filter to form AND chained filter, the AND chain breaks at the point any filter is not enabled. For example: If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set) but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result ANDed with Filter 3 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 2 is not enabled (bit 0 in Filter 2 command is reset), then since setting of Filter 2 And_Previous bit has no effect only Filter 1 result ORed with Filter 3 result is considered. -- If filters chained by And_Previous bit setting have complementary programming, then a frame might never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type. - Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled. Filter i Offset: The filter i offset register defines the offset (within the packet) from which the filter i examines the packets. - This 8-bit pattern-offset is the offset for the filter i first byte to be examined. - The minimum allowed offset is 12, which refers to the 13th byte of the packet. - The offset value 0 refers to the first byte of the packet. Filter i CRC-16: The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register. - The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1 - Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following: -- 32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC-16 calculation. -- 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations.

Type	Size	Offset	Default
MMIO	32 bit	502200C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**RWK Packet Filter (WKUPFRMFTR):** This field contains the various controls of RWK Packet filter.

14.20.3.33 MAC_LPI_CONTROL_STATUS — Offset 502200D0h

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

Type	Size	Offset	Default
MMIO	32 bit	502200D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**LPI Tx Clock Stop Enable (LPITCSE):** When this bit is set, the MAC indicates that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not indicate that the Tx clock to MAC can be stopped after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. 0x0 (DISABLE): LPI Tx Clock Stop is disabled. 0x1 (ENABLE): LPI Tx Clock Stop is enabled.
20	0h RW	**LPI Timer Enable (LPIATE):** This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. 0x0 (DISABLE): LPI Timer is disabled. 0x1 (ENABLE): LPI Timer is enabled.
19	0h RW	**LPI Tx Automate (LPITXA):** This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. 0x0 (DISABLE): LPI Tx Automate is disabled. 0x1 (ENABLE): LPI Tx Automate is enabled.
18	0h RW	**PHY Link Status Enable (PLSEN):** This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. 0x0 (DISABLE): PHY Link Status is disabled. 0x1 (ENABLE): PHY Link Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**PHY Link Status (PLS):** This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. 0x0 (DISABLE): link is down. 0x1 (ENABLE): link is okay (UP).
16	0h RW	**LPI Enable (LPIEN):** When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. 0x0 (DISABLE): LPI state is disabled. 0x1 (ENABLE): LPI state is enabled.
15:10	0h RO	**Reserved**
9	0h RO	**Receive LPI State (RLPIST):** When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Receive LPI state not detected. 0x1 (ACTIVE): Receive LPI state detected.
8	0h RO	**Transmit LPI State (TLPIST):** When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. 0x0 (INACTIVE): Transmit LPI state not detected. 0x1 (ACTIVE): Transmit LPI state detected.
7:4	0h RO	**Reserved**
3	0h RO	**Receive LPI Exit (RLPIEX):** When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI exit not detected. 0x1 (ACTIVE): Receive LPI exit detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Receive LPI Entry (RLPIEN):** When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. 0x0 (INACTIVE): Receive LPI entry not detected. 0x1 (ACTIVE): Receive LPI entry detected.
1	0h RO	**Transmit LPI Exit (TLPIEX):** When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI exit not detected. 0x1 (ACTIVE): Transmit LPI exit detected.
0	0h RO	**Transmit LPI Entry (TLPIEN):** When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Transmit LPI entry not detected. 0x1 (ACTIVE): Transmit LPI entry detected.

14.20.3.34 MAC_LPI_TIMERS_CONTROL — Offset 502200D4h

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

Type	Size	Offset	Default
MMIO	32 bit	502200D4h	03E80000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:16	3E8h RW	**LPI LS Timer (LST):** This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	0000h RW	**LPI TW Timer (TWT):** This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

14.20.3.35 MAC_LPI_ENTRY_TIMER — Offset 502200D8h

This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	502200D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:3	00000h RW	**LPI Entry Timer (LPIET):** This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	0h RO	**Reserved**

14.20.3.36 MAC_1US_TIC_COUNTER — Offset 502200DCh

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.

Type	Size	Offset	Default
MMIO	32 bit	502200DCh	00000063h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	063h RW	**1US TIC Counter (TIC_1US_CNTR):** The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

14.20.3.37 MAC_PHYIF_CONTROL_STATUS — Offset 502200F8h

The PHY Interface Control and Status register indicates the status signals received by the SGMII, RGMII, or SMII interface (selected at reset) from the PHY. This register is optional.

Type	Size	Offset	Default
MMIO	32 bit	502200F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO	**Link Status (LNKSTS):** This bit indicates whether the link is up (1'b1) or down (1'b0). 0x0 (INACTIVE): Link down. 0x1 (ACTIVE): Link up.
18:17	0h RO	**Link Speed (LNKSPEED):** This bit indicates the current speed of the link. 0x0 (M_2500K): 2.5 MHz. 0x1 (M_25M): 25 MHz. 0x2 (M_125M): 125 MHz. 0x3 (RSVD): Reserved.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**Link Mode (LNKMOD):** This bit indicates the current mode of operation of the link. 0x0 (HDUPLX): Half-duplex mode. 0x1 (FDUPLX): Full-duplex mode.
15:2	0h RO	**Reserved**
1	0h RW	**Link Up or Down (LUD):** This bit indicates whether the link is up or down during transmission of configuration in the RGMII or SGMII interface. 0x0 (LINKDOWN): Link down. 0x1 (LINKUP): Link up.
0	0h RW	**Transmit Configuration in RGMII or SGMII (TC):** When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: - "Reduced Gigabit Media Independent Interface" - "Serial Media Independent Interface" - "Serial Gigabit Media Independent Interface" 0x0 (DISABLE): Disable Transmit Configuration in RGMII or SGMII. 0x1 (ENABLE): Enable Transmit Configuration in RGMII or SGMII.

14.20.3.38 MAC_VERSION — Offset 50220110h

The version register identifies the version of the GbE Controller. This register contains two bytes: one that Synopsys uses to identify the core release number, and the other that you set while configuring the core.

Type	Size	Offset	Default
MMIO	32 bit	50220110h	00005152h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	51h RO	**USERVER:** Version code
7:0	52h RO	**SNPSVER:** Version code

14.20.3.39 MAC_DEBUG — Offset 50220114h

The Debug register provides the debug status of various MAC blocks.

Type	Size	Offset	Default
MMIO	32 bit	50220114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RO	**MAC Transmit Packet Controller Status (TFCSTS):** This field indicates the state of the MAC Transmit Packet Controller module. 0x0 (IDLE): Idle state. 0x1 (WAITING): Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over. 0x2 (GEN_TX_PAU): Generating and transmitting a Pause control packet (in full-duplex mode). 0x3 (TRNSFR): Transferring input packet for transmission.
16	0h RO	**MAC GMII or MII Transmit Protocol Engine Status (TPESTS):** When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Transmit Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Transmit Protocol Engine Status detected.
15:3	0h RO	**Reserved**
2:1	0h RO	**MAC Receive Packet Controller FIFO Status (RFCFCSTS):** When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	0h RO	**MAC GMII or MII Receive Protocol Engine Status (RPESTS):** When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected. 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected.

14.20.3.40 MAC_HW_FEATURE0 — Offset 5022011Ch

This register indicates the presence of first set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks. Note: All bits are set or reset according to the features selected while configuring the core in coreConsultant.

Type	Size	Offset	Default
MMIO	32 bit	5022011Ch	0EFD73F7h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	0h RO	**Active PHY Selected (ACTPHYSEL):** When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. 0x0 (GMII_MII): GMII or MII. 0x1 (RGMII): RGMII. 0x2 (SGMII): SGMII. 0x3 (TBI): TBI. 0x4 (RMII): RMII. 0x5 (RTBI): RTBI. 0x6 (SMII): SMII. 0x7 (REVMIII): RevMII.
27	1h RO	**Source Address or VLAN Insertion Enable (SAVLANINS):** This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected 0x0 (INACTIVE): Source Address or VLAN Insertion Enable option is not selected. 0x1 (ACTIVE): Source Address or VLAN Insertion Enable option is selected.
26:25	3h RO	**Timestamp System Time Source (TSSTSSEL):** This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INTRNL): Internal. 0x1 (EXTRNL): External. 0x2 (BOTH): Both. 0x3 (RSVD): Reserved.
24	0h RO	**MAC Addresses 64-127 Selected (MACADR64SEL):** This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected 0x0 (INACTIVE): MAC Addresses 64-127 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 64-127 Select option is selected.
23	1h RO	**MAC Addresses 32-63 Selected (MACADR32SEL):** This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected 0x0 (INACTIVE): MAC Addresses 32-63 Select option is not selected. 0x1 (ACTIVE): MAC Addresses 32-63 Select option is selected.
22:18	1Fh RO	**MAC Addresses 1-31 Selected (ADDMACADRSEL):** This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option
17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	1h RO	**Receive Checksum Offload Enabled (RXCOESEL):** This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected 0x0 (INACTIVE): Receive Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Receive Checksum Offload Enable option is selected.
15	0h RO	**Reserved**
14	1h RO	**Transmit Checksum Offload Enabled (TXCOESEL):** This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected 0x0 (INACTIVE): Transmit Checksum Offload Enable option is not selected. 0x1 (ACTIVE): Transmit Checksum Offload Enable option is selected.
13	1h RO	**Energy Efficient Ethernet Enabled (EEESEL):** This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected 0x0 (INACTIVE): Energy Efficient Ethernet Enable option is not selected. 0x1 (ACTIVE): Energy Efficient Ethernet Enable option is selected.
12	1h RO	**IEEE 1588-2008 Timestamp Enabled (TSSEL):** This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected 0x0 (INACTIVE): IEEE 1588-2008 Timestamp Enable option is not selected. 0x1 (ACTIVE): IEEE 1588-2008 Timestamp Enable option is selected.
11:10	0h RO	**Reserved**
9	1h RO	**ARP Offload Enabled (ARPOFFSEL):** This bit is set to 1 when the Enable IPv4 ARP Offload option is selected 0x0 (INACTIVE): ARP Offload Enable option is not selected. 0x1 (ACTIVE): ARP Offload Enable option is selected.
8	1h RO	**RMON Module Enable (MMCSEL):** This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected 0x0 (INACTIVE): RMON Module Enable option is not selected. 0x1 (ACTIVE): RMON Module Enable option is selected.
7	1h RO	**PMT Magic Packet Enable (MGKSEL):** This bit is set to 1 when the Enable Magic Packet Detection option is selected 0x0 (INACTIVE): PMT Magic Packet Enable option is not selected. 0x1 (ACTIVE): PMT Magic Packet Enable option is selected.
6	1h RO	**PMT Remote Wake-up Packet Enable (RWKSEL):** This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected 0x0 (INACTIVE): PMT Remote Wake-up Packet Enable option is not selected. 0x1 (ACTIVE): PMT Remote Wake-up Packet Enable option is selected.
5	1h RO	**SMA (MDIO) Interface (SMASEL):** This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected 0x0 (INACTIVE): SMA (MDIO) Interface not selected. 0x1 (ACTIVE): SMA (MDIO) Interface selected.
4	1h RO	**VLAN Hash Filter Selected (VLHASH):** This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected 0x0 (INACTIVE): VLAN Hash Filter not selected. 0x1 (ACTIVE): VLAN Hash Filter selected.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**PCS Registers (TBI, SGMII, or RTBI PHY interface) (PCSSEL):** This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected 0x0 (INACTIVE): No PCS Registers (TBI, SGMII, or RTBI PHY interface). 0x1 (ACTIVE): PCS Registers (TBI, SGMII, or RTBI PHY interface).
2	1h RO	**Half-duplex Support (HDSEL):** This bit is set to 1 when the half-duplex mode is selected 0x0 (INACTIVE): No Half-duplex support. 0x1 (ACTIVE): Half-duplex support.
1	1h RO	**1000 Mbps Support (GMIISEL):** This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 1000 Mbps support. 0x1 (ACTIVE): 1000 Mbps support.
0	1h RO	**10 or 100 Mbps Support (MIISEL):** This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation 0x0 (INACTIVE): No 10 or 100 Mbps support. 0x1 (ACTIVE): 10 or 100 Mbps support.

14.20.3.41 MAC_HW_FEATURE1 — Offset 50220120h

This register indicates the presence of second set of the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks. Note: All bits are set or reset according to the features selected while configuring the core in coreConsultant.

Type	Size	Offset	Default
MMIO	32 bit	50220120h	119F7A69h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	2h RO	**Total number of L3 or L4 Filters (L3L4FNUM):** This field indicates the total number of L3 or L4 filters: 0x0 (NOFILT): No L3 or L4 Filter. 0x1 (M_1FILT): 1 L3 or L4 Filter. 0x2 (M_2FILT): 2 L3 or L4 Filters. 0x3 (M_3FILT): 3 L3 or L4 Filters. 0x4 (M_4FILT): 4 L3 or L4 Filters. 0x5 (M_5FILT): 5 L3 or L4 Filters. 0x6 (M_6FILT): 6 L3 or L4 Filters. 0x7 (M_7FILT): 7 L3 or L4 Filters. 0x08 (M_8FILT): 8 L3 or L4 Filters.
26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	1h RO	**Hash Table Size (HASHTBLSZ):** This field indicates the size of the hash table: 0x0 (NO_HT): No hash table. 0x1 (M_64): 64. 0x2 (M_128): 128. 0x3 (M_256): 256.
23	1h RO	**One Step for PTP over UDP/IP Feature Enable (POUOST):** This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. 0x0 (INACTIVE): One Step for PTP over UDP/IP Feature is not selected. 0x1 (ACTIVE): One Step for PTP over UDP/IP Feature is selected.
22	0h RO	**Reserved**
21	0h RO	**Rx Side Only AV Feature Enable (RAVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. 0x0 (INACTIVE): Rx Side Only AV Feature is not selected. 0x1 (ACTIVE): Rx Side Only AV Feature is selected.
20	1h RO	**AV Feature Enable (AVSEL):** This bit is set to 1 when the Enable Audio Video Bridging option is selected. 0x0 (INACTIVE): AV Feature is not selected. 0x1 (ACTIVE): AV Feature is selected.
19	1h RO	**DMA Debug Registers Enable (DBGMEMA):** This bit is set to 1 when the Debug Mode Enable option is selected 0x0 (INACTIVE): DMA Debug Registers option is not selected. 0x1 (ACTIVE): DMA Debug Registers option is selected.
18	1h RO	**TCP Segmentation Offload Enable (TSOEN):** This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected 0x0 (INACTIVE): TCP Segmentation Offload Feature is not selected. 0x1 (ACTIVE): TCP Segmentation Offload Feature is selected.
17	1h RO	**Split Header Feature Enable (SPHEN):** This bit is set to 1 when the Enable Split Header Structure option is selected 0x0 (INACTIVE): Split Header Feature is not selected. 0x1 (ACTIVE): Split Header Feature is selected.
16	1h RO	**DCB Feature Enable (DCBEN):** This bit is set to 1 when the Enable Data Center Bridging option is selected 0x0 (INACTIVE): DCB Feature is not selected. 0x1 (ACTIVE): DCB Feature is selected.
15:14	1h RO	**Address Width. (ADDR64):** This field indicates the configured address width: 0x0 (M_32): 32. 0x1 (M_40): 40. 0x2 (M_48): 48. 0x3 (RSVD): Reserved.
13	1h RO	**IEEE 1588 High Word Register Enable (ADVTHWORD):** This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected 0x0 (INACTIVE): IEEE 1588 High Word Register option is not selected. 0x1 (ACTIVE): IEEE 1588 High Word Register option is selected.

Bit Range	Default & Access	Field Name (ID): Description
12	1h RO	**PTP Offload Enable (PTOEN):** This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. 0x0 (INACTIVE): PTP Offload feature is not selected. 0x1 (ACTIVE): PTP Offload feature is selected.
11	1h RO	**One-Step Timestamping Enable (OSTEN):** This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. 0x0 (INACTIVE): One-Step Timestamping feature is not selected. 0x1 (ACTIVE): One-Step Timestamping feature is selected.
10:6	08h RO	**MTL Transmit FIFO Size (TXFIFOSIZE):** This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (RSVD): Reserved.
5	1h RO	**Single Port RAM Enable (SPRAM):** This bit is set to 1 when the Use single port RAM Feature is selected. 0x0 (INACTIVE): Single Port RAM feature is not selected. 0x1 (ACTIVE): Single Port RAM feature is selected.
4:0	08h RO	**MTL Receive FIFO Size (RXFIFOSIZE):** This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: 0x0 (M_128B): 128 bytes. 0x1 (M_256B): 256 bytes. 0x2 (M_512B): 512 bytes. 0x3 (M_1024B): 1024 bytes. 0x4 (M_2048B): 2048 bytes. 0x5 (M_4096B): 4096 bytes. 0x6 (M_8192B): 8192 bytes. 0x7 (M_16384B): 16384 bytes. 0x08 (M_32KB): 32 KB. 0x09 (M_64KB): 64 KB. 0x0A (M_128KB): 128 KB. 0x0B (M_256KB): 256 KB. 0x0C (RSVD): Reserved.

14.20.3.42 MAC_HW_FEATURE2 — Offset 50220124h

This register indicates the presence of third set of the optional features or functions of the GbE ControllerGbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	50220124h	225D71C7h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	2h RO	**Number of Auxiliary Snapshot Inputs (AUXSNAPNUM):** This field indicates the number of auxiliary snapshot inputs: 0x0 (NO_AUXI): No auxiliary input. 0x1 (M_1_AUXI): 1 auxiliary input. 0x2 (M_2_AUXI): 2 auxiliary input. 0x3 (M_3_AUXI): 3 auxiliary input. 0x4 (M_4_AUXI): 4 auxiliary input. 0x5 (RSVD): Reserved.
27	0h RO	**Reserved**
26:24	2h RO	**Number of PPS Outputs (PPSOUTNUM):** This field indicates the number of PPS outputs: 0x0 (NO_PPSO): No PPS output. 0x1 (M_1_PPSO): 1 PPS output. 0x2 (M_2_PPSO): 2 PPS output. 0x3 (M_3_PPSO): 3 PPS output. 0x4 (M_4_PPSO): 4 PPS output. 0x5 (RSVD): Reserved.
23:22	3h RO	**Tx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (TDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
21:18	7h RO	**Number of DMA Transmit Channels (TXCHCNT):** This field indicates the number of DMA Transmit channels: 0x0 (M_1TXCH): 1 MTL Tx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1TDCSZ): 4. 0x1 (M_2TXCH): 2 MTL Tx Channels. 0x2 (M_2TDCSZ): 8. 0x2 (M_3TXCH): 3 MTL Tx Channels. 0x3 (M_3TDCSZ): 16. 0x3 (M_4TXCH): 4 MTL Tx Channels. 0x4 (M_5TXCH): 5 MTL Tx Channels. 0x5 (M_6TXCH): 6 MTL Tx Channels. 0x6 (M_7TXCH): 7 MTL Tx Channels. 0x7 (M_8TXCH): 8 MTL Tx Channels.

Bit Range	Default & Access	Field Name (ID): Description
17:16	3h RO	**Rx DMA Descriptor Cache Size in terms of 16 bytes descriptors: (RDCSZ):** 00 - Cache Not configured 01 - 4 16 bytes descriptor 10 - 8 16 bytes descriptor 11 - 16 16 bytes descriptor
15:12	7h RO	**Number of DMA Receive Channels (RXCHCNT):** This field indicates the number of DMA Receive channels: 0x0 (M_1RXCH): 1 MTL Rx Channel. 0x0 (NO_DCACHE): Desc Cache not configured. 0x1 (M_1RDCSZ): 4. 0x1 (M_2RXCH): 2 MTL Rx Channels. 0x2 (M_2RDCSZ): 8. 0x2 (M_3RXCH): 3 MTL Rx Channels. 0x3 (M_3RDCSZ): 16. 0x3 (M_4RXCH): 4 MTL Rx Channels. 0x4 (M_5RXCH): 5 MTL Rx Channels. 0x5 (M_6RXCH): 6 MTL Rx Channels. 0x6 (M_7RXCH): 7 MTL Rx Channels. 0x7 (M_8RXCH): 8 MTL Rx Channels.
11:10	0h RO	**Reserved**
9:6	7h RO	**Number of MTL Transmit Queues (TXQCNT):** This field indicates the number of MTL Transmit queues: 0x0 (M_1TXQ): 1 MTL Tx Queue. 0x1 (M_2TXQ): 2 MTL Tx Queues. 0x2 (M_3TXQ): 3 MTL Tx Queues. 0x3 (M_4TXQ): 4 MTL Tx Queues. 0x4 (M_5TXQ): 5 MTL Tx Queues. 0x5 (M_6TXQ): 6 MTL Tx Queues. 0x6 (M_7TXQ): 7 MTL Tx Queues. 0x7 (M_8TXQ): 8 MTL Tx Queues.
5:4	0h RO	**Reserved**
3:0	7h RO	**Number of MTL Receive Queues (RXQCNT):** This field indicates the number of MTL Receive queues: 0x0 (M_1RXQ): 1 MTL Rx Queue. 0x1 (M_2RXQ): 2 MTL Rx Queues. 0x2 (M_3RXQ): 3 MTL Rx Queues. 0x3 (M_4RXQ): 4 MTL Rx Queues. 0x4 (M_5RXQ): 5 MTL Rx Queues. 0x5 (M_6RXQ): 6 MTL Rx Queues. 0x6 (M_7RXQ): 7 MTL Rx Queues. 0x7 (M_8RXQ): 8 MTL Rx Queues.

14.20.3.43 MAC_HW_FEATURE3 — Offset 50220128h

This register indicates the presence of fourth set the optional features or functions of the GbE Controller. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	50220128h	2C395632h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	2h RO	**Automotive Safety Package (ASP):** Following are the encoding for the different Safety features 0x0 (NONE): No Safety features selected. 0x1 (ECC_ONLY): Only "ECC protection for external memory" feature is selected. 0x2 (AS_NPPE): All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature. 0x3 (AS_PPE): All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature.
27	1h RO	**Time Based Scheduling Enable (TBSSEL):** This bit is set to 1 when the Time Based Scheduling feature is selected. 0x0 (INACTIVE): Time Based Scheduling Enable feature is not selected. 0x1 (ACTIVE): Time Based Scheduling Enable feature is selected.
26	1h RO	**Frame Preemption Enable (FPESEL):** This bit is set to 1 when the Enable Frame preemption feature is selected. 0x0 (INACTIVE): Frame Preemption Enable feature is not selected. 0x1 (ACTIVE): Frame Preemption Enable feature is selected.
25:22	0h RO	**Reserved**
21:20	3h RO	**Width of the Time Interval field in the Gate Control List (ESTWID):** This field indicates the width of the Configured Time Interval Field 0x0 (NOWIDTH): Width not configured. 0x1 (WIDTH16): 16. 0x2 (WIDTH20): 20. 0x3 (WIDTH24): 24.
19:17	4h RO	**Depth of the Gate Control List (ESTDEP):** This field indicates the depth of Gate Control list expressed as Log2(512)-5 0x0 (NODEPTH): No Depth configured. 0x1 (DEPTH64): 64. 0x2 (DEPTH128): 128. 0x3 (DEPTH256): 256. 0x4 (DEPTH512): 512. 0x5 (DEPTH1024): 1024. 0x6 (RSVD): Reserved.
16	1h RO	**Enhancements to Scheduling Traffic Enable (ESTSEL):** This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. 0x0 (INACTIVE): Enable Enhancements to Scheduling Traffic feature is not selected. 0x1 (ACTIVE): Enable Enhancements to Scheduling Traffic feature is selected.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:13	2h RO	**Flexible Receive Parser Table Entries size (FRPES):** This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. 0x0 (M_64ENTR): 64 Entries. 0x1 (M_128ENTR): 128 Entries. 0x2 (M_256ENTR): 256 Entries. 0x3 (RSVD): Reserved.
12:11	2h RO	**Flexible Receive Parser Buffer size (FRPBS):** This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. 0x0 (M_64BYTES): 64 Bytes. 0x1 (M_128BYTES): 128 Bytes. 0x2 (M_256BYTES): 256 Bytes. 0x3 (RSVD): Reserved.
10	1h RO	**Flexible Receive Parser Selected (FRPSEL):** This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. 0x0 (INACTIVE): Flexible Receive Parser feature is not selected. 0x1 (ACTIVE): Flexible Receive Parser feature is selected.
9	1h RO	**Broadcast/Multicast Packet Duplication (PDUPSEL):** This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. 0x0 (INACTIVE): Broadcast/Multicast Packet Duplication feature is not selected. 0x1 (ACTIVE): Broadcast/Multicast Packet Duplication feature is selected.
8:6	0h RO	**Reserved**
5	1h RO	**Double VLAN Tag Processing Selected (DVLAN):** This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. 0x0 (INACTIVE): Double VLAN option is not selected. 0x1 (ACTIVE): Double VLAN option is selected.
4	1h RO	**Queue/Channel based VLAN tag insertion on Tx Enable (CBTISEL):** This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. 0x0 (INACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected. 0x1 (ACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is selected.
3	0h RO	**Reserved**
2:0	2h RO	**Number of Extended VLAN Tag Filters Enabled (NRVF):** This field indicates the Number of Extended VLAN Tag Filters selected: 0x0 (NO_ERVLAN): No Extended Rx VLAN Filters. 0x1 (M_4_ERVLAN): 4 Extended Rx VLAN Filters. 0x2 (M_8_ERVLAN): 8 Extended Rx VLAN Filters. 0x3 (M_16_ERVLAN): 16 Extended Rx VLAN Filters. 0x4 (M_24_ERVLAN): 24 Extended Rx VLAN Filters. 0x5 (M_32_ERVLAN): 32 Extended Rx VLAN Filters. 0x6 (RSVD): Reserved.

14.20.3.44 MAC_DPP_FSM_INTERRUPT_STATUS — Offset 50220140h

This register contains the status of Automotive Safety related Data Path Parity Errors, Interface Timeout Errors, FSM State Parity Errors and FSM State Timeout Errors. All the non-Reserved bits are cleared on read.

Type	Size	Offset	Default
MMIO	32 bit	50220140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**FSM State Parity Error Status (FSMPES):** This field when set indicates one of the FSMs State registers has a parity error detected. 0x0 (INACTIVE): FSM State Parity Error Status not detected. 0x1 (ACTIVE): FSM State Parity Error Status detected.
23:18	0h RO	**Reserved**
17	0h RW	**Slave Read/Write Timeout Error Status (SLVTES):** This field when set indicates that an Application/CSR Timeout has occurred on the AXI slave interface. 0x0 (INACTIVE): Slave Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Slave Read/Write Timeout Error Status detected.
16	0h RW	**Master Read/Write Timeout Error Status (MSTTES):** This field when set indicates that an Application/CSR Timeout has occurred on the master (AXI/AHB/ARI/ATI) interface. 0x0 (INACTIVE): Master Read/Write Timeout Error Status not detected. 0x1 (ACTIVE): Master Read/Write Timeout Error Status detected.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Status (PTES):** This field when set indicates that one of the PTP FSM Timeout has occurred. 0x0 (INACTIVE): PTP FSM Timeout Error Status not detected. 0x1 (ACTIVE): PTP FSM Timeout Error Status detected.
11	0h RW	**APP FSM Timeout Error Status (ATES):** This field when set indicates that one of the APP FSM Timeout has occurred. 0x0 (INACTIVE): APP FSM Timeout Error Status not detected. 0x1 (ACTIVE): APP FSM Timeout Error Status detected.
10	0h RW	**CSR FSM Timeout Error Status (CTES):** This field when set indicates that one of the CSR FSM Timeout has occurred. 0x0 (INACTIVE): CSR FSM Timeout Error Status not detected. 0x1 (ACTIVE): CSR FSM Timeout Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Rx FSM Timeout Error Status (RTES):** This field when set indicates that one of the Rx FSM Timeout has occurred. 0x0 (INACTIVE): Rx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Rx FSM Timeout Error Status detected.
8	0h RW	**Tx FSM Timeout Error Status (TTES):** This field when set indicates that one of the Tx FSM Timeout has occurred. 0x0 (INACTIVE): Tx FSM Timeout Error Status not detected. 0x1 (ACTIVE): Tx FSM Timeout Error Status detected.
7	0h RW	**AXI Slave Read data path Parity checker Error Status (ASRPES):** This bit when set indicates that parity error is detected at the AXI Slave read data interface. 0x0 (INACTIVE): AXI Slave Read data path Parity checker Error Status not detected. 0x1 (ACTIVE): AXI Slave Read data path Parity checker Error Status detected.
6	0h RW	**CSR Write data path Parity checker Error Status (CWPES):** This bit when set indicates that parity error is detected at the CSR write data interface on mci_wdata_i (or at PC8 checker as shown in AXI slave Interface Data path parity protection diagram). When EPSI bit of MTL_DPP_Control register is set and if any parity mis-match is detected on the input slave parity ports (or at PC7 checker in the AXI slave Interface Data path parity protection diagram) sets this bit to one. 0x0 (INACTIVE): CSR Write data path Parity checker Error Status not detected. 0x1 (ACTIVE): CSR Write data path Parity checker Error Status detected.
5	0h RW	**Application Receive interface data path Parity Error Status (ARPES):** This bit when set indicates that a parity error is detected by the hardware internally at the interface with the application. 0x0 (INACTIVE): Application Receive interface data path Parity Error Status not detected. 0x1 (ACTIVE): Application Receive interface data path Parity Error Status detected.
4	0h RW	**MTL TX Status data path Parity checker Error Status (MTSPES):** This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL TX Status data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL TX Status data path Parity checker Error Status detected.
3	0h RW	**MTL data path Parity checker Error Status (MPES):** This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): MTL data path Parity checker Error Status not detected. 0x1 (ACTIVE): MTL data path Parity checker Error Status detected.
2	0h RW	**Read Descriptor Parity checker Error Status (RDPES):** This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): Read Descriptor Parity checker Error Status not detected. 0x1 (ACTIVE): Read Descriptor Parity checker Error Status detected.
1	0h RW	**TSO data path Parity checker Error Status (TPES):** This bit when set indicates that a parity error is detected at the DMA TSO parity checker (or at PC2 as shown in Transmit data path parity protection diagram). 0x0 (INACTIVE): TSO data path Parity checker Error Status not detected. 0x1 (ACTIVE): TSO data path Parity checker Error Status detected.

14.20.3.45 MAC_FSM_CONTROL — Offset 50220148h

This register is used to control the FSM State parity and timeout error injection in Debug mode.

Type	Size	Offset	Default
MMIO	32 bit	50220148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**PTP Large/Normal Mode Select (PLGRNML):** This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for PTP domain. 0x1 (ENABLE): large mode tic generation is used for PTP domain.
27	0h RW	**APP Large/Normal Mode Select (ALGRNML):** This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for APP domain. 0x1 (ENABLE): large mode tic generation is used for APP domain.
26	0h RW	**CSR Large/Normal Mode Select (CLGRNML):** This field when set indicates that large mode tic generation is used for CSR domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for CSR domain. 0x1 (ENABLE): large mode tic generation is used for CSR domain.
25	0h RW	**Rx Large/Normal Mode Select (RLGRNML):** This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Rx domain. 0x1 (ENABLE): large mode tic generation is used for Rx domain.
24	0h RW	**Tx Large/Normal Mode Select (TLGRNML):** This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used. 0x0 (DISABLE): normal mode tic generation is used for Tx domain. 0x1 (ENABLE): large mode tic generation is used for Tx domain.
23:21	0h RO	**Reserved**
20	0h RW	**PTP FSM Parity Error Injection (PPEIN):** This field when set indicates that Error Injection for PTP FSM Parity is enabled. 0x0 (DISABLE): PTP FSM Parity Error Injection is disabled. 0x1 (ENABLE): PTP FSM Parity Error Injection is enabled.
19	0h RW	**APP FSM Parity Error Injection (APEIN):** This field when set indicates that Error Injection for APP FSM Parity is enabled. 0x0 (DISABLE): APP FSM Parity Error Injection is disabled. 0x1 (ENABLE): APP FSM Parity Error Injection is enabled.
18	0h RW	**CSR FSM Parity Error Injection (CPEIN):** This field when set indicates that Error Injection for CSR Parity is enabled. 0x0 (DISABLE): CSR FSM Parity Error Injection is disabled. 0x1 (ENABLE): CSR FSM Parity Error Injection is enabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Rx FSM Parity Error Injection (RPEIN):** This field when set indicates that Error Injection for RX FSM Parity is enabled. 0x0 (DISABLE): Rx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Rx FSM Parity Error Injection is enabled.
16	0h RW	**Tx FSM Parity Error Injection (TPEIN):** This field when set indicates that Error Injection for TX FSM Parity is enabled. 0x0 (DISABLE): Tx FSM Parity Error Injection is disabled. 0x1 (ENABLE): Tx FSM Parity Error Injection is enabled.
15:13	0h RO	**Reserved**
12	0h RW	**PTP FSM Timeout Error Injection (PTEIN):** This field when set indicates that Error Injection for PTP FSM timeout is enabled. 0x0 (DISABLE): PTP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): PTP FSM Timeout Error Injection is enabled.
11	0h RW	**APP FSM Timeout Error Injection (ATEIN):** This field when set indicates that Error Injection for APP FSM timeout is enabled. 0x0 (DISABLE): APP FSM Timeout Error Injection is disabled. 0x1 (ENABLE): APP FSM Timeout Error Injection is enabled.
10	0h RW	**CSR FSM Timeout Error Injection (CTEIN):** This field when set indicates that Error Injection for CSR timeout is enabled. 0x0 (DISABLE): CSR FSM Timeout Error Injection is disabled. 0x1 (ENABLE): CSR FSM Timeout Error Injection is enabled.
9	0h RW	**Rx FSM Timeout Error Injection (RTEIN):** This field when set indicates that Error Injection for RX FSM timeout is enabled. 0x0 (DISABLE): Rx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Rx FSM Timeout Error Injection is enabled.
8	0h RW	**Tx FSM Timeout Error Injection (TTEIN):** This field when set indicates that Error Injection for TX FSM timeout is enabled. 0x0 (DISABLE): Tx FSM Timeout Error Injection is disabled. 0x1 (ENABLE): Tx FSM Timeout Error Injection is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**PRTYEN:** This bit when set indicates that the FSM parity feature is enabled. 0x0 (DISABLE): FSM Parity feature is disabled. 0x1 (ENABLE): FSM Parity feature is enabled.
0	0h RW	**TMOUTEN:** This bit when set indicates that the FSM timeout feature is enabled. 0x0 (DISABLE): FSM timeout feature is disabled. 0x1 (ENABLE): FSM timeout feature is enabled.

14.20.3.46 MAC_FSM_ACT_TIMER — Offset 5022014Ch

This register is used to select the FSM and Interface Timeout values.

Type	Size	Offset	Default
MMIO	32 bit	5022014Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**LTMRMD:** This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
19:16	0h RW	**NTMRMD:** This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given below 0x0 (DISABLE): Timer disabled. 0x1 (M_1MICRO_SEC): 1us. 0x2 (M_4MILLI_SEC): 1.024ms (~4ms). 0x3 (M_16MILLI_SEC): 16.384ms (~16ms). 0x4 (M_64MILLI_SEC): 65.536ms (~64ms). 0x5 (M_256MILLI_SEC): 262.144ms (~256ms). 0x6 (M_1SEC): 1.048sec (~1sec). 0x7 (M_4SEC): 4.194sec (~4sec). 0x08 (M_16SEC): 16.777sec (~16sec). 0x09 (M_32SEC): 33.554sec (~32sec). 0x0A (M_64SEC): 67.108sec (~64sec). 0x0B (RSVD): Reserved.
15:10	0h RO	**Reserved**
9:0	000h RW	**TMR:** This field indicates the number of CSR clocks required to generate 1us tic.

14.20.3.47 SNPS_SCS_REG1 — Offset 50220150h

Synopsys Reserved Register

Type	Size	Offset	Default
MMIO	32 bit	50220150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Reserved**

14.20.3.48 MAC_MDIO_ADDRESS — Offset 50220200h

The MDIO Address register controls the management cycles to external PHY through a management interface.

Type	Size	Offset	Default
MMIO	32 bit	50220200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**Preamble Suppression Enable (PSE):** When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. 0x0 (DISABLE): Preamble Suppression disabled. 0x1 (ENABLE): Preamble Suppression enabled.
26	0h RW	**Back to Back transactions (BTB):** When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. 0x0 (DISABLE): Back to Back transactions disabled. 0x1 (ENABLE): Back to Back transactions enabled.

Bit Range	Default & Access	Field Name (ID): Description
25:21	00h RW	**Physical Layer Address (PA):** This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	00h RW	**Register/Device Address (RDA):** These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	0h RO	**Reserved**
14:12	0h RW	**Number of Trailing Clocks (NTC):** This field controls the number of trailing clock cycles generated on the MDIO Clock (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	0h RW	**CSR Clock Range (CR):** The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: - 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 - 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 - 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 - 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 - 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 - 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 - 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 - 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz freqency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: - 1000: CSR clock/4 - 1001: CSR clock/6 - 1010: CSR clock/8 - 1011: CSR clock/10 - 1100: CSR clock/12 - 1101: CSR clock/14 - 1110: CSR clock/16 - 1111: CSR clock/18
7:5	0h RO	**Reserved**
4	0h RW	**Skip Address Packet (SKAP):** When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0x0 (DISABLE): Skip Address Packet is disabled. 0x1 (ENABLE): Skip Address Packet is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GMII Operation Command 1 (GOC_1):** This bit is higher bit of the operation command to the PHY or GOC_1 and GOC_O are encoded as follows: - 00: Reserved - 01: Write - 10: Post Read Increment Address for Clause 45 PHY - 11: Read When Clause 22 PHY is enabled, only Write and Read commands are valid. 0x0 (DISABLE): GMII Operation Command 1 is disabled. 0x1 (ENABLE): GMII Operation Command 1 is enabled.
2	0h RW	**GMII Operation Command 0 (GOC_0):** This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. 0x0 (DISABLE): GMII Operation Command 0 is disabled. 0x1 (ENABLE): GMII Operation Command 0 is enabled.
1	0h RW	**Clause 45 PHY Enable (C45E):** When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0x0 (DISABLE): Clause 45 PHY is disabled. 0x1 (ENABLE): Clause 45 PHY is enabled.
0	0h RW	**GMII Busy (GB):** The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDI field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): GMII Busy is disabled. 0x1 (ENABLE): GMII Busy is enabled.

14.20.3.49 MAC_MDIO_DATA — Offset 50220204h

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

Type	Size	Offset	Default
MMIO	32 bit	50220204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Register Address (RA):** This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	0000h RW	**GMII Data (GD):** This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

14.20.3.50 MAC_GPIO_CONTROL — Offset 50220208h

The GPIO Control register controls the GPIO.

Type	Size	Offset	Default
MMIO	32 bit	50220208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

14.20.3.51 MAC_GPIO_STATUS — Offset 5022020Ch

The General Purpose IO register provides the control to drive the following: up to 16 bits of output ports (GPO) and status of up to 16 input ports (GPIS).

Type	Size	Offset	Default
MMIO	32 bit	5022020Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW	**Trigger Snapshot (GPO1)**: Active-high signal. The rising edge of this signal triggers snapshot of current PMC ART and System timer values. The system timer value is stored into AUX FIFO. An interrupt is generated upon snapshotting. The PMC ART timer values is stored in 4x 16-bit ART snapshot register and is read through MDIO registers. MAC_GPIO[3] / MAC_GPIO[0] / PTP REF Clock to GbE MAC 0 / 0 / Reserved 0 / 1 / Reserved 1 / 0 / Reserved 1 / 1 / PSE PLL_PTP = 200MHz 19th bit and 16th bit are used for selecting Precision Time Protocol (PTP). This bits programming are used in GbE Time Synchronization CTS Test. - 19th Bit: MAC_GPIO[3] - 16th Bit: MAC_GPIO[0]
15:4	0h RO	**Reserved**
3:0	0h RW	**GPIS:** General Purpose Input Status. This field gives the status of the signals connected to the gpi_i port. This field is of the following types based on the setting of the corresponding GPIT field of MAC_GPIO_Control register: - Latched-Low (LL): This field is cleared when the corresponding gpi_i input becomes low. This field remains low until the application reads this field after which this field reflects the current value of gpi_i input. - Latched-High (LH): This field is set when the corresponding gpi_i input becomes high. This field remains high until the application reads this field after which this field reflects the current value of gpi_i input. The number of bits available in this field depends on the GP Input Signal Width option. Other bits are not used (reserved and always reset). 0000H

14.20.3.52 MAC_ARP_ADDRESS — Offset 50220210h

The ARP Address register contains the IPv4 Destination Address of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50220210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ARP Protocol Address (ARPPA):** This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

14.20.3.53 MAC_CSR_SW_CTRL — Offset 50220230h

This register contains SW programmable controls for changing the CSR access response and status bits clearing.

Type	Size	Offset	Default
MMIO	32 bit	50220230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Slave Error Response Enable (SEEN):** When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space. 0x0 (DISABLE): Slave Error Response is disabled. 0x1 (ENABLE): Slave Error Response is enabled.
7:1	0h RO	**Reserved**
0	0h RW	**Register Clear on Write 1 Enable (RCWE):** When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. 0x0 (DISABLE): Register Clear on Write 1 is disabled. 0x1 (ENABLE): Register Clear on Write 1 is enabled.

14.20.3.54 MAC_FPE_CTRL_STS — Offset 50220234h

This register controls the operation of Frame Preemption.

Type	Size	Offset	Default
MMIO	32 bit	50220234h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Transmitted Respond Frame (TRSP):** Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Respond Frame. 0x1 (ACTIVE): transmitted Respond Frame.
18	0h RW	**Transmitted Verify Frame (TVER):** Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not transmitted Verify Frame. 0x1 (ACTIVE): transmitted Verify Frame.
17	0h RW	**Received Respond Frame (RRSP):** Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Respond Frame. 0x1 (ACTIVE): Received Respond Frame.
16	0h RW	**Received Verify Frame (RVER):** Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Not received Verify Frame. 0x1 (ACTIVE): Received Verify Frame.
15:4	0h RO	**Reserved**
3	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Send Respond mPacket (SRSP):** When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Respond mPacket is disabled. 0x1 (ENABLE): Send Respond mPacket is enabled.
1	0h RW	**Send Verify mPacket (SVER):** When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Send Verify mPacket is disabled. 0x1 (ENABLE): Send Verify mPacket is enabled.
0	0h RW	**Enable Tx Frame Preemption (EFPE):** When set Frame Preemption Tx functionality is enabled. 0x0 (DISABLE): Tx Frame Preemption is disabled. 0x1 (ENABLE): Tx Frame Preemption is enabled.

14.20.3.55 MAC_EXT_CFG1 — Offset 50220238h

This register contains Split mode control field and offset field for Split Header feature.

Type	Size	Offset	Default
MMIO	32 bit	50220238h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h RW	**Split Mode (SPLM):** These bits indicate the mode of splitting the incoming Rx packets. They are 0x0 (L3L4): Split at L3/L4 header. 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame. 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped. 0x3 (RSVD): Reserved.
7	0h RO	**Reserved**
6:0	02h RW	**Split Offset (SPLOFST):** These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

14.20.3.56 MAC_PRESN_TIME_NS — Offset 50220240h

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns Exists when DWC_EQOS_FLEXI_PPS_OUT_EN is configured

Type	Size	Offset	Default
MMIO	32 bit	50220240h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MAC 1722 Presentation Time in ns (MPTN):** These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns

14.20.3.57 MAC_PRESN_TIME_UPDT — Offset 50220244h

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). Exists when DWC_EQOS_FLEXI_PPS_OUT_EN is configured

Type	Size	Offset	Default
MMIO	32 bit	50220244h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MAC 1722 Presentation Time Update (MPTU):** This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction

14.20.3.58 MAC_ADDRESS0_HIGH — Offset 50220300h

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if

0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] of the MAC Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50220300h	8000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Address Enable (AE):** This bit is always set to 1. 0x0 (DISABLE): INVALID : This bit must be always set to 1. 0x1 (ENABLE): This bit is always set to 1.
30:24	0h RO	**Reserved**
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	FFFFh RW	**MAC Address0[47:32] (ADDRHI):** This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

14.20.3.59 MAC_ADDRESS0_LOW — Offset 50220304h

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	50220304h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address0[31:0] (ADDRLO):** This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

14.20.3.60 MAC_ADDRESS1_HIGH — Offset 50220308h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	50220308h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30	0h RW	**Source Address (SA):** When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet. 0x0 (DA): Compare with Destination Address. 0x1 (SA): Compare with Source Address.
29:24	00h RW	**Mask Byte Control (MBC):** These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	00h RW	**DMA Channel Select (DCS):** If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**MAC Address1 [47:32] (ADDRHI):** This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

14.20.3.61 MAC_ADDRESS1_LOW — Offset 5022030Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	5022030Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address1 [31:0] (ADDRLO):** This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

14.20.3.62 MAC_ADDRESS2_HIGH — Offset 50220310h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.63 MAC_ADDRESS2_LOW — Offset 50220314h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.64 MAC_ADDRESS3_HIGH — Offset 50220318h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.65 MAC_ADDRESS3_LOW — Offset 5022031Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.66 MAC_ADDRESS4_HIGH — Offset 50220320h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.67 MAC_ADDRESS4_LOW — Offset 50220324h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.68 MAC_ADDRESS5_HIGH — Offset 50220328h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.69 MAC_ADDRESS5_LOW — Offset 5022032Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.70 MAC_ADDRESS6_HIGH — Offset 50220330h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.71 MAC_ADDRESS6_LOW — Offset 50220334h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.72 MAC_ADDRESS7_HIGH — Offset 50220338h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.73 MAC_ADDRESS7_LOW — Offset 5022033Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.74 MAC_ADDRESS8_HIGH — Offset 50220340h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.75 MAC_ADDRESS8_LOW — Offset 50220344h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.76 MAC_ADDRESS9_HIGH — Offset 50220348h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.77 MAC_ADDRESS9_LOW — Offset 5022034Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.78 MAC_ADDRESS10_HIGH — Offset 50220350h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.79 MAC_ADDRESS10_LOW — Offset 50220354h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.80 MAC_ADDRESS11_HIGH — Offset 50220358h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.81 MAC_ADDRESS11_LOW — Offset 5022035Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.82 MAC_ADDRESS12_HIGH — Offset 50220360h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.83 MAC_ADDRESS12_LOW — Offset 50220364h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.84 MAC_ADDRESS13_HIGH — Offset 50220368h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.85 MAC_ADDRESS13_LOW — Offset 5022036Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.86 MAC_ADDRESS14_HIGH — Offset 50220370h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.87 MAC_ADDRESS14_LOW — Offset 50220374h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.88 MAC_ADDRESS15_HIGH — Offset 50220378h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.89 MAC_ADDRESS15_LOW — Offset 5022037Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.90 MAC_ADDRESS16_HIGH — Offset 50220380h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.91 MAC_ADDRESS16_LOW — Offset 50220384h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.92 MAC_ADDRESS17_HIGH — Offset 50220388h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.93 MAC_ADDRESS17_LOW — Offset 5022038Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.94 MAC_ADDRESS18_HIGH — Offset 50220390h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.95 MAC_ADDRESS18_LOW — Offset 50220394h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.96 MAC_ADDRESS19_HIGH — Offset 50220398h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.97 MAC_ADDRESS19_LOW — Offset 5022039Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.98 MAC_ADDRESS20_HIGH — Offset 502203A0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.99 MAC_ADDRESS20_LOW — Offset 502203A4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.100MAC_ADDRESS21_HIGH — Offset 502203A8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.101MAC_ADDRESS21_LOW — Offset 502203ACh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.102MAC_ADDRESS22_HIGH — Offset 502203B0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.103MAC_ADDRESS22_LOW — Offset 502203B4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.104MAC_ADDRESS23_HIGH — Offset 502203B8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.105MAC_ADDRESS23_LOW — Offset 502203BCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.106MAC_ADDRESS24_HIGH — Offset 502203C0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.107MAC_ADDRESS24_LOW — Offset 502203C4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.108MAC_ADDRESS25_HIGH — Offset 502203C8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.109MAC_ADDRESS25_LOW — Offset 502203CCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.110MAC_ADDRESS26_HIGH — Offset 502203D0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.111MAC_ADDRESS26_LOW — Offset 502203D4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.112MAC_ADDRESS27_HIGH — Offset 502203D8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.113MAC_ADDRESS27_LOW — Offset 502203DCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.114MAC_ADDRESS28_HIGH — Offset 502203E0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.115MAC_ADDRESS28_LOW — Offset 502203E4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.116MAC_ADDRESS29_HIGH — Offset 502203E8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.117MAC_ADDRESS29_LOW — Offset 502203ECh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.118MAC_ADDRESS30_HIGH — Offset 502203F0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.119MAC_ADDRESS30_LOW — Offset 502203F4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.120MAC_ADDRESS31_HIGH — Offset 502203F8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 50220308h.

14.20.3.121MAC_ADDRESS31_LOW — Offset 502203FCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 5022030Ch.

14.20.3.122MAC_ADDRESS32_HIGH — Offset 50220400h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	50220400h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Enable (AE):** When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0x0 (DISABLE): Address is ignored. 0x1 (ENABLE): Address is enabled.
30:19	0h RO	**Reserved**
18:16	0h RW	**DMA Channel Select (DCS):** This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**MAC Address32 [47:32] (ADDRHI):** This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

14.20.3.123MAC_ADDRESS32_LOW — Offset 50220404h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	50220404h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**MAC Address32 [31:0] (ADDRLO):** This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

14.20.3.124MAC_ADDRESS33_HIGH — Offset 50220408h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.125MAC_ADDRESS33_LOW — Offset 5022040Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.126MAC_ADDRESS34_HIGH — Offset 50220410h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.127MAC_ADDRESS34_LOW — Offset 50220414h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.128MAC_ADDRESS35_HIGH — Offset 50220418h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.129MAC_ADDRESS35_LOW — Offset 5022041Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.130MAC_ADDRESS36_HIGH — Offset 50220420h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.131MAC_ADDRESS36_LOW — Offset 50220424h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.132MAC_ADDRESS37_HIGH — Offset 50220428h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.133MAC_ADDRESS37_LOW — Offset 5022042Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.134MAC_ADDRESS38_HIGH — Offset 50220430h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.135MAC_ADDRESS38_LOW — Offset 50220434h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.136MAC_ADDRESS39_HIGH — Offset 50220438h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.137MAC_ADDRESS39_LOW — Offset 5022043Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.138MAC_ADDRESS40_HIGH — Offset 50220440h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.139MAC_ADDRESS40_LOW — Offset 50220444h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.140MAC_ADDRESS41_HIGH — Offset 50220448h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.141MAC_ADDRESS41_LOW — Offset 5022044Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.142MAC_ADDRESS42_HIGH — Offset 50220450h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.143MAC_ADDRESS42_LOW — Offset 50220454h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.144MAC_ADDRESS43_HIGH — Offset 50220458h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.145MAC_ADDRESS43_LOW — Offset 5022045Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.146MAC_ADDRESS44_HIGH — Offset 50220460h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.147MAC_ADDRESS44_LOW — Offset 50220464h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.148MAC_ADDRESS45_HIGH — Offset 50220468h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.149MAC_ADDRESS45_LOW — Offset 5022046Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.150MAC_ADDRESS46_HIGH — Offset 50220470h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.151MAC_ADDRESS46_LOW — Offset 50220474h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.152MAC_ADDRESS47_HIGH — Offset 50220478h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.153MAC_ADDRESS47_LOW — Offset 5022047Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.154MAC_ADDRESS48_HIGH — Offset 50220480h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.155MAC_ADDRESS48_LOW — Offset 50220484h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.156MAC_ADDRESS49_HIGH — Offset 50220488h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.157MAC_ADDRESS49_LOW — Offset 5022048Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.158MAC_ADDRESS50_HIGH — Offset 50220490h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.159MAC_ADDRESS50_LOW — Offset 50220494h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.160MAC_ADDRESS51_HIGH — Offset 50220498h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.161MAC_ADDRESS51_LOW — Offset 5022049Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.162MAC_ADDRESS52_HIGH — Offset 502204A0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.163MAC_ADDRESS52_LOW — Offset 502204A4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.164MAC_ADDRESS53_HIGH — Offset 502204A8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.165MAC_ADDRESS53_LOW — Offset 502204ACh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.166MAC_ADDRESS54_HIGH — Offset 502204B0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.167MAC_ADDRESS54_LOW — Offset 502204B4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.168MAC_ADDRESS55_HIGH — Offset 502204B8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.169MAC_ADDRESS55_LOW — Offset 502204BCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.170MAC_ADDRESS56_HIGH — Offset 502204C0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.171MAC_ADDRESS56_LOW — Offset 502204C4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.172MAC_ADDRESS57_HIGH — Offset 502204C8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.173MAC_ADDRESS57_LOW — Offset 502204CCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.174MAC_ADDRESS58_HIGH — Offset 502204D0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.175MAC_ADDRESS58_LOW — Offset 502204D4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.176MAC_ADDRESS59_HIGH — Offset 502204D8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.177MAC_ADDRESS59_LOW — Offset 502204DCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.178MAC_ADDRESS60_HIGH — Offset 502204E0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.179MAC_ADDRESS60_LOW — Offset 502204E4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.180MAC_ADDRESS61_HIGH — Offset 502204E8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.181MAC_ADDRESS61_LOW — Offset 502204ECh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.182MAC_ADDRESS62_HIGH — Offset 502204F0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.183MAC_ADDRESS62_LOW — Offset 502204F4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.184MAC_ADDRESS63_HIGH — Offset 502204F8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 50220400h.

14.20.3.185MAC_ADDRESS63_LOW — Offset 502204FCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 50220404h.

14.20.3.186MMC_CONTROL — Offset 50220700h

This register establishes the operating mode of MMC.

Type	Size	Offset	Default
MMIO	32 bit	50220700h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Update MMC Counters for Dropped Broadcast Packets (UCDBC):** Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. 0x0 (DISABLE): Update MMC Counters for Dropped Broadcast Packets is disabled. 0x1 (ENABLE): Update MMC Counters for Dropped Broadcast Packets is enabled.
7:6	0h RO	**Reserved**
5	0h RW	**Full-Half Preset (CNTPRSTLVL):** When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. 0x0 (DISABLE): Full-Half Preset is disabled. 0x1 (ENABLE): Full-Half Preset is enabled.
4	0h RW	**Counters Preset (CNTPRST):** When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
3	0h RW	**MMC Counter Freeze (CNTFREEZ):** When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. 0x0 (DISABLE): MMC Counter Freeze is disabled. 0x1 (ENABLE): MMC Counter Freeze is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Reset on Read (RSTONRD):** When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. 0x0 (DISABLE): Reset on Read is disabled. 0x1 (ENABLE): Reset on Read is enabled.
1	0h RW	**Counter Stop Rollover (CNTSTOPRO):** When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0x0 (DISABLE): Counter Stop Rollover is disabled. 0x1 (ENABLE): Counter Stop Rollover is enabled.
0	0h RW	**Counters Reset (CNTRST):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.

14.20.3.187MMC_RX_INTERRUPT — Offset 50220704h

This register maintains the interrupts generated from all Receive statistics counters. The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur: - Receive statistic counters reach half of their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter). - Receive statistic counters cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit. Note: R_SS_RC means that this register bit is set internally, and it is cleared when the Counter register is read.

Type	Size	Offset	Default
MMIO	32 bit	50220704h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Receive LPI transition counter interrupt status (RXLPITRCIS):** This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Receive LPI microsecond counter interrupt status (RXLPIUSCIS):** This bit is set when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Receive Control Packet Counter Interrupt Status (RXCTRLPIS):** This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Control Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Control Packet Counter Interrupt Status detected.
24	0h RO	**MMC Receive Error Packet Counter Interrupt Status (RXRCVERRPIS):** This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Error Packet Counter Interrupt Status detected.
23	0h RO	**MMC Receive Watchdog Error Packet Counter Interrupt Status (RXWDOGPIS):** This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected.
22	0h RO	**MMC Receive VLAN Good Bad Packet Counter Interrupt Status (RXVLANGBPIS):** This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**MMC Receive FIFO Overflow Packet Counter Interrupt Status (RXFOVPIS):** This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status detected.
20	0h RO	**MMC Receive Pause Packet Counter Interrupt Status (RXPAUSPIS):** This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected.
19	0h RO	**MMC Receive Out Of Range Error Packet Counter Interrupt Status. (RXORANGEPIS):** This bit is set when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Out Of Range Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Receive Length Error Packet Counter Interrupt Status (RXLENERPIS):** This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Length Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Length Error Packet Counter Interrupt Status detected.
17	0h RO	**MMC Receive Unicast Good Packet Counter Interrupt Status (RXUCGPIS):** This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status detected.
16	0h RO	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (RX1024TMAXOCTGBPIS):** This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
15	0h RO	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (RX512T1023OCTGBPIS):** This bit is set when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status (RX256T511OCTGBPIS):** This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
13	0h RO	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status (RX128T255OCTGBPIS):** This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status (RX65T127OCTGBPIS):** This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status (RX64OCTGBPIS):** This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive Oversize Good Packet Counter Interrupt Status (RXOSIZEGPIS):** This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive Undersize Good Packet Counter Interrupt Status (RXUSIZEGPIS):** This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MMC Receive Jabber Error Packet Counter Interrupt Status (RXJABERPIS):** This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status detected.
7	0h RO	**MMC Receive Runt Packet Counter Interrupt Status (RXRUNTPIS):** This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Runt Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Runt Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive Alignment Error Packet Counter Interrupt Status (RXALGNERPIS):** This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive CRC Error Packet Counter Interrupt Status (RXCRCERPIS):** This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive Multicast Good Packet Counter Interrupt Status (RXMCGPIS):** This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive Broadcast Good Packet Counter Interrupt Status (RXBCGPIS):** This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive Good Octet Counter Interrupt Status (RXGOCTIS):** This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Octet Counter Interrupt Status detected.
1	0h RO	**MMC Receive Good Bad Octet Counter Interrupt Status (RXGBOCTIS):** This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status detected.
0	0h RO	**MMC Receive Good Bad Packet Counter Interrupt Status (RXGBPKTIS):** This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status detected.

14.20.3.188MMC_TX_INTERRUPT — Offset 50220708h

This register maintains the interrupts generated from all Transmit statistics counters. The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	50220708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**MMC Transmit LPI transition counter interrupt status (TXLPITRCIS):** This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI transition Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI transition Counter Interrupt Status detected.
26	0h RO	**MMC Transmit LPI microsecond counter interrupt status (TXLPIUSCIS):** This bit is set when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit LPI microsecond Counter Interrupt Status detected.
25	0h RO	**MMC Transmit Oversize Good Packet Counter Interrupt Status (TXOSIZEGPIS):** This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status detected.
24	0h RO	**MMC Transmit VLAN Good Packet Counter Interrupt Status (TXVLANGPIS):** This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status detected.
23	0h RO	**MMC Transmit Pause Packet Counter Interrupt Status (TXPAUSPIS):** This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**MMC Transmit Excessive Deferral Packet Counter Interrupt Status (TXEXDEFPIS):** This bit is set when the txexcessdef counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Deferral Packet Counter Interrupt Status detected.
21	0h RO	**MMC Transmit Good Packet Counter Interrupt Status (TXGPKTIS):** This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Packet Counter Interrupt Status detected.
20	0h RO	**MMC Transmit Good Octet Counter Interrupt Status (TXGOCTIS):** This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Octet Counter Interrupt Status detected.
19	0h RO	**MMC Transmit Carrier Error Packet Counter Interrupt Status (TXCARERPIS):** This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Carrier Error Packet Counter Interrupt Status detected.
18	0h RO	**MMC Transmit Excessive Collision Packet Counter Interrupt Status (TXEXCOLPIS):** This bit is set when the txexesscol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Excessive Collision Packet Counter Interrupt Status detected.
17	0h RO	**MMC Transmit Late Collision Packet Counter Interrupt Status (TXLATCOLPIS):** This bit is set when the txlatecol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Late Collision Packet Counter Interrupt Status detected.
16	0h RO	**MMC Transmit Deferred Packet Counter Interrupt Status (TXDEFPIS):** This bit is set when the txdeferred counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Deferred Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Status (TXMCOLGPIS):** This bit is set when the txmulticol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Status detected.
14	0h RO	**MMC Transmit Single Collision Good Packet Counter Interrupt Status (TXSCOLGPIS):** This bit is set when the txsinglecol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Single Collision Good Packet Counter Interrupt Status detected.
13	0h RO	**MMC Transmit Underflow Error Packet Counter Interrupt Status (TXUFLOWERPIS):** This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status (TXBCGBPIS):** This bit is set when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status detected.
11	0h RO	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Status (TXMCGBPIS):** The bit is set when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Status detected.
10	0h RO	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Status (TXUCGBPIS):** This bit is set when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status (TX1024TMAXOCTGBPIS):** This bit is set when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected.
8	0h RO	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status (TX512T1023OCTGBPIS):** This bit is set when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected.
7	0h RO	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status (TX256T511OCTGBPIS):** This bit is set when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected.
6	0h RO	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status (TX128T255OCTGBPIS):** This bit is set when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected.
5	0h RO	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status (TX65T127OCTGBPIS):** This bit is set when the tx65to127octets_gb counter reaches half the maximum value, and also when it reaches the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected.
4	0h RO	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status (TX64OCTGBPIS):** This bit is set when the tx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**MMC Transmit Multicast Good Packet Counter Interrupt Status (TXMCGPIS):** This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status detected.
2	0h RO	**MMC Transmit Broadcast Good Packet Counter Interrupt Status (TXBCGPIS):** This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status detected.
1	0h RO	**MMC Transmit Good Bad Packet Counter Interrupt Status (TXGBPKTIS):** This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status detected.
0	0h RO	**MMC Transmit Good Bad Octet Counter Interrupt Status (TXGBOCTIS):** This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status detected.

14.20.3.189MMC_RX_INTERRUPT_MASK — Offset 5022070Ch

This register maintains the masks for interrupts generated from all Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	5022070Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Receive LPI transition counter interrupt Mask (RXLPITRCIM):** Setting this bit masks the interrupt when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Receive LPI microsecond counter interrupt Mask (RXLPIUSCIM):** Setting this bit masks the interrupt when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive LPI microsecond counter interrupt Mask is enabled.
25	0h RW	**MMC Receive Control Packet Counter Interrupt Mask (RXCTRLPIM):** Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Control Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Control Packet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive Error Packet Counter Interrupt Mask (RXRCVERRPIM):** Setting this bit masks the interrupt when the rxrcverror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Error Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Receive Watchdog Error Packet Counter Interrupt Mask (RXWDOGPIM):** Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Receive VLAN Good Bad Packet Counter Interrupt Mask (RXVLANGBPIM):** Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive FIFO Overflow Packet Counter Interrupt Mask (RXFOVPIM):** Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**MMC Receive Pause Packet Counter Interrupt Mask (RXPAUSPIM):** Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive Out Of Range Error Packet Counter Interrupt Mask (RXORANGEPIM):** Setting this bit masks the interrupt when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Out Of Range Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive Length Error Packet Counter Interrupt Mask (RXLENERPIM):** Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Length Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Length Error Packet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Receive Unicast Good Packet Counter Interrupt Mask (RXUCGPIM):** Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask. (RX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
15	0h RW	**MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (RX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (RX256T511OCTGBPIM):** Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (RX128T255OCTGBPIM):** Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (RX65T127OCTGBPIM):** Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask (RX64OCTGBPIM):** Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Receive Oversize Good Packet Counter Interrupt Mask (RXOSIZEGPIM):** Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive Undersize Good Packet Counter Interrupt Mask (RXUSIZEGPIM):** Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive Jabber Error Packet Counter Interrupt Mask (RXJABERPIM):** Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive Runt Packet Counter Interrupt Mask (RXRUNTPIM):** Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Runt Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Runt Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive Alignment Error Packet Counter Interrupt Mask (RXALGNERPIM):** Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive CRC Error Packet Counter Interrupt Mask (RXCRCERPIM):** Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**MMC Receive Multicast Good Packet Counter Interrupt Mask (RXMCGPIM):** Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Receive Broadcast Good Packet Counter Interrupt Mask (RXBCGPIM):** Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Receive Good Octet Counter Interrupt Mask (RXGOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Octet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive Good Bad Octet Counter Interrupt Mask (RXGBOCTIM):** Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive Good Bad Packet Counter Interrupt Mask (RXGBPKTIM):** Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is enabled.

14.20.3.190MMC_TX_INTERRUPT_MASK — Offset 50220710h

This register maintains the masks for interrupts generated from all Transmit statistics counters. The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	50220710h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**MMC Transmit LPI transition counter interrupt Mask (TXLPITRCIM):** Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI transition counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI transition counter interrupt Mask is enabled.
26	0h RW	**MMC Transmit LPI microsecond counter interrupt Mask (TXLPIUSCIM):** Setting this bit masks the interrupt when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit LPI microsecond counter interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit LPI microsecond counter interrupt Mask is enabled.
25	0h RW	**MMC Transmit Oversize Good Packet Counter Interrupt Mask (TXOSIZEGPIM):** Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Transmit VLAN Good Packet Counter Interrupt Mask (TXVLANGPIM):** Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Transmit Pause Packet Counter Interrupt Mask (TXPAUSPIM):** Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled.
22	0h RW	**MMC Transmit Excessive Deferral Packet Counter Interrupt Mask (TXEXDEFPIM):** Setting this bit masks the interrupt when the txexcessdef counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Deferral Packet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Transmit Good Packet Counter Interrupt Mask (TXGPKTIM):** Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**MMC Transmit Good Octet Counter Interrupt Mask (TXGOCTIM):** Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Transmit Carrier Error Packet Counter Interrupt Mask (TXCARERPIM):** Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Transmit Excessive Collision Packet Counter Interrupt Mask (TXEXCOLPIM):** Setting this bit masks the interrupt when the txexcesscol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Excessive Collision Packet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Transmit Late Collision Packet Counter Interrupt Mask (TXLATCOLPIM):** Setting this bit masks the interrupt when the txlatecol counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Late Collision Packet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Transmit Deferred Packet Counter Interrupt Mask (TXDEFPIM):** Setting this bit masks the interrupt when the txdeferred counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Deferred Packet Counter Interrupt Mask is enabled.
15	0h RW	**MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask (TXMCOLGPIM):** Setting this bit masks the interrupt when the txmulticol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask is enabled.
14	0h RW	**MMC Transmit Single Collision Good Packet Counter Interrupt Mask (TXSCOLGPIM):** Setting this bit masks the interrupt when the txsinglecol_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Single Collision Good Packet Counter Interrupt Mask is enabled.
13	0h RW	**MMC Transmit Underflow Error Packet Counter Interrupt Mask (TXUFLOWERPIM):** Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask (TXBCGBPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask (TXMCGBPIM):** Setting this bit masks the interrupt when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask (TXUCGBPIM):** Setting this bit masks the interrupt when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask (TX1024TMAXOCTGBPIM):** Setting this bit masks the interrupt when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask (TX512T1023OCTGBPIM):** Setting this bit masks the interrupt when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask (TX256T511OCTGBPIM):** Setting this bit masks the interrupt when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask (TX128T255OCTGBPIM):** Setting this bit masks the interrupt when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask (TX65T127OCTGBPIM):** Setting this bit masks the interrupt when the tx65to127octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask (TX64OCTGBPIM):** Setting this bit masks the interrupt when the tx64octets_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask is enabled.
3	0h RW	**MMC Transmit Multicast Good Packet Counter Interrupt Mask (TXMCGPIM):** Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Transmit Broadcast Good Packet Counter Interrupt Mask (TXBCGPIM):** Setting this bit masks the interrupt when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Transmit Good Bad Packet Counter Interrupt Mask (TXGBPKTIM):** Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Good Bad Octet Counter Interrupt Mask (TXGBOCTIM):** Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled.

14.20.3.191TX_OCTET_COUNT_GOOD_BAD — Offset 50220714h

This register provides the number of bytes transmitted by the GbE Controller, exclusive of preamble and retried bytes, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	50220714h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good Bad (TXOCTGB):** This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

14.20.3.192TX_PACKET_COUNT_GOOD_BAD — Offset 50220718h

This register provides the number of good and bad packets transmitted by GbE Controller, exclusive of retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50220718h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good Bad (TXPKTGB):** This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

14.20.3.193TX_BROADCAST_PACKETS_GOOD — Offset 5022071Ch

This register provides the number of good broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	5022071Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good (TXBCASTG):** This field indicates the number of good broadcast packets transmitted.

14.20.3.194TX_MULTICAST_PACKETS_GOOD — Offset 50220720h

This register provides the number of good multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220720h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good (TXMCASTG):** This field indicates the number of good multicast packets transmitted.

14.20.3.195TX_64OCTETS_PACKETS_GOOD_BAD — Offset 50220724h

This register provides the number of good and bad packets transmitted by GbE Controller with length 64 bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50220724h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 64Octets Packets Good_Bad (TX64OCTGB):** This field indicates the number of good and bad packets transmitted with length 64 bytes, exclusive of preamble and retried packets.

14.20.3.196TX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 50220728h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50220728h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**TX65_127OCTGB:** Tx 65To127Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.3.197TX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 5022072Ch

This register provides the number of good and bad packets transmitted by GbE Controller with length between 128 to 255 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	5022072Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 128To255Octets Packets Good Bad (TX128_255OCTGB):** This field indicates the number of good and bad packets transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.3.198TX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 50220730h

This register provides the number of good and bad packets transmitted by GbE Controller with length between 256 to 511 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50220730h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 256To511Octets Packets Good Bad (TX256_511OCTGB):** This field indicates the number of good and bad packets transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.3.199TX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 50220734h

This register provides the number of good and bad packets transmitted by GbE Controller with length 512 to 1023 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50220734h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 512To1023Octets Packets Good Bad (TX512_1023OCTGB):** This field indicates the number of good and bad packets transmitted with length between 512 and 1023 (inclusive) bytes, exclusive of preamble and retried packets.

14.20.3.200TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 50220738h

This register provides the number of good and bad packets transmitted by GbE Controller with length 1024 to maxsize (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	50220738h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx 1024ToMaxOctets Packets Good Bad (TX1024_MAXOCTGB):** This field indicates the number of good and bad packets transmitted with length between 1024 and maxsize (inclusive) bytes, exclusive of preamble and retried packets.

14.20.3.201TX_UNICAST_PACKETS_GOOD_BAD — Offset 5022073Ch

This register provides the number of good and bad unicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	5022073Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Unicast Packets Good Bad (TXUCASTGB):** This field indicates the number of good and bad unicast packets transmitted.

14.20.3.202TX_MULTICAST_PACKETS_GOOD_BAD — Offset 50220740h

This register provides the number of good and bad multicast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220740h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multicast Packets Good Bad (TXMCASTGB):** This field indicates the number of good and bad multicast packets transmitted.

14.20.3.203TX_BROADCAST_PACKETS_GOOD_BAD — Offset 50220744h

This register provides the number of good and bad broadcast packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220744h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Broadcast Packets Good Bad (TXBCASTGB):** This field indicates the number of good and bad broadcast packets transmitted.

14.20.3.204TX_UNDERFLOW_ERROR_PACKETS — Offset 50220748h

This register provides the number of packets aborted by GbE Controller because of packets underflow error.

Type	Size	Offset	Default
MMIO	32 bit	50220748h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Underflow Error Packets (TXUNDRFLW):** This field indicates the number of packets aborted because of packets underflow error.

14.20.3.205TX_SINGLE_COLLISION_GOOD_PACKETS — Offset 5022074Ch

This register provides the number of successfully transmitted packets by GbE Controller after a single collision in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	5022074Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Single Collision Good Packets (TXSNGLCOLG):** This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

14.20.3.206TX_MULTIPLE_COLLISION_GOOD_PACKETS — Offset 50220750h

This register provides the number of successfully transmitted packets by GbE Controller after multiple collisions in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	50220750h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Multiple Collision Good Packets (TXMULTCOLG):** This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

14.20.3.207TX_DEFERRED_PACKETS — Offset 50220754h

This register provides the number of successfully transmitted by GbE Controller after a deferral in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	50220754h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Deferred Packets (TXDEFRD):** This field indicates the number of successfully transmitted after a deferral in the half-duplex mode.

14.20.3.208TX_LATE_COLLISION_PACKETS — Offset 50220758h

This register provides the number of packets aborted by GbE Controller because of late collision error.

Type	Size	Offset	Default
MMIO	32 bit	50220758h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Late Collision Packets (TXLATECOL):** This field indicates the number of packets aborted because of late collision error.

14.20.3.209TX_EXCESSIVE_COLLISION_PACKETS — Offset 5022075Ch

This register provides the number of packets aborted by GbE Controller because of excessive (16) collision errors.

Type	Size	Offset	Default
MMIO	32 bit	5022075Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Collision Packets (TXEXSCOL):** This field indicates the number of packets aborted because of excessive (16) collision errors.

14.20.3.210TX_CARRIER_ERROR_PACKETS — Offset 50220760h

This register provides the number of packets aborted by GbE Controller because of carrier sense error (no carrier or loss of carrier).

Type	Size	Offset	Default
MMIO	32 bit	50220760h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Carrier Error Packets (TXCARR):** This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

14.20.3.211TX_OCTET_COUNT_GOOD — Offset 50220764h

This register provides the number of bytes transmitted by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	50220764h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Octet Count Good (TXOCTG):** This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

14.20.3.212TX_PACKET_COUNT_GOOD — Offset 50220768h

This register provides the number of good packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220768h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Packet Count Good (TXPKTG):** This field indicates the number of good packets transmitted.

14.20.3.213TX_EXCESSIVE_DEFERRAL_ERROR — Offset 5022076Ch

This register provides the number of packets aborted by GbE Controller because of excessive deferral error (deferred for more than two max-sized packet times).

Type	Size	Offset	Default
MMIO	32 bit	5022076Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Excessive Deferral Error (TXEXSDEF):** This field indicates the number of packets aborted because of excessive deferral error (deferred for more than two max-sized packet times).

14.20.3.214TX_PAUSE_PACKETS — Offset 50220770h

This register provides the number of good Pause packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220770h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Pause Packets (TXPAUSE):** This field indicates the number of good Pause packets transmitted.

14.20.3.215TX_VLAN_PACKETS_GOOD — Offset 50220774h

This register provides the number of good VLAN packets transmitted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220774h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx VLAN Packets Good (TXVLANG):** This field provides the number of good VLAN packets transmitted.

14.20.3.216TX_OSIZE_PACKETS_GOOD — Offset 50220778h

This register provides the number of packets transmitted by GbE Controller without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	50220778h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx OSize Packets Good (TXOSIZG):** This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

14.20.3.217RX_PACKETS_COUNT_GOOD_BAD — Offset 50220780h

This register provides the number of good and bad packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220780h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packets Count Good Bad (RXPKTGB):** This field indicates the number of good and bad packets received.

14.20.3.218RX_OCTET_COUNT_GOOD_BAD — Offset 50220784h

This register provides the number of bytes received by DWC_ther_qos, exclusive of preamble, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	50220784h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good Bad (RXOCTGB):** This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

14.20.3.219RX_OCTET_COUNT_GOOD — Offset 50220788h

This register provides the number of bytes received by GbE Controller, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	50220788h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Octet Count Good (RXOCTG):** This field indicates the number of bytes received, exclusive of preamble, only in good packets.

14.20.3.220RX_BROADCAST_PACKETS_GOOD — Offset 5022078Ch

This register provides the number of good broadcast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	5022078Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Broadcast Packets Good (RXBCASTG):** This field indicates the number of good broadcast packets received.

14.20.3.221RX_MULTICAST_PACKETS_GOOD — Offset 50220790h

This register provides the number of good multicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	50220790h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Multicast Packets Good (RXMCASTG):** This field indicates the number of good multicast packets received.

14.20.3.222RX_CRC_ERROR_PACKETS — Offset 50220794h

This register provides the number of packets received by GbE Controller with CRC error.

Type	Size	Offset	Default
MMIO	32 bit	50220794h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx CRC Error Packets (RXCRCERR):** This field indicates the number of packets received with CRC error.

14.20.3.223RX_ALIGNMENT_ERROR_PACKETS — Offset 50220798h

This register provides the number of packets received by GbE Controller with alignment (dribble) error. It is valid only in 10/100 mode.

Type	Size	Offset	Default
MMIO	32 bit	50220798h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Alignment Error Packets (RXALGNERR):** This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode.

14.20.3.224RX_RUNT_ERROR_PACKETS — Offset 5022079Ch

This register provides the number of packets received by GbE Controller with runt (length less than 64 bytes and CRC error) error.

Type	Size	Offset	Default
MMIO	32 bit	5022079Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Runt Error Packets (RXRUNTERR):** This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error.

14.20.3.225RX_JABBER_ERROR_PACKETS — Offset 502207A0h

This register provides the number of giant packets received by GbE Controller with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

Type	Size	Offset	Default
MMIO	32 bit	502207A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Jabber Error Packets (RXJABERR):** This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

14.20.3.226RX_UNDERSIZE_PACKETS_GOOD — Offset 502207A4h

This register provides the number of packets received by GbE Controller with length less than 64 bytes, without any errors.

Type	Size	Offset	Default
MMIO	32 bit	502207A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Undersize Packets Good (RXUNDERSZG):** This field indicates the number of packets received with length less than 64 bytes, without any errors.

14.20.3.227RX_OVERSIZE_PACKETS_GOOD — Offset 502207A8h

This register provides the number of packets received by GbE Controller without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	502207A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Oversize Packets Good (RXOVERSZG):** This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

14.20.3.228RX_64OCTETS_PACKETS_GOOD_BAD — Offset 502207ACh

This register provides the number of good and bad packets received by GbE Controller with length 64 bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502207ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 64 Octets Packets Good Bad (RX64OCTGB):** This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble.

14.20.3.229RX_65TO127OCTETS_PACKETS_GOOD_BAD — Offset 502207B0h

This register provides the number of good and bad packets received by GbE Controller with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502207B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX65_127OCTGB:** Rx 65-127 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

14.20.3.230RX_128TO255OCTETS_PACKETS_GOOD_BAD — Offset 502207B4h

This register provides the number of good and bad packets received by GbE Controller with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502207B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX128_255OCTGB:** Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

14.20.3.231RX_256TO511OCTETS_PACKETS_GOOD_BAD — Offset 502207B8h

This register provides the number of good and bad packets received by GbE Controller with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502207B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX256_511OCTGB:** Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

14.20.3.232RX_512TO1023OCTETS_PACKETS_GOOD_BAD — Offset 502207BCh

This register provides the number of good and bad packets received by GbE Controller with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502207BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RX 512-1023 Octets Packets Good Bad (RX512_1023OCTGB):** This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

14.20.3.233RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD — Offset 502207C0h

This register provides the number of good and bad packets received by GbE Controller with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	502207C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx 1024-Max Octets Good Bad (RX1024_MAXOCTGB):** This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

14.20.3.234RX_UNICAST_PACKETS_GOOD — Offset 502207C4h

This register provides the number of good unicast packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Unicast Packets Good (RXUCASTG):** This field indicates the number of good unicast packets received.

14.20.3.235RX_LENGTH_ERROR_PACKETS — Offset 502207C8h

This register provides the number of packets received by GbE Controller with length error (Length Type field not equal to packet size), for all packets with valid length field.

Type	Size	Offset	Default
MMIO	32 bit	502207C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Length Error Packets (RXLENERR):** This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

14.20.3.236RX_OUT_OF_RANGE_TYPE_PACKETS — Offset 502207CCh

This register provides the number of packets received by GbE Controller with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

Type	Size	Offset	Default
MMIO	32 bit	502207CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Out of Range Type Packet (RXOUTOFRNG):** This field indicates the number of packets received with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

14.20.3.237RX_PAUSE_PACKETS — Offset 502207D0h

This register provides the number of good and valid Pause packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Pause Packets (RXPAUSEPKT):** This field indicates the number of good and valid Pause packets received.

14.20.3.238RX_FIFO_OVERFLOW_PACKETS — Offset 502207D4h

This register provides the number of missed received packets because of FIFO overflow in GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FIFO Overflow Packets (RXFIFOOVFL):** This field indicates the number of missed received packets because of FIFO overflow.

14.20.3.239RX_VLAN_PACKETS_GOOD_BAD — Offset 502207D8h

This register provides the number of good and bad VLAN packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx VLAN Packets Good Bad (RXVLANPKTGB):** This field indicates the number of good and bad VLAN packets received.

14.20.3.240RX_WATCHDOG_ERROR_PACKETS — Offset 502207DCh

This register provides the number of packets received by GbE Controller with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

Type	Size	Offset	Default
MMIO	32 bit	502207DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Watchdog Error Packets (RXWDGERR):** This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

14.20.3.241RX_RECEIVE_ERROR_PACKETS — Offset 502207E0h

This register provides the number of packets received by GbE Controller with Receive error or Packet Extension error on the GMII or MII interface.

Type	Size	Offset	Default
MMIO	32 bit	502207E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Receive Error Packets (RXRCVERR):** This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface.

14.20.3.242RX_CONTROL_PACKETS_GOOD — Offset 502207E4h

This register provides the number of good control packets received by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Control Packets Good (RXCTRLG):** This field indicates the number of good control packets received.

14.20.3.243TX_LPI_USEC_CNTR — Offset 502207ECh

This register provides the number of microseconds Tx LPI is asserted by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Microseconds Counter (TXLPIUSC):** This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

14.20.3.244TX_LPI_TRAN_CNTR — Offset 502207F0h

This register provides the number of times GbE Controller has entered Tx LPI.

Type	Size	Offset	Default
MMIO	32 bit	502207F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx LPI Transition counter (TXLPITRC):** This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments.

14.20.3.245RX_LPI_USEC_CNTR — Offset 502207F4h

This register provides the number of microseconds Rx LPI is sampled by GbE Controller.

Type	Size	Offset	Default
MMIO	32 bit	502207F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Microseconds Counter (RXLPIUSC):** This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

14.20.3.246RX_LPI_TRAN_CNTR — Offset 502207F8h

This register provides the number of times GbE Controller has entered Rx LPI.

Type	Size	Offset	Default
MMIO	32 bit	502207F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx LPI Transition counter (RXLPITRC):** This field indicates the number of times Rx LPI Entry has occurred.

14.20.3.247MMC_IPC_RX_INTERRUPT_MASK — Offset 50220800h

This register maintains the mask for the interrupt generated from the receive IPC statistic counters. The MMC Receive Checksum Off load Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Off load) statistic counters reach half their maximum value, and when they reach their maximum values. This register is 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	50220800h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**MMC Receive ICMP Error Octet Counter Interrupt Mask (RXICMPEROIM):** Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled.
28	0h RW	**MMC Receive ICMP Good Octet Counter Interrupt Mask (RXICMPGOIM):** Setting this bit masks the interrupt when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Octet Counter Interrupt Mask is enabled.
27	0h RW	**MMC Receive TCP Error Octet Counter Interrupt Mask (RXTCPEROIM):** Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Octet Counter Interrupt Mask is enabled.
26	0h RW	**MMC Receive TCP Good Octet Counter Interrupt Mask (RXTCPGOIM):** Setting this bit masks the interrupt when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Octet Counter Interrupt Mask is enabled.
25	0h RW	**MMC Receive UDP Good Octet Counter Interrupt Mask (RXUDPEROIM):** Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Octet Counter Interrupt Mask is enabled.
24	0h RW	**MMC Receive IPV6 No Payload Octet Counter Interrupt Mask (RXUDPGOIM):** Setting this bit masks the interrupt when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Octet Counter Interrupt Mask is enabled.
23	0h RW	**MMC Receive IPV6 Header Error Octet Counter Interrupt Mask (RXIPV6NOPAYOIM):** Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6HEROIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
21	0h RW	**MMC Receive IPV6 Good Octet Counter Interrupt Mask (RXIPV6GOIM):** Setting this bit masks the interrupt when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Octet Counter Interrupt Mask is enabled.
20	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask (RXIPV4UDSBLOIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask is enabled.
19	0h RW	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask (RXIPV4FRAGOIM):** Setting this bit masks the interrupt when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask is enabled.
18	0h RW	**MMC Receive IPV4 No Payload Octet Counter Interrupt Mask (RXIPV4NOPAYOIM):** Setting this bit masks the interrupt when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Octet Counter Interrupt Mask is enabled.
17	0h RW	**MMC Receive IPV4 Header Error Octet Counter Interrupt Mask (RXIPV4HEROIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled.
16	0h RW	**MMC Receive IPV4 Good Octet Counter Interrupt Mask (RXIPV4GOIM):** Setting this bit masks the interrupt when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Octet Counter Interrupt Mask is enabled.
15:14	0h RO	**Reserved**
13	0h RW	**MMC Receive ICMP Error Packet Counter Interrupt Mask (RXICMPERPIM):** Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**MMC Receive ICMP Good Packet Counter Interrupt Mask (RXICMPGPIM):** Setting this bit masks the interrupt when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive ICMP Good Packet Counter Interrupt Mask is enabled.
11	0h RW	**MMC Receive TCP Error Packet Counter Interrupt Mask (RXTCPERPIM):** Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Error Packet Counter Interrupt Mask is enabled.
10	0h RW	**MMC Receive TCP Good Packet Counter Interrupt Mask (RXTCPGPIM):** Setting this bit masks the interrupt when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive TCP Good Packet Counter Interrupt Mask is enabled.
9	0h RW	**MMC Receive UDP Error Packet Counter Interrupt Mask (RXUDPERPIM):** Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Error Packet Counter Interrupt Mask is enabled.
8	0h RW	**MMC Receive UDP Good Packet Counter Interrupt Mask (RXUDPGPIM):** Setting this bit masks the interrupt when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive UDP Good Packet Counter Interrupt Mask is enabled.
7	0h RW	**MMC Receive IPV6 No Payload Packet Counter Interrupt Mask (RXIPV6NOPAYPIM):** Setting this bit masks the interrupt when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 No Payload Packet Counter Interrupt Mask is enabled.
6	0h RW	**MMC Receive IPV6 Header Error Packet Counter Interrupt Mask (RXIPV6HERPIM):** Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled.
5	0h RW	**MMC Receive IPV6 Good Packet Counter Interrupt Mask (RXIPV6GPIM):** Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled.
4	0h RW	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask (RXIPV4UDSBLPIM):** Setting this bit masks the interrupt when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask (RXIPV4FRAGPIM):** Setting this bit masks the interrupt when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask is enabled.
2	0h RW	**MMC Receive IPV4 No Payload Packet Counter Interrupt Mask (RXIPV4NOPAYPIM):** Setting this bit masks the interrupt when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 No Payload Packet Counter Interrupt Mask is enabled.
1	0h RW	**MMC Receive IPV4 Header Error Packet Counter Interrupt Mask (RXIPV4HERPIM):** Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled.
0	0h RW	**MMC Receive IPV4 Good Packet Counter Interrupt Mask (RXIPV4GPIM):** Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. 0x0 (DISABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled.

14.20.3.248MMC_IPC_RX_INTERRUPT — Offset 50220808h

This register maintains the interrupt that the receive IPC statistic counters generate. The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits[7:0]) must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	50220808h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RO	**MMC Receive ICMP Error Octet Counter Interrupt Status (RXICMPEROIS):** This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Octet Counter Interrupt Status detected.
28	0h RO	**MMC Receive ICMP Good Octet Counter Interrupt Status (RXICMPGOIS):** This bit is set when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Octet Counter Interrupt Status detected.
27	0h RO	**MMC Receive TCP Error Octet Counter Interrupt Status (RXTCPEROIS):** This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Octet Counter Interrupt Status detected.
26	0h RO	**MMC Receive TCP Good Octet Counter Interrupt Status (RXTCPGOIS):** This bit is set when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Octet Counter Interrupt Status detected.
25	0h RO	**MMC Receive UDP Error Octet Counter Interrupt Status (RXUDPEROIS):** This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Octet Counter Interrupt Status detected.
24	0h RO	**MMC Receive UDP Good Octet Counter Interrupt Status (RXUDPGOIS):** This bit is set when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**MMC Receive IPV6 No Payload Octet Counter Interrupt Status (RXIPV6NOPAYOIS):** This bit is set when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Octet Counter Interrupt Status detected.
22	0h RO	**MMC Receive IPV6 Header Error Octet Counter Interrupt Status (RXIPV6HEROIS):** This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected.
21	0h RO	**MMC Receive IPV6 Good Octet Counter Interrupt Status (RXIPV6GOIS):** This bit is set when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Octet Counter Interrupt Status detected.
20	0h RO	**RXIPV4UDSBLOIS:** MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status This bit is set when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status detected.
19	0h RO	**MMC Receive IPV4 Fragmented Octet Counter Interrupt Status (RXIPV4FRAGOIS):** This bit is set when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Octet Counter Interrupt Status detected.
18	0h RO	**MMC Receive IPV4 No Payload Octet Counter Interrupt Status (RXIPV4NOPAYOIS):** This bit is set when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Octet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**MMC Receive IPV4 Header Error Octet Counter Interrupt Status (RXIPV4HEROIS):** This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected.
16	0h RO	**MMC Receive IPV4 Good Octet Counter Interrupt Status (RXIPV4GOIS):** This bit is set when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Octet Counter Interrupt Status detected.
15:14	0h RO	**Reserved**
13	0h RO	**MMC Receive ICMP Error Packet Counter Interrupt Status (RXICMPERPIS):** This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Error Packet Counter Interrupt Status detected.
12	0h RO	**MMC Receive ICMP Good Packet Counter Interrupt Status (RXICMPGPIS):** This bit is set when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive ICMP Good Packet Counter Interrupt Status detected.
11	0h RO	**MMC Receive TCP Error Packet Counter Interrupt Status (RXTCPERPIS):** This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Error Packet Counter Interrupt Status detected.
10	0h RO	**MMC Receive TCP Good Packet Counter Interrupt Status (RXTCPGPIS):** This bit is set when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive TCP Good Packet Counter Interrupt Status detected.
9	0h RO	**MMC Receive UDP Error Packet Counter Interrupt Status (RXUDPERPIS):** This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Error Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**MC Receive UDP Good Packet Counter Interrupt Status (RXUDPGPIS):** This bit is set when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive UDP Good Packet Counter Interrupt Status detected.
7	0h RO	**MMC Receive IPV6 No Payload Packet Counter Interrupt Status (RXIPV6NOPAYPIS):** This bit is set when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 No Payload Packet Counter Interrupt Status detected.
6	0h RO	**MMC Receive IPV6 Header Error Packet Counter Interrupt Status (RXIPV6HERPIS):** This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected.
5	0h RO	**MMC Receive IPV6 Good Packet Counter Interrupt Status (RXIPV6GPIS):** This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV6 Good Packet Counter Interrupt Status detected.
4	0h RO	**MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status (RXIPV4UDSBLPIS):** This bit is set when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value. 0x0 (INACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status detected.
3	0h RO	**MMC Receive IPV4 Fragmented Packet Counter Interrupt Status (RXIPV4FRAGPIS):** This bit is set when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Fragmented Packet Counter Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MMC Receive IPV4 No Payload Packet Counter Interrupt Status (RXIPV4NOPAYPIS):** This bit is set when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 No Payload Packet Counter Interrupt Status detected.
1	0h RO	**MMC Receive IPV4 Header Error Packet Counter Interrupt Status (RXIPV4HERPIS):** This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected.
0	0h RO	**MMC Receive IPV4 Good Packet Counter Interrupt Status (RXIPV4GPIS):** This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Receive IPV4 Good Packet Counter Interrupt Status detected.

14.20.3.249RXIPV4_GOOD_PACKETS — Offset 50220810h

This register provides the number of good IPv4 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50220810h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Packets (RXIPV4GDPKT):** This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

14.20.3.250RXIPV4_HEADER_ERROR_PACKETS — Offset 50220814h

RxIPv4 Header Error Packets This register provides the number of IPv4 datagrams received by GbE Controller with header (checksum, length, or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	50220814h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Packets (RXIPV4HDRERRPKT):** This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

14.20.3.251RXIPV4_NO_PAYLOAD_PACKETS — Offset 50220818h

This register provides the number of IPv4 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50220818h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Packets (RXIPV4NOPAYPKT):** This field indicates the number of IPv4 datagram packets received that did not have a TCP, UDP, or ICMP payload.

14.20.3.252RXIPV4_FRAGMENTED_PACKETS — Offset 5022081Ch

This register provides the number of good IPv4 datagrams received by GbE Controller with fragmentation.

Type	Size	Offset	Default
MMIO	32 bit	5022081Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Packets (RXIPV4FRAGPKT):** This field indicates the number of good IPv4 datagrams received with fragmentation.

14.20.3.253RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS — Offset 50220820h

This register provides the number of good IPv4 datagrams received by GbE Controller that had a UDP payload with checksum disabled.

Type	Size	Offset	Default
MMIO	32 bit	50220820h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disabled Packets (RXIPV4UDSBLPKT):** This field indicates the number of good IPv4 datagrams received that had a UDP payload with checksum disabled.

14.20.3.254RXIPV6_GOOD_PACKETS — Offset 50220824h

This register provides the number of good IPv6 datagrams received by GbE Controller with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50220824h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Packets (RXIPV6GDPKT):** This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

14.20.3.255RXIPV6_HEADER_ERROR_PACKETS — Offset 50220828h

This register provides the number of IPv6 datagrams received by GbE Controller with header (length or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	50220828h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Packets (RXIPV6HDRERRPKT):** This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

14.20.3.256RXIPV6_NO_PAYLOAD_PACKETS — Offset 5022082Ch

This register provides the number of IPv6 datagram packets received by GbE Controller that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

Type	Size	Offset	Default
MMIO	32 bit	5022082Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Packets (RXIPV6NOPAYPKT):** This field indicates the number of IPv6 datagram packets received that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

14.20.3.257RXUDP_GOOD_PACKETS — Offset 50220830h

This register provides the number of good IP datagrams received by GbE Controller with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

Type	Size	Offset	Default
MMIO	32 bit	50220830h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Packets (RXUDPGDPKT):** This field indicates the number of good IP datagrams received with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

14.20.3.258RXUDP_ERROR_PACKETS — Offset 50220834h

This register provides the number of good IP datagrams received by GbE Controller whose UDP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	50220834h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Packets (RXUDPERRPKT):** This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

14.20.3.259RXTCP_GOOD_PACKETS — Offset 50220838h

This register provides the number of good IP datagrams received by GbE Controller with a good TCP payload.

Type	Size	Offset	Default
MMIO	32 bit	50220838h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Packets (RXTCPGDPKT):** This field indicates the number of good IP datagrams received with a good TCP payload.

14.20.3.260RXTCP_ERROR_PACKETS — Offset 5022083Ch

This register provides the number of good IP datagrams received by GbE Controller whose TCP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	5022083Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Packets (RXTCPERRPKT):** This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

14.20.3.261RXICMP_GOOD_PACKETS — Offset 50220840h

This register provides the number of good IP datagrams received by GbE Controller with a good ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	50220840h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Packets (RXICMPGDPKT):** This field indicates the number of good IP datagrams received with a good ICMP payload.

14.20.3.262RXICMP_ERROR_PACKETS — Offset 50220844h

This register provides the number of good IP datagrams received by GbE Controller whose ICMP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	50220844h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Packets (RXICMPERRPKT):** This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

14.20.3.263RXIPV4_GOOD_OCTETS — Offset 50220850h

This register provides the number of bytes received by GbE Controller in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50220850h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Good Octets (RXIPV4GDOCT):** This field indicates the number of bytes received in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.264RXIPV4_HEADER_ERROR_OCTETS — Offset 50220854h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50220854h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Header Error Octets (RXIPV4HDRERROCT):** This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.265RXIPV4_NO_PAYLOAD_OCTETS — Offset 50220858h

This register provides the number of bytes received by GbE Controller in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50220858h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Payload Octets (RXIPV4NOPAYOCT):** This field indicates the number of bytes received in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.266RXIPV4_FRAGMENTED_OCTETS — Offset 5022085Ch

This register provides the number of bytes received by GbE Controller in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	5022085Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 Fragmented Octets (RXIPV4FRAGOCT):** This field indicates the number of bytes received in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.267RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS — Offset 50220860h

This register provides the number of bytes received by GbE Controller in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50220860h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv4 UDP Checksum Disable Octets (RXIPV4UDSBLOCT):** This field indicates the number of bytes received in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.268RXIPV6_GOOD_OCTETS — Offset 50220864h

This register provides the number of bytes received by GbE Controller in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50220864h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Good Octets (RXIPV6GDOCT):** This field indicates the number of bytes received in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.269RXIPV6_HEADER_ERROR_OCTETS — Offset 50220868h

This register provides the number of bytes received by GbE Controller in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	50220868h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Header Error Octets (RXIPV6HDRERROCT):** This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.270RXIPV6_NO_PAYLOAD_OCTETS — Offset 5022086Ch

This register provides the number of bytes received by GbE Controller in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	5022086Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxIPv6 Payload Octets (RXIPV6NOPAYOCT):** This field indicates the number of bytes received in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

14.20.3.271RXUDP_GOOD_OCTETS — Offset 50220870h

This register provides the number of bytes received by GbE Controller in a good UDP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50220870h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Good Octets (RXUDPGDOCT):** This field indicates the number of bytes received in a good UDP segment. This counter does not count IP header bytes.

14.20.3.272RXUDP_ERROR_OCTETS — Offset 50220874h

This register provides the number of bytes received by GbE Controller in a UDP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50220874h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxUDP Error Octets (RXUDPERROCT):** This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

14.20.3.273RXTCP_GOOD_OCTETS — Offset 50220878h

This register provides the number of bytes received by GbE Controller in a good TCP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50220878h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Good Octets (RXTCPGDOCT):** This field indicates the number of bytes received in a good TCP segment. This counter does not count IP header bytes.

14.20.3.274RXTCP_ERROR_OCTETS — Offset 5022087Ch

This register provides the number of bytes received by GbE Controller in a TCP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	5022087Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxTCP Error Octets (RXTCPERROCT):** This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

14.20.3.275RXICMP_GOOD_OCTETS — Offset 50220880h

This register provides the number of bytes received by GbE Controller in a good ICMP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50220880h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Good Octets (RXICMPGDOCT):** This field indicates the number of bytes received in a good ICMP segment. This counter does not count IP header bytes.

14.20.3.276RXICMP_ERROR_OCTETS — Offset 50220884h

This register provides the number of bytes received by GbE Controller in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	50220884h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**RxICMP Error Octets (RXICMPERROCT):** This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

14.20.3.277MMC_FPE_TX_INTERRUPT — Offset 502208A0h

This register maintains the interrupts generated from all FPE related Transmit statistics counters. The MMC FPE Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	502208A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MMC Tx Hold Request Counter Interrupt Status (HRCIS):** This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected.
0	0h RO	**MMC Tx FPE Fragment Counter Interrupt status (FCIS):** This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected. 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected.

14.20.3.278MMC_FPE_TX_INTERRUPT_MASK — Offset 502208A4h

This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	502208A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**MMC Transmit Hold Request Counter Interrupt Mask (HRCIM):** Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. 0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled.
0	0h RW	**MMC Transmit Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled.

14.20.3.279MMC_TX_FPE_FRAGMENT_CNTR — Offset 502208A8h

This register provides the number of additional mPackets transmitted due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	502208A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx FPE Fragment counter (TXFFC):** This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.3.280MMC_TX_HOLD_REQ_CNTR — Offset 502208ACh

This register provides the count of number of times a hold request is given to MAC

Type	Size	Offset	Default
MMIO	32 bit	502208ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Tx Hold Request Counter (TXHRC):** This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

14.20.3.281MMC_FPE_RX_INTERRUPT — Offset 502208C0h

This register maintains the interrupts generated from all FPE related Receive statistics counters. The MMC FPE Receive Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	502208C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**MMC Rx FPE Fragment Counter Interrupt Status (FCIS):** This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected.
2	0h RO	**MMC Rx Packet Assembly OK Counter Interrupt Status (PAOCIS):** This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected.
1	0h RO	**MMC Rx Packet SMD Error Counter Interrupt Status (PSECIS):** This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected.
0	0h RO	**MMC Rx Packet Assembly Error Counter Interrupt Status (PAECIS):** This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected. 0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected.

14.20.3.282MMC_FPE_RX_INTERRUPT_MASK — Offset 502208C4h

This register maintains the masks for interrupts generated from all FPE related Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	502208C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**MMC Rx FPE Fragment Counter Interrupt Mask (FCIM):** Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled.
2	0h RW	**MMC Rx Packet Assembly OK Counter Interrupt Mask (PAOCIM):** Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled.
1	0h RW	**MMC Rx Packet SMD Error Counter Interrupt Mask (PSECIM):** Setting this bit masks the interrupt when the R Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled.
0	0h RW	**MMC Rx Packet Assembly Error Counter Interrupt Mask (PAECIM):** Setting this bit masks the interrupt when the R Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. 0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled. 0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled.

14.20.3.283MMC_RX_PACKET_ASSEMBLY_ERR_CNTR — Offset 502208C8h

This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.

Type	Size	Offset	Default
MMIO	32 bit	502208C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly Error Counter (PAEC):** This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.3.284MMC_RX_PACKET_SMD_ERR_CNTR — Offset 502208CCh

This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.

Type	Size	Offset	Default
MMIO	32 bit	502208CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet SMD Error Counter (PSEC):** This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.3.285MMC_RX_PACKET_ASSEMBLY_OK_CNTR — Offset 502208D0h

This register provides the number of MAC frames that were successfully reassembled and delivered to MAC.

Type	Size	Offset	Default
MMIO	32 bit	502208D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx Packet Assembly OK Counter (PAOC):** This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.3.286MMC_RX_FPE_FRAGMENT_CNTR — Offset 502208D4h

This register provides the number of additional mPackets received due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	502208D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rx FPE Fragment Counter (FFC):** This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

14.20.3.287MAC_L3_L4_CONTROL0 — Offset 50220900h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	50220900h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN0):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**
26:24	0h RW	**DMA Channel Number (DMCHN0):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM0):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM0):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM0):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Reserved**
16	0h RW	**Layer 4 Protocol Enable (L4PEN0):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.
15:11	00h RW	**L3HDBM0:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM0:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM0):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM0):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN0):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

14.20.3.288MAC_LAYER4_ADDRESS0 — Offset 50220904h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core. You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	50220904h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP0):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP0):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

14.20.3.289MAC_LAYER3_ADDR0_REG0 — Offset 50220910h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50220910h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A00):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

14.20.3.290MAC_LAYER3_ADDR1_REG0 — Offset 50220914h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50220914h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A10):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

14.20.3.291MAC_LAYER3_ADDR2_REG0 — Offset 50220918h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50220918h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A20):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.3.292MAC_LAYER3_ADDR3_REG0 — Offset 5022091Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	5022091Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A30):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.3.293MAC_L3_L4_CONTROL1 — Offset 50220930h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	50220930h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMA Channel Select Enable (DMCHEN1):** When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter. 0x0 (DISABLE): DMA Channel Select is disabled. 0x1 (ENABLE): DMA Channel Select is enabled.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**DMA Channel Number (DMCHN1):** When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**Layer 4 Destination Port Inverse Match Enable (L4DPIM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high. 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled.
20	0h RW	**Layer 4 Destination Port Match Enable (L4DPM1):** When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0 (DISABLE): Layer 4 Destination Port Match is disabled. 0x1 (ENABLE): Layer 4 Destination Port Match is enabled.
19	0h RW	**Layer 4 Source Port Inverse Match Enable (L4SPIM1):** When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high. 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled.
18	0h RW	**Layer 4 Source Port Match Enable (L4SPM1):** When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0 (DISABLE): Layer 4 Source Port Match is disabled. 0x1 (ENABLE): Layer 4 Source Port Match is enabled.
17	0h RO	**Reserved**
16	0h RW	**Layer 4 Protocol Enable (L4PEN1):** When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set. 0x0 (DISABLE): Layer 4 Protocol is disabled. 0x1 (ENABLE): Layer 4 Protocol is enabled.

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RW	**L3HDBM1:** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM1:** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**Layer 3 IP DA Inverse Match Enable (L3DAIM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high. 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled.
4	0h RW	**Layer 3 IP DA Match Enable (L3DAM1):** When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP DA Match is disabled. 0x1 (ENABLE): Layer 3 IP DA Match is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Layer 3 IP SA Inverse Match Enable (L3SAIM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set. 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled.
2	0h RW	**Layer 3 IP SA Match Enable (L3SAM1):** When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering. 0x0 (DISABLE): Layer 3 IP SA Match is disabled. 0x1 (ENABLE): Layer 3 IP SA Match is enabled.
1	0h RO	**Reserved**
0	0h RW	**Layer 3 Protocol Enable (L3PEN1):** When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set. 0x0 (DISABLE): Layer 3 Protocol is disabled. 0x1 (ENABLE): Layer 3 Protocol is enabled.

14.20.3.294MAC_LAYER4_ADDRESS1 — Offset 50220934h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core. You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	50220934h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Layer 4 Destination Port Number Field (L4DP1):** When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**Layer 4 Source Port Number Field (L4SP1):** When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

14.20.3.295MAC_LAYER3_ADDR0_REG1 — Offset 50220940h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50220940h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 0 Field (L3A01):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

14.20.3.296MAC_LAYER3_ADDR1_REG1 — Offset 50220944h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50220944h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 1 Field (L3A11):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

14.20.3.297MAC_LAYER3_ADDR2_REG1 — Offset 50220948h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	50220948h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 2 Field (L3A21):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.3.298MAC_LAYER3_ADDR3_REG1 — Offset 5022094Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	5022094Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Layer 3 Address 3 Field (L3A31):** When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

14.20.3.299MAC_TIMESTAMP_CONTROL — Offset 50220B00h

This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver.

Type	Size	Offset	Default
MMIO	32 bit	50220B00h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**AV 802.1AS Mode Enable (AV8021ASMEN):** When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. 0x0 (DISABLE): AV 802.1AS Mode is disabled. 0x1 (ENABLE): AV 802.1AS Mode is enabled.
27:25	0h RO	**Reserved**
24	0h RW	**Transmit Timestamp Status Mode (TXTSSTSM):** When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. 0x0 (DISABLE): Transmit Timestamp Status Mode is disabled. 0x1 (ENABLE): Transmit Timestamp Status Mode is enabled.
23:21	0h RO	**Reserved**
20	0h RW	**External System Time Input (ESTI):** When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: - To take the timestamp provided as status - To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time. 0x0 (DISABLE): External System Time Input is disabled. 0x1 (ENABLE): External System Time Input is enabled.
19	0h RW	**Enable checksum correction during OST for PTP over UDP/IPv4 packets (CSC):** When this bit is set, the last two bytes of PTP message sent over UDP/IPv4 is updated to keep the UDP checksum correct, for changes made to origin timestamp and/or correction field as part of one step timestamp operation. The application shall form the packet with these two dummy bytes. When reset, no updates are done to keep the UDP checksum correct. The application shall form the packet with UDP checksum set to 0. 0x0 (DISABLE): checksum correction during OST for PTP over UDP/IPv4 packets is disabled. 0x1 (ENABLE): checksum correction during OST for PTP over UDP/IPv4 packets is enabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Enable MAC Address for PTP Packet Filtering (TSENMACADDR):** When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. 0x0 (DISABLE): MAC Address for PTP Packet Filtering is disabled. 0x1 (ENABLE): MAC Address for PTP Packet Filtering is enabled.
17:16	0h RW	**Select PTP packets for Taking Snapshots (SNAPTYPSEL):** These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	0h RW	**Enable Snapshot for Messages Relevant to Master (TSMSTRENA):** When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. 0x0 (DISABLE): Snapshot for Messages Relevant to Master is disabled. 0x1 (ENABLE): Snapshot for Messages Relevant to Master is enabled.
14	0h RW	**Enable Timestamp Snapshot for Event Messages (TSEVNTENA):** When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. 0x0 (DISABLE): Timestamp Snapshot for Event Messages is disabled. 0x1 (ENABLE): Timestamp Snapshot for Event Messages is enabled.
13	1h RW	**Enable Processing of PTP Packets Sent over IPv4-UDP (TSIPV4ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv4-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv4-UDP is enabled.
12	0h RW	**Enable Processing of PTP Packets Sent over IPv6-UDP (TSIPV6ENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. 0x0 (DISABLE): Processing of PTP Packets Sent over IPv6-UDP is disabled. 0x1 (ENABLE): Processing of PTP Packets Sent over IPv6-UDP is enabled.
11	0h RW	**Enable Processing of PTP over Ethernet Packets (TSIPENA):** When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. 0x0 (DISABLE): Processing of PTP over Ethernet Packets is disabled. 0x1 (ENABLE): Processing of PTP over Ethernet Packets is enabled.
10	0h RW	**Enable PTP Packet Processing for Version 2 Format (TSVER2ENA):** When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. 0x0 (DISABLE): PTP Packet Processing for Version 2 Format is disabled. 0x1 (ENABLE): PTP Packet Processing for Version 2 Format is enabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Timestamp Digital or Binary Rollover Control (TSCTRLSSR):** When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. 0x0 (DISABLE): Timestamp Digital or Binary Rollover Control is disabled. 0x1 (ENABLE): Timestamp Digital or Binary Rollover Control is enabled.
8	0h RW	**Enable Timestamp for All Packets (TSENALL):** When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. 0x0 (DISABLE): Timestamp for All Packets disabled. 0x1 (ENABLE): Timestamp for All Packets enabled.
7	0h RO	**Reserved**
6	0h RW	**Presentation Time Generation Enable (PTGE):** When this bit is set the Presentation Time generation is enabled. 0x0 (DISABLE): Presentation Time Generation is disabled. 0x1 (ENABLE): Presentation Time Generation is enabled.
5	0h RW	**Update Addend Register (TSADDREG):** When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Addend Register is not updated. 0x1 (ENABLE): Addend Register is updated.
4	0h RO	**Reserved**
3	0h RW	**Update Timestamp (TSUPDT):** When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not updated. 0x1 (ENABLE): Timestamp is updated.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Initialize Timestamp (TSINIT):** When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is DWC_EQOS_FLEXI_PPS_OUT_EN=1 enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Timestamp is not initialized. 0x1 (ENABLE): Timestamp is initialized.
1	0h RW	**Fine or Coarse Timestamp Update (TSCFUPDT):** When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. 0x0 (COARSE): Coarse method is used to update system timestamp. 0x1 (FINE): Fine method is used to update system timestamp.
0	0h RW	**Enable Timestamp (TSENA):** When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. 0x0 (DISABLE): Timestamp is disabled. 0x1 (ENABLE): Timestamp is enabled.

14.20.3.300MAC_SUB_SECOND_INCREMENT — Offset 50220B04h

This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock.

Type	Size	Offset	Default
MMIO	32 bit	50220B04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**Sub-second Increment Value (SSINC):** The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:8	00h RW	**Sub-nanosecond Increment Value (SNSINC):** This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C.
7:0	0h RO	**Reserved**

14.20.3.301MAC_SYSTEM_TIME_SECONDS — Offset 50220B08h

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

Type	Size	Offset	Default
MMIO	32 bit	50220B08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Timestamp Second (TSS):** The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

14.20.3.302MAC_SYSTEM_TIME_NANOSECONDS — Offset 50220B0Ch

The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50220B0Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Timestamp Sub Seconds (TSSS):** The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

14.20.3.303MAC_SYSTEM_TIME_SECONDS_UPDATE — Offset 50220B10h

The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both registers before setting the TSINIT or TSUPDT bits in DWC_eqos_top_map/EQOS_MAC/MAC_Timestamp_Control.

Type	Size	Offset	Default
MMIO	32 bit	50220B10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Seconds (TSS):** The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

14.20.3.304MAC_SYSTEM_TIME_NANOSECONDS_UPDATE — Offset 50220B14h

MAC System Time Nanoseconds Update register.

Type	Size	Offset	Default
MMIO	32 bit	50220B14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Add or Subtract Time (ADDSUB):** When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. 0x0 (ADD): Add time. 0x1 (SUB): Subtract time.
30:0	00000000h RW	**Timestamp Sub Seconds (TSSS):** The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

14.20.3.305MAC_TIMESTAMP_ADDEND — Offset 50220B18h

Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register). The content of this register is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Type	Size	Offset	Default
MMIO	32 bit	50220B18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Addend Register (TSAR):** This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

14.20.3.306MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS — Offset 50220B1Ch

System Time - Higher Word Seconds register.

Type	Size	Offset	Default
MMIO	32 bit	50220B1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Timestamp Higher Word Register (TSHWR):** This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.

14.20.3.307MAC_TIMESTAMP_STATUS — Offset 50220B20h

Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register.

Type	Size	Offset	Default
MMIO	32 bit	50220B20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Number of Auxiliary Timestamp Snapshots (ATSNS):** This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	0h RO	**Auxiliary Timestamp Snapshot Trigger Missed (ATSSTM):** This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. 0x0 (INACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status detected.
23:20	0h RO	**Reserved**
19:16	0h RO	**Auxiliary Timestamp Snapshot Trigger Identifier (ATSSTN):** These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: - Bit 16: Auxiliary trigger 0 - Bit 17: Auxiliary trigger 1 - Bit 18: Auxiliary trigger 2 - Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15	0h RO	**Tx Timestamp Status Interrupt Status (TXTSSIS):** In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). 0x0 (INACTIVE): Tx Timestamp Status Interrupt status not detected. 0x1 (ACTIVE): Tx Timestamp Status Interrupt status detected.
14:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Timestamp Target Time Error (TSTRGTERR1):** This bit is set when the latest target time programmed in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.
4	0h RO	**Timestamp Target Time Reached for Target Time PPS1 (TSTARGT1):** When this bit is set and MCGREN1 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN1 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[1] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
3	0h RO	**Timestamp Target Time Error (TSTRGTERR0):** This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Target Time Error status not detected. 0x1 (ACTIVE): Timestamp Target Time Error status detected.
2	0h RO	**Auxiliary Timestamp Trigger Snapshot (AUXTSTRIG):** This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Auxiliary Timestamp Trigger Snapshot status not detected. 0x1 (ACTIVE): Auxiliary Timestamp Trigger Snapshot status detected.
1	0h RO	**Timestamp Target Time Reached (TSTARGT0):** When this bit is set and MCGREN0 of MAC_PPS_Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. When this bit is set and MCGREN0 of MAC_PPS_Control register is set, it indicates that mcgr_dma_req_o[0] is asserted. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
0	0h RO	**Timestamp Seconds Overflow (TSSOVF):** When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. 0x0 (INACTIVE): Timestamp Seconds Overflow status not detected. 0x1 (ACTIVE): Timestamp Seconds Overflow status detected.

14.20.3.308MAC_TX_TIMESTAMP_STATUS_NANOSECONDS — Offset 50220B30h

This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled.

The MAC_Tx_Timestamp_Status_Nanoseconds register, along with MAC_Tx_Timestamp_Status_Seconds, gives the 64-bit timestamp captured for the PTP packet successfully transmitted by the MAC. This value is considered to be read by the application when the last byte (bits[31:24]) of MAC_Tx_Timestamp_Status_Nanoseconds is read.

If the application does not read these registers and timestamp of another packet is captured, then either the current timestamp is lost (overwritten) or the new timestamp is lost (dropped), depending on the setting of the TXTSSTSM bit of the MAC_Timestamp_Control register. The status bit TXTSC bit [15] in MAC_Timestamp_Status register is set whenever the MAC transmitter captures the timestamp.

Type	Size	Offset	Default
MMIO	32 bit	50220B30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Transmit Timestamp Status Missed (TXTSSMIS):** When this bit is set, it indicates one of the following: - The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset - The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Transmit Timestamp Status Missed status not detected. 0x1 (ACTIVE): Transmit Timestamp Status Missed status detected.
30:0	00000000h RO	**Transmit Timestamp Status Low (TXTSSLO):** This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

14.20.3.309MAC_TX_TIMESTAMP_STATUS_SECONDS — Offset 50220B34h

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.

Type	Size	Offset	Default
MMIO	32 bit	50220B34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmit Timestamp Status High (TXTSSHI):** This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

14.20.3.310MAC_AUXILIARY_CONTROL — Offset 50220B40h

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.

Type	Size	Offset	Default
MMIO	32 bit	50220B40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Auxiliary Snapshot 1 Enable (ATSEN1):** This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
4	0h RW	**Auxiliary Snapshot 0 Enable (ATSEN0):** This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. 0x0 (DISABLE): Auxiliary Snapshot $i is disabled. 0x1 (ENABLE): Auxiliary Snapshot $i is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Auxiliary Snapshot FIFO Clear (ATSFC):** When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Auxiliary Snapshot FIFO Clear is disabled. 0x1 (ENABLE): Auxiliary Snapshot FIFO Clear is enabled.

14.20.3.311MAC_AUXILIARY_TIMESTAMP_NANOSECONDS — Offset 50220B48h

The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected while configuring the core.

You can store multiple snapshots in this FIFO. Bits[29:25] in MAC_Timestamp_Status indicate the fill-level of the FIFO. The top of the FIFO is removed only when the last byte (9bits[31:24]) of MAC_Auxiliary_Timestamp_Seconds register is read.

Type	Size	Offset	Default
MMIO	32 bit	50220B48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO	**Auxiliary Timestamp (AUXTSLO):** Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

14.20.3.312MAC_AUXILIARY_TIMESTAMP_SECONDS — Offset 50220B4Ch

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Type	Size	Offset	Default
MMIO	32 bit	50220B4Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Auxiliary Timestamp (AUXTSHI):** Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

14.20.3.313MAC_TIMESTAMP_INGRESS_ASYM_CORR — Offset 50220B50h

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	50220B50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Ingress Asymmetry Correction (OSTIAC):** This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

14.20.3.314MAC_TIMESTAMP_EGRESS_ASYM_CORR — Offset 50220B54h

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	50220B54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**One-Step Timestamp Egress Asymmetry Correction (OSTEAC):** This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000(2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216).

14.20.3.315MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND — Offset 50220B58h

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

Type	Size	Offset	Default
MMIO	32 bit	50220B58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Ingress Correction (TSIC):** This field contains the ingress path correction value as defined by the Ingress Correction expression.

14.20.3.316MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND — Offset 50220B5Ch

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

Type	Size	Offset	Default
MMIO	32 bit	50220B5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Timestamp Egress Correction (TSEC):** This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

14.20.3.317MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC — Offset 50220B60h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for ingress direction.

Type	Size	Offset	Default
MMIO	32 bit	50220B60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Ingress Correction, sub-nanoseconds (TSICSNS):** This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression.
7:0	0h RO	**Reserved**

14.20.3.318MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC — Offset 50220B64h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for egress direction.

Type	Size	Offset	Default
MMIO	32 bit	50220B64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Timestamp Egress Correction, sub-nanoseconds (TSECSNS):** This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression.
7:0	0h RO	**Reserved**

14.20.3.319MAC_TIMESTAMP_INGRESS_LATENCY — Offset 50220B68h

This register holds the Ingress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	50220B68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Ingress Timestamp Latency, in sub-nanoseconds (ITLNS):** This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	00h RO	**Ingress Timestamp Latency, in nanoseconds (ITLSNS):** This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	0h RO	**Reserved**

14.20.3.320MAC_TIMESTAMP_EGRESS_LATENCY — Offset 50220B6Ch

This register holds the Egress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	50220B6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO	**Egress Timestamp Latency, in nanoseconds (ETLNS):** This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	00h RO	**Egress Timestamp Latency, in sub-nanoseconds (ETLSNS):** This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	0h RO	**Reserved**

14.20.3.321MAC_PPS_CONTROL — Offset 50220B70h

PPS Control register. Bits[30:24] of this register are valid only when four Flexible PPS outputs are selected. Bits[22:16] are valid only when three or more Flexible PPS outputs are selected. Bits[14:8] are valid only when two or more Flexible PPS outputs are selected. Bits[6:4] are valid only when Flexible PPS feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50220B70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Time Select (TRGTMODSEL1):** When set, 64-bit PTP time is used to capture time at MCGR trigger[0] input. When reset, presentation time is used to capture time at trigger input, maintaining backward compatibility.
27:16	0h RO	**Reserved**
15	0h RW	**MCGR Mode Enable for PPS1 Output (MCGREN1):** This field enables the 1st PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (DISABLE): 1st PPS instance is disabled to operate in PPS or MCGR mode. 0x1 (ENABLE): 1st PPS instance is enabled to operate in PPS or MCGR mode.
14:13	0h RW	**Target Time Register Mode for PPS1 Output (TIMESEL):** This field indicates the Target Time registers (MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds) mode for PPS1 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT1 (MAC_Timestamp_Status[4]). 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
12	0h RO	**Reserved**
11:8	0h RW	**Flexible PPS1 Output Control (PPSCMD1):** This field controls the flexible PPS1 output signal. This field is similar to the PPSCMD0 field. If MCGREN1 is set, then PPSCMD1 indicated by these 4 bits [11:8] are taken as Presentation Time Control bits for media clock generation and recovery for comparator instance 1. This field is similar to the PPSCMD0 Presentation Time Control bits. If MCGREN1 is not set then only 3 bits from [10:8] is used as PPSCMD1 and the 4th bit is to be set as 0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**MCGR Mode Enable for PPS0 Output (MCGREN0):** This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode. 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Target Time Register Mode for PPS0 Output (TRGTMODSEL0):** Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal. 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding Pulse Per Second (PPS) output signal. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT0 (MAC_Timestamp_Status[1]) 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted.
4	0h RW	**Flexible PPS Output Mode Enable (PPSEN0):** When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). 0x0 (DISABLE): Flexible PPS Output Mode is disabled. 0x1 (ENABLE): Flexible PPS Output Mode is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**PPS Output Frequency Control (PPSCTRL_PPSCMD):** This field controls the frequency of the PPS0 output signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: - 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. - 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. - 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. - 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. - .. - 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output signal has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: - When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms - When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) - When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high) This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. or Flexible PPS Output Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: - 0000: No Command - 0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. - 0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. - 0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. - 0100: STOP Pulse train at time This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. - 0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). - 110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. - 0111-1111: Reserved or Presentation Time Control If MCGREN0 is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: - 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed - 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0100-1000: Reserved - 1001: Toggle output on compare - 1010: Pulse output low on compare for one PTP-clock cycle - 1011: Pulse output high on compare for one PTP-clock cycle - 1100-1111: Reserved

14.20.3.322MAC_PPS0_TARGET_TIME_SECONDS — Offset 50220B80h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	50220B80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH0):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

14.20.3.323MAC_PPS0_TARGET_TIME_NANOSECONDS — Offset 50220B84h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	50220B84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY0):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL0):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

14.20.3.324MAC_PPS0_INTERVAL — Offset 50220B88h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50220B88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT0):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

14.20.3.325MAC_PPS0_WIDTH — Offset 50220B8Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50220B8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH0):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

14.20.3.326MAC_PPS1_TARGET_TIME_SECONDS — Offset 50220B90h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	50220B90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Target Time Seconds Register (TSTRH1):** This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

14.20.3.327MAC_PPS1_TARGET_TIME_NANOSECONDS — Offset 50220B94h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	50220B94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PPS Target Time Register Busy (TRGTBUSY1):** The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected. 0x1 (ACTIVE): PPS Target Time Register Busy is detected.
30:0	00000000h RW	**Target Time Low for PPS Register (TTSL1):** This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

14.20.3.328MAC_PPS1_INTERVAL — Offset 50220B98h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50220B98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Interval (PPSINT1):** These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

14.20.3.329MAC_PPS1_WIDTH — Offset 50220B9Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	50220B9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPS Output Signal Width (PPSWIDTH1):** These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

14.20.3.330MAC_PTO_CONTROL — Offset 50220BC0h

This register controls the PTP Offload Engine operation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50220BC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Domain Number (DN):** This field indicates the domain Number in which the PTP node is operating.
7	0h RW	**Disable Peer Delay Response response generation (PDRDIS):** When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not be generated for received Peer Delay Request (Pdelay_Req) request packet, as required by the programmed mode. Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in Hardware and/or Pdelay_Resp generation is handled by Software. 0x0 (ENABLE): Peer Delay Response response generation is enabled. 0x1 (DISABLE): Peer Delay Response response generation is disabled.
6	0h RW	**Disable PTO Delay Request/Response response generation (DRRDIS):** When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode. 0x0 (ENABLE): PTO Delay Request/Response response generation is enabled. 0x1 (DISABLE): PTO Delay Request/Response response generation is disabled.
5	0h RW	**Automatic PTP Pdelay_Req message Trigger (APDREQTRIG):** When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP Pdelay_Req message Trigger is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message Trigger is enabled.
4	0h RW	**Automatic PTP SYNC message Trigger (ASYNCTRIG):** When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Automatic PTP SYNC message Trigger is disabled. 0x1 (ENABLE): Automatic PTP SYNC message Trigger is enabled.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Automatic PTP Pdelay_Req message Enable (APDREQEN):** When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode. 0x0 (DISABLE): Automatic PTP Pdelay_Req message is disabled. 0x1 (ENABLE): Automatic PTP Pdelay_Req message is enabled.
1	0h RW	**Automatic PTP SYNC message Enable (ASYNCEN):** When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Master mode. 0x0 (DISABLE): Automatic PTP SYNC message is disabled. 0x1 (ENABLE): Automatic PTP SYNC message is enabled.
0	0h RW	**PTP Offload Enable (PTOEN):** When this bit is set, the PTP Offload feature is enabled. 0x0 (DISABLE): PTP Offload feature is disabled. 0x1 (ENABLE): PTP Offload feature is enabled.

14.20.3.331MAC_SOURCE_PORT_IDENTITY0 — Offset 50220BC4h

This register contains Bits[31:0] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50220BC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 0 (SPI0):** This field indicates bits [31:0] of sourcePortIdentity of PTP node.

14.20.3.332MAC_SOURCE_PORT_IDENTITY1 — Offset 50220BC8h

This register contains Bits[63:32] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50220BC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Source Port Identity 1 (SPI1):** This field indicates bits [63:32] of sourcePortIdentity of PTP node.

14.20.3.333MAC_SOURCE_PORT_IDENTITY2 — Offset 50220BCCh

This register contains Bits[79:64] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50220BCCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Source Port Identity 2 (SPI2):** This field indicates bits [79:64] of sourcePortIdentity of PTP node.

14.20.3.334MAC_LOG_MESSAGE_INTERVAL — Offset 50220BD0h

This register contains the periodic intervals for automatic PTP packet generation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	50220BD0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**Log Min Pdelay_Req Interval (LMPDRI):** This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15.Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	0h RO	**Reserved**
10:8	0h RW	**DRSYNCR:** Delay_Req to SYNC Ratio In Slave mode, it is used for controlling frequency of Delay_Req messages transmitted. - 0: DelayReq generated for every received SYNC - 1: DelayReq generated every alternate reception of SYNC - 2: for every 4 SYNC messages - 3: for every 8 SYNC messages - 4: for every 16 SYNC messages - 5: for every 32 SYNC messages - 6-7: Reserved The master sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the slave. The GbE Controller Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Slave mode, the host must not write/update this register unless it has to override the received value. In Master mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. 0x0 (SYNC1): DelayReq generated for every received SYNC. 0x1 (SYNC2): DelayReq generated every alternate reception of SYNC. 0x2 (SYNC4): for every 4 SYNC messages. 0x3 (SYNC8): for every 8 SYNC messages. 0x4 (SYNC16): for every 16 SYNC messages. 0x5 (SYNC32): for every 32 SYNC messages. 0x6 (RSVD): Reserved.
7:0	00h RW	**LSI:** Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Master. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.

14.20.3.335MTL_OPERATION_MODE — Offset 50220C00h

The Operation Mode register establishes the Transmit and Receive operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	50220C00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Flexible Rx parser Enable (FRPE):** When this bit is set to 1, the Programmable Rx Parser functionality is enabled. When the Rx parser is disabled and if the Rx parser is in the middle of the parsing then it gets disabled only after completing the current packet parsing. When the Rx parser is enabled from disabled state then the Rx parser gets activated for the next immediate packet. 0x0 (DISABLE): Flexible Rx parser is disabled. 0x1 (ENABLE): Flexible Rx parser is enabled.
14	0h RW	**RxParser Software Error/Incomplete Parsing Packet Drop Enable (RXPED):** When set to 0, packets encountering software programming errors (NPE/NVE/frame offset overflow errors) or incomplete parsing are forwarded to application with the corresponding RxParser status. When set to 1, backward compatibility is maintained where all above mentioned packets are dropped (when RA is not set). 0x0 (DISABLE): Flexible Rx parser, packet drop in case software error is disabled. 0x1 (ENABLE): Flexible Rx parser, packet drop in case software error is enabled.
13:10	0h RO	**Reserved**
9	0h RW	**Counters Reset (CNTCLR):** When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters are not reset. 0x1 (ENABLE): All counters are reset.
8	0h RW	**Counters Preset (CNTPRST):** When this bit is set, - MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Counters Preset is disabled. 0x1 (ENABLE): Counters Preset is enabled.
7	0h RO	**Reserved**
6:5	0h RW	**Tx Scheduling Algorithm (SCHALG):** This field indicates the algorithm for Tx scheduling: 0x0 (WRR): WRR algorithm. 0x1 (WFQ): WFQ algorithm when DCB feature is selected.Otherwise, Reserved. 0x2 (DWRR): DWRR algorithm when DCB feature is selected.Otherwise, Reserved. 0x3 (SP): Strict priority algorithm.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RO	**Reserved**
2	0h RW	**Receive Arbitration Algorithm (RAA):** This field is used to select the arbitration algorithm for the Rx side. - 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. - 1: Weighted Strict Priority (WSP) 0x0 (SP): Strict priority (SP). 0x1 (WSP): Weighted Strict Priority (WSP).
1	0h RW	**Drop Transmit Status (DTXSTS):** When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. 0x0 (DISABLE): Drop Transmit Status is disabled. 0x1 (ENABLE): Drop Transmit Status is enabled.
0	0h RO	**Reserved**

14.20.3.336MTL_DBG_CTL — Offset 50220C08h

The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	50220C08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RW	**ECC Inject Error Control for Tx, Rx and TSO memories (EIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
16	0h RW	**ECC Inject Error Enable for Tx, Rx and TSO memories (EIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Tx, Rx and TSO memories is disabled. 0x1 (ENABLE): ECC Inject Error for Tx, Rx and TSO memories is enabled.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Transmit Status Available Interrupt Status Enable (STSIE):** When this bit is set, an interrupt is generated when Transmit status is available in slave mode. 0x0 (DISABLE): Transmit Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Transmit Packet Available Interrupt Status is enabled.
14	0h RW	**Receive Packet Available Interrupt Status Enable (PKTIE):** When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. 0x0 (DISABLE): Receive Packet Available Interrupt Status is disabled. 0x1 (ENABLE): Receive Packet Available Interrupt Status is enabled.
13:12	0h RW	**FIFO Selected for Access (FIFOSEL):** This field indicates the FIFO selected for debug access: 0x0 (TXFIFO): Tx FIFO. 0x1 (TXSTSFIFO): Tx Status FIFO (only read access when SLVMOD is set). 0x2 (TSOFIFO): TSO FIFO (cannot be accessed when SLVMOD is set). 0x3 (RXFIFO): Rx FIFO.
11	0h RW	**FIFO Write Enable (FIFOWREN):** When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Write is disabled. 0x1 (ENABLE): FIFO Write is enabled.
10	0h RW	**FIFO Read Enable (FIFORDEN):** When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): FIFO Read is disabled. 0x1 (ENABLE): FIFO Read is enabled.
9	0h RW	**Reset Pointers of Selected FIFO (RSTSEL):** When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset Pointers of Selected FIFO is disabled. 0x1 (ENABLE): Reset Pointers of Selected FIFO is enabled.
8	0h RW	**Reset All Pointers (RSTALL):** When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0x0 (DISABLE): Reset All Pointers is disabled. 0x1 (ENABLE): Reset All Pointers is enabled.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Encoded Packet State (PKTSTATE):** This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
4	0h RO	**Reserved**
3:2	0h RW	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
1	0h RW	**Debug Mode Access to FIFO (DBGMOD):** When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: - Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO - Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: - Write access to the Tx FIFO - Read access to the Rx FIFO and Tx Status FIFO 0x0 (DISABLE): Debug Mode Access to FIFO is disabled. 0x1 (ENABLE): Debug Mode Access to FIFO is enabled.
0	0h RW	**FIFO Debug Access Enable (FDBGEN):** When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. 0x0 (DISABLE): FIFO Debug Access is disabled. 0x1 (ENABLE): FIFO Debug Access is enabled.

14.20.3.337MTL_DBG_STS — Offset 50220C0Ch

The FIFO Debug Status register contains the status of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	50220C0Ch	00000018h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RO	**Remaining Locations in the FIFO (LOCR):** Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively.
14:10	0h RO	**Reserved**
9	0h RW	**Transmit Status Available Interrupt Status (STSI):** When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Transmit Status Available Interrupt Status not detected. 0x1 (ACTIVE): Transmit Status Available Interrupt Status detected.
8	0h RW	**Receive Packet Available Interrupt Status (PKTI):** When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. 0x0 (INACTIVE): Receive Packet Available Interrupt Status not detected. 0x1 (ACTIVE): Receive Packet Available Interrupt Status detected.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:3	3h RO	**Byte Enables (BYTEEN):** This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. 0x0 (B0_VAL): Byte 0 valid. 0x1 (B01_VAL): Byte 0 and Byte 1 are valid. 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid. 0x3 (B0123_VAL): All four bytes are valid.
2:1	0h RO	**Encoded Packet State (PKTSTATE):** This field is used to get the control or status information of the selected FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. 0x0 (PKT_DATA): Packet Data. 0x1 (CW_NS): Control Word/Normal Status. 0x2 (SOP_LS): SOP Data/Last Status. 0x3 (EOP): EOP Data/EOP.
0	0h RO	**FIFO Busy (FIFOBUSY):** When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: - All other fields of this register - All fields of the MTL_FIFO_Debug_Data register 0x0 (INACTIVE): FIFO Busy not detected. 0x1 (ACTIVE): FIFO Busy detected.

14.20.3.338MTL_FIFO_DEBUG_DATA — Offset 50220C10h

The FIFO Debug Data register contains the data to be written to or read from the FIFOs.

Type	Size	Offset	Default
MMIO	32 bit	50220C10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FIFO Debug Data (FDBGDATA):** During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

14.20.3.339MTL_INTERRUPT_STATUS — Offset 50220C20h

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50220C20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MTL Rx Parser Interrupt Status (MTLPIS):** This bit indicates that there is an interrupt from Rx Parser Block. To reset this bit, the application must read the MTL_ Rxp_Interrupt_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Rx Parser Interrupt status not detected. 0x1 (ACTIVE): MTL Rx Parser Interrupt status detected.
22:19	0h RO	**Reserved**
18	0h RO	**EST (TAS- 802.1Qbv) Interrupt Status (ESTIS):** This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt. 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected. 0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Debug Interrupt status (DBGIS):** This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Debug Interrupt status not detected. 0x1 (ACTIVE): Debug Interrupt status detected.
16:8	0h RO	**Reserved**
7	0h RO	**Queue 7 Interrupt status (Q7IS):** This bit indicates that there is an interrupt from Queue 7. To reset this bit, the application must read the MTL_Q7_Interrupt_Control_Status Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 7 Interrupt status not detected. 0x1 (ACTIVE): Queue 7 Interrupt status detected.
6	0h RO	**Queue 6 Interrupt status (Q6IS):** This bit indicates that there is an interrupt from Queue 6. To reset this bit, the application must read the MTL_Q6_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 6 Interrupt status not detected. 0x1 (ACTIVE): Queue 6 Interrupt status detected.
5	0h RO	**Queue 5 Interrupt status (Q5IS):** This bit indicates that there is an interrupt from Queue 5. To reset this bit, the application must read the MTL_Q5_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 5 Interrupt status not detected. 0x1 (ACTIVE): Queue 5 Interrupt status detected.
4	0h RO	**Queue 4 Interrupt status (Q4IS):** This bit indicates that there is an interrupt from Queue 4. To reset this bit, the application must read the MTL_Q4_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 4 Interrupt status not detected. 0x1 (ACTIVE): Queue 4 Interrupt status detected.
3	0h RO	**Queue 3 Interrupt status (Q3IS):** This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 3 Interrupt status not detected. 0x1 (ACTIVE): Queue 3 Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Queue 2 Interrupt status (Q2IS):** This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 2 Interrupt status not detected. 0x1 (ACTIVE): Queue 2 Interrupt status detected.
1	0h RO	**Queue 1 Interrupt status (Q1IS):** This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 1 Interrupt status not detected. 0x1 (ACTIVE): Queue 1 Interrupt status detected.
0	0h RO	**Queue 0 Interrupt status (Q0IS):** This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): Queue 0 Interrupt status not detected. 0x1 (ACTIVE): Queue 0 Interrupt status detected.

14.20.3.340MTL_RXQ_DMA_MAP0 — Offset 50220C30h

The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	50220C30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection (Q3DDMACH):** When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]). 0x0 (DISABLE): Queue 3 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 3 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**Queue 3 Mapped to DMA Channel (Q3MDMACH):** This field controls the routing of the received packet in Queue 3 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. Note: The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved
23:21	0h RO	**Reserved**
20	0h RW	**Queue 2 Enabled for DA-based DMA Channel Selection (Q2DDMACH):** When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]). 0x0 (DISABLE): Queue 2 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 2 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**
18:16	0h RW	**Queue 2 Mapped to DMA Channel (Q2MDMACH):** This field controls the routing of the received packet in Queue 2 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 1 Enabled for DA-based DMA Channel Selection (Q1DDMACH):** When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]). 0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Queue 1 Mapped to DMA Channel (Q1MDMACH):** This field controls the routing of the received packet in Queue 1 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**
4	0h RW	**Queue 0 Enabled for DA-based DMA Channel Selection (Q0DDMACH):** When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field. 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 0 Mapped to DMA Channel (Q0MDMACH):** This field controls the routing of the packet received in Queue 0 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

14.20.3.341MTL_RXQ_DMA_MAP1 — Offset 50220C34h

The Receive Queue and DMA Channel Mapping 1 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	50220C34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Queue 7 Enabled for DA-based DMA Channel Selection (Q7DDMACH):** When set, this bit indicates that the packets received in Queue 7 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 7 are routed to the DMA Channel programmed in the Q7MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
27	0h RO	**Reserved**
26:24	0h RW	**Queue 7 Mapped to DMA Channel (Q7MDMACH):** This field controls the routing of the packet received in Queue 7 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q7DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
23:21	0h RO	**Reserved**
20	0h RW	**Queue 6 Enabled for DA-based DMA Channel Selection (Q6DDMACH):** When set, this bit indicates that the packets received in Queue 6 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 6 are routed to the DMA Channel programmed in the Q6MDMACH field. 0x0 (DISABLE): Queue 6 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 6 enabled for DA-based DMA Channel Selection.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RW	**Queue 6 Mapped to DMA Channel (Q6MDMACH):** This field controls the routing of the packet received in Queue 6 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q6DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
15:13	0h RO	**Reserved**
12	0h RW	**Queue 5 Enabled for DA-based DMA Channel Selection (Q5DDMACH):** When set, this bit indicates that the packets received in Queue 5 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 5 are routed to the DMA Channel programmed in the Q5MDMACH field. 0x0 (DISABLE): Queue 5 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 5 enabled for DA-based DMA Channel Selection.
11	0h RO	**Reserved**
10:8	0h RW	**Queue 5 Mapped to DMA Channel (Q5MDMACH):** This field controls the routing of the packets received in Queue 5 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q5DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Queue 4 Enabled for DA-based DMA Channel Selection (Q4DDMACH):** When set, this bit indicates that the packets received in Queue 4 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 4 are routed to the DMA Channel programmed in the Q4MDMACH field. 0x0 (DISABLE): Queue 4 disabled for DA-based DMA Channel Selection. 0x1 (ENABLE): Queue 4 enabled for DA-based DMA Channel Selection.
3	0h RO	**Reserved**
2:0	0h RW	**Queue 4 Mapped to DMA Channel (Q4MDMACH):** This field controls the routing of the packet received in Queue 4 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q4DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

14.20.3.342MTL_TBS_CTRL — Offset 50220C40h

This register controls the operation of Time Based Scheduling.

Type	Size	Offset	Default
MMIO	32 bit	50220C40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**Launch Expiry Offset (LEOS):** The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Launch Expiry GSN Offset (LEGOS):** The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	**Reserved**
1	0h RW	**Launch Expiry Offset Valid (LEOV):** When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time. 0x0 (INVALID): LEOS field is invalid. 0x1 (VALID): LEOS field is valid.
0	0h RW	**EST offset Mode (ESTM):** When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8]. 0x0 (DISABLE): EST offset Mode is disabled. 0x1 (ENABLE): EST offset Mode is enabled.

14.20.3.343MTL_EST_CONTROL — Offset 50220C50h

This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	50220C50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PTP Time Offset Value (PTOV):** The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23:12	000h RW	**Current Time Offset Value (CTOV):** Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Time Interval Left Shift Amount (TILS):** This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. - 000: No left shift needed (equal to x1ns) - 001: Left shift TI by 1 bit (equal to x2ns) - 010: Left shift TI by 2 bits (equal to x4ns) - . - . - 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.
7:6	0h RW	**Loop Count to report Scheduling Error (LCSE):** Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register. 0x0 (M_4_ITERNS): 4 iterations. 0x1 (M_8_ITERNS): 8 iterations. 0x2 (M_16_ITERNS): 16 iterations. 0x3 (M_32_ITERNS): 32 iterations.
5	0h RW	**Drop Frames causing Scheduling Error (DFBS):** When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped. 0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error. 0x1 (DROP): Drop Frames causing Scheduling Error.
4	0h RW	**Do not Drop frames during Frame Size Error (DDBF):** When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register). 0x0 (DROP): Drop frames during Frame Size Error. 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error.
3:2	0h RO	**Reserved**
1	0h RW	**Switch to S/W owned list (SSWL):** When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Switch to S/W owned list is disabled. 0x1 (ENABLE): Switch to S/W owned list is enabled.
0	0h RW	**Enable EST (EEST):** When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. If any uncorrectable error is detected in the EST memory the hardware resets this bit and disables the EST function. 0x0 (DISABLE): EST is disabled. 0x1 (ENABLE): EST is enabled.

14.20.3.344MTL_EST_STATUS — Offset 50220C58h

This register provides Status related to Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	50220C58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Current GCL Slot Number (CGSN):** Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:8	00h RO	**BTR Error Loop Count (BTRL):** Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "11111111" indicates the iterations exceeded the value of 128 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	0h RO	**S/W owned list (SWOL):** When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default. 0x0 (INACTIVE): Gate control list number "0" is owned by software. 0x1 (ACTIVE): Gate control list number "1" is owned by software.
6:5	0h RO	**Reserved**
4	0h RW	**Constant Gate Control Error (CGCE):** This error occurs when the list length (LLR) is 1 and the Cycle Time (CTR) is less than or equal to the programmed Time Interval (TI) value after the optional Left Shifting. The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Constant Gate Control Error not detected. 0x1 (ACTIVE): Constant Gate Control Error detected.
3	0h RO	**Head-Of-Line Blocking due to Scheduling (HLBS):** Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Head-Of-Line Blocking due to Frame Size (HLBF):** Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros. 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected. 0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected.
1	0h RW	**BTR Error (BTRE):** When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "11111111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "11111111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): BTR Error not detected. 0x1 (ACTIVE): BTR Error detected.
0	0h RW	**Switch to S/W owned list Complete (SWLC):** When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Switch to S/W owned list Complete not detected. 0x1 (ACTIVE): Switch to S/W owned list Complete detected.

14.20.3.345MTL_EST_SCH_ERROR — Offset 50220C60h

This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout).

Type	Size	Offset	Default
MMIO	32 bit	50220C60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Schedule Error Queue Number (SEQN):** The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

14.20.3.346MTL_EST_FRM_SIZE_ERROR — Offset 50220C64h

This register provides the One Hot encoded Queue Numbers that are having the Frame Size related error.

Type	Size	Offset	Default
MMIO	32 bit	50220C64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Frame Size Error Queue Number (FEQN):** The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

14.20.3.347MTL_EST_FRM_SIZE_CAPTURE — Offset 50220C68h

This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error.

Type	Size	Offset	Default
MMIO	32 bit	50220C68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO	**Queue Number of HLBF (HBFQ):** Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	0h RO	**Reserved**
14:0	0000h RO	**Frame Size of HLBF (HBFS):** Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

14.20.3.348MTL_EST_INTR_ENABLE — Offset 50220C70h

This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status register.

Type	Size	Offset	Default
MMIO	32 bit	50220C70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**Interrupt Enable for CGCE (CGCE):** When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt 0x0 (DISABLE): Interrupt for CGCE is disabled. 0x1 (ENABLE): Interrupt for CGCE is enabled.
3	0h RW	**Interrupt Enable for HLBS (IEHS):** When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBS is disabled. 0x1 (ENABLE): Interrupt for HLBS is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt Enable for HLBF (IEHF):** When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for HLBF is disabled. 0x1 (ENABLE): Interrupt for HLBF is enabled.
1	0h RW	**Interrupt Enable for BTR Error (IEBE):** When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for BTR Error is disabled. 0x1 (ENABLE): Interrupt for BTR Error is enabled.
0	0h RW	**Interrupt Enable for Switch List (IECC):** When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt. 0x0 (DISABLE): Interrupt for Switch List is disabled. 0x1 (ENABLE): Interrupt for Switch List is enabled.

14.20.3.349MTL_EST_GCL_CONTROL — Offset 50220C80h

This register provides the control information for reading/writing to the Gate Control lists.

Type	Size	Offset	Default
MMIO	32 bit	50220C80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**ECC Inject Error Control for EST Memory (ESTEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
21	0h RW	**EST ECC Inject Error Enable (ESTEIEE):** When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): EST ECC Inject Error is disabled. 0x1 (ENABLE): EST ECC Inject Error is enabled.
20:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16:8	000h RW	**Gate Control List Address: (GCLA when GCRR is "0"). (ADDR):** Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. - 000: BTR Low (31:0) - 001: BTR High (63:31) - 010: CTR Low (31:0) - 011: CTR High (39:32) - 100: TER (31:0) - 101: LLR (n:0) (where n is (log{512} / log2)) - Others: Reserved
7:6	0h RO	**Reserved**
5	0h RW	**Debug Mode Bank Select (DBGB):** When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used. 0x0 (BANK0): R/W in debug mode should be directed to Bank 0. 0x1 (BANK1): R/W in debug mode should be directed to Bank 1.
4	0h RW	**Debug Mode (DBGM):** When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use. 0x0 (DISABLE): Debug Mode is disabled. 0x1 (ENABLE): Debug Mode is enabled.
3	0h RO	**Reserved**
2	0h RW	**Gate Control Related Registers (GCRR):** When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA. 0x0 (DISABLE): Gate Control Related Registers are disabled. 0x1 (ENABLE): Gate Control Related Registers are enabled.
1	0h RW	**Read '1', Write '0': (R1W0):** When set to '1': Read Operation When set to '0': Write Operation. 0x0 (WRITE): Write Operation. 0x1 (READ): Read Operation.
0	0h RW	**Start Read/Write Op (SRWO):** When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Start Read/Write Op disabled. 0x1 (ENABLE): Start Read/Write Op enabled.

14.20.3.350MTL_EST_GCL_DATA — Offset 50220C84h

This register holds the read data or write data in case of reads and writes respectively.

Type	Size	Offset	Default
MMIO	32 bit	50220C84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Gate Control Data (GCD):** The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

14.20.3.351MTL_FPE_CTRL_STS — Offset 50220C90h

This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br).

Type	Size	Offset	Default
MMIO	32 bit	50220C90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**HRS:** Hold/Release Status - 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. - 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State.
27:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**Preemption Classification (PEC):** When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	0h RO	**Reserved**
1:0	0h RW	**Additional Fragment Size (AFSZ):** used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes

14.20.3.352MTL_FPE_ADVANCE — Offset 50220C94h

This register holds the Hold and Release Advance time.

Type	Size	Offset	Default
MMIO	32 bit	50220C94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Release Advance (RADV):** The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.
15:0	0000h RW	**Hold Advance (HADV):** The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

14.20.3.353MTL_RXP_CONTROL_STATUS — Offset 50220CA0h

The MTL_RXP_Control_Status register establishes the operating mode of Rx Parser and provides some status.

Type	Size	Offset	Default
MMIO	32 bit	50220CA0h	80FF00FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**RX Parser in Idle state (RXPI):** This status bit is set to 1 when the Rx parser is in Idle State and waiting for a new packet for processing. This bit is used as a handshake with software when parser gets disables. After disabling, when bit is set then software can update the Rx parser instruction table. 0x0 (INACTIVE): RX Parser not in Idle state. 0x1 (ACTIVE): RX Parser in Idle state.
30:24	0h RO	**Reserved**
23:16	FFh RW	**Number of parsable entries in the Instruction table (NPE):** This control indicates the number of parsable entries in the Instruction Memory. This is used in Rx parser logic to detect programming Error. In case number of parsed entries for a packet is more than this entry then NPEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set.
15:8	0h RO	**Reserved**
7:0	FFh RW	**Number of valid entry address/index in the Instruction table (NVE):** This control indicates the number of valid entries address/index in the Instruction Memory (i.e. when NVE field in register=31, the maximum valid entry address is NVE+1 i.e. addresses/indices=0 to 32, or 33 entries). This is used in Rx parser logic to detect any programming Error. In case while parsing Table address (memory address) found to be more than this maximum valid entry address then NVEOVIS bit in the MTL_RXP_Interrupt_Control_Status register is set. Note: The minimum value of this should be 2.

14.20.3.354MTL_RXP_INTERRUPT_CONTROL_STATUS — Offset 50220CA4h

The MTL_RXP_Interrupt_Control_Status registers provides enable control for the interrupts and provides interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	50220CA4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Packet Drop due to RF Interrupt Enable (PDRFIE):** When this bit is set, the PDRFIS interrupt is enabled. When this bit is reset, the PDRFIS interrupt is disabled. 0x0 (DISABLE): Packet Drop due to RF Interrupt is disabled. 0x1 (ENABLE): Packet Drop due to RF Interrupt is enabled.
18	0h RW	**Frame Offset Overflow Interrupt Enable (FOOVIE):** When this bit is set, the FOOVIS interrupt is enabled. When this bit is reset, the FOOVIS interrupt is disabled. 0x0 (DISABLE): Frame Offset Overflow Interrupt is disabled. 0x1 (ENABLE): Frame Offset Overflow Interrupt is enabled.
17	0h RW	**Number of Parsable Entries Overflow Interrupt Enable (NPEOVIE):** When this bit is set, the NPEOVIS interrupt is enabled. When this bit is reset, the NPEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Parsable Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Parsable Entries Overflow Interrupt is enabled.
16	0h RW	**Number of Valid Entries Overflow Interrupt Enable (NVEOVIE):** When this bit is set, the NVEOVIS interrupt is enabled. When this bit is reset, the NVEOVIS interrupt is disabled. 0x0 (DISABLE): Number of Valid Entries Overflow Interrupt is disabled. 0x1 (ENABLE): Number of Valid Entries Overflow Interrupt is enabled.
15:4	0h RO	**Reserved**
3	0h RW	**Packet Dropped due to RF Interrupt Status (PDRFIS):** If the Rx Parser result says to drop the packet by setting RF=1 in the instruction memory, then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Packet Dropped due to RF Interrupt Status not detected. 0x1 (ACTIVE): Packet Dropped due to RF Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Frame Offset Overflow Interrupt Status (FOOVIS):** While parsing if the Instruction table entry's 'Frame Offset' found to be more than EOF offset, then then this bit is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Frame Offset Overflow Interrupt Status not detected. 0x1 (ACTIVE): Frame Offset Overflow Interrupt Status detected.
1	0h RW	**Number of Parsable Entries Overflow Interrupt Status (NPEOVIS):** While parsing a packet if the number of parsed entries found to be more than NPE[] (Number of Parseable Entries in MTL_RXP_Control register),then this bit is set to 1. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Parsable Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Parsable Entries Overflow Interrupt Status detected.
0	0h RW	**Number of Valid Entry Address/Index Overflow Interrupt Status (NVEOVIS):** While parsing if the Instruction address found to be more than NVE (Number of Valid Entry Address/index in MTL_RXP_Control register), then this bit is set to 1. For example, when NVE field in register=31, the maximum valid entry address/index is NVE+1 i.e. 32 (addresses/indices=0 to 32, or 33 entries), so NVEOVIS is set when currently processed entry indicates next address is 33 or more i.e. 34th or later entries. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Number of Valid Entries Overflow Interrupt Status not detected. 0x1 (ACTIVE): Number of Valid Entries Overflow Interrupt Status detected.

14.20.3.355MTL_RXP_DROP_CNT — Offset 50220CA8h

The MTL_RXP_Drop_Cnt register provides the drop count of Rx Parser initiated drops.

Type	Size	Offset	Default
MMIO	32 bit	50220CA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Drop Counter Overflow Bit (RXPDCOVF):** When set, this bit indicates that the MTL_RXP_Drop_cnt (RXPDC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Drop count overflow not occurred. 0x1 (ACTIVE): Rx Parser Drop count overflow occurred.
30:0	00000000h RO	**Rx Parser Drop count (RXPDC):** This 31-bit counter is implemented whenever a Rx Parser Drops a packet due to RF =1. The counter is cleared when the register is read.

14.20.3.356MTL_RXP_ERROR_CNT — Offset 50220CACh

The MTL_RXP_Error_Cnt register provides the Rx Parser related error occurrence count.

Type	Size	Offset	Default
MMIO	32 bit	50220CACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Error Counter Overflow Bit (RXPECOVF):** When set, this bit indicates that the MTL_RXP_Error_cnt (RXPEC) Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Error count overflow not occurred. 0x1 (ACTIVE): Rx Parser Error count overflow occurred.
30:0	00000000h RO	**Rx Parser Error count (RXPEC):** This 31-bit counter is implemented whenever a Rx Parser encounters following Error scenarios - Entry address >= NVE[] - Number Parsed Entries >= NPE[] - Entry address > EOF data entry address The counter is cleared when the register is read.

14.20.3.357MTL_RXP_INDIRECT_ACC_CONTROL_STATUS — Offset 50220CB0h

The MTL_RXP_Indirect_Acc_Control_Status register provides the Indirect Access control and status for Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	50220CB0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**FRP Instruction Table Access Busy (STARTBUSY):** When this bit is set to 1 by the software then it indicates to start the Read/Write operation from/to the Rx Parser Memory. Software should read this bit as 0 before issuing read or write request to access the Parser Memory Instructions. This bit when set to 1 indicates that hardware is busy until its gets cleared by hardware and software should not issue any read or write operation. 0x0 (INACTIVE): hardware not busy. 0x1 (ACTIVE): hardware is busy (Read/Write operation from/to the Rx Parser Memory).
30:23	0h RO	**Reserved**
22:21	0h RW	**ECC Inject Error Control for Rx Parser Memory (RXPEIEC):** When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. 0x0 (M_1BIT): Insert 1 bit error. 0x1 (M_2BIT): Insert 2 bit errors. 0x2 (M_3BIT): Insert 3 bit errors. 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field.
20	0h RW	**ECC Inject Error Enable for Rx Parser Memory (RXPEIEE):** When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature. 0x0 (DISABLE): ECC Inject Error for Rx Parser Memory is disabled. 0x1 (ENABLE): ECC Inject Error for Rx Parser Memory is enabled.
19:17	0h RO	**Reserved**
16	0h RW	**Read Write Control (WRRDN):** When this bit is set to 1 indicates the write operation to the Rx Parser Memory. When this bit is set to 0 indicates the read operation to the Rx Parser Memory. 0x0 (READ): Read operation to the Rx Parser Memory. 0x1 (WRITE): Write operation to the Rx Parser Memory.
15:10	0h RO	**Reserved**
9:0	000h RW	**FRP Instruction Table Offset Address (ADDR):** This field indicates the ADDR of the 32-bit entry in Rx parser instruction table. Each entry has 128-bit (4x32-bit words). There are 256 FRP entries. This must be written by the software before issuing any Read/Write command. The hardware does not support auto-increment of ADDR.

14.20.3.358MTL_RXP_INDIRECT_ACC_DATA — Offset 50220CB4h

The MTL_RXP_Indirect_Acc_Data registers holds the data associated to Indirect Access to Rx Parser memory.

Type	Size	Offset	Default
MMIO	32 bit	50220CB4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**FRP Instruction Table Write/Read Data (DATA):** Software should write this register before issuing any write command. The hardware provides the read data from the Rx Parser Memory for read operation when STARTBUSY =0 after read command.

14.20.3.359MTL_ECC_CONTROL — Offset 50220CC0h

The MTL_ECC_Control register establishes the operating mode of ECC related to MTL memories.

Type	Size	Offset	Default
MMIO	32 bit	50220CC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**MTL ECC Error Address Status Over-ride (MEEAO):** When set, the following error address fields hold the last valid address where the error is detected. When reset, the following error address fields hold the first address where the error is detected. EUEAS/ECEAS of MTL_ECC_Err_Addr_Status register. 0x0 (DISABLE): MTL ECC Error Address Status Over-ride is disabled. 0x1 (ENABLE): MTL ECC Error Address Status Over-ride is enabled.
7:5	0h RO	**Reserved**
4	0h RW	**TSO memory ECC Enable (TSOEE):** When set to 1, enables the ECC feature for TSO memory in DMA. When set to zero, disables the ECC feature for TSO memory in DMA. 0x0 (DISABLE): TSO memory ECC is disabled. 0x1 (ENABLE): TSO memory ECC is enabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**MTL Rx Parser ECC Enable (MRXPEE):** When set to 1, enables the ECC feature for Rx Parser memory. When set to zero, disables the ECC feature for Rx Parser memory. 0x0 (DISABLE): MTL Rx Parser ECC is disabled. 0x1 (ENABLE): MTL Rx Parser ECC is enabled.
2	0h RW	**MTL EST ECC Enable (MESTEE):** When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory. 0x0 (DISABLE): MTL EST ECC is disabled. 0x1 (ENABLE): MTL EST ECC is enabled.
1	0h RW	**MTL Rx FIFO ECC Enable (MRXEE):** When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory. 0x0 (DISABLE): MTL Rx FIFO ECC is disabled. 0x1 (ENABLE): MTL Rx FIFO ECC is enabled.
0	0h RW	**MTL Tx FIFO ECC Enable (MTXEE):** When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory. 0x0 (DISABLE): MTL Tx FIFO ECC is disabled. 0x1 (ENABLE): MTL Tx FIFO ECC is enabled.

14.20.3.360MTL_SAFETY_INTERRUPT_STATUS — Offset 50220CC4h

The MTL_Safety_Interrupt_Status registers provides Safety interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	50220CC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO	**MTL ECC Uncorrectable error Interrupt Status (MEUIS):** This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**MTL ECC Correctable error Interrupt Status (MECIS):** This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register. 0x0 (INACTIVE): MTL ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL ECC Correctable error Interrupt Status detected.

14.20.3.361MTL_ECC_INTERRUPT_ENABLE — Offset 50220CC8h

The MTL_ECC_Interrupt_Enable register provides enable bits for the ECC interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50220CC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Rx Parser memory Correctable Error Interrupt Enable (RPCEIE):** When set, generates an interrupt when an uncorrectable error is detected at the Rx Parser memory interface. It is indicated in RPCES status bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx Parser memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx Parser memory Correctable Error Interrupt is enabled.
11:9	0h RO	**Reserved**
8	0h RW	**EST memory Correctable Error Interrupt Enable (ECEIE):** When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): EST memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): EST memory Correctable Error Interrupt is enabled.
7:5	0h RO	**Reserved**
4	0h RW	**Rx memory Correctable Error Interrupt Enable (RXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Rx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Rx memory Correctable Error Interrupt is enabled.
3:1	0h RO	**Reserved**
0	0h RW	**Tx memory Correctable Error Interrupt Enable (TXCEIE):** When set, generates an interrupt when a correctable error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): Tx memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): Tx memory Correctable Error Interrupt is enabled.

14.20.3.362MTL_ECC_INTERRUPT_STATUS — Offset 50220CCCh

The MTL_ECC_Interrupt_Status register provides MTL ECC Interrupt Status.

Type	Size	Offset	Default
MMIO	32 bit	50220CCCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**Rx Parser memory Uncorrectable Error Status (RPUES):** When set, indicates that an uncorrectable error is detected at Rx Parser memory interface. 0x0 (INACTIVE): Rx Parser memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): Rx Parser memory Uncorrectable Error Status detected.
13	0h RW	**MTL Rx Parser memory Address Mismatch Status (RPAMS):** This bit when set indicates that address mismatch is found for address bus of Rx Parser memory. 0x0 (INACTIVE): MTL Rx Parser memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Address Mismatch Status detected.
12	0h RW	**MTL Rx Parser memory Correctable Error Status (RPCES):** This bit when set indicates that correctable error is detected at RX Parser memory interface. 0x0 (INACTIVE): MTL Rx Parser memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx Parser memory Correctable Error Status detected.
11	0h RO	**Reserved**
10	0h RW	**MTL EST memory Uncorrectable Error Status (EUES):** When set, indicates that an uncorrectable error is detected at MTL EST memory interface. 0x0 (INACTIVE): MTL EST memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Uncorrectable Error Status detected.
9	0h RW	**MTL EST memory Address Mismatch Status (EAMS):** This bit when set indicates that address mismatch is found for address bus of MTL EST memory. 0x0 (INACTIVE): MTL EST memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL EST memory Address Mismatch Status detected.
8	0h RW	**MTL EST memory Correctable Error Status (ECES):** This bit when set indicates that correctable error is detected at the MTL EST memory. 0x0 (INACTIVE): MTL EST memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL EST memory Correctable Error Status detected.
7	0h RO	**Reserved**
6	0h RW	**MTL Rx memory Uncorrectable Error Status (RXUES):** When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface. 0x0 (INACTIVE): MTL Rx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory Uncorrectable Error Status detected.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**MTL Rx memory Address Mismatch Status (RXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Rx memory Address Mismatch Status detected.
4	0h RW	**MTL Rx memory Correctable Error Status (RXCES):** This bit when set indicates that correctable error is detected at the MTL Rx memory. 0x0 (INACTIVE): MTL Rx memory correctable Error Status not detected. 0x1 (ACTIVE): MTL Rx memory correctable Error Status detected.
3	0h RO	**Reserved**
2	0h RW	**MTL Tx memory Uncorrectable Error Status (TXUES):** When set, indicates that an uncorrectable error is detected at the MTL TX memory interface. 0x0 (INACTIVE): MTL Tx memory Uncorrectable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Uncorrectable Error Status detected.
1	0h RW	**MTL Tx memory Address Mismatch Status (TXAMS):** This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Address Mismatch Status not detected. 0x1 (ACTIVE): MTL Tx memory Address Mismatch Status detected.
0	0h RW	**MTL Tx memory Correctable Error Status (TXCES):** This bit when set indicates that a correctable error is detected at the MTL Tx memory. 0x0 (INACTIVE): MTL Tx memory Correctable Error Status not detected. 0x1 (ACTIVE): MTL Tx memory Correctable Error Status detected.

14.20.3.363MTL_ECC_ERR_STS_RCTL — Offset 50220CD0h

The MTL_ECC_Err_Sts_Rctl register establishes the control for ECC Error status capture.

Type	Size	Offset	Default
MMIO	32 bit	50220CD0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**Clear Uncorrectable Error Status (CUES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Uncorrectable Error Status not detected. 0x1 (ACTIVE): Clear Uncorrectable Error Status detected.
4	0h RW	**Clear Correctable Error Status (CCES):** When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared. 0x0 (INACTIVE): Clear Correctable Error Status not detected. 0x1 (ACTIVE): Clear Correctable Error Status detected.
3:1	0h RW	**MTL ECC Memory Selection (EMS):** When EESRE bit of this register is set, this field indicates which memory's error status value to be read. The memory selection encoding is as described below. 0x0 (TX_MEM): MTL Tx memory. 0x1 (RX_MEM): MTL Rx memory. 0x2 (EST_MEM): MTL EST memory. 0x3 (RXP_MEM): MTL Rx Parser memory. 0x4 (TSO_MEM): DMA TSO memory.
0	0h RW	**MTL ECC Error Status Read Enable (EESRE):** When this bit is set, based on the EMS field of this register, the respective memory's error status values are captured as described: - The correctable and uncorrectable error count values are captured into MTL_ECC_Err_Cnt_Status register - The address location's of correctable and uncorrectable errors are captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers. 0x0 (DISABLE): MTL ECC Error Status Read is disabled. 0x1 (ENABLE): MTL ECC Error Status Read is enabled.

14.20.3.364MTL_ECC_ERR_ADDR_STATUS — Offset 50220CD4h

The MTL_ECC_Err_Addr_Status register provides the memory addresses for the correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	50220CD4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**MTL ECC Uncorrectable Error Address Status (EUEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected.
15:0	0000h RO	**MTL ECC Correctable Error Address Status (ECEAS):** Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected.

14.20.3.365MTL_ECC_ERR_CNTR_STATUS — Offset 50220CD8h

The MTL_ECC_Err_Cntr_Status register provides ECC Error count for Correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	50220CD8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO	**MTL ECC Uncorrectable Error Counter Status (EUECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's uncorrectable error count value.
15:8	0h RO	**Reserved**
7:0	00h RO	**MTL ECC Correctable Error Counter Status (ECECS):** Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value.

14.20.3.366MTL_DPP_CONTROL — Offset 50220CE0h

The MTL_DPP_Control establishes the operating mode of Data Parity protection and error injection.

Type	Size	Offset	Default
MMIO	32 bit	50220CE0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**Insert Parity error in CSR Read data parity generator (IPECW):** When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in AXI slave Interface Data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in CSR Read data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in CSR Read data parity generator is enabled.
12	0h RW	**Insert Parity error in AXI Slave Write data parity generator (IPEASW):** When set to 1, parity bit of first valid data generated by the AXI parity generator is (or at PG9 as shown in AXI slave Interface Data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in AXI Slave Write data parity generator is disabled. 0x1 (ENABLE): Insert Parity error in AXI Slave Write data parity generator is enabled.
11	0h RW	**Insert Parity error in Rx write-back Descriptor parity generator (IPERD):** When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Receive data path parity protection diagram) is flipped. 0x0 (DISABLE): Insert Parity error in Rx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Rx write-back Descriptor parity generator is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Insert Parity error in Tx write-back Descriptor parity generator (IPETD):** When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity error in Tx write-back Descriptor parity generator is disabled. 0x1 (ENABLE): Insert Parity error in Tx write-back Descriptor parity generator is enabled.
9	0h RW	**Insert Parity Error in DMA TSO parity generator (IPETSO):** When set to 1, parity bit of first valid data generated by the DMA TSO parity generator is (or at PG3 as shown in Transmit data path parity protection diagram) flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA TSO parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA TSO parity generator is enabled.
8	0h RW	**Insert Parity Error in DMA DTX Control word parity generator (IPEDDC):** When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in DMA DTX Control word parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in DMA DTX Control word parity generator is enabled.
7	0h RW	**Insert Parity Error in MTL Rx FIFO read control parity generator (IPEMRF):** When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Receive data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is enabled.
6	0h RW	**Insert Parity Error in MTL Tx Status parity generator (IPEMTS):** When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL Tx Status parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL Tx Status parity generator is enabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Insert Parity Error in MTL checksum parity generator (IPEMC):** When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in MTL checksum parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in MTL checksum parity generator is enabled.
4	0h RW	**Insert Parity Error in Interface Data parity generator (IPEID):** When set to 1, parity bit of first valid input data generated by the Interface data parity generator (or at PG1 as shown in Transmit data path parity protection diagram) is flipped. Following are the input data bus on which parity bits are generated based on configuration selected In AHB Config, hrdata_i In AXI config, rdata_m_i In DMA Config, mdc_rdata_i In MTL Config, ati_data_i Hardware clears this bit once the respective parity bit is flipped. 0x0 (DISABLE): Insert Parity Error in Interface Data parity generator is disabled. 0x1 (ENABLE): Insert Parity Error in Interface Data parity generator is enabled.
3:2	0h RO	**Reserved**

14.20.3.367MTL_TXQ0_OPERATION_MODE — Offset 50220D00h

The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	50220D00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Reserved - 2'b10: Enabled - 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

14.20.3.368MTL_TXQ0_UNDERFLOW — Offset 50220D04h

The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	50220D04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO	**Overflow Bit for Underflow Packet Counter (UFCNTOVF):** This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter. 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter.
10:0	000h RO	**Underflow Packet Counter (UFFRMCNT):** This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

14.20.3.369MTL_TXQ0_DEBUG — Offset 50220D08h

The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	50220D08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO	**Number of Status Words in Tx Status FIFO of Queue (STXSTSF):** This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO	**Number of Packets in the Transmit Queue (PTXQ):** This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	**Reserved**
5	0h RO	**MTL Tx Status FIFO Full Status (TXSTSFSTS):** When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected. 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected.
4	0h RO	**MTL Tx Queue Not Empty Status (TXQSTS):** When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected. 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected.
3	0h RO	**MTL Tx Queue Write Controller Status (TWCSTS):** When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected. 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected.
2:1	0h RO	**MTL Tx Queue Read Controller Status (TRCSTS):** This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state. 0x1 (READ): Read state (transferring data to the MAC transmitter). 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter. 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC.
0	0h RO	**Transmit Queue in Pause (TXQPAUSED):** When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled 0x0 (INACTIVE): Transmit Queue in Pause status is not detected. 0x1 (ACTIVE): Transmit Queue in Pause status is detected.

14.20.3.370MTL_TXQ0_ETS_STATUS — Offset 50220D14h

The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	50220D14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

14.20.3.371MTL_TXQ0_QUANTUM_WEIGHT — Offset 50220D18h

The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	50220D18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**Quantum or Weights (ISCQW):** When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.

14.20.3.372MTL_Q0_INTERRUPT_CONTROL_STATUS — Offset 50220D2Ch

This register contains the interrupt enable and status bits for the queue 0 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50220D2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Receive Queue Overflow Interrupt Enable (RXOIE):** When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled. 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled.
23:17	0h RO	**Reserved**
16	0h RW	**Receive Queue Overflow Interrupt Status (RXOVFIS):** This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected. 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected.
15:10	0h RO	**Reserved**
9	0h RW	**Average Bits Per Slot Interrupt Enable (ABPSIE):** When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event. 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled. 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled.
8	0h RW	**Transmit Queue Underflow Interrupt Enable (TXUIE):** When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled. 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled.

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved**
1	0h RW	**Average Bits Per Slot Interrupt Status (ABPSIS):** When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected. 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected.
0	0h RW	**Transmit Queue Underflow Interrupt Status (TXUNFIS):** This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected. 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected.

14.20.3.373MTL_RXQ0_OPERATION_MODE — Offset 50220D30h

The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	50220D30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:20	00h RW	**Receive Queue Size (RQS):** This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) (RFD):** These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1 KB, that is, FULL 1 KB - 1: Full minus 1.5 KB, that is, FULL 1.5 KB - 2: Full minus 2 KB, that is, FULL 2 KB - 3: Full minus 2.5 KB, that is, FULL 2.5 KB - ... - 62: Full minus 32 KB, that is, FULL 32 KB - 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**Threshold for Activating Flow Control (in half-duplex and full-duplex (RFA):** These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**Enable Hardware Flow Control (EHFC):** When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. 0x0 (DISABLE): Hardware Flow Control is disabled. 0x1 (ENABLE): Hardware Flow Control is enabled.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Disable Dropping of TCP/IP Checksum Error Packets (DIS_TCP_EF):** When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled. 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled.
5	0h RW	**Receive Queue Store and Forward (RSF):** When this bit is set, the GbE Controller reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0 (DISABLE): Receive Queue Store and Forward is disabled. 0x1 (ENABLE): Receive Queue Store and Forward is enabled.
4	0h RW	**Forward Error Packets (FEP):** When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0 (DISABLE): Forward Error Packets is disabled. 0x1 (ENABLE): Forward Error Packets is enabled.
3	0h RW	**Forward Undersized Good Packets (FUP):** When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0 (DISABLE): Forward Undersized Good Packets is disabled. 0x1 (ENABLE): Forward Undersized Good Packets is enabled.
2	0h RO	**Reserved**
1:0	0h RW	**Receive Queue Threshold Control (RTC):** These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64. 0x1 (M_32BYTE): 32. 0x2 (M_96BYTE): 96. 0x3 (M_128BYTE): 128.

14.20.3.374MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT — Offset 50220D34h

The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	50220D34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO	**Missed Packet Counter Overflow Bit (MISCNTOVF):** When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Missed Packet Counter overflow not detected. 0x1 (ACTIVE): Missed Packet Counter overflow detected.
26:16	000h RO	**Missed Packet Counter (MISPKTCNT):** This field indicates the number of packets missed by the GbE Controller because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO	**Overflow Counter Overflow Bit (OVFCNTOVF):** When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Overflow Counter overflow not detected. 0x1 (ACTIVE): Overflow Counter overflow detected.
10:0	000h RO	**Overflow Packet Counter (OVFPKTCNT):** This field indicates the number of packets discarded by the GbE Controller because of Receive queue overflow. This counter is incremented each time the GbE Controller discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

14.20.3.375MTL_RXQ0_DEBUG — Offset 50220D38h

The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	50220D38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Number of Packets in Receive Queue (PRXQ):** This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/ Min_Packet_Size.
15:6	0h RO	**Reserved**
5:4	0h RO	**MTL Rx Queue Fill-Level Status (RXQSTS):** This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty. 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold. 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold. 0x3 (FULL): Rx Queue full.
3	0h RO	**Reserved**
2:1	0h RO	**MTL Rx Queue Read Controller State (RRCSTS):** This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state. 0x1 (READ_DATA): Reading packet data. 0x2 (READ_STS): Reading packet status (or timestamp). 0x3 (FLUSH): Flushing the packet data and status.
0	0h RO	**MTL Rx Queue Write Controller Active Status (RWCSTS):** When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected. 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected.

14.20.3.376MTL_RXQ0_CONTROL — Offset 50220D3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	50220D3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**Receive Queue Packet Arbitration (RXQ_FRM_ARBIT):** When this bit is set, the GbE Controller drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the GbE Controller drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the GbE Controller drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled. 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled.
2:0	0h RW	**Receive Queue Weight (RXQ_WEGT):** This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register.

14.20.3.377MTL_TXQ1_OPERATION_MODE — Offset 50220D40h

The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	50220D40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW	**Transmit Queue Size (TQS):** This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Transmit Queue Enable (TXQEN):** This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0x0 (DISABLE): Not enabled. 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV). 0x2 (ENABLE): Enabled. 0x3 (RSVD2): Reserved.
1	0h RW	**Transmit Store and Forward (TSF):** When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0 (DISABLE): Transmit Store and Forward is disabled. 0x1 (ENABLE): Transmit Store and Forward is enabled. Note: This bit should always be set as we do not support cut through mode.
0	0h RW	**Flush Transmit Queue (FTQ):** When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Flush Transmit Queue is disabled. 0x1 (ENABLE): Flush Transmit Queue is enabled.

14.20.3.378MTL_TXQ1_UNDERFLOW — Offset 50220D44h

The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.379MTL_TXQ1_DEBUG — Offset 50220D48h

The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.380MTL_TXQ1_ETS_CONTROL — Offset 50220D50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	50220D50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**Slot Count (SLC):** If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows: 0x0 (M_1_SLOT): 1 slot. 0x1 (M_2_SLOT): 2 slots. 0x2 (M_4_SLOT): 4 slots. 0x3 (M_8_SLOT): 8 slots. 0x4 (M_16_SLOT): 16 slots. 0x5 (RSVD): Reserved.
3	0h RW	**Credit Control (CC):** When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated. 0x0 (DISABLE): Credit Control is disabled. 0x1 (ENABLE): Credit Control is enabled.
2	0h RW	**AV Algorithm (AVALG):** When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected. 0x0 (DISABLE): CBS Algorithm is disabled. 0x1 (ENABLE): CBS Algorithm is enabled.
1:0	0h RO	**Reserved**

14.20.3.381MTL_TXQ1_ETS_STATUS — Offset 50220D54h

The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	50220D54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO	**Average Bits per Slot (ABS):** This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

14.20.3.382MTL_TXQ1_QUANTUM_WEIGHT — Offset 50220D58h

The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	50220D58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW:** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

14.20.3.383MTL_TXQ1_SENDSLOPECREDIT — Offset 50220D5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	50220D5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**sendSlopeCredit Value (SSC):** When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

14.20.3.384MTL_TXQ1_HICREDIT — Offset 50220D60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	50220D60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**hiCredit Value (HC):** When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

14.20.3.385MTL_TXQ1_LOCREDIT — Offset 50220D64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	50220D64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**loCredit Value (LC):** When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

14.20.3.386MTL_Q1_INTERRUPT_CONTROL_STATUS — Offset 50220D6Ch

This register contains the interrupt enable and status bits for the queue 1 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.387MTL_RXQ1_OPERATION_MODE — Offset 50220D70h

The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.388MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT — Offset 50220D74h

The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.389MTL_RXQ1_DEBUG — Offset 50220D78h

The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.390MTL_RXQ1_CONTROL — Offset 50220D7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.391MTL_TXQ2_OPERATION_MODE — Offset 50220D80h

The Queue 2 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50220D40h.

14.20.3.392MTL_TXQ2_UNDERFLOW — Offset 50220D84h

The Queue 2 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.393MTL_TXQ2_DEBUG — Offset 50220D88h

The Queue 2 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.394MTL_TXQ2_ETS_CONTROL — Offset 50220D90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50220D50h.

14.20.3.395MTL_TXQ2_ETS_STATUS — Offset 50220D94h

The Queue 2 ETS Status register provides the average traffic transmitted in Queue 2.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50220D54h.

14.20.3.396MTL_TXQ2_QUANTUM_WEIGHT — Offset 50220D98h

The Queue 2 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 2.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50220D58h.

14.20.3.397MTL_TXQ2_SENDSLOPECREDIT — Offset 50220D9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50220D5Ch.

14.20.3.398MTL_TXQ2_HICREDIT — Offset 50220DA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50220D60h.

14.20.3.399MTL_TXQ2_LOCREDIT — Offset 50220DA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50220D64h.

14.20.3.400MTL_Q2_INTERRUPT_CONTROL_STATUS — Offset 50220DACh

This register contains the interrupt enable and status bits for the queue 2 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.401MTL_RXQ2_OPERATION_MODE — Offset 50220DB0h

The Queue 2 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.402MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT — Offset 50220DB4h

The Queue 2 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.403MTL_RXQ2_DEBUG — Offset 50220DB8h

The Queue 2 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.404MTL_RXQ2_CONTROL — Offset 50220DBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.405MTL_TXQ3_OPERATION_MODE — Offset 50220DC0h

The Queue 3 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50220D40h.

14.20.3.406MTL_TXQ3_UNDERFLOW — Offset 50220DC4h

The Queue 3 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.407MTL_TXQ3_DEBUG — Offset 50220DC8h

The Queue 3 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.408MTL_TXQ3_ETS_CONTROL — Offset 50220DD0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50220D50h.

14.20.3.409MTL_TXQ3_ETS_STATUS — Offset 50220DD4h

The Queue 3 ETS Status register provides the average traffic transmitted in Queue 3.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50220D54h.

14.20.3.410MTL_TXQ3_QUANTUM_WEIGHT — Offset 50220DD8h

The Queue 3 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 3.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50220D58h.

14.20.3.411MTL_TXQ3_SENDSLOPECREDIT — Offset 50220DDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50220D5Ch.

14.20.3.412MTL_TXQ3_HICREDIT — Offset 50220DE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50220D60h.

14.20.3.413MTL_TXQ3_LOCREDIT — Offset 50220DE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50220D64h.

14.20.3.414MTL_Q3_INTERRUPT_CONTROL_STATUS — Offset 50220DECh

This register contains the interrupt enable and status bits for the queue 3 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.415MTL_RXQ3_OPERATION_MODE — Offset 50220DF0h

The Queue 3 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.416MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT — Offset 50220DF4h

The Queue 3 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.417MTL_RXQ3_DEBUG — Offset 50220DF8h

The Queue 3 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.418MTL_RXQ3_CONTROL — Offset 50220DFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.419MTL_TXQ4_OPERATION_MODE — Offset 50220E00h

The Queue 4 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50220D40h.

14.20.3.420MTL_TXQ4_UNDERFLOW — Offset 50220E04h

The Queue 4 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.421MTL_TXQ4_DEBUG — Offset 50220E08h

The Queue 4 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.422MTL_TXQ4_ETS_CONTROL — Offset 50220E10h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50220D50h.

14.20.3.423MTL_TXQ4_ETS_STATUS — Offset 50220E14h

The Queue 4 ETS Status register provides the average traffic transmitted in Queue 4.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50220D54h.

14.20.3.424MTL_TXQ4_QUANTUM_WEIGHT — Offset 50220E18h

The Queue 4 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 4.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50220D58h.

14.20.3.425MTL_TXQ4_SENDSLOPECREDIT — Offset 50220E1Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50220D5Ch.

14.20.3.426MTL_TXQ4_HICREDIT — Offset 50220E20h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50220D60h.

14.20.3.427MTL_TXQ4_LOCREDIT — Offset 50220E24h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50220D64h.

14.20.3.428MTL_Q4_INTERRUPT_CONTROL_STATUS — Offset 50220E2Ch

This register contains the interrupt enable and status bits for the queue 4 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.429MTL_RXQ4_OPERATION_MODE — Offset 50220E30h

The Queue 4 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.430MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT — Offset 50220E34h

The Queue 4 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.431MTL_RXQ4_DEBUG — Offset 50220E38h

The Queue 4 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.432MTL_RXQ4_CONTROL — Offset 50220E3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.433MTL_TXQ5_OPERATION_MODE — Offset 50220E40h

The Queue 5 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50220D40h.

14.20.3.434MTL_TXQ5_UNDERFLOW — Offset 50220E44h

The Queue 5 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.435MTL_TXQ5_DEBUG — Offset 50220E48h

The Queue 5 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.436MTL_TXQ5_ETS_CONTROL — Offset 50220E50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50220D50h.

14.20.3.437MTL_TXQ5_ETS_STATUS — Offset 50220E54h

The Queue 5 ETS Status register provides the average traffic transmitted in Queue 5.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50220D54h.

14.20.3.438MTL_TXQ5_QUANTUM_WEIGHT — Offset 50220E58h

The Queue 5 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 5.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50220D58h.

14.20.3.439MTL_TXQ5_SENDSLOPECREDIT — Offset 50220E5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50220D5Ch.

14.20.3.440MTL_TXQ5_HICREDIT — Offset 50220E60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50220D60h.

14.20.3.441MTL_TXQ5_LOCREDIT — Offset 50220E64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50220D64h.

14.20.3.442MTL_Q5_INTERRUPT_CONTROL_STATUS — Offset 50220E6Ch

This register contains the interrupt enable and status bits for the queue 5 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.443MTL_RXQ5_OPERATION_MODE — Offset 50220E70h

The Queue 5 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.444MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT — Offset 50220E74h

The Queue 5 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.445MTL_RXQ5_DEBUG — Offset 50220E78h

The Queue 5 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.446MTL_RXQ5_CONTROL — Offset 50220E7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.447MTL_TXQ6_OPERATION_MODE — Offset 50220E80h

The Queue 6 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50220D40h.

14.20.3.448MTL_TXQ6_UNDERFLOW — Offset 50220E84h

The Queue 6 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.449MTL_TXQ6_DEBUG — Offset 50220E88h

The Queue 6 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.450MTL_TXQ6_ETS_CONTROL — Offset 50220E90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50220D50h.

14.20.3.451MTL_TXQ6_ETS_STATUS — Offset 50220E94h

The Queue 6 ETS Status register provides the average traffic transmitted in Queue 6.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50220D54h.

14.20.3.452MTL_TXQ6_QUANTUM_WEIGHT — Offset 50220E98h

The Queue 6 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 6.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50220D58h.

14.20.3.453MTL_TXQ6_SENDSLOPECREDIT — Offset 50220E9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50220D5Ch.

14.20.3.454MTL_TXQ6_HICREDIT — Offset 50220EA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50220D60h.

14.20.3.455MTL_TXQ6_LOCREDIT — Offset 50220EA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50220D64h.

14.20.3.456MTL_Q6_INTERRUPT_CONTROL_STATUS — Offset 50220EACh

This register contains the interrupt enable and status bits for the queue 6 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.457MTL_RXQ6_OPERATION_MODE — Offset 50220EB0h

The Queue 6 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.458MTL_RXQ6_MISSED_PACKET_OVERFLOW_CNT — Offset 50220EB4h

The Queue 6 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.459MTL_RXQ6_DEBUG — Offset 50220EB8h

The Queue 6 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.460MTL_RXQ6_CONTROL — Offset 50220EBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.461MTL_TXQ7_OPERATION_MODE — Offset 50220EC0h

The Queue 7 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset 50220D40h.

14.20.3.462MTL_TXQ7_UNDERFLOW — Offset 50220EC4h

The Queue 7 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset 50220D04h.

14.20.3.463MTL_TXQ7_DEBUG — Offset 50220EC8h

The Queue 7 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset 50220D08h.

14.20.3.464MTL_TXQ7_ETS_CONTROL — Offset 50220ED0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset 50220D50h.

14.20.3.465MTL_TXQ7_ETS_STATUS — Offset 50220ED4h

The Queue 7 ETS Status register provides the average traffic transmitted in Queue 7.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset 50220D54h.

14.20.3.466MTL_TXQ7_QUANTUM_WEIGHT — Offset 50220ED8h

The Queue 7 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 7.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset 50220D58h.

14.20.3.467MTL_TXQ7_SENDSLOPECREDIT — Offset 50220EDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset 50220D5Ch.

14.20.3.468MTL_TXQ7_HICREDIT — Offset 50220EE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset 50220D60h.

14.20.3.469MTL_TXQ7_LOCREDIT — Offset 50220EE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset 50220D64h.

14.20.3.470MTL_Q7_INTERRUPT_CONTROL_STATUS — Offset 50220EECh

This register contains the interrupt enable and status bits for the queue 7 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset 50220D2Ch.

14.20.3.471MTL_RXQ7_OPERATION_MODE — Offset 50220EF0h

The Queue 7 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset 50220D30h.

14.20.3.472MTL_RXQ7_MISSED_PACKET_OVERFLOW_CNT — Offset 50220EF4h

The Queue 7 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset 50220D34h.

14.20.3.473MTL_RXQ7_DEBUG — Offset 50220EF8h

The Queue 7 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset 50220D38h.

14.20.3.474MTL_RXQ7_CONTROL — Offset 50220EFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset 50220D3Ch.

14.20.3.475DMA_MODE — Offset 50221000h

The Bus Mode register establishes the bus operating modes for the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50221000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**Rx DMA's Maximum Number of Descriptors to be fetched in a burst (RNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2
21:20	0h RW	**Tx DMA's Maximum Number of Descriptors to be fetched in a burst (TNDF):** 0x0 (MODE0): 16 0x1 (MODE1): 8 0x2 (MODE2): 4 0x3 (MODE3): 2
19	0h RW	**Descriptor Cache Enable (DCHE):** When set enables prefetching of descriptors to the Descriptor Cache. When reset descriptor cache feature is disabled. 0x0 (DISABLE): Descriptor Cache Support is disabled. 0x1 (ENABLE): Descriptor Cache Support is enabled.
18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Interrupt Mode (INTM):** This field defines the interrupt mode of GbE Controller. The behavior of the following outputs changes depending on the following settings: - sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) - sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) - sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. - 00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. - 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 11: Reserved 0x0 (MODE0): See above description. 0x1 (MODE1): See above description. 0x2 (MODE2): See above description. 0x3 (RSVD): Reserved.
15:11	0h RO	**Reserved**
10	0h RW	**Reserved**
9	0h RO	**Reserved**
8	0h RW	**Descriptor Posted Write (DSPW):** When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. 0x0 (DISABLE): Descriptor Posted Write is disabled. 0x1 (ENABLE): Descriptor Posted Write is enabled.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4:2	0h RW	**Transmit Arbitration Algorithm (TAA):** This field is used to select the arbitration algorithm for the Transmit side when multiple Tx DMAs are selected. 0x0 (FP): Fixed priority (Channel 0 has the lowest priority and the last channel has the highest priority). 0x1 (WSP): Weighted Strict Priority (WSP). 0x2 (WRR): Weighted Round-Robin (WRR). 0x3 (RSVD): Reserved (for 3'b011 to 3'b111).
1	0h RO	**Reserved**
0	0h RW	**Software Reset (SWR):** When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all GbE Controller clock domains. Before reprogramming any GbE Controller register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0 (DISABLE): Software Reset is disabled. 0x1 (ENABLE): Software Reset is enabled.

14.20.3.476DMA_SYSBUS_MODE — Offset 50221004h

The System Bus mode register controls the behavior of the AHB or AXI master. It mainly controls burst splitting and number of outstanding requests.

Type	Size	Offset	Default
MMIO	32 bit	50221004h	01010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Low Power Interface (LPI) (EN_LPI):** When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. 0x0 (DISABLE): Low Power Interface (LPI) is disabled. 0x1 (ENABLE): Low Power Interface (LPI) is enabled.
30	0h RW	**Unlock on Magic Packet or Remote Wake-Up Packet (LPI_XIT_PKT):** When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. 0x0 (DISABLE): Unlock on Magic Packet or Remote Wake-Up Packet is disabled. 0x1 (ENABLE): Unlock on Magic Packet or Remote Wake-Up Packet is enabled.
29:28	0h RO	**Reserved**
27:24	1h RW	**AXI Maximum Write Outstanding Request Limit (WR_OSR_LMT):** This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1
23:20	0h RO	**Reserved**
19:16	1h RW	**AXI Maximum Read Outstanding Request Limit (RD_OSR_LMT):** This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1
15:14	0h RO	**Reserved**
13	0h RW	**1 KB Boundary Crossing Enable for the EQOS-AXI Master (ONEKBBE):** When set, the burst transfers performed by the EQOS-AXI master do not cross 1 KB boundary. When reset, the burst transfers performed by the EQOS-AXI master do not cross 4 KB boundary. 0x0 (DISABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is disabled. 0x1 (ENABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is enabled.
12	0h RW	**Address-Aligned Beats (AAL):** When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. 0x0 (DISABLE): Address-Aligned Beats is disabled. 0x1 (ENABLE): Address-Aligned Beats is enabled.
11	0h RW	**Enhanced Address Mode Enable. (EAME):** When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. 0x0 (DISABLE): Enhanced Address Mode is disabled. 0x1 (ENABLE): Enhanced Address Mode is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Automatic AXI LPI enable (AALE):** When set to 1, enables the AXI master to enter into LPI state when there is no activity in the GbE Controller for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. 0x0 (DISABLE): Automatic AXI LPI is disabled. 0x1 (ENABLE): Automatic AXI LPI is enabled.
9:8	0h RO	**Reserved**
7	0h RW	**AXI Burst Length 256 (BLEN256):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 256 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 256.
6	0h RW	**AXI Burst Length 128 (BLEN128):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 128 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 128.
5	0h RW	**AXI Burst Length 64 (BLEN64):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 64 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 64.
4	0h RW	**AXI Burst Length 32 (BLEN32):** When this bit is set to 1, the EQOS-AXI master can select a burst length of 32 on the AXI interface. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 32.
3	0h RW	**AXI Burst Length 16 (BLEN16):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 16.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**AXI Burst Length 8 (BLEN8):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 8.
1	0h RW	**AXI Burst Length 4 (BLEN4):** When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. 0x0 (DISABLE): No effect. 0x1 (ENABLE): AXI Burst Length 4.
0	0h RW	**FB:** Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. - Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field - Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. 0x0 (DISABLE): Fixed Burst Length is disabled. 0x1 (ENABLE): Fixed Burst Length is enabled.

14.20.3.477DMA_INTERRUPT_STATUS — Offset 50221008h

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	50221008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO	**MAC Interrupt Status (MACIS):** This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MAC Interrupt Status not detected. 0x1 (ACTIVE): MAC Interrupt Status detected.
16	0h RO	**MTL Interrupt Status (MTLIS):** This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): MTL Interrupt Status not detected. 0x1 (ACTIVE): MTL Interrupt Status detected.
15:8	0h RO	**Reserved**
7	0h RO	**DMA Channel 7 Interrupt Status (DC7IS):** This bit indicates an interrupt event in DMA Channel 7. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 7 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 7 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 7 Interrupt Status detected.
6	0h RO	**DMA Channel 6 Interrupt Status (DC6IS):** This bit indicates an interrupt event in DMA Channel 6. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 6 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 6 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 6 Interrupt Status detected.
5	0h RO	**DMA Channel 5 Interrupt Status (DC5IS):** This bit indicates an interrupt event in DMA Channel 5. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 5 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 5 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 5 Interrupt Status detected.
4	0h RO	**DMA Channel 4 Interrupt Status (DC4IS):** This bit indicates an interrupt event in DMA Channel 4. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 4 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 4 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 4 Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**DMA Channel 3 Interrupt Status (DC3IS):** This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 3 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 3 Interrupt Status detected.
2	0h RO	**DMA Channel 2 Interrupt Status (DC2IS):** This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 2 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 2 Interrupt Status detected.
1	0h RO	**DMA Channel 1 Interrupt Status (DC1IS):** This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 1 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 1 Interrupt Status detected.
0	0h RO	**DMA Channel 0 Interrupt Status (DC0IS):** This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. 0x0 (INACTIVE): DMA Channel 0 Interrupt Status not detected. 0x1 (ACTIVE): DMA Channel 0 Interrupt Status detected.

14.20.3.478DMA_DEBUG_STATUS0 — Offset 5022100Ch

The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose.

Type	Size	Offset	Default
MMIO	32 bit	5022100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 2 Transmit Process State (TPS2):** This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 2 Receive Process State (RPS2):** This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 1 Transmit Process State (TPS1):** This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO	**DMA Channel 1 Receive Process State (RPS1):** This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
15:12	0h RO	**DMA Channel 0 Transmit Process State (TPS0):** This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
11:8	0h RO	**DMA Channel 0 Receive Process State (RPS0):** This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:2	0h RO	**Reserved**
1	0h RO	**AXI Master Read Channel Status (AXRHSTS):** When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. 0x0 (INACTIVE): AXI Master Read Channel Status not detected. 0x1 (ACTIVE): AXI Master Read Channel Status detected.
0	0h RO	**AXI Master Write Channel (AXWHSTS):** When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. 0x0 (INACTIVE): AXI Master Write Channel or AHB Master Status not detected. 0x1 (ACTIVE): AXI Master Write Channel or AHB Master Status detected.

14.20.3.479DMA_DEBUG_STATUS1 — Offset 50221010h

The Debug Status1 register gives the Receive and Transmit process status for DMA Channel 3-Channel 6.

Type	Size	Offset	Default
MMIO	32 bit	50221010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**DMA Channel 6 Transmit Process State (TPS6):** This field indicates the Tx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
27:24	0h RO	**DMA Channel 6 Receive Process State (RPS6):** This field indicates the Rx DMA FSM state for Channel 6. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
23:20	0h RO	**DMA Channel 5 Transmit Process State (TPS5):** This field indicates the Tx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO	**DMA Channel 5 Receive Process State (RPS5):** This field indicates the Rx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
15:12	0h RO	**DMA Channel 4 Transmit Process State (TPS4):** This field indicates the Tx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO	**DMA Channel 4 Receive Process State (RPS4):** This field indicates the Rx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).
7:4	0h RO	**DMA Channel 3 Transmit Process State (TPS3):** This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 3 Receive Process State (RPS3):** This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

14.20.3.480DMA_DEBUG_STATUS2 — Offset 50221014h

The Debug Status Register 2 gives the Receive and Transmit process status for DMA Channel 7.

Type	Size	Offset	Default
MMIO	32 bit	50221014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	0h RO	**DMA Channel 7 Transmit Process State (TPS7):** This field indicates the Tx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued). 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor). 0x2 (RUN_WS): Running (Waiting for status). 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)). 0x4 (TSTMP_WS): Timestamp write state. 0x5 (RSVD): Reserved for future use. 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow). 0x7 (RUN_CTD): Running (Closing Tx Descriptor).
3:0	0h RO	**DMA Channel 7 Receive Process State (RPS7):** This field indicates the Rx DMA FSM state for Channel 7. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued). 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor). 0x2 (RSVD): Reserved for future use. 0x3 (RUN_WRP): Running (Waiting for Rx packet). 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable). 0x5 (RUN_CRD): Running (Closing the Rx Descriptor). 0x6 (TSTMP): Timestamp write state. 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory).

14.20.3.481AXI4_TX_AR_ACE_CONTROL — Offset 50221020h

This register is used to control the AXI4 Cache Coherency Signals for read transactions by all the Transmit DMA channels. The following signals of the AXI4 interface are driven with different values as programmed for corresponding type (descriptor, buffer1, buffer2) of access. - arcache_m_o[3:0] - ardomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	50221020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:20	0h RW	**Transmit DMA First Packet Buffer or TSO Header Domain Control (THD):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO Header data.
19:16	0h RW	**Transmit DMA First Packet Buffer or TSO Header Cache Control (THC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO Header data.
15:14	0h RO	**Reserved**
13:12	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Domain Control (TED):** When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO payload data.
11:8	0h RW	**Transmit DMA Extended Packet Buffer or TSO Payload Cache Control (TEC):** When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO payload data.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Read Descriptor Domain Control (TDRD):** This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the Descriptor.
3:0	0h RW	**Transmit DMA Read Descriptor Cache Control (TDRC):** This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor.

14.20.3.482AXI4_RX_AW_ACE_CONTROL — Offset 50221024h

This register is used to control the AXI4 Cache Coherency Signals for write transactions by all the Receive DMA channels. The following signals of the AXI4 interface are driven with different values as programmed for corresponding type (descriptor, buffer1, buffer2) of access. - awcache_m_o[3:0] - awdomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	50221024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Receive DMA Buffer Domain Control (RDD):** This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
27:24	0h RW	**Receive DMA Buffer Cache Control (RDC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
23:22	0h RO	**Reserved**
21:20	0h RW	**Receive DMA Header Domain Control (RHD):** This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
19:16	0h RW	**Receive DMA Header Cache Control (RHC):** This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Payload Domain Control (RPD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
11:8	0h RW	**Receive DMA Payload Cache Control (RPC):** This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
7:6	0h RO	**Reserved**
5:4	0h RW	**Receive DMA Write Descriptor Domain Control (RDWD):** This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor.
3:0	0h RW	**Receive DMA Write Descriptor Cache Control (RDWC):** This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor.

14.20.3.483AXI4_TXRX_AWAR_ACE_CONTROL — Offset 50221028h

This register is used to control the AXI4 Cache Coherency Signals for Descriptor write transactions by all the TxDMA channels and Descriptor read transactions by all the RxDMA channels. It also controls the values to be driven on awprot_m_o and arprot_m_o.

Type	Size	Offset	Default
MMIO	32 bit	50221028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RW	**DMA Write Protection control (WRP):** This field is used to drive awprot_m_o[2:0] signal on the AXI Write Channel.
19	0h RO	**Reserved**
18:16	0h RW	**DMA Read Protection control (RDP):** This field is used to drive arprot_m_o[2:0] signal during all read requests.
15:14	0h RO	**Reserved**
13:12	0h RW	**Receive DMA Read Descriptor Domain control (RDRD):** This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor.
11:8	0h RW	**Receive DMA Read Descriptor Cache control (RDRC):** This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor.
7:6	0h RO	**Reserved**
5:4	0h RW	**Transmit DMA Write Descriptor Domain control (TDWD):** This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor.
3:0	0h RW	**Transmit DMA Write Descriptor Cache control (TDWC):** This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor.

14.20.3.484AXI_LPI_ENTRY_INTERVAL — Offset 50221040h

This register is used to control the AXI LPI entry interval.

Type	Size	Offset	Default
MMIO	32 bit	50221040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**LPI Entry Interval (LPIEI):** Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the GbE Controller to enter into the AXI low power state 0 indicates 64 clock cycles

14.20.3.485DMA_TBS_CTRL0 — Offset 50221050h

Type	Size	Offset	Default
MMIO	32 bit	50221050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Fetch Time Offset (FTOS):** The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**Fetch GSN Offset (FGOS):** The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**Fetch Time Offset Valid (FTOV):** Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions. 0x0 (INVALID): Fetch Time Offset is invalid. 0x1 (VALID): Fetch Time Offset is valid.

14.20.3.486DMA_TBS_CTRL1 — Offset 50221054h

Note: Bit definitions are the same as DMA_TBS_CTRL0, offset 50221050h.

14.20.3.487DMA_TBS_CTRL2 — Offset 50221058h

Note: Bit definitions are the same as DMA_TBS_CTRL0, offset 50221050h.

14.20.3.488DMA_TBS_CTRL3 — Offset 5022105Ch

Note: Bit definitions are the same as DMA_TBS_CTRL0, offset 50221050h.

14.20.3.489DMA_SAFETY_INTERRUPT_STATUS — Offset 50221080h

This register indicates summary (whether error occured in DMA/MTL/MAC and correctable/uncorrectable) of the Automotive Safety related error interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50221080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**MAC Safety Uncorrectable Interrupt Status (MCSIS):** Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC. 0x0 (INACTIVE): MAC Safety Uncorrectable Interrupt Status not detected. 0x1 (ACTIVE): MAC Safety Uncorrectable Interrupt Status detected.
30	0h RO	**Reserved**
29	0h RO	**MTL Safety Uncorrectable error Interrupt Status (MSUIS):** This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Uncorrectable error Interrupt Status detected.
28	0h RO	**MTL Safety Correctable error Interrupt Status (MSCIS):** This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register. 0x0 (INACTIVE): MTL Safety Correctable error Interrupt Status not detected. 0x1 (ACTIVE): MTL Safety Correctable error Interrupt Status detected.

Bit Range	Default & Access	Field Name (ID): Description
27:2	0h RO	**Reserved**
1	0h RO	**DMA ECC Uncorrectable error Interrupt Status (DEUIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Uncorrectable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Uncorrectable error Interrupt Status detected.
0	0h RO	**DMA ECC Correctable error Interrupt Status (DECIS):** This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register. 0x0 (INACTIVE): DMA ECC Correctable error Interrupt Status not detected. 0x1 (ACTIVE): DMA ECC Correctable error Interrupt Status detected.

14.20.3.490DMA_ECC_INTERRUPT_ENABLE — Offset 50221084h

This register is used to enable the Automotive Safety related TSO memory ECC error interrupt.

Type	Size	Offset	Default
MMIO	32 bit	50221084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TSO memory Correctable Error Interrupt Enable (TCEIE):** When set, generates an interrupt when a correctable error is detected at the DMA TSO memory interface. It is indicated in the TCES bit of DMA_ECC_Interrupt_Status register. When reset this event does not generates an interrupt. 0x0 (DISABLE): TSO memory Correctable Error Interrupt is disabled. 0x1 (ENABLE): TSO memory Correctable Error Interrupt is enabled.

14.20.3.491DMA_ECC_INTERRUPT_STATUS — Offset 50221088h

This register indicates the Automotive Safety related TSO memory ECC error interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	50221088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**DMA TSO memory Uncorrectable Error status (TUES):** When set, indicates that an uncorrectable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Uncorrectable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Uncorrectable Error status detected.
1	0h RW	**DMA TSO memory Address Mismatch status (TAMS):** This bit when set indicates that address mismatch is found for address bus of DMA TSO memory. 0x0 (INACTIVE): DMA TSO memory Address Mismatch status not detected. 0x1 (ACTIVE): DMA TSO memory Address Mismatch status detected.
0	0h RW	**DMA TSO memory Correctable Error status (TCES):** This bit when set indicates that correctable error is detected at DMA TSO memory interface. 0x0 (INACTIVE): DMA TSO memory Correctable Error status not detected. 0x1 (ACTIVE): DMA TSO memory Correctable Error status detected.

14.20.3.492DMA_CH0_CONTROL — Offset 50221100h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	50221100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:14	0h RO	**Reserved**
13:0	0000h RW	**Maximum Segment Size (MSS):** This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

14.20.3.493DMA_CH0_TX_CONTROL — Offset 50221104h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	50221104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:29	0h RW	**Time Select (TFSEL):** Select bits for one of the four DMA_TBS_CTRL register fields (FTOS, FGSN, FTOV) for the channel. 0x0: DMA_TBS_CTRL0 selected. 0x1: DMA_TBS_CTRL1 selected. 0x2: DMA_TBS_CTRL2 selected. 0x3: DMA_TBS_CTRL3 selected.
28	0h RW	**Enhanced Descriptor Enable (EDSE):** When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0x0 (DISABLE): Enhanced Descriptor is disabled. 0x1 (ENABLE): Enhanced Descriptor is enabled.
27:24	0h RW	**Transmit QOS. (TQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Transmit Programmable Burst Length (TXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**Ignore PBL Requirement (IPBL):** When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled. 0x1 (ENABLE): Ignore PBL Requirement is enabled.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**TSE_MODE:** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved 0x0 (TSO_USO): TSO/USO. 0x1 (UFOWC): UFO with Checksum. 0x2 (UFOWOC): UFO without Checksum. 0x3 (RSVD): Reserved.
12	0h RW	**TCP Segmentation Enabled (TSE):** When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/ Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled. 0x1 (ENABLE): TCP Segmentation is enabled.
11:5	0h RO	**Reserved**
4	0h RW	**Operate on Second Packet (OSF):** When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled. 0x1 (ENABLE): Operate on Second Packet enabled.
3:1	0h RW	**Transmit Channel Weight (TCW):** This field indicates the weight assigned to the corresponding Transmit channel. When reset is complete, this field is set to 0 for all channels by default, resulting in equal weights to all channels.
0	0h RW	**Start or Stop Transmission Command (ST):** When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command. 0x1 (START): Start Transmission Command.

14.20.3.494DMA_CH0_RX_CONTROL — Offset 50221108h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	50221108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Rx Packet Flush. (RPF):** When this bit is set to 1, then GbE Controller automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the GbE Controller not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA Channel. 0x0 (DISABLE): Rx Packet Flush is disabled. 0x1 (ENABLE): Rx Packet Flush is enabled.
30:28	0h RO	**Reserved**
27:24	0h RW	**Rx AXI4 QOS. (RQOS):** This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**Receive Programmable Burst Length (RXPBL):** These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:4	000h RW	**Receive Buffer size High (RBSZ_13_Y):** RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO	**Receive Buffer size Low (RBSZ_X_0):** RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**Start or Stop Receive (SR):** When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive. 0x1 (START): Start Receive.

14.20.3.495DMA_CH0_TXDESC_LIST_HADDRESS — Offset 50221110h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	50221110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Transmit List (TDESHA):** This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

14.20.3.496DMA_CH0_TXDESC_LIST_ADDRESS — Offset 50221114h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	50221114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Transmit List (TDESLA):** This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.3.497DMA_CH0_RXDESC_LIST_HADDRESS — Offset 50221118h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	50221118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**Start of Receive List (RDESHA):** This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

14.20.3.498DMA_CH0_RXDESC_LIST_ADDRESS — Offset 5022111Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	5022111Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Start of Receive List (RDESLA):** This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.3.499DMA_CH0_TXDESC_TAIL_POINTER — Offset 50221120h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	50221120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Transmit Descriptor Tail Pointer (TDTP):** This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.3.500DMA_CH0_RXDESC_TAIL_POINTER — Offset 50221128h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	50221128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**Receive Descriptor Tail Pointer (RDTP):** This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

14.20.3.501DMA_CH0_TXDESC_RING_LENGTH — Offset 5022112Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	5022112Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Transmit Descriptor Ring Length (TDRL):** This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

14.20.3.502DMA_CH0_RXDESC_RING_LENGTH — Offset 50221130h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	50221130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**Receive Descriptor Ring Length (RDRL):** This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

14.20.3.503DMA_CH0_INTERRUPT_ENABLE — Offset 50221134h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	50221134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**Normal Interrupt Summary Enable (NIE):** When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled. 0x1 (ENABLE): Normal Interrupt Summary is enabled.
14	0h RW	**Abnormal Interrupt Summary Enable (AIE):** When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled. 0x1 (ENABLE): Abnormal Interrupt Summary is enabled.
13	0h RW	**Context Descriptor Error Enable (CDEE):** When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled. 0x1 (ENABLE): Context Descriptor Error is enabled.
12	0h RW	**Fatal Bus Error Enable (FBEE):** When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled. 0x1 (ENABLE): Fatal Bus Error is enabled.
11	0h RW	**Early Receive Interrupt Enable (ERIE):** When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled. 0x1 (ENABLE): Early Receive Interrupt is enabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Early Transmit Interrupt Enable (ETIE):** When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled. 0x1 (ENABLE): Early Transmit Interrupt is enabled.
9	0h RW	**Receive Watchdog Timeout Enable (RWTE):** When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled. 0x1 (ENABLE): Receive Watchdog Timeout is enabled.
8	0h RW	**Receive Stopped Enable (RSE):** When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0 (DISABLE): Receive Stopped is disabled. 0x1 (ENABLE): Receive Stopped is enabled.
7	0h RW	**Receive Buffer Unavailable Enable (RBUE):** When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled. 0x1 (ENABLE): Receive Buffer Unavailable is enabled.
6	0h RW	**Receive Interrupt Enable (RIE):** When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled. 0x1 (ENABLE): Receive Interrupt is enabled.
5:3	0h RO	**Reserved**
2	0h RW	**Transmit Buffer Unavailable Enable (TBUE):** When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled. 0x1 (ENABLE): Transmit Buffer Unavailable is enabled.
1	0h RW	**Transmit Stopped Enable (TXSE):** When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled. 0x1 (ENABLE): Transmit Stopped is enabled.
0	0h RW	**Transmit Interrupt Enable (TIE):** When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled. 0x1 (ENABLE): Transmit Interrupt is enabled.

14.20.3.504DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50221138h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	50221138h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Receive Interrupt Watchdog Timer Count Units (RWTU):** This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**Receive Interrupt Watchdog Timer Count (RWT):** This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

14.20.3.505DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS — Offset 5022113Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	5022113Ch	000007C0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO	**Reference Slot Number (RSN):** This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.
15:4	07Ch RW	**Slot Interval Value (SIV):** This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us
3:2	0h RO	**Reserved**
1	0h RW	**Advance Slot Check (ASC):** When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set. 0x0 (DISABLE): Advance Slot Check is disabled. 0x1 (ENABLE): Advance Slot Check is enabled.
0	0h RW	**Enable Slot Comparison (ESC):** When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets. 0x0 (DISABLE): Slot Comparison is disabled. 0x1 (ENABLE): Slot Comparison is enabled.

14.20.3.506DMA_CH0_CURRENT_APP_TXDESC — Offset 50221144h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50221144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Descriptor Address Pointer (CURTDESAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

14.20.3.507DMA_CH0_CURRENT_APP_RXDESC — Offset 5022114Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	5022114Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Descriptor Address Pointer (CURRDESAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

14.20.3.508DMA_CH0_CURRENT_APP_TXBUFFER_H — Offset 50221150h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50221150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTRH):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

14.20.3.509DMA_CH0_CURRENT_APP_TXBUFFER — Offset 50221154h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50221154h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Transmit Buffer Address Pointer (CURTBUFAPTR):** The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

14.20.3.510DMA_CH0_CURRENT_APP_RXBUFFER_H — Offset 50221158h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	50221158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTRH):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

14.20.3.511DMA_CH0_CURRENT_APP_RXBUFFER — Offset 5022115Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	5022115Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Application Receive Buffer Address Pointer (CURRBUFAPTR):** The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

14.20.3.512DMA_CH0_STATUS — Offset 50221160h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	50221160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO	**Rx DMA Error Bits (REB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO	**Tx DMA Error Bits (TEB):** This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	0h RW	**Normal Interrupt Summary (NIS):** Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected. 0x1 (ACTIVE): Normal Interrupt Summary status detected.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Abnormal Interrupt Summary (AIS):** Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected. 0x1 (ACTIVE): Abnormal Interrupt Summary status detected.
13	0h RW	**Context Descriptor Error (CDE):** This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected. 0x1 (ACTIVE): Context Descriptor Error status detected.
12	0h RW	**Fatal Bus Error (FBE):** This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected. 0x1 (ACTIVE): Fatal Bus Error status detected.
11	0h RW	**Early Receive Interrupt (ERI):** This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected. 0x1 (ACTIVE): Early Receive Interrupt status detected.
10	0h RW	**Early Transmit Interrupt (ETI):** This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected. 0x1 (ACTIVE): Early Transmit Interrupt status detected.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Receive Watchdog Timeout (RWT):** This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0x0 (INACTIVE): Receive Watchdog Timeout status not detected. 0x1 (ACTIVE): Receive Watchdog Timeout status detected.
8	0h RW	**Receive Process Stopped (RPS):** This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected. 0x1 (ACTIVE): Receive Process Stopped status detected.
7	0h RW	**Receive Buffer Unavailable (RBU):** This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected. 0x1 (ACTIVE): Receive Buffer Unavailable status detected.
6	0h RW	**Receive Interrupt (RI):** This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected. 0x1 (ACTIVE): Receive Interrupt status detected.
5:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Transmit Buffer Unavailable (TBU):** This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected. 0x1 (ACTIVE): Transmit Buffer Unavailable status detected.
1	0h RW	**Transmit Process Stopped (TPS):** This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected. 0x1 (ACTIVE): Transmit Process Stopped status detected.
0	0h RW	**Transmit Interrupt (TI):** This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected. 0x1 (ACTIVE): Transmit Interrupt status detected.

14.20.3.513DMA_CH0_MISS_FRAME_CNT — Offset 50221164h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	50221164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**Overflow status of the MFC Counter (MFCO):** When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred. 0x1 (ACTIVE): Miss Frame Counter overflow occurred.
14:11	0h RO	**Reserved**
10:0	000h RO	**Dropped Packet Counters (MFC):** This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

14.20.3.514DMA_CH0_RXP_ACCEPT_CNT — Offset 50221168h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Type	Size	Offset	Default
MMIO	32 bit	50221168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Parser Accept Counter Overflow Bit (RXPACOF):** When set, this bit indicates that the RXPAC Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Rx Parser Accept Counter overflow not occurred. 0x1 (ACTIVE): Rx Parser Accept Counter overflow occurred.
30:0	00000000h RO	**Rx Parser Accept Counter (RXPAC):** This 31-bit counter is implemented whenever a Rx Parser Accept a packet due to AF =1. The counter is cleared when the register is read.

14.20.3.515DMA_CH0_RX_ERI_CNT — Offset 5022116Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	5022116Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO	**ERI Counter (ECNT):** When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

14.20.3.516DMA_CH1_CONTROL — Offset 50221180h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 50221100h.

14.20.3.517DMA_CH1_TX_CONTROL — Offset 50221184h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.518DMA_CH1_RX_CONTROL — Offset 50221188h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.519DMA_CH1_TXDESC_LIST_HADDRESS — Offset 50221190h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.520DMA_CH1_TXDESC_LIST_ADDRESS — Offset 50221194h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.521DMA_CH1_RXDESC_LIST_HADDRESS — Offset 50221198h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.522DMA_CH1_RXDESC_LIST_ADDRESS — Offset 5022119Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.523DMA_CH1_TXDESC_TAIL_POINTER — Offset 502211A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.524DMA_CH1_RXDESC_TAIL_POINTER — Offset 502211A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.525DMA_CH1_TXDESC_RING_LENGTH — Offset 502211ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.526DMA_CH1_RXDESC_RING_LENGTH — Offset 502211B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.527DMA_CH1_INTERRUPT_ENABLE — Offset 502211B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.528DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502211B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.529DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS — Offset 502211BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.530DMA_CH1_CURRENT_APP_TXDESC — Offset 502211C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.531DMA_CH1_CURRENT_APP_RXDESC — Offset 502211CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.532DMA_CH1_CURRENT_APP_TXBUFFER_H — Offset 502211D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.533DMA_CH1_CURRENT_APP_TXBUFFER — Offset 502211D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.534DMA_CH1_CURRENT_APP_RXBUFFER_H — Offset 502211D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.535DMA_CH1_CURRENT_APP_RXBUFFER — Offset 502211DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.536DMA_CH1_STATUS — Offset 502211E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.537DMA_CH1_MISS_FRAME_CNT — Offset 502211E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.538DMA_CH1_RXP_ACCEPT_CNT — Offset 502211E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.539DMA_CH1_RX_ERI_CNT — Offset 502211ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.3.540DMA_CH2_CONTROL — Offset 50221200h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 50221100h.

14.20.3.541DMA_CH2_TX_CONTROL — Offset 50221204h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.542DMA_CH2_RX_CONTROL — Offset 50221208h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.543DMA_CH2_TXDESC_LIST_HADDRESS — Offset 50221210h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.544DMA_CH2_TXDESC_LIST_ADDRESS — Offset 50221214h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.545DMA_CH2_RXDESC_LIST_HADDRESS — Offset 50221218h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.546DMA_CH2_RXDESC_LIST_ADDRESS — Offset 5022121Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.547DMA_CH2_TXDESC_TAIL_POINTER — Offset 50221220h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.548DMA_CH2_RXDESC_TAIL_POINTER — Offset 50221228h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.549DMA_CH2_TXDESC_RING_LENGTH — Offset 5022122Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.550DMA_CH2_RXDESC_RING_LENGTH — Offset 50221230h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.551DMA_CH2_INTERRUPT_ENABLE — Offset 50221234h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.552DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50221238h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.553DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS — Offset 5022123Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.554DMA_CH2_CURRENT_APP_TXDESC — Offset 50221244h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.555DMA_CH2_CURRENT_APP_RXDESC — Offset 5022124Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.556DMA_CH2_CURRENT_APP_TXBUFFER_H — Offset 50221250h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.557DMA_CH2_CURRENT_APP_TXBUFFER — Offset 50221254h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.558DMA_CH2_CURRENT_APP_RXBUFFER_H — Offset 50221258h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.559DMA_CH2_CURRENT_APP_RXBUFFER — Offset 5022125Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.560DMA_CH2_STATUS — Offset 50221260h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.561DMA_CH2_MISS_FRAME_CNT — Offset 50221264h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.562DMA_CH2_RXP_ACCEPT_CNT — Offset 50221268h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.563DMA_CH2_RX_ERI_CNT — Offset 5022126Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.3.564DMA_CH3_CONTROL — Offset 50221280h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 50221100h.

14.20.3.565DMA_CH3_TX_CONTROL — Offset 50221284h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.566DMA_CH3_RX_CONTROL — Offset 50221288h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.567DMA_CH3_TXDESC_LIST_HADDRESS — Offset 50221290h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.568DMA_CH3_TXDESC_LIST_ADDRESS — Offset 50221294h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the

corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.569DMA_CH3_RXDESC_LIST_HADDRESS — Offset 50221298h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.570DMA_CH3_RXDESC_LIST_ADDRESS — Offset 5022129Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.571DMA_CH3_TXDESC_TAIL_POINTER — Offset 502212A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.572DMA_CH3_RXDESC_TAIL_POINTER — Offset 502212A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.573DMA_CH3_TXDESC_RING_LENGTH — Offset 502212ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.574DMA_CH3_RXDESC_RING_LENGTH — Offset 502212B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.575DMA_CH3_INTERRUPT_ENABLE — Offset 502212B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.576DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502212B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.577DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS — Offset 502212BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.578DMA_CH3_CURRENT_APP_TXDESC — Offset 502212C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.579DMA_CH3_CURRENT_APP_RXDESC — Offset 502212CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.580DMA_CH3_CURRENT_APP_TXBUFFER_H — Offset 502212D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.581DMA_CH3_CURRENT_APP_TXBUFFER — Offset 502212D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.582DMA_CH3_CURRENT_APP_RXBUFFER_H — Offset 502212D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.583DMA_CH3_CURRENT_APP_RXBUFFER — Offset 502212DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.584DMA_CH3_STATUS — Offset 502212E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.585DMA_CH3_MISS_FRAME_CNT — Offset 502212E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.586DMA_CH3_RXP_ACCEPT_CNT — Offset 502212E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.587DMA_CH3_RX_ERI_CNT — Offset 502212ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.3.588DMA_CH4_CONTROL — Offset 50221300h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	50221300h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**Split Headers (SPH):** When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. 0x0 (DISABLE): Split Headers feature is disabled. 0x1 (ENABLE): Split Headers feature is enabled.
23:21	0h RO	**Reserved**
20:18	0h RW	**Descriptor Skip Length (DSL):** This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**8xPBL mode (PBLX8):** When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled. 0x1 (ENABLE): 8xPBL mode is enabled.
15:0	0h RO	**Reserved**

14.20.3.589DMA_CH4_TX_CONTROL — Offset 50221304h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.590DMA_CH4_RX_CONTROL — Offset 50221308h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.591DMA_CH4_TXDESC_LIST_HADDRESS — Offset 50221310h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.592DMA_CH4_TXDESC_LIST_ADDRESS — Offset 50221314h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.593DMA_CH4_RXDESC_LIST_HADDRESS — Offset 50221318h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.594DMA_CH4_RXDESC_LIST_ADDRESS — Offset 5022131Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped,

this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.595DMA_CH4_TXDESC_TAIL_POINTER — Offset 50221320h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.596DMA_CH4_RXDESC_TAIL_POINTER — Offset 50221328h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.597DMA_CH4_TXDESC_RING_LENGTH — Offset 5022132Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.598DMA_CH4_RXDESC_RING_LENGTH — Offset 50221330h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.599DMA_CH4_INTERRUPT_ENABLE — Offset 50221334h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.600DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50221338h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.601DMA_CH4_SLOT_FUNCTION_CONTROL_STATUS — Offset 5022133Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.602DMA_CH4_CURRENT_APP_TXDESC — Offset 50221344h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.603DMA_CH4_CURRENT_APP_RXDESC — Offset 5022134Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.604DMA_CH4_CURRENT_APP_TXBUFFER_H — Offset 50221350h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.605DMA_CH4_CURRENT_APP_TXBUFFER — Offset 50221354h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.606DMA_CH4_CURRENT_APP_RXBUFFER_H — Offset 50221358h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.607DMA_CH4_CURRENT_APP_RXBUFFER — Offset 5022135Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.608DMA_CH4_STATUS — Offset 50221360h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.609DMA_CH4_MISS_FRAME_CNT — Offset 50221364h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.610DMA_CH4_RXP_ACCEPT_CNT — Offset 50221368h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.611DMA_CH4_RX_ERI_CNT — Offset 5022136Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.3.612DMA_CH5_CONTROL — Offset 50221380h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 50221300h.

14.20.3.613DMA_CH5_TX_CONTROL — Offset 50221384h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.614DMA_CH5_RX_CONTROL — Offset 50221388h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.615DMA_CH5_TXDESC_LIST_HADDRESS — Offset 50221390h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.616DMA_CH5_TXDESC_LIST_ADDRESS — Offset 50221394h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.617DMA_CH5_RXDESC_LIST_HADDRESS — Offset 50221398h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.618DMA_CH5_RXDESC_LIST_ADDRESS — Offset 5022139Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.619DMA_CH5_TXDESC_TAIL_POINTER — Offset 502213A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.620DMA_CH5_RXDESC_TAIL_POINTER — Offset 502213A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.621DMA_CH5_TXDESC_RING_LENGTH — Offset 502213ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.622DMA_CH5_RXDESC_RING_LENGTH — Offset 502213B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.623DMA_CH5_INTERRUPT_ENABLE — Offset 502213B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.624DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502213B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.625DMA_CH5_SLOT_FUNCTION_CONTROL_STATUS — Offset 502213BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.626DMA_CH5_CURRENT_APP_TXDESC — Offset 502213C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.627DMA_CH5_CURRENT_APP_RXDESC — Offset 502213CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.628DMA_CH5_CURRENT_APP_TXBUFFER_H — Offset 502213D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.629DMA_CH5_CURRENT_APP_TXBUFFER — Offset 502213D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.630DMA_CH5_CURRENT_APP_RXBUFFER_H — Offset 502213D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.631DMA_CH5_CURRENT_APP_RXBUFFER — Offset 502213DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.632DMA_CH5_STATUS — Offset 502213E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.633DMA_CH5_MISS_FRAME_CNT — Offset 502213E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.634DMA_CH5_RXP_ACCEPT_CNT — Offset 502213E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.635DMA_CH5_RX_ERI_CNT — Offset 502213ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.3.636DMA_CH6_CONTROL — Offset 50221400h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 50221300h.

14.20.3.637DMA_CH6_TX_CONTROL — Offset 50221404h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.638DMA_CH6_RX_CONTROL — Offset 50221408h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.639DMA_CH6_TXDESC_LIST_HADDRESS — Offset 50221410h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.640DMA_CH6_TXDESC_LIST_ADDRESS — Offset 50221414h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.641DMA_CH6_RXDESC_LIST_HADDRESS — Offset 50221418h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.642DMA_CH6_RXDESC_LIST_ADDRESS — Offset 5022141Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.643DMA_CH6_TXDESC_TAIL_POINTER — Offset 50221420h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.644DMA_CH6_RXDESC_TAIL_POINTER — Offset 50221428h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.645DMA_CH6_TXDESC_RING_LENGTH — Offset 5022142Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.646DMA_CH6_RXDESC_RING_LENGTH — Offset 50221430h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.647DMA_CH6_INTERRUPT_ENABLE — Offset 50221434h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.648DMA_CH6_RX_INTERRUPT_WATCHDOG_TIMER — Offset 50221438h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.649DMA_CH6_SLOT_FUNCTION_CONTROL_STATUS — Offset 5022143Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.650DMA_CH6_CURRENT_APP_TXDESC — Offset 50221444h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.651DMA_CH6_CURRENT_APP_RXDESC — Offset 5022144Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.652DMA_CH6_CURRENT_APP_TXBUFFER_H — Offset 50221450h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.653DMA_CH6_CURRENT_APP_TXBUFFER — Offset 50221454h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.654DMA_CH6_CURRENT_APP_RXBUFFER_H — Offset 50221458h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.655DMA_CH6_CURRENT_APP_RXBUFFER — Offset 5022145Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.656DMA_CH6_STATUS — Offset 50221460h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.657DMA_CH6_MISS_FRAME_CNT — Offset 50221464h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.658DMA_CH6_RXP_ACCEPT_CNT — Offset 50221468h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.659DMA_CH6_RX_ERI_CNT — Offset 5022146Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.3.660DMA_CH7_CONTROL — Offset 50221480h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 50221300h.

14.20.3.661DMA_CH7_TX_CONTROL — Offset 50221484h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 50221104h.

14.20.3.662DMA_CH7_RX_CONTROL — Offset 50221488h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 50221108h.

14.20.3.663DMA_CH7_TXDESC_LIST_HADDRESS — Offset 50221490h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 50221110h.

14.20.3.664DMA_CH7_TXDESC_LIST_ADDRESS — Offset 50221494h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 50221114h.

14.20.3.665DMA_CH7_RXDESC_LIST_HADDRESS — Offset 50221498h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 50221118h.

14.20.3.666DMA_CH7_RXDESC_LIST_ADDRESS — Offset 5022149Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 5022111Ch.

14.20.3.667DMA_CH7_TXDESC_TAIL_POINTER — Offset 502214A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 50221120h.

14.20.3.668DMA_CH7_RXDESC_TAIL_POINTER — Offset 502214A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 50221128h.

14.20.3.669DMA_CH7_TXDESC_RING_LENGTH — Offset 502214ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 5022112Ch.

14.20.3.670DMA_CH7_RXDESC_RING_LENGTH — Offset 502214B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 50221130h.

14.20.3.671DMA_CH7_INTERRUPT_ENABLE — Offset 502214B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 50221134h.

14.20.3.672DMA_CH7_RX_INTERRUPT_WATCHDOG_TIMER — Offset 502214B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 50221138h.

14.20.3.673DMA_CH7_SLOT_FUNCTION_CONTROL_STATUS — Offset 502214BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 5022113Ch.

14.20.3.674DMA_CH7_CURRENT_APP_TXDESC — Offset 502214C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 50221144h.

14.20.3.675DMA_CH7_CURRENT_APP_RXDESC — Offset 502214CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 5022114Ch.

14.20.3.676DMA_CH7_CURRENT_APP_TXBUFFER_H — Offset 502214D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 50221150h.

14.20.3.677DMA_CH7_CURRENT_APP_TXBUFFER — Offset 502214D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 50221154h.

14.20.3.678DMA_CH7_CURRENT_APP_RXBUFFER_H — Offset 502214D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 50221158h.

14.20.3.679DMA_CH7_CURRENT_APP_RXBUFFER — Offset 502214DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 5022115Ch.

14.20.3.680DMA_CH7_STATUS — Offset 502214E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH(#i)_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 50221160h.

14.20.3.681DMA_CH7_MISS_FRAME_CNT — Offset 502214E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 50221164h.

14.20.3.682DMA_CH7_RXP_ACCEPT_CNT — Offset 502214E8h

The DMA_CH(#i)_RXP_Accept_Cnt registers provides the count of the number of frames accepted by Rx Parser.

Note: Bit definitions are the same as DMA_CH0_RXP_ACCEPT_CNT, offset 50221168h.

14.20.3.683DMA_CH7_RX_ERI_CNT — Offset 502214ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 5022116Ch.

14.20.4 GbE_1 TSN MISC Registers Summary

Table 14-47. Summary of GbE_1 TSN MISC Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50230000h	4	DMA ControlChannel0 (DMA_CTL_CH0)	00000000h
50230004h	4	DMA ControlChannel1 (DMA_CTL_CH1)	00000000h
50230008h	4	DMA ControlChannel2 (DMA_CTL_CH2)	00000000h
5023000Ch	4	DMA ControlChannel3 (DMA_CTL_CH3)	00000000h
50230010h	4	DMA ControlChannel4 (DMA_CTL_CH4)	00000000h
50230014h	4	DMA ControlChannel5 (DMA_CTL_CH5)	00000000h
50230018h	4	DMA ControlChannel6 (DMA_CTL_CH6)	00000000h
5023001Ch	4	DMA ControlChannel7 (DMA_CTL_CH7)	00000000h
50230020h	4	DMA ControlChannel8 (DMA_CTL_CH8)	00000000h
50230024h	4	DMA ControlChannel9 (DMA_CTL_CH9)	00000000h
50230028h	4	DMA ControlChannel10 (DMA_CTL_CH10)	00000000h
5023002Ch	4	DMA ControlChannel11 (DMA_CTL_CH11)	00000000h
50230030h	4	DMA ControlChannel12 (DMA_CTL_CH12)	00000000h
50230034h	4	DMA ControlChannel13 (DMA_CTL_CH13)	00000000h
50230038h	4	DMA ControlChannel14 (DMA_CTL_CH14)	00000000h
5023003Ch	4	DMA ControlChannel15 (DMA_CTL_CH15)	00000000h
50230100h	4	DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0)	00000000h
50230104h	4	DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1)	00000000h
50230108h	4	DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2)	00000000h
5023010Ch	4	DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3)	00000000h
50230110h	4	DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4)	00000000h
50230114h	4	DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5)	00000000h
50230118h	4	DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6)	00000000h
5023011Ch	4	DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7)	00000000h
50230120h	4	DMA CH8 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH8)	00000000h
50230124h	4	DMA CH9 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH9)	00000000h
50230128h	4	DMA CH10 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH10)	00000000h
5023012Ch	4	DMA CH11 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH11)	00000000h
50230130h	4	DMA CH12 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH12)	00000000h
50230134h	4	DMA CH13 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH13)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50230138h	4	DMA CH14 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH14)	00000000h
5023013Ch	4	DMA CH15 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH15)	00000000h
50230200h	4	DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0)	00000000h
50230204h	4	DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1)	00000000h
50230208h	4	DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2)	00000000h
5023020Ch	4	DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3)	00000000h
50230210h	4	DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4)	00000000h
50230214h	4	DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5)	00000000h
50230218h	4	DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6)	00000000h
5023021Ch	4	DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7)	00000000h
50230220h	4	DMA CH8 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH8)	00000000h
50230224h	4	DMA CH9 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH9)	00000000h
50230228h	4	DMA CH10 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH10)	00000000h
5023022Ch	4	DMA CH11 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH11)	00000000h
50230230h	4	DMA CH12 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH12)	00000000h
50230234h	4	DMA CH13 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH13)	00000000h
50230238h	4	DMA CH14 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH14)	00000000h
5023023Ch	4	DMA CH15 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH15)	00000000h
50230410h	4	D0i3 Control (D0I3C)	00000008h
50230414h	4	Clock Gating And Soft Rset (CSGR)	00000000h
50230418h	4	GBE DMA Interrupt Enable (DMA_INT_EN)	0000FFFFh
50230500h	4	DLL Configuration (DLL_CFG)	00000010h

14.20.4.1 DMA ControlChannel0 (DMA_CTL_CH0) — Offset 50230000h

DMA Control register channel0.

Type	Size	Offset	Default
MMIO	32 bit	50230000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface. When RT_Disable fuse is active, this bit is internally tied to '0'.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel0 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel0 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.2 DMA ControlChannel1 (DMA_CTL_CH1) — Offset 50230004h

DMA Control register channel1.

Type	Size	Offset	Default
MMIO	32 bit	50230004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel1 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel1 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.3 DMA ControlChannel2 (DMA_CTL_CH2) — Offset 50230008h

DMA Control register channel2.

Type	Size	Offset	Default
MMIO	32 bit	50230008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel2 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel2 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.4 DMA ControlChannel3 (DMA_CTL_CH3) — Offset 5023000Ch

DMA Control register channel3.

Type	Size	Offset	Default
MMIO	32 bit	5023000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel3 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel3 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.5 DMA ControlChannel4 (DMA_CTL_CH4) — Offset 50230010h

DMA Control register channel4.

Type	Size	Offset	Default
MMIO	32 bit	50230010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel4 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel4 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.6 DMA ControlChannel5 (DMA_CTL_CH5) — Offset 50230014h

DMA Control register channel5.

Type	Size	Offset	Default
MMIO	32 bit	50230014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel5 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel5 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.7 DMA ControlChannel6 (DMA_CTL_CH6) — Offset 50230018h

DMA Control register channel6.

Type	Size	Offset	Default
MMIO	32 bit	50230018h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel6 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel6 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.8 DMA ControlChannel7 (DMA_CTL_CH7) — Offset 5023001Ch

DMA Control register channel7.

Type	Size	Offset	Default
MMIO	32 bit	5023001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel7 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel7 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.9 DMA ControlChannel8 (DMA_CTL_CH8) — Offset 50230020h

DMA Control register channel8.

Type	Size	Offset	Default
MMIO	32 bit	50230020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel8 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel8 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.10 DMA ControlChannel9 (DMA_CTL_CH9) — Offset 50230024h

DMA Control register channel9.

Type	Size	Offset	Default
MMIO	32 bit	50230024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel9 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel9 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.11 DMA ControlChannel10 (DMA_CTL_CH10) — Offset 50230028h

DMA Control register channel10.

Type	Size	Offset	Default
MMIO	32 bit	50230028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel10 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel10 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.12 DMA ControlChannel11 (DMA_CTL_CH11) — Offset 5023002Ch

DMA Control register channel11.

Type	Size	Offset	Default
MMIO	32 bit	5023002Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel11 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel11 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.13 DMA ControlChannel12 (DMA_CTL_CH12) — Offset 50230030h

DMA Control register channel12.

Type	Size	Offset	Default
MMIO	32 bit	50230030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel12 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel12 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.14 DMA ControlChannel13 (DMA_CTL_CH13) — Offset 50230034h

DMA Control register channel13.

Type	Size	Offset	Default
MMIO	32 bit	50230034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel13 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel13 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.15 DMA ControlChannel14 (DMA_CTL_CH14) — Offset 50230038h

DMA Control register channel14.

Type	Size	Offset	Default
MMIO	32 bit	50230038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channe14 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel14 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.16 DMA ControlChannel15 (DMA_CTL_CH15) — Offset 5023003Ch

DMA Control register channel15.

Type	Size	Offset	Default
MMIO	32 bit	5023003Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RW	**Vc0/1 Wr (IOSF_WR_VC01):** When set, enables VC1 transaction on IOSF AXI Write port. When reset, enables VC0 transaction on IOSF AXI Write port. When RT_Disable fuse is active, this bit is internally tied to '0'.
10	0h RW	**Vc0/1 Rd (IOSF_RD_VC01):** When set, enables VC1 transaction on IOSF AXI Read port. When reset, enables VC0 transaction on IOSF AXI Read port. When RT_Disable fuse is active, this bit is internally tied to '0'.
9	0h RW	**Write Non Snoop Attribute (WR_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF write port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
8	0h RW	**Read Non Snoop Attribute (RD_NON_SNOOP):** If asserted indicates the transaction from DMA channel0 on IOSF read port is not required to be snooped This bit comes out as req_ns on IOSF master interface.
7	0h RO	**Reserved**
6:5	0h RO	**Write Root Space (WR_RS):** Root Space attribute for DMA channel15 writes on IOSF. The read value of these bits will always be 00 .
4:3	0h RO	**Read Root Space (RD_RS):** Root Space attribute for DMA channel15 reads on IOSF. The read value of these bits will always be 00 .
2	0h RO	**Reserved**
1:0	0h RW	**DMA Transfer Mode (TRANSFER_MODE):** Indicates mode of transfer for DMA channel0. Four modes are possible: 11 - DRAM to DRAM mode (external, read from DRAM and write to DRAM), 10 - DRAM to SRAM (read from DRAM and write to SRAM), 01 - SRAM to DRAM (read from SRAM and write to DRAM), 00 - SRAM to SRAM (internal, read from SRAM and write to SRAM). In host owned mode, these bits are internally tied to 11 . In proxy mode (when GBE_PROXYMODE bit '0' is set), these bits are internally tied to '00'.

14.20.4.17 DMA CH0 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH0) — Offset 50230100h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Type	Size	Offset	Default
MMIO	32 bit	50230100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Maddr MSB (ADDR_FILLIN):** MSB bits of maddr to drive on IOSF.

14.20.4.18 DMA CH1 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH1) — Offset 50230104h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.19 DMA CH2 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH2) — Offset 50230108h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.20 DMA CH3 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH3) — Offset 5023010Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.21 DMA CH4 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH4) — Offset 50230110h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.22 DMA CH5 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH5) — Offset 50230114h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.23 DMA CH6 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH6) — Offset 50230118h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.24 DMA CH7 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH7) — Offset 5023011Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.25 DMA CH8 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH8) — Offset 50230120h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.26 DMA CH9 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH9) — Offset 50230124h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.27 DMA CH10 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH10) — Offset 50230128h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.28 DMA CH11 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH11) — Offset 5023012Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.29 DMA CH12 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH12) — Offset 50230130h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.30 DMA CH13 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH13) — Offset 50230134h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.31 DMA CH14 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH14) — Offset 50230138h

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.32 DMA CH15 Read Address Fillin (IOSF_ADDR_FILLIN_DMA_CH15) — Offset 5023013Ch

This register defines the upper MSB bits of maddress port to drive on the IOSF maddr for reads.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.33 DMA CH0 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH0) — Offset 50230200h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.34 DMA CH1 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH1) — Offset 50230204h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.35 DMA CH2 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH2) — Offset 50230208h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.36 DMA CH3 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH3) — Offset 5023020Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.37 DMA CH4 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH4) — Offset 50230210h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.38 DMA CH5 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH5) — Offset 50230214h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.39 DMA CH6 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH6) — Offset 50230218h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.40 DMA CH7 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH7) — Offset 5023021Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.41 DMA CH8 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH8) — Offset 50230220h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.42 DMA CH9 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH9) — Offset 50230224h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.43 DMA CH10 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH10) — Offset 50230228h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.44 DMA CH11 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH11) — Offset 5023022Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.45 DMA CH12 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH12) — Offset 50230230h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.46 DMA CH13 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH13) — Offset 50230234h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.47 DMA CH14 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH14) — Offset 50230238h

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.48 DMA CH15 Write Address Fillin (IOSF_DEST_ADDR_FILLIN_DMA_CH15) — Offset 5023023Ch

This register defines the upper MSB bits to drive on the IOSF maddr for writes.

Note: Bit definitions are the same as IOSF_ADDR_FILLIN_DMA_CH0, offset 50230100h.

14.20.4.49 D0i3 Control (D0I3C) — Offset 50230410h

This register is will be used for D0i3 SW flow. This will be mapped to a different MMIO address from the other IPC registers. (MMIO and OCP address value are To be done) The description below also includes the type of access expected for the ISH FW for each configuration bit: 1. The Restore Required (RR) bit (bit [3]) should be RW for the ISH FW which can determine when to set and/or clear these bits depending on when the ISH FW determines whether restore is required although for ISH restore is never required since the power is never lost. 2. The D0i3 (i3) bit (bit [2]) should be RO for ISH FW as it needs to be written only by host SW. The ISH FW can determine to go to a low power state based on this bit. 3. The Interrupt Required (IR) bit (bit [1]) can be RO register for ISH FW and ISH FW can send an interrupt to Host by writing to the ish2host IPC doorbell register when this bit is set by SW. 4. The Command in Progress (CIP) register bit (bit [0]) is HW set and need to be cleared by ISH FW (Write 1 to clear). The CIP register bit will be tied to a RTE entry in the IOAPIC as an interrupt source. Hence ISH FW will get an interrupt when the In addition to the registers, the IOSF2OCP Bridge should be parameterized for the following: 1. The device idle capability parameter (ENABLE_PCI_IDLE_CAP) need to be connected to a soft strap for ISH with a value of 1. 2. The STRAP for the MMIO address (strap_d0i3_offset) of D0i3 register (IPC offset address: h6D0) and the d0i3 valid (strap_d0i3_valid) bit needs should be appropriately tied. 3. The PCE register is made RO register by setting the appropriate parameter (Bridge top level strap: set_device_pg_config_type[5:0] is set to all 0s). This registers reset and clock domain will be in the OCP domain.

Type	Size	Offset	Default
MMIO	32 bit	50230410h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0. For ISH this bit will be tied to 0.
3	1h RW/1C	**Restore Required (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Required (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RW/1C	**Command In Progress (CIP):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.

14.20.4.50 Clock Gating And Soft Rset (CSGR) — Offset 50230414h

This register is used to clock gate or soft reset an IP by Host/Remote Host.

Type	Size	Offset	Default
MMIO	32 bit	50230414h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**Clock Gate Nable (CG):** Setting this field to 1 clock gates the IP.
15:1	0h RO	**Reserved**
0	0h RW	**Soft Reest (SR):** Setting this bit to 1 resets the IP.

14.20.4.51 GBE DMA Interrupt Enable (DMA_INT_EN) — Offset 50230418h

This register is used to program the interrupt enables for GBE Tx/Rx Interrupts.

Type	Size	Offset	Default
MMIO	32 bit	50230418h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW	**Rx Ch 7 Interrupt Enable (INT_EN_RX_CH7):** When Bit 15 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 7. When Bit 15 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 7.
14	1h RW	**Rx Ch 6 Interrupt Enable (INT_EN_RX_CH6):** When Bit 14 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 6. When Bit 14 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 6.
13	1h RW	**Rx Ch 5 Interrupt Enable (INT_EN_RX_CH5):** When Bit 13 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 5. When Bit 13 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 5.
12	1h RW	**Rx Ch 4 Interrupt Enable (INT_EN_RX_CH4):** When Bit 12 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 4. When Bit 12 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 4.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Rx Ch 3 Interrupt Enable (INT_EN_RX_CH3):** When Bit 11 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 3. When Bit 11 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 3.
10	1h RW	**Rx Ch 2 Interrupt Enable (INT_EN_RX_CH2):** When Bit 10 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 2. When Bit 10 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 2.
9	1h RW	**Rx Ch 1 Interrupt Enable (INT_EN_RX_CH1):** When Bit 9 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 1. When Bit 9 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 1.
8	1h RW	**Rx Ch 0 Interrupt Enable (INT_EN_RX_CH0):** When Bit 8 is set, it enables the VC0/VC1 MSI interrupt for GBE Rx channel 0. When Bit 8 is reset, it disables the VC0/VC1 MSI interrupt for GBE Rx channel 0.
7	1h RW	**Tx Ch 7 Interrupt Enable (INT_EN_TX_CH7):** When Bit 7 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 7. When Bit 7 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 7.
6	1h RW	**Tx Ch 6 Interrupt Enable (INT_EN_TX_CH6):** When Bit 6 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 6. When Bit 6 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 6.
5	1h RW	**Tx Ch 5 Interrupt Enable (INT_EN_TX_CH5):** When Bit 5 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 5. When Bit 5 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 5.
4	1h RW	**Tx Ch 4 Interrupt Enable (INT_EN_TX_CH4):** When Bit 4 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 4. When Bit 4 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 4.
3	1h RW	**Tx Ch 3 Interrupt Enable (INT_EN_TX_CH3):** When Bit 3 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 3. When Bit 3 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 3.
2	1h RW	**Tx Ch 2 Interrupt Enable (INT_EN_TX_CH2):** When Bit 2 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 2. When Bit 2 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 2.
1	1h RW	**Tx Ch 1 Interrupt Enable (INT_EN_TX_CH1):** When Bit 1 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 1. When Bit 1 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 1.
0	1h RW	**Tx Ch 0 Interrupt Enable (INT_EN_TX_CH0):** When Bit 0 is set, it enables the VC0/VC1 MSI interrupt for GBE Tx channel 0. When Bit 0 is reset, it disables the VC0/VC1 MSI interrupt for GBE Tx channel 0.

14.20.4.52 DLL Configuration (DLL_CFG) — Offset 50230500h

This register is used to configure DLL slave delay elements, to bypass the DLL slave and to read to DLL master lock live status.

Type	Size	Offset	Default
MMIO	32 bit	50230500h	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO/V	**DLL Master Lock (DLL_LOCK):** When 1 indicated DLL master is locked.
6	0h RW	**DLL Slave Bypass (DLL_BYPASS):** Setting this bit to 1 bypass the DLL slave.
5:0	10h RW	**DLL Slave Delay Elements (TX_DELAY):** Configure total number of delay elements in DLL slave. Resolution is 125ps.

14.21 CAN Interface Registers

There are two CAN Interface registers:-

- CAN_0 Registers
- CAN_1 Registers

Each of CAN register consists; TTCAN, CTL and Parity registers.

CAN Registers	Address Offset	Table
CAN_0	50300000h - 50300614h	Table 14-48
CAN_1	50310000h - 50310614h	Table 14-49

14.21.1 CAN_0 Registers Summary

Table 14-48. Summary of CAN_0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50300000h	4	Core Release Register (CREL)	32150323h
50300004h	4	Endian Register (ENDN)	87654321h
50300008h	4	Customer Register (CUST)	00000000h
5030000Ch	4	Fast Bit Timing and Prescaler Register (DBTP)	00000A33h
50300010h	4	Test Register (TEST)	00000000h
50300014h	4	RAM Watchdog (RWD)	00000000h
50300018h	4	CC Control Register (CCCR)	00000001h
5030001Ch	4	Bit Timing and Prescaler Register (BTP)	06000A03h
50300020h	4	Timestamp Counter Configuration (TSCC)	00000000h
50300024h	4	Timestamp Counter Value (TSCV)	00000000h
50300028h	4	Timeout Counter Configuration (TOCC)	FFFF0000h
5030002Ch	4	Timeout Counter Value (TOCV)	0000FFFFh
50300040h	4	Error Counter Register (ECR)	00000000h
50300044h	4	Protocol Status Register (PSR)	00000707h
50300048h	4	Transmitter Delay Compensation Register (TDCR)	00000000h
50300050h	4	Interrupt Register (IR)	00000000h
50300054h	4	Interrupt Enable (IE)	00000000h
50300058h	4	Interrupt Line Select (ILS)	00000000h
5030005Ch	4	Interrupt Line Enable (ILE)	00000000h
50300080h	4	Global Filter Configuration (GFC)	00000000h
50300084h	4	Standard ID Filter Configuration (SIDFC)	00000000h
50300088h	4	Extended ID Filter Configuration (XIDFC)	00000000h
50300090h	4	Extended ID AND Mask (XIDAM)	1FFFFFFFh
50300094h	4	High Priority Message Status (HPMS)	00000000h
50300098h	4	New Data 1 (NDAT1)	00000000h
5030009Ch	4	New Data 2 (NDAT2)	00000000h
503000A0h	4	RX FIFO 0 Configuration (RXF0C)	00000000h
503000A4h	4	RX FIFO 0 Status (RXF0S)	00000000h
503000A8h	4	RX FIFO 0 Acknowledge (RXF0A)	00000000h
503000ACh	4	RX Buffer Configuration (RXBC)	00000000h
503000B0h	4	RX FIFO 1 Configuration (RXF1C)	00000000h
503000B4h	4	RX FIFO 1 Status (RXF1S)	00000000h
503000B8h	4	RX FIFO 1 Acknowledge (RXF1A)	00000000h
503000BCh	4	Rx Buffer / FIFO Element Size Configuration (RXESC)	00000000h
503000C0h	4	TX Buffer Configuration (TXBC)	00000000h
503000C4h	4	TX FIFO/Queue Status (TXFQS)	00000000h
503000C8h	4	TX Buffer Element Size Configuration (TXESC)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
503000CCh	4	TX Buffer Request Pending (TXBRP)	00000000h
503000D0h	4	TX Buffer Add Request (TXBAR)	00000000h
503000D4h	4	TX Buffer Cancellation Request (TXBCR)	00000000h
503000D8h	4	TX Buffer Transmission Occured (TXBTO)	00000000h
503000DCh	4	TX Buffer Cancellation Finished (TXBCF)	00000000h
503000E0h	4	TX Buffer Transmission Interrupt Enable (TXBTIE)	00000000h
503000E4h	4	Tx Buffer Cancellation Finished Interrupt Enable (TXBCIE)	00000000h
503000F0h	4	TX Event FIFO Configuration (TXEFC)	00000000h
503000F4h	4	TX Event FIFO Status (TXEFS)	00000000h
503000F8h	4	TX Event FIFO Acknowledge (TXEFA)	00000000h
50300100h	4	TT Trigger Memory Configuration (TTTMC)	00000000h
50300104h	4	TT Reference Message Configuration (TTRMC)	00000000h
50300108h	4	TT Operation Configuration (TTOCF)	00010000h
5030010Ch	4	TT Matrix Limits (TTMLM)	00000000h
50300110h	4	TUR Configuration (TURCF)	10000000h
50300114h	4	TT Operation Control (TTOCN)	00000000h
50300118h	4	TT Global Time Preset (TTGTP)	00000000h
5030011Ch	4	TT Time Mark (TTTMK)	00000000h
50300120h	4	TT Interrupt Register (TTIR)	00000000h
50300124h	4	TT Interrupt Enable (TTIE)	00000000h
50300128h	4	TT Interrupt Line Select (TTILS)	00000000h
5030012Ch	4	TT Operation Status (TTOST)	00000080h
50300130h	4	TUR Numerator Actual (TURNA)	00000000h
50300134h	4	TT Local and Global Time (TTLGT)	00000000h
50300138h	4	TT Cycle Time & Count (TTCTC)	003F0000h
5030013Ch	4	TT Capture Time (TTCPT)	00000000h
50300140h	4	TT Cycle Sync Mark (TTCSM)	00000000h
50300500h	4	Message RAM Size (MSG_RAM_SIZE)	00004600h
50300504h	4	CTL	00000000h
50300508h	4	Interrupt Control (INT_CTL)	00000000h
5030050Ch	4	Interrupt Status (INT_STAT)	00000000h
50300510h	4	MSGRAM Address Conflict Status (MSGRAM_ADDR_CONFLICT_STAT)	00000000h
50300514h	4	TTCAN TIMESTAMP CONTROL REGISTER (TIMESTAMP_CTL)	00000000h
50300518h	4	TTCAN LOCAL TIMESTAMP HIGH (LOCALTIMESTAMP_HIGH)	00000000h
5030051Ch	4	TTCAN LOCAL TIMESTAMP LOW (LOCALTIMESTAMP_LOW)	00000000h
50300600h	4	CAN Parity Error Control and Status (PAR_CTL_STAT)	00000003h
50300604h	4	Parity Error Offset (PAR_ERR_OFFSET)	00000000h
50300608h	4	Parity Error Injection Control and Status (PAR_EINJ_CTL_STAT)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5030060Ch	4	Parity Error Injection Offset (PAR_EINJ_OFFSET)	00000000h
50300610h	4	Parity Error Injection Data Mask (PAR_EINJ_DATA_MASK)	00000000h
50300614h	4	Parity Error Injection Parity Mask (PAR_EINJ_PARITY_MASK)	00000000h

14.21.1.1 Core Release Register (CREL) — Offset 50300000h

Type	Size	Offset	Default
MMIO	32 bit	50300000h	32150323h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Core Release (REL):** One digit, BCD-coded. - @@jstokes, Need to wait for IP delivery for reset value
27:24	2h RO	**Step of Core Release (STEP):** One digit, BCD-coded. - @@jstokes, Need to wait for IP delivery for reset value
23:20	1h RO	**Sub-step of Core Release (SUBSTEP):** One digit, BCD-coded. eed to wait for IP delivery for reset value
19:16	5h RO	**Time Stamp Year (YEAR):** One digit, BCD-coded. @@jstokes, Need to wait for IP integration for reset value
15:8	03h RO	**Time Stamp Month (MON):** Two digits, BCD-coded. @@jstokes, Need to wait for IP integration for reset value
7:0	23h RO	**Time Stamp Day (DAY):** Two digits, BCD-coded. @@jstokes, Need to wait for IP integration for reset value

14.21.1.2 Endian Register (ENDN) — Offset 50300004h

Endianness Test Value

Type	Size	Offset	Default
MMIO	32 bit	50300004h	87654321h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	87654321h RO	**Endianness Test Value (ETV):** The endianness test value is 0x87654321

14.21.1.3 Customer Register (CUST) — Offset 50300008h

Address 0x08 is reserved for an optional 32 bit customer-specific register. The Customer Register is intended to hold customer-specific configuration, control, and status bits.

Type	Size	Offset	Default
MMIO	32 bit	50300008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Customer Register Field (CUST_FIELD):** Customer specific register field

14.21.1.4 Fast Bit Timing and Prescaler Register (DBTP) — Offset 5030000Ch

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 25 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 m_ttcan_cclk periods. tq = (FBRP + 1) m_ttcan_cclk period.

FTSEG1 is the sum of Prop_Seg and Phase_Seg1. FTSEG2 is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [FTSEG1 + FTSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq.

The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Note: With a CAN clock (m_ttcan_cclk) of 8 MHz, the reset value of 0x00000A33 configures the M_TTCAN for a fast bit rate of 500 kBit/s.

Note: The bit rate configured for the CAN FD data phase via FBTP must be higher or equal to the bit rate configured for the arbitration phase via BTP.

Type	Size	Offset	Default
MMIO	32 bit	5030000Ch	00000A33h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/L	**Tranceiver Delay Compensation (TDC):** 0= Transceiver Delay Compensation disabled 1= Transceiver Delay Compensation enabled
22:21	0h RO	**Reserved**
20:16	00h RW/L	**Fast Baud Rate Prescaler (FBRP):** 0x00-0x1F : The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:13	0h RO	**Reserved**
12:8	0Ah RW/L	**Fast time segment before sample point (FTSEG1):** 0x1-0xF : Valid values are 1 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7:4	3h RW/L	**Fast time segment after sample point (FTSEG2):** 0x0-0x7 : Valid values are 0 to 7. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
3:0	3h RW/L	**Fast (Re) Synchronization Jump Width (FSJW):** 0x0-0x3 : Valid values are 0 to 3. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

14.21.1.5 Test Register (TEST) — Offset 50300010h

Write access to the Test Register has to be enabled by setting bit CCCR.TEST to . All Test Register functions are set to their reset values when bit CCCR.TEST is reset.

Loop Back Mode and software control of pin can*_tx_o are hardware test modes. Programming of TX not equal to h0 may disturb the message transfer on the CAN bus.

Type	Size	Offset	Default
MMIO	32 bit	50300010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**Receive Pin (RX):** Monitors the actual value of pin can*_rx_i 0= The CAN bus is dominant (can*_rx_i = 0) 1= The CAN bus is recessive (can*_rx_i = 1)
6:5	0h RW/L	**Control of Transmit Pin (TX):** 00 Reset value, can*_tx_o controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin can*_tx_o 10 Dominant (0) level at pin can*_tx_o 11 Recessive (1) at pin m_ttcan_tx
4	0h RW/L	**Loop Back Mode (LBCK):** 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled
3	0h RO	**Check ASC Transmit Control (CAT):** Monitors level at output pin ttcan*_asct_i. 0= Output pin ttcan*_asct_i = 0 1= Output pin ttcan*_asct_i = 1
2	0h RO	**Check ASC Multiplexer Control (CAM):** Monitors level at output pin ttcan*_ascm_i. 0= Output pin ttcan*_ascm_i = 0 1= Output pin ttcan*_ascm_i = 1
1	0h RW/L	**Check ASC Transmit Control (TAT):** Controls output pin ttcan*_asct_i in test mode, ORed with the signal from the FSE 0= Level at pin ttcan*_asct_i controlled by FSE 1= Level at pin ttcan*_asct_i = 1
0	0h RW/L	**Test ASC Transmit Control (TAM):** Controls output pin ttcan*_ascm_i in test mode, ORed with the signal from the FSE 0= Level at pin ttcan*_ascm_i controlled by FSE 1= Level at pin ttcan*_ascm_i = 1

14.21.1.6 RAM Watchdog (RWD) — Offset 50300014h

The RAM Watchdog monitors the READY output of the Message RAM (m_ttcan_aeim_ready). A Message RAM access via the M_TTCANs Generic Master Interface (m_ttcan_aeim_sel active) starts the Message RAM Watchdog Counter with the value configured by RWD.WDC. The counter is reloaded with RWD.WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag IR.WDI is set. The RAM Watchdog Counter is clocked by the Host clock (m_ttcan_hclk).

Type	Size	Offset	Default
MMIO	32 bit	50300014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Watchdog Value (WDV):** Actual Message RAM Watchdog Counter Value.
7:0	00h RW/L	**Watchdog Configuration (WDC):** Start value of the Message RAM Watchdog Counter. With the reset value of 00 the counter is disabled.

14.21.1.7 CC Control Register (CCCR) — Offset 50300018h

Type	Size	Offset	Default
MMIO	32 bit	50300018h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/L	**Non ISO Operation (NISO):** If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO11898-1 1= CAN FD frame format according to Bosch CAN FD Specification V1.0
14	0h RW/L	**Transmit Pause (TXP):** If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame 0= Transmit pause disabled 1= Transmit pause enabled
13	0h RW/L	**Edge Filtering durint Bus Integration (EFBI):** 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/L	**Protocol Exception Handling Disable (PXHD):** 0= Protocol exception handling enabled 1= Protocol exception handling disabled
11:10	0h RO	**Reserved**
9	0h RW/L	**Bit Rate Switch Enable (BRSE):** 0 = Bit rate switching for transmission disabled 1 = Bit rate switching for transmission enabled
8	0h RW/L	**FD Operateion Enable (FDOE):** 0 = FD operation disabled 1 = FD operation enabled
7	0h RW/V/L	**Test Mode Enable (TEST):** 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
6	0h RW/L	**Disable Automatic Retransmission (DAR):** 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled
5	0h RW/V/L	**Bus Monitoring Mode (MON):** Bit MON can only be set by the Host when both CCE and INIT are set to 1. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
4	0h RW	**Clock Stop Request (CSR):** 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	0h RO	**Clock Stop Acknowledge (CSA):** 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk
2	0h RW/V/L	**Restricted Operation Mode (ASM):** Bit ASM can only be set by the Host when both CCE and INIT are set to 1. The bit can be reset by the Host at any time. 0= Normal CAN operation 1= Restricted Operation Mode active This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
1	0h RW/L	**Configuration Change Enable (CCE):** 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = 1)
0	1h RW	**INIT:** 0= Normal Operation 1= Initialization is started

14.21.1.8 Bit Timing and Prescaler Register (BTP) — Offset 5030001Ch

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 81 time quanta. The CAN time quantum may be programmed in the range of 1 to 1024 m_ttcan_cclk periods. tq = (BRP + 1) m_ttcan_cclk period. TSEG1 is the sum of Prop_Seg and Phase_Seg1. TSEG2 is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [TSEG1 + TSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq.

The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Type	Size	Offset	Default
MMIO	32 bit	5030001Ch	06000A03h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	03h RW/L	**Nominal (Re)Synchronization Jump Width (NSJW):** 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
24:16	000h RW/L	**Nominal Bit Rate Prescaler (BRP):** 0x000-0x1FF. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 1023. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With a CAN clock (m_ttcan_cclk) of 8 MHz, the reset value of 0x00000A33 configures the M_TTCAN for a bit rate of 500 kBit/s.
15	0h RO	**Reserved**
14:8	0Ah RW/L	**Time segment before sample point (TSEG1):** 0x01-0xFF. Valid values are 1 to 63. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7	0h RO	**Reserved**
6:0	03h RW/L	**Time segment after sample point (TSEG2):** 0x0-0x7F. Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.

14.21.1.9 Timestamp Counter Configuration (TSCC) — Offset 50300020h

Type	Size	Offset	Default
MMIO	32 bit	50300020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW/L	**Timestamp Counter Prescaler (TCP):** 0x0-0xF. Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:2	0h RO	**Reserved**
1:0	0h RW/L	**Timestamp Select (TSS):** 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as 00

14.21.1.10 Timestamp Counter Value (TSCV) — Offset 50300024h

Type	Size	Offset	Default
MMIO	32 bit	50300024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C	**Timestamp Counter (TSC):** The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = 01, the Timestamp Counter is incremented in multiples of CAN bit times [116] depending on the configuration of TSCC.TCP. Awr ap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = 10, TSC reflects the external Timestamp Counter value. A write access has no impact. Note: A wrap around is a change of the Timestamp Counter value from non-zero to zero not caused by write access to TSCV.

14.21.1.11 Timeout Counter Configuration (TOCC) — Offset 50300028h

Type	Size	Offset	Default
MMIO	32 bit	50300028h	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RW/L	**Timeout Period (TOP):** Start value of the Timeout Counter (down-counter). Configures the Timeout Period.
15:3	0h RO	**Reserved**
2:1	0h RW/L	**Timeout Select (TOS):** When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1
0	0h RW/L	**Enable Timeout Counter (ETOC):** 0= Timeout Counter disabled 1= Timeout Counter enabled

14.21.1.12 Timeout Counter Value (TOCV) — Offset 5030002Ch

Type	Size	Offset	Default
MMIO	32 bit	5030002Ch	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	FFFFh RW/1C	**Timeout Counter (TOC):** The Timeout Counter is decremented in multiples of CAN bit times [116] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS.

14.21.1.13 Error Counter Register (ECR) — Offset 50300040h

Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented. This enables monitoring of collisions between CAN frames and ASC frames.

Type	Size	Offset	Default
MMIO	32 bit	50300040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RO/C	**CAN Error Logging (CEL):** The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO.
15	0h RO	**Recieve Error Passive (RP):** 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128
14:8	00h RO	**Recieve Error Counter (REC):** Actual state of the Receive Error Counter, values between 0 and 127
7:0	00h RO	**Transmit Error Counter (TEC):** Actual state of the Transmit Error Counter, values between 0 and 255

14.21.1.14 Protocol Status Register (PSR) — Offset 50300044h

Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in FLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.

Note: The Bus_Off recovery sequence cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

Type	Size	Offset	Default
MMIO	32 bit	50300044h	00000707h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RO	**Trasmitter Delay Compensation Value (TDCV):** 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_ttcan_tx to m_ttcan_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point Valid values are 0 to 127 mtq
15	0h RO	**Reserved**
14	0h RO/C	**Protocol Exception Event (PXE):** 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred
13	0h RO/C	**Received a CAN FD Message (RFDF):** This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with EDL flag set has been received
12	0h RO/C	**BRS flag of last received CAN FD Message (RBRS):** This bit is set together with REDL, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO/C	**ESI flag of last received CAN FD Message (RESI):** This bit is set together with REDL, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set
10:8	7h RO/V	**Fast Last Error Code (FLEC):** Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	0h RO	**Bus_Off Status (B0):** 0= The M_TTCAN is not Bus_Off 1= The M_TTCAN is in Bus_Off state
6	0h RO	**Warning Status (EW):** 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96
5	0h RO	**Error Passive (EP):** 0= The M_TTCAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_TTCAN is in the Error_Passive state
4:3	0h RO	**ACT:** Monitors the modules CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter
2:0	7h RO/V	**Last Error Code (LEC):** The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0 when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value 1), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to 7. When the LEC shows the value 7, no CAN bus event was detected since the last CPU read access to the Protocol Status Register.

14.21.1.15 Transmitter Delay Compensation Register (TDCR) — Offset 50300048h

Type	Size	Offset	Default
MMIO	32 bit	50300048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:8	00h RW	**Trasmitter Delay Compensation Offset (TDCO):** 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq.
7	0h RO	**Reserved**
6:0	00h RW	**Trasmitter Delay Compensation Filter Window Length (TDCF):** 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measure

14.21.1.16 Interrupt Register (IR) — Offset 50300050h

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position.

Writing a 0 has no effect. A hard reset will clear the register. The configuration of IE controls whether an interrupt is generated. The configuration of ILS controls on which interrupt line an interrupt is signalled.

Type	Size	Offset	Default
MMIO	32 bit	50300050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**Access to Reserved Address (ARA):** 0 = No access to reserved address occurred 1 = Access to reserved address occurred
28	0h RW/1C	**Protocol Error in Data Phase (Data Bit Time is used) (PED):** 0= No Protocol Error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7)
27	0h RW/1C	**Protocol Error in Arbitration Phase (Nominal Bit Time is used) (PEA):** 0= No Arbitration Error in data phase 1= Arbitration error in data phase detected (PSR.DLEC != 0,7)
26	0h RW/1C	**Watchdog Interrupt (WDI):** 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY
25	0h RW/1C	**Bus_Off Status (BO):** 0= Bus_Off status unchanged 1= Bus_Off status changed
24	0h RW/1C	**Warning Status (EW):** 0= Error_Warning status unchanged 1= Error_Warning status changed
23	0h RW/1C	**Error Passive (EP):** 0= Error_Warning status unchanged 1= Error_Warning status changed
22	0h RW/1C	**Error Logging Overflow (ELO):** 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred
21	0h RW/1C	**Bit Error Uncorrected (BEU):** Message RAM bit error detected, uncorrected. Controlled by input signal m_ttcan_aeim_berr[1] generated by an optional external parity / ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to 1. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected (e.g. parity logic)
20	0h RW/1C	**Bit Error Corrected (BEC):** Message RAM bit error detected and corrected. Controlled by input signal m_ttcan_aeim_berr[0] generated by an optional external parity / ECC logic attached to the Message RAM. 0= No bit error detected when reading from Message RAM 1= Bit error detected and corrected (e.g. ECC)

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C	**Message Stored to Dedicated RX Buffer (DRX):** The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer
18	0h RW/1C	**Timeout Occured (TOO):** 0= No timeout 1= Timeout reached
17	0h RW/1C	**Message RAM Access Failure (MRAF):** The flag is set, when the Rx Handler * has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. * was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred
16	0h RW/1C	**Timestamp Wraparound (TSW):** 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around
15	0h RW/1C	**TX Event FIFO Element Lost (TEFL):** 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	0h RW/1C	**TX Event FIFO Full (TEFF):** 0= Tx Event FIFO not full 1= Tx Event FIFO full
13	0h RW/1C	**TX Event FIFO Watermark Reached (TEFW):** 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark
12	0h RW/1C	**TX Event FIFO New Entry (TEFN):** 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element
11	0h RW/1C	**TX FIFO Empty (TFE):** 0= Tx FIFO non-empty 1= Tx FIFO empty
10	0h RW/1C	**Transmission Cancellation Finished (TCF):** 0= No transmission cancellation finished 1= Transmission cancellation finished
9	0h RW/1C	**Transmission Completed (TC):** 0= No transmission completed 1= Transmission completed

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**High Priority Message (HPM):** 0= No high priority message received 1= High priority message received
7	0h RW/1C	**RX FIFO 1 Message Lost (RF1L):** 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	0h RW/1C	**RX FIFO 1 Full (RF1F):** 0= Rx FIFO 1 not full 1= Rx FIFO 1 full
5	0h RW/1C	**RX FIFO 1 Watermark Reached (RF1W):** 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark
4	0h RW/1C	**RX FIFO 1 New Message (RF1N):** 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1
3	0h RW/1C	**RX FIFO 0 Message Lost (RF0L):** 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	0h RW/1C	**RX FIFO 0 Full (RF0F):** 0= Rx FIFO 0 not full 1= Rx FIFO 0 full
1	0h RW/1C	**RX FIFO 0 Watermark Reached (RF0W):** 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark
0	0h RW/1C	**RX FIFO 0 New Message (RF0N):** 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0

14.21.1.17 Interrupt Enable (IE) — Offset 50300054h

The settings in the Interrupt Enable register determine which status changes in the Interrupt Register will be signalled on an interrupt line.

0= Interrupt disabled

1= Interrupt enabled

Type	Size	Offset	Default
MMIO	32 bit	50300054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Access to Reserved Address Enable (ARAE):** 0 = No access to reserved address Disabled 1 = Access to reserved address Enabled
28	0h RW	**Protocol Error in Data Phase Enable (PEDE):** 0= Protocol Error in data phase Disabled 1= Protocol error in data phase Enabled
27	0h RW	**Protocol Error in Arbitration Phase Enable (PEAE):** 0= Arbitration Error in data phase Disabled 1= Arbitration error in data phase Enabled
26	0h RW	**Watchdog Interrupt Interrupt Enable (WDIE):**
25	0h RW	**Bus_Off Status Interrupt Enable (BOE):**
24	0h RW	**Warning Status Interrupt Enable (EWE):**
23	0h RW	**Error Passive Interrupt Enable (EPE):**
22	0h RW	**Error Logging Overflow Interrupt Enable (ELOE):**
21	0h RW	**Bit Error Uncorrected Interrupt Enable (BEUE):**
20	0h RW	**Bit Error Corrected Interrupt Enable (BECE):**
19	0h RW	**Message Stored to Dedicated RX Buffer Interrupt Enable (DRXE):**
18	0h RW	**Timeout Occured Interrupt Enable (TOOE):**
17	0h RW	**Message RAM Access Failure Interrupt Enable (MRAFE):**
16	0h RW	**Timestamp Wraparound Interrupt Enable (TSWE):**
15	0h RW	**TX Event FIFO Element Lost Interrupt Enable (TEFLE):**
14	0h RW	**TX Event FIFO Full Interrupt Enable (TEFFE):**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**TX Event FIFO Watermark Reached Interrupt Enable (TEFWE):**
12	0h RW	**TX Event FIFO New Entry Interrupt Enable (TEFNE):**
11	0h RW	**TX FIFO Empty Interrupt Enable (TFEE):**
10	0h RW	**Transmission Cancellation Finished Interrupt Enable (TCFE):**
9	0h RW	**Transmission Completed Interrupt Enable (TCE):**
8	0h RW	**High Priority Message Interrupt Enable (HPME):**
7	0h RW	**RX FIFO 1 Message Lost Interrupt Enable (RF1LE):**
6	0h RW	**RX FIFO 1 Full Interrupt Enable (RF1FE):**
5	0h RW	**RX FIFO 1 Watermark Reached Interrupt Enable (RF1WE):**
4	0h RW	**RX FIFO 1 New Message Interrupt Enable (RF1NE):**
3	0h RW	**RX FIFO 0 Message Lost Interrupt Enable (RF0LE):**
2	0h RW	**RX FIFO 0 Full Interrupt Enable (RF0FE):**
1	0h RW	**RX FIFO 0 Watermark Reached Interrupt Enable (RF0WE):**
0	0h RW	**RX FIFO 0 New Message Interrupt Enable (RF0NE):**

14.21.1.18 Interrupt Line Select (ILS) — Offset 50300058h

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

0= Interrupt assigned to interrupt line m_ttcan_int0

1= Interrupt assigned to interrupt line m_ttcan_int1

Type	Size	Offset	Default
MMIO	32 bit	50300058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Access to Reserved Address Interrupt Line (ARAL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
28	0h RW	**Protocol Error in Data Phase Interrupt Line (PEDL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
27	0h RW	**Protocol Error in Arbitration Phase Interrupt Line (PEAL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
26	0h RW	**Watchdog Interrupt Interrupt Line (WDIL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
25	0h RW	**Bus_Off Status Interrupt Line (BOL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
24	0h RW	**Warning Status Interrupt Line (EWL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
23	0h RW	**Error Passive Interrupt Line (EPL):**
22	0h RW	**Error Logging Overflow Interrupt Line (ELOL):**
21	0h RW	**Bit Error Uncorrected Interrupt Line (BEUL):**
20	0h RW	**Bit Error Corrected Interrupt Line (BECL):**
19	0h RW	**Message Stored to Dedicated RX Buffer Interrupt Line (DRXL):**
18	0h RW	**Timeout Occured Interrupt Line (TOOL):**
17	0h RW	**Message RAM Access Failure Interrupt Line (MRAFL):**
16	0h RW	**Timestamp Wraparound Interrupt Line (TSWL):**
15	0h RW	**TX Event FIFO Element Lost Interrupt Line (TEFLL):**

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**TX Event FIFO Full Interrupt Line (TEFFL):**
13	0h RW	**TX Event FIFO Watermark Reached Interrupt Line (TEFWL):**
12	0h RW	**TX Event FIFO New Entry Interrupt Line (TEFNL):**
11	0h RW	**TX FIFO Empty Interrupt Line (TFEL):**
10	0h RW	**Transmission Cancellation Finished Interrupt Line (TCFL):**
9	0h RW	**Transmission Completed Interrupt Line (TCL):**
8	0h RW	**High Priority Message Interrupt Line (HPML):**
7	0h RW	**RX FIFO 1 Message Lost Interrupt Line (RF1LL):**
6	0h RW	**RX FIFO 1 Full Interrupt Line (RF1FL):**
5	0h RW	**RX FIFO 1 Watermark Reached Interrupt Line (RF1WL):**
4	0h RW	**RX FIFO 1 New Message Interrupt Line (RF1NL):**
3	0h RW	**RX FIFO 0 Message Lost Interrupt Line (RF0LL):**
2	0h RW	**RX FIFO 0 Full Interrupt Line (RF0FL):**
1	0h RW	**RX FIFO 0 Watermark Reached Interrupt Line (RF0WL):**
0	0h RW	**RX FIFO 0 New Message Interrupt Line (RF0NL):**

14.21.1.19 Interrupt Line Enable (ILE) — Offset 5030005Ch

Each of the two interrupt lines to the CPU can be enabled / disabled separately by programming bits EINT0 and EINT1.

Type	Size	Offset	Default
MMIO	32 bit	5030005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Enable Interrupt Line 1 (EINT1):** 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled
0	0h RW	**Enable Interrupt Line 0 (EINT0):** 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled

14.21.1.20 Global Filter Configuration (GFC) — Offset 50300080h

Global settings for Message ID filtering.

Type	Size	Offset	Default
MMIO	32 bit	50300080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW/L	**Accept Non-matching Frames Standard (ANFS):** Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW/L	**Accept Non-matching Frames Extended (ANFE):** Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject
1	0h RW/L	**Reject Remote Frames Standard (RRFS):** 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs
0	0h RW/L	**Reject Remote Frames Extended (RRFE):** 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs

14.21.1.21 Standard ID Filter Configuration (SIDFC) — Offset 50300084h

Settings for 11-bit standard Message ID filtering.

Type	Size	Offset	Default
MMIO	32 bit	50300084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW/L	**List Size Standard (LSS):** 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements >128= Values greater than 128 are interpreted as 128
15:2	0000h RW/L	**Filter List Standard Start Address (FLSSA):** Start address of standard Message ID filter list (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.22 Extended ID Filter Configuration (XIDFC) — Offset 50300088h

Settings for 29-bit extended Message ID filtering.

Type	Size	Offset	Default
MMIO	32 bit	50300088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW/L	**List Size Extended (LSE):** 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements >64= Values greater than 64 are interpreted as 64
15:2	0000h RW/L	**Filter List Extended Start Address (FLESA):** Start address of extended Message ID filter list (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.23 Extended ID AND Mask (XIDAM) — Offset 50300090h

Type	Size	Offset	Default
MMIO	32 bit	50300090h	1FFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	1FFFFFFFh RW/L	**Extended ID Mask (EIDM):** For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

14.21.1.24 High Priority Message Status (HPMS) — Offset 50300094h

This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Type	Size	Offset	Default
MMIO	32 bit	50300094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**Filter List (FLST):** Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List
14:8	00h RO	**Filter Index (FIDX):** Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7:6	0h RO	**Message Storage Indicator (MSI):** 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1
5:0	00h RO	**Buffer Index (BIDX):** Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = 1.

14.21.1.25 New Data 1 (NDAT1) — Offset 50300098h

Type	Size	Offset	Default
MMIO	32 bit	50300098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**New Data (ND):** The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message

14.21.1.26 New Data 2 (NDAT2) — Offset 5030009Ch

Type	Size	Offset	Default
MMIO	32 bit	5030009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**New Data (ND):** The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message

14.21.1.27 RX FIFO 0 Configuration (RXF0C) — Offset 503000A0h

Type	Size	Offset	Default
MMIO	32 bit	503000A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**FIFO 0 Operation Mode (F0OM):** FIFO 0 can be operated in blocking or in overwrite mode. 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode
30:24	00h RW/L	**RX FIFO 0 Watermark (F0WM):** 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) >64= Watermark interrupt disabled
23	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
22:16	00h RW/L	**RX FIFO 0 Size (F0S):** 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements >64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1
15:2	0000h RW/L	**RX FIFO 0 Start Address (F0SA):** Start address of Rx FIFO 0 in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.28 RX FIFO 0 Status (RXF0S) — Offset 503000A4h

Type	Size	Offset	Default
MMIO	32 bit	503000A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**RX FIFO 0 Message Lost (RF0L):** This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Note: Overwriting the oldest message when RXF0C.F0OM = 1 will not set this flag.
24	0h RO	**RX FIFO 0 Full (F0F):** 0= Rx FIFO 0 not full 1= Rx FIFO 0 full
23:22	0h RO	**Reserved**
21:16	00h RO	**RX FIFO 0 Put Index (F0PI):** Rx FIFO 0 write index pointer, range 0 to 63.
15:14	0h RO	**Reserved**
13:8	00h RO	**RX FIFO 0 Get Index (F0GI):** Rx FIFO 0 read index pointer, range 0 to 63.
7	0h RO	**Reserved**
6:0	00h RO	**RX FIFO 0 Fill Level (F0FL):** Number of elements stored in Rx FIFO 0, range 0 to 64.

14.21.1.29 RX FIFO 0 Acknowledge (RXF0A) — Offset 503000A8h

Type	Size	Offset	Default
MMIO	32 bit	503000A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RX FIFO 0 Acknowledge Index (F0AI):** After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

14.21.1.30 RX Buffer Configuration (RXBC) — Offset 503000ACh

Type	Size	Offset	Default
MMIO	32 bit	503000ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:2	0000h RW/L	**RX Buffer Start Address (RBSA):** Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C.
1:0	0h RO	**Reserved**

14.21.1.31 RX FIFO 1 Configuration (RXF1C) — Offset 503000B0h

Type	Size	Offset	Default
MMIO	32 bit	503000B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**FIFO 1 Operation Mode (F1OM):** FIFO 1 can be operated in blocking or in overwrite mode 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode
30:24	00h RW/L	**RX FIFO 1 Watermark (F1WM):** 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) >64= Watermark interrupt disabled
23	0h RO	**Reserved**
22:16	00h RW/L	**RX FIFO 1 Size (F1S):** 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements >64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S-1
15:2	0000h RW/L	**RX FIFO 1 Start Address (F1SA):** Start address of Rx FIFO 1 in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.32 RX FIFO 1 Status (RXF1S) — Offset 503000B4h

Type	Size	Offset	Default
MMIO	32 bit	503000B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**RX FIFO 1 Message Lost (RF1L):** This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Note: Overwriting the oldest message when RXF1C.F1OM = 1 will not set this flag.
24	0h RO	**RX FIFO 1 Full (F1F):** 0= Rx FIFO 1 not full 1= Rx FIFO 1 full
23:22	0h RO	**Reserved**
21:16	00h RO	**RX FIFO 1 Put Index (F1PI):** Rx FIFO 1 write index pointer, range 0 to 63.
15:14	0h RO	**Reserved**
13:8	00h RO	**RX FIFO 1 Get Index (F1GI):** Rx FIFO 1 read index pointer, range 0 to 63.
7	0h RO	**Reserved**
6:0	00h RO	**RX FIFO 1 Fill Level (F1FL):** Number of elements stored in Rx FIFO 1, range 0 to 64.

14.21.1.33 RX FIFO 1 Acknowledge (RXF1A) — Offset 503000B8h

Type	Size	Offset	Default
MMIO	32 bit	503000B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RX FIFO 1 Acknowledge Index (F1AI):** After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

14.21.1.34 Rx Buffer / FIFO Element Size Configuration (RXESC) — Offset 503000BCh

Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Note: In case the data field size of an acceptedCANframe exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frames data field is ignored.

Type	Size	Offset	Default
MMIO	32 bit	503000BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10:8	0h RW/L	**RX Buffer Data Field Size (RBDS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field
7	0h RO	**Reserved**
6:4	0h RW/L	**RX FIFO 1 Data Field Size (F1DS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field
3	0h RO	**Reserved**
2:0	0h RW/L	**RX FIFO 0 Data Field Size (F0DS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field

14.21.1.35 TX Buffer Configuration (TXBC) — Offset 503000C0h

Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

Type	Size	Offset	Default
MMIO	32 bit	503000C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW/L	**TX FIFO/Queue Mode (TFQM):** 0= Tx FIFO operation 1= Tx Queue operation
29:24	00h RW/L	**Transmit FIFO/Queue Size (TFQS):** 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue >32= Values greater than 32 are interpreted as 32
23:22	0h RO	**Reserved**
21:16	00h RW/L	**Number of Dedicated Transmit Buffers (NDTB):** 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers >32= Values greater than 32 are interpreted as 32
15:2	0000h RW/L	**TX Buffers Start Address (TBSA):** Start address of Tx Buffers section in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.36 TX FIFO/Queue Status (TXFQS) — Offset 503000C4h

The Tx FIFO/Queue status is related to the pending Tx requests listed in register TXBRP. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (TXBRP not yet updated).

Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers.

Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.

Type	Size	Offset	Default
MMIO	32 bit	503000C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**TX FIFO/Queue Full (TFQF):** 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full
20:16	00h RO	**TX FIFO/Queue Put Index (TFQPI):** Tx FIFO/Queue write index pointer, range 0 to 31.
15:13	0h RO	**Reserved**
12:8	00h RO	**TX FIFO Get Index (TFGI):** Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1).
7:6	0h RO	**Reserved**
5:0	00h RO	**TX FIFO Free Level (TFFL):** Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1)

14.21.1.37 TX Buffer Element Size Configuration (TXESC) — Offset 503000C8h

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Type	Size	Offset	Default
MMIO	32 bit	503000C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**TX Buffer Data Field Size (TBDS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as 0xCC (padding bytes).

14.21.1.38 TX Buffer Request Pending (TXBRP) — Offset 503000CCh

Type	Size	Offset	Default
MMIO	32 bit	503000CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmission Request Pending (TRP):** Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signalled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission. In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding TXBRP bit is reset.

14.21.1.39 TX Buffer Add Request (TXBAR) — Offset 503000D0h

Type	Size	Offset	Default
MMIO	32 bit	503000D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Add Request (AR):** Each Tx Buffer has its own Add Request bit. Writing a 1 will set the corresponding Add Request bit; writing a 0 has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored.

14.21.1.40 TX Buffer Cancellation Request (TXBCR) — Offset 503000D4h

Type	Size	Offset	Default
MMIO	32 bit	503000D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cancellation Request (CR):** Each Tx Buffer has its own Cancellation Request bit. Writing a 1 will set the corresponding Cancellation Request bit; writing a 0 has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending

14.21.1.41 TX Buffer Transmission Occured (TXBTO) — Offset 503000D8h

Type	Size	Offset	Default
MMIO	32 bit	503000D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmission Occured (TO):** Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding, TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred

14.21.1.42 TX Buffer Cancellation Finished (TXBCF) — Offset 503000DCh

Type	Size	Offset	Default
MMIO	32 bit	503000DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Cancellation Finished (CF):** Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding, TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished

14.21.1.43 TX Buffer Transmission Interrupt Enable (TXBTIE) — Offset 503000E0h

Type	Size	Offset	Default
MMIO	32 bit	503000E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Transmission Interrupt Enable (TIE):** Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable

14.21.1.44 Tx Buffer Cancellation Finished Interrupt Enable (TXBCIE) — Offset 503000E4h

Type	Size	Offset	Default
MMIO	32 bit	503000E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cancellation Finished Interrupt Enable (CFIE):** Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled

14.21.1.45 TX Event FIFO Configuration (TXEFC) — Offset 503000F0h

Type	Size	Offset	Default
MMIO	32 bit	503000F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	00h RW/L	**Event FIFO Watermark (EFWM):** 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) >32= Watermark interrupt disabled
23:22	0h RO	**Reserved**
21:16	00h RW/L	**Event FIFO Size (EFS):** 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements >32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1
15:2	0000h RW/L	**Event FIFO Start Address (EFSA):** Start address of Tx Event FIFO in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.46 TX Event FIFO Status (TXEFS) — Offset 503000F4h

Type	Size	Offset	Default
MMIO	32 bit	503000F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TX Event FIFO Lost (TEFL):** This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	0h RO	**Event FIFO Full (EFF):** 0= Tx Event FIFO not full 1= Tx Event FIFO full
23:21	0h RO	**Reserved**
20:16	00h RO	**Event FIFO Put Index (EFPI):** Tx Event FIFO write index pointer, range 0 to 31.
15:13	0h RO	**Reserved**
12:8	00h RO	**Event FIFO Get Index (EFGI):** Tx Event FIFO read index pointer, range 0 to 31.
7:6	0h RO	**Reserved**
5:0	00h RO	**Event FIFO Fill Level (EFFL):** Number of elements stored in Tx Event FIFO, range 0 to 32.

14.21.1.47 TX Event FIFO Acknowledge (TXEFA) — Offset 503000F8h

Type	Size	Offset	Default
MMIO	32 bit	503000F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Event FIFO Acknowledge Index (EFAI):** After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the FIFO 0 Fill Level TXEFS.EFFL.

14.21.1.48 TT Trigger Memory Configuration (TTTMC) — Offset 50300100h

Type	Size	Offset	Default
MMIO	32 bit	50300100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW/P	**Trigger Memory Elements (TME):** b0: No Trigger Memory b1-b1000000: Number of Trigger Memory elements >b1000000: Values greater than 64 are interpreted as 64
15:2	0000h RW/P	**Trigger Memory Start Address (TMSA):** Start address of Trigger Memory in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.1.49 TT Reference Message Configuration (TTRMC) — Offset 50300104h

Type	Size	Offset	Default
MMIO	32 bit	50300104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Reference Message Payload Select (RMPS):** Ignored in case of time slaves. b0: Reference message has no additional payload b1: The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB (Level 1: bytes 2-8, Level 0,2: bytes 5-8)
30	0h RW/P	**Extended Identifier (XTD):** b0: 11-bit standard Identifier b1: 29-bit extended Identifier
29	0h RO	**Reserved**
28:0	00000000h RW/P	**Reference Identifier (RID):** Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference Identifier depending on Bit XTD. A standard Identifier has to be written to ID[28:18].

14.21.1.50 TT Operation Configuration (TTOCF) — Offset 50300108h

Type	Size	Offset	Default
MMIO	32 bit	50300108h	00010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Event Trigger Polarity (EVTP):** b0: Rising edge trigger b1: Falling edge trigger
25	0h RW/P	**Enable Clock Calibration (ECC):** b0: Automatic clock calibration in TTCAN Level 0,2 is disabled b1: Automatic clock calibration in TTCAN Level 0,2 is enabled
24	0h RW/P	**Enable Global Time Filtering (EGTF):** b0: Global time filtering in TTCAN Level 0,2 is disabled b1: Global time filtering in TTCAN Level 0,2 is enabled

Bit Range	Default & Access	Field Name (ID): Description
23:16	01h RW/P	**Application Watchdog Limit (AWL):** The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF: Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs.
15	0h RW/P	**Enable External Clock Synchronization (EECS):** If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. b0: External clock synchronization in TTCAN Level 0,2 disabled b1: External clock synchronization in TTCAN Level 0,2 enabled
14:8	00h RW/P	**Initial Reference Trigger Offset (IRTO):** 0x00-7F: Positive offset, range from 0 to 127
7:5	0h RW/P	**LD of Synchronization Deviation Limit (LDSDL):** The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2^(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7: LD of Synchronization Deviation Limit (SDL less than or equal to 32 ... 4096)
4	0h RW/P	**Time Master (TM):** b0: Time Master function disabled b1: Potential Time Master
3	0h RW/P	**Gap Enable (GEN):** b0: Strictly time-triggered operation b1: External event-synchronized time-triggered operation
2	0h RO	**Reserved**
1:0	0h RW/P	**Operation Mode (OM):** b0: Event-driven CAN communication, default b1: TTCAN level 1 b10: TTCAN level 2 b11: TTCAN level 0

14.21.1.51 TT Matrix Limits (TTMLM) — Offset 5030010Ch

Type	Size	Offset	Default
MMIO	32 bit	5030010Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RW/P	**Expected Number of Tx Triggers (ENTT):** 0x000-FFF: Expected number of Tx Triggers in one Matrix Cycle
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW/P	**Tx Enable Window (TXEW):** Length of Tx enable window, 1-16 NTU cycles
7:6	0h RW/P	**Cycle Start Synchronization (CSS):** b0: No sync pulse b1: Sync pulse at start of basic cycle b10: Sync pulse at start of matrix cycle b11: Reserved
5:0	00h RW/P	**Cycle Count Max (CCM):** 0x00: 1 Basic Cycle per Matrix Cycle 0x01: 2 Basic Cycles per Matrix Cycle 0x03: 4 Basic Cycles per Matrix Cycle 0x07: 8 Basic Cycles per Matrix Cycle 0x0F: 16 Basic Cycles per Matrix Cycle 0x1F: 32 Basic Cycles per Matrix Cycle 0x3F: 64 Basic Cycles per Matrix Cycle others: Reserved

14.21.1.52 TUR Configuration (TURCF) — Offset 50300110h

The length of the NTU is given by: NTU = CAN Clock Period X NC/DC NC is an 18-bit value. Its high part, NCH[17:16] is hard wired to 0b01. Therefore the range of NC is 0x10000...0x1FFFF. The value configured by NCL is the initial value for TURNA.NAV[15:0]. DC is set to 0x1000 by hardware reset and it may not be written to 0x0000. Level 1: NC >= 4 X DC and NTU = CAN bit time Level 0,2: NC >= 8 X DC The actual value of TUR may be changed by the clock drift compensation function of TTCAN Level 0 and Level 2 in order to adjust the nodes local view of the NTU to the time masters view of the NTU. DC will not be changed by the automatic drift compensation, TURNA.NAV may be adjusted around NC in the range of the Synchronisation Deviation Limit given by TTOCF.LDSDL. NC and DC should be programmed to the largest suitable values in order to allow the best computational accuracy for the drift compensation process.

Type	Size	Offset	Default
MMIO	32 bit	50300110h	10000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Enable Local Time (ELT):** b0: Local time is stopped, default b1: Local time is enabled **Note:** Local time is started by setting ELT. It remains active until ELT is reset or until the next hardware reset. TURCF.DC is locked when TURCF.ELT = b1. If ELT is written to b0, the readable value will stay at b1 until the new value has been synchronized into the CAN clock domain. During this time write access to the other bits of the register remains locked.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO	**Reserved**
29:16	1000h RW/P	**Denominator configuration (DC):** 0x0000: Illegal value 0x0001-3FFF: Denominator configuration
15:0	0000h RW/P	**Numerator configuration Low (NCL):** Write access to the TUR Numerator configuration Low is only possible during configuration with TURCF.ELT = b0 or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT configuration Mode, the new value takes effect when TTOST.WECS is cleared to b0. NCL is locked TTOST.WECS is b1. 0x0000-FFFF: Numerator configuration Low **Note:** If NC < 7 X DC in TTCAN Level 1, then it is required that subsequent time marks in the Trigger Memory must differ by at least 2 NTU**.**

14.21.1.53 TT Operation Control (TTOCN) — Offset 50300114h

Type	Size	Offset	Default
MMIO	32 bit	50300114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**TT Operation Control Register Locked (LCKC):** Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. b0: Write access to TTOCN enabled b1: Write access to TTOCN locked
14	0h RO	**Reserved**
13	0h RW	**External Synchronization Control (ESCN):** If enabled the M_TTCAN synchronizes its cycle time phase to an external event signalled by a rising edge at pin m_ttcan_evt b0: External synchronization disabled b1: External synchronization enabled
12	0h RW	**Next is Gap (NIG):** This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = b1) b0: No action, reset by reception of any reference message b1: Transmit next reference message with Next_is_Gap = b1
11	0h RW	**Time Mark Gap (TMG):** b0: Reset by each reference message b1: Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated
10	0h RW	**Finish Gap (FGP):** Set by the CPU, reset by each reference message b0: No reference message requested b1: Application requested start of reference message

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Gap Control Select (GCS):** b0: Gap control independent from m_ttcan_evt b1: Gap control by input pin m_ttcan_evt
8	0h RW	**Trigger Time Mark Interrupt Pulse Enable (TTIE):** External time mark events are configured by trigger memory element TMEX. A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. b0: Trigger Time Mark Interrupt output m_ttcan_tmp disabled b1: Trigger Time Mark Interrupt output m_ttcan_tmp enabled
7:6	0h RW	**Register Time Mark Compare (TMC):** b00: No Register Time Mark Interrupt generated b01: Register Time Mark Interrupt if Time Mark = cycle time b10: Register Time Mark Interrupt if Time Mark = local time b11: Register Time Mark Interrupt if Time Mark = global time. **Note:** When changing the time mark reference (cycle, local, global time), it is recommended to first write TMC = b0, then reconfigure TTTMK, and finally set TMC to the intended time reference.
5	0h RW	**Register Time Mark Interrupt Pulse Enable (RTIE):** Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one m_ttcan_clk period is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. b0: Register Time Mark Interrupt output m_ttcan_rtp disabled b1: Register Time Mark Interrupt output m_ttcan_rtp enabled
4:3	0h RW	**Stop Watch Source (SWS):** b00: Stop Watch disabled b01: Actual value of cycle time is copied to TTCPT.SWV b10: Actual value of local time is copied to TTCPT.SWV b11: Actual value of global time is copied to TTCPT.SWV
2	0h RW	**Stop Watch Polarity (SWP):** b0: Rising edge trigger b1: Falling edge trigger
1	0h RW	**External Clock Synchronization (ECS):** Writing a b1 to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle.
0	0h RW	**Set Global time (SGT):** Writing a b1 to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. 51

14.21.1.54 TT Global Time Preset (TTGTP) — Offset 50300118h

If TTOST.WGDT is set, the next reference message will be transmitted with the Master_Ref_Mark modified by the preset value and with Disc_Bit = b1, presetting the global time in all nodes simultaneously. TP is reset to 0x0000 each time a reference message with Disc_Bit = b1 becomes valid or if the node is not the current Time

Master. TP is locked while TTOST.WGTD = b1 after setting TTOCN.SGT until the reference message with Disc_Bit = b1 becomes valid or until the node is no longer the current Time Master.

Type	Size	Offset	Default
MMIO	32 bit	50300118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Cycle Time Target Phase (CTP):** CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set. 0x0000-FFFF: Defines target value of cycle time when a rising edge of m_ttcan_evt is expected
15:0	0000h RW	**Time Preset (TP):** TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF: Next Master Reference Mark = Master Reference Mark + TP 0x8000: reserved 0x8001-FFFF: Next Master Reference Mark = Master Reference Mark - (0x10000 - TP)

14.21.1.55 TT Time Mark (TTTMK) — Offset 5030011Ch

A time mark interrupt (TTIR.RTMI = b1) is generated when the time base indicated by TTOCN.TMC (cycle time, local time, or global time) has the same value as TM.

Type	Size	Offset	Default
MMIO	32 bit	5030011Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**TT Time Mark Register Locked (LCKM):** Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC 00. Reset when the registers have been synchronized into the CAN clock domain. b0: Write access to TTTMK enabled b1: Write access to TTTMK locked

Bit Range	Default & Access	Field Name (ID): Description
30:23	0h RO	**Reserved**
22:16	00h RW	**Time Mark Cycle Code (TICC):** Cycle count for which the time mark is valid. 0b000000x: valid for all cycles 0b000001c: valid every second cycle at cycle count mod2 = c 0b00001cc: valid every fourth cycle at cycle count mod4 = cc 0b0001ccc: valid every eighth cycle at cycle count mod8 = ccc 0b001cccc: valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc: valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc: valid every sixty-fourth cycle at cycle count mod64 = cccccc
15:0	0000h RW	**Time Mark (TM):** 0x0000-FFFF: Time Mark **Note:** When using byte access to register TTTMK it is recommended to first disable the time mark compare function (TTOCN.TMC = b0) to avoid compares on inconsistent register values.

14.21.1.56 TT Interrupt Register (TTIR) — Offset 50300120h

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. A flag is cleared by writing a b1 to the corresponding bit position. Writing a b0 has no effect. A hard reset will clear the register.

Type	Size	Offset	Default
MMIO	32 bit	50300120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/1C	**Configuration Error (CER):** Trigger out of order. b0: No error found in trigger list b1: Error found in trigger list
17	0h RW/1C	**Application Watchdog (AW):** b0: Application watchdog served in time b1: Application watchdog not served in time
16	0h RW/1C	**Watch Trigger (WT):** b0: No missing reference message b1: Missing reference message (Level 0: cycle time 0xFF00)
15	0h RW/1C	**Initialization Watch Trigger (IWT):** The initialization is restarted by resetting IWT. b0: No missing reference message during system startup b1: No system startup due to missing reference message
14	0h RW/1C	**Error Level Changed (ELC):** Not set when error level changed during initialization. b0: No change in error level b1: Error level changed
13	0h RW/1C	**Scheduling Error 2 (SE2):** b0: No scheduling error 2 b1: Scheduling error 2 occurred

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**Scheduling Error 1 (SE1):** b0: No scheduling error 1 b1: Scheduling error 1 occurred
11	0h RW/1C	**Tx Count Overflow (TXO):** b0: Number of Tx Trigger as expected b1: More Tx trigger than expected in one matrix cycle
10	0h RW/1C	**Tx Count Underflow (TXU):** b0: Number of Tx Trigger as expected b1: Less Tx trigger than expected in one matrix cycle
9	0h RW/1C	**Global Time Error (GTE):** Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. b0: Synchronization deviation within limit b1: Synchronization deviation exceeded limit
8	0h RW/1C	**Global Time Discontinuity (GTD):** b1: No discontinuity of global time b0: Discontinuity of global time
7	0h RW/1C	**Global Time Wrap (GTW):** b0: No global time wrap occurred b1: Global time wrap from 0xFFFF to 0x0000 occurred
6	0h RW/1C	**Stop Watch Event (SWE):** b0: No rising/falling edge at stop watch trigger pin m_ttcan_swt detected b1: Rising/falling edge at stop watch trigger pin m_ttcan_swt detected
5	0h RW/1C	**Trigger Time Mark Event Internal (TTMI):** Internal time mark events are configured by trigger memory element TMIN. Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. b0: Time mark not reached b1: Time mark reached (Level 0: cycle time TTOCF.IRTO X 0x200)
4	0h RW/1C	**Register Time Mark Interrupt (RTMI):** Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. b0: Time mark not reached b1: Time mark reached
3	0h RW/1C	**Start of Gap (SOG):** b0: No reference message seen with Next_is_Gap bit set b1: Reference message with Next_is_Gap bit set becomes valid
2	0h RW/1C	**Change of Synchronization Mode (CSM):** b0: No change in master to slave relation or schedule synchronization b1: Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset
1	0h RW/1C	**Start of Matrix Cycle (SMC):** b0: No Matrix Cycle started since bit has been reset b1: Matrix Cycle started
0	0h RW/1C	**Start of Basic Cycle (SBC):** b0: No Basic Cycle started since bit has been reset b1: Basic Cycle started

14.21.1.57 TT Interrupt Enable (TTIE) — Offset 50300124h

The settings in the TT Interrupt Enable register determine which status changes in the TT Interrupt Register will result in an interrupt.

Type	Size	Offset	Default
MMIO	32 bit	50300124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**Configuration Error Interrupt Enable (CERE):** b0: interrupt disabled b1: interrupt enabled
17	0h RW	**Application Watchdog Interrupt Enable (AWE):** b0: interrupt disabled b1: interrupt enabled
16	0h RW	**Watch Trigger Interrupt Enable (WTE):** b0: interrupt disabled b1: interrupt enabled
15	0h RW	**Initialization Watch Trigger Interrupt Enable (IWTE):** b0: interrupt disabled b1: interrupt enabled
14	0h RW	**Change Error Level Interrupt Enable (ELCE):** b0: interrupt disabled b1: interrupt enabled
13	0h RW	**Scheduling Error 2 Interrupt Enable (SE2E):** b0: interrupt disabled b1: interrupt enabled
12	0h RW	**Scheduling Error 1 Interrupt Enable (SE1E):** b0: interrupt disabled b1: interrupt enabled
11	0h RW	**Tx Count Overflow Interrupt Enable (TXOE):** b0: interrupt disabled b1: interrupt enabled
10	0h RW	**Tx Count Underflow Interrupt Enable (TXUE):** b0: interrupt disabled b1: interrupt enabled
9	0h RW	**Global Time Error Interrupt Enable (GTEE):** b0: interrupt disabled b1: interrupt enabled
8	0h RW	**Global Time Discontinuity Interrupt Enable (GTDE):** b0: interrupt disabled b1: interrupt enabled
7	0h RW	**Global Time Wrap Interrupt Enable (GTWE):** b0: interrupt disabled b1: interrupt enabled
6	0h RW	**Stop Watch Event Interrupt Enable (SWEE):** b0: interrupt disabled b1: interrupt enabled
5	0h RW	**Trigger Time Mark Event Internal Enable (TTMIE):** b0: interrupt disabled b1: interrupt enabled
4	0h RW	**Register Time Mark Interrupt Enable (RTMIE):** b0: interrupt disabled b1: interrupt enabled
3	0h RW	**Start of Gap Interrupt Enable (SOGE):** b0: interrupt disabled b1: interrupt enabled

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Change of Synchronization Mode Interrupt Enable (CSME):** b0: interrupt disabled b1: interrupt enabled
1	0h RW	**Start of Matrix Cycle Interrupt Enable (SMCE):** b0: interrupt disabled b1: interrupt enabled
0	0h RW	**Start of Basic Cycle Interrupt Enable (SBCE):** b0: interrupt disabled b1: interrupt enabled

14.21.1.58 TT Interrupt Line Select (TTILS) — Offset 50300128h

The TT Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the TT Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1. b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int1.

Type	Size	Offset	Default
MMIO	32 bit	50300128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**Configuration Error Interrupt Line (CERL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int1
17	0h RW	**Application Watchdog Interrupt Line (AWL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int2
16	0h RW	**Watch Trigger Interrupt Line (WTL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int3
15	0h RW	**Initialization Watch Trigger Interrupt Line (IWTL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int4
14	0h RW	**Change Error Level Interrupt Line (ELCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int5
13	0h RW	**Scheduling Error 2 Interrupt Line (SE2L):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int6
12	0h RW	**Scheduling Error 1 Interrupt Line (SE1L):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int7

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Tx Count Overflow Interrupt Line (TXOL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int8
10	0h RW	**Tx Count Underflow Interrupt Line (TXUL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int9
9	0h RW	**Global Time Error Interrupt Line (GTEL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int10
8	0h RW	**Global Time Discontinuity Interrupt Line (GTDL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int11
7	0h RW	**Global Time Wrap Interrupt Line (GTWL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int12
6	0h RW	**Stop Watch Event Interrupt Line (SWEL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int13
5	0h RW	**Trigger Time Mark Event Internal Line (TTMIL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int14
4	0h RW	**Register Time Mark Interrupt Line (RTMIL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int15
3	0h RW	**Start of Gap Interrupt Line (SOGL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int16
2	0h RW	**Change of Synchronization Mode Interrupt Line (CSML):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int17
1	0h RW	**Start of Matrix Cycle Interrupt Line (SMCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int18
0	0h RW	**Start of Basic Cycle Interrupt Line (SBCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int19

14.21.1.59 TT Operation Status (TTOST) — Offset 5030012Ch

Type	Size	Offset	Default
MMIO	32 bit	5030012Ch	00000080h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Schedule Phase Lock (SPL):** The Bit is valid only when external synchronization is enabled (TTOCN.ESCN = b1). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU b0: Phase outside range b1: Phase inside range
30	0h RO	**Wait for External Clock Synchronization (WECS):** b0: No external clock synchronization pending b1: Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle.
29	0h RO	**Application Watchdog Event (AWE):** The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. b0: Application Watchdog served in time b1: Failed to serve Application Watchdog in time
28	0h RO	**Wait for Event (WFE):** b0: No Gap announced, reset by a reference message with Next_is_Gap = b0 b1: Reference message with Next_is_Gap = b1 received
27	0h RO	**Gap Started Indicator (GSI):** b0: No Gap in schedule, reset by each reference message and for all time slaves b1: Gap time after Basic Cycle has started
26:24	0h RO	**Time Master Priority (TMP):** 0x0-7: Priority of actual Time Master
23	0h RO	**Gap Finished Indicator (GFI):** Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = b1, or via input pin m_ttcan_evt if TTOCN.GCS = b1. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. b0: Reset at the end of each reference message b1: Gap finished by M_TTCAN
22	0h RO	**Wait for Global Time Discontinuity (WGTD):** b0: No global time preset pending b1: Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = b1 or after it received a reference message.
21:16	0h RO	**Reserved**
15:8	00h RO	**Reference Trigger Offset (RTO):** The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = b11), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF: Actual Reference Trigger offset value

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Quality of Clock Speed (QCS):** Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to b1. b0: Local clock speed not synchronized to Time Master clock speed b1: Synchronization Deviation <= SDL
6	0h RO	**Quality of Global Time Phase (QGTP):** Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to b0. b0: Global time not valid b1: Global time in phase with Time Master
5:4	0h RO	**Synchronization State (SYS):** b00: Out of Synchronization b01: Synchronizing to TTCAN communication b10: Schedule suspended by Gap (In_Gap) b11: Synchronized to schedule (In_Schedule)
3:2	0h RO	**Master State (MS):** b00: Master_Off, no master properties relevant b01: Operating as Time Slave b10: Operating as Backup Time Master b11: Operating as current Time Master
1:0	0h RO	**Error Level (EL):** b00: Severity 0 - No Error b01: Severity 1 - Warning b10: Severity 2 - Error b11: Severity 3 - Severe Error

14.21.1.60 TUR Numerator Actual (TURNA) — Offset 50300130h

There is no drift compensation in TTCAN Level 1 (NAV = NC). In TTCAN Level 0 and Level 2, the drift between the nodes local clock and the time masters local clock is calculated. The drift is compensated when the Synchronisation Deviation (difference between NC and the calculated NAV) is not more than 2(TTOCF.LDSDL + 5). With TTOCF.LDSDL 7, this results in a maximum range for NAV of (NC - 0x1000) NAV (NC + 0x1000). From sction 2.3.59 of M_TTCAN Users Manual Revision 3.0.2

Type	Size	Offset	Default
MMIO	32 bit	50300130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:0	00000h RO	**Numerator Actual Value (NAV):** <= 0x0EFFF: Illegal value 0x0F000-20FFF: Actual numerator value >= 0x21000: Illegal value

14.21.1.61 TT Local and Global Time (TTLGT) — Offset 50300134h

Type	Size	Offset	Default
MMIO	32 bit	50300134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Global Time (GT):** Non-fractional part of the sum of the nodes local time and its local offset. 0x0000-FFFF: Global time value of TTCAN network
15:0	0000h RO	**Local Time (LT):** Non-fractional part of local time, incremented once each local NTU. 0x0000-FFFF: Local time value of TTCAN node

14.21.1.62 TT Cycle Time & Count (TTCTC) — Offset 50300138h

Type	Size	Offset	Default
MMIO	32 bit	50300138h	003F0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:16	3Fh RO	**Cycle Count (CC):** 0x00-3F Number of actual Basic Cycle in the System Matrix
15:0	0000h RO	**Cycle Time (CT):** Non-fractional part of the difference of the node's local time and Ref_Mark. 0x0000-FFFF Cycle time value of TTCAN Basic Cycle

14.21.1.63 TT Capture Time (TTCPT) — Offset 5030013Ch

Type	Size	Offset	Default
MMIO	32 bit	5030013Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Stop Watch Value (SWV):** On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is not equal to b0 and TTIR.SWE is b0, the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to b1. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF: Captured Stop Watch value
15:6	0h RO	**Reserved**
5:0	00h RO	**Cycle Count Value (CCV):** Cycle count value captured together with SWV. 0x00-3F: Captured cycle count value

14.21.1.64 TT Cycle Sync Mark (TTCSM) — Offset 50300140h

Type	Size	Offset	Default
MMIO	32 bit	50300140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RO	**Cycle Sync Mark (CSM):** The Cycle Sync Mark is measured in cycle time. It is updated when the reference message becomes valid and retains its value until the next reference message becomes valid. 0x0000-FFFF Captured cycle time

14.21.1.65 Message RAM Size (MSG_RAM_SIZE) — Offset 50300500h

Type	Size	Offset	Default
MMIO	32 bit	50300500h	00004600h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00004600h RO	**Size Bytes (SIZE_B):** Read only value of the size in bytes of the Message RAM of this dby_can instance @@jstokes3, need to set the default value where this RDL is instantiated

14.21.1.66 CTL — Offset 50300504h

Type	Size	Offset	Default
MMIO	32 bit	50300504h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**M_TTCAN Disable Error Data Modification on Read (CAN_DIS_MORD):** Set to 1 to prevent reads to ECR.CEL and PSR.LEC from resetting the CAN error data in the register.

14.21.1.67 Interrupt Control (INT_CTL) — Offset 50300508h

Type	Size	Offset	Default
MMIO	32 bit	50300508h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**PUNIT Interrupt Enable (PUNIT_INT_EN):** Enables the dby_can PUNIT interrupt output int_punit_o. Software is expected to set PUNIT_INT_EN or PRIMARY_INT_EN to b1, but not both.
0	0h RW	**Primary Interrupt Enable (PRIMARY_INT_EN):** Enables the primary interrupt output int_o. Software is expected to set PUNIT_INT_EN or PRIMARY_INT_EN to b1, but not both.

14.21.1.68 Interrupt Status (INT_STAT) — Offset 5030050Ch

Type	Size	Offset	Default
MMIO	32 bit	5030050Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Other CAN Parity Error Interrupt (OTHER_CAN_PERR_INT):** Parity error interrupt for the other CAN instance.
2	0h RO	**Other Controller Interrupt Status (OTHER_CAN_CONT_INT):** If asserted then the other instance of the M_TTCAN controller has its interrupt asserted.
1	0h RO	**This CAN Parity Error Interrupt (THIS_CAN_PERR_INT):** Parity error interrupt for this CAN instance.
0	0h RO	**This CAN Controller Interrupt Status (THIS_CAN_CONT_INT):** If asserted then this instance of the M_TTCAN controller has its interrupt asserted.

14.21.1.69 MSGRAM Address Conflict Status (MSGRAM_ADDR_CONFLICT_STAT) — Offset 50300510h

Type	Size	Offset	Default
MMIO	32 bit	50300510h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Address Conflict Occurred (ADDR_CONFLICT_OCCURED):** A flag to indicate that an address conflict has occurred. This can be used to help the debug of the CAN device driver. Note that this does not cause an interrupt.
15	0h RO	**Reserved**
14:0	0000h RO	**M_TTCAN Address Conflict Offset (CAN_ADDR_CONFLICT_OFFSET):** The M_TTCAN address that the conflict between an AHB access to the MSGRAM simultaneous to an M_TTCAN access to MSGRAM.

14.21.1.70 TTCAN TIMESTAMP CONTROL REGISTER (TIMESTAMP_CTL) — Offset 50300514h

Type	Size	Offset	Default
MMIO	32 bit	50300514h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Remote Cross Timestamp Valid (RXTSV):**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Local Cross Timestamp Valid (LXTSV):**
1	0h RW	**Capture Remote Cross Timestamp (RXTSC):**
0	0h RW	**Capture Local Cross Timestamp (LXTSC):**

14.21.1.71 TTCAN LOCAL TIMESTAMP HIGH (LOCALTIMESTAMP_HIGH) — Offset 50300518h

Type	Size	Offset	Default
MMIO	32 bit	50300518h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Local Timestamp High (LTH):**

14.21.1.72 TTCAN LOCAL TIMESTAMP LOW (LOCALTIMESTAMP_LOW) — Offset 5030051Ch

Type	Size	Offset	Default
MMIO	32 bit	5030051Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Local Timestamp Low (LTL):**

14.21.1.73 CAN Parity Error Control and Status (PAR_CTL_STAT) — Offset 50300600h

Control and Status of Parity Check Functionality

Type	Size	Offset	Default
MMIO	32 bit	50300600h	00000003h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW/1C/P	**Parity Error Occured (PERR_OCCURED):** Sticky register which asserts when a parity error has been detected on a read from the message RAM. A write of b1 clears this field to b0. If they are enabled, the int_o and int_punit_o interrupt outputs may assert when this field is set to 1. The interrupts will clear when this field is cleared. This register field can only be reset on a powergoodrst_n.
1	1h RO	**Parity Initialisation In Progress (PARITY_INIT_IN_PROG):** Immediately on coming out of a reset (hresetn asserted) the message RAM will be parity initialised with writes of b0. While this is taking place, this field will read as 1. While this PARITY_INIT_IN_PROG is 1, reads to the message RAM will be stalled until completion of parity initialisation.
0	1h RW	**Parity Enable (PARITY_EN):** 1 - Parity bit generation, checking, error reporting and error injection are enabled for dby_can. 0 - All parity functionality is disabled for dby_can. The value of this field can only be updated by software when PARITY_INIT_IN_PROG == 0.

14.21.1.74 Parity Error Offset (PAR_ERR_OFFSET) — Offset 50300604h

Stores the message RAM offset at which a parity error occured in dby_can message RAM space

Type	Size	Offset	Default
MMIO	32 bit	50300604h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/P	**Parity Error In Upper 16 bits (PAR_ERR_UPP):** Indicates a that a parity error was detected in the upper 16 bits of the word at this offset. This register field can only be reset on a powergoodrst_n.
16	0h RO/P	**Parity Error In Lower 16 bits (PAR_ERR_LOW):** Indicates a that a parity error was detected in the lower 16 bits of the word at this offset. This register field can only be reset on a powergoodrst_n.
15	0h RO	**Reserved**
14:0	0000h RO/P	**Parity Error Offset (PAR_ERR_OFFSET):** Captures the message RAM offset at which a parity error occured. A new offset can only be captured when PERR_OCCURED is b0. This offset is relative to 0x0 in dby_can memory space. This register field can only be reset on a powergoodrst_n.

14.21.1.75 Parity Error Injection Control and Status (PAR_EINJ_CTL_STAT) — Offset 50300608h

Control and status for parity error injection to the dby_can message RAM.

Type	Size	Offset	Default
MMIO	32 bit	50300608h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO	**One Time Parity Error Injection Occured (EINJ_ONE_TIME_ERR_OCCURED):** Asserts when a parity error is injected and EINJ_MODE = 0 (one time error injection). Cleared when EINJ_EN is set to b1 Once the one time parity error is injected, EINJ_EN deasserts. The intention then is that EINJ_ONE_TIME_ERR_OCCURED is the record that an error was injected.
1	0h RW	**Parity Error Injection Mode (EINJ_MODE):** b1 : Continuous error injection. All writes to the message RAM are corrupted based on the value of EINJ_MASK b0 : One time error injection. Only the first write to the address defined in EINJ_OFFSET is corrupted. After which EINJ_EN is cleared to b0 and EINJ_ONE_TIME_ERR_OCCURED is set to b1.
0	0h RW/AC	**Error Injection Enable (EINJ_EN):** 1 - Parity error injection is enabled 0 - Parity error injection is disabled Once the one time parity error is injected, EINJ_EN deasserts.

14.21.1.76 Parity Error Injection Offset (PAR_EINJ_OFFSET) — Offset 5030060Ch

Parity error injection offset in dby_can message RAM

Type	Size	Offset	Default
MMIO	32 bit	5030060Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:0	0000h RW	**Error Injection Offset (EINJ_OFFSET):** Offset at which an error will be injected, if enabled. This offset is relative to 0x0 in dby_can memory space.

14.21.1.77 Parity Error Injection Data Mask (PAR_EINJ_DATA_MASK) — Offset 50300610h

Parity error injection data mask for dby_can

Type	Size	Offset	Default
MMIO	32 bit	50300610h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Error Injection Data Mask (EINJ_DATA_MASK):** This field is XOR'd with the incoming write data in order to flip data bit/bits with respect to the value the parity bit was calculated for

14.21.1.78 Parity Error Injection Parity Mask (PAR_EINJ_PARITY_MASK) — Offset 50300614h

Parity error injection data mask for dby_can

Type	Size	Offset	Default
MMIO	32 bit	50300614h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Error Injection Parity Mask (EINJ_PARITY_MASK):** This field is XOR'd with the parity bits in order to flip data bit/bits with respect to the value the parity bit was calculated for

14.21.2 CAN_1 Registers Summary

Table 14-49. Summary of CAN_1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50310000h	4	Core Release Register (CREL)	32150323h
50310004h	4	Endian Register (ENDN)	87654321h
50310008h	4	Customer Register (CUST)	00000000h
5031000Ch	4	Fast Bit Timing and Prescaler Register (DBTP)	00000A33h
50310010h	4	Test Register (TEST)	00000000h
50310014h	4	RAM Watchdog (RWD)	00000000h
50310018h	4	CC Control Register (CCCR)	00000001h
5031001Ch	4	Bit Timing and Prescaler Register (BTP)	06000A03h
50310020h	4	Timestamp Counter Configuration (TSCC)	00000000h
50310024h	4	Timestamp Counter Value (TSCV)	00000000h
50310028h	4	Timeout Counter Configuration (TOCC)	FFFF0000h
5031002Ch	4	Timeout Counter Value (TOCV)	0000FFFFh
50310040h	4	Error Counter Register (ECR)	00000000h
50310044h	4	Protocol Status Register (PSR)	00000707h
50310048h	4	Transmitter Delay Compensation Register (TDCR)	00000000h
50310050h	4	Interrupt Register (IR)	00000000h
50310054h	4	Interrupt Enable (IE)	00000000h
50310058h	4	Interrupt Line Select (ILS)	00000000h
5031005Ch	4	Interrupt Line Enable (ILE)	00000000h
50310080h	4	Global Filter Configuration (GFC)	00000000h
50310084h	4	Standard ID Filter Configuration (SIDFC)	00000000h
50310088h	4	Extended ID Filter Configuration (XIDFC)	00000000h
50310090h	4	Extended ID AND Mask (XIDAM)	1FFFFFFFh
50310094h	4	High Priority Message Status (HPMS)	00000000h
50310098h	4	New Data 1 (NDAT1)	00000000h
5031009Ch	4	New Data 2 (NDAT2)	00000000h
503100A0h	4	RX FIFO 0 Configuration (RXF0C)	00000000h
503100A4h	4	RX FIFO 0 Status (RXF0S)	00000000h
503100A8h	4	RX FIFO 0 Acknowledge (RXF0A)	00000000h
503100ACh	4	RX Buffer Configuration (RXBC)	00000000h
503100B0h	4	RX FIFO 1 Configuration (RXF1C)	00000000h
503100B4h	4	RX FIFO 1 Status (RXF1S)	00000000h
503100B8h	4	RX FIFO 1 Acknowledge (RXF1A)	00000000h
503100BCh	4	Rx Buffer / FIFO Element Size Configuration (RXESC)	00000000h
503100C0h	4	TX Buffer Configuration (TXBC)	00000000h
503100C4h	4	TX FIFO/Queue Status (TXFQS)	00000000h
503100C8h	4	TX Buffer Element Size Configuration (TXESC)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
503100CCh	4	TX Buffer Request Pending (TXBRP)	00000000h
503100D0h	4	TX Buffer Add Request (TXBAR)	00000000h
503100D4h	4	TX Buffer Cancellation Request (TXBCR)	00000000h
503100D8h	4	TX Buffer Transmission Occured (TXBTO)	00000000h
503100DCh	4	TX Buffer Cancellation Finished (TXBCF)	00000000h
503100E0h	4	TX Buffer Transmission Interrupt Enable (TXBTIE)	00000000h
503100E4h	4	Tx Buffer Cancellation Finished Interrupt Enable (TXBCIE)	00000000h
503100F0h	4	TX Event FIFO Configuration (TXEFC)	00000000h
503100F4h	4	TX Event FIFO Status (TXEFS)	00000000h
503100F8h	4	TX Event FIFO Acknowledge (TXEFA)	00000000h
50310100h	4	TT Trigger Memory Configuration (TTTMC)	00000000h
50310104h	4	TT Reference Message Configuration (TTRMC)	00000000h
50310108h	4	TT Operation Configuration (TTOCF)	00010000h
5031010Ch	4	TT Matrix Limits (TTMLM)	00000000h
50310110h	4	TUR Configuration (TURCF)	10000000h
50310114h	4	TT Operation Control (TTOCN)	00000000h
50310118h	4	TT Global Time Preset (TTGTP)	00000000h
5031011Ch	4	TT Time Mark (TTTMK)	00000000h
50310120h	4	TT Interrupt Register (TTIR)	00000000h
50310124h	4	TT Interrupt Enable (TTIE)	00000000h
50310128h	4	TT Interrupt Line Select (TTILS)	00000000h
5031012Ch	4	TT Operation Status (TTOST)	00000080h
50310130h	4	TUR Numerator Actual (TURNA)	00000000h
50310134h	4	TT Local and Global Time (TTLGT)	00000000h
50310138h	4	TT Cycle Time & Count (TTCTC)	003F0000h
5031013Ch	4	TT Capture Time (TTCPT)	00000000h
50310140h	4	TT Cycle Sync Mark (TTCSM)	00000000h
50310500h	4	Message RAM Size (MSG_RAM_SIZE)	00004600h
50310504h	4	CTL	00000000h
50310508h	4	Interrupt Control (INT_CTL)	00000000h
5031050Ch	4	Interrupt Status (INT_STAT)	00000000h
50310510h	4	MSGRAM Address Conflict Status (MSGRAM_ADDR_CONFLICT_STAT)	00000000h
50310514h	4	TTCAN TIMESTAMP CONTROL REGISTER (TIMESTAMP_CTL)	00000000h
50310518h	4	TTCAN LOCAL TIMESTAMP HIGH (LOCALTIMESTAMP_HIGH)	00000000h
5031051Ch	4	TTCAN LOCAL TIMESTAMP LOW (LOCALTIMESTAMP_LOW)	00000000h
50310600h	4	CAN Parity Error Control and Status (PAR_CTL_STAT)	00000003h
50310604h	4	Parity Error Offset (PAR_ERR_OFFSET)	00000000h
50310608h	4	Parity Error Injection Control and Status (PAR_EINJ_CTL_STAT)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5031060Ch	4	Parity Error Injection Offset (PAR_EINJ_OFFSET)	00000000h
50310610h	4	Parity Error Injection Data Mask (PAR_EINJ_DATA_MASK)	00000000h
50310614h	4	Parity Error Injection Parity Mask (PAR_EINJ_PARITY_MASK)	00000000h

14.21.2.1 Core Release Register (CREL) — Offset 50310000h

Type	Size	Offset	Default
MMIO	32 bit	50310000h	32150323h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Core Release (REL):** One digit, BCD-coded. - @@jstokes, Need to wait for IP delivery for reset value
27:24	2h RO	**Step of Core Release (STEP):** One digit, BCD-coded. - @@jstokes, Need to wait for IP delivery for reset value
23:20	1h RO	**Sub-step of Core Release (SUBSTEP):** One digit, BCD-coded. eed to wait for IP delivery for reset value
19:16	5h RO	**Time Stamp Year (YEAR):** One digit, BCD-coded. @@jstokes, Need to wait for IP integration for reset value
15:8	03h RO	**Time Stamp Month (MON):** Two digits, BCD-coded. @@jstokes, Need to wait for IP integration for reset value
7:0	23h RO	**Time Stamp Day (DAY):** Two digits, BCD-coded. @@jstokes, Need to wait for IP integration for reset value

14.21.2.2 Endian Register (ENDN) — Offset 50310004h

Endianness Test Value

Type	Size	Offset	Default
MMIO	32 bit	50310004h	87654321h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	87654321h RO	**Endianness Test Value (ETV):** The endianness test value is 0x87654321

14.21.2.3 Customer Register (CUST) — Offset 50310008h

Address 0x08 is reserved for an optional 32 bit customer-specific register. The Customer Register is intended to hold customer-specific configuration, control, and status bits.

Type	Size	Offset	Default
MMIO	32 bit	50310008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Customer Register Field (CUST_FIELD):** Customer specific register field

14.21.2.4 Fast Bit Timing and Prescaler Register (DBTP) — Offset 5031000Ch

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 25 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 m_ttcan_cclk periods. tq = (FBRP + 1) m_ttcan_cclk period.

FTSEG1 is the sum of Prop_Seg and Phase_Seg1. FTSEG2 is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [FTSEG1 + FTSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq.

The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Note: With a CAN clock (m_ttcan_cclk) of 8 MHz, the reset value of 0x00000A33 configures the M_TTCAN for a fast bit rate of 500 kBit/s.

Note: The bit rate configured for the CAN FD data phase via FBTP must be higher or equal to the bit rate configured for the arbitration phase via BTP.

Type	Size	Offset	Default
MMIO	32 bit	5031000Ch	00000A33h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/L	**Tranceiver Delay Compensation (TDC):** 0= Transceiver Delay Compensation disabled 1= Transceiver Delay Compensation enabled
22:21	0h RO	**Reserved**
20:16	00h RW/L	**Fast Baud Rate Prescaler (FBRP):** 0x00-0x1F : The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:13	0h RO	**Reserved**
12:8	0Ah RW/L	**Fast time segment before sample point (FTSEG1):** 0x1-0xF : Valid values are 1 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7:4	3h RW/L	**Fast time segment after sample point (FTSEG2):** 0x0-0x7 : Valid values are 0 to 7. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
3:0	3h RW/L	**Fast (Re) Synchronization Jump Width (FSJW):** 0x0-0x3 : Valid values are 0 to 3. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

14.21.2.5 Test Register (TEST) — Offset 50310010h

Write access to the Test Register has to be enabled by setting bit CCCR.TEST to . All Test Register functions are set to their reset values when bit CCCR.TEST is reset.

Loop Back Mode and software control of pin can*_tx_o are hardware test modes. Programming of TX not equal to h0 may disturb the message transfer on the CAN bus.

Type	Size	Offset	Default
MMIO	32 bit	50310010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**Receive Pin (RX):** Monitors the actual value of pin can*_rx_i 0= The CAN bus is dominant (can*_rx_i = 0) 1= The CAN bus is recessive (can*_rx_i = 1)
6:5	0h RW/L	**Control of Transmit Pin (TX):** 00 Reset value, can*_tx_o controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin can*_tx_o 10 Dominant (0) level at pin can*_tx_o 11 Recessive (1) at pin m_ttcan_tx
4	0h RW/L	**Loop Back Mode (LBCK):** 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled
3	0h RO	**Check ASC Transmit Control (CAT):** Monitors level at output pin ttcan*_asct_i. 0= Output pin ttcan*_asct_i = 0 1= Output pin ttcan*_asct_i = 1
2	0h RO	**Check ASC Multiplexer Control (CAM):** Monitors level at output pin ttcan*_ascm_i. 0= Output pin ttcan*_ascm_i = 0 1= Output pin ttcan*_ascm_i = 1
1	0h RW/L	**Check ASC Transmit Control (TAT):** Controls output pin ttcan*_asct_i in test mode, ORed with the signal from the FSE 0= Level at pin ttcan*_asct_i controlled by FSE 1= Level at pin ttcan*_asct_i = 1
0	0h RW/L	**Test ASC Transmit Control (TAM):** Controls output pin ttcan*_ascm_i in test mode, ORed with the signal from the FSE 0= Level at pin ttcan*_ascm_i controlled by FSE 1= Level at pin ttcan*_ascm_i = 1

14.21.2.6 RAM Watchdog (RWD) — Offset 50310014h

The RAM Watchdog monitors the READY output of the Message RAM (m_ttcan_aeim_ready). A Message RAM access via the M_TTCANs Generic Master Interface (m_ttcan_aeim_sel active) starts the Message RAM Watchdog Counter with the value configured by RWD.WDC. The counter is reloaded with RWD.WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag IR.WDI is set. The RAM Watchdog Counter is clocked by the Host clock (m_ttcan_hclk).

Type	Size	Offset	Default
MMIO	32 bit	50310014h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Watchdog Value (WDV):** Actual Message RAM Watchdog Counter Value.
7:0	00h RW/L	**Watchdog Configuration (WDC):** Start value of the Message RAM Watchdog Counter. With the reset value of 00 the counter is disabled.

14.21.2.7 CC Control Register (CCCR) — Offset 50310018h

Type	Size	Offset	Default
MMIO	32 bit	50310018h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/L	**Non ISO Operation (NISO):** If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO11898-1 1= CAN FD frame format according to Bosch CAN FD Specification V1.0
14	0h RW/L	**Transmit Pause (TXP):** If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame. 0= Transmit pause disabled 1= Transmit pause enabled
13	0h RW/L	**Edge Filtering durint Bus Integration (EFBI):** 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/L	**Protocol Exception Handling Disable (PXHD):** 0= Protocol exception handling enabled 1= Protocol exception handling disabled
11:10	0h RO	**Reserved**
9	0h RW/L	**Bit Rate Switch Enable (BRSE):** 0 = Bit rate switching for transmission disabled 1 = Bit rate switching for transmission enabled
8	0h RW/L	**FD Operateion Enable (FDOE):** 0 = FD operation disabled 1 = FD operation enabled
7	0h RW/V/L	**Test Mode Enable (TEST):** 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
6	0h RW/L	**Disable Automatic Retransmission (DAR):** 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled
5	0h RW/V/L	**Bus Monitoring Mode (MON):** Bit MON can only be set by the Host when both CCE and INIT are set to 1. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
4	0h RW	**Clock Stop Request (CSR):** 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	0h RO	**Clock Stop Acknowledge (CSA):** 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk
2	0h RW/V/L	**Restricted Operation Mode (ASM):** Bit ASM can only be set by the Host when both CCE and INIT are set to 1. The bit can be reset by the Host at any time. 0= Normal CAN operation 1= Restricted Operation Mode active This field may be written to b1 only when CCCR.INIT==1 AND CCCR.CCE==1, but may be cleared to 0 at any time
1	0h RW/L	**Configuration Change Enable (CCE):** 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = 1)
0	1h RW	**INIT:** 0= Normal Operation 1= Initialization is started

14.21.2.8 Bit Timing and Prescaler Register (BTP) — Offset 5031001Ch

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 81 time quanta. The CAN time quantum may be programmed in the range of 1 to 1024 m_ttcan_cclk periods. tq = (BRP + 1) m_ttcan_cclk period.

TSEG1 is the sum of Prop_Seg and Phase_Seg1. TSEG2 is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [TSEG1 + TSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq. The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Type	Size	Offset	Default
MMIO	32 bit	5031001Ch	06000A03h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	03h RW/L	**Nominal (Re)Synchronization Jump Width (NSJW):** 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
24:16	000h RW/L	**Nominal Bit Rate Prescaler (BRP):** 0x000-0x1FF. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 1023. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With a CAN clock (m_ttcan_cclk) of 8 MHz, the reset value of 0x00000A33 configures the M_TTCAN for a bit rate of 500 kBit/s.
15	0h RO	**Reserved**
14:8	0Ah RW/L	**Time segment before sample point (TSEG1):** 0x01-0xFF. Valid values are 1 to 63. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7	0h RO	**Reserved**
6:0	03h RW/L	**Time segment after sample point (TSEG2):** 0x0-0x7F. Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.

14.21.2.9 Timestamp Counter Configuration (TSCC) — Offset 50310020h

Type	Size	Offset	Default
MMIO	32 bit	50310020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW/L	**Timestamp Counter Prescaler (TCP):** 0x0-0xF. Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:2	0h RO	**Reserved**
1:0	0h RW/L	**Timestamp Select (TSS):** 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as 00

14.21.2.10 Timestamp Counter Value (TSCV) — Offset 50310024h

Type	Size	Offset	Default
MMIO	32 bit	50310024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW/1C	**Timestamp Counter (TSC):** The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = 01, the Timestamp Counter is incremented in multiples of CAN bit times [116] depending on the configuration of TSCC.TCP. Awr ap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = 10, TSC reflects the external Timestamp Counter value. A write access has no impact. Note: A wrap around is a change of the Timestamp Counter value from non-zero to zero not caused by write access to TSCV.

14.21.2.11 Timeout Counter Configuration (TOCC) — Offset 50310028h

Type	Size	Offset	Default
MMIO	32 bit	50310028h	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RW/L	**Timeout Period (TOP):** Start value of the Timeout Counter (down-counter). Configures the Timeout Period.

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2:1	0h RW/L	**Timeout Select (TOS):** When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1
0	0h RW/L	**Enable Timeout Counter (ETOC):** 0= Timeout Counter disabled 1= Timeout Counter enabled

14.21.2.12 Timeout Counter Value (TOCV) — Offset 5031002Ch

Type	Size	Offset	Default
MMIO	32 bit	5031002Ch	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	FFFFh RW/1C	**Timeout Counter (TOC):** The Timeout Counter is decremented in multiples of CAN bit times [116] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS.

14.21.2.13 Error Counter Register (ECR) — Offset 50310040h

Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented. This enables monitoring of collisions between CAN frames and ASC frames.

Type	Size	Offset	Default
MMIO	32 bit	50310040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RO/C	**CAN Error Logging (CEL):** The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO.
15	0h RO	**Recieve Error Passive (RP):** 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128
14:8	00h RO	**Recieve Error Counter (REC):** Actual state of the Receive Error Counter, values between 0 and 127
7:0	00h RO	**Transmit Error Counter (TEC):** Actual state of the Transmit Error Counter, values between 0 and 255

14.21.2.14 Protocol Status Register (PSR) — Offset 50310044h

Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in FLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.

Note: The Bus_Off recovery sequence cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

Type	Size	Offset	Default
MMIO	32 bit	50310044h	00000707h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RO	**Trasmitter Delay Compensation Value (TDCV):** 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_ttcan_tx to m_ttcan_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point Valid values are 0 to 127 mtq
15	0h RO	**Reserved**
14	0h RO/C	**Protocol Exception Event (PXE):** 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred
13	0h RO/C	**Received a CAN FD Message (RFDF):** This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with EDL flag set has been received
12	0h RO/C	**BRS flag of last received CAN FD Message (RBRS):** This bit is set together with REDL, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set
11	0h RO/C	**ESI flag of last received CAN FD Message (RESI):** This bit is set together with REDL, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set
10:8	7h RO/V	**Fast Last Error Code (FLEC):** Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	0h RO	**Bus_Off Status (B0):** 0= The M_TTCAN is not Bus_Off 1= The M_TTCAN is in Bus_Off state
6	0h RO	**Warning Status (EW):** 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Error Passive (EP):** 0= The M_TTCAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_TTCAN is in the Error_Passive state
4:3	0h RO	**ACT:** Monitors the modules CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter
2:0	7h RO/V	**Last Error Code (LEC):** The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0 when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value 1), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to 7. When the LEC shows the value 7, no CAN bus event was detected since the last CPU read access to the Protocol Status Register.

14.21.2.15 Transmitter Delay Compensation Register (TDCR) — Offset 50310048h

Type	Size	Offset	Default
MMIO	32 bit	50310048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:8	00h RW	**Trasmitter Delay Compensation Offset (TDCO):** 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq.
7	0h RO	**Reserved**
6:0	00h RW	**Trasmitter Delay Compensation Filter Window Length (TDCF):** 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measure

14.21.2.16 Interrupt Register (IR) — Offset 50310050h

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position.

Writing a 0 has no effect. Ahard reset will clear the register. The configuration of IE controls whether an interrupt is generated. The configuration of ILS controls on which interrupt line an interrupt is signalled.

Type	Size	Offset	Default
MMIO	32 bit	50310050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**Access to Reserved Address (ARA):** 0 = No access to reserved address occurred 1 = Access to reserved address occurred
28	0h RW/1C	**Protocol Error in Data Phase (Data Bit Time is used) (PED):** 0= No Protocol Error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7)
27	0h RW/1C	**Protocol Error in Arbitration Phase (Nominal Bit Time is used) (PEA):** 0= No Arbitration Error in data phase 1= Arbitration error in data phase detected (PSR.DLEC != 0,7)
26	0h RW/1C	**Watchdog Interrupt (WDI):** 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY
25	0h RW/1C	**Bus_Off Status (BO):** 0= Bus_Off status unchanged 1= Bus_Off status changed
24	0h RW/1C	**Warning Status (EW):** 0= Error_Warning status unchanged 1= Error_Warning status changed
23	0h RW/1C	**Error Passive (EP):** 0= Error_Warning status unchanged 1= Error_Warning status changed
22	0h RW/1C	**Error Logging Overflow (ELO):** 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred
21	0h RW/1C	**Bit Error Uncorrected (BEU):** Message RAM bit error detected, uncorrected. Controlled by input signal m_ttcan_aeim_berr[1] generated by an optional external parity / ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to 1. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected (e.g. parity logic)
20	0h RW/1C	**Bit Error Corrected (BEC):** Message RAM bit error detected and corrected. Controlled by input signal m_ttcan_aeim_berr[0] generated by an optional external parity / ECC logic attached to the Message RAM. 0= No bit error detected when reading from Message RAM 1= Bit error detected and corrected (e.g. ECC)

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C	**Message Stored to Dedicated RX Buffer (DRX):** The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer
18	0h RW/1C	**Timeout Occured (TOO):** 0= No timeout 1= Timeout reached
17	0h RW/1C	**Message RAM Access Failure (MRAF):** The flag is set, when the Rx Handler * has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. * was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred
16	0h RW/1C	**Timestamp Wraparound (TSW):** 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around
15	0h RW/1C	**TX Event FIFO Element Lost (TEFL):** 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	0h RW/1C	**TX Event FIFO Full (TEFF):** 0= Tx Event FIFO not full 1= Tx Event FIFO full
13	0h RW/1C	**TX Event FIFO Watermark Reached (TEFW):** 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark
12	0h RW/1C	**TX Event FIFO New Entry (TEFN):** 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element
11	0h RW/1C	**TX FIFO Empty (TFE):** 0= Tx FIFO non-empty 1= Tx FIFO empty
10	0h RW/1C	**Transmission Cancellation Finished (TCF):** 0= No transmission cancellation finished 1= Transmission cancellation finished
9	0h RW/1C	**Transmission Completed (TC):** 0= No transmission completed 1= Transmission completed
8	0h RW/1C	**High Priority Message (HPM):** 0= No high priority message received 1= High priority message received

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**RX FIFO 1 Message Lost (RF1L):** 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	0h RW/1C	**RX FIFO 1 Full (RF1F):** 0= Rx FIFO 1 not full 1= Rx FIFO 1 full
5	0h RW/1C	**RX FIFO 1 Watermark Reached (RF1W):** 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark
4	0h RW/1C	**RX FIFO 1 New Message (RF1N):** 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1
3	0h RW/1C	**RX FIFO 0 Message Lost (RF0L):** 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	0h RW/1C	**RX FIFO 0 Full (RF0F):** 0= Rx FIFO 0 not full 1= Rx FIFO 0 full
1	0h RW/1C	**RX FIFO 0 Watermark Reached (RF0W):** 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark
0	0h RW/1C	**RX FIFO 0 New Message (RF0N):** 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0

14.21.2.17 Interrupt Enable (IE) — Offset 50310054h

The settings in the Interrupt Enable register determine which status changes in the Interrupt Register will be signalled on an interrupt line.

0= Interrupt disabled

1= Interrupt enabled

Type	Size	Offset	Default
MMIO	32 bit	50310054h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Access to Reserved Address Enable (ARAE):** 0 = No access to reserved address Disabled 1 = Access to reserved address Enabled
28	0h RW	**Protocol Error in Data Phase Enable (PEDE):** 0= Protocol Error in data phase Disabled 1= Protocol error in data phase Enabled
27	0h RW	**Protocol Error in Arbitration Phase Enable (PEAE):** 0= Arbitration Error in data phase Disabled 1= Arbitration error in data phase Enabled
26	0h RW	**Watchdog Interrupt Interrupt Enable (WDIE):**
25	0h RW	**Bus_Off Status Interrupt Enable (BOE):**
24	0h RW	**Warning Status Interrupt Enable (EWE):**
23	0h RW	**Error Passive Interrupt Enable (EPE):**
22	0h RW	**Error Logging Overflow Interrupt Enable (ELOE):**
21	0h RW	**Bit Error Uncorrected Interrupt Enable (BEUE):**
20	0h RW	**Bit Error Corrected Interrupt Enable (BECE):**
19	0h RW	**Message Stored to Dedicated RX Buffer Interrupt Enable (DRXE):**
18	0h RW	**Timeout Occured Interrupt Enable (TOOE):**
17	0h RW	**Message RAM Access Failure Interrupt Enable (MRAFE):**
16	0h RW	**Timestamp Wraparound Interrupt Enable (TSWE):**
15	0h RW	**TX Event FIFO Element Lost Interrupt Enable (TEFLE):**
14	0h RW	**TX Event FIFO Full Interrupt Enable (TEFFE):**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**TX Event FIFO Watermark Reached Interrupt Enable (TEFWE):**
12	0h RW	**TX Event FIFO New Entry Interrupt Enable (TEFNE):**
11	0h RW	**TX FIFO Empty Interrupt Enable (TFEE):**
10	0h RW	**Transmission Cancellation Finished Interrupt Enable (TCFE):**
9	0h RW	**Transmission Completed Interrupt Enable (TCE):**
8	0h RW	**High Priority Message Interrupt Enable (HPME):**
7	0h RW	**RX FIFO 1 Message Lost Interrupt Enable (RF1LE):**
6	0h RW	**RX FIFO 1 Full Interrupt Enable (RF1FE):**
5	0h RW	**RX FIFO 1 Watermark Reached Interrupt Enable (RF1WE):**
4	0h RW	**RX FIFO 1 New Message Interrupt Enable (RF1NE):**
3	0h RW	**RX FIFO 0 Message Lost Interrupt Enable (RF0LE):**
2	0h RW	**RX FIFO 0 Full Interrupt Enable (RF0FE):**
1	0h RW	**RX FIFO 0 Watermark Reached Interrupt Enable (RF0WE):**
0	0h RW	**RX FIFO 0 New Message Interrupt Enable (RF0NE):**

14.21.2.18 Interrupt Line Select (ILS) — Offset 50310058h

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

0= Interrupt assigned to interrupt line m_ttcan_int0

1= Interrupt assigned to interrupt line m_ttcan_int1

Type	Size	Offset	Default
MMIO	32 bit	50310058h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Access to Reserved Address Interrupt Line (ARAL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
28	0h RW	**Protocol Error in Data Phase Interrupt Line (PEDL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
27	0h RW	**Protocol Error in Arbitration Phase Interrupt Line (PEAL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
26	0h RW	**Watchdog Interrupt Interrupt Line (WDIL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
25	0h RW	**Bus_Off Status Interrupt Line (BOL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
24	0h RW	**Warning Status Interrupt Line (EWL):** 0= Interrupt assigned to interrupt line m_ttcan_int0 1= Interrupt assigned to interrupt line m_ttcan_int1
23	0h RW	**Error Passive Interrupt Line (EPL):**
22	0h RW	**Error Logging Overflow Interrupt Line (ELOL):**
21	0h RW	**Bit Error Uncorrected Interrupt Line (BEUL):**
20	0h RW	**Bit Error Corrected Interrupt Line (BECL):**
19	0h RW	**Message Stored to Dedicated RX Buffer Interrupt Line (DRXL):**
18	0h RW	**Timeout Occured Interrupt Line (TOOL):**
17	0h RW	**Message RAM Access Failure Interrupt Line (MRAFL):**
16	0h RW	**Timestamp Wraparound Interrupt Line (TSWL):**
15	0h RW	**TX Event FIFO Element Lost Interrupt Line (TEFLL):**

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**TX Event FIFO Full Interrupt Line (TEFFL):**
13	0h RW	**TX Event FIFO Watermark Reached Interrupt Line (TEFWL):**
12	0h RW	**TX Event FIFO New Entry Interrupt Line (TEFNL):**
11	0h RW	**TX FIFO Empty Interrupt Line (TFEL):**
10	0h RW	**Transmission Cancellation Finished Interrupt Line (TCFL):**
9	0h RW	**Transmission Completed Interrupt Line (TCL):**
8	0h RW	**High Priority Message Interrupt Line (HPML):**
7	0h RW	**RX FIFO 1 Message Lost Interrupt Line (RF1LL):**
6	0h RW	**RX FIFO 1 Full Interrupt Line (RF1FL):**
5	0h RW	**RX FIFO 1 Watermark Reached Interrupt Line (RF1WL):**
4	0h RW	**RX FIFO 1 New Message Interrupt Line (RF1NL):**
3	0h RW	**RX FIFO 0 Message Lost Interrupt Line (RF0LL):**
2	0h RW	**RX FIFO 0 Full Interrupt Line (RF0FL):**
1	0h RW	**RX FIFO 0 Watermark Reached Interrupt Line (RF0WL):**
0	0h RW	**RX FIFO 0 New Message Interrupt Line (RF0NL):**

14.21.2.19 Interrupt Line Enable (ILE) — Offset 5031005Ch

Each of the two interrupt lines to the CPU can be enabled / disabled separately by programming bits EINT0 and EINT1.

Type	Size	Offset	Default
MMIO	32 bit	5031005Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Enable Interrupt Line 1 (EINT1):** 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled
0	0h RW	**Enable Interrupt Line 0 (EINT0):** 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled

14.21.2.20 Global Filter Configuration (GFC) — Offset 50310080h

Global settings for Message ID filtering.

Type	Size	Offset	Default
MMIO	32 bit	50310080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RW/L	**Accept Non-matching Frames Standard (ANFS):** Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW/L	**Accept Non-matching Frames Extended (ANFE):** Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject
1	0h RW/L	**Reject Remote Frames Standard (RRFS):** 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs
0	0h RW/L	**Reject Remote Frames Extended (RRFE):** 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs

14.21.2.21 Standard ID Filter Configuration (SIDFC) — Offset 50310084h

Settings for 11-bit standard Message ID filtering.

Type	Size	Offset	Default
MMIO	32 bit	50310084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW/L	**List Size Standard (LSS):** 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements >128= Values greater than 128 are interpreted as 128
15:2	0000h RW/L	**Filter List Standard Start Address (FLSSA):** Start address of standard Message ID filter list (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.22 Extended ID Filter Configuration (XIDFC) — Offset 50310088h

Settings for 29-bit extended Message ID filtering.

Type	Size	Offset	Default
MMIO	32 bit	50310088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW/L	**List Size Extended (LSE):** 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements >64= Values greater than 64 are interpreted as 64
15:2	0000h RW/L	**Filter List Extended Start Address (FLESA):** Start address of extended Message ID filter list (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.23 Extended ID AND Mask (XIDAM) — Offset 50310090h

Type	Size	Offset	Default
MMIO	32 bit	50310090h	1FFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	1FFFFFFFh RW/L	**Extended ID Mask (EIDM):** For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

14.21.2.24 High Priority Message Status (HPMS) — Offset 50310094h

This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Type	Size	Offset	Default
MMIO	32 bit	50310094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**Filter List (FLST):** Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List
14:8	00h RO	**Filter Index (FIDX):** Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7:6	0h RO	**Message Storage Indicator (MSI):** 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1
5:0	00h RO	**Buffer Index (BIDX):** Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = 1.

14.21.2.25 New Data 1 (NDAT1) — Offset 50310098h

Type	Size	Offset	Default
MMIO	32 bit	50310098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**New Data (ND):** The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hardreset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message

14.21.2.26 New Data 2 (NDAT2) — Offset 5031009Ch

Type	Size	Offset	Default
MMIO	32 bit	5031009Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/1C	**New Data (ND):** The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. Aflag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message

14.21.2.27 RX FIFO 0 Configuration (RXF0C) — Offset 503100A0h

Type	Size	Offset	Default
MMIO	32 bit	503100A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**FIFO 0 Operation Mode (F0OM):** FIFO 0 can be operated in blocking or in overwrite mode. 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode
30:24	00h RW/L	**RX FIFO 0 Watermark (F0WM):** 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) >64= Watermark interrupt disabled
23	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
22:16	00h RW/L	**RX FIFO 0 Size (F0S):** 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements >64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1
15:2	0000h RW/L	**RX FIFO 0 Start Address (F0SA):** Start address of Rx FIFO 0 in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.28 RX FIFO 0 Status (RXF0S) — Offset 503100A4h

Type	Size	Offset	Default
MMIO	32 bit	503100A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**RX FIFO 0 Message Lost (RF0L):** This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Note: Overwriting the oldest message when RXF0C.F0OM = 1 will not set this flag.
24	0h RO	**RX FIFO 0 Full (F0F):** 0= Rx FIFO 0 not full 1= Rx FIFO 0 full
23:22	0h RO	**Reserved**
21:16	00h RO	**RX FIFO 0 Put Index (F0PI):** Rx FIFO 0 write index pointer, range 0 to 63.
15:14	0h RO	**Reserved**
13:8	00h RO	**RX FIFO 0 Get Index (F0GI):** Rx FIFO 0 read index pointer, range 0 to 63.
7	0h RO	**Reserved**
6:0	00h RO	**RX FIFO 0 Fill Level (F0FL):** Number of elements stored in Rx FIFO 0, range 0 to 64.

14.21.2.29 RX FIFO 0 Acknowledge (RXF0A) — Offset 503100A8h

Type	Size	Offset	Default
MMIO	32 bit	503100A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RX FIFO 0 Acknowledge Index (F0AI):** After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

14.21.2.30 RX Buffer Configuration (RXBC) — Offset 503100ACh

Type	Size	Offset	Default
MMIO	32 bit	503100ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:2	0000h RW/L	**RX Buffer Start Address (RBSA):** Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C.
1:0	0h RO	**Reserved**

14.21.2.31 RX FIFO 1 Configuration (RXF1C) — Offset 503100B0h

Type	Size	Offset	Default
MMIO	32 bit	503100B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**FIFO 1 Operation Mode (F1OM):** FIFO 1 can be operated in blocking or in overwrite mode . 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode
30:24	00h RW/L	**RX FIFO 1 Watermark (F1WM):** 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) >64= Watermark interrupt disabled
23	0h RO	**Reserved**
22:16	00h RW/L	**RX FIFO 1 Size (F1S):** 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements >64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S-1
15:2	0000h RW/L	**RX FIFO 1 Start Address (F1SA):** Start address of Rx FIFO 1 in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.32 RX FIFO 1 Status (RXF1S) — Offset 503100B4h

Type	Size	Offset	Default
MMIO	32 bit	503100B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**RX FIFO 1 Message Lost (RF1L):** This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Note: Overwriting the oldest message when RXF1C.F1OM = 1 will not set this flag.
24	0h RO	**RX FIFO 1 Full (F1F):** 0= Rx FIFO 1 not full 1= Rx FIFO 1 full
23:22	0h RO	**Reserved**
21:16	00h RO	**RX FIFO 1 Put Index (F1PI):** Rx FIFO 1 write index pointer, range 0 to 63.
15:14	0h RO	**Reserved**
13:8	00h RO	**RX FIFO 1 Get Index (F1GI):** Rx FIFO 1 read index pointer, range 0 to 63.
7	0h RO	**Reserved**
6:0	00h RO	**RX FIFO 1 Fill Level (F1FL):** Number of elements stored in Rx FIFO 1, range 0 to 64.

14.21.2.33 RX FIFO 1 Acknowledge (RXF1A) — Offset 503100B8h

Type	Size	Offset	Default
MMIO	32 bit	503100B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:0	00h RW	**RX FIFO 1 Acknowledge Index (F1AI):** After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

14.21.2.34 Rx Buffer / FIFO Element Size Configuration (RXESC) — Offset 503100BCh

Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Note: In case the data field size of an acceptedCANframe exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frames data field is ignored.

Type	Size	Offset	Default
MMIO	32 bit	503100BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10:8	0h RW/L	**RX Buffer Data Field Size (RBDS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field
7	0h RO	**Reserved**
6:4	0h RW/L	**RX FIFO 1 Data Field Size (F1DS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field
3	0h RO	**Reserved**
2:0	0h RW/L	**RX FIFO 0 Data Field Size (F0DS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field

14.21.2.35 TX Buffer Configuration (TXBC) — Offset 503100C0h

Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

Type	Size	Offset	Default
MMIO	32 bit	503100C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW/L	**TX FIFO/Queue Mode (TFQM):** 0= Tx FIFO operation 1= Tx Queue operation
29:24	00h RW/L	**Transmit FIFO/Queue Size (TFQS):** 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue >32= Values greater than 32 are interpreted as 32
23:22	0h RO	**Reserved**
21:16	00h RW/L	**Number of Dedicated Transmit Buffers (NDTB):** 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers >32= Values greater than 32 are interpreted as 32
15:2	0000h RW/L	**TX Buffers Start Address (TBSA):** Start address of Tx Buffers section in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.36 TX FIFO/Queue Status (TXFQS) — Offset 503100C4h

The Tx FIFO/Queue status is related to the pending Tx requests listed in register TXBRP. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (TXBRP not yet

updated).

Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers.

Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.

Type	Size	Offset	Default
MMIO	32 bit	503100C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**TX FIFO/Queue Full (TFQF):** 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full
20:16	00h RO	**TX FIFO/Queue Put Index (TFQPI):** Tx FIFO/Queue write index pointer, range 0 to 31.
15:13	0h RO	**Reserved**
12:8	00h RO	**TX FIFO Get Index (TFGI):** Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1).
7:6	0h RO	**Reserved**
5:0	00h RO	**TX FIFO Free Level (TFFL):** Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1)

14.21.2.37 TX Buffer Element Size Configuration (TXESC) — Offset 503100C8h

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Type	Size	Offset	Default
MMIO	32 bit	503100C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2:0	0h RW/L	**TX Buffer Data Field Size (TBDS):** 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as 0xCC (padding bytes).

14.21.2.38 TX Buffer Request Pending (TXBRP) — Offset 503100CCh

Type	Size	Offset	Default
MMIO	32 bit	503100CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmission Request Pending (TRP):** Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). Acancellation request resets the corresponding transmission request pending bit of register. TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signalled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission. In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding TXBRP bit is reset.

14.21.2.39 TX Buffer Add Request (TXBAR) — Offset 503100D0h

Type	Size	Offset	Default
MMIO	32 bit	503100D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Add Request (AR):** Each Tx Buffer has its own Add Request bit. Writing a 1 will set the corresponding Add Request bit; writing a 0 has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored.

14.21.2.40 TX Buffer Cancellation Request (TXBCR) — Offset 503100D4h

Type	Size	Offset	Default
MMIO	32 bit	503100D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cancellation Request (CR):** Each Tx Buffer has its own Cancellation Request bit. Writing a 1 will set the corresponding, Cancellation Request bit; writing a 0 has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending

14.21.2.41 TX Buffer Transmission Occured (TXBTO) — Offset 503100D8h

Type	Size	Offset	Default
MMIO	32 bit	503100D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Transmission Occured (TO):** Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred

14.21.2.42 TX Buffer Cancellation Finished (TXBCF) — Offset 503100DCh

Type	Size	Offset	Default
MMIO	32 bit	503100DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Cancellation Finished (CF):** Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished

14.21.2.43 TX Buffer Transmission Interrupt Enable (TXBTIE) — Offset 503100E0h

Type	Size	Offset	Default
MMIO	32 bit	503100E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Transmission Interrupt Enable (TIE):** Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable

14.21.2.44 Tx Buffer Cancellation Finished Interrupt Enable (TXBCIE) — Offset 503100E4h

Type	Size	Offset	Default
MMIO	32 bit	503100E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Cancellation Finished Interrupt Enable (CFIE):** Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled

14.21.2.45 TX Event FIFO Configuration (TXEFC) — Offset 503100F0h

Type	Size	Offset	Default
MMIO	32 bit	503100F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	00h RW/L	**Event FIFO Watermark (EFWM):** 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) >32= Watermark interrupt disabled
23:22	0h RO	**Reserved**
21:16	00h RW/L	**Event FIFO Size (EFS):** 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements >32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1
15:2	0000h RW/L	**Event FIFO Start Address (EFSA):** Start address of Tx Event FIFO in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.46 TX Event FIFO Status (TXEFS) — Offset 503100F4h

Type	Size	Offset	Default
MMIO	32 bit	503100F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**TX Event FIFO Lost (TEFL):** This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	0h RO	**Event FIFO Full (EFF):** 0= Tx Event FIFO not full 1= Tx Event FIFO full
23:21	0h RO	**Reserved**
20:16	00h RO	**Event FIFO Put Index (EFPI):** Tx Event FIFO write index pointer, range 0 to 31.
15:13	0h RO	**Reserved**
12:8	00h RO	**Event FIFO Get Index (EFGI):** Tx Event FIFO read index pointer, range 0 to 31.
7:6	0h RO	**Reserved**
5:0	00h RO	**Event FIFO Fill Level (EFFL):** Number of elements stored in Tx Event FIFO, range 0 to 32.

14.21.2.47 TX Event FIFO Acknowledge (TXEFA) — Offset 503100F8h

Type	Size	Offset	Default
MMIO	32 bit	503100F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Event FIFO Acknowledge Index (EFAI):** After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the FIFO 0 Fill Level TXEFS.EFFL.

14.21.2.48 TT Trigger Memory Configuration (TTTMC) — Offset 50310100h

Type	Size	Offset	Default
MMIO	32 bit	50310100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:16	00h RW/P	**Trigger Memory Elements (TME):** b0: No Trigger Memory b1-b1000000: Number of Trigger Memory elements >b1000000: Values greater than 64 are interpreted as 64
15:2	0000h RW/P	**Trigger Memory Start Address (TMSA):** Start address of Trigger Memory in Message RAM (32-bit word address).
1:0	0h RO	**Reserved**

14.21.2.49 TT Reference Message Configuration (TTRMC) — Offset 50310104h

Type	Size	Offset	Default
MMIO	32 bit	50310104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Reference Message Payload Select (RMPS):** Ignored in case of time slaves. b0: Reference message has no additional payload b1: The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB (Level 1: bytes 2-8, Level 0,2: bytes 5-8)
30	0h RW/P	**Extended Identifier (XTD):** b0: 11-bit standard Identifier b1: 29-bit extended Identifier
29	0h RO	**Reserved**
28:0	00000000h RW/P	**Reference Identifier (RID):** Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference Identifier depending on Bit XTD. A standard Identifier has to be written to ID[28:18].

14.21.2.50 TT Operation Configuration (TTOCF) — Offset 50310108h

Type	Size	Offset	Default
MMIO	32 bit	50310108h	00010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW/P	**Event Trigger Polarity (EVTP):** b0: Rising edge trigger b1: Falling edge trigger
25	0h RW/P	**Enable Clock Calibration (ECC):** b0: Automatic clock calibration in TTCAN Level 0,2 is disabled b1: Automatic clock calibration in TTCAN Level 0,2 is enabled
24	0h RW/P	**Enable Global Time Filtering (EGTF):** b0: Global time filtering in TTCAN Level 0,2 is disabled b1: Global time filtering in TTCAN Level 0,2 is enabled

Bit Range	Default & Access	Field Name (ID): Description
23:16	01h RW/P	**Application Watchdog Limit (AWL):** The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF: Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs.
15	0h RW/P	**Enable External Clock Synchronization (EECS):** If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. b0: External clock synchronization in TTCAN Level 0,2 disabled b1: External clock synchronization in TTCAN Level 0,2 enabled
14:8	00h RW/P	**Initial Reference Trigger Offset (IRTO):** 0x00-7F: Positive offset, range from 0 to 127
7:5	0h RW/P	**LD of Synchronization Deviation Limit (LDSDL):** The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2^(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7: LD of Synchronization Deviation Limit (SDL less than or equal to 32 ... 4096)
4	0h RW/P	**Time Master (TM):** b0: Time Master function disabled b1: Potential Time Master
3	0h RW/P	**Gap Enable (GEN):** b0: Strictly time-triggered operation b1: External event-synchronized time-triggered operation
2	0h RO	**Reserved**
1:0	0h RW/P	**Operation Mode (OM):** b0: Event-driven CAN communication, default b1: TTCAN level 1 b10: TTCAN level 2 b11: TTCAN level 0

14.21.2.51 TT Matrix Limits (TTMLM) — Offset 5031010Ch

Type	Size	Offset	Default
MMIO	32 bit	5031010Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RW/P	**Expected Number of Tx Triggers (ENTT):** 0x000-FFF: Expected number of Tx Triggers in one Matrix Cycle
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW/P	**Tx Enable Window (TXEW):** Length of Tx enable window, 1-16 NTU cycles
7:6	0h RW/P	**Cycle Start Synchronization (CSS):** b0: No sync pulse b1: Sync pulse at start of basic cycle b10: Sync pulse at start of matrix cycle b11: Reserved
5:0	00h RW/P	**Cycle Count Max (CCM):** 0x00: 1 Basic Cycle per Matrix Cycle 0x01: 2 Basic Cycles per Matrix Cycle 0x03: 4 Basic Cycles per Matrix Cycle 0x07: 8 Basic Cycles per Matrix Cycle 0x0F: 16 Basic Cycles per Matrix Cycle 0x1F: 32 Basic Cycles per Matrix Cycle 0x3F: 64 Basic Cycles per Matrix Cycle others: Reserved

14.21.2.52 TUR Configuration (TURCF) — Offset 50310110h

The length of the NTU is given by: NTU = CAN Clock Period X NC/DC NC is an 18-bit value. Its high part, NCH[17:16] is hard wired to 0b01. Therefore the range of NC is 0x10000...0x1FFFF. The value configured by NCL is the initial value for TURNA.NAV[15:0]. DC is set to 0x1000 by hardware reset and it may not be written to 0x0000. Level 1: NC >= 4 X DC and NTU = CAN bit time Level 0,2: NC >= 8 X DC The actual value of TUR may be changed by the clock drift compensation function of TTCAN Level 0 and Level 2 in order to adjust the nodes local view of the NTU to the time masters view of the NTU. DC will not be changed by the automatic drift compensation, TURNA.NAV may be adjusted around NC in the range of the Synchronisation Deviation Limit given by TTOCF.LDSDL. NC and DC should be programmed to the largest suitable values in order to allow the best computational accuracy for the drift compensation process.

Type	Size	Offset	Default
MMIO	32 bit	50310110h	10000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Enable Local Time (ELT):** b0: Local time is stopped, default b1: Local time is enabled **Note:** Local time is started by setting ELT. It remains active until ELT is reset or until the next hardware reset. TURCF.DC is locked when TURCF.ELT = b1. If ELT is written to b0, the readable value will stay at b1 until the new value has been synchronized into the CAN clock domain. During this time write access to the other bits of the register remains locked.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO	**Reserved**
29:16	1000h RW/P	**Denominator configuration (DC):** 0x0000: Illegal value 0x0001-3FFF: Denominator configuration
15:0	0000h RW/P	**Numerator configuration Low (NCL):** Write access to the TUR Numerator configuration Low is only possible during configuration with TURCF.ELT = b0 or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT configuration Mode, the new value takes effect when TTOST.WECS is cleared to b0. NCL is locked TTOST.WECS is b1. 0x0000-FFFF: Numerator configuration Low **Note:** If NC < 7 X DC in TTCAN Level 1, then it is required that subsequent time marks in the Trigger Memory must differ by at least 2 NTU.

14.21.2.53 TT Operation Control (TTOCN) — Offset 50310114h

Type	Size	Offset	Default
MMIO	32 bit	50310114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**TT Operation Control Register Locked (LCKC):** Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. b0: Write access to TTOCN enabled b1: Write access to TTOCN locked
14	0h RO	**Reserved**
13	0h RW	**External Synchronization Control (ESCN):** If enabled the M_TTCAN synchronizes its cycle time phase to an external event signalled by a rising edge at pin m_ttcan_evt. b0: External synchronization disabled b1: External synchronization enabled
12	0h RW	**Next is Gap (NIG):** This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = b1) b0: No action, reset by reception of any reference message b1: Transmit next reference message with Next_is_Gap = b1
11	0h RW	**Time Mark Gap (TMG):** b0: Reset by each reference message b1: Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated
10	0h RW	**Finish Gap (FGP):** Set by the CPU, reset by each reference message b0: No reference message requested b1: Application requested start of reference message

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Gap Control Select (GCS):** b0: Gap control independent from m_ttcan_evt b1: Gap control by input pin m_ttcan_evt
8	0h RW	**Trigger Time Mark Interrupt Pulse Enable (TTIE):** External time mark events are configured by trigger memory element TMEX. A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. b0: Trigger Time Mark Interrupt output m_ttcan_tmp disabled b1: Trigger Time Mark Interrupt output m_ttcan_tmp enabled
7:6	0h RW	**Register Time Mark Compare (TMC):** b00: No Register Time Mark Interrupt generated b01: Register Time Mark Interrupt if Time Mark = cycle time b10: Register Time Mark Interrupt if Time Mark = local time b11: Register Time Mark Interrupt if Time Mark = global time **Note:** When changing the time mark reference (cycle, local, global time), it is recommended to first write TMC = b0, then reconfigure TTTMK, and finally set TMC to the intended time reference.
5	0h RW	**Register Time Mark Interrupt Pulse Enable (RTIE):** Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one m_ttcan_clk period is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. b0: Register Time Mark Interrupt output m_ttcan_rtp disabled b1: Register Time Mark Interrupt output m_ttcan_rtp enabled
4:3	0h RW	**Stop Watch Source (SWS):** b00: Stop Watch disabled b01: Actual value of cycle time is copied to TTCPT.SWV b10: Actual value of local time is copied to TTCPT.SWV b11: Actual value of global time is copied to TTCPT.SWV
2	0h RW	**Stop Watch Polarity (SWP):** b0: Rising edge trigger b1: Falling edge trigger
1	0h RW	**External Clock Synchronization (ECS):** Writing a b1 to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle.
0	0h RW	**Set Global time (SGT):** Writing a b1 to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. 51

14.21.2.54 TT Global Time Preset (TTGTP) — Offset 50310118h

If TTOST.WGDT is set, the next reference message will be transmitted with the Master_Ref_Mark modified by the preset value and with Disc_Bit = b1, presetting the global time in all nodes simultaneously. TP is reset to 0x0000 each time a reference message with Disc_Bit = b1 becomes valid or if the node is not the current Time

Master. TP is locked while TTOST.WGTD = b1 after setting TTOCN.SGT until the reference message with Disc_Bit = b1 becomes valid or until the node is no longer the current Time Master.

Type	Size	Offset	Default
MMIO	32 bit	50310118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Cycle Time Target Phase (CTP):** CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set. 0x0000-FFFF: Defines target value of cycle time when a rising edge of m_ttcan_evt is expected
15:0	0000h RW	**Time Preset (TP):** TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF: Next Master Reference Mark = Master Reference Mark + TP 0x8000: reserved 0x8001-FFFF: Next Master Reference Mark = Master Reference Mark - (0x10000 - TP)

14.21.2.55 TT Time Mark (TTTMK) — Offset 5031011Ch

A time mark interrupt (TTIR.RTMI = b1) is generated when the time base indicated by TTOCN.TMC (cycle time, local time, or global time) has the same value as TM.

Type	Size	Offset	Default
MMIO	32 bit	5031011Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**TT Time Mark Register Locked (LCKM):** Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC 00. Reset when the registers have been synchronized into the CAN clock domain. b0: Write access to TTTMK enabled b1: Write access to TTTMK locked

Bit Range	Default & Access	Field Name (ID): Description
30:23	0h RO	**Reserved**
22:16	00h RW	**Time Mark Cycle Code (TICC):** Cycle count for which the time mark is valid. 0b000000x: valid for all cycles 0b000001c: valid every second cycle at cycle count mod2 = c 0b00001cc: valid every fourth cycle at cycle count mod4 = cc 0b0001ccc: valid every eighth cycle at cycle count mod8 = ccc 0b001cccc: valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc: valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc: valid every sixty-fourth cycle at cycle count mod64 = cccccc
15:0	0000h RW	**Time Mark (TM):** 0x0000-FFFF: Time Mark **Note:** When using byte access to register TTTMK it is recommended to first disable the time mark compare function (TTOCN.TMC = b0) to avoid compares on inconsistent register values.

14.21.2.56 TT Interrupt Register (TTIR) — Offset 50310120h

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. A flag is cleared by writing a b1 to the corresponding bit position. Writing a b0 has no effect. A hard reset will clear the register.

Type	Size	Offset	Default
MMIO	32 bit	50310120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/1C	**Configuration Error (CER):** Trigger out of order. b0: No error found in trigger list b1: Error found in trigger list
17	0h RW/1C	**Application Watchdog (AW):** b0: Application watchdog served in time b1: Application watchdog not served in time
16	0h RW/1C	**Watch Trigger (WT):** b0: No missing reference message b1: Missing reference message (Level 0: cycle time 0xFF00)
15	0h RW/1C	**Initialization Watch Trigger (IWT):** The initialization is restarted by resetting IWT. b0: No missing reference message during system startup b1: No system startup due to missing reference message
14	0h RW/1C	**Error Level Changed (ELC):** Not set when error level changed during initialization. b0: No change in error level b1: Error level changed
13	0h RW/1C	**Scheduling Error 2 (SE2):** b0: No scheduling error 2 b1: Scheduling error 2 occurred

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**Scheduling Error 1 (SE1):** b0: No scheduling error 1 b1: Scheduling error 1 occurred
11	0h RW/1C	**Tx Count Overflow (TXO):** b0: Number of Tx Trigger as expected b1: More Tx trigger than expected in one matrix cycle
10	0h RW/1C	**Tx Count Underflow (TXU):** b0: Number of Tx Trigger as expected b1: Less Tx trigger than expected in one matrix cycle
9	0h RW/1C	**Global Time Error (GTE):** Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. b0: Synchronization deviation within limit b1: Synchronization deviation exceeded limit
8	0h RW/1C	**Global Time Discontinuity (GTD):** b1: No discontinuity of global time b0: Discontinuity of global time
7	0h RW/1C	**Global Time Wrap (GTW):** b0: No global time wrap occurred b1: Global time wrap from 0xFFFF to 0x0000 occurred
6	0h RW/1C	**Stop Watch Event (SWE):** b0: No rising/falling edge at stop watch trigger pin m_ttcan_swt detected b1: Rising/falling edge at stop watch trigger pin m_ttcan_swt detected
5	0h RW/1C	**Trigger Time Mark Event Internal (TTMI):** Internal time mark events are configured by trigger memory element TMIN. Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. b0: Time mark not reached b1: Time mark reached (Level 0: cycle time TTOCF.IRTO X 0x200)
4	0h RW/1C	**Register Time Mark Interrupt (RTMI):** Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. b0: Time mark not reached b1: Time mark reached
3	0h RW/1C	**Start of Gap (SOG):** b0: No reference message seen with Next_is_Gap bit set b1: Reference message with Next_is_Gap bit set becomes valid
2	0h RW/1C	**Change of Synchronization Mode (CSM):** b0: No change in master to slave relation or schedule synchronization b1: Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset
1	0h RW/1C	**Start of Matrix Cycle (SMC):** b0: No Matrix Cycle started since bit has been reset b1: Matrix Cycle started
0	0h RW/1C	**Start of Basic Cycle (SBC):** b0: No Basic Cycle started since bit has been reset b1: Basic Cycle started

14.21.2.57 TT Interrupt Enable (TTIE) — Offset 50310124h

The settings in the TT Interrupt Enable register determine which status changes in the TT Interrupt Register will result in an interrupt.

Type	Size	Offset	Default
MMIO	32 bit	50310124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**Configuration Error Interrupt Enable (CERE):** b0: interrupt disabled b1: interrupt enabled
17	0h RW	**Application Watchdog Interrupt Enable (AWE):** b0: interrupt disabled b1: interrupt enabled
16	0h RW	**Watch Trigger Interrupt Enable (WTE):** b0: interrupt disabled b1: interrupt enabled
15	0h RW	**Initialization Watch Trigger Interrupt Enable (IWTE):** b0: interrupt disabled b1: interrupt enabled
14	0h RW	**Change Error Level Interrupt Enable (ELCE):** b0: interrupt disabled b1: interrupt enabled
13	0h RW	**Scheduling Error 2 Interrupt Enable (SE2E):** b0: interrupt disabled b1: interrupt enabled
12	0h RW	**Scheduling Error 1 Interrupt Enable (SE1E):** b0: interrupt disabled b1: interrupt enabled
11	0h RW	**Tx Count Overflow Interrupt Enable (TXOE):** b0: interrupt disabled b1: interrupt enabled
10	0h RW	**Tx Count Underflow Interrupt Enable (TXUE):** b0: interrupt disabled b1: interrupt enabled
9	0h RW	**Global Time Error Interrupt Enable (GTEE):** b0: interrupt disabled b1: interrupt enabled
8	0h RW	**Global Time Discontinuity Interrupt Enable (GTDE):** b0: interrupt disabled b1: interrupt enabled
7	0h RW	**Global Time Wrap Interrupt Enable (GTWE):** b0: interrupt disabled b1: interrupt enabled
6	0h RW	**Stop Watch Event Interrupt Enable (SWEE):** b0: interrupt disabled b1: interrupt enabled
5	0h RW	**Trigger Time Mark Event Internal Enable (TTMIE):** b0: interrupt disabled b1: interrupt enabled
4	0h RW	**Register Time Mark Interrupt Enable (RTMIE):** b0: interrupt disabled b1: interrupt enabled
3	0h RW	**Start of Gap Interrupt Enable (SOGE):** b0: interrupt disabled b1: interrupt enabled

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Change of Synchronization Mode Interrupt Enable (CSME):** b0: interrupt disabled b1: interrupt enabled
1	0h RW	**Start of Matrix Cycle Interrupt Enable (SMCE):** b0: interrupt disabled b1: interrupt enabled
0	0h RW	**Start of Basic Cycle Interrupt Enable (SBCE):** b0: interrupt disabled b1: interrupt enabled

14.21.2.58 TT Interrupt Line Select (TTILS) — Offset 50310128h

The TT Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the TT Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1. b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int1.

Type	Size	Offset	Default
MMIO	32 bit	50310128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**Configuration Error Interrupt Line (CERL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int1
17	0h RW	**Application Watchdog Interrupt Line (AWL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int2
16	0h RW	**Watch Trigger Interrupt Line (WTL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int3
15	0h RW	**Initialization Watch Trigger Interrupt Line (IWTL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int4
14	0h RW	**Change Error Level Interrupt Line (ELCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int5
13	0h RW	**Scheduling Error 2 Interrupt Line (SE2L):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int6
12	0h RW	**Scheduling Error 1 Interrupt Line (SE1L):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int7

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Tx Count Overflow Interrupt Line (TXOL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int8
10	0h RW	**Tx Count Underflow Interrupt Line (TXUL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int9
9	0h RW	**Global Time Error Interrupt Line (GTEL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int10
8	0h RW	**Global Time Discontinuity Interrupt Line (GTDL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int11
7	0h RW	**Global Time Wrap Interrupt Line (GTWL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int12
6	0h RW	**Stop Watch Event Interrupt Line (SWEL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int13
5	0h RW	**Trigger Time Mark Event Internal Line (TTMIL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int14
4	0h RW	**Register Time Mark Interrupt Line (RTMIL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int15
3	0h RW	**Start of Gap Interrupt Line (SOGL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int16
2	0h RW	**Change of Synchronization Mode Interrupt Line (CSML):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int17
1	0h RW	**Start of Matrix Cycle Interrupt Line (SMCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int18
0	0h RW	**Start of Basic Cycle Interrupt Line (SBCL):** b0: TT interrupt assigned to interrupt line m_ttcan_int0 b1: TT interrupt assigned to interrupt line m_ttcan_int19

14.21.2.59 TT Operation Status (TTOST) — Offset 5031012Ch

Type	Size	Offset	Default
MMIO	32 bit	5031012Ch	00000080h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Schedule Phase Lock (SPL):** The Bit is valid only when external synchronization is enabled (TTOCN.ESCN = b1). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU. b0: Phase outside range b1: Phase inside range
30	0h RO	**Wait for External Clock Synchronization (WECS):** b0: No external clock synchronization pending b1: Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle.
29	0h RO	**Application Watchdog Event (AWE):** The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. b0: Application Watchdog served in time b1: Failed to serve Application Watchdog in time
28	0h RO	**Wait for Event (WFE):** b0: No Gap announced, reset by a reference message with Next_is_Gap = b0 b1: Reference message with Next_is_Gap = b1 received
27	0h RO	**Gap Started Indicator (GSI):** b0: No Gap in schedule, reset by each reference message and for all time slaves b1: Gap time after Basic Cycle has started
26:24	0h RO	**Time Master Priority (TMP):** 0x0-7: Priority of actual Time Master
23	0h RO	**Gap Finished Indicator (GFI):** Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = b1, or via input pin m_ttcan_evt if TTOCN.GCS = b1. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. b0: Reset at the end of each reference message b1: Gap finished by M_TTCAN
22	0h RO	**Wait for Global Time Discontinuity (WGTD):** b0: No global time preset pending b1: Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = b1 or after it received a reference message.
21:16	0h RO	**Reserved**
15:8	00h RO	**Reference Trigger Offset (RTO):** The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = b11), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF: Actual Reference Trigger offset value

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Quality of Clock Speed (QCS):** Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to b1. b0: Local clock speed not synchronized to Time Master clock speed b1: Synchronization Deviation <= SDL
6	0h RO	**Quality of Global Time Phase (QGTP):** Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to b0. b0: Global time not valid b1: Global time in phase with Time Master
5:4	0h RO	**Synchronization State (SYS):** b00: Out of Synchronization b01: Synchronizing to TTCAN communication b10: Schedule suspended by Gap (In_Gap) b11: Synchronized to schedule (In_Schedule)
3:2	0h RO	**Master State (MS):** b00: Master_Off, no master properties relevant b01: Operating as Time Slave b10: Operating as Backup Time Master b11: Operating as current Time Master
1:0	0h RO	**Error Level (EL):** b00: Severity 0 - No Error b01: Severity 1 - Warning b10: Severity 2 - Error b11: Severity 3 - Severe Error

14.21.2.60 TUR Numerator Actual (TURNA) — Offset 50310130h

There is no drift compensation in TTCAN Level 1 (NAV = NC). In TTCAN Level 0 and Level 2, the drift between the nodes local clock and the time masters local clock is calculated. The drift is compensated when the Synchronisation Deviation (difference between NC and the calculated NAV) is not more than 2(TTOCF.LDSDL + 5). With TTOCF.LDSDL 7, this results in a maximum range for NAV of (NC - 0x1000) NAV (NC + 0x1000).

Type	Size	Offset	Default
MMIO	32 bit	50310130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:0	00000h RO	**Numerator Actual Value (NAV):** <= 0x0EFFF: Illegal value 0x0F000-20FFF: Actual numerator value >= 0x21000: Illegal value

14.21.2.61 TT Local and Global Time (TTLGT) — Offset 50310134h

Type	Size	Offset	Default
MMIO	32 bit	50310134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Global Time (GT):** Non-fractional part of the sum of the nodes local time and its local offset. 0x0000-FFFF: Global time value of TTCAN network
15:0	0000h RO	**Local Time (LT):** Non-fractional part of local time, incremented once each local NTU. 0x0000-FFFF: Local time value of TTCAN node

14.21.2.62 TT Cycle Time & Count (TTCTC) — Offset 50310138h

Type	Size	Offset	Default
MMIO	32 bit	50310138h	003F0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:16	3Fh RO	**Cycle Count (CC):** 0x00-3F Number of actual Basic Cycle in the System Matrix
15:0	0000h RO	**Cycle Time (CT):** Non-fractional part of the difference of the node's local time and Ref_Mark. 0x0000-FFFF Cycle time value of TTCAN Basic Cycle

14.21.2.63 TT Capture Time (TTCPT) — Offset 5031013Ch

Type	Size	Offset	Default
MMIO	32 bit	5031013Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Stop Watch Value (SWV):** On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is not equal to b0 and TTIR.SWE is b0, the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to b1. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF: Captured Stop Watch value
15:6	0h RO	**Reserved**
5:0	00h RO	**Cycle Count Value (CCV):** Cycle count value captured together with SWV. 0x00-3F: Captured cycle count value

14.21.2.64 TT Cycle Sync Mark (TTCSM) — Offset 50310140h

Type	Size	Offset	Default
MMIO	32 bit	50310140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RO	**Cycle Sync Mark (CSM):** The Cycle Sync Mark is measured in cycle time. It is updated when the reference message becomes valid and retains its value until the next reference message becomes valid. 0x0000-FFFF Captured cycle time

14.21.2.65 Message RAM Size (MSG_RAM_SIZE) — Offset 50310500h

Type	Size	Offset	Default
MMIO	32 bit	50310500h	00004600h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00004600h RO	**Size Bytes (SIZE_B):** Read only value of the size in bytes of the Message RAM of this dby_can instance @@jstokes3, need to set the default value where this RDL is instantiated

14.21.2.66 CTL — Offset 50310504h

Type	Size	Offset	Default
MMIO	32 bit	50310504h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**M_TTCAN Disable Error Data Modification on Read (CAN_DIS_MORD):** Set to 1 to prevent reads to ECR.CEL and PSR.LEC from resetting the CAN error data in the register.

14.21.2.67 Interrupt Control (INT_CTL) — Offset 50310508h

Type	Size	Offset	Default
MMIO	32 bit	50310508h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**PUNIT Interrupt Enable (PUNIT_INT_EN):** Enables the dby_can PUNIT interrupt output int_punit_o. Software is expected to set PUNIT_INT_EN or PRIMARY_INT_EN to b1, but not both.
0	0h RW	**Primary Interrupt Enable (PRIMARY_INT_EN):** Enables the primary interrupt output int_o. Software is expected to set PUNIT_INT_EN or PRIMARY_INT_EN to b1, but not both.

14.21.2.68 Interrupt Status (INT_STAT) — Offset 5031050Ch

Type	Size	Offset	Default
MMIO	32 bit	5031050Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Other CAN Parity Error Interrupt (OTHER_CAN_PERR_INT):** Parity error interrupt for the other CAN instance.
2	0h RO	**Other Controller Interrupt Status (OTHER_CAN_CONT_INT):** If asserted then the other instance of the M_TTCAN controller has its interrupt asserted.
1	0h RO	**This CAN Parity Error Interrupt (THIS_CAN_PERR_INT):** Parity error interrupt for this CAN instance.
0	0h RO	**This CAN Controller Interrupt Status (THIS_CAN_CONT_INT):** If asserted then this instance of the M_TTCAN controller has its interrupt asserted.

14.21.2.69 MSGRAM Address Conflict Status (MSGRAM_ADDR_CONFLICT_STAT) — Offset 50310510h

Type	Size	Offset	Default
MMIO	32 bit	50310510h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Address Conflict Occurred (ADDR_CONFLICT_OCCURED):** A flag to indicate that an address conflict has occurred. This can be used to help the debug of the CAN device driver. Note that this does not cause an interrupt.
15	0h RO	**Reserved**
14:0	0000h RO	**M_TTCAN Address Conflict Offset (CAN_ADDR_CONFLICT_OFFSET):** The M_TTCAN address that the conflict between an AHB access to the MSGRAM simultaneous to an M_TTCAN access to MSGRAM.

14.21.2.70 TTCAN TIMESTAMP CONTROL REGISTER (TIMESTAMP_CTL) — Offset 50310514h

Type	Size	Offset	Default
MMIO	32 bit	50310514h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO	**Remote Cross Timestamp Valid (RXTSV):**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Local Cross Timestamp Valid (LXTSV):**
1	0h RW	**Capture Remote Cross Timestamp (RXTSC):**
0	0h RW	**Capture Local Cross Timestamp (LXTSC):**

14.21.2.71 TTCAN LOCAL TIMESTAMP HIGH (LOCALTIMESTAMP_HIGH) — Offset 50310518h

Type	Size	Offset	Default
MMIO	32 bit	50310518h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Local Timestamp High (LTH):**

14.21.2.72 TTCAN LOCAL TIMESTAMP LOW (LOCALTIMESTAMP_LOW) — Offset 5031051Ch

Type	Size	Offset	Default
MMIO	32 bit	5031051Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Local Timestamp Low (LTL):**

14.21.2.73 CAN Parity Error Control and Status (PAR_CTL_STAT) — Offset 50310600h

Control and Status of Parity Check Functionality

Type	Size	Offset	Default
MMIO	32 bit	50310600h	00000003h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW/1C/P	**Parity Error Occured (PERR_OCCURED):** Sticky register which asserts when a parity error has been detected on a read from the message RAM. A write of b1 clears this field to b0. If they are enabled, the int_o and int_punit_o interrupt outputs may assert when this field is set to 1. The interrupts will clear when this field is cleared. This register field can only be reset on a powergoodrst_n.
1	1h RO	**Parity Initialisation In Progress (PARITY_INIT_IN_PROG):** Immediately on coming out of a reset (hresetn asserted) the message RAM will be parity initialised with writes of b0. While this is taking place, this field will read as 1. While this PARITY_INIT_IN_PROG is 1, reads to the message RAM will be stalled until completion of parity initialisation.
0	1h RW	**Parity Enable (PARITY_EN):** 1 - Parity bit generation, checking, error reporting and error injection are enabled for dby_can. 0 - All parity functionality is disabled for dby_can. The value of this field can only be updated by software when PARITY_INIT_IN_PROG == 0.

14.21.2.74 Parity Error Offset (PAR_ERR_OFFSET) — Offset 50310604h

Stores the message RAM offset at which a parity error occured in dby_can message RAM space

Type	Size	Offset	Default
MMIO	32 bit	50310604h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/P	**Parity Error In Upper 16 bits (PAR_ERR_UPP):** Indicates a that a parity error was detected in the upper 16 bits of the word at this offset. This register field can only be reset on a powergoodrst_n.
16	0h RO/P	**Parity Error In Lower 16 bits (PAR_ERR_LOW):** Indicates a that a parity error was detected in the lower 16 bits of the word at this offset. This register field can only be reset on a powergoodrst_n.
15	0h RO	**Reserved**
14:0	0000h RO/P	**Parity Error Offset (PAR_ERR_OFFSET):** Captures the message RAM offset at which a parity error occured. A new offset can only be captured when PERR_OCCURED is b0. This offset is relative to 0x0 in dby_can memory space. This register field can only be reset on a powergoodrst_n.

14.21.2.75 Parity Error Injection Control and Status (PAR_EINJ_CTL_STAT) — Offset 50310608h

Control and status for parity error injection to the dby_can message RAM.

Type	Size	Offset	Default
MMIO	32 bit	50310608h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RO	**One Time Parity Error Injection Occured (EINJ_ONE_TIME_ERR_OCCURED):** Asserts when a parity error is injected and EINJ_MODE = 0 (one time error injection). Cleared when EINJ_EN is set to b1 Once the one time parity error is injected, EINJ_EN deasserts. The intention then is that EINJ_ONE_TIME_ERR_OCCURED is the record that an error was injected.
1	0h RW	**Parity Error Injection Mode (EINJ_MODE):** b1 : Continuous error injection. All writes to the message RAM are corrupted based on the value of EINJ_MASK b0 : One time error injection. Only the first write to the address defined in EINJ_OFFSET is corrupted. After which EINJ_EN is cleared to b0 and EINJ_ONE_TIME_ERR_OCCURED is set to b1.
0	0h RW/AC	**Error Injection Enable (EINJ_EN):** 1 - Parity error injection is enabled 0 - Parity error injection is disabled Once the one time parity error is injected, EINJ_EN deasserts.

14.21.2.76 Parity Error Injection Offset (PAR_EINJ_OFFSET) — Offset 5031060Ch

Parity error injection offset in dby_can message RAM

Type	Size	Offset	Default
MMIO	32 bit	5031060Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:0	0000h RW	**Error Injection Offset (EINJ_OFFSET):** Offset at which an error will be injected, if enabled. This offset is relative to 0x0 in dby_can memory space.

14.21.2.77 Parity Error Injection Data Mask (PAR_EINJ_DATA_MASK) — Offset 50310610h

Parity error injection data mask for dby_can

Type	Size	Offset	Default
MMIO	32 bit	50310610h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Error Injection Data Mask (EINJ_DATA_MASK):** This field is XOR'd with the incoming write data in order to flip data bit/bits with respect to the value the parity bit was calculated for

14.21.2.78 Parity Error Injection Parity Mask (PAR_EINJ_PARITY_MASK) — Offset 50310614h

Parity error injection data mask for dby_can

Type	Size	Offset	Default
MMIO	32 bit	50310614h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RW	**Error Injection Parity Mask (EINJ_PARITY_MASK):** This field is XOR'd with the parity bits in order to flip data bit/bits with respect to the value the parity bit was calculated for

14.22 SRAM Registers

SRAM Registers	Address Offset	Table
SRAM	50400000h - 50400234h	Table 14-50

14.22.1 SRAM Registers Summary

Table 14-50. Summary of SRAM Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50400000h	4	SRAM_CFGR	00000000h
50400004h	4	SRAM_INTR_STS	00000000h
50400008h	4	SRAM_INTR_MASK	000000FEh
5040000Ch	4	SRAM_ICCM_ERASE_CTRL	00000000h
50400010h	4	SRAM_ICCM_ERASE_ADDR	00000000h
5040001Ch	4	SRAM_ECC_LOW_FAKE_ERR	00000000h
50400020h	4	SRAM_LOG_EN	00000000h
50400024h	4	SRAM_LOW_DOUBLE_ERR_ECC_LOG	00000000h
50400028h	4	SRAM_LOW_DOUBLE_ECC_CNT	00000000h
5040002Ch	4	SRAM_BANK_STATUS	00000000h
50400030h	4	SRAM_LOW_SINGLE_ERR_ECC_LOG	00000000h
50400034h	4	SRAM_LOW_SINGLE_ECC_CNT	00000000h
50400040h	4	SRAM_LIMIT	00000000h
50400044h	4	SRAM_ICCM_ERROR_LOG	00000000h
50400048h	4	SRAM_DCCM0_ERROR_LOG	00000000h
5040004Ch	4	SRAM_OCP_ERROR_LOG	00000000h
50400050h	4	CCM_BANK_TABLE_0	00010000h
50400054h	4	CCM_BANK_TABLE_1	00010000h
50400058h	4	CCM_BANK_TABLE_2	00010000h
5040005Ch	4	CCM_BANK_TABLE_3	00010000h
50400060h	4	CCM_BANK_TABLE_4	00010101h
50400064h	4	CCM_BANK_TABLE_5	00010101h
50400068h	4	CCM_BANK_TABLE_6	00010101h
5040006Ch	4	CCM_BANK_TABLE_7	00010101h
50400070h	4	CCM_BANK_TABLE_8	00010202h
50400074h	4	CCM_BANK_TABLE_9	00010202h
50400078h	4	CCM_BANK_TABLE_10	00010202h
5040007Ch	4	CCM_BANK_TABLE_11	00010202h
50400080h	4	CCM_BANK_TABLE_12	00010303h
50400084h	4	CCM_BANK_TABLE_13	00010303h
50400088h	4	CCM_BANK_TABLE_14	00010303h
5040008Ch	4	CCM_BANK_TABLE_15	00010303h
50400090h	4	CCM_BANK_TABLE_16	00010404h
50400094h	4	CCM_BANK_TABLE_17	00010404h
50400098h	4	CCM_BANK_TABLE_18	00010404h
5040009Ch	4	CCM_BANK_TABLE_19	00010404h
504000A0h	4	CCM_BANK_TABLE_20	00010505h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
504000A4h	4	CCM_BANK_TABLE_21	00010505h
504000A8h	4	CCM_BANK_TABLE_22	00010505h
504000ACh	4	CCM_BANK_TABLE_23	00010505h
504000B0h	4	CCM_BANK_TABLE_24	11010000h
504000B4h	4	CCM_BANK_TABLE_25	11010101h
504000B8h	4	CCM_BANK_TABLE_26	11010202h
504000BCh	4	CCM_BANK_TABLE_27	11010303h
504000C0h	4	L2_BANK_TABLE_0	00020000h
504000C4h	4	L2_BANK_TABLE_1	00020101h
504000C8h	4	L2_BANK_TABLE_2	00020202h
504000CCh	4	L2_BANK_TABLE_3	00020303h
504000D0h	4	L2_BANK_TABLE_4	00020404h
504000D4h	4	L2_BANK_TABLE_5	00020505h
504000D8h	4	L2_BANK_TABLE_6	00020606h
504000DCh	4	L2_BANK_TABLE_7	00020707h
504000E0h	4	L2_BANK_TABLE_8	00020808h
504000E4h	4	L2_BANK_TABLE_9	00020909h
504000E8h	4	L2_BANK_TABLE_10	00020A0Ah
504000ECh	4	L2_BANK_TABLE_11	00020B0Bh
504000F0h	4	L2_BANK_TABLE_12	00020C0Ch
504000F4h	4	L2_BANK_TABLE_13	00020D0Dh
504000F8h	4	L2_BANK_TABLE_14	00020E0Eh
504000FCh	4	L2_BANK_TABLE_15	00020F0Fh
50400200h	4	SRAM_L2_ERASE_CTRL	00000000h
50400204h	4	SRAM_L2_ERASE_ADDR	00000000h
50400208h	4	SRAM_ECC_HIGH_FAKE_ERR	00000000h
5040020Ch	4	SRAM_HIGH_DOUBLE_ERR_ECC_LOG	00000000h
50400210h	4	SRAM_HIGH_DOUBLE_ECC_CNT	00000000h
50400214h	4	SRAM_HIGH_SINGLE_ERR_ECC_LOG	00000000h
50400218h	4	SRAM_HIGH_SINGLE_ECC_CNT	00000000h
5040021Ch	4	SRAM_DCCM1_ERROR_LOG	00000000h
50400220h	4	SRAM_DCCM_ERASE_CTRL	00000000h
50400224h	4	SRAM_DCCM_ERASE_ADDR	00000000h
50400228h	4	SRAMC_ECC_FSM_CTRL	00000000h
5040022Ch	4	SRAM_DCCM1_HARD_FAULT_ERR_LOG	00000000h
50400230h	4	SRAM_DCCM0_HARD_FAULT_ERR_LOG	00000000h
50400234h	4	SRAM_ICCM_HARD_FAULT_ERR_LOG	00000000h

14.22.1.1 SRAM_CFGR — Offset 50400000h

This register is used to configure the SRAM.

Type	Size	Offset	Default
MMIO	32 bit	50400000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**SRAM Wait Retry Feature Enable (SRAM_WAIT_ENABLE):** SRAM Wait Retry Feature Enable 1: Wait Retry Feature Enabled 0: Wait Retry Feature Disabled .
4	0h RW	**ECC Correction Disable (ECC_DISABLE):** ECC Correction Disable. When this bit is set, ECC correction is disabled and the uncorrected data from memory is fed to the interface logic ECC Correction Disable. When this bit is set, ECC correction is disabled and the uncorrected data from memory is fed to the interface logic .
3	0h RW	**Disable Speculative Uncorrected Data Write (DISABLE_SPEC_RMW):** Disable speculative uncorrected data write during ECC read-modify-write operation.
2:0	0h RO	**Reserved**

14.22.1.2 SRAM_INTR_STS — Offset 50400004h

This register reports the cause of the interrupt from the SRAM block. Note that the individual interrupts are sent separately to the IOAPIC (separate RTEs in the IOAPIC).

Type	Size	Offset	Default
MMIO	32 bit	50400004h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**OCP Address Range Check Error (OCP_ADDR_RANGE_CHECK_ERR):** OCP Address Range Check Error. Hardware sets this bit to 1whenever the OCP range check fails (address is not within legal range). Software clears this bit by writing a 1 to the bit. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit set. The illegal address is trapped in SRAM_OCP_ERROR_LOG register. .
6	0h RW/1C	**DCCM1 Address Range Check Error. (DCCM1_ADDR_RANGE_CHECK_ERR):** DCCM1 Address Range Check Error. Hardware sets this bit to 1whenever the DCCM1 range check fails (address is not within legal range). Software clears this bit by writing a 1 to the bit. Note that this bit is not set in the case CORE signals a dccm_abort. dccm_abort signal is asserted (1 cycle after the read is issued) by the CORE for DCCM1 reads for accesses where the CORE will discard the read data. In these cases, the address from the CORE cannot be guaranteed to be legal and so an exception should not be signaled. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit set. The illegal address is trapped in SRAM_DCCM1_ERROR_LOG register .
5	0h RW/1C	**DCCM0 Address Range Check Error. (DCCM0_ADDR_RANGE_CHECK_ERR):** DCCM0 Address Range Check Error. Hardware sets this bit to 1whenever the DCCM0 range check fails (address is not within legal range). Software clears this bit by writing a 1 to the bit. Note that this bit is not set in the case CORE signals a dccm_abort. dccm_abort signal is asserted (1 cycle after the read is issued) by the CORE for DCCM reads for accesses where the CORE will discard the read data. In these cases, the address from the CORE cannot be guaranteed to be legal and so an exception should not be signaled. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit set. The illegal address is trapped in SRAM_DCCM0_ERROR_LOG register .
4	0h RW/1C	**ICCM Address Range Check Error (ICCM_ADDR_RANGE_CHECK_ERR):** ICCM Address Range Check Error. Hardware sets this bit to 1whenever the ICCM range check fails (address is not within legal range). Software clears this bit by writing a 1 to the bit. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit set. The illegal address is trapped in SRAM_ICCM_ERROR_LOG register .
3	0h RW/C	**ICCM SRAM Erase Complete (ICCM_ERASE_COMPLETE):** ICCM SRAM Erase Complete The hardware sets this bit to 1 when the ICCM SRAM Erase engine has completed. Software clears this bit by writing a 1 to the bit. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit is set. .

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/C	**DCCM SRAM Erase Complete (DCCM_ERASE_COMPLETE):** DCCM SRAM Erase Complete The hardware sets this bit to 1 when the DCCM SRAM Erase engine has completed. Software clears this bit by writing a 1 to the bit. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit is set. .
1	0h RW/1C	**L2 SRAM Erase Complete (L2_ERASE_COMPLETE):** L2 SRAM Erase Complete The hardware sets this bit to 1 when the L2 SRAM Erase engine has completed. Software clears this bit by writing a 1 to the bit. If the corresponding bit is set in the _Mask register, then an interrupt will be generated with this bit is set. .
0	0h RO	**Reserved**

14.22.1.3 SRAM_INTR_MASK — Offset 50400008h

This register is used to mask the interrupts caused by the SRAM block.

Type	Size	Offset	Default
MMIO	32 bit	50400008h	000000FEh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	1h RW	**OCP Range Check Error Mask (OCP_ADDR_RANGE_CHECK_ERR_MASK):** OCP Range Check Error Mask 1 OCP Range Check Error Interrupt masked 0 OCP Range Check Error Interrupt unmasked .
6	1h RW	**DCCM1 Range Check Error Mask (DCCM1_ADDR_RANGE_CHECK_ERR_MASK):** DCCM1 Range Check Error Mask 1 DCCM Range Check Error Interrupt masked 0 DCCM Range Check Error Interrupt unmasked .
5	1h RW	**DCCM0 Range Check Error Mask (DCCM0_ADDR_RANGE_CHECK_ERR_MASK):** DCCM0 Range Check Error Mask 1 DCCM Range Check Error Interrupt masked 0 DCCM Range Check Error Interrupt unmasked .
4	1h RW	**ICCM Range Check Error Mask 1 ICCM Range Check Error Interrupt Masked 0 ICCM Range Check Error Interrupt Unmasked (ICCM_ADDR_RANGE_CHECK_ERR_MASK):** ICCM Range Check Error Mask 1 ICCM Range Check Error Interrupt masked 0 ICCM Range Check Error Interrupt unmasked .
3	1h RW	**ICCM SRAM Erase Complete Mask (ICCM_ERASE_COMPLETE_MASK):** ICCM SRAM Erase Complete Mask 1=Erase Done interrupt masked 2= Erase Done interrupt unmasked.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**DCCM SRAM Erase Complete Mask (DCCM_ERASE_COMPLETE_MASK):** DCCM SRAM Erase Complete Mask 1=Erase Done interrupt masked 2= Erase Done interrupt unmasked.
1	1h RW	**L2 SRAM Erase Complete Mask (L2_ERASE_COMPLETE_MASK):** L2 SRAM Erase Complete Mask 1 = Erase Done interrupt masked 0 = Erase Done interrupt unmasked .
0	0h RO	**Reserved**

14.22.1.4 SRAM_ICCM_ERASE_CTRL — Offset 5040000Ch

This register is used to control the CCM SRAM Erase state machine.

Type	Size	Offset	Default
MMIO	32 bit	5040000Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:2	00000h RW	**CCM Erase Size (ERASE_SIZE):** CCM Erase Size Number of quad words (64 bits) to be erased. The actual length of this field is decided by the RTL parameter and is equal to TOTAL_MEM_SIZE/8. Partial word erase is not supported .
1	0h RO	**Reserved**
0	0h RW/1S	**CCM Erase Start (ERASE_START):** CCM Erase Start when software sets this bit to 1, the state machine will write zero to each Q word as indicated by the starting address in the SRAM_ERASE_ADDR register and the Erase Size field in this register. The state machine will clear this bit when the erase has completed. The ERASE_SIZE(31:2 of this register) must be programmed to a non zero value before starting ERASE operation. Reading this bit 1= Erase in progress. 0 = Erase done. Note :Will also read as O prior to any erase(not requested yet).

14.22.1.5 SRAM_ICCM_ERASE_ADDR — Offset 50400010h

This register sets the starting address for a CCM erase cycle.

Type	Size	Offset	Default
MMIO	32 bit	50400010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**The Starting Offset Address Of The Range To Be Erased. (ERASE_ADDR):** The starting offset address of the range to be erased. Note that this is the local physical address within the CCM memory space. Note: The width of this field is decided by RTL parameter TOTAL_MEM_SIZE and is [ADDR_SEL_HI:0] .

14.22.1.6 SRAM_ECC_LOW_FAKE_ERR — Offset 5040001Ch

This register is used to generate a fake ECC Low (uncorrectable) error to test the FW flows.

Type	Size	Offset	Default
MMIO	32 bit	5040001Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW/1C	**SRAM_ ECC_LOW_FAKE_ERR_STS (SRAM_ECC_FAKE_ERR_STS):** SRAM_ ECC_LOW_FAKE_ERR_STS This is for debug purpose only This bit will be set when there is a DED error detected OR when there is a FAKE error. Write 1: Writing a 1 clears the ecc_error output Write 0: Has no effect Read: Read always returns a zero .
0	0h RW	**SRAM_ECC_FAKE_ERR:** SRAM_ECC_LOW_FAKE_ERR This is for debug purpose only Write 1: Writing a 1 results in ecc error Write to this bit generates a one cycle pulse to emulate ecc_error Write 0: Has no effect Read: Read always returns a zero .

14.22.1.7 SRAM_LOG_EN — Offset 50400020h

This register enables logging of errors. When logging is disabled, the log registers will hold the attributes corresponding to the last erroneous condition.

Type	Size	Offset	Default
MMIO	32 bit	50400020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**SRAM DCCM1 Hard Fault Log Enable (DCCM1_HARD_LOG_ENABLE):** SRAM DCCM1 Hard Fault Log Enable 1: Logging of DCCM1 Hard Fault Logging enabled 0: Logging of DCCM1 Hard Fault Logging disabled When logging enabled, SRAM_DCCM1_HARD_FAULT_LOG will hold the OCP address which caused the hard fault error in DCCM1 I/F. .
9	0h RW	**SRAM DCCM0 Hard Fault Log Enable (DCCM0_HARD_LOG_ENABLE):** SRAM DCCM0 Hard Fault Log Enable 1: Logging of DCCM0 Hard Fault Logging enabled 0: Logging of DCCM0 Hard Fault Logging disabled When logging enabled, SRAM_DCCM0_HARD_FAULT_LOG will hold the OCP address which caused the hard fault error in DCCM0 I/F. .
8	0h RW	**SRAM ICCM Hard Fault Log Enable (ICCM_HARD_LOG_ENABLE):** SRAM ICCM Hard Fault Log Enable 1: Logging of ICCM Hard Fault Logging enabled 0: Logging of ICCM Hard Fault Logging disabled When logging enabled, SRAM_ICCM_HARD_FAULT_LOG will hold the OCP address which caused the hard fault error in ICCM I/F. .
7	0h RW	**SRAM OCP Range Check Error Log Enable (OCP_RANGE_CHECK_ERR_LOG_EN):** SRAM OCP Range Check Error Log Enable 1: Logging of OCP range check error enabled 0: Logging of OCP range check error disabled When logging enabled, SRAM_OCP_ERROR_LOG will hold the illegal OCP address which caused the range check error .
6	0h RW	**SRAM DCCM1 Range Check Error Log Enable (DCCM1_RANGE_CHECK_ERR_LOG_EN):** SRAM DCCM1 Range Check Error Log Enable 1: Logging of DCCM1 range check error enabled 0: Logging of DCCM1 range check error disabled When logging enabled, SRAM_DCCM1_ERROR_LOG will hold the illegal DCCM1 address which caused the range check error .
5	0h RW	**SRAM DCCM0 Range Check Error Log Enable (DCCM0_RANGE_CHECK_ERR_LOG_EN):** SRAM DCCM0 Range Check Error Log Enable 1: Logging of DCCM0 range check error enabled 0: Logging of DCCM0 range check error disabled When logging enabled, SRAM_DCCM0_ERROR_LOG will hold the illegal DCCM0 address which caused the range check error .
4	0h RW	**SRAM ICCM Range Check Error Log Enable (ICCM_RANGE_CHECK_ERR_LOG_EN):** SRAM ICCM Range Check Error Log Enable 1: Logging of ICCM range check error enabled 0: Logging of ICCM range check error disabled When logging enabled, SRAM_ICCM_ERROR_LOG will hold the illegal ICCM address which caused the range check error .
3	0h RW	**SRAM High Single Bit ECC Error Log Enable (SRAM_HIGH_SEC_ECC_LOG_EN):** SRAM High Single Bit ECC Error Log Enable 1: Logging of Single Bit ECC error enabled 0: Logging of Single Bit ECC error disabled .

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**SRAM Low Single Bit ECC Error Log Enable (SRAM_LOW_SEC_ECC_LOG_EN):** SRAM Low Single Bit ECC Error Log Enable 1: Logging of Single Bit ECC error enabled 0: Logging of Single Bit ECC error disabled .
1	0h RW	**SRAM High Double Bit ECC Error Log Enable (SRAM_HIGH_DED_ECC_LOG_EN):** SRAM High Double Bit ECC Error Log Enable 1: Logging of Double Bit ECC error enabled 0: Logging of Double Bit ECC error disabled .
0	0h RW	**SRAM Low Double Bit ECC Error Log Enable (SRAM_LOW_DED_ECC_LOG_EN):** SRAM Low Double Bit ECC Error Log Enable 1: Logging of Double Bit ECC error enabled 0: Logging of Double Bit ECC error disabled .

14.22.1.8 SRAM_LOW_DOUBLE_ERR_ECC_LOG — Offset 50400024h

This register contains the double bit Error ECC error log. This register is NA if RTL parameter ECC_SECDED is 0 (no double error detection).

Type	Size	Offset	Default
MMIO	32 bit	50400024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM Low Double Bit ECC Error Log Lock (SDEELL) (SDEELL):** SRAM Low Double Bit ECC Error Log Lock (SDEELL) When logging is enabled, this bit is set upon the first double bit ECC error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**SRAM Low ECC Error Uncorrectable (SEEUC) (SEEUC):** SRAM Low ECC Error Uncorrectable (SEEUC) Indication that an uncorrectable ECC error occurred on the data bus. .
29:24	00h RO	**SRAM Low ECC Error Bank (SEEB) For CCM (SEEB_CCM):** SRAM Low ECC Error Bank (SEEB) for CCM SRAM bank from PB Low which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
23:18	00h RO	**SRAM Low ECC Error Bank (SEEB) For L2 (SEEB_L2):** SRAM Low ECC Error Bank (SEEB) for L2 SRAM bank from PB Low which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
17:0	00000h RO	**SRAM Low ECC Error Address (SEEA) (SEEA):** SRAM Low ECC Error Address (SEEA) Address within the SRAM bank from PB Low which had the error. The width of this field is set by RTL_PARAMTER [10+LOG2(MEM_TILE_HEIGHT):0] .

14.22.1.9 SRAM_LOW_DOUBLE_ECC_CNT — Offset 50400028h

This register contains the count of double bit ECC errors from Lower Physical Banks.

Type	Size	Offset	Default
MMIO	32 bit	50400028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**SRAM Low Double Bit ECC Error Counter Reset (SDEECR) (SDEECR):** SRAM Low Double Bit ECC Error Counter Reset (SDEECR) Write 1: Clear SDEEC to 0. Write 0: Has No effect Read: always returns zero This is a self clearing bit .
30:16	0h RO	**Reserved**
15:8	00h RO	**SRAM Low Double Bit ECC Error Counter (SDEEC) (SDEEC_L2):** SRAM Low Double Bit ECC Error Counter (SDEEC) from lower PBs for L2 banks Counts the number of ECC errors which occur from PB Low. Cleared when FW writes SDEECR. Saturates at 0xFF. .
7:0	00h RO	**SRAM Low Double Bit ECC Error Counter (SDEEC) (SDEEC_CCM):** SRAM Low Double Bit ECC Error Counter (SDEEC) for CCM banks Counts the number of ECC errors which occur from PB Low. Cleared when FW writes SDEECR. Saturates at 0xFF. .

14.22.1.10 SRAM_BANK_STATUS — Offset 5040002Ch

This register reflects the power status of each of the SRAM banks.

Type	Size	Offset	Default
MMIO	32 bit	5040002Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:10	0000h RO	**SRAM Bank Is Ready To Be Accessed (L2_BANK_STATUS):** Field L2 Sram Bank Status.
9:0	000h RO	**SRAM Bank Is Ready To Be Accessed (SRAM_BANK_STATUS):** SRAM Bank is ready to be accessed. 1 bit status for every physical SRAM bank slice. The width of this field is set by RTL parameter NUM_PHYSICAL_BANKS/ (ACCESS_WIDTH/TILE_WIDTH).

14.22.1.11 SRAM_LOW_SINGLE_ERR_ECC_LOG — Offset 50400030h

This register logs the single bit ECC errors from Lower Physical Bank..

Type	Size	Offset	Default
MMIO	32 bit	50400030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM Low Single Bit ECC Error Log Lock (SSEELL) (SSEELL):** SRAM Low Single Bit ECC Error Log Lock (SSEELL) When logging is enabled, this bit is set upon the first single bit ECC error from PB Low. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**SRAM Low ECC Error Correctable (SEEC) (SEEC):** SRAM Low ECC Error Correctable (SEEC) Indication that a correctable ECC error occurred on the data bus from PB Low. .
29:24	00h RO	**SRAM Low ECC Error Bank (SEEB) For CCM Banks (SEEB_CCM):** SRAM Low ECC Error Bank (SEEB) for CCM banks SRAM bank from PB Low, which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
23:18	00h RO	**SRAM Low ECC Error Bank (SEEB) For L2 Banks (SEEB_CL2):** SRAM Low ECC Error Bank (SEEB) for L2 banks SRAM bank from PB Low which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
17:0	00000h RO	**SRAM Low ECC Error Address (SEEA) (SEEA):** SRAM Low ECC Error Address (SEEA) Address within the SRAM bank which had the error from PB Low. The width of this field is set by RTL_PARAMTER [10+LOG2(MEM_TILE_HEIGHT):0] .

14.22.1.12 SRAM_LOW_SINGLE_ECC_CNT — Offset 50400034h

This register contains the count of single bit ECC errors from Lower Physical Banks.

Type	Size	Offset	Default
MMIO	32 bit	50400034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**SRAM Low Single Bit ECC Error Counter Reset (SSEECR) (SSEECR):** SRAM Low Single Bit ECC Error Counter Reset (SSEECR) Write 1: Clear SSEEC to 0. Write 0: Has No effect Read: always returns zero This is a self clearing bit .
30:16	0h RO	**Reserved**
15:8	00h RO	**SRAM Low Single Bit ECC Error Counter (SSEEC) (SSEEC_L2):** SRAM Low Single Bit ECC Error Counter (SSEEC) from lower PBs for L2 banks Counts the number of ECC errors which occur from PB Low. Cleared when FW writes SSEECR. Saturates at 0xFF. .
7:0	00h RO	**SRAM Low Single Bit ECC Error Counter (SSEEC) (SSEEC_CCM):** SRAM Low Single Bit ECC Error Counter (SSEEC) from Lower PBs for CCM banks Counts the number of ECC errors which occur from PB Low. Cleared when FW writes SSEECR. Saturates at 0xFF. .

14.22.1.13 SRAM_LIMIT — Offset 50400040h

This register is used to program the ICCM LIMIT used to set the size of the ICCM partition. This is also used to check if the address from OCP/DCCM/ICCM is in legal range. The input signal uia_rst_n will reset this register synchronously.

Type	Size	Offset	Default
MMIO	32 bit	50400040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**ICCM LIMIT (ICCM_LIMIT):** ICCM LIMIT: This field defines the size of ICCM in 4KB units. E.g. if ICCM is configured to be 48KB, then this field will indicate 0xCh. This field resets to 0x0, upon any MIA-only reset condition (e.g. SHUTDOWN, IPC initiate reset). The width of this field is set by RTL parameter [LOG2(TOTAL_MEM_SIZE) 2] .

14.22.1.14 SRAM_ICCM_ERROR_LOG — Offset 50400044h

This register holds the address and command of the ICCM access that caused range check error.

Type	Size	Offset	Default
MMIO	32 bit	50400044h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM ICCM Error Log Lock (SIELL) (SIELL):** SRAM ICCM Error Log Lock (SIELL) This bit is set upon the first ICCM range check error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**ICCM Command Corresponding To The Address That Caused Range Check Error (ICCM_RANGE_CHECK_ERR_CMD):** ICCM Command corresponding to the address that caused range check error 0 : READ Command 1: Reserved This field is cleared when S/W clears the SRAM_INTR_STS[3] bit .
29:21	0h RO	**Reserved**
20:0	000000h RO	**ICCM Address That Caused Range Check Error (ICCM_RANGE_CHECK_ERR_ADDR):** ICCM Address that caused range check error. This field is cleared when S/W clears the SRAM_INTR_STS[3] bit. The width of this field is set by RTL parameter [ADDR_SEL_HI:0].

14.22.1.15 SRAM_DCCM0_ERROR_LOG — Offset 50400048h

This register holds the address and command of the DCCM0 access that caused range check error.

Type	Size	Offset	Default
MMIO	32 bit	50400048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM DCCM0 Error Log Lock (SDELL) (SDELL):** SRAM DCCM0 Error Log Lock (SDELL) This bit is set upon the first DCCM0 range check error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**DCCM0 Command Corresponding To The Address That Caused Range Check Error (DCCM_RANGE_CHECK_ERR_CMD):** DCCM0 Command corresponding to the address that caused range check error 0 : READ Command 1: WRITE Command This field is cleared when S/W clears the SRAM_INTR_STS[5] bit .
29:24	0h RO	**Reserved**
23:0	000000h RO	**DCCM0 Address That Caused Range Check Erro (DCCM_RANGE_CHECK_ERR_ADDR):** DCCM0 Address that caused range check error. This field is cleared when S/W clears the SRAM_INTR_STS[5] bit. The width of this field is set by RTL parameter [ADDR_SEL_HI:0].

14.22.1.16 SRAM_OCP_ERROR_LOG — Offset 5040004Ch

This register holds the address and command of the OCP access that caused range check error.

Type	Size	Offset	Default
MMIO	32 bit	5040004Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM OCP Error Log Lock (SOELL) This Bit Is Set Upon The First OCP Range Check Error. When This Bit Is Set, Hardware Cannot Update The Other Log Fields. FW Writes A 1 To This Register To Clear It And Allow Logging Of The Next Error. (SOELL):** SRAM OCP Error Log Lock (SOELL) This bit is set upon the first OCP range check error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**OCP Command Corresponding To The Address That Caused Range Check Error (OCP_RANGE_CHECK_ERR_CMD):** OCP Command corresponding to the address that caused range check error 0 : READ Command 1: WRITE Command This field is cleared when S/W clears the SRAM_INTR_STS[4] bit .
29:24	00h RO	**OCP MConnID Of The Master That Did The Illegal Access (OCP_ILLEGAL_ACCESS):** OCP MConnID of the master that did the illegal access. This field is cleared when S/W clears the SRAM_INTR_STS[5] bit.
23:22	0h RO	**Reserved**
21:0	000000h RO	**OCP Address That Caused Range Check Error (OCP_RANGE_CHECK_ERR_ADDR):** OCP Address that caused range check error. This field is cleared when S/W clears the SRAM_INTR_STS[5] bit. The width of this field is set by RTL parameter [ADDR_SEL_HI:0].

14.22.1.17 CCM_BANK_TABLE_0 — Offset 50400050h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Type	Size	Offset	Default
MMIO	32 bit	50400050h	00010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**CCM_PB_TYPE_HIGH:** CCM Erase Size Number of quad words (64 bits) to be erased. The actual length of this field is decided by the RTL parameter and is equal to TOTAL_MEM_SIZE/8. Partial word erase is not supported.
27:25	0h RO	**Reserved**
24	0h RW	**CCM_PB_TYPE_LOW:** CCM Erase Size Number of quad words (64 bits) to be erased. The actual length of this field is decided by the RTL parameter and is equal to TOTAL_MEM_SIZE/8. Partial word erase is not supported.
23:18	0h RO	**Reserved**
17:16	1h RW	**CCM_LB:** CCM_LB: Logical bank. The size of this bit field is determined by RTL parameter LOG2(NUM_LOGICAL_BANKS) .
15:13	0h RO	**Reserved**
12:8	00h RW	**CCM_PB_HIGH_INDEX:** CCM_PB_HIGH_INDEX: Higher Physical bank index. The size of this bit field is determined by RTL parameter CCM_PB_INDEX_WIDTH .
7:5	0h RO	**Reserved**
4:0	00h RW	**CCM_PB_LOW_INDEX:** CCM_PB_LOW_INDEX: Lower Physical bank index. The size of this bit field is determined by RTL parameter CCM_PB_INDEX_WIDTH .

14.22.1.18 CCM_BANK_TABLE_1 — Offset 50400054h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Type	Size	Offset	Default
MMIO	32 bit	50400054h	00010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**CCM_PB_TYPE_HIGH:** CCM_PB_TYPE: Physical bank type. The size of this bit field is determined by RTL parameter LOG2(CCM_NUM_PB_TYPES) .
27:25	0h RO	**Reserved**
24	0h RW	**CCM_PB_TYPE_LOW:** CCM_PB_TYPE: Physical bank type. The size of this bit field is determined by RTL parameter LOG2(CCM_NUM_PB_TYPES) .
23:18	0h RO	**Reserved**
17:16	1h RW	**CCM_LB:** CCM_LB: Logical bank. The size of this bit field is determined by RTL parameter LOG2(NUM_LOGICAL_BANKS) .
15:13	0h RO	**Reserved**
12:8	00h RW	**CCM_PB_HIGH_INDEX:** CCM_PB_HIGH_INDEX: Higher Physical bank index. The size of this bit field is determined by RTL parameter CCM_PB_INDEX_WIDTH .
7:5	0h RO	**Reserved**
4:0	00h RW	**CCM_PB_LOW_INDEX:** CCM_PB_LOW_INDEX: Lower Physical bank index. The size of this bit field is determined by RTL parameter CCM_PB_INDEX_WIDTH .

14.22.1.19 CCM_BANK_TABLE_2 — Offset 50400058h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.20 CCM_BANK_TABLE_3 — Offset 5040005Ch

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.21 CCM_BANK_TABLE_4 — Offset 50400060h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.22 CCM_BANK_TABLE_5 — Offset 50400064h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.23 CCM_BANK_TABLE_6 — Offset 50400068h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.24 CCM_BANK_TABLE_7 — Offset 5040006Ch

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.25 CCM_BANK_TABLE_8 — Offset 50400070h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.26 CCM_BANK_TABLE_9 — Offset 50400074h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.27 CCM_BANK_TABLE_10 — Offset 50400078h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.28 CCM_BANK_TABLE_11 — Offset 5040007Ch

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.29 CCM_BANK_TABLE_12 — Offset 50400080h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.30 CCM_BANK_TABLE_13 — Offset 50400084h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.31 CCM_BANK_TABLE_14 — Offset 50400088h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.32 CCM_BANK_TABLE_15 — Offset 5040008Ch

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.33 CCM_BANK_TABLE_16 — Offset 50400090h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.34 CCM_BANK_TABLE_17 — Offset 50400094h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.35 CCM_BANK_TABLE_18 — Offset 50400098h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.36 CCM_BANK_TABLE_19 — Offset 5040009Ch

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.37 CCM_BANK_TABLE_20 — Offset 504000A0h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.38 CCM_BANK_TABLE_21 — Offset 504000A4h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.39 CCM_BANK_TABLE_22 — Offset 504000A8h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.40 CCM_BANK_TABLE_23 — Offset 504000ACh

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.41 CCM_BANK_TABLE_24 — Offset 504000B0h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.42 CCM_BANK_TABLE_25 — Offset 504000B4h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.43 CCM_BANK_TABLE_26 — Offset 504000B8h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.44 CCM_BANK_TABLE_27 — Offset 504000BCh

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter CCM_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as CCM_BANK_TABLE_1, offset 50400054h.

14.22.1.45 L2_BANK_TABLE_0 — Offset 504000C0h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Type	Size	Offset	Default
MMIO	32 bit	504000C0h	00020000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**L2_PB_TYPE_HIGH:** L2_PB_TYPE: Physical bank type. The size of this bit field is determined by RTL parameter LOG2(L2_NUM_PB_TYPES) .
27:25	0h RO	**Reserved**
24	0h RW	**L2_PB_TYPE_LOW:** L2_PB_TYPE: Physical bank type. The size of this bit field is determined by RTL parameter LOG2(L2_NUM_PB_TYPES) .
23:18	0h RO	**Reserved**
17:16	2h RW	**L2_LB:** L2_LB: Logical bank. The size of this bit field is determined by RTL parameter LOG2(L2_NUM_LOGICAL_BANKS) .
15:12	0h RO	**Reserved**
11:8	0h RW	**L2_PB_HIGH_INDEX:** L2_PB_HIGH_INDEX: Higher Physical bank index. The size of this bit field is determined by RTL parameter L2_PB_INDEX_WIDTH .
7:4	0h RO	**Reserved**
3:0	0h RW	**L2_PB_LOW_INDEX:** L2_PB_LOW_INDEX: Lower Physical bank index. The size of this bit field is determined by RTL parameter L2_PB_INDEX_WIDTH .

14.22.1.46 L2_BANK_TABLE_1 — Offset 504000C4h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.47 L2_BANK_TABLE_2 — Offset 504000C8h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.48 L2_BANK_TABLE_3 — Offset 504000CCh

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.49 L2_BANK_TABLE_4 — Offset 504000D0h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.50 L2_BANK_TABLE_5 — Offset 504000D4h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.51 L2_BANK_TABLE_6 — Offset 504000D8h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.52 L2_BANK_TABLE_7 — Offset 504000DCh

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.53 L2_BANK_TABLE_8 — Offset 504000E0h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.54 L2_BANK_TABLE_9 — Offset 504000E4h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.55 L2_BANK_TABLE_10 — Offset 504000E8h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.56 L2_BANK_TABLE_11 — Offset 504000ECh

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.57 L2_BANK_TABLE_12 — Offset 504000F0h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.58 L2_BANK_TABLE_13 — Offset 504000F4h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.59 L2_BANK_TABLE_14 — Offset 504000F8h

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.60 L2_BANK_TABLE_15 — Offset 504000FCh

Based on the flexible banking scheme, there will be N such registers, N being determined by RTL derived parameter L2_NUM_ENTRIES (10 for GLV). Each register corresponds to a specific size of memory segment (64K for GLV). Each register has the same format as below. The input signal uia_rst_n will reset this register synchronously.

Note: Bit definitions are the same as L2_BANK_TABLE_0, offset 504000C0h.

14.22.1.61 SRAM_L2_ERASE_CTRL — Offset 50400200h

This register is used to control the L2 SRAM Erase state machine.

Type	Size	Offset	Default
MMIO	32 bit	50400200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:2	00000h RW	**L2 Erase Size (ERASE_SIZE):** L2 Erase Size Number of quad words (64 bits) to be erased. The actual length of this field is decided by the RTL parameter and is equal to TOTAL_MEM_SIZE/8. Partial word erase is not supported .
1	0h RO	**Reserved**
0	0h RW/1S	**L2 Erase Start (ERASE_START):** L2 Erase Start When software sets this bit to 1, the state machine will write zero to each QWord as indicated by the starting address in the SRAM_ERASE_ADDR register and the Erase Size field in this register. The state machine will clear this bit when the erase has completed. The ERASE_SIZE (31:2 of this register) must be programmed to a non-zero value before starting ERASE operation. Reading this bit: 1 = Erase in Progress. 0 = Erase Done. Note: Will also read as 0 prior to any erase (not requested yet). .

14.22.1.62 SRAM_L2_ERASE_ADDR — Offset 50400204h

This register sets the starting address for a L2 erase cycle.

Note: Bit definitions are the same as SRAM_ICCM_ERASE_ADDR, offset 50400010h.

14.22.1.63 SRAM_ECC_HIGH_FAKE_ERR — Offset 50400208h

This register is used to generate a fake ECC High (uncorrectable) error to test the FW flows.

Type	Size	Offset	Default
MMIO	32 bit	50400208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW/1C	**SRAM_ ECC_HIGH_FAKE_ERR_STS (SRAM_ECC_FAKE_ERR_STS):** SRAM_ ECC_HIGH_FAKE_ERR_STS This is for debug purpose only This bit will be set when there is a DED error detected OR when there is a FAKE error. Write 1: Writing a 1 clears the ecc_error output Write 0: Has no effect Read: Read always returns a zero .
0	0h RW	**SRAM_ECC_FAKE_ERR:** SRAM_ECC_HIGH_FAKE_ERR This is for debug purpose only Write 1: Writing a 1 results in ecc error Write to this bit generates a one cycle pulse to emulate ecc_error Write 0: Has no effect Read: Read always returns a zero .

14.22.1.64 SRAM_HIGH_DOUBLE_ERR_ECC_LOG — Offset 5040020Ch

This register contains the double bit Error ECC error log from Higher Physical Bank. This register is NA if RTL parameter ECC_SECDED is 0 (no double error detection).

Type	Size	Offset	Default
MMIO	32 bit	5040020Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM High Double Bit ECC Error Log Lock (SDEELL) (SDEELL):** SRAM High Double Bit ECC Error Log Lock (SDEELL) When logging is enabled, this bit is set upon the first double bit ECC error from PB High. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**SRAM High ECC Error Uncorrectable (SEEUC) (SEEUC):** SRAM High ECC Error Uncorrectable (SEEUC) Indication that an uncorrectable ECC error from PB high occurred on the data bus. .
29:24	00h RO	**SRAM High ECC Error Bank (SEEB) For CCM (SEEB_CCM):** SRAM High ECC Error Bank (SEEB) for CCM SRAM bank from PB High which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
23:18	00h RO	**SRAM High ECC Error Bank (SEEB) For L2 (SEEB_L2):** SRAM High ECC Error Bank (SEEB) for L2 SRAM bank from PB High which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
17:0	00000h RO	**SRAM High ECC Error Address (SEEA) (SEEA):** SRAM High ECC Error Address (SEEA) Address within the SRAM bank from PB High which had the error. The width of this field is set by RTL_PARAMTER [10+LOG2(MEM_TILE_HEIGHT):0] .

14.22.1.65 SRAM_HIGH_DOUBLE_ECC_CNT — Offset 50400210h

This register contains the count of double bit ECC errors from Higher Physical Banks.

Type	Size	Offset	Default
MMIO	32 bit	50400210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**SRAM High Double Bit ECC Error Counter Reset (SDEECR) (SDEECR):** SRAM High Double Bit ECC Error Counter Reset (SDEECR) Write 1: Clear SDEEC to 0. Write 0: Has No effect Read: always returns zero This is a self clearing bit .
30:16	0h RO	**Reserved**
15:8	00h RO	**SRAM High Double Bit ECC Error Counter (SDEEC) (SDEEC_L2):** SRAM High Double Bit ECC Error Counter (SDEEC) from higher PBs for L2 banks Counts the number of ECC errors which occur from PB High. Cleared when FW writes SDEECR. Saturates at 0xFF. .
7:0	00h RO	**SRAM High Double Bit ECC Error Counter (SDEEC) (SDEEC_CCM):** SRAM High Double Bit ECC Error Counter (SDEEC) for CCM banks Counts the number of ECC errors which occur from PB High. Cleared when FW writes SDEECR. Saturates at 0xFF. .

14.22.1.66 SRAM_HIGH_SINGLE_ERR_ECC_LOG — Offset 50400214h

This register logs the single bit ECC errors from Higher Physical Bank.

Type	Size	Offset	Default
MMIO	32 bit	50400214h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM High Single Bit ECC Error Log Lock (SSEELL) (SSEELL):** SRAM High Single Bit ECC Error Log Lock (SSEELL) When logging is enabled, this bit is set upon the first single bit ECC error from PB High. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**SRAM High ECC Error Correctable (SEEC) (SEEC):** SRAM High ECC Error Correctable (SEEC) Indication that a correctable ECC error occurred on the data bus from PB High. .

Bit Range	Default & Access	Field Name (ID): Description
29:24	00h RO	**SRAM High ECC Error Bank (SEEB) For CCM Banks (SEEB_CCM):** SRAM High ECC Error Bank (SEEB) for CCM banks SRAM bank from PB High, which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
23:18	00h RO	**SRAM High ECC Error Bank (SEEB) For L2 Banks (SEEB_L2):** SRAM High ECC Error Bank (SEEB) for L2 banks SRAM bank from PB High which had the error. The width of this field is set by RTL_PARAMETER log2(NUM_PHYSICAL_BANKS) .
17:0	00000h RO	**SRAM High ECC Error Address (SEEA) (SEEA):** SRAM High ECC Error Address (SEEA) Address within the SRAM bank which had the error from PB High. The width of this field is set by RTL_PARAMTER [10+LOG2(MEM_TILE_HEIGHT):0] .

14.22.1.67 SRAM_HIGH_SINGLE_ECC_CNT — Offset 50400218h

This register contains the count of single bit ECC errors from Higher Physical Banks.

Type	Size	Offset	Default
MMIO	32 bit	50400218h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**SRAM High Single Bit ECC Error Counter Reset (SSEECR) (SSEECR):** SRAM High Single Bit ECC Error Counter Reset (SSEECR) Write 1: Clear SSEEC to 0. Write 0: Has No effect Read: always returns zero This is a self clearing bit .
30:16	0h RO	**Reserved**
15:8	00h RO	**SRAM High Single Bit ECC Error Counter (SSEEC) (SSEEC_L2):** SRAM High Single Bit ECC Error Counter (SSEEC) from higher PBs for L2 banks Counts the number of ECC errors which occur from PB High. Cleared when FW writes SSEECR. Saturates at 0xFF. .
7:0	00h RO	**SRAM High Single Bit ECC Error Counter (SSEEC) (SSEEC_CCM):** SRAM High Single Bit ECC Error Counter (SSEEC) from Higher PBs for CCM banks Counts the number of ECC errors which occur from PB High. Cleared when FW writes SSEECR. Saturates at 0xFF. .

14.22.1.68 SRAM_DCCM1_ERROR_LOG — Offset 5040021Ch

This register holds the address and command of the DCCM1 access that caused range check error.

Type	Size	Offset	Default
MMIO	32 bit	5040021Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM DCCM1 Error Log Lock (SDELL) (SDELL):** SRAM DCCM1 Error Log Lock (SDELL) This bit is set upon the first DCCM0 range check error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30	0h RO	**SRAM DCCM1 Error Log Lock (SDELL) (DCCM_RANGE_CHECK_ERR_CMD):** SRAM DCCM1 Error Log Lock (SDELL) This bit is set upon the first DCCM1 range check error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
29:24	0h RO	**Reserved**
23:0	000000h RO	**DCCM0 Address That Caused Range Check Error. (DCCM_RANGE_CHECK_ERR_ADDR):** DCCM1 Address that caused range check error. This field is cleared A S/W clears the SRAM_INTR_STS[5] bit. The width of this field is set by RTLA parameter [ADDR_SEL_HI:0].

14.22.1.69 SRAM_DCCM_ERASE_CTRL — Offset 50400220h

This register is used to control the CCM SRAM Erase state machine.

Note: Bit definitions are the same as SRAM_ICCM_ERASE_CTRL, offset 5040000Ch.

14.22.1.70 SRAM_DCCM_ERASE_ADDR — Offset 50400224h

This register sets the starting address for a CCM erase cycle.

Note: Bit definitions are the same as SRAM_ICCM_ERASE_ADDR, offset 50400010h.

14.22.1.71 SRAMC_ECC_FSM_CTRL — Offset 50400228h

This register is used to program wait retry FSM count for 'N' successive retry's.

Type	Size	Offset	Default
MMIO	32 bit	50400228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**Program N Successive Rd & Wr For Wait Retry FSM (SRAMC_ECC_FSM_CTRL_CNT):** This field is to program counter value. HW FSM will attempt 'N' successive write & read in case of ECC error. Programming value can be done from 1 to 31 . By default, 0 value will be considered as 32 counter value. .

14.22.1.72 SRAM_DCCM1_HARD_FAULT_ERR_LOG — Offset 5040022Ch

This register holds the address and command of the DCCM0 access that hard fault error in the memories.

Type	Size	Offset	Default
MMIO	32 bit	5040022Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM DCCM1 Hard Fault Error Log Lock (SD1HFELL):** SRAM DCCM1 Hard Fault Error Log Lock (SD1HFELL) This bit is set upon the first DCCM1 Hard Fault error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30:24	0h RO	**Reserved**
23:0	000000h RO	**DCCM1 Address That Caused Hard Fault Error (DCCM1_ADDR_HARD_FAULT_ERR):** DCCM Address that caused hard fault.

14.22.1.73 SRAM_DCCM0_HARD_FAULT_ERR_LOG — Offset 50400230h

This register holds the address and command of the DCCM0 access that hard fault error in the memories.

Type	Size	Offset	Default
MMIO	32 bit	50400230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM DCCM0 Hard Fault Error Log Lock (SD0HFELL) (SD0HFELL):** SRAM DCCM0 Hard Fault Error Log Lock (SD0HFELL) This bit is set upon the first DCCM0 Hard Fault error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30:24	0h RO	**Reserved**
23:0	000000h RO	**DCCM0 Address That Caused Hard Fault Error (DCCM0_ADDR_HARD_FAULT_ERR):** DCCM Address that caused hard fault.

14.22.1.74 SRAM_ICCM_HARD_FAULT_ERR_LOG — Offset 50400234h

This register holds the address and command of the ICCM access that hard fault error in the memories.

Type	Size	Offset	Default
MMIO	32 bit	50400234h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SRAM ICCM Hard Fault Error Log Lock (SIHFELL) (SIHFELL):** SRAM ICCM Hard Fault Error Log Lock (SIHFELL) This bit is set upon the first ICCM Hard Fault error. When this bit is set, hardware cannot update the other log fields. FW writes a 1 to this register to clear it and allow logging of the next error. .
30:24	0h RO	**Reserved**
23:0	000000h RO	**ICCM Address That Caused Hard Fault Error (ICCM_ADDR_HARD_FAULT_ERR):** ICCM Address that caused hard fault.