Pentium™ Processor User's Manual

Volume 2: 82496 Cache Controller and 82491 Cache SRAM Data Book

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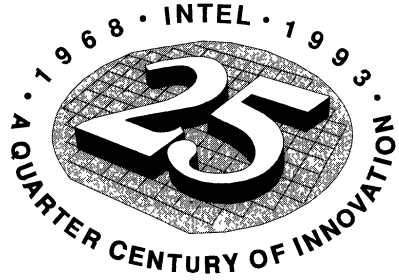

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Pentium™ Processor User's Manual

Volume 2:

82496 Cache Controller and 82491 Cache SRAM Data Book

NOTE: The *Pentium™ Processor User's Manual* consists of three books: *Pentium™ Processor Data Book*, Order Number 241428; the *82496 Cache Controller and 82491 Cache SRAM Data Book*, Order Number 241429; and the *Architecture and Programming Manual*, Order Number 241430.
Please refer to all three volumes when evaluating your design needs.

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NetSight™
OpenNET™
OverDrive™
Paragon™
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82496 CACHE CONTROLLER AND 82491 CACHE SRAM
FOR USE WITH THE PENTIUM™ PROCESSOR

- **High Performance Second Level Cache**
  - **Zero Wait States at 66 MHz**
  - **Two-way Set Associative**
  - **Write-Back with MESI Protocol**
  - **Concurrent CPU bus and memory bus operation**
  - **Boundary Scan**
- **Pentium Processor**
  - **Chip Set Version of Pentium Processor**
  - **Superscalar Architecture**
  - **Enhanced Floating Point**
  - **On-chip 8K Code and 8K Data Caches**
  - **See *Pentium™ Processor Data Book* for more information**
- **Highly Flexible**
  - **256K to 512K with parity**
  - **32, 64, or 128 Bit Wide Memory Bus**
  - **Synchronous, Asynchronous, and Strobed Memory Bus Operation**
  - **Selectable Bus Widths, Line Sizes, Transfers, and Burst Orders**
- **Full Multiprocessing Support**
  - **Concurrent CPU, Memory Bus, and Snoop Operations**
  - **Complete MESI Protocol**
  - **Internal/External Parity Generation/Checking**
  - **Supports Read-for Ownership, Write-Allocation, and Cache-to-Cache Transfers**

The 82496 Cache Controller and multiple 82491 Cache SRAMs combine with the Pentium processor to form a CPU Cache chip set designed for high performance servers and function-rich desktops. The high-speed interconnect between the CPU and cache components has been optimized to provide zero-wait state operation. This CPU Cache chip set is fully compatible with existing software, and has new data integrity features for mission critical applications.

The 82496 cache controller implements the MESI write-back protocol for full multiprocessing support. Dual ported buffers and registers allow the 82496 to concurrently handle CPU bus, memory bus, and internal cache operation for maximum performance.

The 82491 is a customized high-performance SRAM that supports 32, 64, and 128-bit wide memory bus widths, 16, 32, and 64 byte line sizes, and optional sectoring. The data path between the CPU bus and memory bus is separated by the 82491, allowing the CPU bus to handshake synchronously, asynchronously, or with a strobed protocol, and allowing concurrent CPU bus and memory bus operations.

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CHAPTER 1
PINOUTS

1.1. PINOUT DIAGRAMS

1.1.1. Pentium™ Processor Pinouts

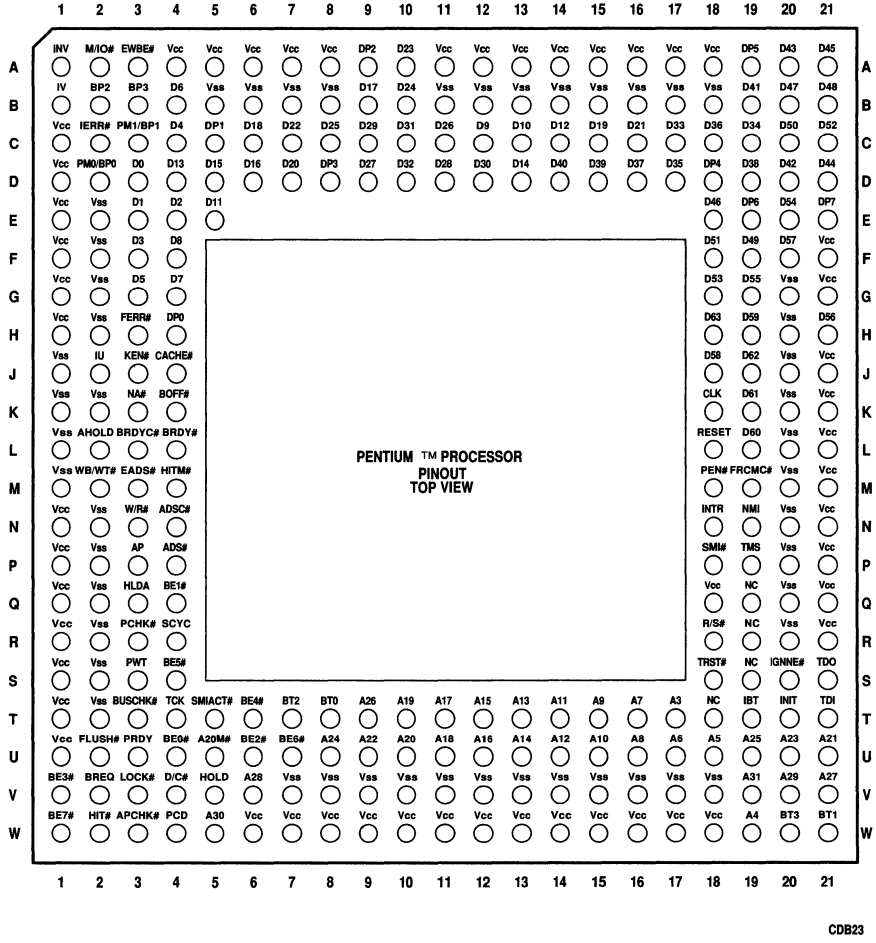

Figure 1-1. Pentium™ Processor Pinout (Top View)

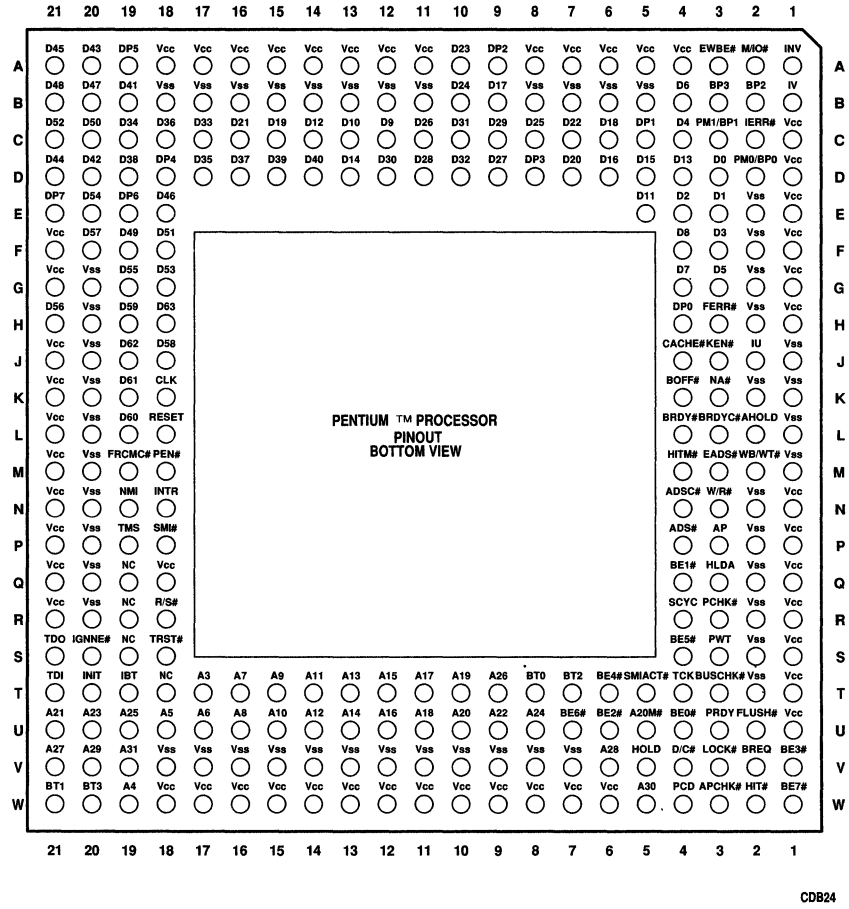

Figure 1-2. Pentium™ Processor Pinout (Bottom View)

1.1.2. 82496 Cache Controller Pinouts

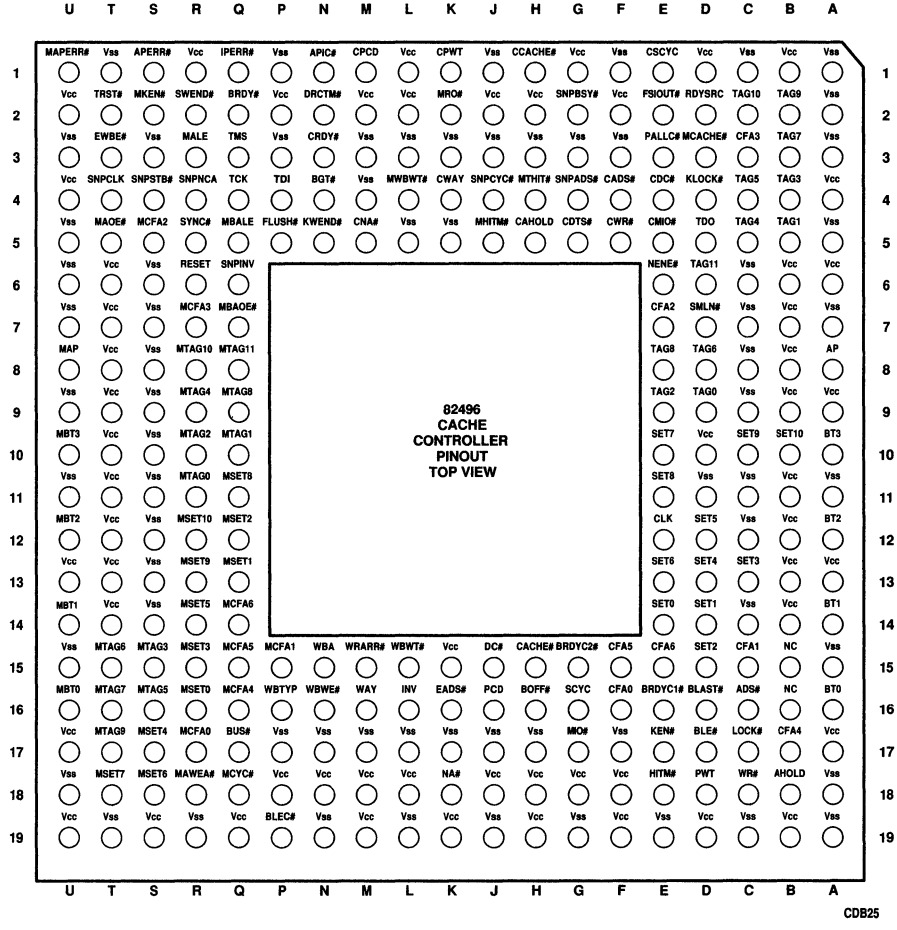

Figure 1-3. 82496 Cache Controller Pinout (Top View)

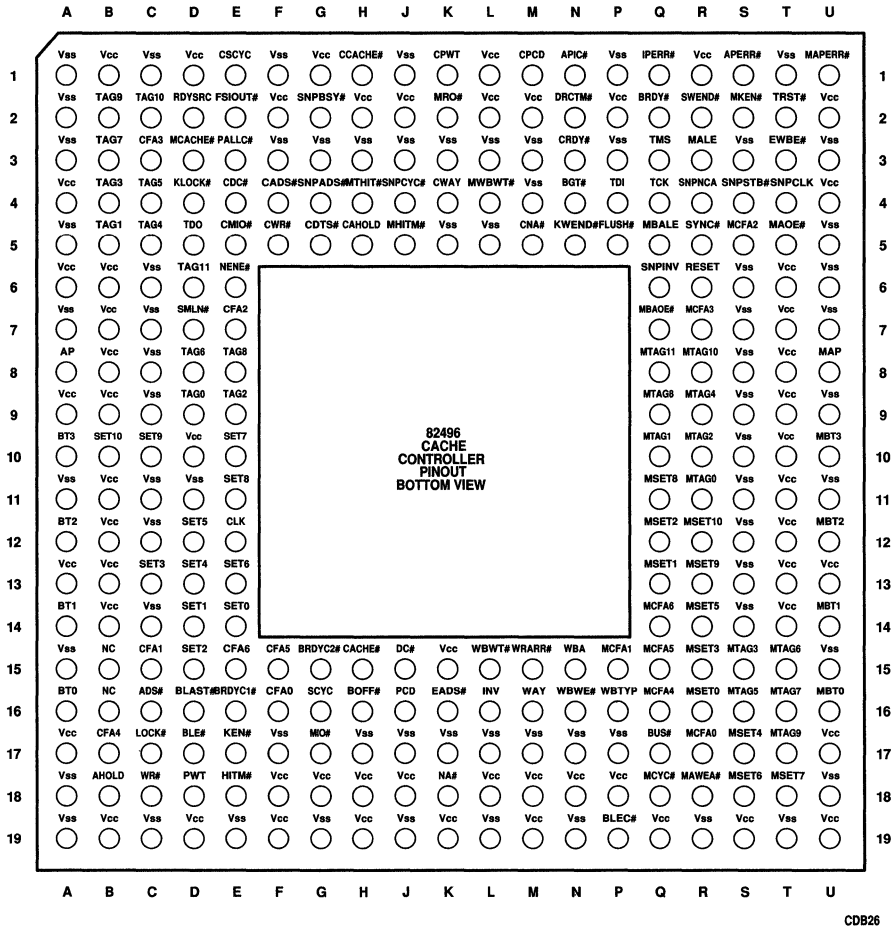

Figure 1-4. 82496 Cache Controller Pinout (Bottom View)

1.1.3. 82491 Cache SRAM Memory Pinouts

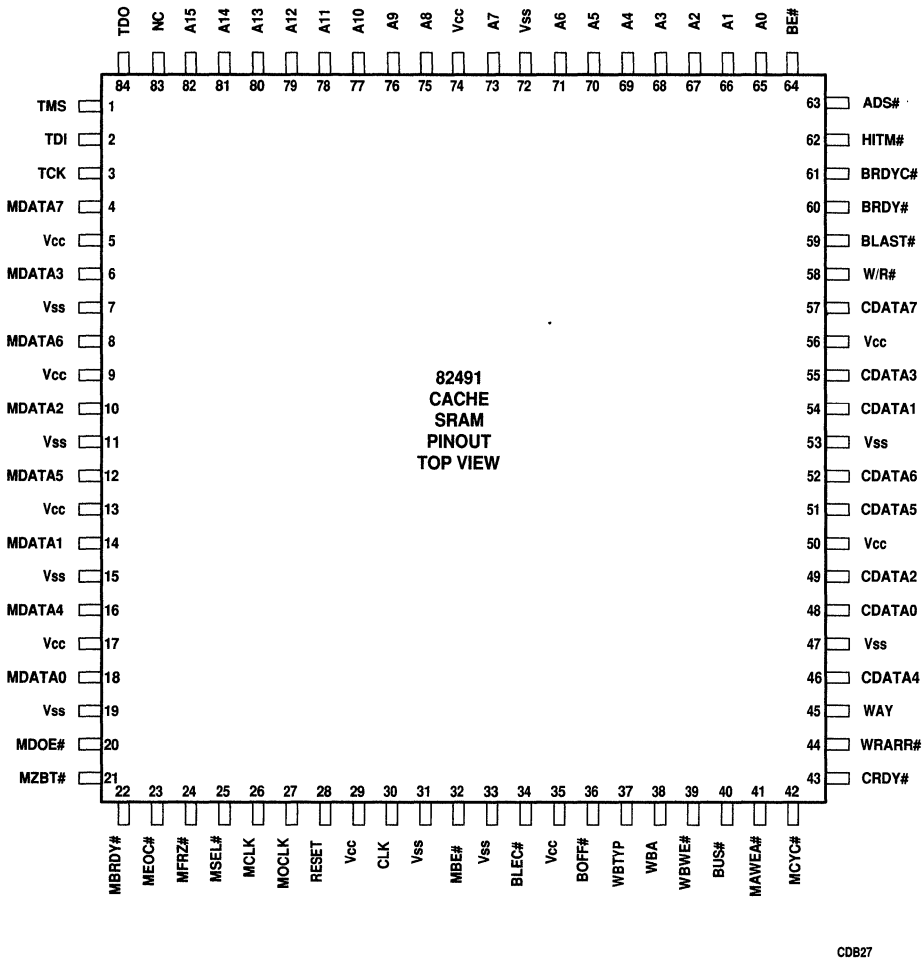

Figure 1-5. 82491 Cache SRAM Memory Pinout (Top View)

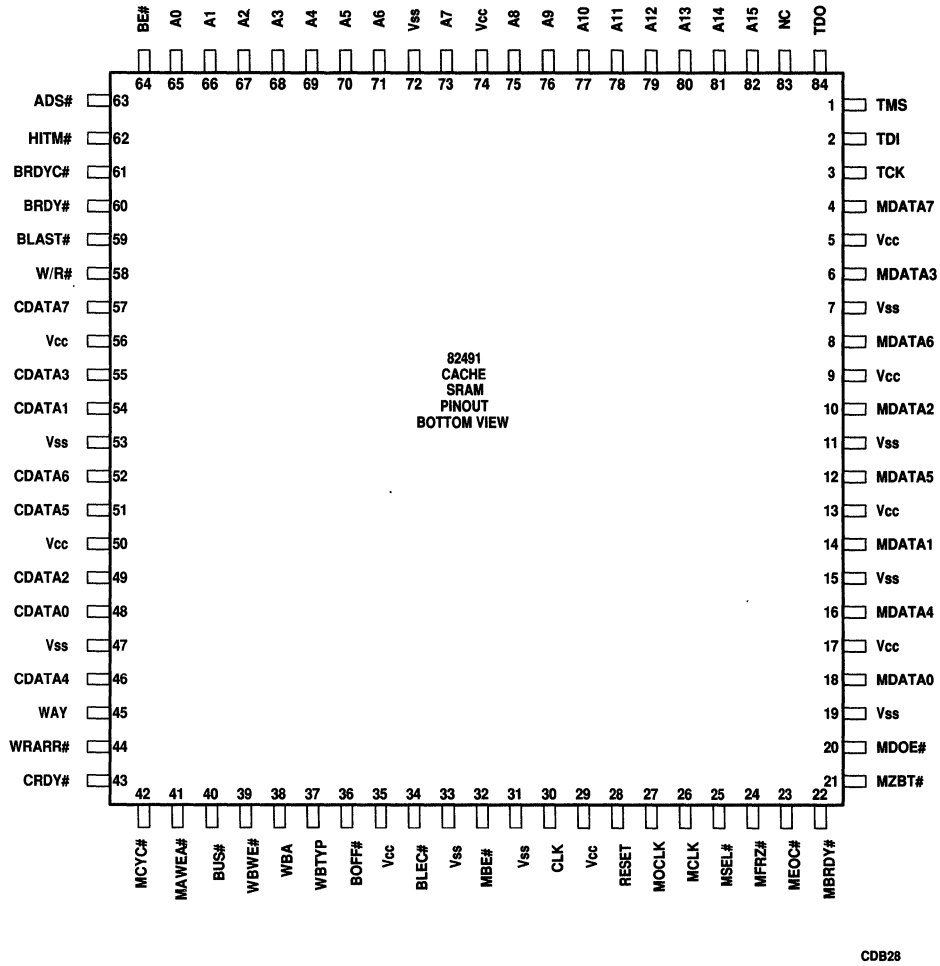

Figure 1-6. 82491 Cache SRAM Pinout (Bottom View)

1.2. PIN CROSS REFERENCE TABLES

1.2.1. Pentium Processor

Table 1-1. Pentium™ Processor Pin Cross Reference by Pin Name

Address		Data				Control			
A3	T17	D0	D03	D32	D10	A20M#	U05	FRCMC#	M19
A4	W19	D1	E03	D33	C17	ADS#	P04	HIT#	W02
A5	U18	D2	E04	D34	C19	ADSC#	N04	HITM#	M04
A6	U17	D3	F03	D35	D17	AHOLD	L02	HLDA	Q03
A7	T16	D4	C04	D36	C18	AP	P03	HOLD	V05
A8	U16	D5	G03	D37	D16	APCHK#	W03	IBT	T19
A9	T15	D6	B04	D38	D19	BE0#	U04	IERR#	C02
A10	U15	D7	G04	D39	D15	BE1#	Q04	IGNNE#	S20
A11	T14	D8	F04	D40	D14	BE2#	U06	INIT	T20
A12	U14	D9	C12	D41	B19	BE3#	V01	INTR	N18
A13	T13	D10	C13	D42	D20	BE4#	T06	INV	A01
A14	U13	D11	E05	D43	A20	BE5#	S04	IU	J02
A15	T12	D12	C14	D44	D21	BE6#	U07	IV	B01
A16	U12	D13	D04	D45	A21	BE7#	W01	KEN#	J03
A17	T11	D14	D13	D46	E18	BOFF#	K04	LOCK#	V03
A18	U11	D15	D05	D47	B20	BP2	B02	M/IO#	A02
A19	T10	D16	D06	D48	B21	BP3	B03	NA#	K03
A20	U10	D17	B09	D49	F19	BRDY#	L04	NMI	N19
A21	U21	D18	C06	D50	C20	BRDYC#	L03	PCD	W04
A22	U09	D19	C15	D51	F18	BREQ	V02	PCHK#	R03
A23	U20	D20	D07	D52	C21	BUSCHK#	T03	PEN#	M18
A24	U08	D21	C16	D53	G18	CACHE#	J04	PM0/BP0	D02
A25	U19	D22	C07	D54	E20	CLK	K18	PM1/BP1	C03
A26	T09	D23	A10	D55	G19	D/C#	V04	PRDY	U03

Table 1-1. Pentium™ Processor Pin Cross Reference by Pin Name (Contd.)

Address		Data				Control			
A27	V21	D24	B10	D56	H21	DP0	H04	PWT	S03
A28	V06	D25	C08	D57	F20	DP1	C05	R/S#	R18
A29	V20	D26	C11	D58	J18	DP2	A09	RESET	L18
A30	W05	D27	D09	D59	H19	DP3	D08	SCYC	R04
A31	V19	D28	D11	D60	L19	DP4	D18	SMI#	P18
		D29	C09	D61	K19	DP5	A19	SMIACT#	T05
BT0	T08	D30	D12	D62	J19	DP6	E19	TCK	T04
BT1	W21	D31	C10	D63	H18	DP7	E21	TDI	T21
BT2	T07					EADS#	M03	TDO	S21
BT3	W20					EWBE#	A03	TMS	P19
						FERR#	H03	TRST#	S18
						FLUSH#	U02	W/R#	N03
								WB/WT#	M02

VCC				VSS					
A04	C01	N21	W08	B05	B15	H02	L20	Q20	V10
A05	D01	P01	W09	B06	B16	H20	M01	R02	V11
A06	E01	P21	W10	B07	B17	J01	M20	R20	V12
A07	F01	Q01	W11	B08	B18	J20	N02	S02	V13
A08	F21	Q18	W12	B11	E02	K01	N20	T02	V14
A11	G01	Q21	W13	B12	F02	K02	P02	V07	V15
A12	G21	R01	W14	B13	G02	K20	P20	V08	V16
A13	H01	R21	W15	B14	G20	L01	Q02	V09	V17
A14	J21	S01	W16						V18
A15	K21	T01	W17						
A16	L21	U01	W18						
A17	M21	W06			**NC:**	Q19	S19	R19	T18
A18	N01	W07							

1.2.2. 82496 Cache Controller

Table 1-2. 82496 Cache Controller Pin Cross Reference by Pin Name

Cache Control							
ADS#	C16	CNA#	M05	MAOE#	T05	SNPADS#	G04
AHOLD	B18	CPCD	M01	MAP	U08	SNPBSY#	G02
AP	A08	CPWT	K01	MAPERR#	U01	SNPCLK	T04
APERR#	S01	CRDY#	N03	MAWEA#	R18	SNPCYC#	J04
APIC#	N01	CSCYC	E01	MBALE	Q05	SNPINV	Q06
BGT#	N04	CW/R#	F05	MBAOE#	Q07	SNPNCA	R04
BLAST#	D16	CWAY	K04	MCACHE#	D03	SNPSTB#	S04
BLE#	D17	D/C#	J15	MCYC#	Q18	SWEND#	R02
BLEC#	P19	DRCTM#	N02	MHITM#	J05	SYNC#	R05
BOFF#	H16	EADS#	K16	MKEN#	S02	TCK	Q04
BRDY#	Q02	EWBE#	T03	MRO#	K02	TDI	P04
BRDYC1#	E16	FLUSH#	P05	MTHIT#	H04	TDO	D05
BRDYC2#	G15	FSIOUT#	E02	MWB/WT#	L04	TMS	Q03
BUS#	Q17	HITM#	E18	NA#	K18	TRST#	T02
CACHE#	H15	INV	L16	NENE#	E06	W/R#	C18
CADS#	F04	IPERR#	Q01	PALLC#	E03	WAY	M16
CAHOLD	H05	KEN#	E17	PCD	J16	WB/WT#	L15
CCACHE#	H01	KLOCK#	D04	PWT	D18	WBA	N15
CD/C#	E04	KWEND#	N05	RDYSRC	D02	WBTYP	P16
CDTS#	G05	LOCK#	C17	RESET	R06	WBWE#	N16
CLK	E12	M/IO#	G17	SCYC	G16	WRARR#	M15
CM/IO#	E05	MALE	R03	SMLN#	D07		

Table 1-2. 82496 Cache Controller Pin Cross Reference by Pin Name (Contd.)

CPU Bus Address					
CFA0	F16	SET0	E14	TAG0	D09
CFA1	C15	SET1	D14	TAG1	B05
CFA2	E07	SET2	D15	TAG2	E09
CFA3	C03	SET3	C13	TAG3	B04
CFA4	B17	SET4	D13	TAG4	C05
CFA5	F15	SET5	D12	TAG5	C04
CFA6	E15	SET6	E13	TAG6	D08
		SET7	E10	TAG7	B03
BT0	A16	SET8	E11	TAG8	E08
BT1	A14	SET9	C10	TAG9	B02
BT2	A12	SET10	B10	TAG10	C02
BT3	A10			TAG11	D06
Memory Bus Address					
MCFA0	R17	MSET0	R16	MTAG0	R11
MCFA1	P15	MSET1	Q13	MTAG1	Q10
MCFA2	S05	MSET2	Q12	MTAG2	R10
MCFA3	R07	MSET3	R15	MTAG3	S15
MCFA4	Q16	MSET4	S17	MTAG4	R09
MCFA5	Q15	MSET5	R14	MTAG5	S16
MCFA6	Q14	MSET6	S18	MTAG6	T15
		MSET7	T18	MTAG7	T16
MBT0	U16	MSET8	Q11	MTAG8	Q09
MBT1	U14	MSET9	R13	MTAG9	T17
MBT2	U12	MSET10	R12	MTAG10	R08
MBT3	U10			MTAG11	Q08

Table 1-2. 82496 Cache Controller Pin Cross Reference by Pin Name (Contd.)

VSS			VCC		
A01	G03	R19	A04	F02	P02
A02	G19	S03	A06	F18	P18
A03	H03	S06	A09	F19	Q19
A05	H17	S07	A13	G01	R01
A07	J01	S08	A17	G18	S19
A11	J03	S09	B01	H02	T06
A15	J17	S10	B06	H18	T07
A18	J19	S11	B07	H19	T08
A19	K03	S12	B08	J02	T09
C01	K05	S13	B09	J18	T10
C06	K17	S14	B11	K15	T11
C07	L03	T01	B12	K19	T12
C08	L05	T19	B13	L01	T13
C09	L17	U03	B14	L02	T14
C11	L19	U05	B19	L18	U02
C12	M03	U06	D01	M02	U04
C14	M04	U07	D10	M18	U13
C19	M17	U09	D19	M19	U17
D11	N17	U11		N18	U19
E19	N19	U15			
F01	P01	U18			
F03	P03		**NC:**	B15	B16
F17	P17				

1.2.3. 82491 Cache SRAM

Table 1-3. 82491 Cache SRAM Pin Cross Reference by Pin Name

Address		CPU Bus Data		Control			
A0	65	CDATA0	48	ADS#	63	MEOC#	23
A1	66	CDATA1	54	BE#	64	MFRZ#	24
A2	67	CDATA2	49	BLAST#	59	MOCLK	27
A3	68	CDATA3	55	BLEC#	34	MSEL#	25
A4	69	CDATA4	46	BOFF#	36	MZBT#	21
A5	70	CDATA5	51	BRDY#	60	RESET	28
A6	71	CDATA6	52	BRDYC#	61	TCK	3
A7	73	CDATA7	57	BUS#	40	TDI	2
A8	75	Memory Bus Data		CLK	30	TDO	84
A9	76			CRDY#	43	TMS	1
A10	77	MDATA0	18	HITM#	62	W/R#	58
A11	78	MDATA1	14	MAWEA#	41	WAY	45
A12	79	MDATA2	10	MBE#	32	WBA	38
A13	80	MDATA3	6	MBRDY#	22	WBTYP	37
A14	81	MDATA4	16	MCLK	26	WBWE#	39
A15	82	MDATA5	12	MCYC#	42	WRARR#	44
		MDATA6	8	MDOE#	20		
		MDATA7	4				

NC	VCC			VSS		
83	5	17	50	7	19	47
	9	29	56	11	31	53
	13	35	74	15	33	72

1.3. BRIEF PIN DESCRIPTIONS

This section provides brief descriptions of all signals of the Pentium processor CPU-Cache Chip Set.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

Tables 1-4 through 1-9 list the signals which comprise each interface — both external (i.e. to the memory bus controller) and internal (i.e. the Pentium processor CPU-Cache Chip Set optimized interface).

Figure 1-7 illustrates signal partitioning.

Table 1-10 describes all Pentium processor signals to which the Memory Bus Controller has access, all 82496 Cache Controller signals, all 82491 Cache SRAM signals, and all Optimized interface signals.

Tables 1-11 to 1-13 list the Pentium processor CPU-Cache Chip Set signals which have internal pull-up or pull-down resistors and are glitch free.

Table 1-14 lists the interconnects between the optimized interface signals.

Tables 1-15 to 1-18 list pin states at reset, Output pins, Input pins, and Input/Output pins.

The following abbreviations may be used in Tables 1-7 through 1-18: P (Pentium processor), CC (82496 Cache Controller), and CS (82491 Cache SRAM).

For detailed Pentium processor pin descriptions, refer to the *Pentium™ Processor Data Book.* For detailed 82496 Cache Controller and 82491 Cache SRAM pin descriptions refer to the Hardware Interface chapter. **Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior of the 82496 Cache Controller and 82491 Cache SRAM.**

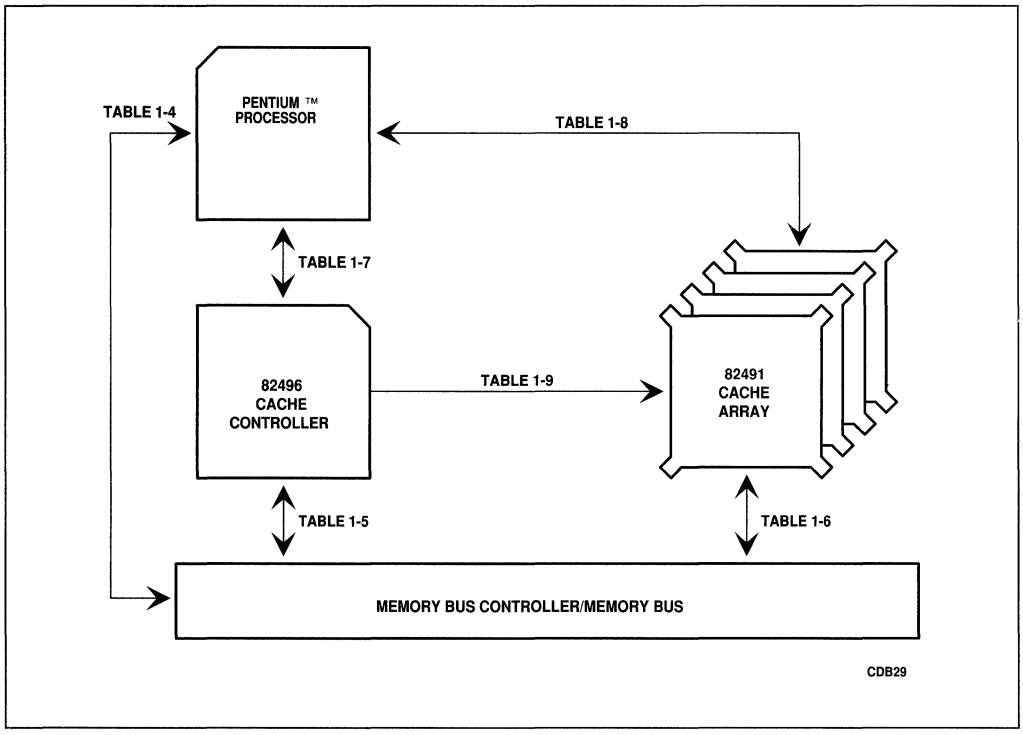

Figure 1-7. Brief Pin Description Table Cross Reference

In the following tables, a signal name in brackets "[ ]" represents a configuration input signal sampled at RESET, and a signal name in parenthesis "( )" represents a strobed mode signal.

Table 1-4. Pentium™ Processor/MBC Interface Signals

APCHK#	CLK	HOLD	INTR	PEN#	SMIACT#
BP[3:2],PM/BP[1:0]	FERR#	IBT	IU	PRDY	TCK
BRDY#	FLUSH#	IERR#	IV	R/S#	TDI
BREQ	HLDA	IGNNE#	NMI	RESET	TDO
BUSCHK#	HIT#	INIT	PCHK#	SMI#	TMS
					TRST#

Table 1-5. 82496 Cache Controller/MBC Interface Signals

APERR#	CM/IO#	KLOCK#	MRO#	SNPINV
APIC#	CNA# [CFG0]	KWEND# [CFG2]	MTHIT#	SNPNCA
BGT# [CLDRV]	CPCD	MALE [WWOR#]	MWB/WT#	SNPSTB#
BLE#	CPWT	MAOE#	NENE#	SWEND# [CFG1]
BRDY#	CRDY# [SLFTST#]	MAP	PALLC#	SYNC# [MALDRV]
CADS#	CSCYC	MAPERR#	RDYSRC	TCK
CAHOLD	CW/R#	MBALE [HIGHZ#]	RESET	TDI
CCACHE#	CWAY	MBAOE#	SMLN#	TDO
CD/C#	DRCTM#	MBT[3:0]	SNPADS#	TMS
CDTS#	FLUSH#	MCACHE#	SNPBSY#	TRST#
CFG[2:0]	FSIOUT#	MHITM#	SNPCLK [SNPMD]	
CLK	IPERR#	MKEN#	SNPCYC#	
MCFA[6:0], MSET[10:0], MTAG[11:0]				

Table 1-6. 82491 Cache SRAM/MBC Interface Signals

BRDY#	MBRDY# (MISTB)	MEOC#	MZBT# [MX4/8#]	TDO
CLK	MCLK [MSTBM]	MFRZ# [MDLDRV]	RESET	TMS
CRDY#	MDATA[7:0]	MOCLK (MOSTB)	TCK	
MBE# [PAR#]	MDOE#	MSEL# [MTR4/8#]	TDI	

Table 1-7. Pentium™ Processor/82496 Cache Controller Interface Signals

ADSC#/ADS#	BRDYC#/BRDYC1 #	EADS#	KEN#	PCD
AHOLD	BT[3:0]	EWBE#	LOCK#	PWT
AP	CACHE#	HITM#	M/IO#	SCYC
BOFF#	D/C#	INV	NA#	W/R#
A[31:3]/CFA[6:0], SET[10:0], TAG[11:0]				WB/WT#

Table 1-8. Pentium™ Processor/82491 Cache SRAM Interface Signals

A[17:3]/A[15:1]	ADS#	BE[7:0]#/BE#	D[63:0]/CDATA[7:0]
HITM#	W/R#	BE[7:0]#/CDATA[7:4][1-1]	DP[3:0]/CDATA[3:0][1-1]

1-1 82491 Cache SRAMs configured as parity devices.

Table 1-9. 82496 Cache Controller/82491 Cache SRAM Interface Signals

BLAST#	BRDYC2#/BRDYC#	MCYC#	WBTYP [LR0]
BLEC#	BUS#	WAY	WBWE# [LR1]
BOFF#	MAWEA#	WBA [SEC2#]	WRARR#

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions

Symbol	Type	Part	Name and Function
A[15:0] A[31:3]	I I/O	P CC	Pentium™ processor **Address** pins. 82491 Cache SRAM **Address** inputs. As outputs, the CPU address lines, along with the byte enables, define the physical area of memory or I/O accessed. The 82496 Cache Controller drives the inquire address to the Pentium processor on A[31:5]. Note that 82491 Cache SRAM address pin A0 is always connected to VSS.
A20M#	I	P	When the **Address bit 20 Mask** pin is asserted, the Pentium processor emulates the address wraparound at one Mbyte which occurs on the 8086. When A20M# is asserted, the Pentium processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
ADS#	I I O	CC CS P	**Address Strobe** signal from the Pentium processor to the 82491 Cache SRAMs. ADS# indicates the start of a new, valid CPU bus cycle and is functionally identical to ADSC#. The 82496 Cache Controller ADS# input is connected to the Pentium processor ADSC# output.
ADSC#	O	P	**Address Strobe** signal from the Pentium processor to the 82496 Cache Controller ADS# input. ADSC# indicates the start of a CPU cycle and is functionally identical to ADS#.
AHOLD	O I	CC P	In response to the assertion of **Address Hold**, the Pentium processor will stop driving the address lines (A[31:3]), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles. AHOLD is driven by the 82496 Cache Controller to the Pentium processor AHOLD input during back-invalidation cycles and inquire cycles.
AP	I/O I/O	CC P	**Address Parity** is driven by the Pentium processor with even parity information on all Pentium processor generated cycles in the same clock that the address is driven. Even parity is driven back to the Pentium processor during inquire cycles on this pin in the same clock as EADS# by the 82496 Cache Controller to ensure that the correct parity check status is indicated by the Pentium processor.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
APCHK#	O	P	This is the **address parity check status** pin. APCHK# is asserted two clocks after EADS# is sampled active if the Pentium processor has detected a parity error on the address bus during 82496 Cache Controller inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
APERR#	O	CC	The **Address Parity Error** output indicates that the 82496 Cache Controller has detected a CPU bus address parity error.
APIC#	O	CC	The **Advanced Programmable Interrupt Controller Address Decoding** output indicates, when active, that the current address is an APIC address (ie. 0 FE E0 00 00 to 0 FE E0 03 FF Hex).
BE# BE[7:0]#	I O	CS P	The **Byte Enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A[31:3]). One Pentium processor byte enable output, BE[7:0]#, is connected to either one or two (cache size dependent) 82491 Cache SRAM BE# input. When a 82491 Cache SRAM is configured to be a parity device, the CPU byte enables are connected to the 82491 Cache SRAM CDATA[7:4] pins (BE[7:4]# to one parity 82491 Cache SRAM, and BE[3:0]# to the other).
BGT#	I	CC	**Bus Guaranteed Transfer** is generated by the Memory Bus Controller (MBC) to indicate that it is committed to completing a given memory bus cycle. Until BGT# is active, the 82496 Cache Controller owns the cycle and may abort the cycle upon an intervening bus snoop. Once BGT# is asserted, the MBC owns the cycle, freeing the 82496 Cache Controller for other operations. BGT# shares a pin with the Configuration signal CLDRV.
BLAST#	O I	CC CS	The **Burst Last** signal indicates the end of a burst cycle when it comes together with BRDY# or BRDYC#.
BLE#	O	CC	The 82496 Cache Controller asserts **Byte Latch Enable** to latch PCD, PWT, BE0#-BE7#, CACHE# and SCYC from the CPU into an external 377-type latch. This signal is not necessary with the 82496 Cache Controller /82491 Cache SRAM secondary cache since those signals are latched into the 82496 Cache Controller and 82491 Cache SRAM devices.
BLEC#	O I	CC CS	The 82496 Cache Controller asserts **Byte Latch Enable** to the 82491 Cache SRAM to latch the Pentium processor byte enables (BE[7:0]#). If active (LOW), the 82491 Cache SRAM will latch new byte enable data upon the rising edge of CLK. If inactive (HIGH), the latch will be closed.
BOFF#	O I I	CC CS P	The **Back-Off** Pentium processor signal is driven by the 82496 Cache Controller to resolve In response to BOFF#, the Pentium processor and 82491 Cache SRAM (if driving CDATA lines to the Pentium processor) will float their buses on the next CLK. The CPU remains in bus hold until BOFF# is negated, at which time the Pentium processor restarts the aborted bus cycles.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
BP[3:2] PM/BP[1:0]	O O	P P	The **Breakpoint** pins correspond to the debug registers DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **Performance Monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of reset configured for performance monitoring (for more information, see Appendix A).
BRDY#	I I I	CC CS P	The **Burst Ready** input indicates that the 82496 Cache Controller has presented valid data on the data pins in response to a read or that the 82496 Cache Controller has accepted the Pentium processor data in response to a write request. BRDY# is generated by the Memory Bus Controller (MBC).
BRDYC#	I I	CS P	**Burst Ready Cache** is an input to the Pentium processor from the cache used for unlocked cache hit cycles and posted writes. The Pentium processor BRDYC# input is connected to the 82496 Cache Controller BRDYC1# output. The 82491 Cache SRAM BRDYC# input is connected to the 82496 Cache Controller BRDYC2# output and is used for tracking these hit and posted write cycles.
BRDYC1#	O	CC	**Burst Ready Cache 1** is output by the 82496 Cache Controller to the Pentium processor BRDYC# input during cache hit and posted cycles.
BRDYC2#	O	CC	**Burst Ready Cache 2** is output by the 82496 Cache Controller to the 82491 Cache SRAM BRDYC# input during cache hit and posted cycles.
BREQ	O	P	The **Bus Request** output indicates to the external system that the Pentium has internally generated a bus request. This signal is always driven whether or not the Pentium processor is driving its bus.
BT[3:0]	I O	CC P	The **Branch Trace Outputs** provide bits 2:0 of the branch target linear address (BT[2:0]) and the default operand size (BT3) during a branch trace message special cycle.
BUS#	O I	CC CS	The **Bus/Array Select** output of the 82496 Cache Controller multiplexes either the memory bus path or array path to the CPU bus of the 82491 Cache SRAM.
BUSCHK#	I	P	The **Bus Check** input pin allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor will vector to the machine check exception. For proper Pentium processor /82496 Cache Controller /82491 Cache SRAM operation, BUSCHK# must be asserted as detailed in Chapter 4.
CACHE#	I O	CC P	For Pentium processor-initiated cycles, the **Cache** signal indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
CADS#	O	CC	**Cache Address Strobe** is generated by the 82496 Cache Controller to request that the Memory Bus Controller execute a memory bus cycle. When active, CADS# indicates that the memory bus address (if MAOE#, MBAOE#, MALE, and MBALE are active), control, and attribute signals are valid.
CAHOLD	O	CC	82496 Cache Controller **CAHOLD** is generated by the 82496 Cache Controller to track the CPU AHOLD signal. This is useful to the MBC during warm reset (INIT), Locked sequences, and flush or write-back special cycles. CAHOLD also provides information relevant to 82496 Cache Controller built-in self-test (BIST).
CCACHE#	O	CC	82496 Cache Controller **Internal Caching Indication** is a latched version of the Pentium processor CACHE# attribute. CCACHE# indicates to the MBC how many BRDY#s it must return to the Pentium processor. If CCACHE# is inactive (HIGH), the MBC must return one BRDY#. If CCACHE# is active (LOW), the MBC must return four BRDY#s for cycles cacheable in the Pentium processor, and one for cycles not cacheable in the Pentium processor (depends upon the values of MKEN#, MRO#, and CD/C#). CCACHE# is valid with CADS# and SNPADS#.
CD/C#	O	CC	**Cache Data/Control** is driven by the 82496 Cache Controller to indicate whether a requested memory bus cycle needs data or code.
CDATA[7:0]	I/O	CS	**Cache Data** I/O pins are the 8 bits comprising the I/O data bus interface between each 82491 Cache SRAM and the Pentium processor data bus. When a 82491 Cache SRAM is configured to be a parity device, bits 3-0 are used for parity (connected to CPU DP[7:4] or DP[3:0]) and bits 7-4 are used for bit enables (connected to CPU BE[7:4]# or BE[3:0]#). For cache configurations which only require 4 CDATA pins, bits 3-0 are used.
CDTS#	O	CC	**Cache Data Strobe** indicates to the memory bus controller that the data path is ready. In read cycles, CDTS# indicates that the memory bus controller can generate the first BRDY# in the next CLK. For write cycles, CDTS# indicates that data is available on the memory bus in the next CLK. CDTS# permits independent address and data strobes for CADS# and SNPADS# cycles.
CFA[6:0] SET[10:0] TAG[11:0]	I/O I/O I/O	CC CC CC	**Configurable Address** pins of the 82496 Cache Controller are multiplexed to the Pentium processor address pins according to the 82496 Cache Controller configuration.
CFG[2:0]	I	CC	During the falling edge of RESET, **Configuration Pins 0,1, and 2** are used to configure the 82496 Cache Controller in any of five modes that determine 82496 Cache Controller /Pentium processor line ratio, cache tag size (4K-Tags or 8K-Tags) and lines per sector. CFG2 shares a pin with the 82496 Cache Controller input signal KWEND#. CFG1 shares a pin with the 82496 Cache Controller input signal SWEND#. CFG0 shares a pin with the 82496 Cache Controller input signal CNA#.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
CLDRV	I	CC	During RESET, the **Cache Low Drive Configuration** signal determines the driving strength of the connections between the 82496 Cache Controller and 82491 Cache SRAM components. CLDRV shares a pin with the 82496 Cache Controller input signal BGT#.
CLK	I I I	CC CS P	The **Clock** input provides the fundamental timing for the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM components. Its frequency is the internal operating frequency of the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, and TRST# are specified with respect to the rising edge of CLK. The clock inputs must be provided with minimal skew between devices.
CM/IO#	O	CC	**Cache Memory/IO** is driven by the 82496 Cache Controller to indicate whether a requested memory bus cycle is for memory or for I/O.
CNA#	I	CC	**Cache Next Address Enable** is driven by the memory bus controller to dynamically pipeline the 82496 Cache Controller cycles. If a cycle is pending and CNA# is given, a new CADS# is driven with the new cycle information. CNA# shares a pin with the Configuration signal CFG0.
CPCD	O	CC	82496 Cache Controller **Page Cache Disable** is a latched version of the Pentium processor PCD attribute to give the memory bus controller direct access. CPCD is valid with CADS# and SNPADS#.
CPWT	O	CC	82496 Cache Controller **Page Write-Through** is a latched version of the Pentium processor PWT attribute to give the memory bus controller direct access. CPWT is valid with CADS# and SNPADS#.
CRDY#	I I	CC CS	**Cache Memory Bus Ready** is generated by the memory bus controller to indicate to the 82496 Cache Controller and 82491 Cache SRAM that a memory bus cycle has completed and the devices should make resources available for the next cycle. The 82496 Cache Controller CRDY# input signal shares a pin with the Configuration signal SLFTST#.
CCCYC	O	CC	82496 Cache Controller **Split Cycle Indication** is a latched version of the Pentium processor SCYC attribute to give the memory bus controller direct access. CSCYC is active only for locked cycles with SCYC active, and inactive for all others. CSCYC is valid with CADS# and SNPADS#.
CW/R#	O	CC	**Cache Write/Read** is driven by the 82496 Cache Controller to indicate a requested memory bus cycle requires a read or a write.
CWAY	O	CC	**Cache Way** is driven by the 82496 Cache Controller to indicate to the memory bus controller in which cache "way" the line will be loaded during line fills or driven from during write-backs. CWAY is valid with CADS# and is used to facilitate external tracking tags.
D/C#	I O	CC P	The **Data/Code** signal is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
D[63:0]	I/O	P	These are the 64 **Data Lines** for the processor. Lines D[7:0] define the least significant byte of the data bus; lines D[63:56] define the most significant byte of the data bus. During reads, the CPU samples the data bus when BRDY# is returned. The Pentium processor Data Bus pins are distributed to each 82491 Cache SRAM .
DP[7:0]	I/O	P	These are the **Data Parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor . DP7 applies to D[63:56], DP0 applies to D[7:0]. The Pentium processor Data Parity Bus pins are distributed to each 82491 Cache SRAM configured to be a parity device. The CPU data parity pins are connected to the 82491 Cache SRAM CDATA[3:0] pins.
DRCTM#	I	CC	Memory Bus **Direct to [M] State** allows the memory bus to inform the 82496 Cache Controller of a request to skip the [E] state and move a line directly to the [M] state. DRCTM# allows the chip set to support read-for-ownership and cache-to-cache transfers (without main memory update), and is sampled when SWEND# is asserted.
EADS#	O I	CC P	The **External Address Strobe** is driven by the 82496 Cache Controller during back-invalidations or inquire cycles to maintain inclusion and indicates that a valid external address has been driven onto the Pentium processor address pins to be used for an inquire cycle.
EWBE#	O I	CC P	The Pentium processor **External Write-Back Buffer Empty** input is driven by the 82496 Cache Controller for use in Strong Write Ordering mode. EWBE#, when inactive (HIGH), indicates that a write-through cycle is posted in the 82496 Cache Controller /82491 Cache SRAM cache. When the Pentium processor generates a write, and EWBE# is sampled inactive, the Pentium will hold off all subsequent writes to all E or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# going active when the posted write receives BGT# from the MBC. When the 82496 Cache Controller is configured in weak write ordering mode, EWBE# will always be driven active (low).
FERR#	O	P	The **Floating Point Error** pin is driven active when an unmasked floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type floating point error reporting.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
FLUSH#	I I	CC P	When asserted to the Pentium processor , the **Cache Flush** signal forces the CPU to write back all modified lines in the data cache and invalidate its internal caches. A flush acknowledge special cycle will be generated by the Pentium processor indicating completion of the invalidation and write back. When asserted to the 82496 Cache Controller , **FLUSH#** causes the 82496 Cache Controller to execute a write-back to main memory of any modified cache lines and then invalidate all 82496 Cache Controller tag locations. FLUSH# also causes the 82496 Cache Controller to inquire the CPU and write-back all Pentium processor modified lines in the data cache and invalidate all cache lines. Note: For proper Pentium processor /82496 Cache Controller operation, FLUSH# must be HIGH at the falling edge of RESET.
FRCMC#	I	P	The **Functional Redundancy Checking Master/Checker** mode input is used to determine whether the Pentium processor is configured in master mode or checker mode. When using the 82496 Cache Controller /82491 Cache SRAM secondary cache, the Pentium processor must be configured as a Master Device (i.e. FRCMC#=1).
FSIOUT#	O	CC	**Flush/Sync/Initialization Output** indicates the start and end of Flush, Sync and Initialization operations.
HIGHZ#	I	CC	If active along with SLFTST#, the **High Impedance Output Configuration** signal causes the 82496 Cache Controller to float all output pins. HIGHZ# shares a pin with the 82496 Cache Controller input signal MBALE.
HIT#	O	P	The **Hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted by the processor. If the inquire cycle misses Pentium processor cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles. This signal is not used by the 82496 Cache Controller cache controller, but may be accessed by the MBC.
HITM#	I I O	CC CS P	The **Hit to a Modified Line** signal is driven by the Pentium processor to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	P	The **Bus Hold Acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor will resume driving the bus. If the Pentium processor has a bus cycle pending, it will be driven in the same clock that HLDA is deasserted.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
HOLD	I	P	In response to the **Bus Hold Request**, the Pentium processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor will maintain its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The Pentium processor will recognize HOLD during reset.
IBT	O	P	The **Instruction Branch Taken** pin is driven active (high) for one clock to indicate that a branch was taken. This output is always driven by the Pentium processor.
IERR#	O	P	The Pentium processor **Internal Error** pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. If a parity error occurs on a read from an internal array, the Pentium processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	P	This is the **Ignore Numeric Error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor will ignore any pending unmasked numeric exception and continue executing floating point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, or FSTCW, the Pentium processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is zero, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1) and the floating point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, or FSTCW, the Pentium processor will stop execution and wait for an external interrupt.
INIT	I	P	The Pentium processor **Initialization** input pin forces the Pentium processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, model specific registers, and floating point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low the Pentium processor will perform built-in self test prior to the start of program execution.
INTR	I	P	An active **Maskable Interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	O I	CC P	The Pentium processor **Invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
IPERR#	O	CC	**Internal Parity Error** is driven active for TAGRAM parity errors and for internal address path parity errors.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
IU	O	P	The **U-Pipe Instruction Complete** signal is driven active (high) for 1 clock to indicate that an instruction in the u-pipeline has completed execution. This pin is always driven by the Pentium processor.
IV	O	P	The **V-Pipe Instruction Complete** signal is driven active (high) for one clock to indicate that an instruction in the v-pipeline has completed execution. This pin is always driven by the Pentium processor.
KEN#	O I	CC P	The **Cache Enable** pin is used to determine whether the current cycle is cacheable by the CPU or not and is, consequently, used to determine cycle length. When the Pentium processor generates a cycle that can be cached (CACHE# asserted) and KEN# is returned active by the 82496 Cache Controller, the cycle will be transformed into a burst line fill cycle.
KLOCK#	O	CC	82496 Cache Controller **Cache LOCK#** is driven by the 82496 Cache Controller and indicates to the memory bus controller that a request to execute atomic read-modify-write sequences is present. KLOCK# tracks the LOCK# signal of the Pentium processor.
KWEND#	I	CC	**Cacheability Window End** is generated by the MBC to indicate to the 82496 Cache Controller that the Cacheability Window (the period during which cacheability is determined) has expired. When KWEND# is asserted, the 82496 Cache Controller latches the memory cacheability signal (MKEN#) and the Memory Read-Only Signal (MRO#), and makes determinations based on the cacheability attributes (e.g. whether a line is cacheable, is read-only, requires a replacement, or requires an allocation). KWEND# shares a pin with the Configuration signal CFG2.
LOCK#	I O	CC P	The **Bus Lock** pin indicates that the current bus cycle is locked. The Pentium processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back to back locked cycles. The LOCK# pin is driven to the 82496 Cache Controller which, in turn, drives the memory bus KLOCK# output.
LR[1:0]	O I	CC CS	The **Line Ratio 1 and 0 Optimized Interface Configuration** signals are driven by the 82496 Cache Controller to the 82491 Cache SRAM at RESET to pass along line ratio information. LR1 shares pins with the 82496 Cache Controller and 82491 Cache SRAM WBWE# signals. LR0 shares pins with the 82496 Cache Controller and 82491 Cache SRAM WBTYP signals.
M/IO#	I O	CC P	The **Memory/Input-Output** signal is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MALDRV	I	CC	During the falling edge of RESET, the 82496 Cache Controller **Memory Address Bus Low Drive Configuration** input is sampled to determine the 82496 Cache Controller's memory address bus driving strength. MALDRV shares a pin with the 82496 Cache Controller input signal SYNC#.
MALE	I	CC	**Memory Bus, Address Latch Enable** is generated by the memory bus controller to control transparent address latches (resembling 373-series TTL logic) within the 82496 Cache Controller. CADS# generates a new address at the input of the internal address latch. If MALE and MAOE# are both active, the address flows to the memory bus. When MALE becomes inactive (low), the address is latched. MALE shares a pin with the Configuration signal WWOR#.
MAOE#	I	CC	**Memory Bus Address Output Enable** is generated by the memory bus controller to control the output buffers of the 82496 Cache Controller's memory bus address latches. If MAOE# is active (low), the 82496 Cache Controller drives the memory bus address lines. If MAOE# is inactive (high), the 82496 Cache Controller's address inputs are driven to the hi-z state. Snoops are enabled only while MAOE# is inactive.
MAP	I/O	CC	**Memory Address Parity** is an input when MAOE#=1 (Snoop cycle), and indicates the address parity of the line address bits. **MAP** is an Output when MAOE#=0 (82496 Cache Controller initiated cycle), and indicates the address parity of the line address bits.
MAPERR#	O	CC	**Memory Address Parity Error** is driven active during 82496 Cache Controller snoop cycles whenever there is a memory address bus parity error.
MAWEA#	O I	CC CS	The 82496 Cache Controller asserts **Memory Bus Array Write Enable or Allocation** signal to the 82491 Cache SRAM to indicate that the data in the memory buffers should be written to the array, or that an allocation should occur.
MBALE	I	CC	82496 Cache Controller **Memory Bus Sub-Line Address Latch Enable** functions as MALE but controls only the 82496 Cache Controller sub-line addresses. MBALE is generated by the memory bus controller to control transparent address latches (resembling 373-series TTL logic) within the 82496 Cache Controller. CADS# generates a new address at the internal address latch input. If MBALE and MBAOE# are both active, the sub-line address flows to the memory bus. If MBALE becomes inactive (LOW), the sub-line address is latched. A separate subline control input is provided because the 82496 Cache Controller only provides the starting sub-line address. MBALE shares a pin with the 82496 Cache Controller Configuration signal HIGHZ#.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MBAOE#	I	CC	82496 Cache Controller **Memory Bus Sub-Line Address Output Enable** functions like MAOE# but only controls the 82496 Cache Controller sub-line addresses. If MBAOE# is active (low), the 82496 Cache Controller drives the sub-line portion of the address onto the memory bus. Otherwise, the 82496 Cache Controller's sub-line address is driven to the hi-z state. MBAOE# is also sampled during snoop cycles. If MBAOE# is sampled inactive in conjunction with SNPSTB#, snoop write back cycles begin at the sub-line address provided. If MBAOE# is sampled active with SNPSTB#, snoop write back cycles begin at sub-line address 0. A separate sub-line control input is provided because the 82496 Cache Controller only provides the starting sub-line address.
MBE#	O	CS	The 82491 Cache SRAM **Memory Byte Enable** output is a latched version of the Pentium processor byte enable outputs, BE[7:0]#. The memory cycle byte enables (MBE#) are always valid either with or one CLK after CADS#. MBE# shares a pin with the 82491 Cache SRAM Configuration pin PAR#.
MBRDY#	I	CS	In clocked memory bus mode, **Memory Bus Ready** is used to clock data into and out of the 82491 Cache SRAM . When active (LOW), MBRDY# indicates that the 82491 Cache SRAM will increment the burst counter and output or accept the next data upon the rising edge of MCLK (or MOCLK for writes, if applicable). MBRDY# is qualified by MSEL#. MBRDY# shares a pin with the 82491 Cache SRAM input signal MISTB.
MBT[3:0]	O	CC	The Memory **Branch Trace Address** signals echo the Pentium processor BT[3:0] bits which provide bits 2:0 of the branch target linear address (MBT[2:0]) and the default operand size (MBT3) during a branch trace message special cycle. MBT[3:0] must be pulled low with an external resistor for proper cache operation.
MCACHE#	O	CC	82496 Cache Controller **Internal Cacheability** is driven during read cycles to indicate whether the current cycle is potentially cacheable in the 82496 Cache Controller /82491 Cache SRAM. During write operations, MCACHE# is only active for write-back cycles. MCACHE# is inactive during I/O, special and locked cycles.
MCFA[6:0] MSET[10:0] MTAG[11:0]	I/O I/O I/O	CC CC CC	**Memory Bus Configurable address lines** **Memory bus SET number** **Memory bus TAG bits** The **Memory Address** lines are used along with the 8 MBE#s to define the areas of memory or I/O to be accessed. They are driven during normal memory bus cycles and are inputs during snoop operations.
MCLK	I	CS	**Memory Bus Clock** is the memory bus clock input to the 82491 Cache SRAM while in clocked memory bus mode. Here, memory bus signals and data are sampled on the rising edge of MCLK. During clocked memory bus writes, data is driven with respect to MCLK or MOCLK, depending on the configuration. MCLK inputs to each 82491 Cache SRAM must be within proper skew specifications. MCLK shares a pin with the Configuration signal MSTBM.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MCYC#	O I	CC CS	The 82496 Cache Controller asserts **Memory Bus Cycle** to the 82491 Cache SRAM to indicate that the current cycle will use the memory buffers.
MDATA[7:0]	I/O	CS	The **Memory Data Pins** are each 82491 Cache SRAM's data I/O pins. Together with other 82491 Cache SRAM components, they form a 64-, or 128-bit wide memory bus. In clocked memory bus mode, data is sampled or driven on MDATA[7:0] with the rising edge of MCLK when MBRDY# is active. MOCLK is used as a latch enable to hold write data on the MDATA[7:0] pins. In strobed memory bus mode, data is sampled or driven on MDATA[7:0] with MISTB, MOSTB, or MEOC# edges. For cache configurations which only require 4 MDATA pins, bits 3-0 are used.
MDLDRV	I	CS	During the falling edge of RESET, the **Memory Data Bus Low Drive Configuration** signal is sampled to indicate the memory data bus driver strength of the 82491 Cache SRAM, which offers normal (MDLDRV=HIGH) and high drive (MDLDRV=LOW) capability buffers. MDLDRV shares a pin with the 82491 Cache SRAM input signal MFRZ#.
MDOE#	I	CS	**Memory Data Output Enable** controls when the 82491 Cache SRAM drives the data onto the memory bus. When MDOE# is inactive (high), the MDATA pins are tri-stated. When MDOE# is active (low), the MDATA pins drive data. Because it is unrelated to CLK and MCLK, MDOE# functions the same during strobed and clocked memory bus operations.
MEOC#	I	CS	**Memory End of Cycle** ends the current cycle. Because it is synchronous to the memory bus clock and asynchronous to the CPU CLK, MEOC# can end a memory bus cycle and begin a new cycle without waiting for Pentium processor CLK synchronization. MEOC# also causes data to be latched or driven and resets the memory burst counter. In clocked memory bus mode, MEOC# is sampled on the rising edge of MCLK. In strobed mode, actions occur on MEOC# falling edge.
MFRZ#	I	CS	**Memory Freeze** is used during write cycles that could cause allocation cycles. When MFRZ# is sampled active (low) with MEOC#, write data is latched within the 82491 Cache SRAM. The subsequent allocation will not overwrite latched data, thereby avoiding the memory write on the memory bus. Because memory is not updated, the allocated line must be cached in the [M] state. MFRZ# shares a pin with the Configuration signal MDLDRV.
MHITM#	O	CC	**Memory Bus Hit to Modified Line** is driven during snoop cycles to indicate whether snooping addresses hit a modified cache line within the 82496 Cache Controller /82491 Cache SRAM. When snoop hits to [M] occur, the 82496 Cache Controller automatically schedules the write-back of modified lines. MHITM# is valid in the CLK following SNPCYC#. If active, MHITM# remains active until the CLK of CRDY# of the snoop write back.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MISTB	I	CS	In strobed memory bus mode, **Memory Input Strobe** is the 82491 Cache SRAM's input data strobe. On each edge of MISTB, the chip set latches data and increments the burst counter. MISTB is qualified by MSEL#. MISTB shares a pin with the 82491 Cache SRAM input signal MBRDY#.
MKEN#	I	CC	**Memory Bus Cacheability** is driven by the memory bus controller to indicate to the 82496 Cache Controller whether the current memory bus cycle is cacheable to the 82496 Cache Controller /82491 Cache SRAM cache. MKEN# is sampled when KWEND# is asserted.
MOCLK	I	CS	In clocked memory bus mode, **Memory Output Clock** controls a transparent latch at the 82491 Cache SRAM's data outputs. MDATA hold time may be increased through a clock input skewed from MCLK. MOCLK shares a pin with the 82491 Cache SRAM input signal MOSTB.
MOSTB	I	CS	In strobed memory bus mode, each edge of the **Memory Output Strobe** signal outputs new data onto the memory bus. MOSTB is qualified by MSEL#. MOSTB shares a pin with the 82491 Cache SRAM input signal MOCLK.
MRO#	I	CC	**Memory Bus Read-Only** indicates to the 82496 Cache Controller that an accessed line is READ-ONLY. For the Pentium processor, READ-ONLY code lines are cacheable in the first level cache; Read-Only data lines are not cacheable in the first level cache. READ-ONLY lines are cached in the 82496 Cache Controller in the [S] state if both MKEN# and MRO# are sampled active during KWEND#. MRO# is sampled with KWEND# assertion. Subsequent writes to Read-Only lines are not updated but instead posted to the memory system.
MSEL#	I	CS	**Memory Select** is a chip select input which provides three functions. (1) In clocked mode, MSEL# qualifies the MBRDY# 82491 Cache SRAM input. In strobed mode, MSEL# qualifies the MISTB and MOSTB inputs. (2) If MSEL# is active with MEOC#, MZBT# is sampled for the next cycle. (3) MSEL# going inactive causes the 82491 Cache SRAM 's memory burst counter to reset. Note that in clocked mode, MZBT# is sampled on every MCLK rising edge with MSEL# inactive. MSEL# shares a pin with the Configuration signal MTR4/8#.
MSET[10:0]	I/O	CC	See MCFA[6:0].
MSTBM	I	CS	The **Memory Bus Strobed Mode Configuration** signal determines whether the 82491 Cache SRAM will operate in the strobed memory bus mode or in clocked memory bus mode. If a clock is detected on this pin any time after reset, the 82491 Cache SRAM will operate in clocked mode. If this input remains stable at VSS or VCC, the 82491 Cache SRAM will operate in strobed mode. MSTBM shares a pin with the 82491 Cache SRAM input signal MCLK.
MTAG[11:0]	I/O	CC	See MCFA[6:0].

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
MTHIT#	O	CC	**Memory Bus Tag Hit** is driven by the 82496 Cache Controller during snoop cycles to indicate whether a snooping address hits an exclusive, shared, or modified cache line. MTHIT# is valid in the CLK following SNPCYC# and remains valid until the CLK of the next SNPCYC#.
MTR4/8#	I	CS	The **Memory Transfer Configuration** signal is sampled at the falling edge of RESET and determines the number of transfers needed on the memory bus for each cache line. If MTR4/8# is high, there are four transfers for each cache line; If MTR4/8# is low, there are eight transfers. MTR4/8# shares a pin with the 82491 Cache SRAM input signal MSEL#.
MWB/WT#	I	CC	**Memory Bus Write Policy** allows the memory bus to dynamically indicate to the 82496 Cache Controller whether the write policy is write-through or write-back. MWB/WT# is sampled when SWEND# becomes active. If MWB/WT# is sampled low, the tag state changes to shared (used, for example, when the line is detected in another cache). If MWB/WT# is sampled high, the tag state can change to an exclusive state.
MX4/8#	I	CS	On the falling edge of RESET, the **Memory I/O Bits Configuration** signal is sampled to determine the number of I/O pins to be used for the memory bus. If MX4/8# is HIGH, four I/O pins are used. If MX4/8# is LOW, eight I/O pins are used. MX4/8# shares a pin with the 82491 Cache SRAM input signal MZBT#.
MZBT#	I	CS	When sampled active with MSEL# inactive or MEOC# active, **Memory Zero Based Transfer** indicates that burst location zero of the memory bus cycle should be the starting sub-line address independent of the sub-line address requested by the Pentium processor. MZBT# shares a pin with the Configuration signal MX4/8#.
NA#	O I	CC P	An active **Next Address** signal indicates that the 82496 Cache Controller is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor will drive out a pending cycle two clocks after NA# is asserted. The Pentium processor supports up to 2 outstanding bus cycles.
NENE#	O	CC	**Next Near** allows the memory bus controller (MBC) to take advantage of paged or static column DRAMs by indicating whether a requested memory address is "near" the previously generated address (i.e., within the same 2K-Byte DRAM page). NENE# is valid with CADS# and undefined during SNPADS#.
NMI	I	P	The **Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PALLC#	O	CC	**Potential Allocate** indicates to the memory bus controller that the current write cycle could potentially allocate a cache line. PALLC# is active for write miss cycles in which LOCK#, PCD and PWT are inactive.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
PAR#	I	CS	The **Parity Configuration** signal, when sampled active during RESET, causes the 82491 Cache SRAM to be configured solely as a parity device. For 82491 Cache SRAM s configured as parity devices, PAR# remains tri-stated following Reset. PAR# shares a pin with the 82491 Cache SRAM output signal MBE#.
PCD	I O	CC P	The **Page Cache Disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	P	The **Parity Check** signal indicates the result of a parity check on a data read. It is driven by the Pentium processor with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	P	The **Parity Enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium processor will vector to the machine check exception before the beginning of the next instruction.
PRDY	O	P	The PRDY output pin indicates that the processor has stopped normal execution in response to the R/S# pin going inactive or Probe Mode being entered (see Appendix A for more information regarding Probe Mode). This pin is provided for use with the Intel debug port described in the *Pentium™ Processor Data Book*.
PWT	I O	CC P	The **Page Write Through** pin reflects the state of the PWT bit in CR3, the Page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external writeback indication on a page by page basis. PWT active causes the 82496 Cache Controller to put the line in 'S' state in cases of linefill regardless of the value of MWB/WT#. PWT is ignored by the 82496 Cache Controller if the line is in the cache in 'E' or 'M' state.
R/S#	I	P	The R/S# input is an asynchronous, edge sensitive input used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary. This pin is provided for use with the Intel debug port described in the *Pentium™ Processor Data Book*.
RDYSRC	O	CC	**Ready Source** indicates whether the MBC or the 82496 Cache Controller provides BRDY# to the Pentium processor . If RDYSRC is high, the memory bus controller must generate BRDY#. If RDYSRC is low, the 82496 Cache Controller generates BRDY#.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
RESET	I I I	CC CS P	**Reset** forces the Pentium processor to begin execution at a known state. All the Pentium processor internal caches will be invalidated upon the reset. Modified lines in the data cache are not written back. When asserted to the 82496 Cache Controller and 82491 Cache SRAM, the reset signal initiates cache execution at a known state. RESET going inactive causes the state of the configuration input pins to be sampled. **The following 82496 Cache Controller pins are sampled during the falling edge of RESET:** CNA#[CFG0]: CFG0 line of 82496 Cache Controller configuration inputs. SWEND#[CFG1]: CFG1 line of 82496 Cache Controller configuration inputs. KWEND#[CFG2]: CFG2 line of 82496 Cache Controller configuration inputs. BGT#[CLDRV]: Indicates the driving strength of the 82496 Cache Controller /82491 Cache SRAM interface. SYNC#[MALDRV]: Indicates the 82496 Cache Controller's memory address bus driving strength. SNPCLK[SNPMD]: Indicates whether the snoop mode is synchronous, clocked, or strobed. MALE[WWOR#]: Enforces strong or weak write-ordering consistency. CRDY#[SLFTST#]: Invokes 82496 Cache Controller self-test if HIGHZ# high. MBALE[HIGHZ#]: Tristates 82496 Cache Controller outputs if active with SLFTST#. Note: For proper Pentium processor/82496 Cache Controller operation, 82496 Cache Controller FLUSH# must be HIGH at the falling edge of RESET. **The following 82491 Cache SRAM pins are sampled during the falling edge of RESET:** MZBT#[MX4/8#]: Determines whether each 82491 Cache SRAM uses four or eight I/O pins on the memory bus. MSEL#[MTR4/8#]: Determines the number of memory bus transfers needed to fill each cache line - four transfers if HIGH, eight if LOW. MCLK[MSTBM]: Indicates the memory bus configuration - strobed if stable (high or low), clocked if toggling. MFRZ#[MDLDRV]: Indicates the 82491 Cache SRAM 's memory data bus driving strength. MBE# [PAR#]: Configures the 82491 Cache SRAM as a parity storage device. WBA[SEC2#]: Configures the 82491 Cache SRAM to be 2 Lines per Sector. WBTYP[LR0]: Line Ratio information, bit 0. WBWE#[LR1]: Line Ration information, bit 1.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
			The following Pentium processor pins are sampled during the falling edge of RESET: BUSCHK#, BRDYC#, CLRDRV: used to configure I/O buffers. FLUSH#, FRCMC# and INIT: sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if BIST will be run.
SCYC	I O	CC P	The **Split Cycle** signal is asserted during misaligned LOCK transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SEC2#	O I	CC CS	The 82496 Cache Controller drives the **2 lines per sector Optimized Interface Configuration** signal during RESET to the 82491 Cache SRAM to pass along lines/sector information. If active, SEC2# indicates 2 lines per sector. SEC2# shares pins with the 82496 Cache Controller and 82491 Cache SRAM WBA signals.
SET[10:0]	I/O	CC	See CFA[6:0].
SLFTST#	I	CC	If the **82496 Cache Controller Self Test Configuration** signal is sampled LOW (active) during the falling edge of RESET while MBALE is HIGH (active), 82496 Cache Controller self-test is invoked. SLFTST# shares a pin with the 82496 Cache Controller input signal CRDY#.
SMI#	I	P	The **System Management Interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	P	An active **System Management Interrupt Active** signal indicates that the processor is operating in System Management Mode (SMM).
SMLN#	O	CC	**Same Cache Line** indicates to the memory bus controller that the current cycle accesses the same 82496 Cache Controller line as the previous memory (not I/O) cycle. SMLN# is valid together with CADS# and can be used to selectively activate SNPSTB# for other caches. For example, SMLN# can prevent consecutive snoops to the same line.
SNPADS#	O	CC	**Cache Snoop Address Strobe** functions exactly like CADS# but is generated only on snoop write-back cycles. Because snoop write-back cycles must be immediately serviced on the memory bus, the separate address strobe eases memory bus controller (MBC) implementation. When SNPADS# is active, the MBC aborts all pending cycles (ie. those for which BGT# has not been issued; after BGT#, snoop lookups are delayed). The 82496 Cache Controller may re-issue cycles following snoop completion.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
SNPBSY#	O	CC	When active (LOW), **Snoop Busy** indicates that the 82496 Cache Controller will latch the snoop address and attributes, but will delay the snoop lookup. SNPBSY# is activated when a snoop hits a modified line or when back-invalidation is needed for a snoop in progress. The 82496 Cache Controller does not perform snoop lookups until SNPBSY# is deactivated.
SNPCLK	I	CC	**Snoop Clock** provides the 82496 Cache Controller with a snoop clock so the MBC can snoop at its own rate. During clocked mode, SNPSTB#, SNPINV, SNPNCA, MBAOE#, MAOE#, MAP, and all Address lines are sampled by SNPCLK. SNPCLK shares a pin with the Configuration signal SNPMD.
SNPCYC#	O	CC	**Snoop Cycle** indicates when a snoop lookup is occurring within the 82496 Cache Controller TAGRAM. MHITM# and MTHIT# are valid from the clock following SNPCYC#.
SNPINV	I	CC	**Snoop Invalidation** is sampled with SNPSTB# and indicates the state of a cache line following snoop hit cycle. If active, SNPINV forces the line to become invalid.
SNPMD	I	CC	When HIGH during RESET, the **Snoop Mode Configuration** signal indicates strobed snooping mode. If LOW during reset, SNPMD indicates synchronous snooping mode. In clocked snooping mode, SNPMD is connected to the snoop clock source. SNPMD shares a pin with the 82496 Cache Controller input signal SNPCLK.
SNPNCA	I	CC	**Snoop Non Caching Device Access** is sampled with SNPSTB# and indicates to the 82496 Cache Controller whether a bus master is a non caching device (e.g. a DMA controller). SNPNCA helps prevent the 82496 Cache Controller from unnecessarily changing cache line states from exclusive or modified to shared.
SNPSTB#	I	CC	**Snoop Strobe** causes snoop address and parameters to be latched and initiates a snoop. The 82496 Cache Controller supports three latching modes: Clocked, Strobed, and Synchronous latching modes. In clocked mode, address and attribute signals are latched when SNPSTB# becomes active with the rising edge of SNPCLK. In strobed mode, addresses and attributes are latched at the falling edge of SNPSTB#. In synchronous mode, address and attribute signals are latched when SNPSTB# becomes active with the rising edge of CLK.
SWEND#	I	CC	**Snoop Window End** is generated by the memory bus controller to indicate that the Snoop Window has expired. When SWEND# is asserted, the 82496 Cache Controller latches the Write Policy (MWB/WT#) and Direct to Memory Transfer (DRCTM#) attributes. By the end of the window, all devices have snooped the bus master address and generated the snoop results. Once a cycle has received BGT#, the 82496 Cache Controller prevents snooping until it receives SWEND#. The 82496 Cache Controller can then update its tag RAM. SWEND# shares a pin with the Configuration signal CFG1.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
SYNC#	I	CC	The **Synchronize Pentium processor CPU Cache Chip Set** signal synchronizes the 82496 Cache Controller /82491 Cache SRAM tag array with main memory. All modified cache lines in the 82496 Cache Controller /82491 Cache SRAM are written back to main memory. SYNC# differs from FLUSH# in that it doesn't invalidate the 82496 Cache Controller or Pentium processor tag array. All E,I, and S state lines remain in the E,I, and S states. All modified cache lines (M state) cause the 82496 Cache Controller to inquire the CPU (the Pentium processor will write back 'M' state data to the 82496 Cache Controller /82491 Cache SRAM) and become non-modified (E state) by writing modified data to the memory bus. SYNC# shares a pin with the Configuration signal MALDRV.
TAG[11:0]	I/O	CC	See CFA[6:0].
TCK	I I I	CC CS P	The **Testability Clock** input provides the clocking function for the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM boundary scan in accordance with the JTAG/Boundary Scan interface (IEEE Std 1149.1). It is used to clock state information and data into and out of the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM during boundary scan.
TDI	I I I	CC CS P	The **Test Data Input** is a serial input pin for the test logic. TAP instructions and data are shifted into the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM components on the TDI input pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O O O	CC CS P	The **Test Data Output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM on the TDO pin on the falling edge of TCK when the TAP controller is in the appropriate state.
TMS	I I I	CC CS P	The value of the **Test Mode Select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes for the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM components.
TRST#	I I	CC P	The **Test Reset** pin. When asserted, it allows the TAP controller to be asynchronously initialized.
W/R#	I I O	CC CS P	**Write/Read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WAY	O I	CC CS	The 82496 Cache Controller **Way** indication is used by the 82491 Cache SRAM to properly load and store buffers as well as update the MRU bit.
WB/WT#	O I	CC P	The **WriteBack/WriteThrough** signal allows a Pentium processor data cache line to be defined as write back or write through on a line by line basis. As a result, it determines whether a cache line is initially in the S or E state in the CPU data cache. This signal provides the L1/L2 cache consistency protocol. NOTE: the 82496 Cache Controller forces the Pentium processor into a write-once mode in order to maintain Modified data inclusion and assure cache consistency.

Table 1-10. Pentium™ Processor CPU-Cache Chip Set Brief Pin Descriptions (Contd.)

Symbol	Type	Part	Name and Function
WBA	O I	CC CS	The **Write back Buffer Address** pin is driven by the 82496 Cache Controller to indicate which line is loaded into the write-back buffer by the 82491 Cache SRAM for replacement write-backs. For snoop write-backs, WBA indicates a snoop hit to the write-back buffer. WBA shares a pin with the Optimized Interface Configuration signal SEC2#
WBTYP	O I	CC CS	The 82496 Cache Controller **Write Back Cycle Type** pin is driven to the 82491 Cache SRAM to indicate a replacement write-back or snoop write-back cycle. WBTYP shares a pin with the Optimized Interface Configuration signal LR0.
WBWE#	0 I	CC CS	The 82496 Cache Controller **Write-Back Buffer Write Enable** pin is used in conjunction with the WBA and WBTYP pins to load the write-back buffers of the 82491 Cache SRAM. WBWE# shares a pin with the Optimized Interface Configuration signal LR1.
WRARR#	O I	CC CS	The 82496 Cache Controller **Write to 82491 Cache SRAM Array** signal controls the writing of data into the 82491 Cache SRAM array and updating of the MRU bit.
WWOR#	I	CC	The **Weak Write Ordering Configuration** signal configures the 82496 Cache Controller into strong or weak write ordering modes. In strong ordering mode, the chip set writes data to memory in the order in which it was received from the Pentium processor. WWOR# shares a pin with the 82496 Cache Controller input signal MALE.

Table 1-11. Pentium™ Processor CPU-Cache Chip Set Internal Pull-Up Resistors

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
BUSCHK#	ADS#	ADS#
R/S#	BGT#	BOFF#
SMI#	CNA#	HITM#
TCK	DRCTM#	MBE#
TDI	FLUSH#	MCLK
TMS	KWEND#	MFRZ#
TRST#	MRO#	MOCLK
	NA#	MZBT#
	SNPCLK	TCK
	SNPSTB#	TDI
	SWEND#	TMS
	SYNC#	
	TCK	
	TDI	
	TMS	
	TRST#	

NOTE: Internal pull-up resistor values are approximately 25K to 100K ohms.

Table 1-12. Pentium™ Processor CPU-Cache Chip Set Internal Pull-Down Resistors

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
none	none	BLEC#

Table 1-13. Pentium™ Processor CPU-Cache Chip Set Glitch Free Pins

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
APCHK#	APERR#	MISTB#[2]
FERR#	CADS#	MOSTB#[2]
HLDA	CDTS#	MEOC#[2]
IERR#	IPERR#	MSEL#[2]
LOCK#	KLOCK#	MZBT#[2]
PCHK#	MAPERR#	
	SNPADS#	
	SNPCYC#	

NOTES:

1. Glitch Free pins are always at a valid logic level following RESET.
2. These signals must be glitch free when the C8C is configured in strobed memory bus mode.

Table 1-14. Signal Interconnects on Optimized Interface

Pentium™ Processor	82496 Cache Controller			82491 Cache SRAM		
(I/O)	**256KB:**	(I/O)	**512KB:**	**256KB:**	(I/O)	**512KB:**
VSS	--		--	A0		--
VSS	CFA5		CFA4	A1		A0
A[4:3]	CFA[1:0]		CFA[1:0]	A[3:2]		A[2:1]
A5	CFA6		CFA5	A4		A3
A6	SET0		CFA6	A5		A4
A[16:7]	SET[10:1]		SET[9:0]	A[15:6]		A[14:5]
A17	TAG0		SET10			A15
A[28:18]	TAG[11:1]		TAG[10:0]			
A29	CFA2		TAG 11			
A30	CFA3		CFA2			
A31	CFA4		CFA3			
ADS# (O)				ADS# (I)		
ADSC# (O)	ADS# (I)					
AHOLD (I)	AHOLD (O)					
AP (I/O)	AP (I/O)					
BE[7:0]# (O)				BE# (I), CDATA[7:4] (I) *		
	BLAST# (O)			BLAST# (I)		
	BLEC# (O)			BLEC# (I)		
BOFF# (I)	BOFF# (O)			BOFF# (I)		
BRDYC# (I)	BRDYC1# (O)					
	BRDYC2# (O)			BRDYC# (I)		
BT[3:0] (I/O)	BT[3:0] (I/O)					
	BUS# (O)			BUS# (I)		
CACHE# (O)	CACHE# (I)					
D[63:0] (I/O)				CDATA[7:0] (I/O)		
D/C# (O)	D/C# (I)					
DP[7:0] (I/O)				CDATA[3:0] (I/O) *		
EADS# (I)	EADS# (O)					
EWBE# (I)	EWBE# (O)					

Table 1-14. Signal Interconnects on Optimized Interface (Contd.)

Pentium™ Processor	82496 Cache Controller	82491 Cache SRAM
HITM# (O)	HITM# (I)	HITM# (I)
INV (I)	INV (O)	
KEN# (I)	KEN# (O)	
LOCK# (O)	LOCK# (I)	
M/IO# (O)	M/IO# (I)	
	MAWEA# (O)	MAWEA# (I)
	MCYC# (O)	MCYC# (I)
NA# (I)	NA# (O)	
PCD (O)	PCD (I)	
PWT (O)	PWT (I)	
SCYC (O)	SCYC (I)	
W/R# (O)	W/R# (I)	W/R# (I)
	WAY (O)	WAY (I)
WB/WT# (I)	WB/WT# (O)	
	WBA [SEC2#] (O)	WBA [SEC2#] (I)
	WBTYP [LR0] (O)	WBTYP [LR0] (I)
	WBWE# [LR1] (O)	WBWE# [LR1] (I)
	WRARR# (O)	WRARR# (I)

* The Pentium processor Byte Enable outputs are connected to 82491 Cache SRAM CDATA[7:4] pins for 82491 Cache SRAM s configured to be data parity devices. The Pentium processor Data Parity signals are connected to 82491 Cache SRAM CDATA[3:0] pins for 82491 Cache SRAM s configured to be parity devices.

Table 1-15. Pin States During RESET

Pin Name	Part	State During RESET
APCHK#	Pentium™ processor	High
APERR#	82496 Cache Controller	High
APIC#	82496 Cache Controller	Undefined
BLE#	82496 Cache Controller	Low
BP[3:2],	Pentium processor	Low
BP/PM[1:0]		
BREQ	Pentium processor	Low
BT[3:0]	Pentium processor	Low
CADS#	82496 Cache Controller	High
CAHOLD	82496 Cache Controller	Note 1
CCACHE#	82496 Cache Controller	Undefined
CD/C#	82496 Cache Controller	Undefined
CDTS#	82496 Cache Controller	High
CM/IO#	82496 Cache Controller	Undefined
CPCD .	82496 Cache Controller	Undefined
CPWT	82496 Cache Controller	Undefined
CSCYC	82496 Cache Controller	Undefined
CW/R#	82496 Cache Controller	Undefined
CWAY	82496 Cache Controller	Undefined
FERR#	Pentium processor	High
FSIOUT#	82496 Cache Controller	Low
HIT#	Pentium processor	High
HLDA	Pentium processor	Low
IBT	Pentium processor	Low
IERR#	Pentium processor	High
IPERR#	82496 Cache Controller	High

Pin Name	Part	State During RESET
IU	Pentium processor	Low
IV	Pentium processor	Low
KLOCK#	82496 Cache Controller	High
MAP	82496 Cache Controller	Undefined
MAPERR#	82496 Cache Controller	High
MBT[3:0]	82496 Cache Controller	Low
MCACHE#	82496 Cache Controller	Undefined
MCFA[6:0]	82496 Cache Controller	Undefined
MDATA[7:0]	82491 Cache SRAM	High-Z
MHITM#	82496 Cache Controller	High
MSET[10:0]	82496 Cache Controller	Undefined
MTAG[11:0]	82496 Cache Controller	Undefined
MTHIT#	82496 Cache Controller	High
NENE#	82496 Cache Controller	Undefined
PALLC#	82496 Cache Controller	Undefined
PCHK#	Pentium processor	High
PRDY	Pentium processor	Low
RDYSRC	82496 Cache Controller	Undefined
SMIACT#	Pentium processor	High
SMLN#	82496 Cache Controller	Undefined
SNPADS#	82496 Cache Controller	High
SNPBSY#	82496 Cache Controller	Low
SNPCYC#	82496 Cache Controller	High
TDO	Pentium processor	Note 2
	82496 Cache Controller	
	82491 Cache SRAM	

NOTES:

1. The state of CAHOLD depends upon whether self-test is selected.
2. The state of TDO is determined by boundary scan which is independent of all other signals including RESET.

Note that "Undefined" does not mean that the signal is floating. It means that the value being driven during RESET will vary.

Table 1-16. Pentium™ Processor CPU-Cache Chip Set Output Pins

Pin Name	Component	Active Level	Synchronous / Asynchronous	When Floated
ADS#	Pentium™ processor	Low	Synchronous to CLK	Bus Hold, BOFF#
ADSC#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
AHOLD	82496 Cache Controller	High	Synchronous to CLK	—
APCHK#	Pentium processor	Low	Synchronous to CLK	—
APERR#	82496 Cache Controller	Low	Synchronous to CLK	—
APIC#	82496 Cache Controller	Low	Synchronous to CLK	—
BE[7:0]#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
BLAST#	82496 Cache Controller	Low	Synchronous to CLK	—
BLE#	82496 Cache Controller	—	Synchronous to CLK	—
BLEC#	82496 Cache Controller	—	Synchronous to CLK	—
BOFF#	82496 Cache Controller	Low	Synchronous to CLK	—
BP[3:2], PM/BP[1:0]	Pentium processor		Synchronous to CLK	—
BRDYC1#	82496 Cache Controller	Low	Synchronous to CLK	—
BRDYC2#	82496 Cache Controller	Low	Synchronous to CLK	—
BREQ	Pentium processor	High	Synchronous to CLK	—
BT[3:0]	Pentium processor	—	Synchronous to CLK	Address Hold, Bus Hold, BOFF#
BUS#	82496 Cache Controller	Low	Synchronous to CLK	—
CACHE#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
CADS#	82496 Cache Controller	Low	Synchronous to CLK	—
CAHOLD	82496 Cache Controller	High	Synchronous to CLK	—
CCACHE#	82496 Cache Controller	Low	Synchronous to CLK	—
CD/C#	82496 Cache Controller	—	Synchronous to CLK	—
CDTS#	82496 Cache Controller	Low	Synchronous to CLK	—
CM/IO#	82496 Cache Controller	—	Synchronous to CLK	—
CPCD	82496 Cache Controller	High	Synchronous to CLK	—
CPWT	82496 Cache Controller	High	Synchronous to CLK	—
CSCYC	82496 Cache Controller	High	Synchronous to CLK	—

Table 1-16. Pentium™ Processor CPU-Cache Chip Set Output Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous	When Floated
CW/R#	82496 Cache Controller	—	Synchronous to CLK	—
CWAY	82496 Cache Controller	—	Synchronous to CLK	—
D/C#	Pentium processor	—	Synchronous to CLK	Bus Hold, BOFF#
EADS#	82496 Cache Controller	Low	Synchronous to CLK	—
EWBE#	82496 Cache Controller	Low	Synchronous to CLK	—
FERR#	Pentium processor	Low	Synchronous to CLK	—
FSIOUT#	82496 Cache Controller	Low	Synchronous to CLK	—
HIT#	Pentium processor	Low	Synchronous to CLK	—
HITM#	Pentium processor	Low	Synchronous to CLK	—
HLDA	Pentium processor	High	Synchronous to CLK	—
IBT	Pentium processor	High	Asynchronous	—
IERR#	Pentium processor	Low	Synchronous to CLK	—
INV	82496 Cache Controller	High	Synchronous to CLK	—
IPR#	82496 Cache Controller	Low	Synchronous to CLK	—
IU	Pentium processor	High	Synchronous to CLK	—
IV	Pentium processor	High	Synchronous to CLK	—
KEN#	82496 Cache Controller	Low	Synchronous to CLK	—
KLOCK#	82496 Cache Controller	Low	Synchronous to CLK	—
LOCK#	Pentium processor	Low	Synchronous to CLK	Bus Hold, BOFF#
M/IO#	Pentium processor	—	Synchronous to CLK	Bus Hold, BOFF#
MAPERR#	82496 Cache Controller	Low	Synchronous to CLK	—
MAWEA#	82496 Cache Controller	Low	Synchronous to CLK	—
MBE#	82491 Cache SRAM	Low	Synchronous to CLK	Reset to first CADS#
MBT[3:0]	82496 Cache Controller	—	Synchronous to CLK	MAOE# inactive
MCACHE#	82496 Cache Controller	Low	Synchronous to CLK	—
MCYC#	82496 Cache Controller	Low	Synchronous to CLK	—
MHITM#	82496 Cache Controller	Low	Synchronous to CLK	—
MTHIT#	82496 Cache Controller	Low	Synchronous to CLK	—

Table 1-16. Pentium™ Processor CPU-Cache Chip Set Output Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous	When Floated
NA#	82496 Cache Controller	Low	Synchronous to CLK	—
NENE#	82496 Cache Controller	Low	Synchronous to CLK	—
PALLC#	82496 Cache Controller	Low	Synchronous to CLK	—
PCD	Pentium processor	High	Synchronous to CLK	Bus Hold, BOFF#
PCHK#	Pentium processor	Low	Synchronous to CLK	—
PRDY	Pentium processor	High	Synchronous to CLK	—
PWT	Pentium processor	High	Synchronous to CLK	Bus Hold, BOFF#
RDYSRC	82496 Cache Controller	—	Synchronous to CLK	
SCYC	Pentium processor	High	Synchronous to CLK	Bus Hold, BOFF#
SMIACT#	Pentium processor	Low	Asynchronous	—
SMLN#	82496 Cache Controller	Low	Synchronous to CLK	—
SNPADS#	82496 Cache Controller	Low	Synchronous to CLK	—
SNPBSY#	82496 Cache Controller	Low	Synchronous to CLK	—
SNPCYC#	82496 Cache Controller	Low	Synchronous to CLK	—
TDO	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	—	Synchronous to TCK	All states except Shift-DR and Shift IR
W/R#	Pentium processor	—	Synchronous to CLK	Bus Hold, BOFF#
WAY	82496 Cache Controller	—	Synchronous to CLK	—
WB/WT#	82496 Cache Controller	—	Synchronous to CLK	—
WBA [SEC2#]	82496 Cache Controller	—	Synchronous to CLK	—
WBTYP [LR0]	82496 Cache Controller	—	Synchronous to CLK	—
WBWE# [LR1]	82496 Cache Controller	Low	Synchronous to CLK	—
WRARR#	82496 Cache Controller	Low	Synchronous to CLK	—

Table 1-17. Pentium™ Processor CPU-Cache Chip Set Input Pins

Pin Name	Component	Active Level	Synchronous / Asynchronous
A[15:0]	82491 Cache SRAM	—	Synchronous to CLK
A20M#	Pentium™ processor	Low	Asynchronous
ADS#	82491 Cache SRAM	Low	Synchronous to CLK
ADSC#	82496 Cache Controller	Low	Synchronous to CLK
AHOLD	Pentium processor	High	Synchronous to CLK
BE#	82491 Cache SRAM	Low	Synchronous to CLK
BGT# [CLDRV]	82496 Cache Controller	Low [—]	Synchronous to CLK
BLAST#	82491 Cache SRAM	Low	Synchronous to CLK
BLEC#	82491 Cache SRAM	Low	Synchronous to CLK
BOFF#	Pentium processor, 82491 Cache SRAM	Low	Synchronous to CLK
BRDY#	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	Low	Synchronous to CLK
BRDYC#	Pentium processor, 82491 Cache SRAM	Low	Synchronous to CLK
BT[3:0]	82496 Cache Controller	—	Synchronous to CLK
BUS#	82491 Cache SRAM	Low	Synchronous to CLK
BUSCHK#	Pentium processor	Low	Synchronous to CLK
CACHE#	82496 Cache Controller	Low	Synchronous to CLK
CLK	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	—	n/a
CNA# [CFG0]	82496 Cache Controller	Low [—]	Synchronous to CLK
CRDY# [SLFTST#]	82496 Cache Controller, 82491 Cache SRAM [CC]	Low [Low]	Synchronous to CLK
D/C#	82496 Cache Controller	—	Synchronous to CLK
DRCTM#	82496 Cache Controller	Low	Synchronous to CLK (Note 1)
EADS#	Pentium processor	Low	Synchronous to CLK
EWBE#	Pentium processor	Low	Synchronous to CLK

Table 1-17. Pentium™ Processor CPU-Cache Chip Set Input Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous
FLUSH#	Pentium processor, 82496 Cache Controller	Low	Asynchronous
FRCMC#	Pentium processor	Low	Asynchronous
HITM#	82496 Cache Controller, 82491 Cache SRAM	Low	Synchronous to CLK
HOLD	Pentium processor	High	Synchronous to CLK
IGNNE#	Pentium processor	Low	Asynchronous
INIT	Pentium processor	High	Asynchronous
INTR	Pentium processor	High	Asynchronous
INV	Pentium processor	High	Synchronous to CLK
KEN#	Pentium processor	Low	Synchronous to CLK
KWEND# [CFG2]	82496 Cache Controller	Low [—]	Synchronous to CLK
LOCK#	82496 Cache Controller	Low	Synchronous to CLK
M/IO#	82496 Cache Controller	—	Synchronous to CLK
MALE [WWOR#]	82496 Cache Controller	High [Low]	Asynchronous [Synchronous to CLK]
MAOE#	82496 Cache Controller	Low	Asynchronous (Note 2)
MAWEA#	82491 Cache SRAM	Low	Synchronous to CLK
MBALE [HIGHZ#]	82496 Cache Controller	High [Low]	Asynchronous [Synchronous to CLK]
MBAOE#	82496 Cache Controller	Low	Asynchronous (Note 2)
MBRDY#	82491 Cache SRAM	Low	Synchronous to MCLK
MCLK [MSTBM]	82491 Cache SRAM	— [—]	n/a [Synchronous to CLK]
MCYC#	82491 Cache SRAM	Low	Synchronous to CLK
MDOE#	82491 Cache SRAM	Low	Asynchronous
MEOC#	82491 Cache SRAM	Low	Synchronous to MCLK or Asynchronous
MFRZ# [MDLDRV]	82491 Cache SRAM	Low [—]	Synchronous to MCLK or Asynchronous [Synchronous to CLK]
MISTB	82491 Cache SRAM	Transition	Asynchronous
MKEN#	82496 Cache Controller	Low	Synchronous to CLK (Note 1)

Table 1-17. Pentium™ Processor CPU-Cache Chip Set Input Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous
MOCLK	82491 Cache SRAM	—	n/a
MOSTB	82491 Cache SRAM	Transition	Asynchronous
MRO#	82496 Cache Controller	Low	Synchronous to CLK (Note 1)
MSEL# [MTR4/8#]	82491 Cache SRAM	Low [—]	Synchronous to MCLK or Asynchronous [Synchronous to CLK]
MWB/WT#	82496 Cache Controller	—	Synchronous to CLK (Note 1)
MZBT# [MX4/8#]	82491 Cache SRAM	Low [—]	Synchronous to MCLK or Asynchronous [Synchronous to CLK]
NA#	Pentium processor	Low	Synchronous to CLK
NMI	Pentium processor	High	Asynchronous
PAR# (Note 3)	82491 Cache SRAM	Low	Synchronous to CLK
PCD	82496 Cache Controller	High	Synchronous to CLK
PWT	82496 Cache Controller	High	Synchronous to CLK
PEN#	Pentium processor	Low	Synchronous to CLK
R/S#	Pentium processor	—	Asynchronous
RESET	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	High	Asynchronous
SCYC	82496 Cache Controller	High	Synchronous to CLK
SMI#	Pentium processor	Low	Asynchronous
SNPCLK [SNPMD]	82496 Cache Controller	— [—]	n/a [Synchronous to CLK]
SNPINV	82496 Cache Controller	High	Note 2
SNPNCA	82496 Cache Controller	High	Note 2
SNPSTB#	82496 Cache Controller	Low	Note 2
SWEND# [CFG1]	82496 Cache Controller	Low [—]	Synchronous to CLK
SYNC# [MALDRV]	82496 Cache Controller	Low [—]	Asynchronous [Synchronous to CLK]
TCK	Pentium processor, 82496 Cache Controller 82491 Cache SRAM	—	n/a
TDI	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM	—	Synchronous to TCK
TMS	Pentium processor, 82496 Cache Controller 82491 Cache SRAM	—	Synchronous to TCK

Table 1-17. Pentium™ Processor CPU-Cache Chip Set Input Pins (Contd.)

Pin Name	Component	Active Level	Synchronous / Asynchronous
TRST#	Pentium processor, 82496 Cache Controller	Low	Asynchronous
W/R#	82496 Cache Controller, 82491 Cache SRAM	—	Synchronous to CLK
WAY	82491 Cache SRAM	—	Synchronous to CLK
WB/WT#	Pentium processor	—	Synchronous to CLK
WBA [SEC2#]	82491 Cache SRAM	—[—]	Synchronous to CLK
WBTYP [LR0]	82491 Cache SRAM	— [—]	Synchronous to CLK
WBWE# [LR1]	82491 Cache SRAM	Low [—]	Synchronous to CLK
WRARR#	82491 Cache SRAM	Low	Synchronous to CLK

NOTES:

1. DRCTM# and MWB/WT# must be synchronous to CLK while SWEND# is active. MKEN# and MRO# must be synchronous to CLK when KWEND# is active.
2. SNPSTB# is Synchronous to CLK in Synchronous snoop mode, Synchronous to SNPCLK in Clocked snoop mode, and Asynchronous in Strobed snoop mode. MAOE#, MBAOE#, SNPINV, and SNPNCA are sampled with SNPSTB#.
3. PAR# is a configuration input which shares a pin with the MBE# output signal.

Table 1-18. Pentium™ Processor CPU-Cache Chip Set Input/Output Pins

Pin Name	Component	Synchronous / Asynchronous	When Floated
A[31:3]	Pentium™ processor	Synchronous to CLK	Address Hold, Bus Hold, BOFF#, Note 3
AP	Pentium processor, 82496 Cache Controller	Synchronous to CLK	Address Hold, Bus Hold, BOFF#, Note 3
CDATA[7:0]	82491 Cache SRAM	Synchronous to CLK	RESET, BOFF#, see conditions 1,2 below (Note #5)
CFA[6:0], SET[10:0], TAG[11:0]	82496 Cache Controller	Synchronous to CLK	—
D[63:0]	Pentium processor	Synchronous to CLK	Bus Hold, BOFF#
DP[7:0]	Pentium processor	Synchronous to CLK	Bus Hold, BOFF#
MAP	82496 Cache Controller	Note 1	MAOE# inactive
MCFA[6:0], MSET[10:0], MTAG[11:0]	82496 Cache Controller	Note 1	MAOE# or MBAOE# inactive, Note 4
MDATA[7:0]	82491 Cache SRAM	Note 2	RESET, BOFF#, MDOE# inactive

NOTES:

1. When inputs: Synchronous to CLK, SNPCLK or SNPSTB#. When outputs: Synchronous to CLK, MAOE# active and MALE high.
2. Synchronous to CLK, MCLK, MOCLK or Asynchronous (MISTB/MOSTB).
3. The 82496 Cache Controller always asserts AHOLD to the Pentium processor (to float the CPU address signals) prior to BOFF# assertion (to float the 82491 Cache SRAM data signals). Technically, therefore, the BOFF# signal does not cause the Address lines to float since they have already been floated with AHOLD.
4. The specific 82496 Cache Controller address signals floated with MAOE# or MBAOE# are configuration dependant (refer to section 4.2.7).
5. The following conditions also cause the Cache SRAM CDATA[7:0] outputs to be tristated:
   (a) A write cycle on the memory bus
   (b) After the last BLAST#/BRDY# of a read cycle

Note that the appropriate signals on the CPU bus are floated in the CLK after either BOFF# or AHOLD is asserted.

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2

Cache Architecture Overview

CHAPTER 2
CACHE ARCHITECTURE OVERVIEW

The Pentium processor CPU-Cache Chip Set is Intel's next generation high-performance CPU/Cache Core solution for servers and high-end desktop systems.

The 82496 Cache Controller/82491 Cache SRAM second level cache solution is an enhanced version of the 82495DX/82490DX cache which was designed for use with the 50-MHz Intel486™ DX microprocessor. The 82496 Cache Controller provide the enhancements needed to support the Pentium processor's features.

The Pentium processor CPU Cache Chip Set is comprised of a Pentium processor, a 82496 cache controller and a variable number of 82491 Cache SRAMs for a 256K or 512K byte second level cache size. The chip set provides zero-wait-state operation on the CPU bus and can be interfaced to a memory bus of 32, 64 or 128 bits in size using a variety of memory bus protocols. (A 32-bit memory bus is an implementation alternative, 64 and 128 bits are selectable configurations.)

The 82496 Cache Controller is a high-performance write-back/write-through cache controller providing integrated tags and comparators and implementing the popular high performance MESI cache consistency protocol.

The 82491 Cache SRAM is a high-performance dual-ported custom SRAM supporting 32, 64, and 128-byte line sizes and optional sectoring. The tightly coupled 82496/82491 Cache SRAM interface is optimized for speed and concurrency. The 82496 Cache Controller/82491 Cache SRAM separates the Intel Pentium processor bus from the memory bus. The 82496 Cache controller and memory bus can handshake synchronously, asynchronously, or with a strobed protocol. The Pentium processor CPU Cache Chip Set interface allows for concurrent CPU bus and memory bus operation.

The Pentium processor CPU Cache Chip Set operates at either 60 MHz or 66 MHz. The Pentium processor is implemented in a 273 pin ceramic PGA package. The 82496 Cache Controller is implemented in a 280 pin ceramic PGA package. The 82491 Cache SRAM is implemented in an 84 lead PQFP package.

2.1. MAIN FEATURES

The 82496 Cache Controller/82491 Cache SRAM have the following main fetaures:

- Tracking of Pentium processor speed
- Large Cache Size support:
  - 4K or 8K Tags
  - 1 or 2 lines per sector
  - 4 or 8 transactions per line
  - 64 or 128-bit wide configurable memory bus
  - elementary 32-bit memory bus implementation
  - 256K or 512K byte cache
- Write-Back cache design with full multiprocessing consistency support:
  - supports the MESI protocol
  - monitors memory bus to ensure cache consistency
  - maintains inclusion with CPU cache
  - may be used as a write-through cache
  - allows write-allocations
- Two-way set-associative with MRU hit prediction and replacement algorithm
- Zero wait-state read hit cycles on MRU hit. One wait-state read hit on MRU misses
- Zero wait-state write hit cycles
- Concurrent CPU and Memory Bus transactions
- Support of synchronous, asynchronous, and strobed memory bus architectures
- Support of write posting
- Support of weak or strong memory write ordering
- Address parity checking and error notification on CPU and memory bus
- Internal tagRAM and address path parity checking and error notification
- Data parity storage and transfer to CPU bus via 82491 Cache SRAM parity devices

2.2. CPU/CACHE CORE DESCRIPTION

2.2.1. 82496 Cache Controller

The 82496 Cache Controller is the main control unit for the 82496 Cache Controller/82491 Cache SRAM second-level cache subsystem (see Figure 2-1). The 82496 Cache Controller contains tags, line states, and read-only information, and determines cache hits and misses. The controller handles all CPU request traffic including requests for memory bus access. The

82496 Cache Controller controls the data paths for cache hits and misses to provide the CPU with the proper requested data. The controller dynamically adds one wait state on read hits according to the most recently used (MRU) prediction mechanism. The 82496 Cache Controller is also responsible for performing CPU and memory bus snoop operations while other devices are using the memory bus. The 82496 Cache Controller drives the cycle address and other attributes during memory bus accesses.

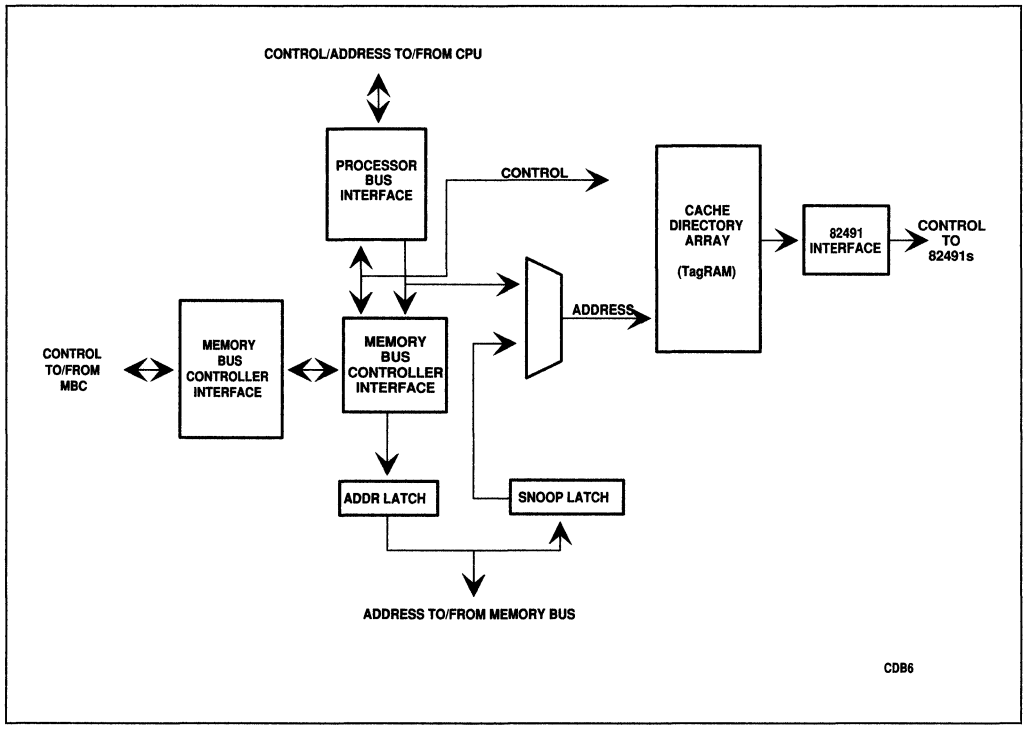

Figure 2-1. 82496 Cache Controller Block Diagram

2.2.2. 82491 Cache SRAMs

82491 Cache SRAMs are used to implement cache SRAM storage and data path. The 82491 Cache SRAM contains latches, multiplexers and glue logic that enable the cache to work in lock step with the 82496 cache controller (see Figure 2-2). The 82491 Cache SRAM efficiently serves Pentium processor requests, whether or not needed data resides in the 82491 Cache SRAM itself. The 82491 Cache SRAM takes full advantage of optimized and integrated internal silicon flexibility to provide a degree of performance that cannot be attained with discrete implementations. The 82491 Cache SRAM supports zero waitstate cache hit accesses, as well as concurrent CPU and memory bus accesses. The 82491 Cache SRAM replicates the MRU bits to provide autonomous way prediction. During memory bus cycles, the 82491 Cache SRAM acts as a gateway between CPU and memory buses.

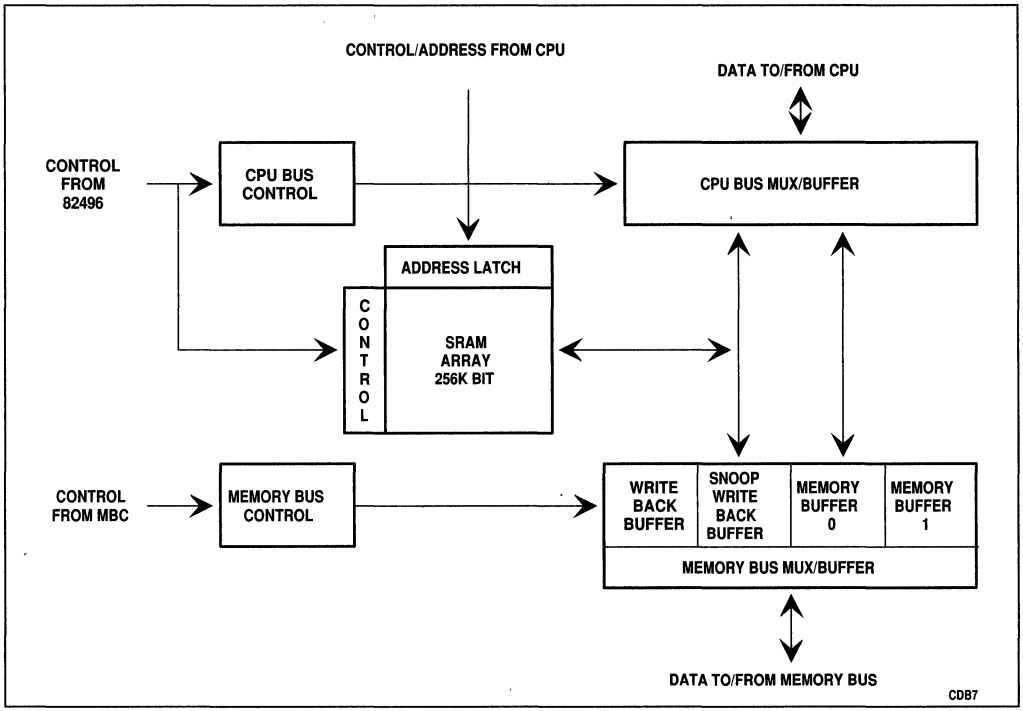

Figure 2-2. 82491 Cache SRAM Block Diagram

2.2.3. Memory Bus Controller

The memory bus controller (MBC) is the server for memory bus cycles. It adapts the Pentium processor/82496 Cache Controller/82491 Cache SRAM cache core to a specific memory bus protocol (see Figure 2-3). The MBC works with the 82496 Cache Controller to perform all operations which reach the memory bus, including line fills (including allocations) and write-backs. System designers can optimize their MBC designs to suit specific architectures. The memory bus controller handles all cycle control, data transfer and snooping operations as well as any needed synchronization between the memory bus and the Pentium processor/82496 Cache Controller/82491 Cache SRAM. Chapter 5 includes details about memory bus controller design as well as a description of all 82496 Cache Controller/82491 Cache SRAM cycles.

Intel does not currently supply a standard MBC for the Pentium processor/82496 Cache Controller/82491 Cache SRAM cache subsystem. The specific implementation is left up to the system designer.

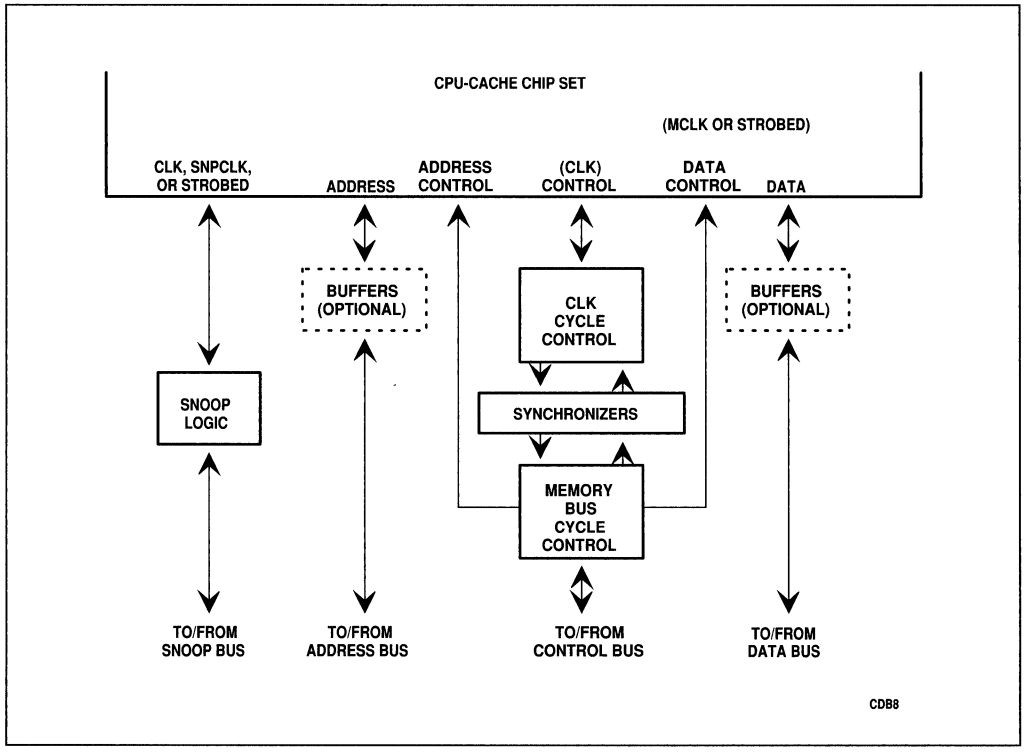

Figure 2-3. MBC Block Diagram

2.3. CONFIGURATION

The 82496 Cache Controller/82491 Cache SRAM can be configured in many different ways. A system designer can choose how to configure the 82496 Cache Controller/82491 Cache SRAM physically (line size, sectoring, etc.), what snooping mode to use, and which memory bus mode is optimal.

Configurations are selected by altering the 82496 Cache Controller/82491 Cache SRAM inputs during RESET. Cache configurations are not dynamically changeable. To conserve pins some configuration inputs become 82496 Cache Controller or 82491 Cache SRAM inputs/outputs after RESET.

2.3.1. Physical Cache

Physically, the 82496 Cache Controller/82491 Cache SRAM can be configured to support many different cache configurations. By selecting one cache configuration, other configurations are excluded. The 82496 Cache Controller/82491 Cache SRAM can be configured to support:

- 256-Kbyte or 512-Kbyte cache
- 64 or 128 bit wide memory bus
- One or two lines per sector
- 1:1, 1:2, or 1:4 CPU to 82496 Cache Controller line size ratio
- 4 or 8 memory bus transactions
- 4K or 8K tag size
- Strong/weak write ordering

2.3.2. Snoop Modes

When another master snoops the 82496 Cache Controller, the MBC must initiate the snoop request and pass on the 82496 Cache Controller response. The 82496 Cache Controller allows the MBC to initiate this snoop request in one of three modes: synchronous, clocked (asynchronous), and strobed. The snoop response of the 82496 Cache Controller is always synchronous.

2.3.2.1. SYNCHRONOUS SNOOP MODE

When the MBC initiates the snoop in synchronous snoop mode, the 82496 Cache Controller latches all snoop information synchronous to the CPU CLK. The snoop is then performed on the next CLK edge (if resources are available). The snoop response is given on the CLK edge after the snoop is performed. This is the fastest possible method of snooping.

2.3.2.2. CLOCKED (ASYNCHRONOUS) SNOOP MODE

In clocked (asynchronous) snooping mode, the 82496 Cache Controller latches snoop information with respect to an external snoop clock (SNPCLK). SNPCLK frequency is slower than CLK frequency. The 82496 Cache Controller must internally synchronize this information to CLK and provide a response.

2.3.2.3. STROBED SNOOP MODE

In strobed snooping mode, the 82496 Cache Controller latches snoop information with respect to the falling edge of SNPSTB#. Thus, snoop initiation is clock independent. The 82496 Cache Controller again synchronizes this snoop information with CLK.

2.3.3. Memory Bus Modes

The 82491 Cache SRAM may be configured in one of two memory bus modes: clocked mode and strobed mode. The memory bus mode determines how data will be passed on to/off of the data bus. The memory bus mode is not related to the snoop mode.

2.3.3.1. CLOCKED MEMORY BUS MODE

In clocked memory bus mode, the 82496 Cache Controller/82491 Cache SRAM drives or reads data with respect to MCLK (an external memory clock source). MCLK is completely independent of the CPU CLK source. There are inherent performance advantages, however, in making this clock source synchronous or half-clock (divided) synchronous to the CPU CLK.

2.3.3.2. STROBED MEMORY BUS MODE

In strobed memory bus mode, the 82491 Cache SRAM drives data with respect to the rising or falling edge of one signal. The 82491 Cache SRAM reads data with respect to the rising or falling edge of another signal. Like strobed snooping mode, strobed memory bus mode causes no clock skew problems or memory bus speed limitations.

2.4. PENTIUM PROCESSOR BUS INTERFACE

The CPU bus interface is the connection between the 82496 Cache Controller/82491 Cache SRAM and the Pentium processor. This interface is optimized for maximum performance. The signals contained within this interface are not specified with setup, hold, and valid delay times. Intel provides layouts and 'flight-time' specifications for these signals. These flight times must be strictly adhered to in order to guarantee proper operation of the Pentium processor/82496 Cache Controller/82491 Cache SRAM chip set. The flight time specifications are described in the Electrical Specifications chapter.

Some CPU signals are accessible by the MBC. These are shown in Table 2-1.

Table 2-1. Pentium™ Processor Signals Accessible by the MBC

Functional		B Scan	Diagnostic
A20M#	IGNNE#	TCK	IV
APCHK#	INIT	TDI	IU
BRDY#	INTR	TDO	IBT
BREQ	NMI	TMS	BP[3:2]
FERR#	PCHK#	TRST#	PM/BP[1:0]
FLUSH#	PEN#		PRDY
HIT#	RESET		R/S#
HLDA	SMI		BUSCHK#
HOLD	SMIACT#	**Special**	FRCMC#*
IERR#		CLK	

* FRCMC# must be tied to VCC when using the Pentium™ processor with the 82496 Cache Controller/82491 Cache SRAM secondary cache.

The 82496 Cache Controller and 82491 Cache SRAM latch several Pentium processor outputs. Table 2-2 below lists the Pentium processor outputs latched by the 82496 Cache Controller/82491 Cache SRAM. Refer to Chapter 5 for detailed functional pin descriptions.

Table 2-2. Pentium™ Processor Signals Latched in the 82496 Cache Controller and 82491 Cache SRAM

Pentium™ Processor Outputs	82491 Cache SRAM Outputs	82496 Cache Controller Outputs
BE[7:0]#	MBE#	
CACHE		CCACHE#
PCD		CPCD
PWT		CPWT
SCYC		CSCYC

2.5. 82496 CACHE CONTROLLER/82491 CACHE SRAM OPTIMIZED INTERFACE

The 82496 Cache Controller/82491 Cache SRAM interface is the connection between 82496 Cache Controller and 82491 Cache SRAM. Like the CPU bus interface, this optimized interface is designed to provide the highest speed goal between the devices; therefore, reference layouts and 'flight-time' specifications should be strictly adhered to.

2.6. MEMORY BUS INTERFACE

The Memory Bus Controller (MBC) is the interface logic required to control the Pentium processor/82496 Cache Controller/82491 Cache SRAM and connect it to the memory bus and rest of the system. The MBC may be simple enough to support a single-CPU write-through cache, or complex enough to support a multiprocessing cache with external tags. The 82496 Cache Controller/82491 Cache SRAM is a very flexible chipset. The MBC determines exactly how the 82496 Cache Controller/82491 Cache SRAM will work in a system.

An MBC consists of a few basic blocks: a snoop logic block, a memory bus cycle control block (with synchronizers if necessary), and a clock cycle control block. The snoop block must be able to communicate with the other caches when snooping is necessary. At the same time, the cycle control blocks must interface to some arbitration logic external address and/or data buffers.

2.6.1. Snooping Logic

The MBC snooping logic is responsible for initiating a snoop in the 82496 Cache Controller and providing the snoop response to the rest of the system. Snoop logic must also delay snoop initiation if the 82496 Cache Controller is not capable of responding to a snoop.

When the master 82496 Cache Controller begins a cycle on the bus, all other caches snoop. Once all the snoop results are returned to the master 82496 Cache Controller MBC, its snoop logic must recognize the result and alter the cycle appropriately. The MBC may abort the current cycle in memory, delay the cycle until a write-back is performed, or change the master 82496 Cache Controller's tag state according to the snoop information.

2.6.2. Cycle Control Logic

Cycle control logic is responsible for initiating a memory bus cycle, providing proper 82496 Cache Controller cycle attributes during the cycle, and terminating the cycle. Cycle control logic determines all aspects of the progress of a cycle. For example, cycle control logic determines whether a given cycle is cacheable or allocatable.

Cycle control logic interfaces memory bus signals to the 82496 Cache Controller. Since the memory bus may be asynchronous to the 82496 Cache Controller CLK, cycle control logic must also provide proper synchronization. Careful design of this synchronization logic can minimize or eliminate synchronization penalties.

Address path control logic controls when and how the address is driven onto the memory bus. It also performs address parity calculation and checking if desired.

Data path control logic controls how data is written from or read into the 82491 Cache SRAM and CPU. It handles the actual transfer of data to/from the memory data bus. Data path control logic also handles the CPU burst order and the holding of data during cache to cache transfers.

If 82491 Cache SRAMs are used as data parity devices, the MBC must drive valid data parity values into the parity 82491 Cache SRAM devices during snoop cycles.

2.7. TEST

The 82496 Cache Controller/82491 Cache SRAM provides two means of cache testing: built-in self-test and boundary scan test. The 82496 Cache Controller and Pentium processor built-in self-test (BIST) can be initiated during RESET. Boundary scan test uses separate and dedicated pins on the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM. Boundary scan functionality is described in the Testability Chapter.

3

Component Operation

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CHAPTER 3
COMPONENT OPERATION

This section presents the cache consistency protocol of the 82496 Cache Controller and explains the architectural decisions underlying the design of the component.

Cache consistency protocols are designed to ensure that, in a shared memory system, cache data and main memory data are consistent. A number of cache architectures can be employed to maintain consistency, including write-through, posted write, write-back (also called copy-back), and two-level mixed (primary write-through with secondary write-back). Write-through and write-back designs are the most popular.

3.1. WRITE-THROUGH CACHE DESIGNS

In write-through cache designs, cache memory remains consistent with main memory. In a write-through cache design, every CPU write operation accesses both cache memory and main memory. A write-through cache must monitor bus masters other than the CPU that could alter main memory locations. The cache must then render some of its contents invalid based on these alterations. To maintain consistency, a write-through cache employs a valid/invalid protocol. 'Valid' indicates that a cache tag contains a memory location which is unaltered from main memory. 'Invalid' indicates that the tag is empty. The 82496 Cache Controller/82491 Cache SRAM can be implemented as a write-through cache by using available control signals (ie. MWB/WT#, MKEN#). These control signals cause the tag state to use only the shared and invalid MESI cache coherency protocol states.

3.2. WRITE-BACK CACHE DESIGNS

In write-back cache architectures, writes may be made to the cache exclusively. Modified cache lines are subsequently written back into main memory. The "modified bit" associated with each cache line is used by the cache controller to determine whether a specific main memory locations needs to be updated.

The 82496 Cache Controller/82491 Cache SRAM employs such a write-back architecture. In addition, the 82496 Cache Controller/82491 Cache SRAM tracks data that can be shared by multiple bus masters within a shared memory system. This additional tracking is accomplished using the MESI protocol, wherein each cache line is classified as modified [M], exclusive [E], shared [S], or invalid [I].

3.3. 82496 CACHE CONTROLLER CACHE CONSISTENCY PROTOCOL

The 82496 Cache Controller/82491 Cache SRAM is designed to supplement the Pentium processor with the cache and cache management resources needed to implement high-

performance uniprocessor or multiprocessor systems. The 82496 Cache Controller/82491 Cache SRAM secondary cache provides 8 or 16 82491 Cache SRAM components and a 82496 Cache Controller cache controller that offers full multiprocessor cache consistency support. Because the 82496 Cache Controller implements a write-back cache architecture, the 82496 Cache Controller/82491 Cache SRAM will at times contain data that has not yet been written back into main memory. The 82496 Cache Controller is designed to ensure that all of the bus masters in a shared memory system are prevented from reading invalid data.

Multiprocessor systems must not only provide cache consistency, but minimize memory bus access as well. Otherwise, bus masters combine to create a resource bottleneck that can degrade the performance potential of multiple execution units.

The cache consistency protocol used by the 82496 Cache Controller is designed both to ensure cache consistency and to keep memory bus utilization to a minimum. The protocol is based on several common protocols.

The 82496 Cache Controller protocol is implemented by assigning state bits for each cached line. These states are affected both by CPU initiated operations and by snoop operations performed in response to requests from other bus masters.

3.4. MESI CACHE CONSISTENCY PROTOCOL MODEL

The description that follows applies to memory read and write cycles only. I/O and special cycles bypass the cache altogether.

The 82496 Cache Controller/82491 Cache SRAM follows the MESI protocol which is used to indicate whether a given cache line has been modified [M], not modified but valid (exclusive [E] or shared [S]), or is invalid [I].

The MESI states are explained in more detail as follows:

[M] - MODIFIED The [M] state indicates that a line is exclusive to the 82496 Cache Controller/82491 Cache SRAM cache and has been modified. Therefore, the corresponding line in main memory is invalid. This cache line can be modified further without memory bus access, thereby reducing bus traffic. Because the data is exclusive to the 82496 Cache Controller/82491 Cache SRAM's cache, the 82496 Cache Controller/82491 Cache SRAM must at some point write this information back to main memory.

[E] - EXCLUSIVE The [E] state indicates that a particular line is available in the 82496 Cache Controller/82491 Cache SRAM cache exclusively and that the line has not been modified. Therefore, the corresponding main memory line is valid. A write changes this line to the [M] state without accessing the memory bus.

[S] - SHARED The [S] state indicates that a particular line may also exist in other system caches. A shared line may be read from the cache without requiring main memory access. Writing to a shared line updates the cache, but also requires that the 82496 Cache Controller/82491 Cache SRAM generate a write-through to update main memory and invalidate the line where it exists in other caches.

[I] - INVALID The [I] state indicates that a particular line is not available in the cache. A read to this line results in a miss, which, in some cases, causes the 82496 Cache Controller to execute a line fill. A write to this line causes the 82496 Cache Controller/82491 Cache SRAM to execute a write-through to main memory or, in some circumstances, to initiate an allocation.

3.5. BASIC MESI STATE TRANSITIONS

The MESI state of a cache line depends on several factors, including CPU cycle type and memory bus controller operation. Following a snoop, the MESI state of a line may change, or the line may be written back.

This section covers the most common memory accesses. Non-cacheable cycles, locked cycles, read-only cycles, and direct-to-modified cycles are covered in Section 3.6.

One category of memory accesses deals with MESI state changes to the CPU-cache core resulting from internal operations. Another category deals with MESI state changes resulting from actions by external devices. Figure 3-1 diagrams a portion of the MESI coherency protocol. The diagram shows state transitions caused by both categories of memory accesses.

Table 3-1 below shows the basic MESI state transitions implemented by the 82496 Cache Controller/82491 Cache SRAM. The "CURRENT STATE" refers to the state of the 82496 Cache Controller/82491 Cache SRAM line being accessed either by it's Pentium processor or a snoop from another cache on the memory bus. The "ACTION" refers either to a CPU read, CPU write, or a snoop initiated by another bus master attached to the same shared memory bus. The "NEW STATE" refers to the state of the current cache line after the action is performed. The new state is dependent upon the values of SNPINV and SNPNCA for snoop operations, and DRCTM#, MWB/WT#, LOCK#, MKEN#, and MRO# for read and write operations. "MEMORY BUS ACTIVITY" refers to the action which takes place on the memory bus (if any) as a result of the action being performed on the cache line.

Table 3-1. Basic MESI State Transitions

Current State	Action	New State	Memory Bus Activity
M	read	**M**	none
	write	**M**	none
	snoop	**E,S,I**	write-back
E	read	**E**	none
	write	**M**	none
	snoop	**E,S,I**	none
S	read	**S**	none
	write	**M,E,S**	write-through
	snoop	**S, I**	none
I	read	**M,E,S,I**	linefill
	write	**M,E,S,I**	write-through
	snoop	**I**	none

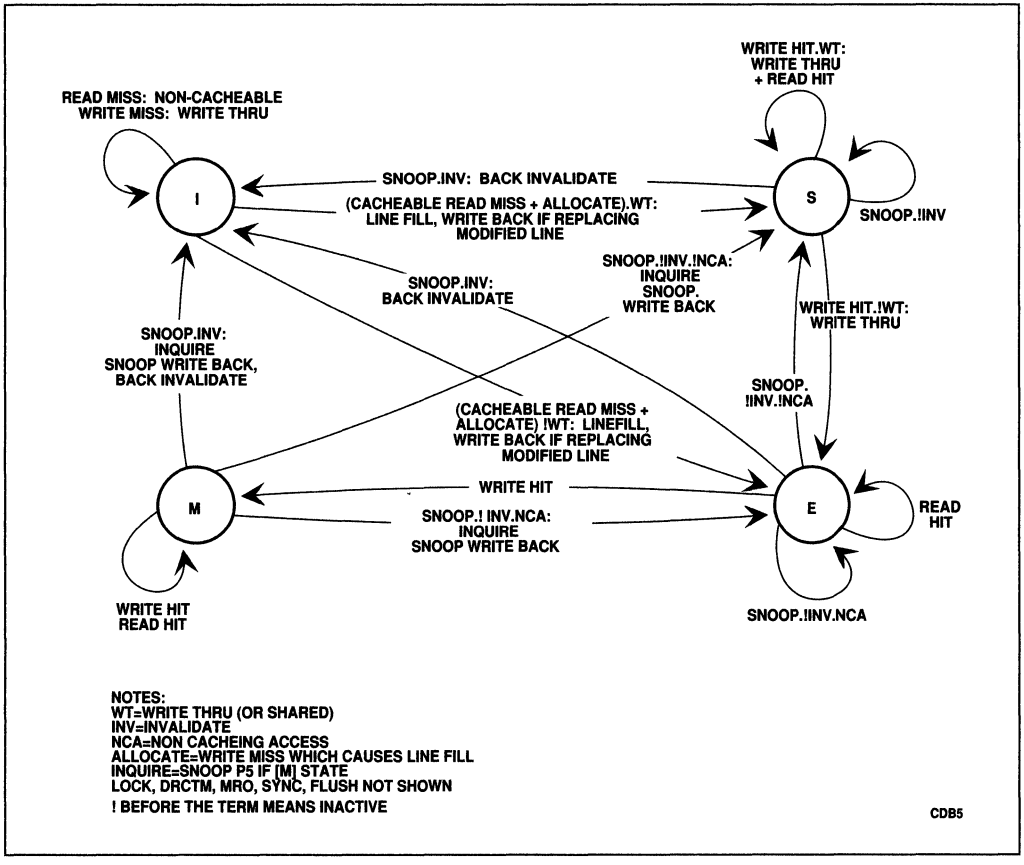

Figure 3-1. State Changes

3.5.1. MESI State Changes Resulting From CPU Bus Operations

The MESI state of a valid 82496 Cache Controller/82491 Cache SRAM's line may change as the controller services Pentium processor read and write requests.

3.5.1.1. READ HIT

A read hit occurs when the CPU requests a read cycle that can be serviced locally by the 82496 Cache Controller/82491 Cache SRAM using data present in the 82496 Cache Controller/82491 Cache SRAM. The MESI state of the cached line ([M], [E] or [S]) remains unchanged by this operation.

3.5.1.2. READ MISS

A read miss occurs when the CPU generates a read cycle that cannot be serviced locally

because the needed data is missing from the cache. The tag lookup either cannot produce a match or else produces a match to an [I] line. Here, the 82496 Cache Controller/82491 Cache SRAM generates a main memory access to fetch the data needed, sometimes along with enough surrounding data to fill the cache line. When a linefill is executed, the new data is written into the 82496 Cache Controller/82491 Cache SRAM, overwriting an invalid line, or replacing the least recently used line if both ways have valid lines. If it has been modified, the least recently used line is also copied into main memory.

Following a linefill into the 82496 Cache Controller/82491 Cache SRAM, the new tag state is determined as follows:

- [S] if the line is Read-Only.
- [S] if the CPU write through attribute is active (PWT High).
- [S] if the memory shared attribute is active (MWB/WT# Low).
- [S] if the line is present in another cache.
- [E] if the line is not present in another cache.
- [M] if modified data comes directly from another cache, without main memory update.

3.5.1.3. WRITE HIT

A write hit occurs when the CPU generates a write cycle while the needed data is already present in the local cache. Here, the cache line is updated and may undergo a MESI state change.

If the line is in the [E] state prior to the write, it changes to the [M] state. If the line is in the [M] state prior to the write, it maintains that state.

If the line is in the [S] state prior to the write, the cache controller writes the data to memory in addition to updating the cache. The write to main memory also invalidates any copy of the data that might reside in another cache. If the line is Read-Only, the cycle will go to the memory bus without updating the 82491 Cache SRAM array and the tag will remain unchanged.

The cache line state changes with activity on the PWT and MWB/WT# pins. If neither of these pins is asserted, the line written to transitions to the [E] state. If either pin is asserted, the line must remain write-through, and the state remains [S].

3.5.1.4. WRITE MISS

A write miss occurs when the CPU generates a write cycle and the data is not present in the local cache. In a simple write miss, the cache operates along with the CPU in writing data to main memory, but it does not cache the data. No cache lines are affected, and no state changes take place.

3.5.1.5. WRITE MISS WITH ALLOCATION

In this special case, the CPU writes to a memory location that is not in the cache at the time of the write, but is later brought into cache and updated. As in a normal write miss, the cache operates along with the CPU in writing data to main memory assists the CPU in writing the data to main memory. When this write completes, the 82496 Cache Controller performs an

allocation (linefill).

The allocation can be performed pending the following circumstances:

- The write is cacheable (active MKEN#)
- PCD and PWT are not asserted
- The write is not LOCKed
- The write is to memory, not to I/O
- The write is a miss, not a hit

3.5.2. MESI State Changes Resulting From Memory Bus Masters

MESI state transitions within the 82496 Cache Controller/82491 Cache SRAM may result from the activities of other processing units within the shared memory system.

The device in control of the bus at any time is called the bus master. When the 82496 Cache Controller/82491 Cache SRAM is not in control of the bus during snoop operations, it is referred to as the "slave".

3.5.2.1. SNOOPING

In snoop operations, the bus master requests the slaves to examine their cache lines for the data that the bus master is requesting from main memory. A "snoop hit" occurs when one of the slaves contains this memory information, whether it be modified or not.

There are three primary purposes of snooping:

1. Requesting modified data from other caches.
2. Invalidating data in other caches in the case of write cycles.
3. Sharing data between caches.

How the slave enacts MESI state changes following a snoop hit depends on the SNPINV and SNPNCA input attributes driven by the bus master.

The SNPINV input directs a slave to invalidate a snooped line since the bus master contains the most recent version of the data. The snooped line is placed in the [I] state.A back-invalidation procedure is initiated to instruct the slave CPU to invalidate any copy of the data that it might also contain. For example, if a bus master performs a write cycle to memory, the slave memory bus controller must snoop and assert SNPINV since its copy will no longer be consistent with memory.

When asserted, the SNPNCA input indicates to a slave that the requesting master is performing a non-cacheable read. A snoop hit to an [M] or [E] line can be placed in the [E] state because the bus master will not cache the line. If SNPNCA is not asserted, the bus master will cache the line. The cache line must be placed in the [S] state to ensure that a future write hit invalidates the line in other caches. Regardless of SNPNCA, an [S] line remains in the [S] state following a snoop hit. In addition, when SNPINV is asserted, it always overrides SNPNCA.

3.5.2.2. CACHE SYNCHRONIZATION

Cache synchronization is performed to make main memory consistent with the 82496 Cache Controller/82491 Cache SRAM. FLUSH and SYNC are used to maintain cache synchronization.

A cache flush is initiated by asserting the FLUSH# pin. Once this operation is initiated, the 82496 Cache Controller/82491 Cache SRAM writes all [M] lines out to main memory and performs processor inquires and back-invalidation cycles. Subsequently, all Pentium processor cache and 82496 Cache Controller/82491 Cache SRAM entries are in the [I] state.

Cache synchronization is initiated by asserting the SYNC# pin. Once the operation is initiated, the 82496 Cache Controller/82491 Cache SRAM writes all [M] lines out to main memory and performs processor inquires. Subsequently, all Pentium processor cache and 82496 Cache Controller/82491 Cache SRAM entries are in a non-modified state (E, S, or I).

3.6. MESI STATE CHANGES FOLLOWING CYCLES WITH SPECIAL ATTRIBUTES

3.6.1. Cacheability Attributes: PCD, MKEN#

The 82496 Cache Controller/82491 Cache SRAM allows cacheability to be determined on a page basis as well as on a line basis. Page cacheability is implemented in the CPU by initialization of the page table so that it drives the PCD output appropriately. The memory bus controller implements line by line cacheability by asserting the MKEN# signal.

The Page Caching Disabled attribute is driven by the processor's PCD output and corresponds to a cacheability bit in the page table entry of a memory location's virtual address. If the PCD bit is asserted when the CPU presents a memory address, the memory location will not be cached in the 82496 Cache Controller/82491 Cache SRAM or the CPU.

MKEN# is a 82496 Cache Controller input which connects to the memory bus controller or to the bus itself. When MKEN# is inactive, it prevents a memory location from being cached in the 82496 Cache Controller/82491 Cache SRAM and the CPU. MKEN# affects only the current access.

If the PCD output or MKEN# input render a read miss non-cacheable, the line will not be cached in the 82496 Cache Controller/82491 Cache SRAM or the CPU cache, leaving cache state information unaltered. On a write miss, a non-cacheable indication from either input initiates a write miss without allocation. PCD has no effect on read hit cycles if the 82496 Cache Controller/82491 Cache SRAM already has a valid copy of a given line.

3.6.2. Write Through Protocol: PWT, MWB/WT#

The 82496 Cache Controller/82491 Cache SRAM allows write-through protocol to be implemented on a page basis as well as on a line basis. Write through policy is selected for a particular line by either using the PWT attribute in the CPU page table or driving the

MWB/WT# pin LOW whenever the address corresponding to the line is referenced. Note that using the PWT attribute in the CPU page table causes an entire page to be write-through; a line in a write-through page is also write-through. The PWT attribute does not allow the system designer to implement line-by-line write-through protocol. Write through cache consistency protocol only uses S and I cache line states.

The Page Write Through attribute is driven by the processor's PWT output and corresponds to a write through bit in the page table entry of a memory location's virtual address. If the PWT bit is asserted when the CPU presents a memory address, the memory location will not be cached in the exclusive or modified states in either the 82496 Cache Controller/82491 Cache SRAM or the Pentium processor caches.

MWB/WT# is a 82496 Cache Controller input which connects to the memory bus controller or to the bus itself. When MWB/WT# is low, it also prevents lines from being cached in exclusive or modified states in either the 82496 Cache Controller/82491 Cache SRAM or the CPU caches. MWB/WT# only affects the current access.

If the Pentium processor PWT output is active or the 82496 Cache Controller MWB/WT# input is low, the current line will never be placed into the exclusive or modified states. On a linefill, the state of the line will always be shared. Note that if the 82496 Cache Controller/82491 Cache SRAM already has an exclusive or modified copy of the line, PWT has no effect on the cycle.

3.6.3. Read Only Accesses: MRO#

The Memory Read Only input (MRO#) is driven by the memory bus to indicate that a memory location is read-only.

When asserted during a read miss line fill, MRO# causes the current line to be placed in the 82496 Cache Controller/82491 Cache SRAM in the [S] state. MRO# also sets a read-only bit in the cache tag.

On subsequent write hits to a read-only line, data is written to main memory without updating the 82496 Cache Controller/82491 Cache SRAM line. The cached line remains in the [S] state with the read-only bit set. Subsequent read hits to read-only data will not be cacheable in the CPU cache.

The 82496 Cache Controller supports caching of Read-Only code lines in the CPU cache by using the KEN# signal to the CPU. Read-only code (CD/C# low) is cached in the Pentium processor by asserting KEN# to the CPU during a line fill. The Pentium processor automatically invalidates cache lines in its code cache if they are written to. If KEN# is deasserted to the CPU, read only data will not be cached in the Pentium processor cache.

3.6.4. Locked Accesses: LOCK#

The LOCK# signal is driven by the CPU to indicate that the requested cycle should lock the memory location for an atomic memory access. Because locked cycles are used for inter-processor and inter-task synchronization, all locked cycles must appear on the memory bus.

During locked write cycles, the 82496 Cache Controller/82491 Cache SRAM treats accesses as write-through cycles. The 82496 Cache Controller/82491 Cache SRAM sends data to the

memory bus, updaes memory, and invalidates other cached copies. Data that is also present in the 82496 Cache Controller/82491 Cache SRAM is updated, but its MESI state remains unchanged.

During locked read cycles, the 82496 Cache Controller/82491 Cache SRAM follows the cache miss procedure: it initiates a memory read cycle. If the line resides in the 82496 Cache Controller/82491 Cache SRAM, the MESI state of the line remains unchanged. If the data resides in the 82496 Cache Controller/82491 Cache SRAM in the [M] state when the memory bus returns data, the 82496 Cache Controller/82491 Cache SRAM uses the data from the 82491 Cache SRAM and ignores the data on the memory bus.

Locked read and write cycles that miss the 82496 Cache Controller/82491 Cache SRAM cache are non-cacheable in the 82496 Cache Controller/82491 Cache SRAM cache and the CPU.

3.6.5. Direct-To-Modified Attribute: DRCTM#

The direct-to-modified input pin (DRCTM#) indicates to the 82496 Cache Controller/82491 Cache SRAM that it should circumvent the [E] and [S] state designations and place a data line directly into the [M] state. If MWB/WT# is sampled low, DRCTM# has no effect on the final line state. DRCTM# can be asserted during main memory reads for special 82496 Cache Controller/82491 Cache SRAM data accesses including allocation, read-for-ownership, and cache-to-cache-transfer (without main memory update).

3.7. STATE TRANSITIONS

Lines cached by the 82496 Cache Controller can change states as a result of either the CPU bus activity (that sometimes require the 82496 Cache Controller to become a Memory Bus Master) or as a result of Memory Bus activity generated by other System Masters (e.g. Snooping).

The following section details: CPU and memory bus signals that affect state changes, tag state changes, and cycles generated on the CPU/memory bus due to state transitions.

3.7.1. CPU Bus Signals

The following CPU bus signals affect 82496 Cache Controller/82491 Cache SRAM state transitions:

- *PWT* (Page Write Through, 82496 Cache Controller **PWT** input pin): Indicates a CPU bus write-through request. If PWT is active during a linefill, the current line is put in the [S] state. The 82496 Cache Controller will NOT execute allocations (linefills triggered by a write) for write-through lines. **PWT** overrides a write-back indication on the **WB/WT#** pin.
- *PCD* (Page Cacheability Disable, 82496 Cache Controller **PCD** input pin): Indicates that the accessed line is non cacheable. If **PCD** is asserted, it overrides a cacheable indication from an asserted **MKEN#**.
- *WT* (Pentium processor Write-Through indication, 82496 Cache Controller **WB/WT#**

output pin): When active, forces the Pentium processor to keep the accessed line in the shared state.

Write back mode (WB=1) is indicated by the *!WT* notation. In writeback mode, the Pentium processor is allowed to go into exclusive states [E], [M]. *WT* is normally active unless explicitly stated.

- *KEN* (CPU Caching Enable, 82496 Cache Controller **KEN#** output pin): When active indicates that the requested line can be cached by the CPU first level cache. *KEN* is normally active unless explicitly stated.
- *DAT* (CPU Data Control, 82496 Cache Controller **D/C#** input pin): When active indicates that the requested line is data. When inactive indicates that the requested line is code.

3.7.2. Memory Bus Signals

The following memory bus signals affect 82496 Cache Controller/82491 Cache SRAM state transitions:

- *MWT* (Memory Bus Write-Through indication, 82496 Cache Controller **MWB/WT#** input pin): When active, forces the 82496 Cache Controller to keep the accessed line into the shared state. Write back mode (MWB=1) is indicated by the *!MWT* notation. In writeback mode, the 82496 Cache Controller is allowed to go into exclusive states [E], [M].
- *DRCTM* (Memory Bus Direct To [M] indication, DRCTM# input pin): When active, forces the line state to bypas [E] and go to [M] (provided !MWT).
- *MKEN* (Memory Bus Cacheability Enable, 82496 Cache Controller **MKEN#** input pin): When active, indicates that the memory bus cycle is cacheable.
- *MRO* (Memory Bus Read-Only indication, 82496 Cache Controller **MRO#** input pin): When active, forces line to be READ-ONLY ([S] state).
- *MTHIT* (Memory Bus Tag Hit, 82496 Cache Controller **MTHIT#** output pin): Activated by the 82496 Cache Controller during snoop cycles and indicates that the current snooped address hits the 82496 Cache Controller cache.
- *MHITM* (Memory Bus Hit to [M] state, 82496 Cache Controller **MHITM#** output pin): Activated by the 82496 Cache Controller during snoop cycles and indicates that the current snooped address hits a modified line in the 82496 Cache Controller cache.
- *SNPNCA* (Non Caching Access, 82496 Cache Controller **SNPNCA** input pin): When active indicates to the 82496 Cache Controller that the current bus master does not intend to cache the snooped line.
- *SNPINV* (Invalidation, 82496 Cache Controller **SNPINV** input pin): When active indicates to the 82496 Cache Controller that the current snoop cycle will invalidate that address.

3.7.3. Tag State and Cycles Resulting from State Transitions

3.7.3.1. TAG STATE

The following is a 82496 Cache Controller tag state change that may occur with 82496 Cache Controller/82491 Cache SRAM state transitions. Note that other tag state changes are not documented here, as they are not used in the tables that follow.

- *TRO* (Tag Read Only, 82496 Cache Controller Tag bit): When set indicates that the 1 or 2 (if 2 lines per sector) lines associated with the current tag are Read-Only lines.

3.7.3.2. CYCLES RESULTING FROM STATE TRANSITIONS

As a function of State Changes, the 82496 Cache Controller may execute the following cycles:

- *BINV*: CPU Back Invalidation Cycle (Snoop to Pentium processor with **INV** active)
- *INQR*: Pentium processor Inquire Cycle to search for a CPU modified line.

NOTE

An inquire cycle may be executed with INV active, performing a back-invalidation simultaneously.

- *WBCK*: 82496 Cache Controller Write-Back Cycle. The 82496 Cache Controller generates a writeback cycle when MODIFIED data cached in the 82496 Cache Controller needs to be copied back into main memory. A write-back cycle affects a complete 82496 Cache Controller line.
- *WTHR*: 82496 Cache Controller Write Through Cycle. This is a memory bus write cycle in response to a processor write. It may or may not affect the cache SRAM (update). In a write-through cycle, the 82496 Cache Controller drives the Memory Bus with the same Address, Data and Control signals as the CPU does on the CPU Bus. Main memory will be updated, and other caches will invalidate their copies.
- *RTHR*: 82496 Cache Controller Read Through cycle. This is a special read cycle to support locked reads to lines that hit the 82496 Cache Controller cache. The 82496 Cache Controller will request a Memory Bus cycle for lock synchronization reasons. Data will be supplied from the memory BUS except if the current line is in the [M] state. If so, data will be supplied to the Pentium processor from the 82496 Cache Controller/82491 Cache SRAM .
- *LFIL*: 82496 Cache Controller Cache line fill. The 82496 Cache Controller will generate Memory Bus cycles to fetch a new line and deposit it into the cache.

- *RNRM*: 82496 Cache Controller Read Normal Cycle: This is a normal read cycle which will be executed by the 82496 Cache Controller for non-cacheable accesses.
- *SRUP*: 82491 Cache SRAM SRAM update. This cycle occurs any time new information is placed in the 82491 Cache SRAM cache. An SRAM update is implied in the *LFIL* cycle.
- *ALLOC*: 82496 Cache Controller allocation. This cycle is a linefill that results from a cacheable write miss cycle.

3.7.4. MESI State Tables (82496 Cache Controller State Changes)

Table 3-2. Master 82496 Cache Controller Read Cycle

Pres. State	Condition: Next State	Mem Bus Activity	CPU Bus Activity	Comments
M	!LOCK: M	—	!WT	Normal Read Hit [M].
	LOCK: M	RTHR	!KEN	Read Through Cycle, Data From Array.
E	!LOCK: E	—	—	Normal Read Hit [E].
	LOCK: E	RTHR	!KEN	Read Through Cycle, Data From Memory.
S	!LOCK.!TRO: S	—	—	Normal Read Hit [S].
	!LOCK.TRO.DAT: S		!KEN	Normal Read to Read-Only data sector. Stays in [S] state, deactivates KEN# to disable caching in L1 data cache.
	!LOCK.TRO.!DAT: S	—	—	Normal Read to Read-Only code sector. Stays in [S] state, activates KEN# to enable caching in L1 code cache.
	LOCK: S	RTHR	!KEN	Read Through Cycle, Data from Memory.
I	PCD+!MKEN+LOCK: I	RNRM	!KEN	Non-Cacheable Read, Locked cycles.
	!PCD.MKEN.!LOCK.MRO.DAT: S	LFIL	!KEN	Cacheable data read, Read-Only. Fill line to 82496 Cache Controller cache, but not to Pentium™ processor cache. Set the 82496 Cache Controller TRO bit.
	!PCD.MKEN.!LOCK.MRO.!DAT: S	LFIL		Cacheable code read, Read-Only. Fill line to 82496 Cache Controller and Pentium processor caches. Set the TRO bit in the 82496 Cache Controller cache.
	!PCD.MKEN.!LOCK.!MRO.(PWT+ MWT):S	LFIL	—	Cacheable Reads, forced Write-Through.
	!PCD.MKEN.!LOCK.!MRO.!PWT. !MWT. !DRCTM: E	LFIL	—	Line not shared, thus enabling the 82496 Cache Controller to move into an exclusive state.
	!PCD.MKEN.!LOCK.!MRO.!PWT. !MWT. DRCTM: M	LFIL	—	As before with direct [M] state transfer. Keep Pentium processor in Write Through mode.

Table 3-3. Master 82496 Cache Controller Write Cycle

Pres. State	Condition: Next State	Mem Bus Activity	CPU Bus Activity	Comments
M	!LOCK: M	—	SRUP, !WT	Write hit. Write to cache. Allow Pentium™ processor to perform internal write cycles (Enter into [E], [M] states).
	LOCK: M	WTHR	SRUP, !WT	Locked Cycle. Write-Through updating cache SRAM. Most updated copy of the line is still owned by 82496 Cache Controller. All Locked write cycles are posted.
E	!LOCK: M	—	SRUP, !WT	Write hit. Update SRAM. Let Pentium processor execute internal write cycles.
	LOCK: E	WTHR	SRUP	Lock forces cycle to memory bus. Main memory remains updated.
S	TRO: S	WTHR	—	Read-Only. Data is not updated in cache. Write Through cycle to memory bus is performed.
	!TRO.(PWT+MWT+LOCK): S	WTHR	SRUP	Not Read-Only. Write cycle with write through attribute from CPU or memory bus. Locked cycles.
	!TRO.!PWT.!LOCK.!MWT.!DRCTM: E	WTHR	SRUP	Not Read-Only. No write-through cycle, no lock request. Allow going into exclusive state.
	!TRO.!PWT.!LOCK.!MWT.DRCTM: M	WTHR	SRUP	Not Read-Only. No write-through cycle, no lock request allow going into exclusive state. DRCTM# forces final state to M.
I	PCD+!MKEN+PWT+LOCK: I	WTHR	—	Write Miss Non-Cacheable, Write-Through, locked cycle.
	!PCD.MKEN.!PWT.!LOCK.!MRO: I Allocation Final State MWT: S !MWT.!DRCTM: E !MWT.DRCTM: M !PCD.MKEN.!PWT.!LOCK.MRO:I Allocation Final State: S	WTHR ALLOC WTHR ALLOC	— —	Write Miss with allocation. After the write cycle, a line fill (allocation) is scheduled. Normal allocation final state is a function of the line fill attributes. If MRO# is asserted, an allocation to the [S] state will occur, TRO bit is set, and attributes are ignored.

NOTE: The WB/WT# pin will be Write-Back (HIGH) for reads or writes to [M] state lines and for writes to [E] state lines. On all other states, the Pentium processor will be forced to perform Write-Through cycles. This mechanism will make sure that any Pentium processor write cycle is seen at least once on the CPU bus (Write Once protocol).

Table 3-4. Snooping 82496 Cache Controller without Invalidation Request

Pres. State	Condition: Next State	Memory Bus Activity	CPU Bus Activity	Comments
M	!SNPNCA: S SNPNCA: E	MTHIT MHITM WBCK	INQR	Snoop hit to modified line. 82496 Cache Controller indicates tag hit and modified hit. 82496 Cache Controller schedules a write back of the modified line to memory. If non-cacheable access, stay in [E] sate.
E	!SNPNCA: S SNPNCA: E	MTHIT	—	If snooping by a cacheable access, indicate MTHIT and go to shared state. If a non cacheable access, only indicate MTHIT, stay exclusive.
S	S	MTHIT	—	
I	I	—	—	

Table 3-5. Snooping 82496 Cache Controller with Invalidation Request

Pres. State	Next State	Memory Bus Activity	CPU Bus Activity	Comments
M	I	MTHIT MHITM WBCK	INQR, BINV	Snoop hit to modified line. 82496 Cache Controller indicates tag hit and modified hit. 82496 Cache Controller schedules a write back of the modified line to memory. Invalidate CPU.
E	I	MTHIT	BINV	Indicate tag hit, invalidate 82496 Cache Controller, CPU lines.
S	I	MTHIT	BINV	Same as before
I	I	—	—	

Table 3-6. SYNC Cycles

Pres. State	Next State	Memory Bus Activity	CPU Bus Activity	Comments
M	E	WBCK	INQR	Get modified data from Pentium™ processor flush to memory.
E	E	—	—	Memory already synchronized
S	S	—	—	Memory already synchronized
I	I	—	—	

Table 3-7. FLUSH Cycles

Pres. State	Next State	Mem Bus Activity	CPU Bus Activity	Comments
M	I	WBCK	INQR, BINV	Flush and invalidate Pentium™ processor
E	I	—	BINV	Invalidate Pentium processor
S	I	—	BINV	Invalidate Pentium processor
I	I	—	—	

3.8. PRIMARY TO SECONDARY CACHE COHERENCY

3.8.1. Inclusion

The Pentium processor primary caches always maintain the property of inclusion with respect to the 82496 Cache Controller/82491 Cache SRAM (secondary cache). See Figure 3-2. This means that the Pentium processor caches are guaranteed to be a subset of the 82496 Cache Controller/82491 Cache SRAM. Inclusion is the property which explains why the Pentium processor and 82496 Cache Controller/82491 Cache SRAM line states are updated as described in this chapter.

The C5C cache controller utilizes three mechanisms to maintain the inclusion property of the Pentium processor cache: inquires, back invalidations, and the write once policy. The next two sections describe these mechanisms in more detail.

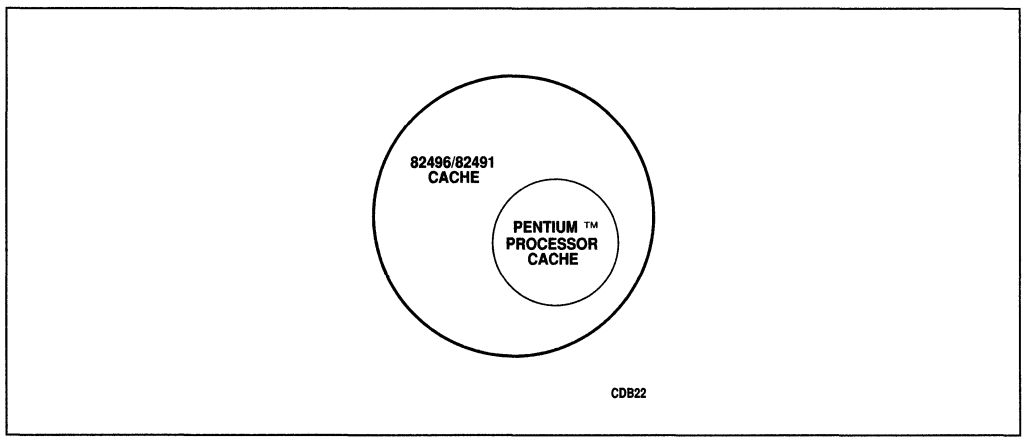

Figure 3-2. Pentium™ Processor CPU-Cache Chip Set Cache Inclusion

3.8.2. Inquire and Back-Invalidation Cycles

Inquire and Back-Invalidation cycles are snoop cycles from the 82496 Cache Controller/82491 Cache SRAM to the Pentium processor.

- Back-Invalidation Cycle: The 82496 Cache Controller/82491 Cache SRAM invalidates a line in the Pentium processor if the address snooped hits the Pentium processor internal cache. If the snooped line in the Pentium processor cache is in the Modified state, it is written back and then invalidated
- Inquire Cycle: The 82496 Cache Controller/82491 Cache SRAM determines if a line is modified in the Pentium processor cache. If the line has been modified, the Pentium processor cache issues a writeback cycle to the 82496 Cache Controller/82491 Cache SRAM.

Snoop cycles are generated from the 82496 Cache Controller to the Pentium processor in the following cases:

- Snoop hit to a Modified line in the 82496 Cache Controller.
- 82496 Cache Controller/82491 Cache SRAM cache flush when a Modified line is hit (flush is initiated by the 82496 Cache Controller FLUSH# input).
- 82496 Cache Controller/82491 Cache SRAM cache sync operation when a Modified Line is hit (sync is initiated by the 82496 Cache Controller SYNC# input).
- Replacement of a modified line in the L2 cache.

During snoop cycles, the 82496 Cache Controller uses the AHOLD signal to float the CPU's address lines and to enable the 82496 Cache Controller to drive the snooping address. It then drives EADS# to indicate that the address is valid and should be strobed for the snoop. The Pentium processor will respond to the snoop with the HIT# and HITM# signals. HIT# active indicates that the line is a hit in the Pentium processor cache, and HITM# active indicates a hit to a modified line in the CPU cache. HIT# is not used by the 82496 Cache Controller, but can be accessed by the MBC if desired.

During back-invalidation cycles, the 82496 Cache Controller drives an additional line to the CPU, INV, which indicates that the snooped line should be invalidated at the end of the cycle. If INV is not asserted during Pentium processor snoop cycles (inquires), a snoop hit to the Pentium processor will leave the line in the [S] state in the Pentium processor cache. The 82496 Cache Controller drives INV active to the CPU during flush cycles, replacement write back cycles, and snoop cycles with invalidation (SNPINV active).

For snoop cycles which hit a modified line in the CPU cache, the Pentium processor will automatically schedule a write-back of the modified line to the 82496 Cache Controller/82491 Cache SRAM. The 82491 Cache SRAM will automatically merge the modified CPU data with the data in its write-back buffer or snoop buffer before completing the write-back on the memory bus.

The BOFF# signal is used to allow the aborting of CPU cycles during deadlock situations. Deadlocks may develop if the 82496 Cache Controller needs the CPU bus to perform an inquire write back cycle, and the CPU needs the bus to complete a transaction. In those cases

the 82496 Cache Controller will abort the CPU cycle by asserting BOFF# and will complete the snoop or replacement first.

When FLUSH# is asserted to the 82496 Cache Controller, the 82496 Cache Controller back-invalidates the CPU cache. If, during back-invalidation of the CPU cache, a modified line is hit, the Pentium processor issues a writeback cycle. When SYNC# is asserted to the 82496 Cache Controller, the 82496 Cache Controller inquires the Pentium processor cache on every 82496 Cache Controller cache hit to a modified line. Both flush and sync cycles can cause the write back of a modified line from the Pentium processor cache and the 82496 Cache Controller/82491 Cache SRAM.

3.8.3. Write Once Policy

The 82496 Cache Controller uses the WB/WT# signal to force the Pentium processor into a write-once mode. This signal is used to ensure that the 82496 Cache Controller will always be aware of Pentium processor potentially modified lines. The 82496 Cache Controller will only allow the Pentium processor to go into exclusive states if the 82496 Cache Controller itself is making a transition from Exclusive to Modified states or is already in M (e.g. from a previous cycle with DRCTM# asserted). This insures that for any Pentium processor exclusive line, the 82496 Cache Controller will be in a modified state. Whenever the 82496 Cache Controller is required to write-back a modified line to memory, it will first check the Pentium processor by executing an inquire cycle.

Read only lines are treated as valid and invalid only. Neither the 82496 Cache Controller nor the Pentium processor will cache read only lines in an exclusive or modified state. Therefore, a 82496 Cache Controller/82491 Cache SRAM line in an M or E state cannot have it's read only bit set.

3.8.4. MESI State Tables (Pentium Processor CPU-Cache Chip Set State Changes)

Table 3-1 shows the basic MESI state transitions which apply to both the Pentium processor and the 82496 Cache Controller/82491 Cache SRAM. The following tables (3-8, 3-9, 3-10) show the state changes of the Pentium processor and 82496 Cache Controller/82491 Cache SRAM during Read, Write, and Snoop cycles (respectively). The tables show the current and final cache line states of both the Pentium processor and 82496 Cache Controller/82491 Cache SRAM. They show the values of specific signals between the CPU and secondary cache which can affect the line state. CPU and Memory bus activities are also shown.

A signal marked as a don't care ('x') in the following tables indicates that the value of the signal is not used in determining the cache line state. The column labeled 'READ ONLY in 82496 Cache Controller/82491 Cache SRAM' represents either a valid line in the [S] state with the read only bit set or a memory bus access with MRO# returned active by the MBC.

The purpose of this section is to highlight Pentium processor state changes; therefore, all possible 82496 Cache Controller state changes are not covered. For a detailed description of 82496 Cache Controller/82491 Cache SRAM line state changes, refer to Tables 3-2 to 3-7.

Table 3-8. MESI State Changes for READ Cycles: CPU to 82496 Cache Controller/ 82491 Cache SRAM Caches

Cycle Type	Initial State of CPU	To Cache			Final State of CPU	CPU Bus Activity	Initial State of Cache	Read Only: Cache	To CPU		Final State of Cache	Memory Bus Activity	Notes
		PWT	D/C#	CACHE#					WB/WT#	KEN#			
Locked	'X'	x	x	1	I	Read	'X'	x	x	x	Same	Read	1
Not Locked	M,E,S	x	x	x	Same	None	M	NO	x	x	M	None	5
	I	x	x	1	I	Read	M	NO	x	x	M	None	5
	I	1	x	0	S	LFIL	M	NO	1	0	M	None	3,5
	I	0	1	0	E	LFIL	M	NO	1	0	M	None	3
	I	0	0	0	S	LFIL	M	NO	1	0	M	None	3,4,5
	S	x	x	x	S	None	E	NO	x	x	E	None	
	I	x	x	1	I	Read	E	NO	x	x	E	None	
	I	x	x	0	S	LFIL	E	NO	0	0	E	None	3
	S	x	x	x	S	None	S	x	x	x	S	None	
	I	x	x	1	I	Read	S	x	x	x	S	None	
	I	x	1	0	I	Read	S	YES	x	1	S	None	2
	I	x	1	0	S	LFIL	S	NO	0	0	S	None	3
	I	x	0	0	S	LFIL	S	x	0	0	S	None	3
	I	1	x	1	I	Read	I	x	x	x	S	LFIL	
	I	0	x	1	I	Read	I	x	x	x	M,E,S	LFIL	
	I	1	x	0	S	LFIL	I	NO	0	0	S	LFIL	
	I	0	x	0	S	LFIL	I	NO	0	0	M,E,S	LFIL	
	I	x	0	0	S	LFIL	I	YES	0	0	S	LFIL	6
	I	x	1	0	I	Read	I	YES	x	1	S	LFIL	6

NOTES:

CPU refers to Pentium™ processor.

Cache refers to 82496 Cache Controller/82491 Cache SRAM.

LFIL = Line Fill

Refer to Table 3-2 for 82496 Cache Controller state transition decisions.

1. A locked hit to a line in the Pentium processor cache will cause that line to transition to [I] independent of its original state. If the line was [M], it will be written back.
2. The 82496 Cache Controller does not return KEN# for data hits to Read-Only lines.
3. The 82496 Cache Controller only returns WB/WT# high on unlocked hits to [M] for which it also returns KEN# active.
4. The Pentium processor instruction cache never contains [M] state lines and does not distinguish between [S] and [E]. Refer to the *Pentium Processor Data Book* for more details.
5. WB/WT# is not used for the state transition decision.
6. MKEN# and MRO# sampled active.

Table 3-9. MESI State Changes for WRITE Cycles: CPU to 82496 Cache Controller/ 82491 Cache SRAM Caches

Cycle Type	Initial State of CPU	To Cache			Final State of CPU	CPU Bus Activity	Initial State of Cache	Read Only: Cache	To CPU		Final State of Cache	Memory Bus Activity	Notes
		PWT	D/C#	CACHE#					WB/WT#	KEN#			
Locked	**I**	x	x	1	**I**	WT	**'X'**	x	x	x	**Same**	WT	1
Not Locked	**M**	x	x	x	**M**	None	**M**	x	x	x	**M**	None	
	E	x	x	x	**M**	None	**M**	x	x	x	**M**	None	
	S	0	x	x	**E**	WT	**M**	x	1	x	**M**	None	2
	S	1	x	x	**S**	WT	**M**	x	1	x	**M**	None	2
	I	x	x	x	**I**	WT	**M**	x	x	x	**M**	None	3
	S	0	x	x	**E**	WT	**E**	x	1	x	**M**	None	
	S	1	x	x	**S**	WT	**E**	x	1	x	**M**	None	
	I	x	x	x	**I**	WT	**E**	x	x	x	**M**	None	3
	S	1	x	x	**S**	WT	**S**	x	0	x	**S**	WT	
	S	0	x	x	**S**	WT	**S**	x	0	x	**M,E,S**	WT	4
	I	1	x	x	**I**	WT	**S**	x	x	x	**S**	WT	3
	I	0	x	x	**I**	WT	**S**	x	x	x	**M,E,S**	WT	3,4
	I	1	x	x	**I**	WT	**I**	x	x	x	**I**	WT	
	I	0	x	x	**I**	WT	**I**	x	x	x	**M,E,S,I**	WT	

NOTES:

CPU refers to Pentium™ processor.

Cache refers to 82496 Cache Controller/82491 Cache SRAM.

WT = Write-Through

Refer to Table 3-3 for 82496 Cache Controller state transition decisions.

1. The locked write cycle always begins and ends with the Pentium processor cache line in state [I]. See Note 1 in the previous table.
2. The 82496 Cache Controller only returns WB/WT# high on unlocked write hits to [M] and [E].
3. The Pentium processor will not perform allocations on write cycles.
4. The Pentium processor cache state will not change. The 82496 Cache Controller cache line state will go to [E] if MWB/WT#=1 and DRCTM#=1. The 82496 Cache Controller cache line state will go to [M] if MWB/WT#=1 and DRCTM#=0. The 82496 Cache Controller cache line state will remain in [S] if MWB/WT#=0.

Table 3-10. MESI State Changes for SNOOP Cycles: 82496 Cache Controller/82491 Cache SRAM to CPU Caches

Initial State of CPU	To CPU: INV	Final State of CPU	CPU Bus Activity	Initial State of Cache	From Mem Bus: SNPNCA	From Mem Bus: SNPINV	Final State of Cache	Memory Bus Activity	Notes
M	0	S	INQR,WB	M	0	0	S	SWB	
M	1	I	INQR,BINV,WB	M	x	1	I	SWB	
M	0	S	INQR,WB	M	1	0	E	SWB	
E	0	S	INQR	M	0	0	S	SWB	
E	1	I	INQR,BINV	M	x	1	I	SWB	
E	0	S	INQR	M	1	0	E	SWB	
S	0	S	INQR	M	0	0	S	SWB	
S	1	I	INQR,BINV	M	x	1	I	SWB	
S	0	S	INQR	M	1	0	E	SWB	
I	1	I	INQR,BINV	M	x	1	I	SWB	
I	0	I	INQR	M	0	0	S	SWB	
I	0	I	INQR	M	1	0	E	SWB	
S	0	S	None	E	0	0	S	None	
S	1	I	BINV	E	x	1	I	None	
S	0	S	None	E	1	0	E	None	
I	1	I	BINV	E	x	1	I	None	
I	0	I	None	E	0	0	S	None	
I	0	I	None	E	1	0	E	None	
S	0	S	None	S	x	0	S	None	
S	1	I	BINV	S	x	1	I	None	
I	1	I	BINV	S	x	1	I	None	
I	0	I	None	S	x	0	S	None	
I	x	I	None	I	x	x	I	None	

NOTE:
CPU refers to Pentium™ processor.
Cache refers to 82496 Cache Controller/82491 Cache SRAM.
SWB = Snoop Write Back
INQR = Inquire (82496 Cache Controller snoops the Pentium processor)
BINV = Back Invalidate
Refer to Table 3-4 and Table 3-5 for 82496 Cache Controller state transition decisions.

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4

Cache Initialization and Configuration

CHAPTER 4
CACHE INITIALIZATION AND CONFIGURATION

This section describes the physical and mode configurations available when using the 82496 Cache Controller and 82491 Cache SRAM. Physical configuration determines the organization of the 512-Kbyte or 256-Kbyte cache. Mode configuration determines how the cache core operates and communicates with the memory bus.

The 82496 Cache Controller supports a wide variety of physical configurations and a variety of mode configurations. Physical and mode configuration decisions are based on arriving at a desired balance between performance and memory bus controller design complexity and cost.

Figure 4-1 summarizes the basic configurations available when using the 82496 Cache Controller/82491 Cache SRAM with the Pentium processor.

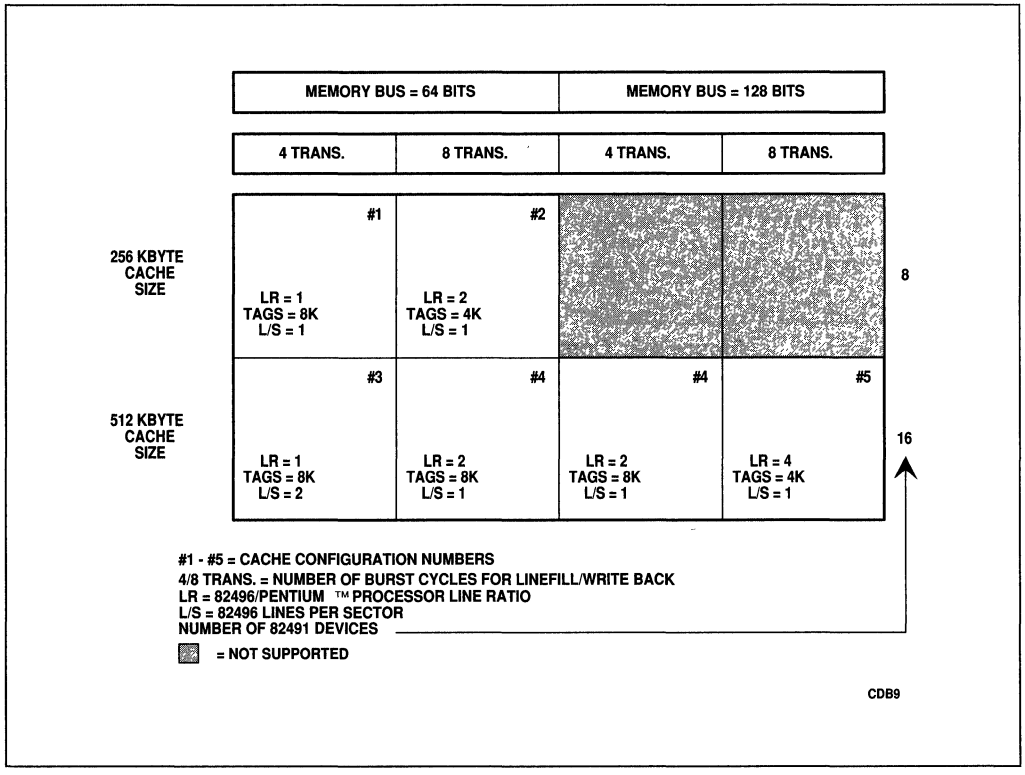


Figure 4-1. 82491 Cache Controller/82491 Cache SRAM Configurations with the Pentium™ Processor

4.1. CONFIGURATION SIGNAL SAMPLING DURING RESET

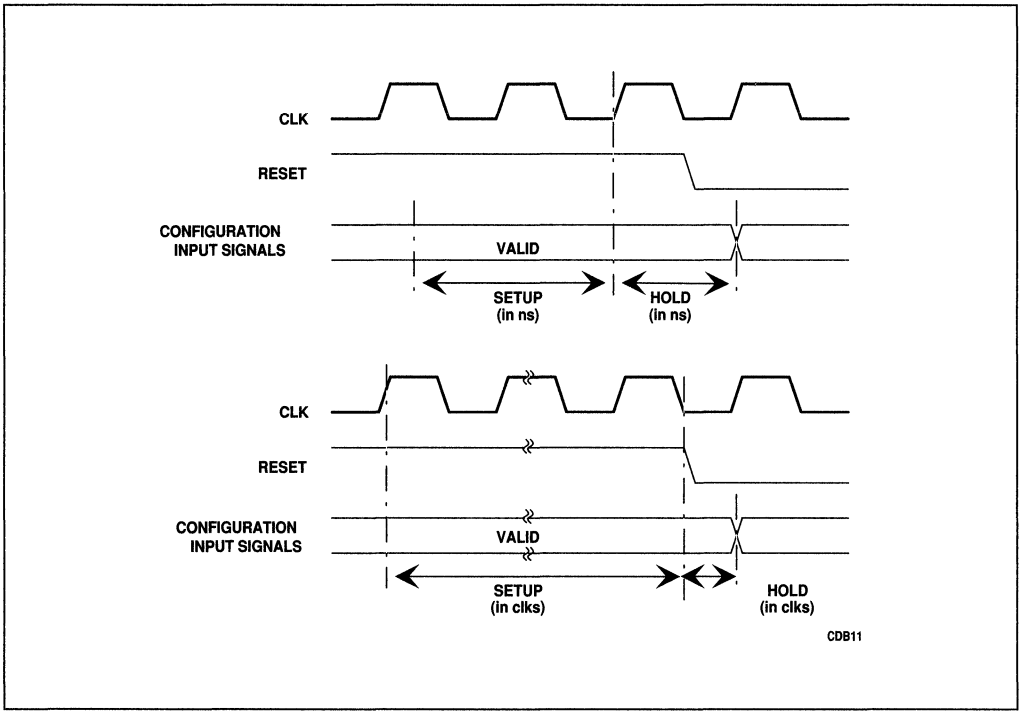


Figure 4-2. Configuration Input Sampling

82496 Cache Controller/82491 Cache SRAM core configuration inputs are sampled with respect to the falling edge of RESET (refer to Figure 4-2). The configuration inputs must meet the following timing requirements with respect to RESET:

1. The configuration inputs must meet setup and hold times with respect to each clock edge during reset (in ns.). The configuration input value sampled on the rising edge of CLK prior to RESET going inactive is used for configuration purposes.
2. The configuration inputs must meet setup and hold times with respect to the falling edge of RESET (in CLKs).
3. Configuration signals must be valid for 10 CLKs before the falling edge of RESET.

Signals that are used to configure the cache core may share pins with other signals.

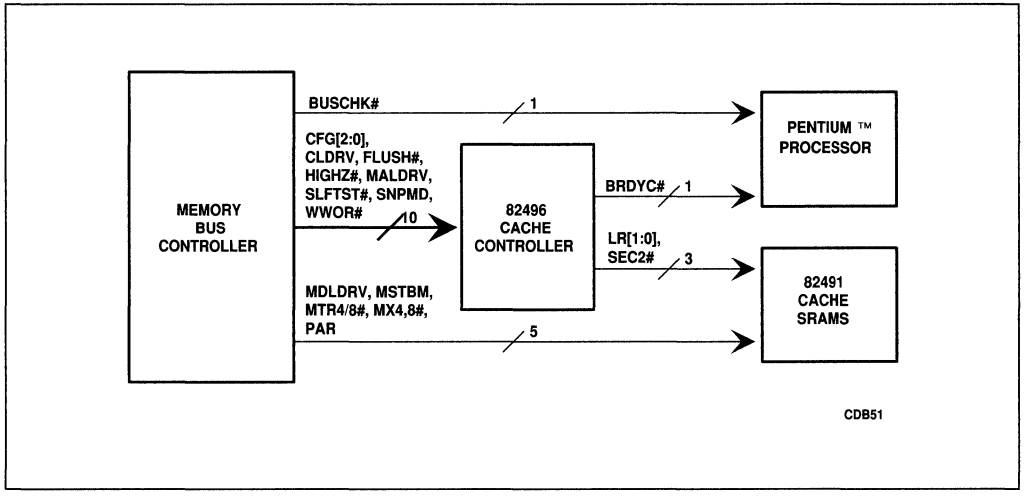


Figure 4-3. CPU-Cache Chip Set Configuration Inputs

Figure 4-3 shows all required configuration signals for each component in the CPU-Cache Chip Set as well as the device that provides each configuration signal.

4.1.1. Initialization Required for Chip Set Mode

The following reset sequence must be followed to configure the I/O buffers of the Pentium processor for use with the 82496 Cache Controller/82491 Cache SRAM:

1. BUSCHK# must be driven to the Pentium processor by the MBC for at least 4 clocks prior to the falling edge of RESET. BUSCHK# configures part of the Pentium processor address and control bus for one of two buffer sizes.
2. BRDYC# is driven low to the Pentium processor by the 82496 Cache Controller during reset to complete CPU-Cache Chip Set configuration requirements.

The 82496 Cache Controller to 82491 Cache SRAM control signals can also be configured for one of two buffers. The buffer selection is made by using the CLDRV configuration input. CLDRV must be driven by the MBC to the desired value for at least 10 CPU clocks prior to the falling edge of RESET.

Table 4-1 describes Intel's recommendation on how to drive BUSCHK# and CLDRV to configure the Pentium processor and 82496 Cache Controller output buffers for different cache configurations. System designers may use either buffer selection provided all flight time and signal quality specifications are met.

Table 4-1. Pentium™ Processor Chip Set Initialization Recommendations

Cache Size	Cache Configurations	BUSCHK# @RESET	CLDRV @RESET
256K	1,2	HIGH	HIGH
512K	3,4,5	LOW	LOW

To simplify the configuration process, the Pentium processor BUSCHK# input path should be designed such that a 0 ohm resistor connects the BUSCHK# pin to the inverse of RESET. The resistor allows the system designer to change the polarity of BUSCHK# with minimal impact to the system design. If the resistor is removed, this input is high due to the internal pullup resistor. If the resistor is in the circuit, the input is low (inverse of the active RESET). Note that the BUSCHK# input must meet all timings with respect to RESET as indicated in Figure 4-2 and in the text above.

The 82496 Cache Controller CLDRV signal shares a pin with the 82496 Cache Controller BGT# signal. During reset, the CLDRV pin should be driven low or high as shown in Table 4-7. During normal operation, this pin acts as the BGT# signal, and should be driven accordingly.

4.2. PHYSICAL CACHE

The 82496 Cache Controller/82491 Cache SRAM's physical configurations consist of basic architectural parameters determining line ratio, cache tagRAM size, lines per sector and bus width. These parameters are sampled in the CLK prior to RESET sampled inactive and cannot be dynamically changed. Table 4-2 shows the appropriate values of the configuration inputs, CFG[2:0], for each possible cache configuration.

Table 4-2. 82496 Cache Controller/82491 Cache SRAM Configuration Inputs

Config No.	Cache Size	Line Ratio	Lines/sec	No. of Tags	CFG2	CFG1	CFG0
1	256KB	1	1	8K	0	0	1
2	256KB	2	1	4K	1	1	1
3	512KB	1	2	8K	0	0	0
4	512KB	2	1	8K	0	1	1
5	512KB	4	1	4K	1	1	0

4.2.1. Memory Bus Width

The CPU-Cache Chip Set core supports 64- and 128-bit memory bus widths. Note that the system designer can choose to implement a 32 bit memory bus (this is NOT a configuration option).

4.2.2. Line Ratio

Line Ratio (LR) is the ratio between the 82496 Cache Controller/82491 Cache SRAM line size and that of the Pentium processor. If LR=2, for example, the 82496 Cache Controller/82491 Cache SRAM second-level cache line size is 64 bytes. Along with the bus width, the LR determines the number of transfers needed to fill a 82496 Cache Controller/82491 Cache SRAM cache line. Only one line is filled on each line fill cycle, regardless of sectoring. The LR is used to determine the number of inquires and back invalidations to the CPU.

4.2.3. TagRAM Size

The 82496 Cache Controller/82491 Cache SRAM tagRAM size can be configured with 4K or 8K tag entries. By reducing tagRAM size, the LR can be doubled without a change in cache size. TagRAM size is actually determined when selecting cache line size and bus width.

4.2.4. TagRAM Structure

Because there are many more lines in main memory than line locations in the cache, the 82496 Cache Controller uses address mapping. Given a physical address in main memory, mapping finds the cache location that contains the corresponding data. The 82496 Cache Controller uses a two-way set associative tagRAM address mapping mechanism (see Figure 4-4).

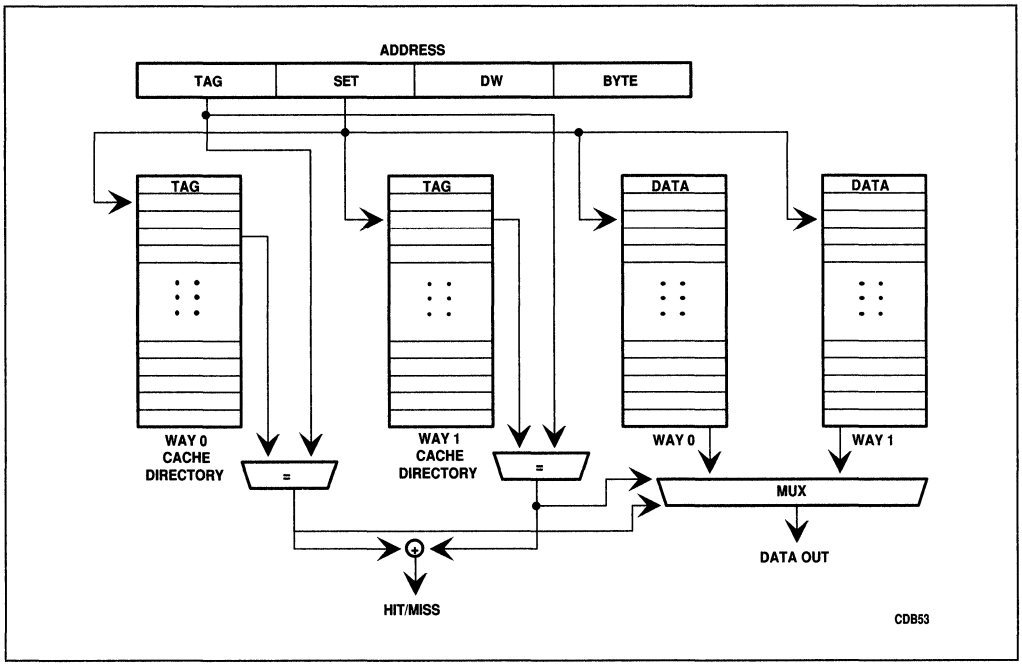


Figure 4-4. Two-Way Set Associative TagRAM Structure

The 82496 Cache Controller tagRAM memory can be configured in either 2K or 4K sets. A set is selected by direct mapping of 11 or 12 bits of the physical address, called the set-address bits (SET[10:0]). Each set contains two ways. Tags are composed of the additional physical address bits needed to identify the line(s) in the sector.

Figure 4-4 shows how the tag bits are stored in the tag array of the 82496 Cache Controller. The sectors corresponding to the tag bits are stored in the 82491 Cache SRAMs. Each sector has a tag. For 4K sets, there are 8K tags with 15 bits per tag. For 2K sets, there are 4K tags with 14 bits per tag.

A read only bit and two state bits are stored with each tag in the tag array of the 82496 Cache Controller. The read-only bit provides compatibility with certain shadow ROM techniques. The two state bits identify which lines contain valid data, help to implement deferred memory updating, and maintain consistency among multiple caches.

The explanation above assumes one line per sector. For configurations which use two lines per sector, the most significant DW bit is used to select which line in the sector is being accessed.

4.2.5. Lines per Sector (L/S)

The 82496 Cache Controller/82491 Cache SRAM can be configured as non-sectored (L/S=1) or with two lines per sector (L/S=2). If L/S=2, the 82496 Cache Controller contains one tag and Read-Only bit for each pair of consecutive cache lines. Each line has its own set of MESI state bits. This configuration enables a single line to be filled during line fills or written back during snoop hits. Both lines are invalidated and written back during replacements if both lines

are modified.

4.2.6. Cache Size

The 82496 Cache Controller/82491 Cache SRAM may be configured as 256K or 512K bytes in size. Cache size is directly proportional to the number of 82491 Cache SRAM devices used. Eight components comprise a 256K cache, while 16 can be combined to construct a 512K cache. Two 82491 Cache SRAM devices can be added to each cache size and configured to be data parity devices.

4.2.7. Configurable Address Connections

Table 4-3 lists which address lines should be connected to each of the CFA[6:0] lines for each cache configuration. CFA[6:0] provide the 82496 Cache Controller with proper multiplexed addresses for each of the possible cache configurations. They may be used as set addresses (S), tag addresses (T), line in sector address (L), 82496 Cache Controller subline address (CL), or CPU subline address (CS), and are passed along to the memory bus.

Table 4-3. Pentium™ Processor CFA Address Connections

Config Number	CFA6	CFA5	CFA4	CFA3	CFA2	CFA[1:0]	TAG [11:0]	SET [10:0]
1	A5(S)	VSS	A31(T)	A30(T)	A29(T)	A[4:3](CS)	A[28:17]	A[16:6]
2	A5(CL)	VSS	A31(T)	A30(T)	A29(T)	A[4:3](CS)	A[28:17]	A[16:6]
3	A6(S)	A5(L)	VSS	A31(T)	A30(T)	A[4:3](CS)	A[29:18]	A[17:7]
4	A6(S)	A5(CL)	VSS	A31(T)	A30(T)	A[4:3](CS)	A[29:18]	A[17:7]
5	A6(CL)	A5(CL)	VSS	A31(T)	A30(T)	A[4:3](CS)	A[29:18]	A[17:7]

The memory address bus signals, MCFA[6:0], correspond directly to the sequence in which the CPU address bus signals, CFA[6:0], are connected. In the cases where the CPU address signals are connected directly to VSS, the memory address signals must be left as no-connects (NC). Therefore, in configurations 1 and 2, MCFA5 is an NC and in configurations 3, 4, and 5, MCFA4 is an NC.

The 82496 Cache Controller memory address bus is controlled by four inputs: MALE and MBALE address latch enables, and MAOE# and MBAOE# address output enables. MALE and MAOE# control the 82496 Cache Controller line address signals (S,T,L), and MBALE and MBAOE# control the subline address signal (CL,CS). Table 4-4 describes which memory bus address signals are controlled by each of the above address control signals. Figure 4-5 shows the line and subline address latches.

Table 4-4. Memory Bus Address Control

Config #	Cache Size	(Line Address) (S,T,L) MALE and MAOE#	(Subline Address) (CL,CS) MBALE and MBAOE#	(NC) Unused pins
1	256KB	MCFA4-MCFA2, MTAG11-MTAG0, MSET10-MSET0, MCFA6	MCFA1, MCFA0	MCFA5
2	256KB	MCFA4-MCFA2, MTAG11-MTAG0, MSET10-MSET0	MCFA6, MCFA1, MCFA0	MCFA5
3	512KB	MCFA3, MCFA2, MTAG11-MTAG0, MSET10-MSET0, MCFA6, MCFA5	MCFA1, MCFA0	MCFA4
4	512KB	MCFA3, MCFA2, MTAG11-MTAG0, MSET10-MSET0, MCFA6	MCFA5, MCFA1, MCFA0	MCFA4
5	512KB	MCFA3, MCFA2, MTAG11-MTAG0, MSET10-MSET0	MCFA6, MCFA5, MCFA1, MCFA0	MCFA4

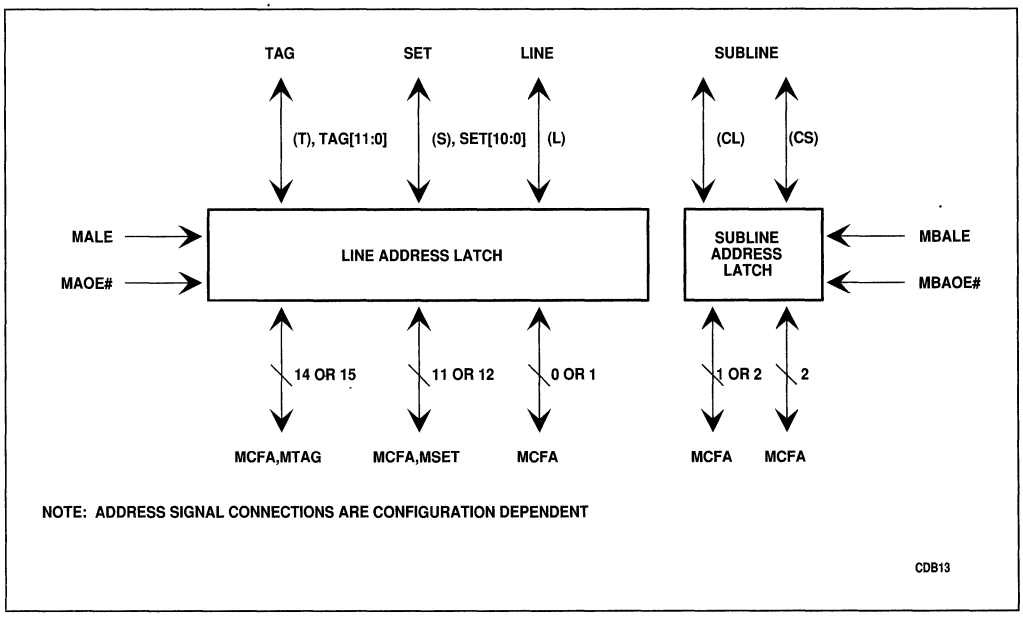


Figure 4-5. Address Latching

4.2.8. 82491 Cache SRAM Bus Configuration

The 82491 Cache SRAM needs to be configured to drive either 4 or 8 MDATA lines. The 82491 Cache SRAM configuration also determines whether the cache SRAM performs 4 or 8 memory transfers per linefill. The 82491 Cache SRAM is configured through the MX4/MX8# and the MTR4/MTR8# configuration inputs. For a given line ratio (memory bus line size /

CPU line size), these configuration inputs should be sampled as shown in Table 4-5.

Table 4-5. MX/MTR Configurations

Config #	Cache Size	Line Ratio	MX4 / MX8# @RESET	MTR4 / MTR8# @RESET	Memory Bus Width	Mem/CPU Bus I/O Pins	# Memory Bus Transactions	# Cache SRAM Devices
1	256KB	1	0	1	64	8/8	4	8
2	256KB	2	0	0	64	8/8	8	8
3	512KB	1	1	1	64	4/4	4	16
4	512KB	2	1	0	64	4/4	8	16
4	512KB	2	0	1	128	8/4	4	16
5	512KB	4	0	0	128	8/4	8	16

NOTE: When only 4 CPU or Memory Data bus pins are needed, the lower order 4 pins are used (i.e. CDATA[3:0] or MDATA[3:0]).

4.2.9. 82491 Cache SRAM Parity Configuration

A 82491 Cache SRAM may be designated as a parity device by driving the MBE# [PAR#] pin low during reset. In parity configuration, CDATA[3:0] are used to store 4 parity bits, and CDATA[7:4] are used as 4 bit enables. The four bit enables allow the writing of individual parity bits.

Every mode and configuration of a non-parity 82491 Cache SRAM may be used and selected on the parity 82491 Cache SRAM device. The 82491 Cache SRAM parity configurations are as shown in Table 4-6.

Table 4-6. Parity Configurations

Configuration Number	Cache Size	Memory Bus Width	# of Parity Devices	82491 Cache SRAM I/O bits (Mem/CPU)
1,2	256K	64	2	4/4
3,4	512K	64	2	4/4
4,5	512K	128	2	8/4

4.2.10. CPU to 82491 Cache SRAM Address Configurations

The 82491 Cache SRAM Address inputs (A) are connected to the CPU address lines (CA) according to the cache size (see Table 4-7).

Table 4-7. 82491 Cache SRAM Address Connections

Config #	Cache Size	82491 Cache SRAM Address Pins															
		A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1,2	256K	CA 16	CA 15	CA 14	CA 13	CA 12	CA 11	CA 10	CA 9	CA 8	CA 7	CA 6	CA 5	CA 4	CA 3	Vss	Vs s
3,4,5	512K	CA 17	CA 16	CA 15	CA 14	CA 13	CA 12	CA 11	CA 10	CA 9	CA 8	CA 7	CA 6	CA 5	CA 4	CA 3	Vs s

4.2.11. Bus Driver Buffer Selection

The 82496 Cache Controller memory bus address signals, MCFA[6:0], MSET[10:0], MTAG[11:0], and MAP can be configured for one of two buffers. The buffer selection depends upon the load on these signals and should be based on simulation results of these signals driving that load. The 82496 Cache Controller configuration input, MALDRV, is used to select the buffer. Refer to Table 7-26 for the buffer selection specifications, and the appropriate value of MALDRV.

Each 82491 Cache SRAM data signal, MDATA[7:0] can be configured for one of two buffers. The buffer selection depends upon the load on these signals and should be based on simulation results of these signals driving that load. The 82491 Cache SRAM configuration input, MDLDRV, is used to select the buffer. Refer to Table 7-26 for the buffer selection specifications, and the appropriate value of MDLDRV.

CLDRV selects the driving strength of the 82496 Cache Controller buffers that interface to the 82491 Cache SRAM.

4.3. CACHE MODES

Cache mode options are sampled at reset and cannot be dynamically changed. When cache mode configuration settings share a pin with another signal (e.g. SYNC# and MDLDRV), the configuration option must meet a designated setup and hold time relative to the last CLK edge in which RESET is sampled active. While the setup time differs (between the 82496 Cache Controller and 82491 Cache SRAM devices) for each configuration input, all configuration options must be held until the CLK prior to RESET being sampled LOW.

4.3.1. Memory Bus Modes

The Pentium processor and 82496 Cache Controller/82491 Cache SRAM operates at maximum clock frequency. Because it is difficult to design a memory system at the same high frequency, the 82496 Cache Controller/82491 Cache SRAM provides two memory bus communication modes. These modes allow the memory bus to run at the frequency the designer chooses.

The two modes, Clocked Memory Bus Mode and Strobed Memory Bus Mode, affect communication and handshaking of the CPU-Cache Chip Set data path and data control

signals. The cycle control signals are synchronous with the CPU/cache core clock frequency (CLK). The CPU and memory address path signals are synchronous to CLK during normal read, write, and replacement write-back cycles. Address control signals are asynchronous. Snoop address control signals, depending upon the snoop mode, may be asynchronous or synchronous to SNPCLK during snoop operations.

4.3.1.1. CLOCKED MODE

In clocked memory bus mode, the Memory Bus Controller (MBC) provides the 82491 Cache SRAM with a memory clock (MCLK) input which drives and provides sampling times for all data path signals. The system designer can select from one of three MCLK frequencies:

MCLK = CLK — This selection provides a synchronous memory bus. Because all signals are driven at very HIGH frequencies, memory bus logic is fast and complex. However, this selection eliminates the need for a synchronization interface between memory bus and cycle control signals.

MCLK*N = CLK — This selection provides a divided synchronous memory bus. The memory bus operates at a reduced speed, thereby simplifying design, while only minimal synchronization is needed to interface memory bus and cycle control signals.

MCLK < CLK — This selection provides an asynchronous memory bus. MCLK may be any frequency that optimizes the memory bus. Synchronization is required to interface memory bus and cycle control signals.

4.3.1.2. STROBED MODE

In strobed memory bus mode, all signals are related to other signals. Clocks are not used to control the data path. For example, data may be strobed into the 82491 Cache SRAM according to the rising and falling edges of MISTB. Because operation is based on handshaking, strobed mode eliminates the need for clocks and clock skews. Strobed mode does require synchronization in interfacing memory bus and cycle control signals.

4.3.1.3. CONFIGURATION OF MEMORY BUS MODE

To put the 82491 Cache SRAM into the Clocked Memory Bus Mode, the memory bus controller (MBC) supplies a clock input to the MCLK pin, which the 82491 Cache SRAM detects at reset. If MCLK is driven HIGH or LOW (MSTBM) at reset, the 82491 Cache SRAM enters Strobed Memory Bus Mode.

4.3.2. Snoop Modes

The 82496 Cache Controller can be configured to one of three different snoop modes. The snoop mode determines how the MBC initiates a snoop to the cache. Regardless of the snoop initiation mode, the 82496 Cache Controller responds to snoops synchronous to CLK.

Snooping may be initiated in Synchronous, Clocked or Strobed Snoop Modes. The snoop mode is not related to the memory bus mode selected for the 82491 Cache SRAM (data path).

MBC snooping begins when the snoop strobe (SNPSTB#) signal is asserted. Subsequently, the 82496 Cache Controller samples other snoop information (e.g. the snoop address) and begins a snoop cycle. The snooping mode determines how the 82496 Cache Controller samples SNPSTB# and other snoop information.

In Synchronous Snoop Mode, SNPSTB# and other snoop indicators are sampled with the rising edge of CLK. As a result, the 82496 Cache Controller can begin a snoop without synchronization and provide quick responses.

In Clocked (Asynchronous) Snoop Mode, SNPSTB# and other snoop indicators are sampled with the rising edge of snoop clock (SNPCLK), which the MBC can provide at any desired frequency (less than or the same as CPU CLK). The 82496 Cache Controller synchronizes snoop information internally before the snoop begins.

In Strobed Snoop Mode, all snoop information is sampled with the falling edge of SNPSTB#. The 82496 Cache Controller synchronizes snoop information internally before the snoop begins.

4.3.2.1. CONFIGURATION OF SNOOP MODE

The snoop mode is determined at reset using the SNPCLK [SNPMD] pin. If this pin is tied LOW, Synchronous Snooping Mode is selected. If tied HIGH, Strobed Snooping Mode is selected. To select Clocked Snooping Mode, the snoop clock source must be connected to the SNPCLK pin. The 82496 Cache Controller will automatically detect the clock and enter Clocked Snooping Mode.

4.3.3. Strong/Weak Write Ordering

4.3.3.1. DESCRIPTION

A system which maintains strong write ordering preserves the sequential ordering of memory write accesses as they are performed. In processors or systems which contain write buffers and utilize caching, the order of memory accesses can sometimes fall out of program order. When the 82496 Cache Controller is configured to be strongly write ordered, it prevents the chip set from writing data to the bus in any order other than that in which it was received from the CPU.

A weakly write ordered system can provide greater system design flexibility and slightly higher performance. When the 82496 Cache Controller is configured to be weakly write ordered, it will always drive the EWBE# signal active to the CPU. This allows the Pentium processor to continue issuing writes to 'E' or 'M' in the CPU data cache.

Strongly ordered systems require that instruction execution order be limited to program order. Increasing the system performance can, therefore, be difficult. A benefit in strongly ordered systems is that software compatibility is guaranteed. Weakly ordered systems, on the other hand, completely remove the restrictions on the order of memory accesses; therefore, there may be software compatibility consequences. When choosing a 82496 Cache Controller memory write ordering mode, system software compatibility must be maintained.

In systems with multiple CPU-Cache Chip Set subsystems, write ordering may be violated (ie. the CPU can receive stale data) when the 82496 Cache Controller has been configured as strongly write ordered. Refer to section 5.1.10 for a description and the memory bus controller rules which will allow the 82496 Cache Controller to operate in strong write ordered mode without coherency problems.

4.3.3.2. CONFIGURATION

If the 82496 Cache Controller WWOR# pin is sampled LOW during RESET, the 82496 Cache Controller operates with weak write-ordering. If the WWOR# pin is sampled HIGH during RESET, the 82496 Cache Controller operates with strong write-ordering.

5

Hardware Interface

CHAPTER 5
HARDWARE INTERFACE

5.1. MEMORY BUS CONTROLLER CONSIDERATIONS

This section explains the functions of a memory bus controller (MBC) for the Pentium processor CPU-Cache Chip Set. The MBC provides the 82496 Cache Controller/82491 Cache SRAM's interface to the system memory bus and to any other bus masters. The MBC serves four primary functions: cycle control, snooping, data control and synchronization.

The 82496 Cache Controller begins each memory bus cycle by signaling the MBC, which then arbitrates, acquires the bus, and begins the cycle. Once a cycle is in progress on the bus, the MBC determines if any other cache in the system contains modified data of the line in progress by signalling these caches to snoop. If another cache signals that it contains modified data, the MBC permits that cache to write out the modified data before it completes the cycle. Once transfers have been completed, the MBC ends the cycle.

When a 82496 Cache Controller/82491 Cache SRAM is not the bus master, the MBC handles snoops from other 82496 Cache Controller/82491 Cache SRAMs or bus masters. If such a snoop is hit to a modified line, the MBC writes the modified data to memory.

The MBC controls data transfers using the BRDY# signal to the CPU for I/O and memory read cycles. The MBC also decodes all memory bus cycles, determines their length and cacheability, and controls them appropriately. Because the CPU core may be running at a different speed than the memory bus, the MBC provides proper handshaking and synchronization. Figure 5-1 shows an MBC block diagram.

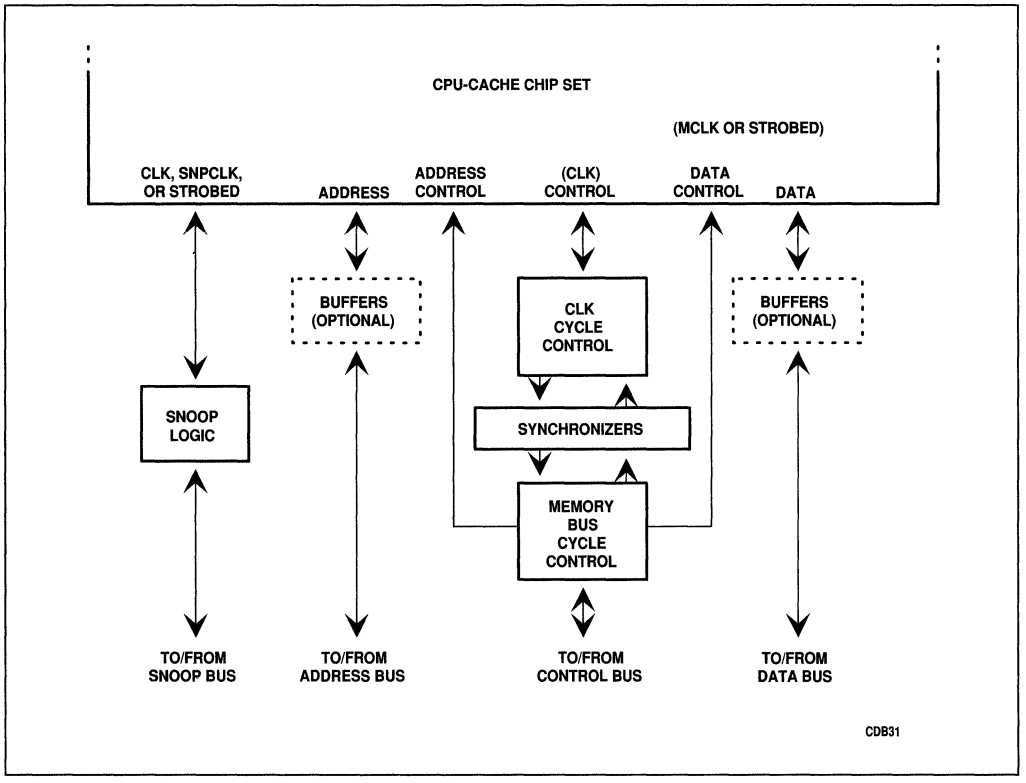


Figure 5-1. MBC Block Diagram

5.1.1. Cycle Control

The 82496 Cache Controller/82491 Cache SRAM can handle unlocked read and write hits to the [E] and [M] states and unlocked read hits to [S] state independently of the MBC and the system. All other cycles require access to memory bus, arbitrated by the MBC.

Cycles on the memory bus are requested by the 82496 Cache Controller to the MBC with address and data strobe outputs. The memory bus controller responds to the request with cycle progress signals and cycle attributes (sampled by the 82496 Cache Controller with select progress signals). Figure 5-2 shows the signals used by the 82496 Cache Controller to request memory bus cycles, and the signals expected from the MBC in order for a cycle to complete normally.

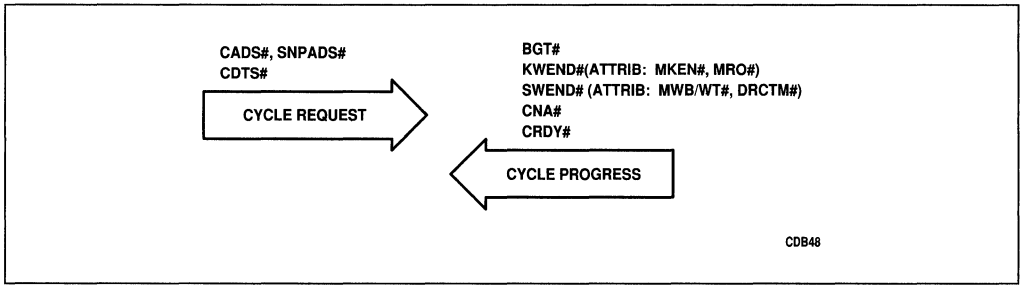


Figure 5-2. Memory Bus Cycle Progress and Attribute Signals

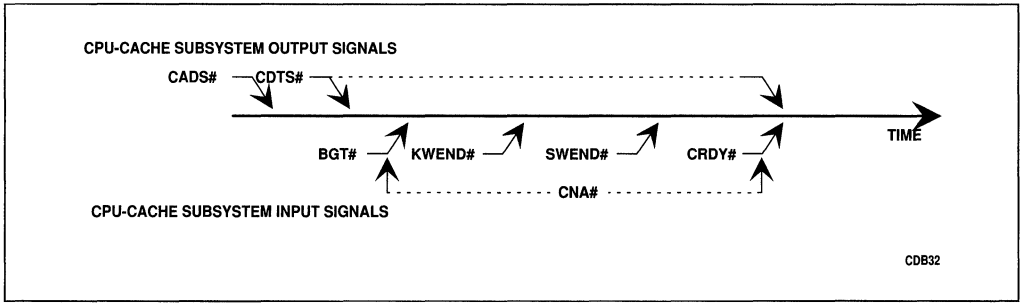


Figure 5-3. Cycle Progress Signals and Responses

Figure 5-3 shows the 82496 Cache Controller signals, and their order (left to right), which affect the progress of a memory bus cycle. The 82496 Cache Controller begins memory bus cycles by asserting the Cache Address Strobe (CADS#) signal, which is generated along with cycle and address control information. CADS# remains active for one CLK to indicate that the 82496 Cache Controller/82491 Cache SRAM is requesting a memory cycle and that the cycle and address control information is valid on the bus.

At this point, the bus may be controlled by another bus master which could activate a snoop to the 82496 Cache Controller. If a snoop hits a modified location (before BGT# of that cycle), the 82496 Cache Controller aborts the request and generates a snoop write-back cycle, which writes back the modified data. Following the snoop write-back, the 82496 Cache Controller usually re-submits the previously aborted memory cycle request. An exception is when a snoop hit occurs to the write-back buffer when the buffer is waiting for the bus. Because the contents of the write-back buffer are written out in response to the snoop hit, the write-back cycle is not re-issued.

With, or some time after CADS# is asserted, the 82496 Cache Controller asserts the Cache Data Strobe signal (CDTS#), which indicates to the MBC that the 82491 Cache SRAM's data path is ready. For read cycles, CDTS# indicates that the CPU bus is free and that the MBC may generate BRDY# in the next CLK to begin data transfer to the CPU. For write cycles, CDTS# indicates that data is available on the memory bus and MBRDY# can be issued in the next CLK. CADS# and CDTS# provide independent address and data information, which are especially useful in pipelining.

When MBC wins memory bus control, it asserts the Bus Guaranteed Transfer Signal (BGT#)

to the 82496 Cache Controller to indicate that the cycle will not be aborted. By quickly returning BGT#, the MBC can begin pipelining using the Cache Next Address signal (CNA#)

At this point, the MBC is driving the bus and provides the address and cycle information needed to begin the cycle. Once the memory system has decoded the address to determine cacheability and read-only status, it signals the MBC to assert the Cacheability Window End signal (KWEND#). On the CLK during which KWEND# is asserted, the 82496 Cache Controller samples the Memory Cache Enable (MKEN#) and Memory Read Only (MRO#) parameters. Quick resolution of KWEND# determines whether the cycle is cacheable and allows the 82496 Cache Controller to initiate replacements or allocations, when needed.

Because the MBC drives the bus with the address, other system caches must snoop to check for modified copies of the data, invalidate their copies of the current data, or mark exclusive (unmodified) data shared if another cache will be using it. If any of them contains a modified line, it must flag the MBC that owns the bus to prevent stale data from being used. If all other caches contain unmodified or invalid data, they flag the MBC to initiate appropriate MESI state changes.

The period beginning with CADS# assertion and ending when all caches have provided snoop responses is called the snoop window. At the end of this period, the MBC asserts the Snoop Window End signal (SWEND#). It indicates to the 82496 Cache Controller that snooping is complete and that MWB/WT# and DRCTM# are valid. At this point, the 82496 Cache Controller can determine which tag state transitions will be caused by the cycle and service snoop requests from other bus masters.

SWEND# indicates to the MBC that data transfers may begin. The MBC may begin transfers early, anticipating that no other cache has modified data. If another cache does need to write-back modified data, the MBC must re-start the transfers. When all transfers are completed, the MBC asserts CRDY# and MEOC# to end the cycle and allow the 82496 Cache Controller/82491 Cache SRAM to free their internal resources for the next cycle.

Once BGT# is asserted, the 82496 Cache Controller allows pipelining requests, which are initiated using CNA#. If a memory cycle is pending, the 82496 Cache Controller generates a new CADS#, along with new address and control information.

The 82496 Cache Controller allows full internal address latch control, which is especially useful during pipelining. The MALE and MBALE signals are latch enable inputs, and MAOE# and MBAOE# are output enable control signals. These signals are asynchronous and are used to control the last stage of the 82496 Cache Controller memory bus address.

5.1.1.1. IDENTIFYING AND EXECUTING CYCLES

This section describes how the MBC identifies the various 82496 Cache Controller/82491 Cache SRAM cycles and discusses the number of transfers needed to service each cycle.

The MBC identifies cycles by sampling the CADS#, CM/IO#, CW/R#, CD/C#, MCACHE# and SNPADS# outputs. The MBC determines the number of CPU bus and memory bus transfers required to execute each cycle by decoding the above signals and by determining the values of the following 82496 Cache Controller signals: MKEN# (82496 Cache Controller input), MRO# (82496 Cache Controller input), RDYSRC (82496 Cache Controller output), CCACHE# (82496 Cache Controller output), CD/C# (82496 Cache Controller output). If a cycle is CPU cacheable, the CPU requires four transfers (CPU is executing a linefill). If a cycle is 82496 Cache Controller/82491 Cache SRAM cacheable, the 82496 Cache

Controller/82491 Cache SRAM requires four or eight transfers. The 82496 Cache Controller/82491 Cache SRAM configuration determines whether the 82496 Cache Controller/82491 Cache SRAM requires four or eight transfers.

The 82496 Cache Controller/82491 Cache SRAM services read and write hit cycles to the [E] or [M] states and reads to the [S] state without MBC control. The MBC must be employed to identify and control all other 82496 Cache Controller cycles. Table 5-1 lists all 82496 Cache Controller cycles that require MBC control.

Table 5-1. Cycle Identification and Length

Cycle Type	CW/R#	CD/C#	CCACHE#	RDYSRC	MCACHE#	MKEN#	MRO#	Number of Memory Bus MBRDY#s*	Number of CPU Bus BRDY#s
Pentium™ processor CPU-Cache Chip Set Cacheable Read	0	1	0	1	0	0	1	82496 Cache Controller Line	4 (processor Line)
Pentium Processor CPU-Cache Chip Set Cacheable Read	0	0	0	1	0	0	x	82496 Cache Controller Line	4 (processor Line)
82496 Cache Controller/82491 Cache SRAM (not Pentium processor) Cacheable Read	0	x	1	1	0	0	x	82496 Cache Controller Line	1
82496 Cache Controller/82491 Cache SRAM (not Pentium processor) Cacheable Read	0	1	0	1	0	0	0	82496 Cache Controller Line	1
Non Cacheable Read (PCD=1 or Locked)	0	x	x	1	1	x	x	x	1
Non Cacheable Read (PCD=0)	0	x	x	1	x	1	x	x	1
82496 Cache Controller/82491 Cache SRAM Allocation (linefill)	0	x	x	0	0	x	x	82496 Cache Controller Line	0
Pentium Processor Memory Write or Locked Write	1	x	1	0	1	x	x	1	0
Replacement or Snoop Write Back	1	x	x	0	0	x	x	82496 Cache Controller Line	0
I/O (CM/IO#=0) or Special Cycle	x	x	x	1	1	x	x	x	1

NOTE: A 82496 Cache Controller line is either 4 or 8 memory bus burst transfers. The number of transfers is related to the configuration and depends upon the MTR4/8# input.

*This column represents the number of data transfers which the 82491 Cache SRAM will be expecting. In clocked memory bus mode, the 82491 Cache SRAM uses MBRDY# to transfer data to/from its buffers. In strobed memory bus mode, any transition on MISTB/MOSTB will cause the 82491 Cache SRAM to latch/output data. In either mode, MEOC# may replace the last MBRDY#, MISTB, or MOSTB. An "x" represents either 0 or 1 transfers. The 82491 Cache SRAM will ignore an extra MBRDY#, MISTB, or MOSTB, if asserted.

The text that follows describes 82496 Cache Controller cycles that both require and do not require MBC identification and control.

5.1.1.1.1. Read Hit

Read hit cycles are reads to the [M],[E], or [S] cache states. The 82496 Cache Controller/82491 Cache SRAM returns information to the CPU without wait-states or in one wait-state, and transparently to the MBC.

During read hit cycles, the 82496 Cache Controller/82491 Cache SRAM returns either a complete line or a portion of a line to the CPU. If a line is marked read-only and data, the 82496 Cache Controller automatically de-asserts KEN# to the CPU so that the information is not cached in the Pentium processor data cache. If a line is code (including read-only) or is non-read-only data, the 82496 Cache Controller will hold KEN# asserted to the CPU to cache the information in the Pentium processor code or data cache.

5.1.1.1.2. Cacheable Read Miss

Read miss cycles cause the 82496 Cache Controller to assert CADS# and request the needed code/data from the memory bus. If the information is cacheable in the 82496 Cache Controller/82491 Cache SRAM, the 82496 Cache Controller asserts the MCACHE# pin to the MBC. During the cycle, the MBC returns MKEN# active to render the line cacheable.

Because the needed information is cacheable to the CPU and the 82496 Cache Controller/82491 Cache SRAM, both require a complete cache line of information. The CPU receives four transfers while the 82496 Cache Controller/82491 Cache SRAM cache receives four or eight, depending on the configuration.

The exception to this rule is a data line-fill in which MRO# is asserted before the first transfer or when CCACHE# and CPCD are inactive. When MRO# is asserted with KWEND#, the 82496 Cache Controller/82491 Cache SRAM caches the entire line (four or eight transfers, depending on the selected configuration). The Pentium processor will, in turn, cache read only information if D/C# is low (code), but not if D/C# is high (data). If CCACHE# and CPCD are both inactive, then the line is cacheable by the 82496 Cache Controller/82491 Cache SRAM and not by the Pentium processor. In this case, the 82496 Cache Controller/82491 Cache SRAM receives four or eight transfers and the Pentium processor only requires one.

Once the 82496 Cache Controller has snooped the other caches for a possible modified line, the MBC asserts SWEND# to put the line in an appropriate MESI state. If the snoop results in a hit to a modified line and the line in the other cache is not invalidated (i.e., SNPINV not asserted), MWB/WT# is driven low to place the line in the shared state. If the line originated from another cache without memory being updated, DRCTM# causes a transition to a modified state.

If both cache WAYS are occupied, the 82496 Cache Controller must initiate a replacement cycle (described later in this section).

Because a 82496 Cache Controller line can be longer than a CPU cache line, there are circumstances where a read miss will be to a line that is currently being filled. If this is the case, the 82496 Cache Controller treats this like a read hit, but supplies data after CRDY# for the line fill. Data is supplied from the 82491 Cache SRAM array.

5.1.1.1.3. Non-Cacheable Read Miss

A non-cacheable read miss is created in several circumstances. If MCACHE# is inactive with CADS#, the line is non-cacheable, regardless of MKEN#. Also the line will not be cacheable if MKEN# is returned inactive, CPCD is active, or the cycle is Locked (KLOCK# active).

If the cycle is non-cacheable, the 82496 Cache Controller will not cache the information. Still, the 82496 Cache Controller/82491 Cache SRAM must return data to the Pentium processor. The number of transfers expected by the CPU is always one for non-cacheable cycles.

5.1.1.1.4. Write Hit [E], [M]

Write hits to the [E] and [M] states are executed within the 82496 Cache Controller/82491 Cache SRAM and transparently to the MBC. The 82491 Cache SRAM's data array is also updated. If the line was in the [E] state, it is upgraded to the [M] state. [M] data remains in the [M] state.

5.1.1.1.5. Write Hit [S]

Write hits to the [S] state are write-through cycles. The 82491 Cache SRAM updates its cache information and posts the write on the memory bus. CADS# is asserted for the write cycle. The data is written to memory, and all other caches are snooped to invalidate copies of the altered line.

If the line is not marked read-only and PWT is not active, it may be upgraded to [E] or [M] states (other caches would have to invalidate that line, if present).

5.1.1.1.6. Write Miss: No Allocation, Allocation

Write misses are writes to the [I] states and are executed similarly to write hits to the [S] state. As long as the write is a miss and PCD, PWT and LOCK# are inactive, PALLC# is asserted by the 82496 Cache Controller to indicate to the MBC that the line might be allocated.

If PALLC# is asserted, the MBC may perform an allocation. The MBC indicates this selection to the 82496 Cache Controller by asserting MKEN# during the write cycle. If MKEN# is not asserted, the allocation is not carried out.

If allocation is selected, the 82496 Cache Controller drives a new CADS# for the allocation cycle using the same address used for the write. This cycle progresses like a cacheable read miss except that the CPU receives no data (KWEND# is also ignored). RDYSRC is inactive, telling the MBC not to generate BRDY#s. The write cycle and allocation cycle need not be contiguous (except during Read For Ownership), and snooping is permitted between the two.

The 82491 Cache SRAM offers a Read For Ownership option which freezes the data from the write cycle in the 82491 Cache SRAM's memory buffer to allow the allocation to fill locations surrounding the just written portion. Carried out using MFRZ#, this operation permits write allocation without actually executing a write to memory. Snoops are forbidden between the

BGT# of the write cycle until the BGT# of the Allocation, or the snoop results may provide stale data. Refer to Section 5.1.1.11 for more information.

5.1.1.1.7. Replacement

During a 82496 Cache Controller/82491 Cache SRAM line fill, a line is placed in the 82496 Cache Controller/82491 Cache SRAM's. If both cache ways are full, one way must be discarded to make room for the new line. If the line to be discarded is in the modified state, it must be written back to memory and this write back is called a replacement write back cycle.

The 82496 Cache Controller generates CADS# for the replacement write back cycle immediately after the line fill completes with CRDY# assertion or after CNA#. The line fill and replacement cycle need not be contiguous, and snooping is allowed between them because the replacement information contained in the write-back buffer may still be snooped.

When MCACHE# is active during a memory write cycle, it is a replacement write-back. The write will accept a cache line of four or eight transfers depending on the 82496 Cache Controller/82491 Cache SRAM configuration.

Because a modified line is being expelled, the 82496 Cache Controller performs an inquire and back-invalidation to the Pentium processor to maintain inclusion.

5.1.1.1.8. Snoop Write Back

A snoop write back cycle is generated when a snoop hits a modified 82496 Cache Controller/82491 Cache SRAM line. The 82496 Cache Controller responds with the MHITM# signal asserted and then drives the SNPADS# signal. SNPADS# is provided because the MBC must receive indication that a snoop write back must be serviced immediately, because some other device is waiting for the data.

The 82496 Cache Controller places the snoop information in the snoop buffer and then drives CDTS#. While the information is being placed in the buffer, the 82496 Cache Controller performs inquires and back-invalidations to the Pentium processor cache to maintain inclusion. The 82496 Cache Controller will not drive CDTS# active until all inquire cycles have completed on the CPU bus.

The MBC handles this cycle like a replacement write back cycle, providing four or eight transfers to the 82491 Cache SRAM and no transfers to the CPU.

Snoop write back cycles are not pipelined into a preceding memory bus cycle, and no memory bus cycle is pipelined into a preceding snoop write back cycle.

5.1.1.1.9. Locked

Locked cycles are composed of "read-modify-write" cycles. The 82496 Cache Controller asserts the KLOCK# signal to echo the CPU LOCK# output. Cycles to the locked address(es) must run contiguously on the memory bus. Snoops to any address other than the locked address(es) are allowed to interrupt the RMW sequence. The Pentium processor automatically inserts one idle CLK between back to back Locked sequences. Therefore, KLOCK# is guaranteed to go inactive for at least one CLK.

The 82496 Cache Controller/82491 Cache SRAM will post Locked reads and writes to the memory bus even when the read or write is a hit. If the Locked read is a hit to a modified line,

the 82496 Cache Controller/82491 Cache SRAM cache will ignore the data that it receives from the memory bus and supply the data to the CPU from the 82491 Cache SRAM array (in accordance with the BRDY#s supplied by the MBC). Locked writes are posted like any other write. Locked cycles, both reads and writes, never change the 82496 Cache Controller tag state.

The 82496 Cache Controller/82491 Cache SRAM will post locked reads and writes to the memory bus even when the read or write is a hit. If the locked read is a hit to modified data, the 82496 Cache Controller/82491 Cache SRAM cache returns data to the CPU, and memory data is ignored.

Locked cycles are non-cacheable by the CPU and by the 82496 Cache Controller/82491 Cache SRAM. For this reason they are treated just like non-cacheable read misses and write misses.

The CSCYC output is only active during locked sequences in which the access is split over two addresses (LOCK# and SCYC active).

5.1.1.1.10. Cache-To-Cache Transfer

A cache-to-cache transfer may be done when the 82496 Cache Controller/82491 Cache SRAM must perform a line fill or allocation by transferring data directly from another cache. The 82496 Cache Controller/82491 Cache SRAM assumes that this data is being updated in main memory as well. Otherwise, the data must be marked as modified and the cache supplying the data must invalidate its copy.

If the data is shared with main memory, the caches mark their copies of the data as shared. For the supplying cache, this designation is done automatically when the cache is snooped by another cache. For the receiving cache, the designation is accomplished by asserting MWB/WT#.

5.1.1.1.11. Read For Ownership

Read For Ownership is when an 82496 Cache Controller/82491 Cache SRAM allocation causes the cache line to go directly to [M] state. This occurs when a memory write miss cycle is frozen in the memory cycle buffer and an allocation cycle is issued.

In some systems it is preferable to eliminate main memory accesses whenever possible to circumvent slow memory. Here, the allocation is carried out from another cache using cache-to-cache transfer. This transfer avoids writing and reading main memory, and puts the allocated line into the [M] state using the DRCTM# input.

Data for the allocation can also come from main memory. This would be the case if the data was not found in another cache, and the MBC wanted to skip the [E] state by asserting DRCTM#.

Read for ownership uses MFRZ# for all write misses so that the write cycle does not access main memory. The MBC must complete this 'dummy' write cycle on the memory bus by providing the cycle progress signals (i.e., KWEND#, SWEND#, and CRDY#) to the 82496 Cache Controller. The subsequent allocation cycle is brought from memory, or from another cache. Since write data is not updated in main memory, the line must be marked in the modified state and all other caches must invalidate that line. If the line originates from another cache, that cache must invalidate its copy. In this way the other cache transfers ownership.

5.1.1.1.12. I/O Cycles

All I/O cycles are transferred to the memory bus and are of length 1 (only 1 MBRDY#/BRDY# are required). The MBC must supply BRDY# to the CPU once the I/O cycle is complete.

I/O cycles can be pipelined into and out of other I/O and memory bus cycles.

5.1.1.1.13. Special Cycles

Special cycles are treated exactly like I/O cycles. They are not posted, and the MBC must provide BRDY# to the CPU.

5.1.1.1.14. FLUSH and SYNC Cycles

To the MBC, cycles initiated by the FLUSH# and SYNC# signals resemble replacement write back cycles and should be handled as such. There is no need to prevent snooping or arbitration between these cycles.

82496 Cache Controller FLUSH# invalidates the entire 82496 Cache Controller and Pentium processor tag arrays. Two clocks are required to lookup a tag entry if the result is a miss. The 82496 Cache Controller also invalidates tags in the CPU cache by executing inquire and back-invalidation cycles to the Pentium processor. There are two reasons for potentially wanting to assert the CPU FLUSH# in addition to the 82496 Cache Controller FLUSH#. One, if the MBC wants to see the Pentium processor flush acknowledge special cycle, and two, to assure that no Pentium processor cache hits are occurring once FLUSH# has been asserted to the 82496 Cache Controller. This is because the 82496 Cache Controller flush operation does not inhibit Pentium processor cache hit operations. For optimum performance, issue FLUSH# to only the 82496 Cache Controller.

SYNC# will cause both the 82496 Cache Controller/82491 Cache SRAM and Pentium processor caches to write back all modified lines. The 82496 Cache Controller causes the CPU cache to write back all modified data by initiating inquire cycles to the Pentium processor when the 82496 Cache Controller/82491 Cache SRAM cache line state is modified.

When the MBC decodes a Pentium processor Flush (due to the INVD or WBINVD instructions) or Write Back (due to the WBINVD instruction) special cycle, it must provide FLUSH# to the 82496 Cache Controller. The 82496 Cache Controller/82491 Cache SRAM treats Flush and Write Back special cycles like I/O cycles. They are not posted, and the MBC must provide BRDY#. The WBINVD instruction causes the Pentium processor to issue the Flush special cycle followed by the Write Back special cycle.

To insure that the processor will not generate an additional bus cycle (code prefetch or page table read) following the INVD or WBINVD instructions, the MBC must delay BRDY# to the 82496 Cache Controller/82491 Cache SRAM for the Flush and Write Back special cycles until it recognizes CAHOLD asserted. Having the MBC Wait to complete the CPU special cycles until the flush operation has been internally recognized by the 82496 Cache Controller insures that no additional CPU or 82496 Cache Controller cycles are generated. The 82496 Cache Controller flush operation is complete when FSIOUT# becomes inactive. Note that the Pentium processor will not pipeline any cycle into a Flush or Write Back special cycle.

5.1.2. Snooping

System caches must snoop on most memory bus cycles for modified lines (data) to prevent stale data from being returned or updated to memory. Snooping also enables the cache bus master to implement the MESI protocol properly. If the master cache is performing a line fill, for example, and another cache has a copy of the unmodified line, then the line being filled should be placed in the Shared [S] state. If the master cache is performing a write cycle, that line, if present in any other cache, must be invalidated.

Snooping may be done in two ways. First, the MBC that is driving the cycle can cause all other caches to snoop. Second, each MBC can generate an independent cache snoop for its local cache as it detects memory cycle. In either case, the MBC must initiate a snoop request to the 82496 Cache Controller and transfer the 82496 Cache Controllers response to the system.

An MBC may initiate 82496 Cache Controller snoops using one of three snoop initiation modes: strobed, clocked, and synchronous. Refer to the Initialization and Configuration chapter for 82496 Cache Controller snoop mode configuration details. At the beginning of each snoop, the 82496 Cache Controller samples for the snoop address, SNPINV, SNPNCA, MBAOE#, MAOE#, and MAP.

If MAOE# is active, the 82496 Cache Controller is driving the bus, and cannot perform a snoop. In this scenario, all other caches in the system perform snoops.

MBAOE# indicates whether the 82496 Cache Controller needs to perform a snoop write-back starting at the provided sub-line address or at sub-line address 0. If MBAOE# is active during snoop initiation, the write-back begins with sub-line address 0.

MAP is driven by the MBC during snoop cycles and indicates the address parity of the 82496 Cache Controller line address bits. MAP must be driven to indicate even parity of the snoop address.

5.1.2.1. CHOOSING A SNOOPING MODE

The CPU-Cache Core supports synchronous, clocked (asynchronous), and strobed snoops. All snoops begin when the snoop strobe signal (SNPSTB#) is asserted and end when the 82496 Cache Controller responds, which is always synchronous to the CPU CLK.

5.1.2.1.1. Synchronous Snooping Mode

Figure 5-4 shows the synchronous snooping mode. Synchronous snoop mode provides the fastest snooping possible. The snoop address, address parity, and snoop parameters are sampled during the rising edge of the CLK in which SNPSTB# is sampled active. If nothing blocks the snoop, the 82496 Cache Controller can snoop on the next clock edge since there is no need to synchronize the snoop information.

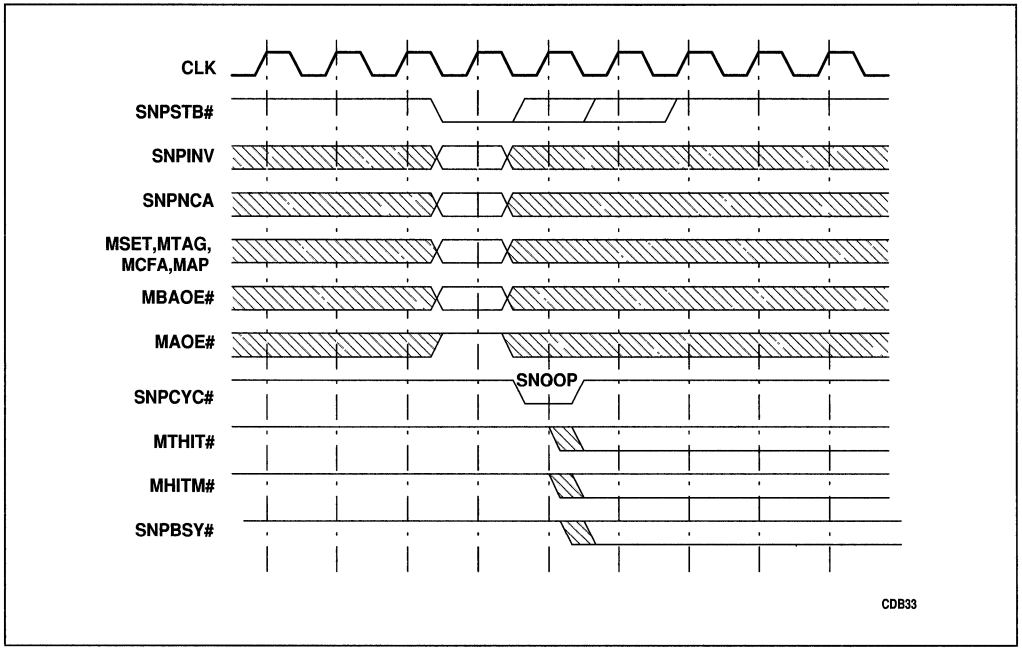


Figure 5-4. Synchronous Snoop Mode

5.1.2.1.2. Asynchronous Snooping Mode

Figure 5-5 shows the clocked asynchronous snooping mode. In clocked snooping mode, the snoop address, address parity, and snoop parameters are sampled with the rising edge of SNPCLK in which SNPSTB# is sampled active. (SNPCLK is an external clock supplied by the MBC.) The 82496 Cache Controller must synchronize the snoop initiation event with its internal CPU CLK, delaying snooping by two CPU CLK cycles.

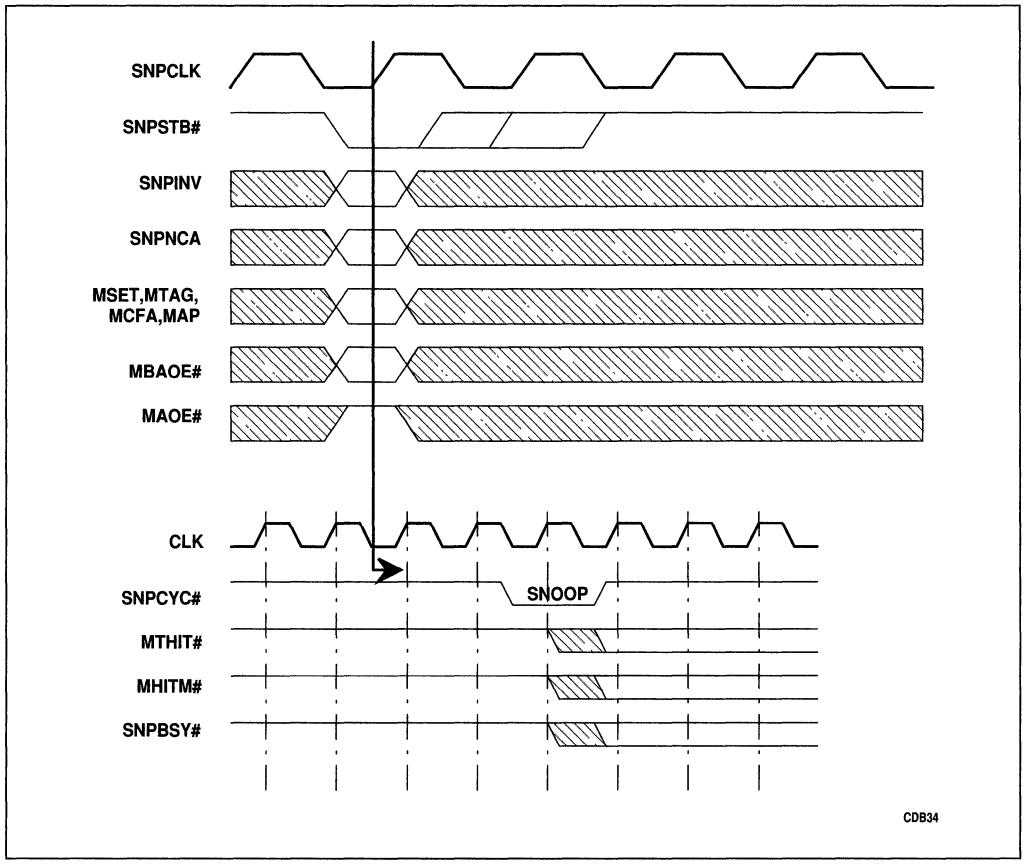


Figure 5-5. Clocked Snoop Mode

5.1.2.1.3. Strobed Snooping Mode

In strobed snooping mode (Figure 5-6), no clocks are needed to initiate the snoop. The snoop address, address parity, and snoop parameters are sampled with the falling edge of SNPSTB#, and the 82496 Cache Controller begins the snoop once it has synchronized this information internally. Synchronization requires an additional two CPU CLK cycles.

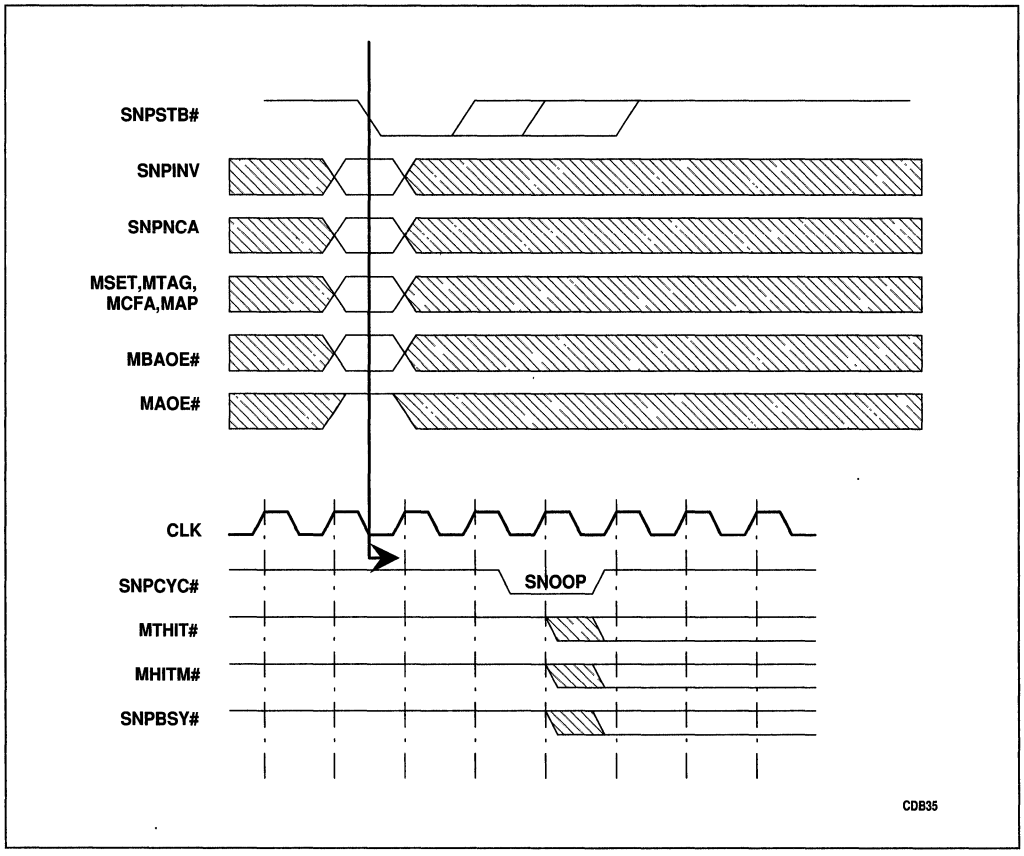


Figure 5-6. Strobed Snoop Mode

Snoop modes are selected using the SNPMD pin with respect to the falling edge of Reset. If SNPMD is strapped low, synchronous mode is selected. If SNPMD is HIGH, strobed mode is selected. If SNPMD is connected to an external clock, clocked mode is selected, and the external clock becomes the external snooping clock source.

5.1.2.2. SNOOP OPERATION

A snoop operation consists of two phases: 1) the initiation phase and 2) the response phase. See Figure 5-7. During the initiation phase, the MBC provides the 82496 Cache Controller with the snoop address information. During the response phase, the 82496 Cache Controller provides the snoop status information.

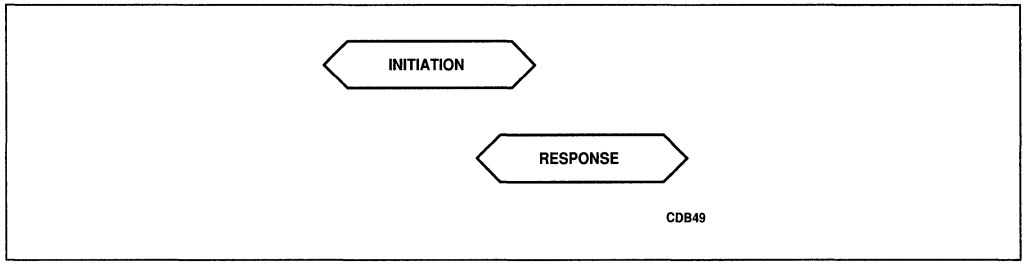


Figure 5-7. 82496 Cache Controller Snooping Operations

To initiate a snoop, the MBC asserts SNPSTB#, which latches snoop information into the 82496 Cache Controller. The 82496 Cache Controller synchronizes this information, if necessary, and generates the snoop cycle signal (SNPCYC#) to indicate that snooping is taking place. SNPCYC# may be delayed by synchronization and/or snoop blocking. SNPCYC# indicates to the MBC that it may read the 82496 Cache Controller's snoop responses on the next CLK.

If the 82496 Cache Controller/82491 Cache SRAM needs to write back a modified line or is already performing a back-invalidation, the Snoop Busy signal (SNPBSY#) is asserted. SNPBSY# indicates that the 82496 Cache Controller can accept another snoop request (once SNPCYC# is asserted), but will not service that snoop until after SNPBSY# goes inactive.

Once SNPCYC# is asserted, the 82496 Cache Controller's snoop latch can accept another snoop request. As a result, snoops may be pipelined. Figures 5-8 and 5-9 show the fastest synchronous and asynchronous snooping possible. Note that the MBC must not assert SNPSTB# for a new snoop operation until it has sampled SNPCYC# active for the first snoop operation (refer to section 5.1.2.4). Note that, during asynchronous snooping, the SNPSTB# for the following snoop can only occur *after* the falling edge of the SNPCYC# of the previous snoop.

The 82496 Cache Controller responds after a snoop look up by driving the MHITM# and MTHIT# signals after the clock in which SNPCYC# is asserted. MHITM# is asserted for snoop hits to an [M] state line. MTHIT# is asserted for snoop hits to [M],[E], and [S] state lines. These signals indicate the state of the 82496 Cache Controller line just prior to the snoop operation.

The MBC can predict the final state of the 82496 Cache Controller line by knowing the initial state and the values of the SNPINV and SNPNCA signals during the snoop operation. Figures 5-10 and 5-11 show the 82496 Cache Controller response to snoops without and with invalidation, respectively.

MHITM#, MTHIT#, SNPCYC#, and SNPBSY# are all synchronous to CLK.

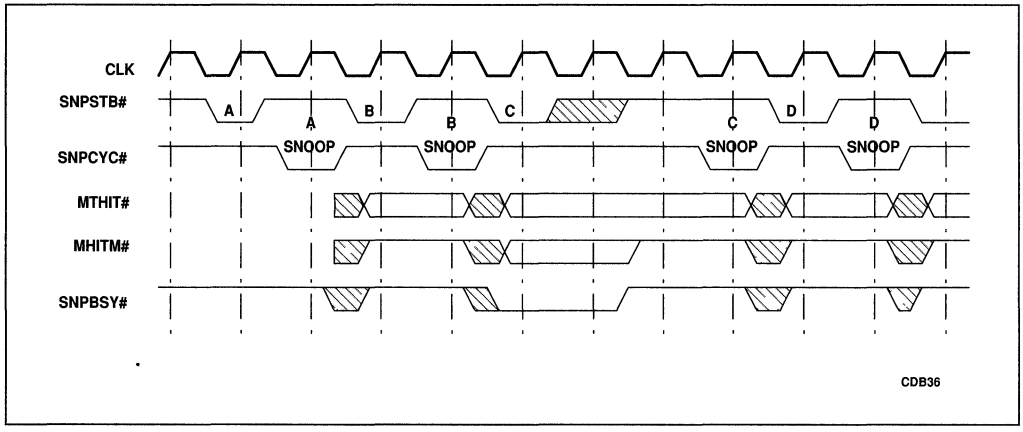


Figure 5-8. Fastest Synchronous Snooping

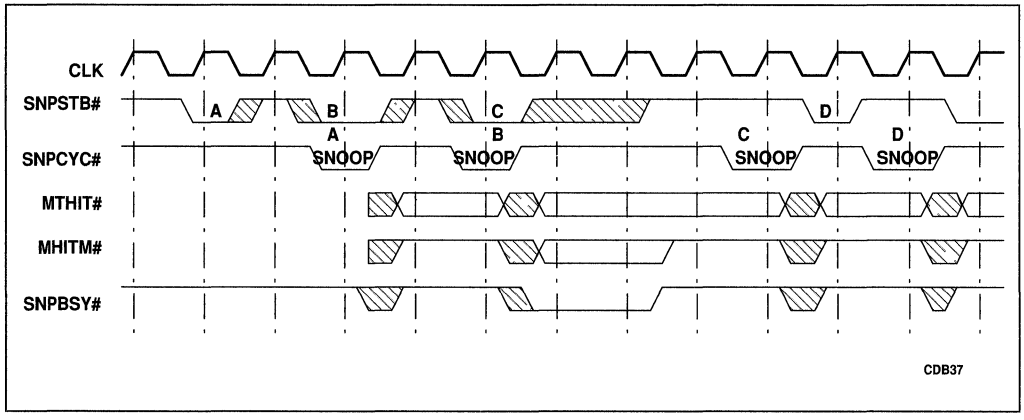


Figure 5-9. Fastest Asynchronous Snooping

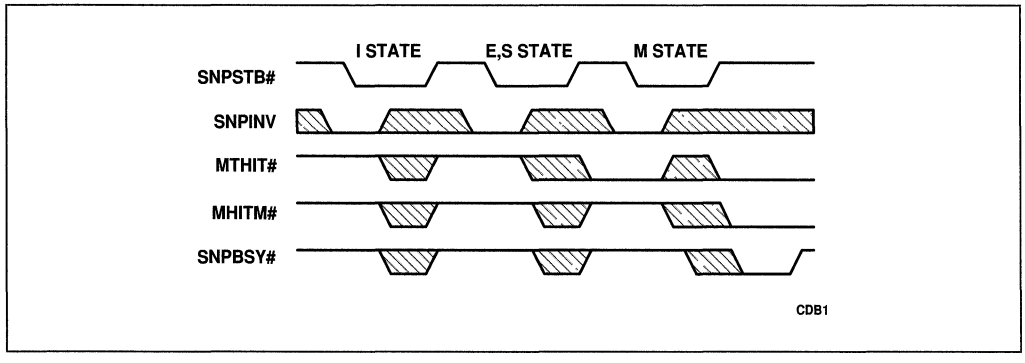


Figure 5-10. Snoops without Invalidation

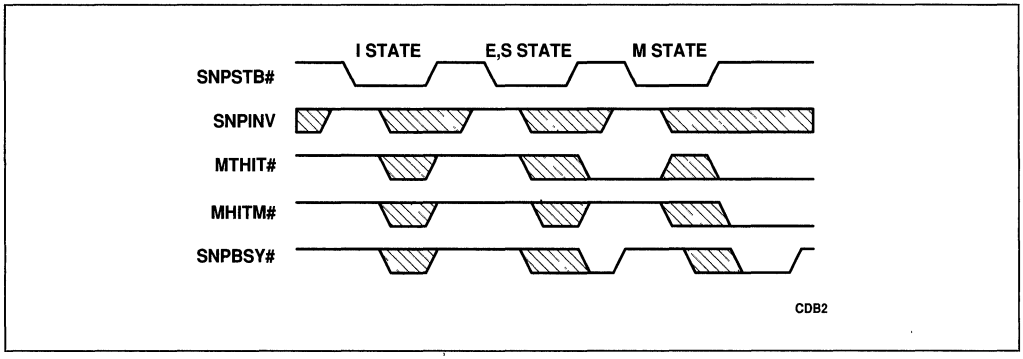


Figure 5-11. Snoops with Invalidation

5.1.2.3. SNOOP BLOCKING

When the MBC asserts SNPSTB#, the 82496 Cache Controller synchronizes the information as necessary, and snoops if the tagRAM is not blocked. Snoop cycles take priority in 82496 Cache Controller/82491 Cache SRAM, so if a snoop request is concurrent with a read request from the CPU, the snoop request is serviced first. However, snoops may be blocked if the 82496 Cache Controller is in the middle of a cycle or servicing another snoop.

If the 82496 Cache Controller is in the middle of executing a cycle, the outcome of a snoop request varies depending on when SNPSTB# is asserted.

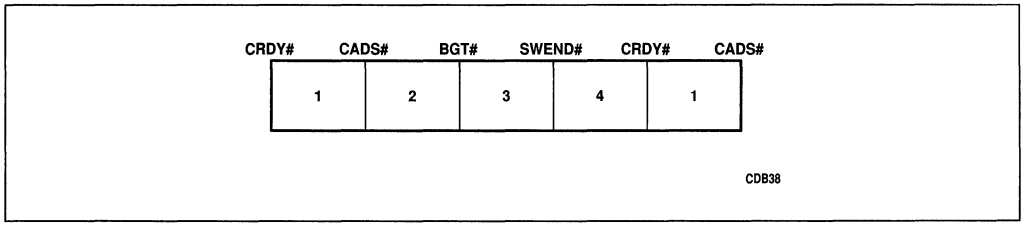


Figure 5-12. Snoop Response During Cycles

Figure 5-12 shows the regions into which a snoop cycle can be partitioned.

Region 1 is after one memory cycle ends (after CRDY#) and before a new cycle begins (before CADS#). A snoop occurring in this region is looked up and serviced immediately.

Region 2 is after a memory cycle has started (CADS#) but before the cycle has been guaranteed to complete (the MBC asserts BGT#). A snoop in this region is looked up and serviced immediately. If a memory cycle was aborted because the snoop hit a modified line, in some cases CADS# is re-issued after the snoop write-back completes.

Region 3 is after the memory cycle has been guaranteed to complete and before the snoop window (SWEND#) has completed. A snoop request occurring in this region is blocked until SWEND# is asserted. After SWEND# is asserted, the look-up will occur 2 CLKs later, the snoop response will be given 1 CLK later, but the write-back (if necessary) will not be initiated until after CRDY#.

Region 4 is after SWEND# is asserted and before CRDY# is asserted. A snoop in this region is looked up immediately but the snoop write-back, if necessary, is delayed until CRDY# is asserted. Here, a snoop write-back is treated as if it had occurred after CRDY# (i.e. snoop hits to modified cache data schedule a write-back that will be executed in the next memory bus cycle). Note that MTHIT# and MHITM# will be available 1 CLK after the look-up (which is 2 CLKs after SWEND#).

The 82496 Cache Controller uses two interlock mechanisms to ensure that snoops are aligned within the proper region. The first interlock ensures that once BGT# is asserted, snoops are blocked until after SWEND#. The second interlock ensures that once a snoop is initiated, BGT# cannot be asserted until after the snoop has been serviced.

Figure 5-13 shows that when the 82496 Cache Controller recognizes the BGT# signal, it blocks all snoops until after SWEND#. If SNPCYC# has not been issued before BGT# is asserted, the snoop is blocked.

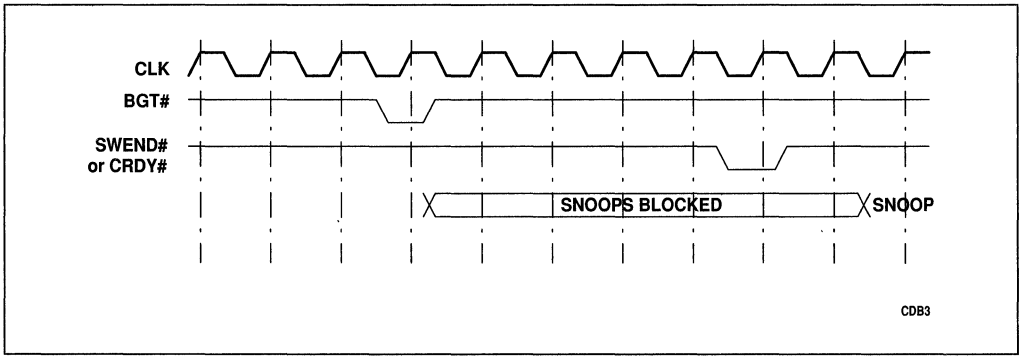


Figure 5-13. Snoop Response Blocking Using BGT#

Figure 5-14 shows a snoop occurring before BGT# is asserted. Once the 82496 Cache Controller acknowledges a snoop, the 82496 Cache Controller may, depending on the result of the snoop, ignore BGT# while the snoop is being serviced. The 82496 Cache Controller always ignores BGT# when SNPCYC# is active. If the snoop results in a hit to a modified cache line (MHITM# active), the 82496 Cache Controller ignores BGT# as long as both SNPBSY# and MHITM# remain active. If the snoop result is not a hit to a modified cache line (MHITM# inactive), the 82496 Cache Controller may accept BGT# even while SNPBSY# is active. This contingency allows the memory bus controller to proceed with a memory bus cycle by asserting BGT# while the 82496 Cache Controller is performing inquires or back-invalidations.

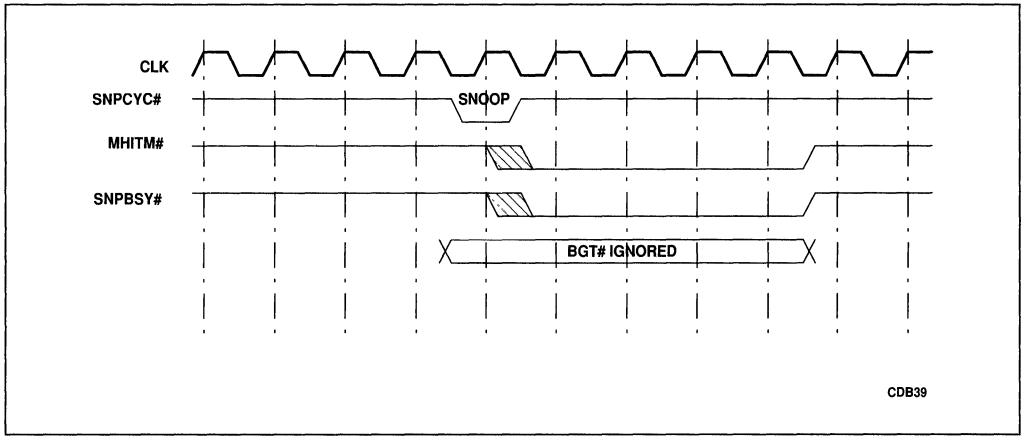


Figure 5-14. Snoop Executing before BGT# Is Asserted

The two interlock mechanisms described above provide a flexible method of ensuring overlapped snoop handling.

NOTE

Even when snoops are delayed, address latching is performed through activation of SNPSTB#. Note that the MBC must not assert SNPSTB# for a new snoop operation until it has sampled SNPCYC# active for the first snoop operation (refer to section 5.1.2.4).

5.1.2.4. WHEN SNOOPING IS NOT ALLOWED

The previous section described the conditions under which snoops would be blocked by the 82496 Cache Controller. There are some cases in which snoops are not blocked by the 82496 Cache Controller, and yet the MBC must not allow snoops to occur. This section describes these cases.

The 82496 Cache Controller allows the memory bus controller to pipeline snoop operations. A second snoop request and snoop address can be supplied to the 82496 Cache Controller prior to the completion of the current snoop operation. Once SNPSTB# has been sampled active, a new SNPSTB# (for a pipelined snoop) will be ignored by the 82496 Cache Controller until it has issued SNPCYC# for the original snoop operation. Figure 5-15 shows the window in which the MBC must not assert an additional SNPSTB# to the 82496 Cache Controller. After SNPCYC# has been asserted, a new snoop address will be latched by the 82496 Cache Controller (with SNPSTB#).

NOTE

For each snoop mode, the MBC must not request a second snoop operation between SNPSTB# and SNPCYC#. For strobed snoop mode, the second falling edge of SNPSTB# must not be until after the falling edge of SNPCYC#. For clocked snoop mode, the second SNPSTB# sampled by

SNPCLK must not be until after the falling edge of SNPCYC#. For synchronous snoop mode, the second SNPSTB# sampled by CLK must not be until the CLK following SNPCYC# active.

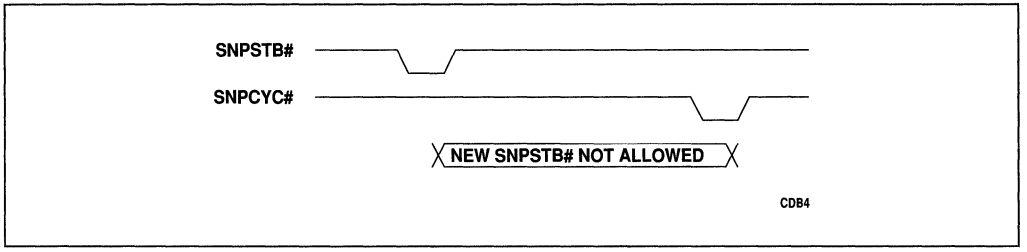


Figure 5-15. New SNPSTB# Not Allowed

Locked cycles are used to guarantee an atomic Read-Modify-Write operation. The MBC must not allow snoops between the BGT# of the first Read portion of the locked sequence, and the BGT# of the last Write portion. This is to ensure that the lock protocol is not violated. Section 5.1.2.5 describes the restriction which, if strictly met, will allow the system to snoop during this portion of the locked sequence.

During read-for-ownership cycles, the MBC must not allow snoops between the BGT# of the write-through and the BGT# of the allocation. This is to ensure that the snoop data is not stale. Between the BGT# of the write-through and the BGT# of the allocation, the line is invalid in the cache doing read-for-ownership (cache 1). Cache 2 (the cache *from which* data is being transferred) has only a *partially* updated line. When the write-back is completed, the 64-bits of recently modified data in cache 1 is surrounded by the modified data from cache 2. The *resulting* line is the most recently modified line. Note that the line in cache 2 is invalidated before the cache-to-cache transfer. Also, once the transfer is complete, the line exists in cache 1 in the modified state.

5.1.2.5. SNOOPING DURING LOCKED CYCLES

Locked cycles are used to guarantee atomic Read-Modify-Write operation. The system assumes that a data item will not be accessed by another device until the read and write have been completed. There is a situation using the 82496 Cache Controller/82491 Cache SRAM where this lock protocol may be violated unless certain restrictions are met.

A snoop write-back cycle takes priority over all other cycles in the 82496 Cache Controller cache controller. If the CPU is performing a Read-Modify-Write (i.e., locked) cycle and the data is Modified in the 82496 Cache Controller/82491 Cache SRAM, the data could be written back on a snoop between the Read and Write parts of the intended atomic cycle. This violates the lock protocol and could cause unintended system operation.

To provide maximum performance in Pentium processor CPU-Cache Chip Set systems, the 82496 Cache Controller allows snooping during locked cycles, however, the following condition must be met: the address being snooped must not be in the same cache line as that of the locked operation.

WARNING

Proper system operation cannot be guaranteed if this restriction is not met!

In order to insure that the above condition is met, system designers must compare the snoop address to the locked address. If those addresses are in the same cache line, the snoop must be blocked by the MBC. If the snoop and locked addresses are not in the same cache line, the MBC can allow the snoop to complete.

5.1.2.5.1. Snooping During Split Locked Cycles

If CSCYC is high with CADS#, the cycle is split. Split cycles have adjacent virtual addresses, but the physical addresses seen on the address bus are not necessarily adjacent. It is possible that the physical addresses might be split across a page boundary. Obviously, split locked cycles add another level of complexity to determining if the locked and snoop addresses are in the same cache line.

The system designer can ensure that all locked data is aligned within a single cache line (in this case CSCYC=0 and there will never be split cycles!). If system software is not under the complete control of the system designer, this may not be an option.

Before allowing snoops to occur during split locked cycles, system hardware designers must be able to determine both of the physical addresses which the locked sequence will read and write. If both addresses are known, snoops may be allowed to any other address. Snoops are not allowed to the second address of a split locked sequence during accesses to the first address and vice versa. BOTH addresses must be barred from snoops during the entire sequence!

5.1.2.6. SNOOP WRITE BACK CYCLES

Snoop write back cycles are generated by the 82496 Cache Controller in response to a snoop from the MBC which hits a modified line in the 82496 Cache Controller/82491 Cache SRAM (and possibly also in the Pentium processor data cache). Snoop write back cycles are requested by the 82496 Cache Controller by activation of SNPADS# instead of CADS#. For these cycles, the 82496 Cache Controller only samples the CRDY# MBC response. The 82496 Cache Controller assumes that the memory bus controller owns the bus to perform the intervening write back and that no other agents will snoop this cycle. This is called "Restricted Back-Off Protocol" because a snoop write back cycle cannot be aborted by the CPU or the MBC. Also, the 82496 Cache Controller will ignore CNA# during snoop write backs (no subsequent cycle can be pipelined into a snoop write back cycle). Figure 5-16 shows the 82496 Cache Controller cycle progress signals required to request and complete a snoop write back cycle.

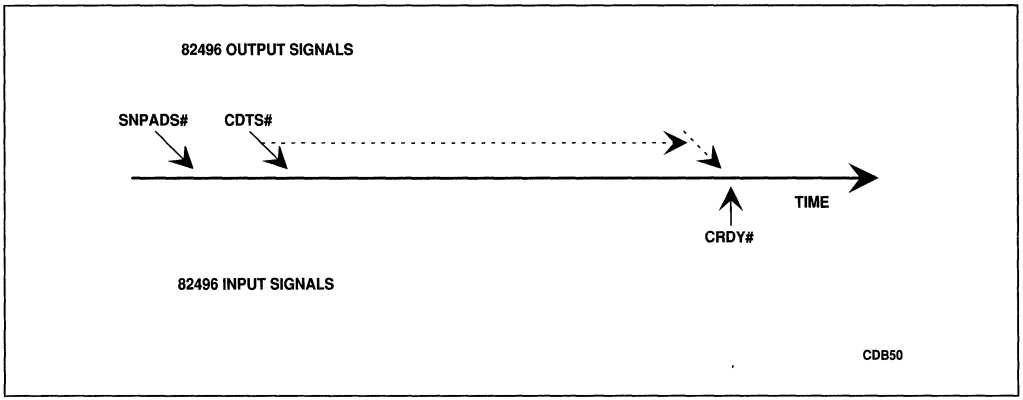


Figure 5-16. Cycle Progress for Snoop Write Back Cycles

5.1.3. Address Integrity

Five pins are available on the 82496 Cache Controller cache controller to support address integrity: two for address parity (AP, MAP), two for address parity errors (APERR#, MAPERR#), and one for the internal address and tagRAM parity errors (IPERR#). Refer to section 5.2 for the detailed pin descriptions of these signals.

This feature allows systems based on Pentium processor CPU-Cache Chip Set to be used in high-reliability applications.

5.1.3.1. CPU BUS ADDRESS PARITY

During every snoop cycle to the Pentium processor, the 82496 Cache Controller calculates even parity for the line address (the specific 82496 Cache Controller address pins are configuration dependent and correspond to CPU address pins A[31:5]) and drives that value on the AP pin. Refer to the *Pentium™ Processor Data Book* for more details. Note that the 82496 Cache Controller does not internally store the address parity bit (it re-generates that bit during each CPU snoop operation).

For Pentium processor initiated cycles, the 82496 Cache Controller samples the address (along with a valid AP bit) and internally calculates the line address parity. If it detects an address parity error, the 82496 Cache Controller drives the APERR# signal low (refer to the APERR# detailed pin description for details) to flag the error to the memory bus controller.

Note that when the Pentium processor is used with the 82496 Cache Controller/82491 Cache SRAM CPU bus address parity is automatically supported. The error indication given by either the CPU (APCHK#) or the 82496 Cache Controller cache controller (APERR#) may be ignored by the MBC if address parity is not supported.

5.1.3.2. MEMORY BUS ADDRESS PARITY

The 82496 Cache Controller cache controller generates and drives the memory address parity

bit (MAP) valid for each cycle it initiates on the memory bus. The MBC can ignore this signal if address parity is not supported.

During 82496 Cache Controller/82491 Cache SRAM snoop cycles, MAP may be driven by the MBC to indicate the line address parity for the snooped address (the specific 82496 Cache Controller address pins are configuration dependent - refer to Table 4-3). If the 82496 Cache Controller detects a memory address parity error (based on the memory bus line address and the MAP bit driven by the MBC), it drives the MAPERR# signal low (refer to the MAPERR# detailed pin description for details) to flag the error to the memory bus controller. Again, the MBC can ignore this error indication if memory bus address parity is not supported.

MAPERR# for any particular snoop operation is valid either from two CLKs after SNPSTB# (synchronous snoop mode) or one CLK after SNPCYC# (clocked and strobed snoop modes) until that same time during the subsequent snoop operation. MAPERR# is driven with the timings shown in Figure 5-17 for synchronous snooping mode and Figure 5-18 for the asynchronous snooping modes (clocked and strobed).

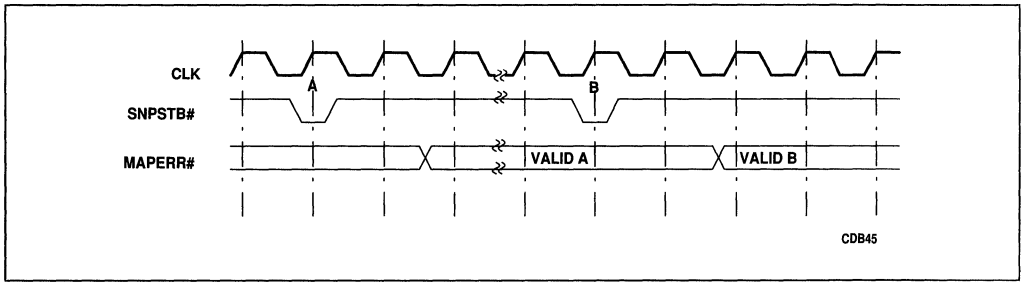


Figure 5-17. MAPERR# Timing for Synchronous Snoop Mode

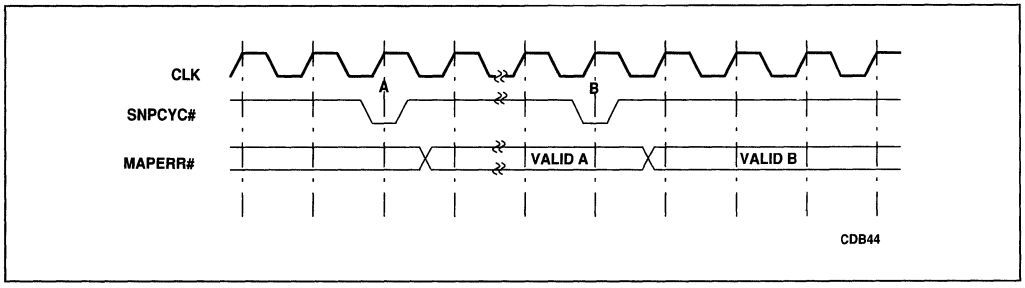


Figure 5-18. MAPERR# Timing for Asynchronous Snoop Modes

5.1.4. Data Control

All data control is handled by the MBC, including handshaking data into and out of the 82496 Cache Controller/82491 Cache SRAM and CPU, freezing data for allocations, pipelining data on the memory bus and retrying data as necessary.

The 82491 Cache SRAM data path is separate from the address path. These paths do not have to operate at the same clock frequency, and it is possible, for example, for the 82491 Cache

SRAM to read data for a line fill even before the cycle has been guaranteed to complete on the memory bus via BGT#.

The Address bus runs at the same clock frequency as the CPU bus (CLK). The memory data bus runs at a speed equal to or less than CLK (MCLK).

Data transfer into and out of the 82491 Cache SRAMs take place in clocked mode or in strobed mode. The data transfer mode may be selected independently of the snoop mode.

5.1.4.1. CPU DATA BUS TRANSFER CONTROL

The Pentium processor latches or drives data upon active sampling of the BRDY# input from the MBC or the BRDYC# input from the 82496 Cache Controller. It is very important to data transfer timings that all of the processor chip set components receive equivalent data control signals. Therefore, it is a requirement that the MBC provide the Pentium processor, 82496 Cache Controller cache controller, and all 82491 Cache SRAMs with the same BRDY# input. The 82496 Cache Controller also provides the Pentium processor and 82491 Cache SRAM functionally equivalent BRDYC# signals. See Figure 5-19 for clarification on BRDY# / BRDYC# / BRDYC1# / BRDYC2# interconnection between the processor chip set components.

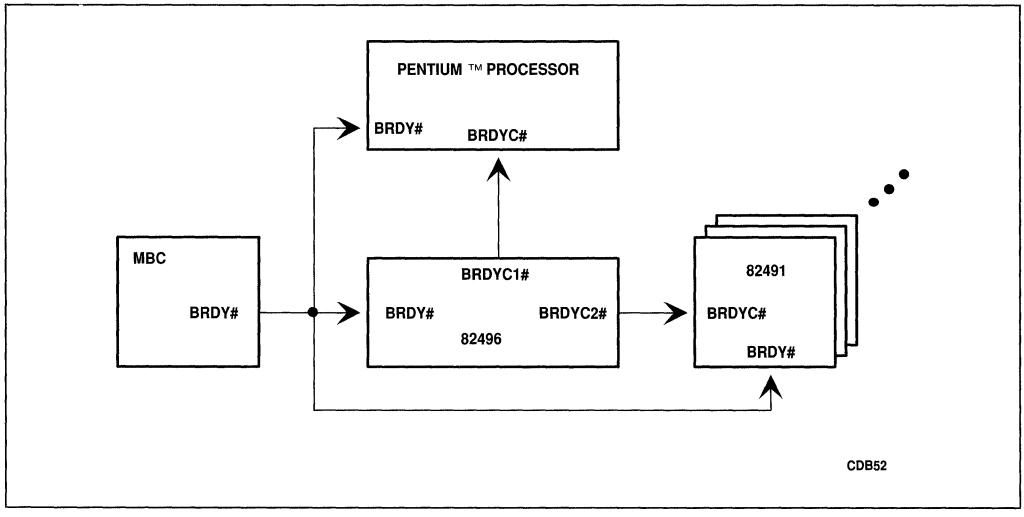


Figure 5-19. BRDY# / BRDYC# / BRDYC1# / BRDYC2# Interconnection

5.1.5. Memory Bus Mode Selection

Clocked memory bus mode and Strobed memory bus mode determine how the MBC transfers data into and out of the 82491 Cache SRAM.

In clocked mode, data is driven with reference to the Memory Clock (MCLK) input. MCLK is supplied by the MBC and can be of any frequency (within specs). To avoid the need for synchronization, MCLK may be such that the CPU clock frequency is a multiple of MCLK

frequency. MCLK may also be completely asynchronous, however, to take advantage of a given memory system or provide easy upgrades to higher clock frequencies.

In clocked mode, MBRDY# clocks data into and out of the 82491 Cache SRAM memory buffers. MBRDY# is sampled on every rising edge of MCLK. When transfers complete, MEOC# ends the current memory cycle and switches to the next buffer. Likewise, MEOC# is sampled on every rising edge of MCLK. Other signals sampled with MCLK are MZBT#, MSEL# and MFRZ#.

Data can also be driven with reference to the Memory Output Clock (MOCLK) input in clocked memory bus mode. MOCLK is a latch enable for the 82491 Cache SRAM data outputs which permits the output data to be skewed relative to MCLK. This allows the MDATA hold time and output valid delay to skew with MOCLK, offering additional flexibility to memory designs.

In strobed mode, all data input and output signals are driven from or referenced to MBC strobing signals (i.e., MSEL#, MEOC#, MISTB, MOSTB). For example, data is driven out of 82491 Cache SRAM with a rising or falling transition of MOSTB. In this way, strobed mode allows the 82491 Cache SRAM data bus to be used without clocks.

In strobed mode, data is driven from the 82491 Cache SRAM with MOSTB transitions. Data is read into the 82491 Cache SRAM with MISTB transitions. The falling edge of MEOC# ends a memory cycle. Other memory signals sampled in strobed mode are MZBT#, MSEL# and MFRZ# (see the detailed pin descriptions for how these signals are sampled). Strobed mode signals have set-up and hold times to asynchronous control signal transitions.

To place the 82491 Cache SRAM in strobed memory bus mode, the MCLK pin (MSTBM) is pulled high or low. If a clock is detected at this input, the 82491 Cache SRAM is placed in clocked mode. The detected clock becomes the MCLK reference.

5.1.6. 82491 Cache SRAM Intelligent Dual-Ported Cache Memory

5.1.6.1. 82491 CACHE SRAM DATA PATH

82491 Cache SRAM cache data control is similar for clocked and strobed mode buses, using the same signals but different references. The following discussion assumes clocked mode.

The section discusses the 82491 Cache SRAM data path in general terms and will be followed with a discussion of handling specific cycles later.

The 82491 Cache SRAM has four memory buffers: two memory cycle buffers, one write-back buffer, and one snoop buffer. Each buffer is capable of holding an entire cache line of the longest configurable length.

The 82491 Cache SRAM's memory cycle buffers are used to post writes, hold data during line-fills, and transfer data on reads and I/O writes. The write-back buffer holds the replaced (modified) line ready to be written back to memory (or 2 lines if 2 lines/sector are used). The write-back buffer can be snooped in the event of a snoop hit. The snoop write-back buffer holds modified data that has been hit by a snoop. Since snoop hits are the highest priority cycles, this buffer will be emptied before any other cycle.

The four 82491 Cache SRAM memory buffers are MUXed to the memory bus. The MUX

determines which buffer and, more specifically, which buffer slice is on the bus. When MBRDY# and MSEL# are asserted, a memory burst counter is incremented, allowing the MUX to select the next buffer slice.

The memory burst counter follows the CPU burst order according to the sub-line address of the initial slice. When MZBT# is sampled active by the 82496 Cache Controller, the CPU initiated burst order is ignored and the memory bus read or write begins with burst address 0. When the MBC finishes with one buffer, MEOC# is asserted to switch the MUX to the next buffer in line. MEOC# also resets the counter and latches the last data slice (if used instead of the last MBRDY# or MISTB/MOSTB).

On the CPU side, the 82491 Cache SRAM contains two CPU buffers and a MUX to each. A CPU buffer captures data from the appropriate memory buffer or array and transfers it to the CPU. The MUX selects the data slice to be MUXed to the CPU bus. The counter associated with the selected MUX is incremented by BRDY#.

The 82491 Cache SRAM array contains a MUX that selects the WAY that data will be read during hit cycles, based on the MRU algorithm. This MUX is used during write cycles to write data according to the proper WAY.

5.1.6.2. MEMORY CYCLE BUFFERS

The 82491 Cache SRAM contains two memory cycle buffers which are used for memory reads, allocations and memory writes. The buffers have a maximum configured width of 128 bytes (distributed over the 16 data 82491 Cache SRAMs). The 82491 Cache SRAM uses the buffers in an alternating fashion, using the buffer available when the other has a posted write or is being used for a memory read.

During allocation cycles, read for ownership may be implemented using the MFRZ# signal. If MFRZ# is sampled active during a write cycle with PALLC# active, the memory cycle buffer freezes write data so that the subsequent line fill loads data to occupy the surrounding locations. In this way, the write cycle need not be written to memory. The MBC must complete this "dummy" write cycle to the 82496 Cache Controller (i.e., provide BGT#, KWEND# and CRDY#). Following the line fill, the line must be tagged as Modified.

5.1.6.3. WRITE-BACK AND SNOOP BUFFERS

The write back and snoop buffers are 128 bytes wide to accommodate the maximum 82491 Cache SRAM line length. The write back buffer is used when replaced data must be written back to main memory (including FLUSH and SYNC cycles) while the snoop buffer is used when data must be written out on a snoop hit to a modified line.

Before a line fill completes, the 82496 Cache Controller determines whether it must remove a modified line to free space for a line fill. If necessary, the modified line is placed in the write-back buffer and the line fill is filled via a memory cycle buffer. If the line fill is non-cacheable, the contents of the memory cycle buffer and the replacement write-back buffer are discarded, and the 82491 Cache SRAM array value is as it was before the line fill.

Line-fill, replacement write-back, FLUSH, and SYNC cycles are not atomic. If a snoop request is initiated between cycles, the write-back buffer can be snooped, and data can be written directly out as needed.

5.1.6.4. MEMORY BUS CONTROL SIGNALS

The main memory bus control signals, used to control the 82491 Cache SRAM's data path, buffers and MUXes, are BRDY#, MSEL#, MEOC#, MBRDY# and CRDY#.

MSEL# enables the 82491 Cache SRAM memory interface and qualifies the MBRDY# signal. If MSEL# is inactive, MBRDY# is not recognized. MSEL# is also used to reset the memory burst counter. If MSEL# becomes inactive, the counter is initialized to its starting value. MSEL# may remain active for many cycles or for all cycles, but it must be inactive for some time after RESET (1 CLK is sufficient) to initialize the memory burst counter the first time.

The MBC asserts MEOC# to finish with the current buffer and switch the memory bus to the next buffer to be used. MEOC# latches the last data segment (if not all MBRDY#s were given) and loads the memory burst counter with the next address before switching to the new buffer.

MBRDY# is used to increment the memory burst counter to select the next data slice. MBRDY# strobes data out of the 82491 Cache SRAM during write cycles and loads data into the 82491 Cache SRAM during read cycles. MBRDY# is ignored by the 82491 Cache SRAM when MSEL# is inactive

CRDY# completes the current cycle. When CRDY# is asserted, the 82491 Cache SRAM discards the buffer contents used in the current cycle and, on line-fills and allocations, loads the data into the 82491 Cache SRAM (cache SRAM) array. CRDY# must be asserted with or sometime after MEOC# has been asserted for a particular cycle. CRDY# is synchronous to the CPU clock but not to the memory clock. MEOC# is provided to allow the cycle to end on the memory bus and to allow a new cycle to begin before it is synchronized as the CRDY# input.

An example of the 82491 Cache SRAM read data path is shown in Figure 5-20. The path between the CPU and the memory bus is "flow-through" rather than clocked. Each line of data in the CPU bus buffer is available at the memory buffer after some propagation delay. Likewise, each line of data in the memory buffer is available in the CPU buffer. Data is burst into and out of the memory buffer using MBRDY# or MISTB/MOSTB. Data is burst into and out of the CPU buffer using BRDY#. In this way, there is no need for synchronization between the memory and CPU data paths.

During a CPU line fill, data may be returned to the CPU in two ways. First, when the memory buffer fills a 64-bit slice (with one MBRDY#), BRDY# may be asserted during the following clock to burst the line back to the CPU. Second, the memory buffer may be filled completely first (with four or eight MBRDY#s), and then BRDY# asserted on four consecutive clocks to burst data back to the CPU.

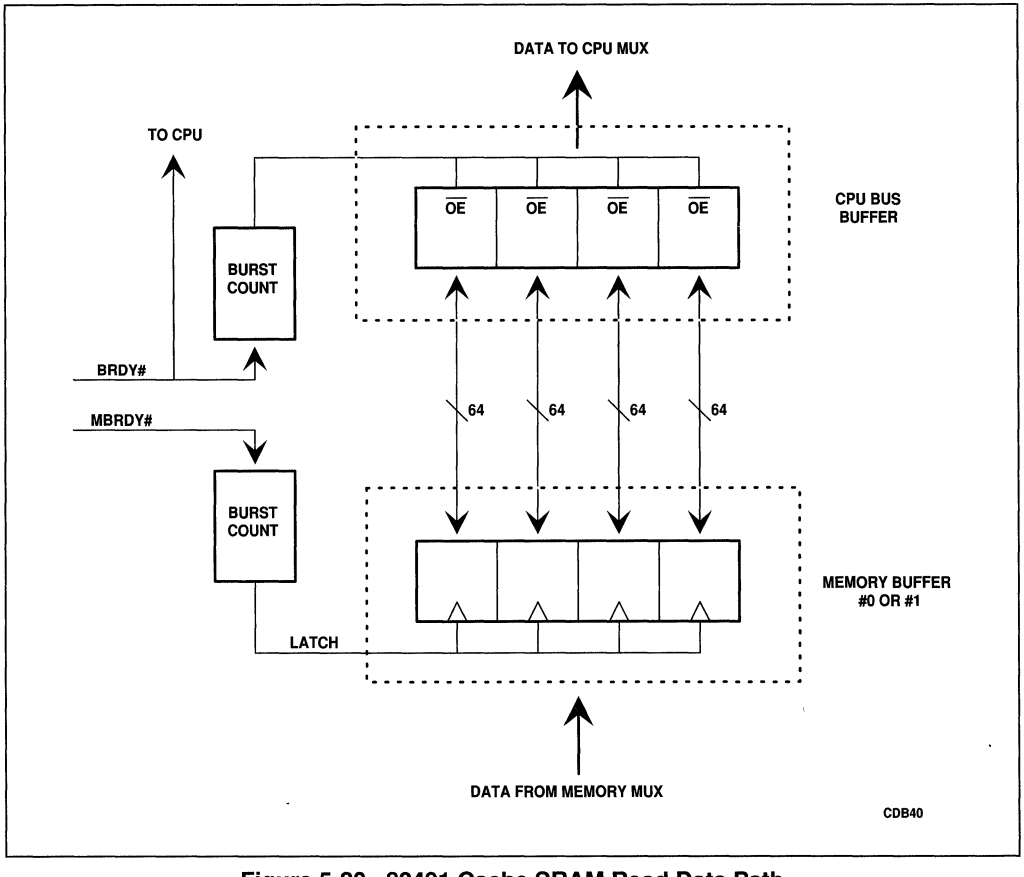


Figure 5-20. 82491 Cache SRAM Read Data Path

5.1.6.5. 82491 CACHE SRAM PARITY DEVICES

A 82491 Cache SRAM may be designated as a parity device. This is done be strapping the MBE#[PAR#] pin low during RESET. Two 82491 Cache SRAM SRAMs are used to provide the memory bus controller full data parity support.

In data parity configuration, the 82491 Cache SRAM CPU bus pins CDATA[3:0] are connected to the Pentium processor Data Parity pins (DP[7:0]) and CDATA[7:4] are connected to the Pentium processor Byte Enable outputs (BE[7:0]). Refer to Figure 5-21.

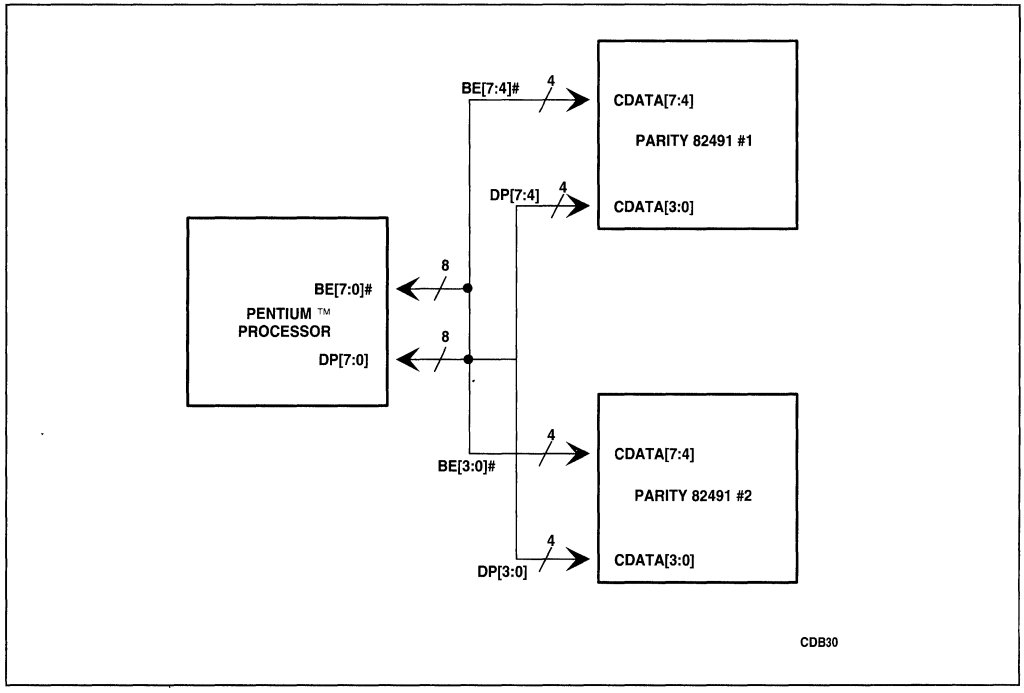


Figure 5-21. Pentium™ Processor/82491 Cache SRAM Data Parity Connections

5.1.7. Signal Synchronization

The MBC must also provide proper synchronization as needed. The Pentium processor CPU-Cache Chip Set runs at 66 MHz, along with most of its address and control-related signals, including CADS#, CDTS#, KWEND#, SWEND#, and CRDY#. Because the 82496 Cache Controller/82491 Cache SRAM allows the memory system to operate at lower frequency, the designer may choose to design an asynchronous memory bus running below 66 MHz. Such a scheme will require synchronization.

Some system designers will choose a divided synchronous memory bus, wherein the memory system runs at 33 MHz and synchronization is unnecessary.

The following is an example of a synchronization path used in generating KWEND#.

KWEND# is generated to provide the 82496 Cache Controller with the MKEN# and MRO# parameters. When the 82496 Cache Controller generates the cycle address, the memory system decodes the address and generates MKEN# and MRO#, based on cacheability and read-only address maps. These signals are asserted to the 82496 Cache Controller along with MKWEND#. MKWEND# tells the MBC that MKEN# and MRO# are valid and that KWEND# must be generated. Since the MKWEND# is synchronous with the memory bus, it must be synchronized to become KWEND#. KWEND# then causes the 82496 Cache Controller to sample MKEN# and MRO#.

5.1.8. Warm Reset

Warm reset enables the CPU portion of the Pentium processor CPU-Cache Chip Set cache core to be reset without resetting the primary or secondary caches (or the Pentium processor floating point unit).

To initialize the Pentium processor without affecting the first level caches, the MBC can assert INIT to the CPU as per the *Pentium™ Processor Data Book*.

NOTE

Refer to the *Pentium™ Processor Data Book* for details on INIT. The 82496 Cache Controller/82491 Cache SRAM cache may be active while the Pentium processor cache is being initialized. This is permitted because the Pentium processor allows back-invalidations during initialization.

5.1.9. Handling of Large Caches / Larger Line Sizes

A 512K cache can be configured with either 64 byte or 128 byte line size. For a 128-bit bus configuration, the 64 byte line size requires 4 bus transactions per cache line, whereas the 128 byte line size requires 8 transactions per cache line. In a 512K cache configuration, each BE[7:0]# output of the Pentium processor connects to the BE# input of two 82491 Cache SRAM devices.

A 512K cache can be connected to a 64-bit memory bus using the existing configuration options, as well as some external logic and control. For a clocked memory bus implementation, a description of a 512K cache connection to a 64-bit memory bus follows. The 82491 Cache MDOE# input is divided into two signals: MDOEL# and MDOEH#. Similarly, the 82491 Cache SRAM MBRDY# input is divided into MBRDYL# and MBRDYH#. The 16 82491 Cache SRAM devices are split into a "low" bank, which outputs/inputs the low 64-bits of data onto/off of the memory bus, and a "high" bank, which outputs/inputs the high 64-bits of data onto/off of the memory bus. The MDOEL# and MBRDYL# signals are connected from the MBC to the low bank; the MDOEH# and MBRDYH# signals are connected from the MBC to the high bank. The MBC is responsible for asserting MDOEL#, MDOEH#, MBRDYL#, and MBRDYH# such that no bus conflict occurs. The MDOEL# and MDOEH# signals retain the same functionality and timing requirements as the MDOE# signal; however, the MDOEL# signal, for example, only acts as the output enable for the low bank of 82491 Cache SRAM devices. Similarly, the MBRDYL# and MBRDYH# signals retain the same functionality as the MBRDY# signal. Refer to Figure 5-22 for a depiction of the 512K cache to 64-bit memory bus connection.

During linefills to both the 82496 Cache Controller/82491 Cache SRAM and the Pentium processor, the processor reads one half of a CPU cache line for each assertion of MBRDY#. The MBC may start to assert BRDY# (for CPU data transfer) after it asserts the second MBRDY# of memory bus transfer.

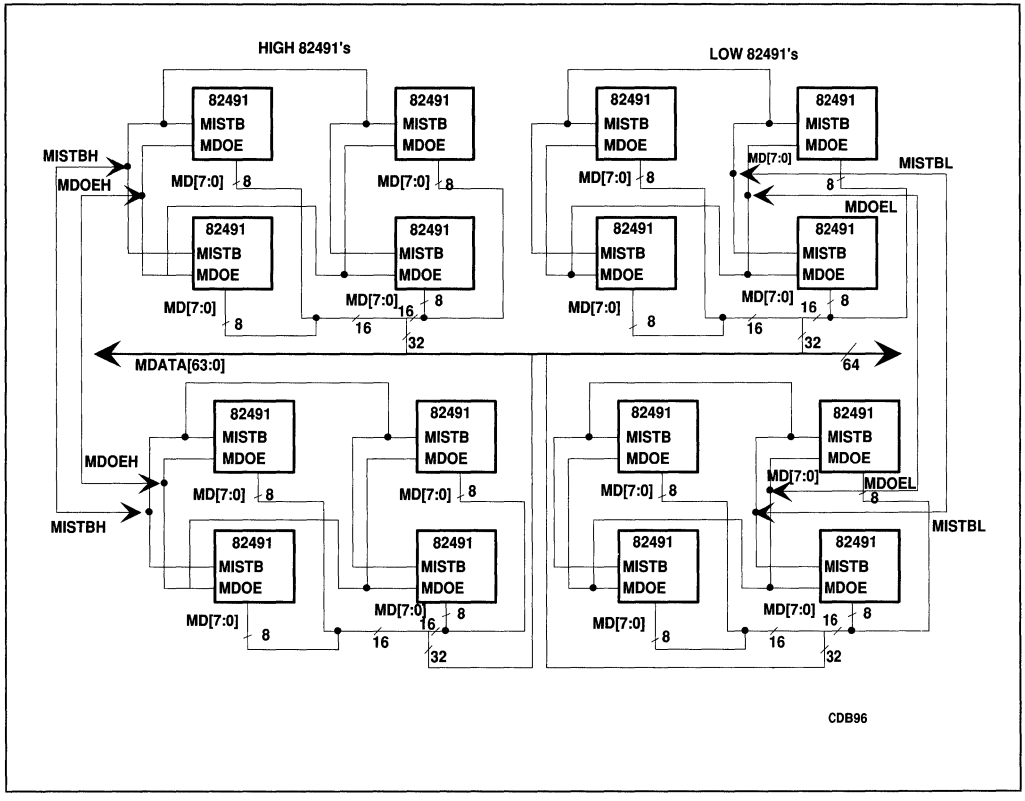


Figure 5-22. 512K Cache, 64-Bit Bus

5.1.10. 82496 Cache Controller Guaranteed Signal Relationships

The 82496 Cache Controller and 82491 Cache SRAM will guarantee certain signal relationships (i.e. specific signal assertion order during normal memory bus cycles). The Memory Bus Controller must also insure certain specific signal relationships for a Pentium processor CPU-Cache Chip Set subsystem. This section describes these signal relationships enforced by the 82496 Cache Controller and 82491 Cache SRAM, and those which the MBC must enforce.

1. CADS# will occur before or with CDTS#. (CADS# <= CDTS#).
2. Address (MSET, MTAG, MCFA), address parity (MAP), cycle control (APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, MBT[3:0], MCACHE#, NENE#, PALLC#, RDYSRC, SMLN#), and locking signals (KLOCK#) will be stable with respect to CADS# (see CADS# pin description for details).
3. Write data from the 82491 Cache SRAM will be stable (or the buffer available) with

respect to CDTS# (see CDTS# pin description for details).

5.1.11. 82496 Cache Controller Cycle Progress Requirements

1. All 82496 Cache Controller memory bus cycles initiated by CADS# (not SNPADS#) require BGT# and CRDY# activation.
2. KWEND# activation represents only the end of the cacheability window, and does not imply that the bus has been guaranteed to the 82496 Cache Controller (BGT#).
3. SWEND# activation represents only the end of the snooping window, and does not imply that the bus has been guaranteed to the 82496 Cache Controller (BGT#) or the closure of the cacheability window (KWEND#).
4. CRDY# activation represents only the end of the current cycle on the memory bus, and does not imply the closure of the snooping window (SWEND#).
5. In cycles which do not require KWEND# and/or SWEND# activation, those signals may be kept inactive. When KWEND# and SWEND# are applicable, they must fulfill the following precedence rule: BGT# <= KWEND# <= SWEND#.
6. Cycles initiated by SNPADS# require CRDY# but do not require other cycle progress signals (BGT#, KWEND#, SWEND#).

5.1.12. 82496 Cache Controller Input Signal Recognition Requirements

1. CNA# is recognized between BGT# and CRDY#. (BGT# <= CNA# <= CRDY#).
2. CNA# is recognized between CDTS# and CRDY#. (CDTS# <= CNA# <= CRDY#).
3. Once a signal is recognized, it is a "don't care" until CRDY#.
4. BGT# is only recognized after CADS# and after the CRDY# of the previous (pipelined) memory bus cycle, but only if neither SNPCYC# nor SNPBSY# and MHITM# are active (If SNPBSY# is active, BGT# is only blocked in hits to [M] cases - where the bus would be writing back the modified data).
5. If a signal is not recognized it may be held active until it is recognized (i.e. a signal is simply ignored until the recognition window opens).

5.1.13. 82496 Cache Controller and 82491 Cache SRAM CRDY# Requirements

1. CRDY# must be after CDTS#. (CDTS# < CRDY#).
2. CRDY# must be after BGT#. (BGT# < CRDY#).
3. Cycles initiated by SNPADS# require CRDY# but do not require other cycle progress signals (BGT#, KWEND#, SWEND#).
4. CRDY# must be after KWEND# for line fills and write-throughs with potential allocation.

(KWEND# < CRDY# (LFIL, WTPA)).

5. CRDY# must be at least 3 CPU clocks after BGT# for line fills and allocations. (BGT# + 3 <= CRDY# (LFIL, ALLOC)). (This to allow enough time for the 82496 Cache Controller to load the write-back buffers from the array if a replacement is needed).
6. On CPU read cycles, the last BRDY# (LBRDY#) of Cycle N must be activated prior to the CRDY# of cycle N+1. This rule insures that only one read cycle can be completed on the memory bus prior to completing delivery of the data to the CPU.
7. MEOC# for cycle N must be sampled with or before CRDY# for that cycle.
8. MEOC# for cycle N+1 must be sampled at least one CLK after CRDY# for cycle N.

5.1.14. 82496 Cache Controller Cycle Attribute Sampling Requirements

1. MKEN# and MRO# must meet set up and hold times to the CPU clock in which KWEND# is sampled active.
2. MWB/WT# and DRCTM# must meet set up and hold times to the CPU clock in which SWEND# is sampled active.

5.1.15. Pentium Processor, 82496 Cache Controller, and 82491 Cache SRAM BRDY# Requirements

1. The first BRDY# must be asserted with or following BGT#. (BRDY# >= BGT#).
2. The first BRDY# must be after CDTS#. (BRDY# > CDTS#).
3. For reads, data must be VALID and stable at the pins of the CPU on the CLK of BRDY#. The MBC is responsible for ensuring that other caches have been snooped (and modified data written back if necessary).
4. The last BRDY# for cycle N must be asserted one CLK before MEOC# for cycle N+1.
5. BRDY# of a non-cacheable 82496 Cache Controller Read cycle (MKEN# returned inactive) which is cacheable by the Pentium processor (active CACHE#), must be issued at least 1 CLK after KWEND# (at which time KEN# and BLAST# are valid).
6. BRDY# of a cacheable 82496 Cache Controller Read cycle (active MKEN#) which is non cacheable by the Pentium processor (inactive CACHE#) can be issued before, with, or after KWEND#.
7. For Read-Miss cycles, the first BRDY# must be > 1 + 4 * LR CLKs from the last SNPCYC# before BGT#. (Note: LR=Line Ratio)
8. For Read-Miss cycles, the first BRDY# of cycle N must be > 4 * LR CLKs from the first BRDY# of cycle N-1. (Note: LR=Line Ratio)

5.1.16. 82496 Cache Controller Cycle Progress Signal Sampling Requirements

Cycle Progress signal need to be active for at least 1 CLK in the specified window. When sampled active, the 82496 Cache Controller will hold their state internally until CRDY# of the cycle. Signals activated outside their specified window will be ignored.

For pipelined memory buses, sampling of the cycle progress signals will NOT be enabled before the CRDY# of the previous cycle.

1. BGT# is required for every CADS# initiated cycle. BGT# is not required for cycles that start with SNPADS#.
2. KWEND# is required only for cycles that use MKEN# and/or MRO# (cacheable memory read and write through with potential allocate).
3. SWEND# is required explicitly only for cycles which use MWB/WT# and/or DRCTM# and change tag states: line-fills, allocations, write-through potentially upgradeables.

NOTE

SWEND# has an additional function of enabling snoops. If SWEND# is not activated for a cycle, snoops will be disabled until CRDY# of the cycle.

4. CRDY# is required explicitly for all cycles, both CADS# and SNPADS# initiated.
5. CNA# is optional for all cycles.
6. During SNPADS# cycles the 82496 Cache Controller insures that CDTS# will be activated at least 1 CLK after SNPADS# and that CADS# and SNPADS# will never be activated on the same clock.
7. Snoop-Write-Back cycles:
   a. The 82496 Cache Controller only samples the CRDY# response.
   b. The 82496 Cache Controller assumes that the Bus Controller owns the bus to perform the intervening write-back (Restricted Back-Off Protocol) and that no other agents will snoop during this cycle.
   c. The 82496 Cache Controller will ignore CNA#.

NOTE

- Line fill = CM/IO# . !CW/R# . !MCACHE# . RDYSRC
- Allocation = CM/IO# . !CW/R# . !MCACHE# . !RDYSRC
- Write through potential allocate = !PALLC#
- Write through potential upgrade = CM/IO# . CW/R# . PALLC# . KLOCK# . !CPCD . !CPWT

5.1.17. 82491 Cache SRAM Data Control Signal Requirements

1. The first MBRDY# must come after CADS# assertion.
2. The last MBRDY# must come before or on the CLK of MEOC# assertion.
3. MEOC# is asserted before or on the same CLK as CRDY#.
4. MEOC# for cycle N+1 must be asserted at least one CLK after the CRDY# of cycle N.
5. MEOC# for cycle N+1 must be asserted at least one CLK after the last BRDY# of cycle N.

5.1.18. Semaphore (Strong Write Ordering) Consistency

In systems with multiple Pentium processor CPU-cache subsystems, it is possible to violate write ordering when the 82496 Cache Controller has been configured to be strong write ordered. This section describes an example of when system integrity can be violated, and provides the MBC "rules" which allow the 82496 Cache Controller to remain strongly write ordered.

The 82496 Cache Controller is optimized for high performance. In order to achieve this high performance the 82496 Cache Controller overlaps back-invalidations of the primary (processor) cache with other activities. Normally this overlapping does not cause any problems. However, in systems where Locked Semaphores are used to insure mutual exclusion of processor access to shared data, special care is needed to insure that once the semaphore has been obtained, that all back-invalidations of the primary Cache have been completed. This special care is needed to ensure that all data accessed within a CRITICAL REGION surrounded by a locked semaphore is strongly consistent (i.e., this will guarantee that the CPUs in the system will not get stale data).

Since the 82496 Cache Controller queues snoop back-invalidation cycles, it could happen that the CPU will get the data of a read-miss (to a semaphore) before the back-invalidation (of the semaphore-protected memory location) occurs. If the snoop is due to another processor writing to the entry protected by the semaphore, a data consistency problem occurs (i.e., the CPU will use stale data - the value prior to the other CPUs write). This can happen ONLY if the MBC provides the data for the read miss fast enough.

MBC rules for driving the first BRDY# of the read miss are defined here in order to ensure no reads around the back invalidation queue occur. These rules apply to READ cycles and I/O writes. These rules are necessary in order to ensure strong write ordering (note that LR is the Line-Ratio, and FBRDY# = first BRDY#):

1. FBRDY(N) > 1 + 4 * LR CLKs from the last SNPCYC# before the BGT# of the current cycle
2. FBRDY(N) > 4 * LR CLKs from FBRDY(N-1)

5.2. DETAILED PENTIUM PROCESSOR CPU-CACHE CHIP SET PIN DESCRIPTIONS

This section provides a detailed functional description of each external interface signal. The signals are listed in alphabetical order. The heading for each description summarizes the key pin attributes and is organized as follows:

Pin Symbol	Name
	Function
	Input or Output, Pin Number
	Synchronous or Asynchronous
	Internal Pull-Up/Down present or Glitch Free signal

Each heading is followed by three sections. The *Signal Description* section provides information about a signal's function, its usage and its operational mode. The *When Sampled/When Driven* section indicates when the signal is generated or sampled. The *Relation to Other Signals* section discusses how other signals are related to the signal, and discusses shared pins and synchronization requirements.

5.2.1. Signal/Category Cross-Reference

5.2.1.1. CONFIGURATION SIGNALS

CFG[2:0], CLDRV, FLUSH# (VCC), HIGHZ#, MALDRV, MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR#, SLFTST#, SNPMD, WWOR#

5.2.1.2. SNOOPING SIGNALS

MHITM#, MTHIT#, SNPADS#, SNPBSY#, SNPCLK, SNPCYC#, SNPINV, SNPNCA, SNPSTB#, MCFA[6:0], MSET[10:0], MTAG[11:0], MAP, MAPERR#

5.2.1.3. CYCLE ATTRIBUTE / PROGRESS SIGNALS

BGT#, BRDY#, CNA#, CRDY#, DRCTM#, KWEND#, MKEN#, MRO#, MWB/WT#, SWEND#

5.2.1.4. CYCLE CONTROL SIGNALS

APIC#, CAHOLD, CADS#, CD/C#, CDTS#, CM/IO#, CCACHE#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MCACHE#, NENE#, PALLC#, RDYSRC, SMLN#

5.2.1.5. MEMORY ADDRESS BUS AND ADDRESS CONTROL SIGNALS

MALE, MAOE#, MBALE, MBAOE#, MBE#[7:0], MBT[3:0], MCFA[6:0], MSET[10:0], MTAG[11:0], MAP, MAPERR#

5.2.1.6. MEMORY DATA BUS AND DATA CONTROL SIGNALS

MBRDY#(MISTB), MDATA[7:0], MDOE#, MEOC#, MFRZ#, MOCLK(MOSTB), MSEL#, MZBT#

5.2.1.7. CACHE SYNCHRONIZATION SIGNALS

FLUSH# (82496 Cache Controller), FSIOUT#, SYNC#

5.2.1.8. CPU SIGNALS

A20M#, APCHK#, BP[3:2], BP/PM[1:0], BRDY#, BREQ, BUSCHK#, CLK, FERR#, FLUSH# (Pentium processor), FRCMC#, HIT#, HLDA, HOLD, IBT, IERR#, IGNNE#, INIT, INTR, IU, IV, NMI, PCHK#, PEN#, PRDY, R/S#, RESET, SMI, SMIACT#

5.2.1.9. TEST SIGNALS

TCK, TDI, TDO, TMS, TRST#

5.2.1.10. PENTIUM PROCESSOR BUS OPTIMIZED INTERFACE SIGNALS

A[31:3] (Pentium processor), A[15:0] (82491 Cache SRAM) ADS#, ADSC#, AHOLD, AP, BE[7:0]#, BOFF#, BRDYC#, BRDYC1#, BT[3:0], CACHE#, CDATA[7:0], CFA[6:0], D/C#, D[63:0], DP[7:0], EADS#, EWBE#, HITM#, INV, KEN#, LOCK#, M/IO#, NA#, PCD, PWT, SCYC, SET[10:0], TAG[11:0], W/R#, WB/WT#

5.2.1.11. 82496 CACHE CONTROLLER/82491 CACHE SRAM OPTIMIZED INTERFACE SIGNALS

BLAST#, BLEC#, BRDYC2#, BUS#, MAWEA#, MCYC#, WAY, WBA[SEC2#], WBTYP[LR0], WBWE#[LR1], WRARR#

5.2.2. Pentium Processor CPU-Cache Chip Set Detailed Pin Descriptions

5.2.2.1. A[31:3]/A[15:0]

A[31:3] A[15:0]	Pentium processor Address bits 82491 Cache SRAM Address bits
	A[31:3] are Pentium processor Address pins and A[15:0] are 82491 Cache SRAM Address Pins.
	Input/Output Pentium processor signals (pins: V19, W05, V20, V06, V21, T09, U19, U08, U20, U09, U21, U10, T10, U11, T11, U12, T12, U13, T13, U14 T14, U15, T15, U16, T16, U17, U18, W19, T17) Input 82491 Cache SRAM signals (pins: 82, 81, 80, 79, 78, 77, 76, 75, 73, 71, 70, 69, 68, 67, 66, 65)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of the CPU A[31:3] signals.

82491 Cache SRAM address pins, A[15:1], are connected to CPU address pins A[17:3], and 82491 Cache SRAM address pin A0 is always connected to VSS. The Pentium processor Address pins, A[31:3], are connected to 82496 Cache Controller address pins CFA[6:0], SET[10:0], and TAG[11:0]. The specific address pin connections are configuration dependent. Refer to the Initialization and Configuration chapter for additional details.

5.2.2.2. A20M#

A20M#	Address bit 20 Mask
	Masks address bit 20.
	Input to Pentium processor (pin U05)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.3. ADS#

ADS#	Address Strobe
	Indicates the start of a CPU cycle to the cache SRAM.
	Output from Pentium processor (pin P04), Input to 82491 Cache SRAM (pin 63), Input to 82496 Cache Controller (pin C16)
	Synchronous to CLK
	82496 Cache Controller and 82491 Cache SRAM internal Pull-ups

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal. The Pentium processor ADS# output signal is connected to the 82491 Cache SRAM ADS# input pin. The 82496 Cache Controller ADS# input pin is connected to the Pentium processor ADSC# output signal.

5.2.2.4. ADSC#

ADSC#	Address Strobe
	Indicates the start of a CPU cycle to the cache controller.
	Output from Pentium processor (pin N04)
	Synchronous to CLK

Signal Description

This signal is functionally identical to the Pentium processor ADS# output signal, and is connected to the 82496 Cache Controller ADS# input. Refer to the *Pentium™ Processor Data Book* for a detailed description of the ADS# signal.

5.2.2.5. AHOLD

AHOLD	Address Hold
	Causes the CPU to float its address bus.
	Output from 82496 Cache Controller (pin B18), Input to Pentium processor (pin L02)
	Synchronous to CLK

Signal Description

AHOLD is the CPU bus address hold request. The 82496 Cache Controller will drive AHOLD active when it needs to perform CPU inquire, back-invalidation, flush, or sync cycles. When AHOLD is active, the CPU does not drive the CPU address bus. During address hold the 82496 Cache Controller will drive the address bus and address parity bits.

When Driven

The 82496 Cache Controller activates AHOLD during snoop write back cycles, replacement write back cycles, reset, initialization, and selftest.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CAHOLD	Reflects the value of AHOLD on the memory bus (except during BIST).

5.2.2.6. AP

AP	Address Parity
	Indicates CPU address bus parity.
	Input/Output between 82496 Cache Controller (pin A08), and Pentium processor (pin P03)
	Synchronous to CLK

Signal Description

AP is a CPU bus address parity signal. It indicates the parity of the Pentium processor line address bits (i.e., A[31:5]).

When Driven

AP is driven by the Pentium processor when AHOLD is inactive (CPU initiated cycles), and is driven by the 82496 Cache Controller when AHOLD is active (for example, during processor snoop, flush, or sync cycles). For processor initiated cycles, AP is valid from ADS# to NA or BRDY#. For processor snoop cycles, the 82496 Cache Controller drives AP valid during the CLK of EADS#. Note that BT[3:0] must be low for the 82496 Cache Controller to generate a correct AP signal.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
A[31:5]	AP represents the parity of the Pentium processor line address, A[31:5], and the corresponding 82496 Cache Controller address lines (i.e., CFA, TAG, SET).
AHOLD	AP is an input to the 82496 Cache Controller (from the Pentium processor) when AHOLD=0, and an output from the 82496 Cache Controller (to the Pentium processor) when AHOLD=1.

5.2.2.7. APCHK#

APCHK#	Address Parity Check Status
	Indicates a CPU address bus parity error during inquire or back invalidation cycles.
	Output from Pentium processor (pin W03)
	Synchronous to CLK
	Glitch Free

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.8. APERR#

APERR#	Address Parity Error
	Indicates that a CPU Bus address parity error occurred.
	Output from 82496 Cache Controller (pin S01)
	Synchronous to CLK
	Glitch Free

Signal Description

APERR# is driven active in CPU cycles whenever there is a CPU address parity checking error.

When Driven

APERR# is activated at least two CLKs after ADS#, and stays active for a minimum of one CPU CLK. The 82496 Cache Controller begins checking address parity on the clock of the CPU ADS#, and will keep checking until the address is internally latched. This internal latching is guaranteed to happen before NA# or the first BRDY#.

APERR# is inactive during RESET, and remains inactive until at least 5 CLKs after RESET goes inactive.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CFA,SET,TAG	APERR# is driven active only after a wrong line address parity is driven to the 82496 Cache Controller on the AP input during a CPU cycle.

5.2.2.9. APIC#

APIC#	Advanced Programmable Interrupt Controller Address Decoding
	Indicates cycle address in an APIC* address.
	Output from 82496 Cache Controller (pin N01)
	Synchronous to CLK

* Refer to the "82489DX Advanced Programmable Interrupt Controller - Advance Information," July 1992, Order Number 290446-001.

Signal Description

APIC# is asserted by the 82496 Cache Controller to indicate that the address of a given memory cycle is an APIC address (i.e., FE E0 00 00 - FE E0 03 FF Hex). APIC is the advanced programmable interrupt controller for 32 bit high performance operating systems. It has features built-in which improve performance in multitasking operating systems (both uniprocessor and multiprocessor). It meets the functional requirements of interrupt controllers in multiprocessor systems. Note that BT[3:0] must be low in order to ensure the proper assertion of APIC#.

When Driven

APIC# is valid with CADS# and remains valid until CNA# or CRDY# is asserted.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
MCFA, MSET, MTAG	APIC# is a pure address decode of MCFA, MSET, MTAG.

5.2.2.10. BE#,BE[7:0]#

BE[7:0]# BE#	Pentium processor Byte Enables 82491 Cache SRAM Byte Enable
	Controls data for partial writes.
	Output from Pentium processor (pins W01, U07, S04, T06, V01, U06, Q04, U04), Input to 82491 Cache SRAM (pin 64)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of the BE[7:0]# signals. For a 512K cache configuration (16 82491 Cache SRAM devices), each BE[7:0]# output of the Pentium processor is connected to the BE# input of two 82491 Cache SRAM devices.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CDATA[7:4]	The Pentium processor byte enable outputs are connected to the 82491 Cache SRAM CDATA[7:4] pins for 82491 Cache SRAMs configured to be data parity devices. Refer to section 5.1.6.5.

5.2.2.11. BGT#

BGT#	Bus Guaranteed Transfer
	Indicates MBC commitment to bus cycle completion.
	Input to 82496 Cache Controller (pin N04)
	Synchronous to CLK
	Internal Pull-up

Signal Description

The 82496 Cache Controller owns all bus cycles initiated by CADS# until the MBC accepts ownership, and within this period, cycles may be aborted because of snoop write-backs. The MBC signals its acceptance of ownership by driving BGT# active. CRDY# signals cycle completion.

Once BGT# is asserted, the 82496 Cache Controller does not perform snoop lookups until the end of the snooping window (until SWEND# is active). A snoop address is latched if SNPSTB# is asserted between BGT# and SWEND#, but the snoop lookup does not begin until the second CLK after SWEND# is sampled active by the 82496 Cache Controller.

When Sampled

The 82496 Cache Controller begins sampling the BGT# input after it asserts CADS#. BGT# should be asserted prior to or with MEOC# for a given cycle.

BGT# is a "don't care" input after it has been recognized for a particular cycle and until CRDY# (regardless of a pipelined CADS# issued before CRDY#). BGT# is ignored if there is no outstanding CADS#. BGT# is also a "don't care" signal once a cycle started by CADS# is aborted by a snoop and until a new CADS# is issued.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDY#	BGT# must be asserted with or before BRDY# assertion by the MBC.
CADS#	BGT# follows every assertion of CADS# unless the cycle is aborted because of a snoop.
CNA#	CNA# is recognized between BGT#/CDTS# (the later of the two) and CRDY#.
CRDY#	BGT# must precede CRDY#. BGT# must precede CRDY# by at least three CLKS for line fills and allocations.
	BGT# is only recognized after the CRDY# of the previous memory bus cycle, but only if neither SNPCYC# nor SNPBSY# and MHITM# are active (If SNPBSY# is active, BGT# is only blocked in hits to [M] cases - where the bus would be writing back the modified data).
KWEND#	BGT# must be asserted before or with the KWEND# and SWEND# assertion.
MEOC#	BGT# must be asserted before or with MEOC# assertion.
MHITM#	BGT# is ignored when SNPCYC# is active and when both SNPBSY# and MHITM# are active.
SNPADS#	BGT# is not required following SNPADS# assertion.
SNPBSY#	BGT# is ignored when SNPCYC# is active and when both SNPBSY# and MHITM# are active.
SNPCYC#	BGT# is ignored when SNPCYC# is active and when both SNPBSY# and MHITM# are active.
SWEND#	BGT# must be asserted before or with the KWEND# and SWEND# assertion.

5.2.2.12. BLAST#

BLAST#	Burst Last
	Indicates the end of a burst cycle.
	Output from 82496 Cache Controller (pin D16), Input to 82491 Cache SRAM (pin 59)
	Synchronous to CLK

Signal Description

BLAST# indicates that the current CPU BRDY# or BRDYC# is the last of the burst sequence. The 82496 Cache Controller will decode cycle length information from the Pentium processor CACHE# and D/C# pins, and from the MKEN# and MRO# inputs from the MBC. It will drive BLAST# as an output to provide the burst last indication to the 82491 Cache SRAMs.

Refer to Table 5-1 in section 5.1.1.1 for cycle identification and length details.

When Driven

BLAST# is driven with the last BRDYC# of a burst sequence or with the single BRDYC# of a non-burst cycle.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDYC#	BLAST# qualifies the BRDYC# signal to the 82491 Cache SRAMs.

5.2.2.13. BLE#

BLE#	Byte Enable Latch Enable
	Controls the enable line of an external byte enable latch.
	Output from 82496 Cache Controller (pin D17)
	Synchronous to CLK

Signal Description

BLE# is used to control the enable line of a 377-type external byte enable latch (Clock Edge Triggered). This signal is not necessary when using the Pentium processor with the 82496 Cache Controller/82491 Cache SRAM cache since those signals are latched within the 82496 Cache Controller and 82491 Cache SRAM and are passed to the MBC. This latch is used to capture CPU signals which were not latched within the C5 Cache Controller or C8 Cache SRAM (e.g. PWT, PCD, CACHE#, SCYC, and BE[7:0]#) for the Intel486™ DX or i860™ XP CPUs.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BLEC#	BLE# is functionally identical to BLEC#.

5.2.2.14. BLEC#

BLEC#	Byte Enable Latch Enable
	Controls the enable line of an internal byte enable latch.
	Output from 82496 Cache Controller (pin P19), Input to 82491 Cache SRAM (pin 34)
	Synchronous to CLK
	82491 Cache SRAM internal Pull-down

Signal Description

BLEC# is used to control the enable line of a 377-type internal byte enable latch (clock edge triggered) in the 82491 Cache SRAMs. BLEC# causes the CPU byte enable signals to be latched within 8 of the 82491 Cache SRAM devices, and held on the 82491 Cache SRAM MBE# outputs.

The byte enable latching is controlled by a 82491 Cache SRAM input, BLEC#, from the 82496 Cache Controller. The latch samples BE# at each clock rising edge when BLEC# is low. When BLEC# is high, the latch is closed and MBE# [PAR#] is driven to the memory bus according to the corresponding CPU BE[7:0]# level.

NOTE

Connect 8 82491 Cache SRAM BLEC# input pins to the 82496 Cache Controller BLEC# output. Remaining 82491 Cache SRAM BLEC# inputs must be either connected to VSS or left as no-connects.

When Driven

BLEC# is driven inactive to hold the CPU byte enables when the 82496 Cache Controller samples ADS# asserted and there is no cycle active on the memory bus. See Figure 5-23.

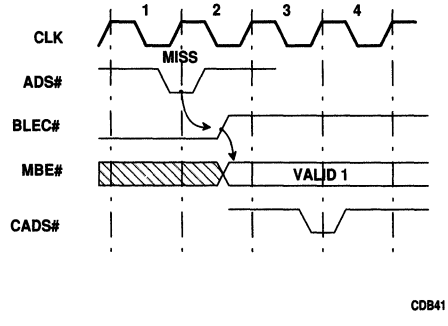


Figure 5-23. BLEC# Deassertion Due to ADS# Assertion

If an ADS# for a cycle which needs the memory bus has been previously issued, and the 82496 Cache Controller samples CNA# or CRDY# asserted (for a previous memory bus cycle), then the 82496 Cache Controller will assert BLEC# for one CLK to latch the CPU byte enables. See Figure 5-24.

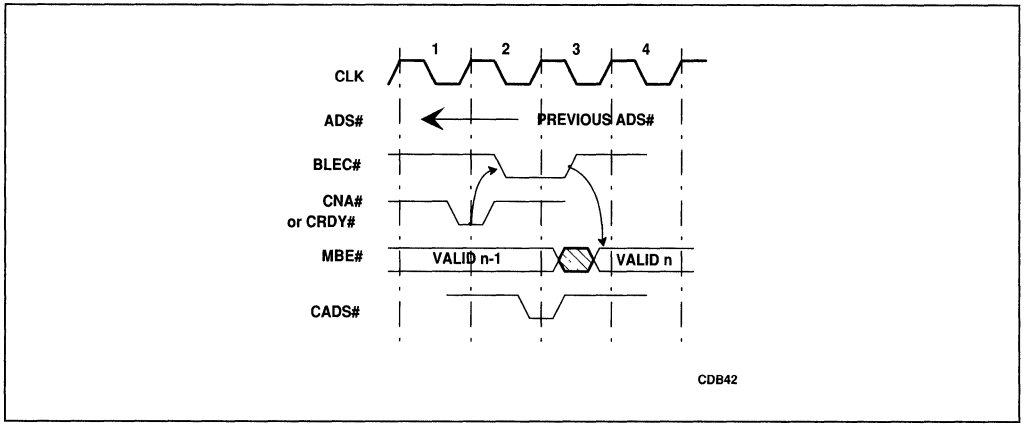


Figure 5-24. BLEC# Assertion Due to CNA# or CRDY# Assertion

If the ADS# cycle to the 82496 Cache Controller is a cache hit, then BLEC# will be asserted immediately (i.e., it could be inactive for as short as one CLK as shown, or longer). See Figure 5-25.

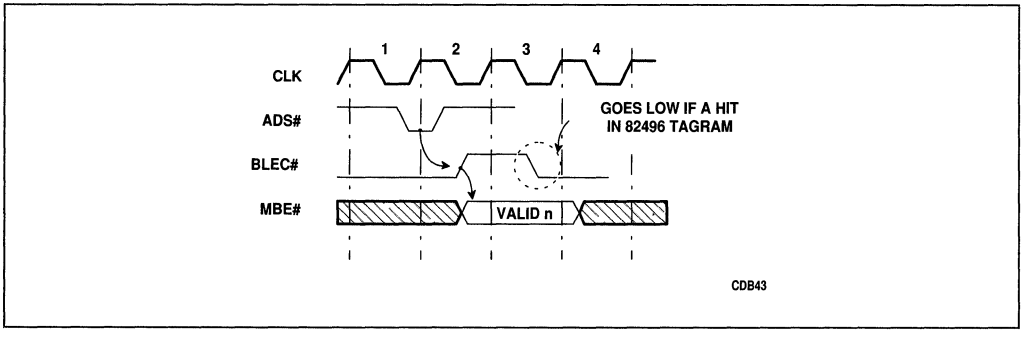


Figure 5-25. BLEC# Assertion Due to Hit in 82496 Cache Controller TagRAM

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BLE#	BLEC# is functionally identical to BLE#.
BE[7:0]#	BLEC# causes the CPU byte enables, BE[7:0]#, to be latched in the 82491 Cache SRAM devices and driven out to the memory bus on the MBE# pins.

5.2.2.15. BOFF#

BOFF#	Back Off
	Prevents CPU bus deadlock by aborting outstanding Pentium processor cycles.
	Output from 82496 Cache Controller (pin H16), Input to Pentium processor (pin K04) and 82491 Cache SRAM (pin 36)
	Synchronous to CLK
	82491 Cache SRAM internal Pull-up

Signal Description

This signal is an input to the Pentium processor and gives the 82496 Cache Controller the capability to abort a CPU cycle when required. The 82496 Cache Controller will only activate BOFF# during situations where a deadlock exists (e.g., CPU miss cycle, 82496 Cache Controller inquire cycle: deadlock on usage of the CPU bus). BOFF#, when asserted, allows the 82496 Cache Controller to prevent CPU bus deadlock by causing the Pentium processor to abort the current cycle and float its bus.

BOFF# is also an input to the 82491 Cache SRAMs and, when active, causes the SRAMs to clear their CPU bus cycle information since the current CPU bus cycle will be aborted. Activity on the memory bus (i.e., a posted write) will continue without interruption.

When Driven

BOFF# is driven when an inquire to the Pentium processor hits a line in [M] state, and there is an outstanding cycle that cannot be completed (cannot receive its last BRDY# or BRDYC#). The BOFF# signal will be driven for 1 CLK only.

Relation to Other Signals

None.

5.2.2.16. BP[3:2], PM/BP[1:0]

BP[3:2], PM/BP[1:0]	Breakpoint and Performance Monitoring
	BP[3:0] externally indicate a breakpoint match.
	Outputs from Pentium processor

Signal Description

Please refer to Appendix A for more information.

5.2.2.17. BRDY#

BRDY#	Burst Ready
	Burst ready input.
	Input to Pentium processor (pin L04), 82496 Cache Controller (pin Q02), and 82491 Cache SRAM (pin 60)
	Synchronous to CLK

Signal Description

BRDY# is an MBC output to the Pentium processor, 82496 Cache Controller cache controller, and 82491 Cache SRAM cache memories. In the CPU, BRDY# provides the BRDY# function described in the Pentium processor DATA BOOK. In the 82491 Cache SRAM memories, BRDY# increments the CPU latch burst counter.

During CPU initiated memory bus read cycles, BRDY# advances the 82491 Cache SRAM CPU latch burst counter to allow the next 64-bit read data slice to be available on the CPU data bus. At the same time, BRDY# latches the previous data slice into the CPU.

With the exception of I/O cycles, BRDY# is not needed during writes because the cache posts CPU write cycles.

During special CPU cycles and I/O cycles, BRDY# is used to end the CPU cycle.

BRDY# must not be asserted until the bus is granted (until BGT# is asserted) and until the data path is ready for transfers (until data is valid-CDTS# is asserted).

When Sampled

BRDY# is sampled by the CPU, 82496 Cache Controller and 82491 Cache SRAM at every CLK edge. BRDY# must always meet proper set-up and hold times. BRDY# assertion advances the CPU latch counter in the 82491 Cache SRAM even when the CPU latch is not in use.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	BRDY# must be asserted on the same CLK or after BGT# is asserted.
	For Read-Miss cycles, the first BRDY# must be > 1 + 4*LR CLKs from the last SNPCYC# before BGT#. (Note: LR=Line Ratio).
BRDY# (N-1)	For Read-Miss cycles, the first BRDY# of cycle N must be > 4*LR CLKs from the first BRDY# of cycle N-1. (Note: LR=Line Ratio).
CDTS#	BRDY# must be asserted after CDTS# is asserted.
CRDY#	On CPU read cycles, the last BRDY# (LBRDY#) of Cycle N must be activated prior to the CRDY# of cycle N+1.
KWEND#	BRDY# of a non-cacheable 82496 Cache Controller cycles (MKEN# returned inactive) which is cacheable by the Pentium processor (active CACHE#), must be issued after KWEND# (at which time KEN# is valid).
MEOC#	MEOC# for cycle N+1 must be asserted at least one CLK after the last BRDY# of cycle N.
SNPCYC#	For Read-Miss cycles, the first BRDY# must be > 1 + 4*LR CLKs from the last SNPCYC# before BGT#. (Note: LR=Line Ratio).

5.2.2.18. BRDYC#

BRDYC#	Burst Ready Cache
	Data input and output control signal.
	Input to Pentium processor (pin L03) and 82491 Cache SRAM (pin 61)
	Synchronous to CLK

Signal Description

See BRDYC1# and BRDYC2# signal descriptions.

5.2.2.19. BRDYC1#

BRDYC1#	Burst Ready Cache 1
	Data input and output control signal.
	Output from 82496 Cache Controller (pin E16), to Pentium processor BRDYC# Input
	Synchronous to CLK

Signal Description

The 82496 Cache Controller burst ready output indicates to the Pentium processor that the 82496 Cache Controller/82491 Cache SRAM cache subsystem has either presented data to the CPU or accepted data from the CPU.

When Driven

BRDYC1# is driven during non-locked read hit cycles when data from the 82491 Cache SRAM is read on the CPU bus. BRDYC1# is driven during write cycles when the 82491 Cache SRAM write buffer and/or 82491 Cache SRAM array is available to accept the write data.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDYC# (processor)	BRDYC1# is connected to the CPU BRDYC# input.
BRDYC2#	BRDYC1# and BRDYC2# are logically equivalent.

5.2.2.20. BRDYC2#

BRDYC2#	Burst Ready Cache 2
	Data input and output control signal.
	Output from 82496 Cache Controller (pin G15) to 82491 Cache SRAM BRDYC# Input
	Synchronous to CLK

Signal Description

The 82496 Cache Controller burst ready output indicates to the 82491 Cache SRAM SRAMs that the 82496 Cache Controller/82491 Cache SRAM cache subsystem has either presented data to the CPU or accepted data from the CPU.

When Driven

BRDYC2# is driven during non-locked read hit cycles when data from the 82491 Cache SRAM is read on the CPU bus. BRDYC2# is driven during write cycles when the 82491 Cache SRAM write buffer and/or 82491 Cache SRAM array is available to accept the write data.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDYC# (82491 Cache SRAM)	BRDYC2# is connected to the 82491 Cache SRAM BRDYC# input.
BRDYC1#	BRDYC2# and BRDYC1# are logically equivalent.

5.2.2.21. BREQ

BREQ	Bus Request
	Indicates that the Pentium processor has generated a bus request.
	Output from Pentium processor (pin V02)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.22. BT[3:0]

BT[3:0]	Branch Trace Address bits
	Provides bits 0-2 of the branch target linear address and the default operand size during a Branch Trace Message Special Cycle.
	Output from Pentium processor (pins: W20, T07, W21, T08) Input to 82496 Cache Controller (pins: A10, A12, A14, A16)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of these signals.

The system designer has the option to either connect or leave unconnected the BT[3:0] pins between the Pentium processor and the 82496 Cache Controller.

If the BT[3:0] pins are left unconnected between the Pentium processor and the 82496 Cache Controller, the MBT[3:0] outputs of the cache controller reflect a latched version of the BT[3:0] inputs during Branch Trace Message Special Cycles.

If the BT[3:0] pins are left unconnected between the Pentium processor and the 82496 Cache Controller, external pulldowns must be connected to the BT[3:0] pins of the 82496 Cache Controller during normal operation. The system designer may then monitor the BT[3:0] outputs of the Pentium processor during Branch Trace Message Special Cycles.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MBT[3:0]	The 82496 Cache Controller MBT[3:0] outputs reflect the BT[3:0] inputs during Branch Trace Message Special Cycles.

5.2.2.23. BUS#

BUS#	Bus/Array Select
	Multiplexes memory bus or array path to Pentium processor/82491 Cache SRAM bus.
	Output from 82496 Cache Controller (pin Q17), Input to 82491 Cache SRAM (pin 40)
	Synchronous to CLK

Signal Description

BUS# controls the selection of CPU buffer data during read operations. When this pin is sampled active, the 82491 Cache SRAM will set an internal mux so that CPU read data comes from the memory bus (memory cycle buffers) instead of the array. The internal mux will stay in this condition until BRDY#*BLAST#.

This signal is used, for example, during locked read hits which hit a modified line in the 82496 Cache Controller/82491 Cache SRAM cache. In these cases data must come from the 82491 Cache SRAM array (BUS# inactive) even though the read cycle goes out to the memory bus.

BUS# has no meaning during write cycles.

Relation to Other Signals

None.

5.2.2.24. BUSCHK#

BUSCHK#	Bus Cycle Check
	Indicates an unsuccessful completion of a bus cycle.
	Input to Pentium processor (pin T03)
	Synchronous to CLK

Signal Description

To configure the I/O buffers of the Pentium processor for use with the 82496 Cache Controller/82491 Cache SRAM secondary cache as a chip set, BUSCHK# must be driven by the MBC to the value shown in Table 4-1 (refer to section 4.1.1 at least 4 CPU clocks prior to the falling edge of RESET.

To simplify the configuration process, the Pentium processor BUSCHK# input can be tied to the inverse of RESET with a 0 ohm resistor in the path. The purpose of the resistor is to allow changing the polarity with minimal impact ot the system design. If the resistor is removed, this input is high due to the internal pullup resistor. If the resistor is in the circuit, the input is low (inverse of the active RESET).

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.25. CACHE#

CACHE#	Pentium processor Internal Caching Indication
	Indicates Pentium processor internal cacheability attribute.
	Output from Pentium processor (pin J04), Input to 82496 Cache Controller (pin H15)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.26. CADS#

CADS#	Cache Address Strobe
	Indicates beginning of a memory bus cycle.
	Output from 82496 Cache Controller (pin F04)
	Synchronous to CLK
	Glitch Free

Signal Description

CADS# requests memory bus cycle execution and indicates that the address (e.g. MSET, MTAG, MCFA, MAP) and cycle control signals (i.e., CW/R#, CM/IO#, CD/C#, CDTS#, CCACHE#, CPCD, CPWT, CSCYC, CWAY, PALLC#, RDYSRC, MBE#, MCACHE#, NENE#, SMLN#, and KLOCK#) are valid.

Every memory bus cycle is initiated by CADS# or SNPADS#.

If the 82496 Cache Controller receives a snoop request and reports a hit to a line in [M] state before BGT# is asserted, the cycle for which CADS# was issued is aborted and sometimes re-issued after the snoop-write-back has completed. If the current line (e.g. issued by the stalled CADS#) is invalidated by the snoop, then that CADS# is canceled (i.e., will not be re-issued after the snoop has completed).

CADS# is a glitch-free signal.

When Driven

CADS# is asserted by the 82496 Cache Controller for exactly one CLK and is always valid.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
Address and Cycle Specification Signals	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
ADS#	Usually CADS# is a 2 CLK delay from Pentium processor ADS# signal.
BGT#	Every cycle that is initiated by CADS# requires BGT# and CRDY# inputs from the MBC.
CDTS#	CADS# = CDTS# for all write-through cycles. Since allocations do not require BRDY#s to the CPU, the CDTS# of an allocation cycle will always occur with CADS# of the linefill.
	CADS# will occur before or with CDTS#. (CADS# <= CDTS#).
CRDY#	Every cycle that is initiated by CADS# requires BGT# and CRDY# inputs from the MBC.
MBRDY#	The first MBRDY# must come after CADS# assertion.
SNPADS#	The 82496 Cache Controller never asserts CADS# and SNPADS# on the same CLK. There are always one or more CLKs between CADS# and a following SNPADS#. There are always one or more CLKs between SNPADS# and a following CADS#.

5.2.2.27. CAHOLD

CAHOLD	Cache AHOLD Output
	AHOLD output and self-test result.
	Output from 82496 Cache Controller (pin H05)
	Synchronous to CLK

Signal Description

CAHOLD reflects the AHOLD input to the Pentium processor (which is generated by the 82496 Cache Controller).

When the Pentium processor AHOLD is asserted, CAHOLD is also asserted. CAHOLD can be monitored by the MBC to determine when the 82496 Cache Controller is performing CPU inquires and back-invalidations. It can also be used to determine when to return BRDY# to the CPU for Flush and Write Back special cycles.

CAHOLD is used during 82496 Cache Controller self-test to indicate the pass/fail condition. It can be sampled in the CLK after the deassertion of FSIOUT# to determine the success or failure of BIST. CAHOLD high indicates the successful completion of BIST.

When Driven

CAHOLD is always at a valid logic level. CAHOLD is asserted whenever AHOLD is asserted to the CPU.

During BIST, CAHOLD is driven low immediately upon the detection of an error (even before FSIOUT# goes inactive).

Relation to Other Signals

Pin Symbol	Relation to Other Signals
AHOLD	Except during 82496 Cache Controller self-test, CAHOLD reflects the value of AHOLD (with no delay).

5.2.2.28. CCACHE#

CCACHE#	Latched Pentium processor CACHE# signal
	A latched version of the Pentium processor CACHE# output signal.
	Output from 82496 Cache Controller (pin H01)
	Synchronous to CLK

Signal Description

CCACHE# reflects the Pentium processor CACHE# output signal during a CPU cycle on the memory bus. CCACHE# is active (LOW) during CPU write-backs and CPU cacheable reads. CCACHE# is undefined for 82496 Cache Controller write back, snoop write back, and allocation cycles.

CCACHE# is used by the MBC to determine the number of BRDY#s to provide to the CPU. See Table 5-2.

Table 5-2. CCACHE# Use in Determining the Number of BRDY#s

Number of BRDY#s	CCACHE#	Read-Only	CD/C#
1	1	x	x
1	x	Yes	1
4	0	Yes	0
4	0	No	x

When Driven

CCACHE# is valid from the CLK of CADS# until the CLK of CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.29. CD/C#

CD/C#	Cache Data/Code
	Indicates whether cycle requests code or data.
	Output from 82496 Cache Controller (pin E04)
	Synchronous to CLK

Signal Description

CD/C#, CW/R# and CM/IO# are 82496 Cache Controller cycle definition signals. CD/C# indicates whether a bus cycle requests data or code.

CD/C# is high for 82496 Cache Controller initiated cycles (i.e., 82496 Cache Controller replacement write back, 82496 Cache Controller snoop write back, and allocation).

During read only read miss cycles, CD/C# helps to determine the number of BRDY#s which the MBC must provide to the CPU. If CD/C# is low, the MBC must provide 4 BRDY#s. If CD/C# is high, the MBC must provide one BRDY# (non-cacheable by the CPU).

When Driven

CD/C# is valid in the same CLK as CADS# and SNPADS# and remains valid until CRDY# or CNA# is asserted. C/DC# remains undefined in other instances.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.30. CDATA[7:0]

CDATA[7:0]	Cache Data Pins
	I/O data bus between the 82491 Cache SRAM and the Pentium processor.
	Input/Output between Pentium processor D[63:0] and 82491 Cache SRAM (pins 57, 52, 51, 46, 55, 49, 54, 48)
	Synchronous to CLK

Signal Description

The 82491 Cache SRAM CDATA[7:0] signals connect to the Pentium processor data pins D[63:0]. The specific data pin connections are cache size and configuration dependent.

For cache configurations which only require 4 MDATA pins, bits 3-0 are used. Unused CDATA[7:4] pins must be tied to either VSS or VCC through resistors.

Refer to the *Pentium™ Processor Data Book* for a detailed description of the Pentium processor D[63:0] signals.

When Driven/Sampled

CDATA[7:0] are sampled with proper valid delays in the CLK that BRDYC# is driven to the Pentium processor. CDATA[7:0] are driven by the 82491 Cache SRAM with proper setup and hold times in the CLK that BRDYC# is driven to the processor. Refer to the *Pentium™ Processor Data Book* for data signal driving/sampling requirements.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BE[7:0]#	The Pentium processor Byte Enable outputs are connected to the 82491 Cache SRAM CDATA[7:4] pins for 82491 Cache SRAMs configured to be data parity devices. Refer to section 5.1.6.5.
DP[7:0]	The Pentium processor Data parity signals are connected to the 82491 Cache SRAM CDATA[3:0] pins for 82491 Cache SRAMs configured to be data parity devices. Refer to section 5.1.6.5.

5.2.2.31. CDTS#

CDTS#	Cache Data Strobe
	Indicates CPU data bus or memory data is available.
	Output from 82496 Cache Controller (pin G05)
	Synchronous to CLK
	Glitch Free

Signal Description

During read cycles, CDTS# indicates that the CPU data bus path is available in the next CLK. CDTS# indicates the earliest period in which BRDY# may be supplied to the CPU. The first BRDY# can be issued to the processor 1 CLK after CDTS# is sampled active by the MBC.

During CPU-initiated write cycles, CDTS# indicates that data is available on the memory bus (the MBC can provide the first MBRDY# in the next CLK).

During write-back and snoop cycles, the 82496 Cache Controller generates CDTS# to indicate to the MBC that write-back data is valid in the 82491 Cache SRAM write-back buffer (the MBC can provide the first MBRDY# in the next CLK).

Note that MBRDY# is sampled by the 82491 Cache SRAM with MCLK (not CPU CLK). It is the responsibility of the MBC to ensure that there is one full CPU CLK between CDTS# driven active and a following MBRDY#.

For processor inquire cycles, CDTS# informs the MBC that the last piece of inquire data is valid on the CPU bus.

CDTS# enables independent address strobes (CADS# and SNPADS#) and data strobes. As soon as addresses are available, the 82496 Cache Controller can use CADS# to indicate to the MBC that a new cycle has begun. This allows memory bus cycles to begin even before data is ready to be provided or received.

When Driven

CDTS# is always valid.

CDTS# is asserted with or following CADS# and after SNPADS# assertion for a duration of one CLK.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDY#	When the MBC samples CDTS# active, it can provide the CPU with read cycle BRDY# signals in the following CLK.
	The first BRDY# must be after CDTS#. (BRDY# > CDTS#).
CADS#	CADS# == CDTS# for all write-through cycles. Since allocations do not require BRDY#s to the CPU, the CDTS# of an allocation cycle will always occur with CADS# of the linefill.
	CADS# will occur before or with CDTS#. (CADS# <= CDTS#).
CNA#	CNA# is recognized between CDTS# and CRDY#. (CDTS# <= CNA# <= CRDY#).
CRDY#	CRDY# must be after CDTS#. (CDTS# < CRDY#).
MBRDY#	For write cycles, when the MBC samples CDTS# active, it can provide the 82491 Cache SRAM MBRDY#s in the following MCLK.
MDATA[7:0]	Write data from the 82491 Cache SRAM will be stable, on the MDATA[7:0] pins (or the buffer available), with respect to CDTS#.
SNPADS#	CDTS# is asserted at least one clock after SNPADS#.

5.2.2.32. CFA[6:0],SET[10:0],TAG[11:0]

CFA[6:0],	Configurable Address Pins
SET[10:0],	Contains the current physical address.
TAG[11:0]	Input/Output between Pentium processor address pins and 82496 Cache Controller (pins E15, F15, B17, C03, E07, C15, F16, B10, C10, E11, E10, E13, D12, D13, C13, D15, D14, E14, D06, C02, B02, E08, B03, D08, C04, C05, B04, E09, B05, D09)
	Synchronous to CLK

Signal Description

These configurable address pins are connected to CPU address pins A[31:3]. The specific address pin connections are configuration dependent. Refer to the Initialization and Configuration chapter for additional details.

Refer to the *Pentium™ Processor Data Book* for a detailed description of the A[31:3] signals.

5.2.2.33. CFG[2:0]

CFG[2:0]	Configuration pins
	Determine cache characteristics.
	Configuration Inputs to 82496 Cache Controller (pins N05, R02, M05)
	Synchronous to CLK

Signal Description

CFG[2:0] are physical cache configuration inputs that determine cache characteristics such as line ratio, tag size and lines per sector.

When Sampled

CFG[2:0] are sampled and used as shown in the Initialization and Configuration chapter. After sampling, CFG[2:0] become cycle progress input signals to the 82496 Cache Controller and are sampled after CADS# of the first cycle.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	CFG[2:0] are sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
CNA#	CFG0 shares a pin with CNA#.
KWEND#	CFG2 shares a pin with KWEND#.
SWEND#	CFG1 shares a pin with SWEND#.

5.2.2.34. CLDRV

CLDRV	82491 Cache SRAM Cache Low Drive
	Selects 82496 Cache Controller output driving buffers for 82491 Cache SRAM signals.
	Configuration Input to 82496 Cache Controller (pin N04)
	Synchronous to CLK

Signal Description

CLDRV selects the driving strength of the 82496 Cache Controller buffers that interface to the 82491 Cache SRAM.

When Sampled

CLDRV is a configuration input which is sampled as shown in the Initialization and Configuration chapter. The 82496 Cache Controller to 82491 Cache SRAM control signals (BLAST#, BLEC#, BUS#, MAWEA#, MCYC#, WAY, WBA[SEC2#], WBTYP[LR0], WBWE#[LR1], WRARR#) can be configured for one of two buffers. The buffer selection is made by using the CLDRV configuration input. CLDRV must be driven by the MBC to the value shown in Table 4-7 for at least 10 CPU clocks prior to the falling edge of RESET.

After it is sampled, CLDRV is a "don't care" signal until after CADS# is asserted for the first time, when it becomes the BGT# pin.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	CLDRV is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
BGT#	CLDRV shares a pin with BGT#.

5.2.2.35. CLK

CLK	Pentium processor CPU-Cache Chip Set Clock
	CPU clock inputs.
	Input to Pentium processor (pin K18), 82496 Cache Controller (pin E12), and 82491 Cache SRAM (pin 30)

Signal Description

The CLK input determines the execution rate and timing of the Pentium processor CPU-Cache Chip Set. Pin timings are specified relative to the rising edge of this signal. The CLK input requires TTL levels for proper operation.

5.2.2.36. CM/IO#

CM/IO#	Cache Memory/IO
	Indicates whether current cycle is Memory or I/O.
	Output from 82496 Cache Controller (pin E05)
	Synchronous to CLK

Signal Description

CM/IO#, CW/R# and CD/C# are 82496 Cache Controller cycle definition signals which indicate whether an 82496 Cache Controller bus cycle request accesses memory or I/O.

CM/IO# is high for 82496 Cache Controller initiated cycles (i.e., 82496 Cache Controller replacement write back, 82496 Cache Controller snoop write back, and allocation).

When Driven

CM/IO# is valid in the same CLK as CADS# and SNPADS# and remains active until CRDY# or CNA#. CM/IO# is undefined in other situations.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.37. CNA#

CNA#	Cache Next Address Enable
	Dynamically pipelines CADS# cycles.
	Input to 82496 Cache Controller (pin M05)
	Synchronous to CLK
	Internal Pull-up

Signal Description

CNA# is used by the MBC to dynamically pipeline CADS# cycles. If CNA# is asserted while a memory or I/O cycle is pending, CADS# is driven along with the address and attributes of the next memory or I/O cycle. The 82496 Cache Controller provides one level of pipelining.

CNA# is an optional input for all cycles initiated with CADS#.

When Sampled

CNA# is sampled beginning in the first CLK in which BGT# is sampled active and until CRDY# is sampled active. Subsequently, CNA# is ignored until BGT# is returned for the next cycle.

CNA# is ignored during snoop write-back cycles. CNA# is ignored before CDTS# is asserted by the 82496 Cache Controller.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	CNA# is recognized between BGT# and CRDY# in a given cycle.
CADS#	When the 82496 Cache Controller samples CNA# active, it issues CADS# as soon as possible for the next memory cycle to begin.
CDTS#	CNA# is recognized between CDTS# and CRDY#.
CFG0	CNA# shares a pin with the CFG0 configuration input.
CRDY#	CNA# is recognized between CDTS# and CRDY#.
	CNA# is recognized between BGT# and CRDY# in a given cycle.

5.2.2.38. CPCD

CPCD	Latched processor PCD pin
	A latched version of the Pentium processor PCD output signal.
	Output from 82496 Cache Controller (pin M01)
	Synchronous to CLK

Signal Description

CPCD reflects the Pentium processor PCD output signal during a CPU cycle on the memory bus. CPCD is inactive (LOW) during write-backs, snoop write-backs, and allocations.

CPCD can be used, along with CPWT, to distinguish between write hit to [S] state and write miss cycles. In all cases PALLC# will be inactive (high). See Table 5-3.

Table 5-3. Using CPCD and CPWT to Determine Write Hit to [S] versus Write Miss

CPCD	CPWT	Cycle Type
0	0	Write Hit to [S]
0	1	Cacheable Write Miss (Non Allocatable Write Through)
1	x	Non Cacheable Write Miss

When Driven

CPCD is valid from the CLK of CADS# and SNPADS# until the CLK of CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.39. CPWT

CPWT	Latched Pentium processor PWT pin
	A latched version of the Pentium processor PWT output signal.
	Output from 82496 Cache Controller (pin K01)
	Synchronous to CLK

Signal Description

CPWT reflects the Pentium processor PWT output signal during a CPU cycle on the memory bus. CPWT is inactive (LOW) during write-backs, snoop write-backs, and allocations. Write cycles with PWT active are not allocatable.

CPWT can be used, along with CPCD, to distinguish between write hit to [S] state and write miss cycles. In all cases PALLC# will be inactive (high). See Table 5-3.

When Driven

CPWT is valid from the CLK of CADS# and SNPADS# until the CLK of CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.40. CRDY#

CRDY#	Cache Ready
	Ends a 82496 Cache Controller/82491 Cache SRAM cache cycle.
	Input to 82496 Cache Controller (pin N03), and 82491 Cache SRAM (pin 43)
	Synchronous to CLK

Signal Description

CRDY# is used by the MBC to end a memory bus cycle. CRDY# indicates full completion of the cycle and allows the 82496 Cache Controller/82491 Cache SRAM to free internal resources for the next cycle. For example, the 82491 Cache SRAM CRDY# indicates that the memory buffer in use must be emptied (i.e. put in array or discarded). CRDY# also allows cycle progress signals (BGT#, KWEND#, SWEND#) to be sampled for the next cycle during pipelining.

CRDY# is required for all 82496 Cache Controller/82491 Cache SRAM memory bus cycles, including snoop-write back cycles.

When Sampled

CRDY# is always sampled by the 82496 Cache Controller and 82491 Cache SRAM, and should be asserted for one CLK only. CRDY# should be inactive except for the 1 CLK width assertion time for every outstanding memory bus cycle.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	CRDY# follows BGT#.
	CRDY# follows BGT# by three CLKs for line fill or allocation cycles.
BRDY#	CRDY# for a cycle N+1 must be sampled active after the last BRDY# for cycle N.
	CRDY# for cycle N can be before, with, or after the BRDY#(s) for that cycle.
CADS#	CRDY# is required for all memory bus cycles initiated by CADS#.
CDTS#	CRDY# follows CDTS#.
CNA#	CNA# is recognized between BGT#/CDTS# (the later of the two) and CRDY#.
KWEND#	CRDY# follows KWEND# for line fill or write-through cycles with potential allocation (PALLC#= 0).
MBRDY#	For read cycles, MBRDY# fills the memory buffer in use. CRDY# empties the current memory cycle buffer (read or write cycles) and makes it available for new cycles.
MEOC#	MEOC# for cycle N must be sampled with or before CRDY# for that cycle.
	MEOC# for cycle N+1 must be sampled at least one CLK after CRDY# for cycle N.
	CRDY# may be asserted with MEOC#, which may be asserted with the last MBRDY#.
SLFTST#	CRDY# shares a pin with the 82496 Cache Controller SLFTST# input.
SNPADS#	CRDY# is required for all memory bus cycles initiated by SNPADS#.
SWEND#	CRDY# activation represents only the end of the current cycle on the memory bus, and does not imply the closure of the snooping window (SWEND#).

5.2.2.41. CSCYC

CSCYC	Latched Pentium processor SCYC pin
	A latched version of the Pentium processor SCYC output signal.
	Output from 82496 Cache Controller (pin E01)
	Synchronous to CLK

Signal Description

CSCYC reflects the Pentium processor SCYC output signal during a CPU LOCKed cycle on the memory bus. CSCYC is inactive (LOW) during write-backs, snoop write-backs, and allocations.

When Driven

CSCYC is valid from the CLK of CADS# and SNPADS# until the CLK of CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.42. CW/R#

CW/R#	Cache Write/Read
	Indicates whether current cycle is write or read.
	Output from 82496 Cache Controller (pin F05)
	Synchronous to CLK

Signal Description

CW/R#, CD/C# and CM/IO# are 82496 Cache Controller cycle definition signals. CW/R# indicates whether the 82496 Cache Controller requests a read cycle or a write cycle.

When Driven

CW/R# is valid with CADS# and SNPADS# and remains valid until CRDY# or CNA# is asserted.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.43. CWAY

CWAY	Cache Way
	Indicates WAY used by the current cycle.
	Output from 82496 Cache Controller (pin K04)
	Synchronous to CLK

Signal Description

CWAY is a cycle definition signal which indicates to the MBC the WAY used by the requested cycle. During line fills, CWAY indicated the WAY in which the line is filled. During write-hits (to [S] state or LOCKed), CWAY indicates the WAY which was hit. During write-backs, CWAY indicates the WAY that was written back.

CWAY can be utilized by external tracking machines to maintain a set of duplicate tags that can accurately duplicate 82496 Cache Controller tags.

When Driven

CWAY is valid with CADS# and remains valid until CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.44. D/C#

D/C#	Data/Code
	Cycle decode signal.
	Output from Pentium processor (pin V04), Input to 82496 Cache Controller (pin J15)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.45. D[63:0]

D[63:0]	Pentium processor Data Pins
	CPU data bus pins.
	Input/Output between Pentium processor (pins H18, J19, K19, L19, H19, J18, F20, H21, G19, E20, G18, C21, F18, C20, F19, B21, B20, E18, A21, D21, A20, D20, B19, D14, D15, D19, D16, C18, D17, C19, C17, D10, C10, D12, C09, D11, D09, C11, C08, B10, A10, C07, C16, D07, C15, C06, B09, D06, D05, D13, D04, C14, E05, C13, C12, F04, G04, B04, G03, C04, F03, E04, E03, D03) and 82491 Cache SRAM CDATA[7:0] pins.
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

These pins are connected to the 82491 Cache SRAM CDATA[7:0] pins. The specific data pin connections are configuration dependent. Refer to the Configuration chapter for additional details.

5.2.2.46. DP[7:0]

DP[7:0]	Data Parity Pins
	CPU data bus Even Byte parity.
	Input/Output between Pentium processor (pins E21, E19, A19, D18, D08, A09, C05, H04) and 82491 Cache SRAM CDATA[3:0] pins.
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CDATA[3:0]	The Pentium processor Data parity signals are connected to the 82491 Cache SRAM CDATA[3:0] pins for 82491 Cache SRAMs configured to be data parity devices. Refer to section 5.1.6.5.

5.2.2.47. DRCTM#

DRCTM#	Memory Bus Direct to [M] State
	Signals 82496 Cache Controller to place cached line directly into [M] state.
	Input to 82496 Cache Controller (pin N02)
	Synchronous to CLK
	Internal Pull-up

Signal Description

DRCTM# is a memory bus input to the 82496 Cache Controller. When DRCTM# is sampled active at the end of the snooping window (while SWEND# is active), the 82496 Cache Controller moves the line being filled directly to the [M] state. Read-Only and Write-Through cycles will ignore DRCTM# since the only valid tag states are [I] and [S].

If MRO# is sampled active during KWEND#, or MWB/WT# is sampled Low during SWEND#, DRCTM# is ignored.

DRCTM# is used in three circumstances:

1. To *simplify external state tracking*. External tracking devices can only track [M], [S] and [I] states. The [E] state can not be tracked externally because cache write hits internally change [E] lines to the [M] state. DRCTM# can be used to eliminate the [E] state from the MESI protocol.

   NOTE

   Usage of DRCTM# to avoid [E] states may be in conflict with the SNPCNA cycle attribute. Snoops with SNPNCA may cause an [E] state transition. Usage of DRCTM# to avoid [E] states may also be in conflict with the SYNC operation. SYNC cycles move an [M] state line to [E]. Refer to Tables 3-4 and 3-6.

2. In *read for ownership*. During write misses with allocation, the MBC may keep write data in the 82491 Cache SRAM buffer rather than write it to memory. When the allocation is initiated, due to MFRZ# being sampled active during MEOC# of the write miss cycle, the read data fills the area surrounding the data from the write in the memory cycle buffer. Subsequently, the memory cycle buffer contents are written to the 82491 Cache SRAM array. The cache would normally tag this data in the [E] state because the cache assumes that the data was written to main memory. Because the data has been modified, DRCTM# must be asserted to the 82496 Cache Controller.

3. In *cache-to-cache transfers*. Here, one cache supplies modified data to another without updating main memory, providing the cache receiving the transfer with modified data. Since the MESI modified state [M] implies modified and exclusive, the supplying cache must invalidate its copy (using SNPINV) and the receiving cache must use DRCTM# to override the default [E] state. Otherwise, the MESI protocol would be violated for both caches.

When Sampled

DRCTM# is synchronous to CLK and is only sampled with SWEND# (at the end of the snooping window). At other times, DRCTM# is ignored and is not required to meet set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MRO#	If MRO# is sampled active during KWEND#, or MWB/WT# is sampled Low during SWEND#, DRCTM# is ignored.
MWB/WT#	DRCTM# and MWB/WT# (write policy) together define the memory bus attributes and are sampled on CLK at the end of the snooping window (when SWEND# is active).
	If MRO# is sampled active during KWEND#, or MWB/WT# is sampled Low during SWEND#, DRCTM# is ignored.
SWEND#	DRCTM# and MWB/WT# are sampled with SWEND#.

5.2.2.48. EADS#

EADS#	External CPU Address Strobe
	Indicates a valid external address is being driven.
	Output of 82496 Cache Controller (pin K16), Input to Pentium processor (pin M03)
	Synchronous to CLK

Signal Description

EADS# indicates that a valid external address has been driven onto the Pentium processor address pins by the 82496 Cache Controller. This address should be used to perform a Pentium processor internal cache invalidation (INV active) or inquire cycle.

When Sampled

EADS# is driven to the Pentium processor when the 82496 Cache Controller has the back-invalidation or inquire address ready on the CPU address bus.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CFA, SET, TAG, AP	When EADS# is driven active to the CPU, the CPU address is also valid (CFA, SET, TAG, AP).

5.2.2.49. EWBE#

EWBE#	External Write-Back Buffer Empty
	Indicates that a Pentium processor write cycle is pending in the second level cache.
	Output of 82496 Cache Controller (pin T03), Input to Pentium processor (pin A03)
	Synchronous to CLK

Signal Description

EWBE# inactive indicates that a write-through cycle is posted in the 82496 Cache Controller/82491 Cache SRAM cache.

When Sampled

EWBE# goes inactive (high) in the CLK following ADS# active for a write cycle, and goes active (low) when the posted write received BGT# from the MBC.

When the 82496 Cache Controller is configured in weak write ordering mode, EWBE# is always driven active by the 82496 Cache Controller.

Relation to Other Signals

None.

5.2.2.50. FERR#

FERR#	Floating Point Error
	Floating point error reporting.
	Output from Pentium processor (pin H03)
	Synchronous to CLK
	Glitch Free

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.51. FLUSH#

FLUSH#	Cache Flush
	Causes a Pentium processor and/or 82496 Cache Controller cache flush.
	Input to 82496 Cache Controller (pin P05), and Pentium processor (pin U02)
	Asynchronous
	82496 Cache Controller internal Pull-up

Signal Description

82496 Cache Controller FLUSH# invalidates the entire 82496 Cache Controller and Pentium processor tag arrays. Two clocks are required to lookup a tag entry if the result is a miss. The 82496 Cache Controller also invalidates tags in the CPU cache by executing inquire and back-invalidation cycles to the Pentium processor. All modified first and second-level cache lines will be written to memory.

There are two reasons for potentially wanting to assert the CPU FLUSH# in addition to the 82496 Cache Controller FLUSH#. One, if the MBC wants to see the processor flush acknowledge special cycle, and two, to assure that no Pentium processor cache hits are occurring once FLUSH# has been asserted to the 82496 Cache Controller. This is because the 82496 Cache Controller flush operation does not inhibit Pentium processor cache hit operations. For optimum performance, issue FLUSH# to only the 82496 Cache Controller.

When the MBC decodes a Pentium processor Flush (due to the INVD or WBINVD instructions) or Write Back (due to the WBINVD instruction) special cycle, it must provide FLUSH# to the 82496 Cache Controller. The 82496 Cache Controller/82491 Cache SRAM treats Flush and Write Back special cycles like I/O cycles. They are not posted, and the MBC must provide BRDY#. The WBINVD instruction causes the Pentium processor to issue the Flush special cycle followed by the Write Back special cycle.

The 82496 Cache Controller/82491 Cache SRAM second-level cache can be snooped during the flush operation. The snooping protocols are the same as with any memory bus cycle.

When Sampled

FLUSH# can be asserted at any time. The 82496 Cache Controller completes all outstanding transactions on the CPU and memory bus before beginning the flush operation (namely, all BRDY#s and CRDY#s have been provided for outstanding memory bus cycles). The memory bus controller does not have to prevent flushing during locked cycles because the 82496 Cache Controller completes locked transactions before the flush begins.

Once a flush has begun (FSIOUT# active), FLUSH# is ignored until the operation completes. If RESET is activated while the flush is in progress, the flush is aborted and RESET is executed immediately.

FLUSH# is an asynchronous input. FLUSH# must have a pulse width of at least two CLKs to ensure recognition by the 82496 Cache Controller.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
ADS#	To initiate a FLUSH, the 82496 Cache Controller completes all pending cycles and prevents the Pentium processor from issuing ADS# while the flush is in progress.
BRDY#	To insure that the Pentium processor will not generate an additional bus cycle (code prefetch or page table read) following the INVD or WBINVD instructions, the MBC must delay BRDY# to the 82496 Cache Controller/82491 Cache SRAM for the Flush and Write Back special cycles until it recognizes CAHOLD asserted. Having the MBC Wait to complete the CPU special cycles until the flush operation has been internally recognized by the 82496 Cache Controller insures that no additional CPU or 82496 Cache Controller cycles are generated. Note that the Pentium processor will not pipeline any cycle into a Flush or Write Back special cycle.
CADS#	Once FLUSH# has begun and FSIOUT# is active, all CADS# and CRDY# signals correspond to write-backs caused by the flush operation.
CAHOLD	See BRDY#.
CRDY#	Once FLUSH# has begun and FSIOUT# is active, all CADS# and CRDY# signals correspond to write-backs caused by the flush operation.
FSIOUT#	The FSIOUT# 82496 Cache Controller output is used to indicate the start and end of the flush. It is asserted when FLUSH# is internally recognized (all outstanding cycles have completed) and deasserted after the last line is invalidated. If the last line was a hit to [M], the FSIOUT# is deasserted after CRDY# of the write back.
	The 82496 Cache Controller flush operation is complete when FSIOUT# becomes inactive.
	FLUSH# is ignored while FSIOUT# is active for an initialization or a previous flush operation.
RESET	FLUSH# must be driven HIGH to the 82496 Cache Controller during RESET for proper Pentium processor/82496 Cache Controller operation.

5.2.2.52. FRCMC#

FRCMC#	Functional Redundancy Checking Mode
	Indicates either master or checker mode.
	Input to Pentium processor (pin M19)
	Asynchronous

Signal Description

When using the 82496 Cache Controller/82491 Cache SRAM second level cache, the Pentium processor must be configured as a Master Device. Therefore, FRCMC# must be tied HIGH.

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.53. FSIOUT#

FSIOUT#	Flush, Sync, Initialization
	Indicates beginning/end of Flush, Sync, Initialization (including self test) operations.
	Output from 82496 Cache Controller (pin E02)
	Synchronous to CLK

Signal Description

This signal indicates the start and the end of a flush, sync or initialization operations (including self-test, if requested). These operations are never active simultaneously. The signal is activated when one of the three operations begins, and goes inactive when the operation is complete.

FSIOUT# active indicates that either Flush, Sync or Initialization operation is in progress. Only one of these operations can take place at a time in the 82496 Cache Controller. Table 5-4 shows the priorities of these three operations.

Table 5-4. FSIOUT# Operation Priorities

Operation	Initiating Signal	Priority
Initialization	RESET	Highest
Flush	FLUSH#	
Sync	SYNC#	Lowest

If a signal of Higher priority is asserted while a lower priority operation is in progress, then the lower priority operation is aborted and the higher priority operation is executed. If a signal of lower priority is asserted when a higher priority operation is taking place, the lower priority signal is ignored. Once a FLUSH# or SYNC# operation has begun, its trigger signal is ignored until the operation completes.

When a higher priority operation aborts a lower priority one, FSIOUT# remains active.

When Driven

This signal is asserted whenever a flush, sync or initialization operation is internally recognized by the 82496 Cache Controller.

FSIOUT# remains asserted until the end of the flush, sync or initialization operation. It is deasserted after the last line is handled. If the last line is a hit to [M], then FSIOUT# is deasserted after the CRDY# of the write back.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
FLUSH# RESET SYNC#	Since RESET, FLUSH#, and SYNC# are all asynchronous, FSIOUT# is activated when the 82496 Cache Controller is actually executing the operation. For BIST, CAHOLD indicates the error results.

5.2.2.54. HIGHZ#

HIGHZ#	High Impedance
	Causes 82496 Cache Controller outputs to be tri-stated.
	Configuration Input to 82496 Cache Controller (pin Q05)
	Synchronous to CLK

Signal Description

If SLFTST# is active while HIGHZ# is inactive during RESET, the 82496 Cache Controller cache controller enters self-test. If SLFTST# and HIGHZ# are both sampled active during RESET, the 82496 Cache Controller floats all 82496 Cache Controller output and I/O signals until the next RESET. If SLFTST# is inactive, a normal initialization occurs. See Table 5-5.

Table 5-5. Actions Based on 82496 Cache Controller Configuration Test Inputs (HIGHZ# and SLFTST#)

HIGHZ#	SLFTST#	Action Taken by 82496 Cache Controller
1	0	Self-Test (BIST)
0	0	Outputs and I/O Floated (High-Z)
x	1	Normal Initialization (Reset)

When Sampled

HIGHZ# is sampled as shown in the Initialization and Configuration chapter. HIGHZ# is a "don't care" until the 82496 Cache Controller/82491 Cache SRAM RESET sequence completes with FSIOUT# going inactive, when it becomes the MBALE pin.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	HIGHZ# is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
SLFTST#	HIGHZ# and SLFTST# determine if either normal 82496 Cache Controller BIST is executed or tri-state test mode is entered.
MBALE	HIGHZ# shares a pin with MBALE. 82496 Cache Controller outputs and I/O signals are tri-stated when HIGHZ# and SLFTST# are both sampled active during RESET.

5.2.2.55. HIT#

HIT#	Hit to a CPU Cache Line
	Indicates a hit to a line in the Pentium processor data or code caches.
	Output from Pentium processor (pin W02)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.56. HITM#

HITM#	Hit to a Modified Line
	Indicates a hit to a Modified line in the Pentium processor data cache.
	Output from Pentium processor (pin M04), Input to 82496 Cache Controller (pin E18), Input to 82491 Cache SRAM (pin 62)
	Synchronous to CLK
	82491 Cache SRAM internal Pull-up

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.57. HLDA

HLDA	Pentium processor Hold Acknowledge
	Provides the Hold Acknowledge handshake from the CPU.
	Output from Pentium processor (pin Q03)
	Synchronous to CLK
	Glitch Free

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.58. HOLD

HOLD	Pentium processor Hold
	Provides the Hold handshake to the CPU.
	Input to Pentium processor (pin V05)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.59. IBT

IBT	Instruction Branch Taken
	Indicates that a branch was taken.
	Output from Pentium processor (pin T19)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.60. IERR#

IERR#	Internal Parity and Functional Redundancy Errors
	Indicates an internal Parity or Functional Redundancy error occurred.
	Output from Pentium processor (pin C02)
	Synchronous to CLK
	Glitch Free

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.61. IGNNE#

IGNNE#	Ignore Numeric Error
	Ignore floating-point error indication.
	Input to Pentium processor (pin S20)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.62. INIT

INIT	Initialization
	Forces the Pentium processor to begin execution at a known state.
	Input to Pentium processor (pin T20)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.63. INTR

INTR	Maskable Interrupt
	Maskable interrupt request to the Pentium processor.
	Input to Pentium processor (pin N18)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.64. INV

INV	Pentium processor Cache Invalidation Request
	Indicates a request to invalidate the CPU cache line.
	Output from 82496 Cache Controller (pin L16), Input to Pentium processor (pin A01)
	Synchronous to CLK

Signal Description

INV is a 82496 Cache Controller output which indicates a request to force the Pentium processor cache line to an invalid state if the inquire or back-invalidation hits the first level cache.

INV is driven active to the CPU when SNPINV is sampled active by the 82496 Cache Controller and during replacements of modified lines in the 82496 Cache Controller/82491 Cache SRAM cache (for example, when a replacement occurs as a result of a linefill).

When Driven

INV is driven to a valid level by the 82496 Cache Controller in the same CLK as EADS# and is a "don't care" at all other times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
EADS#	INV is driven with EADS# to the CPU.

5.2.2.65. IPERR#

IPERR#	Internal Parity Error
	Indicates that a TagRAM or address path parity error occurred.
	Output from 82496 Cache Controller (pin Q01)
	Synchronous to CLK
	Glitch Free

Signal Description

IPERR# is driven active for 82496 Cache Controller TagRAM parity errors, and for internal address path parity errors.

Each TagRAM "set" has 41 memory bits: 20 bits for way "0" (15 bits for the tag, 4 for the line status, and one Read-Only bit), 20 bits for way "1", and one LRU bit. Two parity bits are associated with each TagRAM set. One parity bit represents the parity information for way "0" and the other for way "1". Each parity bit is stored adjacent to the 20 bits of the way it represents (the LRU bit is not covered).

In every lookup cycle, the whole "set" will be read, including the two parity bits. The parity check will be done outside the TagRAM by regenerating the parity and comparing it to the read parity bits. In case of an error, the IPERR# signal will be activated.

The parity bits are written in every TagRAM cycle which causes "set" data modification. Since many of the cycles do partial updates (e.g. a snoop which modifies only the line status, or a write to E which causes a state transition to M), the 82496 Cache Controller will perform a Read-Modify-Write cycle to write the parity.

When Driven

IPERR# is always valid and stays active for a minimum of 1 CPU CLK. If internal parity error checking is desired, IPERR# should always be monitored by the MBC. Since internal parity can be affected by data path errors as well as internal lookups, this internal parity is always valid.

IPERR# is inactive during RESET.

Relation to Other Signals

None.

5.2.2.66. IU

IU	U-Pipeline Instruction
	Indicates completion of an instruction in the U-pipeline.
	Output from Pentium processor (pin J02)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.67. IV

IV	V-Pipeline Instruction
	Indicates completion of an instruction in the V-pipeline.
	Output from Pentium processor (pin B01)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.68. KEN#

KEN#	Cache Enable
	Indicates the cacheability of the cycle to the CPU.
	Output from 82496 Cache Controller (pin E17), Input to Pentium processor (pin J03)
	Synchronous to CLK

Signal Description

This is the cache enable pin. It is used to indicate to the Pentium processor that the current cycle is cacheable or not. KEN# is an output of the 82496 Cache Controller and is connected to the Pentium processor KEN# input. KEN# is normally active and will be deactivated as a function of MKEN# (memory bus cacheability), MRO# (memory bus read only), and D/C# (data or code). KEN# is also determined by the values of CACHE# and LOCK# from the CPU.

When Driven

KEN# is valid with either NA# or the first BRDY# of the cycle (whichever comes first).

Table 5-6 summarizes the cases when KEN# is active and inactive.

Table 5-6. KEN# Operation

Cycle Type	KEN#	Note
Locked cycles	1	3
I/O	x	
Memory Write	x	
Pentium™ processor Non-Cacheable (CACHE#=1) cycles	1	3
Non Cacheable Read Miss	x	
Cacheable Code Read Miss	0	1
Cacheable Code Read Hit	0	
Cacheable Data Read Miss (MRO# sampled inactive)	0	1
Cacheable Data Read Miss (MRO# sampled active)	1	1
Cacheable Data Read Hit (TRO inactive)	0	2
Cacheable Data Read Hit (TRO active)	1	2

NOTES:

1. MKEN# sampled active. If MKEN# is sampled inactive, KEN# will be driven inactive for all cases.
2. TRO = 82496 Cache Controller tagRAM Read Only bit.
3. KEN# will be returned inactive for any cycle in which the 82496 Cache Controller samples CACHE# inactive (i.e. locked and Pentium processor non-cacheable cycles)

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CACHE#	KEN# is driven inactive during cycles in which the 82496 Cache Controller samples CACHE# inactive.
D/C#	KEN# is driven inactive during data (D/C#=1) read cycles with MRO# sampled active.
BRDYC#	KEN# is valid with either NA# or the first BRDY# of the cycle (whichever comes first).
LOCK#	KEN# is always driven inactive during locked cycles.
MKEN#	If MKEN# is sampled inactive by the 82496 Cache Controller, the KEN# will be driven inactive to the CPU.
MRO#	KEN# is driven inactive during data read cycles with MRO# sampled active.
NA#	KEN# is valid with either NA# or the first BRDY# of the cycle (whichever comes first)

5.2.2.69. KLOCK#

KLOCK#	82496 Cache Controller LOCK#
	Request for LOCKed cycle.
	Output from 82496 Cache Controller (pin D04)
	Synchronous to CLK
	Glitch Free

Signal Description

KLOCK# indicates an 82496 Cache Controller request for the MBC to execute a locked cycle. KLOCK# follows the CPU LOCK# request.

KLOCK# is simply a one-CLK flow-through version of the CPU LOCK# signal if the Memory Bus is free. The 82496 Cache Controller activates KLOCK# with CADS# of the first cycle of a LOCKed operation and remains active through CADS# of the last cycle of the LOCKed operation (i.e. the write of a processor read-modify-write sequence) (see Figure 5-26).

Unlike the Intel486 DX CPU, the Pentium processor automatically inserts at least one idle clock between two consecutive locked operations to allow the LOCK# and KLOCK# signals to be sampled inactive by the 82496 Cache Controller and MBC respectively.

KLOCK# activation is not qualified by the tag array look-up (hit/miss indications). As a result, KLOCK# may be active before CADS# is asserted.

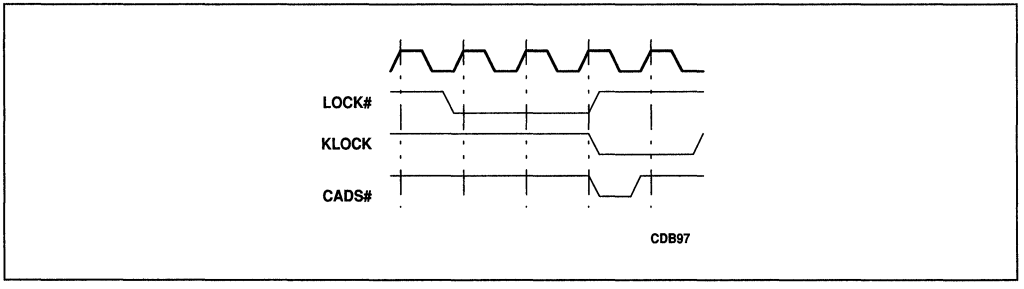


Figure 5-26. KLOCK# to LOCK# Relationship

When Driven

KLOCK# is asserted with CADS# for cycles in which LOCK# was asserted by the Pentium processor with ADS#. KLOCK# de-assertion is a flow-through of one CLK from the CPU LOCK# signal and occurs at least one CLK after the last CADS# in a LOCKed sequence.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.70. KWEND#

KWEND#	Cacheability Window End
	Closes the 82496 Cache Controller cacheability window.
	Input to 82496 Cache Controller (pin N05)
	Synchronous to CLK
	Internal Pull-up

Signal Description

KWEND# is a cycle progress input which closes the cacheability window opened with CADS#, and causes the MKEN# and MRO# cacheability attributes to be sampled.

KWEND# should be asserted by the MBC once the memory address has been decoded and MKEN# (cacheability) and MRO# (read-only) attributes have been determined.

Resolving KWEND# quickly allows the non-snoopable window between BGT# and SWEND# to be closed more quickly. KWEND# activation also allows the 82496 Cache Controller to start allocations and begin replacements.

When Sampled

KWEND# is sampled by the 82496 Cache Controller on the CLK in which BGT# is sampled active or on the following CLKs. Once KWEND# is sampled active, it is not sampled again until BGT# of the next cycle.

BGT#, KWEND# and SWEND# may be asserted on the same CLK edge.

KWEND# need only be activated for cycles requiring MKEN# and MRO# to be sampled (i.e. cacheable read misses and write cycles with potential allocate).

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	KWEND# is sampled on or after BGT# assertion.
BRDY#	KWEND# must be asserted at least 1 CLK before the first BRDY# for those cycles in which the CPU samples KEN#. (KWEND# < FBRDY#).
	BRDY# of a non-cacheable 82496 Cache Controller cycles (MKEN# returned inactive) which is cacheable by the Pentium processor (active CACHE#), must be issued after KWEND# (at which time KEN# is valid).
CFG2	KWEND# shares a pin with CFG2.
CRDY#	Cycle progress implication rules specify that CRDY# must be asserted for at least one CLK after KWEND# for cacheable read misses and write-through cycles with potential allocate.
MKEN#	When KWEND# is activated, MKEN# and MRO# are sampled.
MRO#	When KWEND# is activated, MKEN# and MRO# are sampled.
SWEND#	KWEND# allows SWEND# to be sampled. SWEND# is sampled by the 82496 Cache Controller in the clock in which KWEND# is asserted, and in subsequent clocks.

5.2.2.71. LOCK#

LOCK#	Cycle lock
	Indicates that the current bus cycle is locked.
	Output from Pentium processor (pin V03), Input to 82496 Cache Controller (pin C17)
	Synchronous to CLK
	Glitch Free

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.72. LR[1:0]

LR[1:0]	Line Ratio Pins
	Indicates the line ratio configuration information.
	Configuration Outputs from 82496 Cache Controller (pins N16, P16), Inputs to 82491 Cache SRAM (pins 39, 37)
	Synchronous to CLK

Signal Description

The LR[1:0] signals indicate to the 82491 Cache SRAM which line ratio has been selected by the MBC. Table 5-7 shows the line ratios selected by LR[1:0]. LR[1:0] are driven by the 82496 Cache Controller to the 82491 Cache SRAM during RESET.

Table 5-7. 82491 Cache SRAM Line Ratio Configuration with LR[1:0]

LR1	LR0	Line Ratio
0	0	1
0	1	2
1	0	4

Relation to Other Signals

Pin Symbol	Relation to Other Signals
WBTYP	LR0 shares pins with the 82496 Cache Controller WBTYP output and the 82491 Cache SRAM WBTYP input signals.
WBWE#	LR1 shares pins with the 82496 Cache Controller WBWE# output and the 82491 Cache SRAM WBWE# input signals.

5.2.2.73. M/IO#

M/IO#	Memory or I/O
	Indicates that the current cycle is either memory or I/O.
	Output from Pentium processor (pin A02), Input to 82496 Cache Controller (pin G17)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.74. MALDRV

MALDRV	Memory Address Low Drive
	Selects the low-capacitance address drivers.
	Configuration input to 82496 Cache Controller (pin R05)
	Synchronous to CLK

Signal Description

The 82496 Cache Controller memory bus address signals, MCFA[6:0], MSET[10:0], MTAG[11:0], and MAP can be configured for one of two buffers. The buffer selection depends upon the load on these signals and should be based on simulation results of these signals driving that load. The 82496 Cache Controller configuration input, MALDRV, is used to select the buffer. Refer to Table 7-14 for the buffer selection specifications, and the appropriate value of MALDRV.

When Sampled

MALDRV is sampled as shown in the Initialization and Configuration Chapter. MALDRV becomes the SYNC# input after RESET goes inactive.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	MALDRV is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
SYNC#	MALDRV shares a pin with SYNC#.

5.2.2.75. MALE

MALE	Memory Address Latch Enable
	Enables memory address outputs.
	Input to 82496 Cache Controller (pin R03)
	Asynchronous

Signal Description

The 82496 Cache Controller contains an address latch which controls the last stage of the memory address output from the 82496 Cache Controller. The latch is controlled by four signals: MAOE#, MBAOE#, MALE and MBALE. MALE and MBALE control address latching: MBALE controls the sub-line (burst) portion, and MALE controls the remainder. Refer to Table 4-3 in section 4.2.7 for a table (by cache size) showing which memory bus address signals are controlled by the MALE input.

MALE enables the MBC to control when a subsequent pipelined address is driven. When MALE is HIGH, the 82496 Cache Controller address latch is in flow-through mode, and the 82496 Cache Controller address is available on the memory bus. Any new address issued by the 82496 Cache Controller will immediately appear at the memory bus. When MALE is driven low, the address at the input of the latch is latched. Any subsequent address driven by the 82496 Cache Controller internally is not seen at the memory bus outputs until MALE is driven HIGH again.

MALE controls address latching and address parity latching (i.e., MAP) regardless of the state of MAOE#. When inactive, MAOE# tri-states the memory address bus, and MALE functions independently of MAOE#.

When Sampled

MALE is asynchronous and can be asserted or de-asserted at any time. MALE should always be driven to a valid state because it directly controls address latch operation.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MAOE#/MBAOE#	MAOE# and MBAOE# do not affect the operation of MALE or MBALE.
MAP	MALE controls the latch enable of the memory bus line address parity (MAP) input.
MBALE	MALE and MBALE together control latching of the entire 82496 Cache Controller memory address output.
WWOR#	MALE shares a pin with the WWOR# configuration pin.

5.2.2.76. MAOE#

MAOE#	Memory Address Output Enable
	Tri-states or enables memory address outputs.
	Input to 82496 Cache Controller (pin T05)
	Asynchronous except during snoop cycles (See SNPSTB#)

Signal Description

The 82496 Cache Controller address latch is controlled by a latch enable input, MALE, and an output enable input, MAOE#. MAOE# has two main functions. First, driving MAOE# active enables the 82496 Cache Controller to drive the 82496 Cache Controller address lines (MSET, MTAG, MCFA, MAP). Refer to Table 4-3 in section 4.2.7 for a table (by cache size) showing which memory bus address signals are controlled by the MAOE# input. Second, MAOE# is a qualifier for snoop cycles and must be inactive for a snoop request to be recognized by the 82496 Cache Controller.

In general, MAOE# should be active if the 82496 Cache Controller is the current bus master. When an 82496 Cache Controller gives up the bus, MAOE# should be inactive to float the address lines and allow another bus master to generate a snoop request.

MAOE# controls the 82496 Cache Controller address output, except for the sub-line portion, which has a separate output control (MBAOE#). MAOE# also provides the output enable for the memory line address parity (MAP) latch.

When Sampled

MAOE# is an asynchronous input (except during snoop cycles) and always has full control over the address output. For this reason, MAOE# must always be driven to a valid state.

The 82496 Cache Controller samples MAOE# to qualify snoop cycles. If MAOE# is sampled active, the snoop is ignored. This allows SNPSTB# to share a common line for multiple C5Cs.

In synchronous snoop mode, MAOE# is sampled on the rising edge of the first CLK in which SNPSTB# becomes active. In clocked mode, MAOE# is sampled on the rising edge of the first SNPCLK in which SNPSTB# becomes active. In strobed mode, MAOE# is sampled on the falling edge of SNPSTB#.

MAOE# is only sampled with SNPSTB#. SNPSTB# may be qualified by CLK, SNPCLK, or the falling edge of SNPSTB#, depending on the snoop mode, and must meet set-up and hold times to the edge being sampled. When SNPSTB# is not asserted, MAOE# is a "don't care" signal and is not required to meet set-up and hold times.

MAOE# need not meet any set-up or hold time if it is not being sampled during a snoop cycle.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MALE MAP	MALE and MAOE# together provide full control over the 82496 Cache Controller line address output latch and the memory bus address parity (MAP) latch.
MBAOE#	MAOE# and MBAOE# together control the entire 82496 Cache Controller memory bus address.
SNPSTB#	If MAOE# is active when SNPSTB# is asserted, the snoop request is ignored by the 82496 Cache Controller.

5.2.2.77. MAP

MAP	Memory Bus Address Parity
	Indicates Even Memory Bus address parity.
	Input when MAOE#=1, Output when MAOE#=0 to/from 82496 Cache Controller (pin U08)
	Input synchronous to CLK, SNPCLK or SNPSTB#; Output synchronous to CLK, MAOE# active and MALE high.

Signal Description

MAP indicates the address parity of the 82496 Cache Controller line address bits (i.e., MSET, MTAG, MCFA). During snoop cycles, MAP is driven by the MBC and indicates the line address parity for the snooped address.

When Sampled/Driven

MAP is driven by the 82496 Cache Controller on all 82496 Cache Controller initiated cycles (i.e., when MAOE# is active).

In synchronous snoop mode, MAP is sampled on the rising edge of the first CLK in which SNPSTB# becomes active. In clocked mode, MAP is sampled on the rising edge of the first SNPCLK in which SNPSTB# becomes active. In strobed mode, MAP is sampled on the falling edge of SNPSTB#.

MAP is only sampled with SNPSTB# activation. When SNPSTB# is not asserted, MAP is a "don't care" signal and is not required to meet set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
MALE	MALE and MAOE# together provide full control over the 82496 Cache Controller line address output latch and the memory bus address parity (MAP) latch. MALE controls the latch enable of the memory bus line address parity input.
MAOE#	MALE and MAOE# together provide full control over the 82496 Cache Controller line address output latch and the memory bus address parity (MAP) latch. MAOE# provides the output enable for the memory line address parity latch.
	MAP is an input when MAOE# is high, and an output when MAOE# is low.
MAPERR#	MAPERR# is driven active only after a wrong line address parity is driven to the 82496 Cache Controller on the MAP input during a snoop cycle.
SNPSTB#	MAP is sampled with SNPSTB# activation.

5.2.2.78. MAPERR#

MAPERR#	Memory Address Bus Parity Error
	Indicates that a memory address bus parity error occurred.
	Output from 82496 Cache Controller (pin U01)
	Synchronous to CLK
	Glitch Free

Signal Description

MAPERR# is driven active during 82496 Cache Controller snoop cycles whenever there is a memory address bus parity error (e.g. MAP doesn't match the even parity of the 82496 Cache Controller line address being snooped).

When Driven

MAPERR# will be inactive (HIGH) from the first CLK after the falling edge of RESET. MAPERR# will remain inactive until 1 CLK after initialization or self-test is finished (FSIOUT# goes inactive). During initialization and self-test, the 82496 Cache Controller does not perform address parity check when SNPSTB# is issued.

In synchronous snoop mode, MAPERR# is driven to a valid level (either active or inactive) two CLKs after SNPSTB#, and will remain valid until one CLK after the next SNPSTB#. In asynchronous snoop mode, (e.g. clocked and strobed), MAPERR# is driven to a valid level (either active or inactive) one CLK after SNPCYC#, and will remain valid until the CLK of the next SNPCYC#. Refer to Figures 5-17 and 5-18 in section 5.1.3.2.

MAPERR# is inactive during RESET, and remains inactive until at least 5 CLKs after RESET goes inactive.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MAP	MAPERR# is driven active only after a wrong line address parity is driven to the 82496 Cache Controller on the MAP input during a snoop cycle.

5.2.2.79. MAWEA#

MAWEA#	Memory Bus Array Write Enable or Allocation
	Indicates that the data should be written or an allocation should occur.
	Output from 82496 Cache Controller (pin R18), Input to 82491 Cache SRAM (pin 41)
	Synchronous to CLK

Signal Description

During read cycles, MAWEA# indicates to the 82491 Cache SRAM that data supplied from memory should be written to the array one CLK after CRDY# (the linefill will be executed then). During write cycles, MAWEA# indicates that the 82491 Cache SRAM should schedule an allocation cycle following the current write cycle. The data will be written to the 82491 Cache SRAM array one CLK after the CRDY# of the allocation. MAWEA# is active 1 CLK after KWEND# for cacheable read miss cycles or write through with potential allocation cycles.

Relation to Other Signals

None.

5.2.2.80. MBALE

MBALE	Memory Subline Address Latch Enable
	Enables memory subline address outputs.
	Input to 82496 Cache Controller (pin Q05)
	Asynchronous

Signal Description

The 82496 Cache Controller's memory bus address latch is controlled by four signals: MAOE#, MBAOE#, MALE and MBALE. MALE and MBALE control latching of the entire 82496 Cache Controller address. MBALE controls the sub-line (burst) portion while MALE controls the remainder. Refer to Table 4-3 in section 4.2.7 for a table (by cache size) showing which memory bus address signals are controlled by the MBALE input.

MALE and MBALE provide the MBC with complete flexibility while the next address is driven. When MBALE is HIGH, the sub-line portion of the 82496 Cache Controller address latch is in flow-through mode, and the 82496 Cache Controller sub-line address is available at the memory bus. Changes in the 82496 Cache Controller sub-line address will immediately appear at the memory bus. When MBALE is driven low, the sub-line address at the latch input is latched. Any subsequent sub-line address driven by the 82496 Cache Controller is not seen at the memory bus outputs until MBALE is driven HIGH again.

MBALE latches addresses regardless of the state of MAOE# or MBAOE#. If MBAOE# is inactive, MBALE operates the latch properly, but the sub-line portion of the memory bus is placed in the high-impedance state.

Separate line and sub-line address latch controls are provided so that latch outputs may be driven at different times.

When Sampled

MBALE is asynchronous and can be asserted and de-asserted at any time. MBALE should always be driven to a valid state because it directly controls the operation of the address latch.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
HIGHZ#	MBALE shares a pin with the HIGHZ# configuration pin.
MALE	MALE and MBALE together control latching for the entire 82496 Cache Controller memory output address.
MAOE#/MBAOE#	MAOE# and MBAOE# do not affect the operation of MALE or MBALE.

5.2.2.81. MBAOE#

MBAOE#	Memory Subline Address Output Enable
	Tri-states/enables memory sub-line address outputs.
	Input to 82496 Cache Controller (pin Q07)
	Asynchronous except during snoop cycles (See SNPSTB#)

Signal Description

The 82496 Cache Controller memory bus address latch is controlled by four signals: MAOE#, MBAOE#, MALE, and MBALE. MAOE# and MBAOE# are output enables for the entire memory bus address. MBAOE# controls the sub-line portion of the address and MAOE# controls the line address output enable. Refer to Table 4-3 in section 4.2.7 for a table (by cache size) showing which memory bus address signals are controlled by the MBAOE# input.

MBAOE# has two functions. First, it can tri-state the sub-line portion of the address separately from the rest of the address. Because the 82496 Cache Controller does not sequence through burst addresses, the memory system can provide the burst sub-line addresses, by tri-stating the sub-line address output from the 82496 Cache Controller after the first transfer.

Second, MBAOE# is sampled during snoop cycles. If MBAOE# is sampled inactive, any snoop write-back cycle begins at the sub-line address provided. If MBAOE# is sampled active, the snoop write-back begins at sub-line address 0. This allows snoop write-backs to begin at 0 or at the snooped sub-line address and progress through the normal burst order. Note that MBAOE# controls whether the address driven during a snoop writeback is the snooped address. MZBT# controls the order of the data driven during a snoop writeback. If MBAOE# is 1, the address driven is exactly the snooped address. If MBAOE# is 0, the address driven is the cache controller line address of the line that includes the snoop information.

When Sampled

Like MAOE#, MBAOE# is asynchronous except during snoop cycles and can be asserted or de-asserted at any time. Since MBAOE# has direct control over the address latch, it must always be driven to a valid state.

In synchronous snoop mode, MBAOE# is sampled on the rising edge of the first CLK in which SNPSTB# becomes active. In clocked mode, MBAOE# is sampled on the rising edge of the first SNPCLK in which SNPSTB# becomes active. In strobed mode, MBAOE# is sampled on the falling edge of SNPSTB#.

MBAOE# is only sampled with SNPSTB# activation. When SNPSTB# is not asserted, MBAOE# is a "don't care" signal and is not required to meet set-up and hold times.

If MBAOE# is not being sampled for a snoop (i.e. if SNPSTB# is not asserted), MBAOE# need not meet set-up or hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MALE MBALE	The 82496 Cache Controller memory bus address latch is completely controlled by MALE, MBALE, MAOE# and MBAOE#.
MAOE#	MAOE# and MBAOE# together control the entire 82496 Cache Controller memory bus address.
SNPSTB#	MBAOE# is sampled with SNPSTB# activation.

5.2.2.82. MBE#

MBE#	Memory Byte Enable
	A latched version of the Pentium processor BE[7:0]# output signals.
	Output from 82491 Cache SRAM (pin 32)
	Synchronous to CLK
	Internal Pull-up

Signal Description

The 82491 Cache SRAM includes an on-chip memory byte enable latch that replaces what used to be a discrete component on Intel486 DX CPU-Cache Module and Chip Set. This latch samples the Pentium processor BE# input and passes it as an MBE# (memory byte enable) output to the bus controller.

The byte enable latching is controlled by a 82491 Cache SRAM input, BLEC#, from the 82496 Cache Controller. The latch samples BE# at each clock rising edge when BLEC# is low. When BLEC# is high, the latch is closed and MBE# [PAR#] is driven to the corresponding CPU BE[7:0]# level.

The MBE# output is shared with the PAR# pin and is operative following reset. For a device configured in PARITY mode at reset time, the MBE# output function is tri-stated (PAR# is strapped low).

MBE# is not valid during 82496 Cache Controller replacement write back, snoop write back, and allocation cycles. The MBC must regard all CPU byte enables as active during these cycles.

For a 512-Kbyte cache size design (16 data 82491 Cache SRAM devices), the MBC needs to use only 8 of the 82491 Cache SRAMs to pass CPU byte enable information to the memory system. The remaining MBE# outputs may remain disconnected.

When Driven

On the first memory bus cycle following reset deassertion, MBE# is valid with CADS#. Figure 5-27 illustrates MBE# [PAR#] timing after RESET.

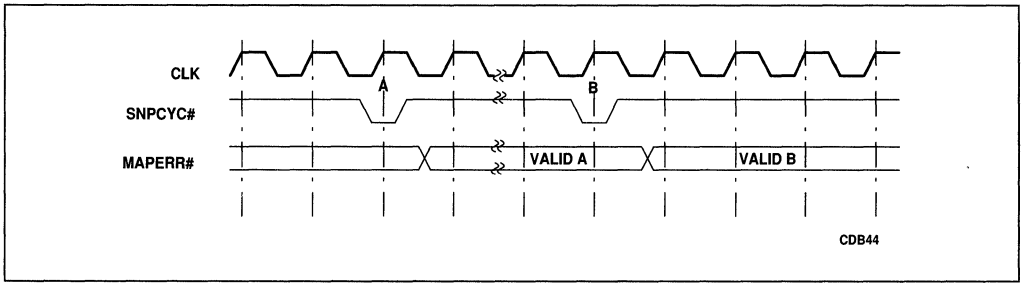


Figure 5-27. MBE# [PAR#] Timing After RESET

If there is no cycle active on the memory bus, the 82496 Cache Controller is able to drive BLEC# inactive in the CLK after ADS# (of a cache miss cycle). In this case, the 82491 Cache SRAM MBE# outputs will be active with the CADS# of the memory bus cycle. Refer to Figure 5-23 (in the BLEC# pin description).

When an ADS# (for a cache miss cycle) has been issued by the CPU, but not yet handled by the 82496 Cache Controller because the memory bus is busy, the 82496 Cache Controller will assert BLEC# for one CLK following CNA# or CRDY# assertion. In this case, the 82491 Cache SRAM MBE# outputs will be valid one CLK after the CADS# of the memory bus cycle. Refer to Figure 5-24 (in the BLEC# pin description).

If a cycle hits in the 82496 Cache Controller tagRAM, then BLEC# will go inactive for one CLK, latching the CPU byte enables for one CLK. These are unnecessary since the cycle does not get issued on the memory bus (i.e., no CADS# is generated). Refer to Figure 5-25 (in the BLEC# pin description).

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
PAR#	MBE# shares a pin with PAR#.

5.2.2.83. MBRDY#

MBRDY#	Memory Burst Ready
	Burst ready input to the memory buffers.
	Input to 82491 Cache SRAM (pin 22)
	Synchronous to MCLK

Signal Description

In clocked memory bus mode, MBRDY# is used with MSEL# active to advance the memory burst address counter of the memory buffer in use. As a result, new data is latched from the memory bus (read cycle) or new data is driven from the 82491 Cache SRAM memory cycle buffer (write cycle). MBRDY# is sampled on all MCLK edges in which MSEL# is sampled active and has no relation to CLK. In strobed mode, MISTB/MOSTB strobes data into and out of the 82496 Cache Controller/82491 Cache SRAM.

For write cycles, the first piece of write data is available at the MDATA bus pins. MBRDY# assertion with MSEL# active causes the next 64- or 128-bit slice of write data to be available. If only one slice is required to be read or driven, MSEL# and MBRDY# need not go active.

For read cycles, the first piece of read data flows through to the CPU (if no MZBT#). MBRDY# assertion with MSEL# activation causes the next slice of memory data to be latched in the memory buffer. The assertion of BRDY# allows this data to be available on the CPU bus and latches the previous doubleword into the CPU. For cacheable cycles, MBRDY# must be asserted four or eight times, depending on cache configuration. MEOC# can replace the last MBRDY# to latch the last slice of data into the 82491 Cache SRAM buffer. MBRDY# causes the memory burst counter to be incremented. MEOC# resets the memory burst counter.

When Sampled

MBRDY# is sampled on all MCLK edges in which MSEL# is sampled active. In this way, MSEL# qualifies the MBRDY# input. If MSEL# is sampled inactive, MBRDY# need not follow MCLK set-up and hold times.

Once the maximum number of MBRDY# signals have been asserted to the 82491 Cache SRAM, MBRDY# is ignored.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	The first MBRDY# must come after CADS# assertion.
MSEL#	MBRDY# is qualified by the MSEL# input. When MSEL# is active, MBRDY# advances the memory burst counter for the memory buffer in use to input or output data through the memory data bus pins.
MEOC#	MEOC# switches the buffers to the next pending cycle, and the last MBRDY# must come before or on the CLK of MEOC# assertion. MEOC# can replace the last MBRDY# to latch the last slice of data into the 82491 Cache SRAM buffer.
	The last MBRDY# must come before or on the CLK of MEOC# assertion.
MISTB	MBRDY# shares a pin with the memory bus input strobe, MISTB.

5.2.2.84. MBT[3:0]

MBT[3:0]	Memory Branch Trace Address bits
	Provides bits 0-2 of the branch target linear address and the default operand size during a Branch Trace Message Special Cycle.
	Output from 82496 Cache Controller (pins: U10, U12, U14, U16)
	Synchronous to CLK

Signal Description

The Memory bus branch trace pins, MBT[3:0], echo the Pentium processor bus branch trace pins. They provide bits 0-2 of the branch target linear address and the default operand size during a Branch Trace Message Special Cycle to the Memory Bus Controller.

MBT0: Pentium processor Address bit A0 of the branch target linear address

MBT1: Pentium processor Address bit A1 of the branch target linear address

MBT2: Pentium processor Address bit A2 of the branch target linear address

MBT3: Driven high if the default operand size is 32 bits
Driven low if the default operand size is 16 bits

The Branch Trace Message Special Cycle is part of the Pentium processor execution tracing protocol. If the execution tracing enable bit (bit 1) in TR12 is set to 1, a branch trace message special cycle will be driven each time IBT is asserted (i.e., whenever a branch is taken).

When Driven

The MBT[3:0] outputs are driven to their valid levels with the CADS# of a branch trace message special cycle. These outputs remain valid until CAHOLD is asserted or the clock after the earlier of CNA# or CRDY#.

During normal operation, the 82496 Cache Controller MBT[3:0] pins may be left unconnected or connected to the memory bus.

If the MBT[3:0] pins are connected between the memory bus and the 82496 Cache Controller, the MBC must always drive MBT[3:0] low during inquire and back-invalidation cycles.

If the MBT[3:0] pins are left unconnected between the 82496 Cache Controller and the memory bus, external pull-downs must be connected to the MBT[3.0] pins of the 82496 Cache Controller.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
BT[3:0]	The MBT[3:0] outputs of the cache controller reflect the BT[3:0] inputs during Branch Trace Message Special Cycles.
IBT (Pentium processor signal)	If TR12.TR (bit 1 in Test Register 12 of Pentium processor) is set to 1, MBT[3:0] are driven along with the branch trace message special cycle for each assertion of IBT.

5.2.2.85. MCACHE#

MCACHE#	Internal Cacheability of Second-Level Cache
	Indicates cycle cacheability attribute and cycle length.
	Output from 82496 Cache Controller (pin D03)
	Synchronous to CLK

Signal Description

MCACHE# is driven by the 82496 Cache Controller to indicate that the current cycle may be cached. Data cacheability is determined later in the cycle by MKEN# assertion. MCACHE# is asserted during allocation, replacement write back cycles, snoop write back cycles, and cacheable read-miss cycles (i.e. read-miss cycles in which PCD and LOCK# are not asserted). MCACHE# is not asserted for I/O, special or locked cycles (see Table 5-8).

Table 5-8. MCACHE# Status versus Cycle Type

Cycle Type	MCACHE#
Posted Writes	1
Replacement Write Backs	0
Snoop Write Backs	0
Read, PCD=0	0
Read, PCD=1	1
Allocation	0
I/O Cycles	1
Locked Cycles	1

Note that MCACHE# does not imply CPU cacheability. The MBC must use the CCACHE# signal to determine Pentium processor cacheability.

When Driven

MCACHE# is valid in the CLK of CADS# and SNPADS#, and remains valid until either CRDY# or CNA# are asserted.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.86. MCFA[6:0], MSET[10:0], MTAG[11:0]

MCFA[6:0]	Memory Address Bus
MSET[10:0]	Memory address bus pins.
MTAG[11:0]	Input/Output between Memory Bus and 82496 Cache Controller (pins Q14, Q15, Q16, R07, S05, P15, R17, R12, R13, Q11, T18, S18, R14, S17, R15, Q12, Q13, R16, Q08, R08, T17, Q09, T16, T15, S16, R09, S15, R10, Q10, R11)
	Input synchronous to CLK, SNPCLK or SNPSTB#; Output synchronous to CLK, MAOE# active and MALE high.

Signal Description

MSET, MTAG, MCFA comprise the 82496 Cache Controller cache memory address bus. They pass through an output latch on the 82496 Cache Controller which can be controlled by the MBC using the signals MALE, MBALE, MAOE# and MBAOE#. MBALE and MALE are the address latch enables for the sub-line address portion and the line address portion, respectively. MBAOE# and MAOE# are the address latch output enables for the sub-line address and the line address portions of the address respectively.

When MAOE# and MBAOE# are active, MSET, MTAG, MCFA are driven by the 82496 Cache Controller cache. MSET, MTAG, MCFA are valid at the start of a memory bus cycle at the input of the address latch in the 82496 Cache Controller. If MALE and MBALE are HIGH (flow-through) and MAOE# and MBAOE# are active (outputs enabled), the address is driven to the memory bus with CADS# and SNPADS#.

If a new cycle starts and MALE and MBALE are low, and MAOE# and MBAOE# are also low, the previous address remains valid on the address pins of the 82496 Cache Controller cache controller. Once MALE/MBALE goes HIGH, the new address flows through with the appropriate propagation delay (MSET, MTAG, MCFA address valid delay from MALE/MBALE going HIGH). The new address appears at the 82496 Cache Controller outputs if MAOE# and MBAOE# are both active.

If a new cycle starts and MALE and MBALE are HIGH while MAOE# and MBAOE# are inactive, the 82496 Cache Controller's MSET, MTAG, MCFA outputs remain in the high-impedance state. Once MAOE# and MBAOE# are asserted, the new address flows through with the appropriate propagation delay (MSET, MTAG, MCFA address valid delay from MAOE#/MBAOE# going active).

MSET, MTAG, MCFA are used as 82496 Cache Controller inputs (with MAOE# and MBAOE# inactive) during snoop cycles. These address lines are sampled by the 82496 Cache Controller during snoop initiation along with the other snoop attributes.

When Sampled/Driven

If MALE and MBALE are HIGH and MAOE# and MBAOE# are low, MSET, MTAG, MCFA are valid with CADS# and SNPADS# with the timing referenced to CLK. Otherwise, they are asserted with a delay from MALE/MBALE HIGH or MAOE#/MBAOE# active.

MSET, MTAG, MCFA may change when CNA# or CRDY# is sampled active. MSET, MTAG, MCFA have a float delay from MAOE#/MBAOE# going inactive. These outputs are undefined after CRDY#/CNA# assertion and before the next CADS# or SNPADS# assertion.

In synchronous snoop mode, MSET, MTAG, MCFA are sampled on the rising edge of the first CLK in which SNPSTB# becomes active. In clocked mode, MSET, MTAG, MCFA are sampled on the rising edge of the first SNPCLK in which SNPSTB# becomes active. In strobed mode, MSET, MTAG, MCFA are sampled on the falling edge of SNPSTB#.

MSET, MTAG, MCFA are only sampled with SNPSTB#. SNPSTB# may be qualified by CLK, SNPCLK, or the falling edge of SNPSTB#, depending on the snoop mode, and must meet set-up and hold times to the edge being sampled. When SNPSTB# is not asserted, MSET, MTAG, MCFA are "don't care" signals and are not required to meet set-up and hold times.

If MAOE# and MBAOE# are inactive and SNPSTB# is not asserted (no snoop), MSET, MTAG, MCFA need not meet any set-up or hold time.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
MALE/MBALE	The address is valid with CADS# as long as MALE and MBALE are HIGH. If MSET, MTAG, MCFA have been asserted but are blocked by MALE/MBALE, they are asserted when MALE/MBALE go active.
MAOE#/MBAOE#	The address is valid with CADS# as long as MAOE# and MBAOE# are active. If MSET, MTAG, MCFA have been asserted but are blocked by MAOE#/MBAOE#, they are asserted when MAOE#/MBAOE# go active. MSET, MTAG, MCFA may be floated by deasserting MAOE# and MBAOE#.
MAP	MAP indicates the address parity of the 82496 Cache Controller line address bits (i.e., MSET, MTAG, MCFA).
SNPADS#	MSET, MTAG, MCFA are also driven with SNPADS#, so they are valid when SNPADS# is sampled active.
SNPSTB#	MSET, MTAG, MCFA are used as inputs during snoop cycles. They are sampled with SNPSTB# along with the snoop attribute signals.

5.2.2.87. MCLK

MCLK	Memory Bus Clock
	Memory bus Clock signal.
	Input to 82491 Cache SRAM (pin 26)
	Internal Pull-up

Signal Description

In clocked memory bus mode, MCLK provides the memory bus clock. 82491 Cache SRAM Memory bus signals and memory bus data are sampled on the rising edge of MCLK. Memory bus write data is driven with respect to MCLK or MOCLK depending upon the configuration. MCLK need not have any relation to CLK. MCLK has minimum and maximum frequencies, the maximum being the same as CLK (i.e., MCLK <= CLK).

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MBRDY#, MDATA[7:0], MFRZ#, MOEC#, MSEL#, MZBT#	In clocked memory bus mode, the memory bus, MSEL#, MFRZ#, MBRDY#, MZBT# and MEOC# pins are sampled synchronously with the rising edge of MCLK. In a clocked memory bus write, the memory bus outputs are driven synchronously with MCLK or MOCLK.
MOCLK	MOCLK is a delayed version of MCLK. MOCLK is provided to allow the system designer to increase the minimum data hold time available to the memory bus relative to MCLK when data is output from the 82491 Cache SRAM.
MSTBM	MCLK shares a pin with MSTBM. Note that the MCLK/MSTBM pin only becomes MCLK after the following condition: MCLK/MSTBM is toggled AFTER the third CLK which occurs after RESET. Refer to the MSTBM pin description for more details.

5.2.2.88. MCYC#

MCYC#	Memory Bus Cycle
	Indicates that the current cycle will use the memory buffers.
	Output from 82496 Cache Controller (pin Q18), Input to 82491 Cache SRAM (pin 42)
	Synchronous to CLK

Signal Description

MCYC# is a one CLK pulse and, when sampled by the 82491 Cache SRAM, latches the current cycle address into one of the memory cycle address buffers. It selects which memory cycle address buffer will provide the array address, and allocates a memory cycle data buffer for the upcoming memory bus cycle.

Relation to Other Signals

None.

5.2.2.89. MDATA[7:0]

MDATA[7:0]	Memory Bus Data Pins
	Chip Set memory data bus.
	Input/Output of 82491 Cache SRAM (pins 4, 8, 12, 16, 6, 10, 14, 18)
	Synchronous to CLK, MCLK, MOCLK or strobed (MISTB/MOSTB)

Signal Description

MDATA[7:0] comprise the memory data bus of the 82496 Cache Controller/82491 Cache SRAM cache. Depending on the cache configuration, only half of these pins may be used. The pins are directly controlled by the MDOE# input. When MDOE# is inactive, these pins are tri-stated and may be used as inputs.

For write cycles, the 82496 Cache Controller asserts CDTS# to indicate that data is available at the memory bus data pins or in its buffer. In clocked memory bus mode, data is output with a valid delay from MCLK or MOCLK, and is changed with respect to MEOC# or MBRDY#. In strobed memory bus mode, data is output using MOSTB.

For read cycles, data read from the memory bus into the 82491 Cache SRAMs using MBRDY# (clocked memory bus mode) or MISTB (strobed memory bus mode).

For cache configurations which only require 4 MDATA pins, bits 3-0 are used. Unused MDATA[7:4] pins MUST be tied either to VSS or to VCC through resistors.

When Sampled/Driven

When the 82496 Cache Controller initiates a write cycle, the write data is written to the appropriate memory buffer and CDTS# is asserted. If MDOE# is active, the first piece of write data is available at the memory bus data pins with some delay from the CPU CLK edge in which CDTS# is asserted. In clocked mode, subsequent pieces of write data are output with some delay from MCLK or MOCLK (mode dependent) from the edge that MBRDY# is sampled active. In strobed mode, subsequent data is output with MOSTB assertion. MEOC# switches memory cycle buffers and outputs the last piece of data if used in place of the last MBRDY# or MOSTB.

For read cycles, the 82496 Cache Controller asserts CDTS# the CLK before the CPU data path is available for read data. This means that the memory data bus is available before CDTS# is asserted. MDOE# must be inactive for the 82491 Cache SRAM to read data. In clocked memory bus mode, read data is clocked into the 82491 Cache SRAM cache by asserting MBRDY# on MCLK edges. In strobed mode, data is read by MISTB. Data that is read into the 82491 Cache SRAM's memory data pins must meet proper set-up and hold times. MEOC# switches memory cycle buffers and latches the last piece of data if used in place of the last MBRDY# or MISTB.

Data at the data inputs need not follow set-up and hold times to MCLK edges that sample MBRDY# inactive.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CDTS#	If MDOE# is active, write data is available on the data bus some time after CDTS# or MEOC# is sampled active. CDTS# assertion by the 82496 Cache Controller/82491 Cache SRAM cache indicates that the read path is available in the next CLK.
MBRDY#	For write back cycles, new write data is available at the data pins after MBRDY# assertion or MOSTB changing. Data on the memory bus is read in with respect to MBRDY# and MCLK or MISTB.
MBRDY#	The MBC must account for the set-up time to the memory buffers, plus a full CPU CLK to read data into the CPU. If properly done, data on the memory bus can be read in by asserting MBRDY#, and in the next full CPU CLK read into the CPU using BRDY#.
MCLK	Data on the memory bus is read in with respect to MBRDY# and MCLK or MISTB.
MDOE#	If MDOE# is active, write data is available on the data bus some time after CDTS# or MEOC# is sampled active. MDOE# must be inactive for reading data on the memory bus.
MEOC#	If MDOE# is active, write data is available on the data bus some time after CDTS# or MEOC# is sampled active.
MISTB	Data on the memory bus is read in with respect to MBRDY# and MCLK or MISTB.
MOSTB	For write back cycles, new write data is available at the data pins after MBRDY# assertion or MOSTB changing.

5.2.2.90. MDLDRV

MDLDRV	Memory Data Low Drive
	Selects low-capacitance data bus drivers.
	Configuration input to 82491 Cache SRAM (pin 24)
	Synchronous to CLK

Signal Description

Each 82491 Cache SRAM cache SRAM data signal, MDATA[7:0] can be configured for one of two buffers. The buffer selection depends upon the load on these signals and should be based on simulation results of these signals driving that load. The 82491 Cache SRAM configuration input, MDLDRV, is used to select the buffer. Refer to Table 7-14 for the buffer selection specifications, and the appropriate value of MDLDRV.

When Sampled

MDLDRV is sampled as shown in the Initialization and Configuration chapter. MDLDRV becomes the MFRZ# input when RESET goes inactive.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	MDLDRV is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
MFRZ#	MDLDRV shares a pin with MFRZ#.

5.2.2.91. MDOE#

MDOE#	Memory Data Output Enable
	Three-states/Enables Memory Data Outputs.
	Input to 82491 Cache SRAM (pin 20)
	Asynchronous

Signal Description

MDOE# is an 82491 Cache SRAM input that causes the 82491 Cache SRAM to drive its memory bus outputs (MDATA[7:0]). When MDOE# is inactive, these lines are floated and may be used as inputs to the 82491 Cache SRAM. MDOE# is not sampled on any CLK and is a direct connection to the memory output drivers.

When Sampled

Since MDOE# is a direct connection to the 82491 Cache SRAM memory output drivers, MDOE# must always be driven to a valid level. When MDOE# becomes active, data in the 82491 Cache SRAM memory buffer is driven to the data outputs with some propagation delay from MDOE# going active. Similarly, there is some float delay from MDOE# going inactive.

MDOE# must be inactive for the 82491 Cache SRAM to read memory bus data.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MDATA[7:0]	MDOE# must be inactive for reading data on the memory bus. MDOE# must be active for write data to be available on the memory bus.

5.2.2.92. MEOC#

MEOC#	Memory End of Cycle
	Ends 82496 Cache Controller/82491 Cache SRAM cycles by switching buffers.
	Input to 82491 Cache SRAM (pin 23)
	Synchronous to MCLK or asynchronous (strobed mode)
	Glitch Free in Strobed Mode

Signal Description

MEOC# ends the current memory bus cycle and switches memory buffers for a new cycle. Switching to the next memory cycle buffer does not cause information to be lost in the memory or CPU buffers in the 82491 Cache SRAM.

MEOC# is provided so that the memory system can switch to a new cycle without CPU CLK synchronization (this is especially useful in pipelining). In clocked memory bus mode, MEOC# is sampled with the rising edge of MCLK. In strobed memory bus mode, the MEOC# function is performed with falling MEOC# edges.

During read or write cycles, MEOC# may be activated on or after the MCLK edge of the last MBRDY# of a particular cycle. If a cycle is pending (i.e. if pipelining is used), the next cycle flows through with a propagation delay. MEOC# is required for all memory bus cycles.

MEOC# provides three functions in addition to switching memory bus cycles:

1. It resets the memory burst counter to its starting value (this value depends upon MZBT#). If MSEL# is active at this point, MZBT# is sampled, allowing MSEL# to remain active between cycles.
2. During write cycles with PALLC# active, MEOC# causes MFRZ# to be sampled for a subsequent allocation (line fill). Note that if MFRZ# is sampled active, the MEOC# will not switch memory cycle buffers (i.e., the allocation will occur in the same 82491 Cache SRAM buffer).
3. MEOC#, if used in place of the last MBRDY# or MxSTB, latches in the last slice of data before switching buffers.

When Sampled

In clocked memory bus mode, MEOC# is sampled on every MCLK edge and must observe MCLK set-up and hold times. In strobed memory bus mode, MEOC# is always valid and the memory end of cycle function is performed with each MEOC# falling edge. Note that, during initialization, MEOC# must be stable between the third and fourth clocks after the deassertion of RESET.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	MEOC# is asserted on or after the CLK in which BGT# is asserted.
BRDY#	MEOC# for cycle N+1 must be asserted at least one CLK after the last BRDY# of cycle N.
CRDY#	MEOC# enables cycles to end on the memory bus and the next cycle to flow-through before CRDY# is asserted.
	MEOC# is asserted before or on the same CLK as CRDY#.
	MEOC# for cycle N+1 must be asserted at least one CLK after the CRDY# of cycle N.
MBRDY#	The last MBRDY# must come before or on the CLK of MEOC# assertion.
MFRZ#	When MEOC# is active with MSEL#, MZBT# and MFRZ# are sampled.
MSEL#	When MEOC# is active with MSEL#, MZBT# and MFRZ# are sampled.
MZBT#	When MEOC# is active with MSEL#, MZBT# and MFRZ# are sampled.

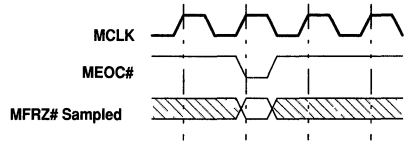
5.2.2.93. MFRZ#

MFRZ#	Memory Data Freeze
	Freezes memory write data in 82491 Cache SRAM buffer.
	Input to 82491 Cache SRAM (pin 24)
	Synchronous to MCLK or asynchronous (strobed mode)
	Internal Pull-up

Signal Description

MFRZ# is a 82491 Cache SRAM input that causes the 82491 Cache SRAM to freeze write data in the current memory cycle buffer. The subsequent allocation fills around the data from the previous write cycle. MFRZ# is provided so that an actual write to memory need not be done in case of an allocation. Using MFRZ# to perform this "dummy write cycle" requires that the MBC put the allocated line in the [M] state. Note that if MFRZ# is sampled active, the MEOC# will not switch memory cycle buffers (i.e., the allocation will occur in the same 82491 Cache SRAM buffer).

PALLC# must be active and MKEN# must be returned active in order for the write cycle to be turned into an allocation (i.e., MFRZ# is ignored if either PALLC# or MKEN# are inactive). MFRZ# is sampled when MEOC# goes active at the end of the write cycle. The subsequent line fill is then filled around the write data to complete the allocation (see Figure 5-28).



NOTES:

1. For strobed mode, MFRZ# is still sampled with respect to MEOC# as shown above; however, MCLK is not active.
2. The MEOC# above occurs at the end of a write cycle. A linefill cycle follows this write cycle.

Figure 5-28. MFRZ# Sampling

In clocked memory bus mode, MFRZ# is sampled with the MCLK rising edge in which MEOC# is sampled active for all CPU write cycles. MFRZ# need only follow a proper set-up and hold time in this situation. Refer to Chapter 6 for an example of a read-for-ownership cycle.

In strobed mode, MFRZ# is sampled with the falling edge of MEOC# for write cycles. MFRZ# need only follow a proper set-up and hold time in this situation.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
DRCTM#	MFRZ# is used so that a dummy write cycle can be performed (to enhance performance). If an allocation is done following this dummy write cycle, DRCTM# must be asserted during the SWEND# window of the line fill to put the allocated line in the [M] state.
MDLDRV	MFRZ# shares a pin with the MDLDRV configuration input.
MEOC#	MFRZ# is sampled with the MEOC# going active or being active for write cycles.
SWEND#	See DRCTM#.

5.2.2.94. MHITM#

MHITM#	Memory Snoop Hit [M]
	Indicates snoop hit to a modified line.
	Output from 82496 Cache Controller (pin J05)
	Synchronous to CLK

Signal Description

MHITM# is asserted by the 82496 Cache Controller to indicate a snoop hit to a line in [M] state. Once a snoop hits a line in the [M] state, the 82496 Cache Controller automatically schedules a snoop write-back. MHITM# is valid one CLK after SNPCYC# and remains valid until the next snoop cycle. If MHITM# is active (LOW) in the CLK after SNPCYC#, it will remain active until the CLK of CRDY# of the snoop write back.

If MHITM# is asserted by any cache during snooping, the bus master should back off from the bus to allow a snoop write back.

When Driven

The snoop lookup is performed in the CLK in which SNPCYC# is asserted. MHITM# for the snoop is driven on the next CLK and remains valid until SNPCYC# is asserted again. MHITM# is not valid in the CLK of SNPCYC#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	The 82496 Cache Controller ignores BGT# while both SNPBSY# and MHITM# are active (i.e., during a snoop write back).
MTHIT#	MTHIT# and MHITM# together indicate the results of an 82496 Cache Controller snoop lookup.
CRDY#	MHITM# goes inactive on clock after CRDY# of a snoop write back cycle.

5.2.2.95. MISTB

MISTB	Memory Bus Input Strobe
	Strobes data into the 82496 Cache Controller/82491 Cache SRAM.
	Input to 82491 Cache SRAM (pin 22)
	Asynchronous

Signal Description

MISTB is an input to the 82491 Cache SRAM that cause the 82491 Cache SRAM to input data through its memory data bus inputs on rising and falling edges. MISTB is used with MSEL# active to advance the memory burst address counter of the memory buffer in use. As a result, new data is latched from the memory bus into the 82491 Cache SRAM memory cycle buffer.

MISTB is used in strobed memory bus mode. In clocked memory bus mode, MISTB is the MBRDY# input.

When Sampled

MISTB is always sampled by the 82491 Cache SRAM. MISTB must meet proper strobed mode active and inactive times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MBRDY#	MISTB shares a pin with MBRDY#.
MSEL#	MISTB is qualified by the MSEL# input. When MSEL# is active, MISTB advances the memory burst counter for the memory buffer in use to input data through the memory data bus pins.
MSTBM	MSTBM determines whether the 82491 Cache SRAM operates in the strobed memory bus mode or in clocked memory bus mode.

5.2.2.96. MKEN#

MKEN#	Memory Cache Enable
	Determines 82496 Cache Controller and CPU cacheability.
	Input to 82496 Cache Controller (pin S02)
	Synchronous to CLK

Signal Description

MKEN# is sampled when the cacheability window is closed (KWEND# is sampled active). MKEN# determines whether the current cycle is cacheable in the 82496 Cache Controller/82491 Cache SRAM cache. A cycle is cacheable by the CPU if, in addition to MKEN# active, CCACHE# is active and the cycle is NOT read only data (MRO# active and CD/C# high).

For read cycles, if MCACHE# and CCACHE# are active, and the cycle is not read only data, KEN# is driven active to the CPU to indicate cacheability. If MKEN# is sampled inactive during KWEND# activation, KEN# to the CPU is made inactive in the next CLK, and the line is non-cacheable by the CPU and the second-level cache. If MCACHE# is inactive, the line is non-cacheable regardless of MKEN#. PCD or LOCK# activation cause MCACHE# to be inactive.

MKEN# is sampled during write-through cycles that are potentially allocatable (PALLC# is active during the write cycle). If MKEN# is sampled active while KWEND# is asserted for the write cycle, an allocation follows the write cycle. During the allocation, MKEN# is ignored. The MBC indicates to the 82496 Cache Controller that it intends to perform an allocation by asserting MKEN#.

MKEN# must be sampled at least one CLK before the first BRDY# assertion to make a line fill non-cacheable to the CPU.

When Sampled

MKEN# is sampled on the CLK edge on which KWEND# is first sampled active. At all other times, MKEN# need not meet set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDY#	MKEN# must be sampled at least one CLK before the first BRDY# assertion to make a line fill non-cacheable to the CPU.
KWEND#	MKEN# and MRO# are sampled when KWEND# is active.

5.2.2.97. MOCLK

MOCLK	Memory Data Output Clock
	Separate CLK reference for memory data output.
	Input to 82491 Cache SRAM (pin 27)
	Asynchronous
	Internal Pull-up

Signal Description

MOCLK is a latch enable for the 82491 Cache SRAM memory data outputs (MDATA[7:0]), and controls the operation of a transparent latch. When MOCLK is HIGH, the data bus is driven from MCLK. When low, data bus outputs are latched. MOCLK may only be used in clocked memory bus mode and only affects output data. The MOCLK input is provided so that a greater memory data minimum output hold time can be obtained (e.g. relative to MCLK). As MOCLK is skewed relative to MCLK, MDATA hold time and output valid delay skews with it. The maximum MOCLK delay allowed is equal to the MCLK high time.

To be used effectively, the MOCLK input must be skewed from MCLK. Figure 5-29 shows how MOCLK can increase the hold time of the output burst data.

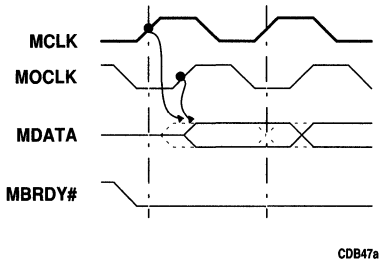


Figure 5-29. Increasing Hold Time of Output Burst Data

When Sampled

MOCLK is sampled during and after RESET to determine whether output data should be driven from MCLK or MOCLK. If MOCLK is toggling, it controls the memory data outputs. If HIGH or LOW, data is driven from MCLK alone. Input data is never referenced to MOCLK.

In strobed memory bus mode the MOCLK signal becomes MOSTB. MOCLK is only used in clocked memory bus mode.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MCLK	To be used effectively, MOCLK must be the same frequency as MCLK but skewed from it. This effectively increases data (memory data bus) hold time to main memory. Main memory must sample the data on MCLK edges.
MOSTB	MOCLK shares a pin with the MOSTB signal.

5.2.2.98. MOSTB

MOSTB	Memory Bus Output Strobe
	Strobes data from the 82496 Cache Controller/82491 Cache SRAM.
	Input to 82491 Cache SRAM (pin 27)
	Asynchronous

Signal Description

MOSTB is an input to the 82491 Cache SRAM that cause the 82491 Cache SRAM to output data through its memory data bus outputs on rising and falling edges. MOSTB is used with MSEL# active to advance the memory burst address counter of the memory buffer in use. As a result, new data is driven from the 82491 Cache SRAM memory cycle or write back buffers.

MOSTB is used only in strobed memory bus mode. In clocked memory bus mode, MOSTB is the MOCLK input.

When Sampled

MOSTB is always sampled by the 82491 Cache SRAM. MOSTB must meet strobed mode active and inactive times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MOCLK	MOSTB shares a pin with MOCLK.
MSEL#	MOSTB is qualified by the MSEL# input. When MSEL# is active, MOSTB advances the memory burst counter for the memory buffer in use to output data through the memory data bus pins.
MSTBM	MSTBM determines whether the 82491 Cache SRAM operates in the strobed memory bus mode or in clocked memory bus mode.

5.2.2.99. MRO#

MRO#	Memory Read-Only
	Designates current line as read-only.
	Input to 82496 Cache Controller (pin K02)
	Synchronous to CLK
	Internal Pull-up

Signal Description

MRO# is sampled at the closing of the cacheability window (on KWEND# activation). If sampled active, MRO# causes the current line fill to the 82496 Cache Controller/82491 Cache SRAM cache to be put in the Shared state with the read only bit set. Read only code is, in turn, cached in the Pentium processor code cache. Read only data is NOT cached in the Pentium processor data cache. Writes during which MRO# is sampled active during KWEND# should not initiate a read for ownership.

Once MRO# is sampled active on KWEND# activation, KEN# to the CPU is driven inactive regardless of the state of MKEN# for data accesses (CD/C#=1). For code accesses (CD/C#=0) in which MRO# is sampled active on KWEND# activation, the value of KEN# driven to the CPU depends upon the value of MKEN#. MKEN# does, however, determine whether the 82496 Cache Controller caches the read-only line. If MKEN# is returned active, the 82496 Cache Controller/82491 Cache SRAM requires an entire cache line from the memory bus. "Read-Only" cache lines are placed in the [S] state.

If MRO# is returned active during KWEND#, DRCTM# and MWB/WT# are ignored during SWEND#.

The linefill portion of an allocation may be placed in the read only state by returning MRO# active during KWEND# of the write. MRO# is ignored at KWEND# of the allocation (linefill).

MRO# must be returned to the 82496 Cache Controller at least one CLK before BRDY# is returned to the CPU so KEN# can be sampled properly (when CD/C#=1 and CCACHE#=0).

There is one read-only bit per 82496 Cache Controller tag. If the cache is configured to have two lines per sector, there is one read-only bit per sector (e.g. two lines). Therefore, in a two lines per sector configuration, the two lines must be both read only or neither read only.

WARNING

If the first line in a sector is cached as read only (the read only bit is set), the 82496 Cache Controller will allow the second to be cached in [E] or [M] states. It is the MBCs responsibility to insure that this does not occur by asserting MRO# for BOTH lines in a read only sector!

When Sampled

MRO# and MKEN# are sampled on the first CLK in which KWEND# is sampled active. For cacheable read miss cycles, they are sampled with the KWEND# of the read. For write-through

with potential allocate cycles, they are sampled with the KWEND# of the write-through (not during the allocation). In all other CLKs, MRO# need not follow set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDY#	To make CPU accesses not cacheable, MRO# must be returned at least one CLK prior to the first BRDY# (when CCACHE#=0 and CD/C#=1).
KWEND#	MRO# and MKEN# are sampled with KWEND# activation.

5.2.2.100. MSEL#

MSEL#	Memory Buffer Chip Select
	Selects 82491 Cache SRAM SRAMs, initiates MZBT# sampling.
	Input to 82491 Cache SRAM (pin 25)
	Synchronous to MCLK or asynchronous (strobed mode)

Signal Description

MSEL# is a 82491 Cache SRAM input providing three main functions:

1. MSEL# active qualifies the MBRDY# input to the 82491 Cache SRAM. If MSEL# is inactive, MBRDY# is not recognized.
2. MSEL# inactive causes MZBT# to be sampled for the next transfer. MSEL# going active latches the MZBT# value for the next transfer.
3. MSEL# going inactive initializes the 82491 Cache SRAM's internal memory burst counter (the value depends upon the sampled value of MZBT#).

The data portion of the 82491 Cache SRAM contains a memory burst counter that counts through the CPU burst order with each MBRDY# assertion (or MISTB or MOSTB transition) and increments a pointer to the memory buffer being accessed.

MSEL# going inactive resets this burst counter to its original burst value if MZBT# was sampled inactive. By resetting this counter before MEOC# assertion, the memory bus can write over the data that was latched into the memory cycle buffers. This would be necessary if the MBC began latching data from main memory prior to the snoop window closure, and the snoop result was a hit to a modified line in another cache.

MSEL# may stay inactive for single transfer cycles such as posted 64-bit write cycles. Once active, MSEL# need not go inactive because the burst counter is RESET with MEOC# activation. Since MZBT# may also be sampled with MEOC#, it is possible to leave MSEL# asserted throughout most basic transfers.

MSEL# or MEOC# must be used to reset the burst counter before any transfer begins. If transfers have begun (due to a very fast memory subsystem) and are interrupted (for example, by a snoop hit to [M] before BGT# assertion), MSEL# must be brought inactive so the burst counter may be reset for the snoop-write-back. MSEL# must be sampled inactive for at least one MCLK after RESET. This resets the memory burst counter for the first transfer.

When Sampled

In clocked memory bus mode, MSEL# is sampled with every rising edge of MCLK. In this mode, if MSEL# is sampled inactive, the memory burst counter is RESET and MZBT# is sampled. If MSEL# is sampled active and MBRDY# is sampled active, the memory burst counter is incremented. Since it is constantly sampled with MCLK, MSEL# must always be driven to a known state and must always meet set-up and hold times to every MCLK edge.

In strobed mode, the falling edge of MSEL# causes MZBT# to be sampled. While MSEL# is active, MISTB and MOSTB cause the memory burst counter to be incremented. The rising edge of MSEL# causes the memory burst counter to be RESET.

MSEL# must be inactive for 1 CLK sometime after RESET (before the first transfer) to initialize the burst counter.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MBRDY#	MSEL# qualifies the use of MBRDY#. Since MSEL# acts as a qualifier for this signal, it may be asserted with MBRDY#.
MISTB	MSEL# qualifies the use of MISTB. Since MSEL# acts as a qualifier for this signal, it may be asserted with MISTB.
MOSTB	MSEL# qualifies the use of MOSTB. Since MSEL# acts as a qualifier for this signal, it may be asserted with MOSTB.
MZBT#	MSEL# causes MZBT# to be sampled.

5.2.2.101. MSTBM

MSTBM	Memory Strobed Mode
	Strobed memory mode selection.
	Configuration input to 82491 Cache SRAM (pin 26)
	Synchronous to CLK

Signal Description

MSTBM determines whether the 82491 Cache SRAM operates in the strobed memory bus mode or in clocked memory bus mode. If MSTBM is sampled (tied) HIGH or LOW on and after the falling edge of RESET, the 82491 Cache SRAM operates in strobed mode. If a CLK is detected on this pin any time after the falling edge of RESET, the 82491 Cache SRAM enters clocked memory bus mode, and the input becomes the memory CLK (MCLK) input.

When Sampled

MSTBM is sampled as shown in the Initialization and Configuration chapter.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	MSTBM is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
MCLK	In clocked memory bus mode, MSTBM is connected to the MCLK source to become the MCLK input.

5.2.2.102. MTHIT#

MTHIT#	Memory Snoop Hit to a Valid State
	Indicates snoop hit.
	Output from 82496 Cache Controller (pin H04)
	Synchronous to CLK

Signal Description

MTHIT# is asserted to indicate that a snoop has hit a line in [M], [E] or [S] state. MTHIT# is valid one CLK after SNPCYC# and remains valid until the next snoop cycle.

When Driven

The snoop lookup is performed in the CLK in which SNPCYC# is asserted. The MTHIT# snoop result is driven on the next CLK and remains valid until the next SNPCYC#. MTHIT# is not valid in the CLK of SNPCYC#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MHITM#	MTHIT# and MHITM# together indicate the results of a 82496 Cache Controller snoop lookup.

5.2.2.103. MTR4/8#

MTR4/8#	Memory 4/8 Transfers
	Select number of transfers.
	Configuration Input to 82491 Cache SRAM (pin 25)
	Synchronous to CLK

Signal Description

MTR4/8# is used to select whether a cache line requires four or eight transfers. This selection depends on the ratio between the 82496 Cache Controller/82491 Cache SRAM's second-level cache line size and its memory data bus width.

When Sampled

MTR4/8# is sampled as shown in the Initialization and Configuration chapter. After RESET goes inactive, MTR4/8# becomes MSEL#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	MTR4/8# is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
MSEL#	MTR4/8# shares a pin with MSEL#.

5.2.2.104. MWB/WT#

MWB/WT#	Memory Write-Back/Write-Through
	Forces write-back or write-through policy.
	Input to 82496 Cache Controller (pin L04)
	Synchronous to CLK

Signal Description

MWB/WT# is a 82496 Cache Controller input that is sampled at the closing of the snoop window (at SWEND# activation). If sampled low, the current line fill is placed in the 82496 Cache Controller in the [S] (write-through) state.

MWB/WT# is used in many situations. For example, when a cache-to-cache transfer updates memory and leaves valid data in another cache (i.e., does not assert SNPINV), the line must be put in the [S] state. Also, a portion of memory may be designated as write-through by making MWB/WT#=0 for appropriate addresses.

DRCTM# does not affect the 82496 Cache Controller if MWB/WT# is sampled low, or if MRO# has been sampled active during KWEND#. If PWT is active or MRO# is sampled active, the line is placed in the [S] state regardless of MWB/WT#.

When Sampled

MWB/WT# is sampled on the first CLK edge on which SWEND# is sampled active. MWB/WT# is sampled during SWEND# of linefills, allocations, and write-throughs with potential upgrade (e.g. a write hit to S state which is not read-only and PWT is inactive). If MWB/WT# is not being sampled, it need not meet set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
DRCTM#	If MWB/WT# is sampled Low during SWEND#, DRCTM# is ignored.
SWEND#	Both MWB/WT# and DRCTM# are sampled with SWEND# assertion.

5.2.2.105. MX4/8#

MX4/8#	Memory 4/8 I/O bus width
	Select memory bus width.
	Configuration Input to 82491 Cache SRAM (pin 21)
	Synchronous to CLK

Signal Description

MX4/8# specifies the memory data bus width. If MX4/8# is sampled HIGH on the falling edge of RESET, the 82491 Cache SRAM is configured to use only the MDATA[3:0] memory data bus pins. If MX4/8# is sampled LOW on the falling edge of RESET, the 82491 Cache SRAM is configured to use all eight memory data bus pins (MDATA[7:0]). The necessary value of MX4/8# is based on the other configuration options chosen (refer to Table 4-4).

When Sampled

MX4/8# is sampled as shown in the Initialization and Configuration chapter. After RESET goes inactive, MX4/8# becomes MZBT#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	MX4/8# is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
MZBT#	MX4/8# shares a pin with MZBT#.

5.2.2.106. MZBT#

MZBT#	Memory Zero Base Transfer
	Forces cycles to begin at sub-line address 0.
	Input to 82491 Cache SRAM (pin 21)
	Synchronous to MCLK or Asynchronous (Strobed Mode)
	Internal Pull-up

Signal Description

MZBT# is an input to the 82491 Cache SRAM that forces a memory bus read or write cycle to begin with burst address 0 regardless of the CPU-generated or snoop initiated burst address. In systems that never force a zero-based transfer, MZBT# may be driven HIGH after RESET.

MZBT# is sampled before the transfer begins with MSEL# inactive or both MSEL# and MEOC# active.

Once sampled active, data input to the 82491 Cache SRAM's data bus begins at burst address 0 and continue through 8, 10, etc. (for 64 bit memory buses) or through 10, 20, etc. (for 128 bit memory buses). If the CPU requests a burst location other than 0, the MBC must hold off any BRDY# until that bursted item is read from the memory bus.

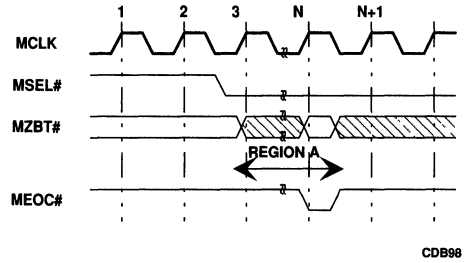
When Sampled

In clocked mode, MZBT# is sampled in two places. First, MZBT# is sampled on all MCLK rising edges in which MSEL# is sampled inactive. Once MSEL# is sampled active, the value of MZBT# that was sampled one MCLK before is used for the next transfer. Second, MZBT# is sampled on MCLK rising edges where MEOC# is sampled active with MSEL# active. The MZBT# value sampled is used for the next transfer. This allows MSEL# to stay asserted between transfers, if needed (see Figure 5-30).

In clocked memory bus mode, MZBT# must follow set-up and hold times to all MCLK edges where MSEL# is sampled inactive or MEOC# is sampled active with MSEL# active.

In strobed mode, MZBT# is sampled with the same signals. First, it is sampled with the falling edge of MSEL#. Second, it is sampled with the falling edge of MEOC# when MSEL# is active.

In strobed memory bus mode, MZBT# must meet set-up and hold times to MSEL# falling edge and MEOC# falling edge if MSEL# is active.



NOTES:

1. In strobed mode, MZBT# is still sampled with respect to MSEL# and MEOC# as shown above; however, MCLK is inactive.
2. The MZBT# value sampled on clock 2 is used for the first transfer that occurs in region A. The MZBT# value sampled on clock n is used for the first transfer that occurs on any clock following clock n.

Figure 5-30. MZBT# Sampling

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MEOC#	MZBT# is sampled with MSEL# and MEOC# and has no affect otherwise.
MSEL#	MZBT# is sampled with MSEL# and MEOC# and has no affect otherwise.
MX4/8#	MZBT# shares a pin with the MX4/8# configuration input.

5.2.2.107. NA#

NA#	Next Address
	Indicates that a new address cycle can be generated.
	Output from 82496 Cache Controller (pin K18), Input to Pentium processor (pin K03)
	Synchronous to CLK
	82496 Cache Controller internal Pull-up

Signal Description

Prior to the 82496 Cache Controller issuing NA# to the Pentium processor, it must insure the following rules:

1. Pipelining is no more than 1.5 deep. This means that no more than two active ADS# cycles are allowed. Therefore, an NA# for a subsequent cycle cannot be issued until the BRDY#.BLAST# or BRDYC#*BLAST# of the first outstanding ADS# cycle has been driven.
2. The CPU Byte Enables (BE[7:0]#) for the current ADS# has been latched in the 82491 Cache SRAM Byte Enable Latch (MBE#). Refer to the BLEC# and MBE# signal descriptions for details.
3. The caching attributes (KEN# and WB/WT#) to the Pentium processor are known or not sampled.

For cycles which sample KWEND# (MKEN#&MRO#), the caching attributes are known one CLK after KWEND#. For cycles which do not sample KWEND#, the caching attributes may be known earlier. An NA# that is driven when the caching attributes are not sampled is called a 'Blind NA#'. A Blind NA# has the advantage of potentially being as early as one CLK after ADS#.

A Blind NA# is issued in the following cases:

1. Locked cycles. The caching attributes do not apply since the cycles are not CPU cacheable.
2. Write cycles. The caching attributes are available as early as one CLK after ADS#.
3. Read cycles which are not cacheable in the CPU (CACHE# is inactive). The caching attributes are not sampled.

When Driven

For non-cacheable hit cycles, a Blind NA# will be issued.

For non-cacheable miss cycles, NA# will be issued once the CPU Byte Enables are latched (using BLEC#).

For cacheable miss cycles, NA# will be issued one CLK after KWEND#. Note that since it is a miss to the 82496 Cache Controller/82491 Cache SRAM cache WB/WT# will always be

driven low to the CPU.

For cacheable hit cycles, NA# is issued once the caching attributes (KEN# & WB/WT#) are ready on the CPU pins.

In all cases, the 1.5 deep pipeline rule will be met.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BLAST#, BRDY(C)#, CNA#, KWEND#	The CLK in which NA# is issued to the CPU is dependent on the following signals: KWEND#, CNA# (which affects BLEC# and MBE#), BRDYC#*BLAST#, or BRDY#*BLAST#.

5.2.2.108. NENE#

NENE#	Next Near
	Indicates cycle address is "near" previous address.
	Output from 82496 Cache Controller (pin E06)
	Synchronous to CLK

NENE# Signal Description

NENE# is asserted by the 82496 Cache Controller to indicate that the memory address of a given memory cycle is in the same 2K DRAM page as the address of the previous cycle. This information may be used by the MBC to optimize accesses to page-mode or static-column DRAMs.

NENE# must be ignored by the MBC if the memory bus accesses to the same page are not consecutive. For example, if a snoop write back cycle is issued between two normal memory bus cycles, the NENE# signal may go active, but has no meaning since the snoop address interfered with the "near" address checking.

When Driven

NENE# is valid with CADS# and SNPADS# and remains valid until CNA# or CRDY# is asserted.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.
CNA#	NENE# may change its state after CNA# or CRDY# is asserted.
CRDY#	NENE# may change its state after CNA# or CRDY# is asserted.

5.2.2.109. NMI

NMI	Non-maskable Interrupt
	Pentium processor non-maskable interrupt.
	Input to Pentium processor (pin N19)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.110. PALLC#

PALLC#	Potential Allocate
	Indicates 82496 Cache Controller intent to allocate current cycle.
	Output from 82496 Cache Controller (pin E03)
	Synchronous to CLK

Signal Description

PALLC# is asserted to indicate to the MBC that the current write cycle may allocate a cache line (i.e. perform a line fill). The MBC indicates that it intends to perform an allocation by driving MKEN# active (note that MRO# can be active) during KWEND# of the write miss cycle. Potential allocate cycles are misses to the second-level cache with PCD and PWT inactive.

PALLC# is asserted upon the following sequence of Pentium processor signals:

(82496 Cache Controller Miss)*!PCD*!PWT*!LOCK#*W/R#*D/C#*M/IO#

PALLC# is inactive during write hits, snoop write back cycles, allocations, and replacement write back cycles.

When Driven

PALLC# is valid with CADS# and SNPADS# and remains valid until CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.111. PAR#

PAR#	Parity Selection
	Selects 82491 Cache SRAM as a parity device.
	Configuration input to 82491 Cache SRAM (pin 32)
	Synchronous to CLK

Signal Description

When PAR# is asserted low at reset, the 82491 Cache SRAM is configured as a dedicated parity device. A 82491 Cache SRAM parity device must be configured in the same manner as all other 82491 Cache SRAM devices in the array; however, the data lines are defined differently. CDATA[3:0] are 4 bit parity I/O lines and CDATA[7:4] are 4 parity bit (or data byte) select lines, allowing each parity bit to be written individually. Parity devices must be used as shown in Table 4-5.

When Sampled

PAR# is a configuration option and must be driven either HIGH or LOW at reset. If PAR# is driven HIGH during RESET, it becomes MBE# after RESET goes inactive.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	PAR# is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
MBE#	PAR# shares a pin with MBE#.
CDATA[7:0]	PAR# affects the definition of the 82491 Cache SRAM CDATA and MDATA lines. For 82491 Cache SRAM parity devices, CDATA[3:0] are connected to four of the Pentium processor DP[7:0] pins, and CDATA[7:4] are connected to four of the Pentium processor BE[7:0] pins.
MDATA[7:0]	PAR# affects the definition of the 82491 Cache SRAM CDATA and MDATA lines. For 82491 Cache SRAM parity devices, MDATA[3:0] drives the data parity bits and MDATA[7:4] drives the CPU byte enables.

5.2.2.112. PCD

PCD	Page Cacheability Disable
	Indicates CPU cycle cacheability.
	Output from Pentium processor (pin W04), Input to 82496 Cache Controller (pin J16)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.113. PCHK#

PCHK#	Parity Status Output
	Pentium processor parity status.
	Output from Pentium processor (pin R03)
	Synchronous to CLK
	Glitch Free

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.114. PEN#

PEN#	Parity Error Enable
	Determines if machine check interrupt is taken on a parity error.
	Input to Pentium processor (pin M18)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.115. PRDY

PRDY	PRDY
	For use with Intel debug port.
	Output from Pentium processor

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.116. PWT

PWT	Page Write Through
	Indicates CPU cycle write through attribute.
	Output from Pentium processor (pin S03), Input to 82496 Cache Controller (pin D18)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.117. R/S#

R/S#	R/S#
	For use with Intel debug port.
	Asynchronous Input
	Internal Pull-up Resistor

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.118. RDYSRC

RDYSRC	Ready Source
	Source of BRDY# indication.
	Output from 82496 Cache Controller (pin D02)
	Synchronous to CLK

Signal Description

RDYSRC is a cycle control signal to the MBC that indicates the source of the CPU BRDY# generation. When RDYSRC is HIGH, it indicates that the MBC should generate the BRDY# signals to the CPU, 82496 Cache Controller, and 82491 Cache SRAM. When low, it indicates that the 82496 Cache Controller will provide the BRDY# signals.

RDYSRC is active (HIGH) for CPU read cycles and I/O cycles. RDYSRC is inactive for Allocation, replacement write back, and snoop write back cycles.

When Driven

RDYSRC is valid with CADS# and SNPADS# and remains valid until CRDY# or CNA#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.119. RESET

RESET	RESET CPU and Second-Level Cache
	Forces Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM to begin executing in a known state.
	Input to Pentium processor (pin L18), 82496 Cache Controller (pin R06), and 82491 Cache SRAM (pin 28)
	Asynchronous

Signal Description

The falling edge of this signal tells the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM to sample all configuration inputs and begin in a known state. See the specific configuration signals for set-up and hold times relative to the falling edge of RESET. RESET can be asserted at any time.

The 82496 Cache Controller and 82491 Cache SRAM devices should be initialized simultaneously. The RESET inputs between the components can have up to a 1 CLK skew.

When Sampled

The RESET signals are asynchronous inputs and the MBC must guarantee a minimum pulse width.

Relation to Other Signals

Table 5-9 lists the signals that are sampled at RESET. Note that a pin that outputs/inputs both a configuration signal (during reset) and another signal changes its value from configuration signal to non-configuration signalon the rising edge of the first clock after RESET deassertion. For example, the pin that inputs CLDRV during reset will input BGT# on the rising edge of the first clock after RESET is deasserted.

Table 5-9. Signals Sampled at RESET

Pentium™ Processor Configuration Inputs	
BUSCHK#	Must be LOW.
82496 Cache Controller Configuration Inputs	
CNA# [CFG0]	CFG0-CFG2 are the configuration inputs that are sampled by the 82496 Cache Controller cache to determine which configuration it should operate in.
SWEND# [CFG1]	
KWEND# [CFG2]	
FLUSH#	Must be HIGH for proper Pentium processor/82496 Cache Controller operation.
BGT# [CLDRV]	Selects the driving strength of the 82496 Cache Controller/82491 Cache SRAM interface buffers.
SYNC# [MALDRV]	Selects the memory address bus driver strength.
SNPCLK# [SNPMD]	Indicates the snooping mode.
MALE [WWOR#]	When low Selects weak write ordering
CRDY#[SLFTST#]	Invokes 82496 Cache Controller self-test if HIGHZ# high.
MBALE[HIGHZ#]	Tristates 82496 Cache Controller outputs if active with SLFTST#.
82491 Cache SRAM Configuration Inputs	
MZBT#[MX4/8#]	Determines whether each 82491 Cache SRAM uses four or eight I/O pins on the memory bus.
MSEL#[MTR4/8#]	Determines the number of memory bus transfers needed to fill each cache line.
MCLK[MSTBM]	Indicates the memory bus configuration: Strobed if high, Clocked if toggling.
MFRZ# [MDLDRV]	Selects the memory data bus driver strength.
MBE#[PAR#]	Configures the 82491 Cache SRAM as a parity storage device if active.

5.2.2.120. SCYC

SCYC	Split Cycle
	Indicates the current locked cycle is misaligned.
	Output from Pentium processor (pin R04), Input to 82496 Cache Controller (pin G16)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.121. SEC2#

SEC2#	Lines per Sector
	Indicates the lines per sector configuration information.
	Configuration Output from 82496 Cache Controller (pin N15), Input to 82491 Cache SRAM (pin 38)
	Synchronous to CLK

Signal Description

When driven low to the 82491 Cache SRAM, SEC2# indicates that each tag will represent two 82496 Cache Controller/82491 Cache SRAM cache lines in the 82491 Cache SRAM SRAM. If SEC2# is driven high to the 82491 Cache SRAM, it indicates that each tag will represent only one cache line in the 82491 Cache SRAM SRAM.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
WBA	SEC2# shares a pin with WBA.

5.2.2.122. SLFTST#

SLFTST#	Self Test
	Executes 82496 Cache Controller self-test.
	Configuration Input to 82496 Cache Controller (pin N03)
	Synchronous to CLK

Signal Description

If SLFTST# is active while HIGHZ# is inactive during RESET, the 82496 Cache Controller cache controller enters self-test. If SLFTST# and HIGHZ# are both sampled active during RESET, the 82496 Cache Controller floats all outputs and I/O signals until the next RESET. If SLFTST# is inactive, a normal initialization occurs. See Table 5-5 (HIGHZ# pin description).

The self-test results are obtained by latching CAHOLD in the first CLK that FSIOUT# is inactive. If CAHOLD is sampled HIGH, self-test completed successfully. If CAHOLD is sampled LOW, a self-test failure occurred.

When Sampled

SLFTST# is sampled with RESET as shown in the Initialization and Configuration Chapter. After the falling edge of RESET, SLFTST# becomes the CRDY# pin.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	SLFTST# is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
CRDY#	SLFTST# shares a pin with CRDY#.
HIGHZ#	The 82496 Cache Controller enters self-test if SLFTST# is sampled active while HIGHZ# is sampled inactive.

5.2.2.123. SMI#

SMI#	System Power Management Interrupt
	Latches a power interrupt request.
	Input to Pentium processor (pin P18)
	Asynchronous
	Internal Pull-up

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.124. SMIACT#

SMIACT#	System Power Management Interrupt Active
	Indicates that the CPU is operating in System Management Mode.
	Output from Pentium processor (pin T05)
	Asynchronous

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.125. SMLN#

SMLN#	Same Line
	Current cycle address in same 82496 Cache Controller line as previous cycle.
	Output from 82496 Cache Controller (pin D07)
	Synchronous to CLK

Signal Description

SMLN# indicates that a given memory cycle accesses the same line in the 82496 Cache Controller's second-level cache as the previous memory cycle. SMLN# can be used by the MBC to selectively activate its SNPSTB# signal to other caches in the system. In this way, for example, back-to-back snoop hits to the same line may be snooped only once.

SMLN# must be ignored by the MBC if the memory bus accesses to the same page are not consecutive. For example, if a snoop write back cycle is issued between two normal memory bus cycles, the SMLN# signal may go active, but has no meaning since the snoop address interfered with the "same line" address checking.

When Driven

SMLN# is asserted with CADS# and SNPADS# and remains valid until CNA# or CRDY#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Address and cycle specification signals (i.e., APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, KLOCK#, MAP, MBT[3:0], MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#) are valid with CADS#.

5.2.2.126. SNPADS#

SNPADS#	Cache Snoop Address Strobe
	Initiates a snoop write-back cycle.
	Output from 82496 Cache Controller (pin G04)
	Synchronous to CLK
	Glitch Free

Signal Description

SNPADS# indicates that cache address, control, and attribute signals are valid for a snoop write-back cycle. SNPADS# functions identically to CADS#, but is generated only on snoop write-backs. Two address status signals (one for normal cycles and another for snoop write-back cycles) are provided to ease MBC implementation.

When SNPADS# is activated, the MBC aborts the pending bus cycle (for which BGT# is not yet issued). The 82496 Cache Controller sometimes re-issues these non-committed cycles after the snoop write-back has completed.

A snoop write back cycle is not pipelined into a previous cycle, and no cycles can be pipelined into a snoop write back cycle.

CRDY#, MBRDY# (or MOSTB), and MEOC# are the only cycle progress signals required during snoop write-back cycles.

When Driven

The 82496 Cache Controller snoop response appears on the MTHIT# and MHITM# pins in the CLK after SNPCYC# becomes active. If MHITM# is driven active, the snoop has resulted in a hit to a modified line, and a snoop write-back is initiated with SNPADS# being asserted. SNPADS# is driven no sooner than two CLKs after SNPCYC#. Like CADS#, SNPADS# remains active for one CLK and is always valid.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	The 82496 Cache Controller never asserts CADS# and SNPADS# on the same CLK. There are always one or more CLKs between CADS# and a following SNPADS#.
CDTS#	CDTS# is always asserted a minimum of 1 CLK after SNPADS#.
CNA#	CNA# is ignored during snoop write back cycles (initiated with SNPADS#).
CRDY#	Cycles initiated by SNPADS# require CRDY# but do not require other cycle progress signals (BGT#, KWEND#, SWEND#).
Snoop Address and Cycle Specification Signals	SNPADS# indicates the start of the write-back cycle. Here, the 82496 Cache Controller drives the following address and cycle specification signals with SNPADS#: APIC#, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, CWAY, MAP, MBE#, MCACHE#, MCFA, MSET, MTAG, NENE#, PALLC#, RDYSRC, and SMLN#.

5.2.2.127. SNPBSY#

SNPBSY#	Snoop Busy
	Indicates snoop resources are busy and the snoop will be delayed.
	Output from 82496 Cache Controller (pin G02)
	Synchronous to CLK

Signal Description

SNPBSY# and SNPCYC# indicate that a snoop is in progress. SNPCYC# is asserted when the snoop look-up is performed on the 82496 Cache Controller tags. If the look-up indicates that a valid line is hit, and the snoop request requires invalidation, the 82496 Cache Controller performs a back-invalidation to the Pentium processor. If the snoop hits a modified line in the 82496 Cache Controller/82491 Cache SRAM cache, the 82496 Cache Controller performs an inquire and a back-invalidation to the Pentium processor. The inquire or back-invalidation is delayed if another snoop cycle (inquire or back-invalidation) to the CPU is in progress. If a snoop hit occurs to a modified line, a snoop write-back must occur. SNPBSY# is driven active during back-invalidations when the BINV of a previous snoop is in progress and during snoop write-backs.

SNPBSY# indicates to the MBC that the next snoop look up is delayed until two CLKs after SNPBSY# goes inactive. If SNPBSY# is active, one snoop request (address) is latched in the 82496 Cache Controller until it has an opportunity to respond to the request.

When Driven

SNPBSY# is activated in two circumstances. First, SNPBSY# is activated whenever back-invalidation is needed and one is already in progress. Second, SNPBSY# is activated when a modified cache line is hit on a snoop. Here, SNPBSY# is asserted together active along with MHITM# until the modified line has been written back (until CRDY# is returned for the snoop write-back).

SNPBSY# will go active, as needed, in the CLK following SNPCYC# and remains active for at least two CLKs.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
SNPCYC#	Following SNPCYC#, a new snoop may be initiated. If SNPBSY# is asserted for the initial snoop, SNPCYC# for the second snoop is delayed until SNPBSY# is de-asserted for the initial snoop to indicate that snoop processing has completed.
BGT#	The 82496 Cache Controller ignores BGT# while both SNPBSY# and MHITM# are active (i.e., during a snoop write back).

5.2.2.128. SNPCLK

SNPCLK	Snooping Clock
	82496 Cache Controller snooping clock for clocked memory bus interfaces.
	Input to 82496 Cache Controller (pin T04)
	Internal Pull-up

Signal Description

The SNPCLK input determines the execution rate and timing of 82496 Cache Controller snoop operations. During clocked snooping operations, SNPSTB#, SNPINV, SNPNCA, MBAOE#, MAOE#, and the address (MCFA, MSET, MTAG) and address parity (MAP) lines are sampled on the rising edge of SNPCLK. The SNPCLK input requires TTL levels for proper operation.

NOTE

SNPCLK frequency <= CPU CLK frequency

Relation to Other Signals

Pin Symbol	Relation to Other Signals
SNPMD	SNPCLK shares a pin with the SNPMD configuration input.

5.2.2.129. SNPCYC#

SNPCYC#	Snoop Cycle
	Indicates snoop look-up in progress.
	Output from 82496 Cache Controller (pin J04)
	Synchronous to CLK
	Glitch Free

Signal Description

SNPCYC# is asserted by the 82496 Cache Controller during the CLK in which the snoop tag look-up is performed. SNPCYC# may be driven on the CLK after SNPSTB# is asserted or may be delayed by several CLKs. SNPCYC# can be delayed when a previous snoop is in progress (when SNPBSY# asserted due to a snoop write-back or back-invalidation for a previous snoop cycle), when an 82496 Cache Controller memory bus cycle is in progress (when SNPSTB# is asserted between BGT# and SWEND#), or during synchronization (as in clocked and strobed snooping modes).

When Driven

SNPCYC# is always a valid 82496 Cache Controller output and is asserted for one CLK whenever an 82496 Cache Controller snoop lookup is performed.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	The 82496 Cache Controller ignores BGT# during SNPCYC#.
BRDY#	For Read-Miss cycles, the first BRDY# must be > 1 + 4 * LR CLKs from the last SNPCYC# before BGT#. (Note: LR=Line Ratio)
MAPERR#	In both clocked and strobed memory bus modes, MAPERR# will go active (if a memory address parity error is detected) in the CLK following SNPCYC# active.
MHITM#/MTHIT#	MHITM# and MTHIT# report valid snoop results in the CLK following SNPCYC# and SNPBSY# is activated when needed.

5.2.2.130. SNPINV

SNPINV	Snoop Invalidation
	Forces invalidation of snoop hits.
	Input to 82496 Cache Controller (pin Q06)
	Synchronous to CLK or SNPCLK, or asynchronous (Strobed Mode)

Signal Description

The 82496 Cache Controller samples SNPINV when SNPSTB# is asserted during snoop cycles. SNPINV invalidates the cache line at the snoop address (places it in the [I] state).

When one bus master performs a bus access, the SNPSTB# signal to all C5Cs is asserted, initiating a snoop for that address. If the master is modifying memory (as in a write cycle), the C5Cs containing valid data must invalidate their entries. This is forced by asserting SNPINV.

If SNPINV is asserted for a snoop and the snoop hits a modified line, the line is invalidated and written back.

SNPINV forces all snoop hits to be invalidated, overriding other inputs or attributes (e.g. SNPNCA). As long as SNPINV is not asserted, cache states are maintained according to the SNPNCA value.

When Sampled

In synchronous snoop mode, SNPINV is sampled on the rising edge of the first CLK in which SNPSTB# becomes active. In clocked mode, SNPINV is sampled on the rising edge of the first SNPCLK in which SNPSTB# becomes active. In strobed mode, SNPINV is sampled on the falling edge of SNPSTB#.

SNPINV is only sampled with SNPSTB#. SNPSTB# may be qualified by CLK, SNPCLK, or the falling edge of SNPSTB#, depending on the snoop mode, and must meet set-up and hold times to the edge being sampled. When SNPSTB# is not asserted, SNPINV is a "don't care" signal and is not required to meet set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
SNPNCA	SNPINV overrides the SNPNCA input, which may also be asserted with SNPSTB#.
SNPSTB#	SNPINV is sampled according to SNPSTB#, which may be qualified by SNPCLK or CLK, depending on the snoop mode.

5.2.2.131. SNPMD

SNPMD	Snooping Mode
	Selects 82496 Cache Controller snooping mode.
	Configuration input to 82496 Cache Controller (pin T04)
	Synchronous to CLK

Signal Description

SNPMD selects whether snoop initiation is in synchronous, clocked or strobed mode (82496 Cache Controller snoop response is always synchronous to CLK).

Synchronous mode is selected if SNPMD is sampled LOW on the falling edge of RESET. Strobed mode is selected if SNPMD is sampled HIGH on the falling edge of RESET. Clocked mode is selected by connecting the memory bus controller (MBC) snoop clock source to SNPMD, thereby making SNPMD the snoop clock (SNPCLK) input.

When Sampled

SNPMD is not used except when clocked mode is selected. When clocked mode is selected, SNPMD becomes SNPCLK in order to clock in snoop requests.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	SNPMD is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
SNPCLK	SNPMD becomes SNPCLK if a clock signal is detected on this input. In clocked snooping mode, SNPCLK is used to clock in SNPSTB#, the snoop address, snoop address parity, and all snoop attributes.

5.2.2.132. SNPNCA

SNPNCA	Snoop Non-Caching device Access
	Indicates to 82496 Cache Controller that the snoop is a non-cacheable access.
	Input to 82496 Cache Controller (pin R04)
	Synchronous to CLK or SNPCLK, or asynchronous (Strobed Mode)

Signal Description

SNPNCA is sampled with SNPSTB# to prevent the cache line at the snoop address from entering the [S] state from [E] or [M] state unnecessarily.

When a bus master performs a bus access, SNPSTB# is asserted to all C5Cs to initiate a snoop for that address. If the snoop is a hit in the 82496 Cache Controller, the tag state changes to [S] because another bus master is requesting the same data. SNPNCA is used to indicate that the current memory bus master will not cache the line, and the 82496 Cache Controller tag can remain in the [E] state (the 82496 Cache Controller need not put the line into [S] state). If SNPNCA is inactive, the 82496 Cache Controller tag state will change to [S] following the snoop operation.

To reduce bus traffic, SNPNCA should be asserted whenever snoops are initiated by accesses which are not cacheable - such as those from DMA controllers, cacheless CPUs, or caches which will not cache the line.

Table 5-10 summarizes the cache operations while SNPNCA is active (and SNPINV is inactive) during a snoop request.

Table 5-10. SNPNCA Asserted During Snoop Requests (Inactive SNPINV)

MESI State	Cache Operation
[M]	CPU is snooped and the Data written to bus (from either the Pentium™ processor or the 82491 Cache SRAMs), line placed in [E] state
[E]	Line remains in [E] state
[S]	Line remains [S] state
[I]	Cache miss, line remains in [I] state

When SNPNCA is not asserted, lines that are currently in the [M], [E], or [S] states are placed in the [S] state (if SNPINV is not asserted). Lines in [M] state cause a write back to the bus (from either the Pentium processor or the 82491 Cache SRAMs).

When Sampled

SNPNCA is sampled when SNPSTB# is sampled active. In synchronous snoop mode, SNPNCA is sampled on the rising edge of the first CLK in which SNPSTB# becomes active. In clocked mode, SNPNCA is sampled on the rising edge of the SNPCLK in which SNPSTB# becomes active. In strobed mode, SNPNCA is sampled on the falling edge of SNPSTB#.

SNPNCA is only sampled with SNPSTB#. SNPSTB# may be qualified by CLK, SNPCLK, or the falling edge of SNPSTB#, depending on the snoop mode, and must meet set-up and hold times to the edge being sampled. When SNPSTB# is not asserted, SNPNCA is a "don't care" signal and is not required to meet set-up and hold times.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
SNPINV	When SNPINV is asserted, it overrides SNPNCA and places all snoop hit lines into the [I] state.
SNPSTB#	SNPNCA is sampled with SNPSTB#, which may be qualified by SNPCLK or CLK, depending on the snoop mode

5.2.2.133. SNPSTB#

SNPSTB#	Snoop Strobe
	Initiates snoops, latches snoop address, address parity, and attributes.
	Input to 82496 Cache Controller (pin S04)
	Synchronous to CLK or SNPCLK, or asynchronous (Strobed Mode)
	Internal Pull-up

Signal Description

SNPSTB# initiates snoop requests. The signal latches the snoop address and snoop attribute signals as required by a particular snooping mode. The three snooping modes are listed in Table 5-11.

Table 5-11. Snooping Modes

Snoop Mode	When Snoop Address/Attributes Sampled
Strobed	Falling edge of SNPSTB#
Clocked	Rising edge of SNPCLK when SNPSTB# sampled active
Synchronous	Rising edge of CLK when SNPSTB# sampled active

SNPSTB# initiates a snoop request to the 82496 Cache Controller and latches the snoop address, address parity, and control signals. SNPSTB# is synchronized, or may be temporarily blocked to delay the snoop request. Once the snoop takes place, SNPCYC# is asserted, and MHITM# and MTHIT# are driven to indicate the result of the snoop.

Snoops may be pipelined by latching a new snoop before the first has completed. Pipelining is done by asserting SNPSTB# after SNPCYC# is driven for the previous snoop.

Once a snoop completes, the MESI state bits of the snoop address can change. The final state depends on the values of SNPINV and SNPNCA, and the current state of the line being snooped.

When Sampled

In clocked or synchronous snoop modes, SNPSTB# is sampled on every SNPCLK or CLK, respectively. In strobed mode, SNPSTB# is constantly sampled. In all snooping modes, once SNPSTB# is sampled active, it must be sampled inactive before another SNPSTB# is recognized.

When a snoop is in progress, a new SNPSTB# is recognized as a new snoop request or a pipelined snoop request. After a pipelined SNPSTB# is asserted, the SNPSTB# signal must not be reasserted until after the next SNPCYC#. In clocked and synchronous modes, SNPSTB# may not be asserted until the CLK after SNPCYC# is active. In strobed mode, SNPSTB# may not be asserted until after the falling edge of SNPCYC#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
MAOE#	If MAOE# is active when SNPSTB# is asserted, the snoop request is ignored.
MAP, MCFA, MSET, MTAG	SNPSTB# latches the 82496 Cache Controller address (MSET, MTAG, MCFA) and address parity (MAP) which is to be snooped.
MBAOE#	SNPSTB# latches MBAOE#, using MAOE# as a qualifier.
	If MBAOE# is active when SNPSTB# is asserted, the 82496 Cache Controller forces all bits in the sub-line address (the address bits controlled by MBAOE#) to 0 on a snoop write-back for a particular snoop and the snoop starts with sub-line address 0.
SNPCYC#	SNPSTB# must not be reasserted for a new snoop until after SNPCYC# is asserted for a previous snoop.
SNPINV	SNPSTB# latches SNPINV, using MAOE# as a qualifier. SNPINV and SNPNCA provide the 82496 Cache Controller with snoop attributes affecting the state of a snoop hit cache entry.
SNPNCA	SNPSTB# latches SNPNCA, using MAOE# as a qualifier. SNPINV and SNPNCA provide the 82496 Cache Controller with snoop attributes affecting the state of a snoop hit cache entry.
SWEND#	Snoops and memory accesses are interlocked. Once the 82496 Cache Controller is granted the bus (when BGT# is asserted), it is capable of latching snoop information with SNPSTB#, but does not execute the snoop (assert SNPCYC#) until after the snoop window closes (when SWEND# is asserted).

5.2.2.134. SWEND#

SWEND#	Snoop Window End
	Closes Snooping Window.
	Input to 82496 Cache Controller (pin R02)
	Synchronous to CLK
	Internal Pull-up

Signal Description

SWEND# closes the snooping window (which started with CADS#) by causing MWB/WT# and DRCTM# to be sampled. DRCTM# and MWB/WT# can be determined after the other C5Cs have been completely snooped.

The 82496 Cache Controller blocks snoop responses between BGT# and SWEND# activation. Accordingly, the sooner SWEND# is asserted, the faster snoop cycles can be completed.

All CPU-generated write cycles and cache read miss cycles cause memory bus snoops. SWEND# may be activated once snooping has completed for these cycles. SWEND# activation causes the internal tags of the 82496 Cache Controller cache controller to change state, as needed, for the current cycle. DRCTM# and MWB/WT# influence the state change decision.

When Sampled

SWEND# need only be active for cycles requiring DRCTM# and MWB/WT# to be sampled (i.e., cacheable read misses, allocations, and write cycles with potential upgrade).

If a cycle does not specifically require SWEND#, and SWEND# is not returned, snooping is blocked from BGT# to CRDY#. For this reason, it may be more efficient to always return SWEND#.

SWEND# should be issued with or after KWEND#, when KWEND# is applicable. For cycles that do not sample KWEND#, SWEND# is sampled with or after BGT#. Once SWEND# is sampled active, it is ignored until CADS# of the next cycle or CRDY# of the current cycle (the latest of the two).

Snoop response is blocked between BGT# and SWEND#. If a snoop is initiated between BGT# and SWEND#, then the snoop lookup (SNPCYC#) is performed 2 CLKs after SWEND# activation. Any subsequent snoop write-back begins after CRDY#.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BGT#	BGT#, KWEND# and SWEND# may be asserted in the same CLK.
CFG1	SWEND# shares a pin with CFG1.
DRCTM#	SWEND# causes MWB/WT# and DRCTM# to be sampled.
KWEND#	BGT#, KWEND# and SWEND# may be asserted in the same CLK.
	When KWEND# and SWEND# are applicable, they must fulfill the following precedence rule: KWEND# <= SWEND#
MWB/WT#	SWEND# causes MWB/WT# and DRCTM# to be sampled.

5.2.2.135. SYNC#

SYNC#	Synchronize
	Synchronizes the cache array with main memory.
	Input to 82496 Cache Controller (pin R05)
	Asynchronous
	Internal Pull-up

Signal Description

This signal causes the 82496 Cache Controller to write all modified second-level cache lines to main memory in order to synchronize them. At the end of the synchronize operation, the 82496 Cache Controller tag array is not invalidated. All shared [S] and exclusive [E] entries remain the same state, and modified [M] lines become unmodified [E] state lines and the lines are written back to main memory.

All 82496 Cache Controller modified lines cause an inquire cycle to the Pentium processor to determine if the Pentium processor contains more recently modified data. If so, the data from the CPU is written back to the 82491 Cache SRAM write back buffers and, sometimes, to the 82491 Cache SRAM cache array. The data from the 82491 Cache SRAMs is then written back to main memory.

To initiate a synchronize operation, the 82496 Cache Controller completes all pending cycles and prevents further assertions of ADS# while the synchronize operation is in progress. The FSIOUT# output signal indicates the start and end of the SYNC# operation. FSIOUT# becomes active when SYNC# is internally recognized (when all outstanding cycles have completed) and is de-activated when the synchronize operation has completed.

The 82496 Cache Controller can be snooped during SYNC# cycles, and the snooping protocols will be the same as with any memory bus cycle.

When Sampled

SYNC# can be asserted at any time. The 82496 Cache Controller completes all outstanding cycles on the CPU and memory bus before beginning the synchronize process. The memory bus controller does not have to prevent SYNC# during locked cycles because the 82496 Cache Controller completes the locked cycle before the synchronize operation begins.

Once a synchronize operation has begun, SYNC# is ignored until the operation completes. If RESET or FLUSH# is asserted while the synchronize operation is in progress, the operation is aborted and a reset or flush is executed immediately.

SYNC# is an asynchronous input. SYNC# must have a pulse width of two CLKs in order to ensure 82496 Cache Controller recognition.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
CADS#	Once SYNC# has begun, and FSIOUT# is active, all CADS# and CRDY# signals correspond with write-backs caused by the synchronize operation.
CRDY#	Once SYNC# has begun, and FSIOUT# is active, all CADS# and CRDY# signals correspond with write-backs caused by the synchronize operation.
FSIOUT#	The FSIOUT# output signal indicates the start and end of the SYNC# operation. FSIOUT# becomes active when SYNC# is internally recognized (when all outstanding cycles have completed) and is de-activated when the synchronize operation has completed.
	SYNC# is ignored while FSIOUT# is active.
MALDRV	SYNC# shares a pin with the MALDRV configuration input.

5.2.2.136. TCK

TCK	Test CLK
	JTAG boundary scan test Clock.
	Input to Pentium processor (pin T04), 82496 Cache Controller (pin Q04), and 82491 Cache SRAM (pin 3)
	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM internal Pull-ups

Signal Description

TCK provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the Pentium processor, 82496 Cache Controller and 82491 Cache SRAM components. State select information and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the Pentium processor CPU-Cache Chip Set on the falling edge of TCK on TDO.

In addition to using TCK as a free running clock, it may be held in a LOW state indefinitely as described in IEEE 1149.1. While TCK is held in the LOW state, the boundary scan latches retain their state.

When boundary scan is not used, TCK should be tied low.

When Sampled

TCK is a clock signal and is used as a reference for sampling other boundary scan signals.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
TDI	TMS and TDI are sampled on the rising edge of TCK.
TDO	TDO is driven on the falling edge of TCK.
TMS	TMS and TDI are sampled on the rising edge of TCK.

5.2.2.137. TDI

TDI	Test Data Input
	Receives serial test instructions and data.
	Input to Pentium processor (pin T21), 82496 Cache Controller (pin P04), and 82491 Cache SRAM (pin 2)
	Synchronous to TCK
	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM internal Pull-ups

Signal Description

TDI is the serial input used to shift JTAG instructions and data into the component. The shifting of instructions and data occurs during the SHIFT-IR and SHIFT-DR TAP controller states, respectively. These states are selected using the TMS signal as described in the testability chapter.

An internal pull up resistor is provided on TDI to ensure a known logic state if an open circuit occurs on the TDI path. Note that when the value 1 is continuously shifted into the instruction register, the BYPASS instruction is selected.

When Sampled

TDI is sampled on the rising edge of TCK, and during the SHIFT-IR and SHIFT-DR states. During all other TAP controller states, TDI is a "don't care".

Relation to Other Signals

Pin Symbol	Relation to Other Signals
TCK	TDI is only sampled when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.
	TMS and TDI are sampled on the rising edge of TCK.
TMS	TDI is only sampled when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.

5.2.2.138. TDO

TDO	Test Data Output
	Outputs serial test instructions and data.
	Output from Pentium processor (pin S21), 82496 Cache Controller (pin D05), and 82491 Cache SRAM (pin 84)
	Synchronous to TCK

Signal Description

TDO is the serial output used to shift JTAG instructions and data out of the component. The shifting of instructions and data occurs during the SHIFT-IR and SHIF-DR TAP controller states, respectively. These states are selected using the TMS signal as described in the testability chapter.

When not in the SHIFT-IR or SHIFT-DR state, TDO is driven to a HIGH impedance state to allow connecting TDO of different devices in parallel.

When Driven

TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the HIGH impedance state.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
TCK	TDO is only driven when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.
TMS	TDO is only driven when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.

5.2.2.139. TMS

TMS	Test Mode Select
	Controls testing by selecting operational mode.
	Input to Pentium processor (pin P19), 82496 Cache Controller (pin Q03), and 82491 Cache SRAM (pin 1)
	Synchronous to TCK
	Pentium processor, 82496 Cache Controller, 82491 Cache SRAM internal Pull-ups

Signal Description

TMS is decoded by the JTAG TAP (Test Access Port) controller to select the operation of the test logic, as described in the Testability chapter.

To ensure deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor. If boundary scan is not used, TMS may be tied HIGH or left unconnected.

When Sampled

TMS is sampled on every rising edge of TCK.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
TDI	TMS is used to select the internal TAP states required to load boundary scan instructions to data on TDI.
	TDI is only sampled when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.
TDO	TDO is only driven when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.

5.2.2.140. TRST#

TRST#	Test Logic Reset
	Allows the TAP controller to be asynchronously initialized.
	Input to Pentium processor (pin S18) and 82496 Cache Controller (pin T02)
	Asynchronous
	Pentium processor and 82496 Cache Controller internal Pull-ups

Signal Description

TRST# is a test logic control pin. When asserted, it will force the TAP controller into the Test Logic Reset State (see the TAP controller state diagram, Figure 11-3).

When in Test-Logic-Reset State, the test logic is disabled so that normal operation of the device can continue unhindered. During initialization, the Pentium processor or 82496 Cache Controller initializes the instruction register such that the IDCODE instruction is loaded.

On power up, the TAP controller is automatically initialized to the test logic reset state (test logic disabled), so normal Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM behavior is the default. The Test Logic Reset State is also entered when TRST# is asserted (Pentium processor or 82496 Cache Controller), or when TMS is high for 5 or more consecutive clocks (Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM).

When Sampled

TRST# is an asynchronous input.

Relation to Other Signals

None.

NOTE

Refer to the *Pentium™ Processor Data Book* for additional details.

5.2.2.141. W/R#

W/R#	Write or Read
	Indicates that the current cycle is a write or a read cycle.
	Output from Pentium processor (pin N03), Input to 82496 Cache Controller (pin C18), Input to 82491 Cache SRAM (pin 58)
	Synchronous to CLK

Signal Description

Refer to the *Pentium™ Processor Data Book* for a detailed description of this signal.

5.2.2.142. WAY

WAY	Way
	Indicates the way in which the current cache cycle is located.
	Output from 82496 Cache Controller (pin M16), Input to 82491 Cache SRAM (pin 45)
	Synchronous to CLK

Signal Description

WAY is driven to the 82491 Cache SRAM from the 82496 Cache Controller to indicate the way of the current cache cycle. If WAY is driven high, the cycle will access way one. If WAY is driven low, the cycle will access way zero.

The 82491 Cache SRAM samples WAY with WRARR# for normal write cycles and read hits which miss the MRU bit. The 82491 Cache SRAM samples WAY with MCYC# for read miss cycles. The 82491 Cache SRAM samples WAY with WBWE# for write back cycles.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
WRARR#	For write cycles, WRARR# qualifies the WAY input to the 82491 Cache SRAM to determine in which way the data will be written.

5.2.2.143. WB/WT#

WB/WT#	Write Back or Write Through
	Indicates that the current cache line can be exclusive or not.
	Output from 82496 Cache Controller (pin L15), Input to Pentium processor (pin M02)
	Synchronous to CLK

Signal Description

WB/WT# provides the 82496 Cache Controller/82491 Cache SRAM to Pentium processor cache consistency protocol. It informs the processor if the current line can go to the [E] state (e.g. write back) or must go to the [S] state (e.g. write through).

WB/WT# is used to ensure that the 82496 Cache Controller will always be aware of Pentium processor potentially modified lines. The 82496 Cache Controller will only allow the Pentium processor to go into exclusive states if the 82496 Cache Controller itself is making a transition from [E] to [M] states or is already in [M] state (e.g. from a previous cycle with DRCTM# asserted). This ensures that for any Pentium processor exclusive line ([E] or [M]), the 82496 Cache Controller will be in a modified state.

The 82496 Cache Controller drives WB/WT# HIGH to the Pentium processor in the following cases:

1. Write cycle to an 82496 Cache Controller line in Exclusive or Modified states.
2. Read cycle to an 82496 Cache Controller line in Modified state.

The 82496 Cache Controller drives WB/WT# LOW for all other CPU-initiated cycles.

When Driven

WB/WT# is valid with either NA# or the first BRDY# of the cycle (whichever comes first).

Relation to Other Signals

Pin Symbol	Relation to Other Signals
BRDYC# NA#	WB/WT# is valid with either NA# or the first BRDY# of the cycle (whichever comes first).

5.2.2.144. WBA

WBA	Write Back Buffer Address
	Indicates which line is loaded into replacement write back buffer.
	Output from 82496 Cache Controller (pin N15), Input to 82491 Cache SRAM (pin 38)
	Synchronous to CLK

Signal Description

WBA is driven to the 82491 Cache SRAM to indicate which line will be written back during the replacement write back. If the 82496 Cache Controller uses 2 lines per sector, WBA distinguishes to the 82491 Cache SRAM which line is to be written back. WBA low selects line 1 and WBA high selects line 2.

In configurations with 1 line per sector (1,2,4,5), WBA is driven low to the 82491 Cache SRAM during write back cycles. In configurations with 2 lines per sector (3), WBA indicates which line in the sector is being accessed. If WBA is low, the first line in the sector is being accessed. If WBA is high, the second line in the sector is being accessed.

WBA is driven high to the 82491 Cache SRAM for snoop cycles which hit the replacement write back buffer and low for cycles which miss the replacement write back buffer.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
SEC2#	WBA shares a pin with the configuration signal SEC2#.
WBWE#	WBA and WBTYP are sampled by the 82491 Cache SRAM with WBWE#.

5.2.2.145. WBTYP

WBTYP	Write Back Cycle Type
	Indicates a replacement or snoop write back cycle.
	Output from 82496 Cache Controller (pin P16), Input to 82491 Cache SRAM (pin 37)
	Synchronous to CLK

Signal Description

WBTYP indicates the type of write back cycle to the 82491 Cache SRAM. This signal is used by the 82491 Cache SRAM to determine which buffer it will load the data to be written back into (either the snoop write back buffer or the replacement write back buffer).

If WBTYP is driven high for snoop write back cycles, and low for replacement write back cycles.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
LR0	WBTYP shares a pin with the configuration signal LR0.
WBWE#	WBA and WBTYP are sampled by the 82491 Cache SRAM with WBWE#.

5.2.2.146. WBWE#

WBWE#	Write Back Buffer Write Enable
	Indicates the write back buffers can be loaded.
	Output from 82496 Cache Controller (pin N16), Input to 82491 Cache SRAM (pin 39)
	Synchronous to CLK

Signal Description

WBWE# indicates to the 82491 Cache SRAM that the next access will be a write back (either a snoop write back from the snoop write back buffer, or a replacement write back from the replacement write back buffer). WBWE# will be active for 2 CLKs if the write back is a replacement of 2 lines (2 L/S mode), and for 1 CLK otherwise.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
LR1	WBWE# shares a pin with the configuration signal LR1.
WBA	WBA and WBTYP are sampled by the 82491 Cache SRAM with WBWE#.
WBTYP	WBA and WBTYP are sampled by the 82491 Cache SRAM with WBWE#.

5.2.2.147. WRARR#

WRARR#	Write to 82491 Cache SRAM Array
	Controls the writing of data into the 82491 Cache SRAM array and updating MRU bit.
	Output from 82496 Cache Controller (pin M15), Input to 82491 Cache SRAM (pin 44)
	Synchronous to CLK

Signal Description

WRARR#, when active, latches the WAY signal in the 82491 Cache SRAM to decide which way should be updated or what MRU value to write.

For read cycles which miss the MRU bit, the 82491 Cache SRAM will update the MRU bit 1 CLK after WRARR# is sampled active. The WAY signal value becomes the MRU value.

For write cycles, WRARR# qualifies the WAY input to the 82491 Cache SRAM to determine in which way the data will be written.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
WAY	For write cycles, WRARR# qualifies the WAY input to the 82491 Cache SRAM to determine in which way the data will be written.

5.2.2.148. WWOR#

WWOR#	Weak Write Ordering Mode
	Enforces strong/weak write-ordering policy.
	Configuration input to 82496 Cache Controller (pin R03)
	Synchronous to CLK

Signal Description

When WWOR# is asserted during RESET, the 82496 Cache Controller enforces a weak write-ordering policy. If WWOR# is de-asserted during RESET, the 82496 Cache Controller enforces a strong write-ordering policy.

In strong write-ordering mode, memory bus writes occur in the order in which they were given by the CPU. In weak write-ordering mode, the following situation can arise:

1. A data from CPU posted write (Write A) resides in an 82491 Cache SRAM memory buffer
2. A subsequent CPU write (Write B) completes in the 82496 Cache Controller/82491 Cache SRAM's second-level cache because of a cache hit to a line in the [M] or [E] state
3. A snoop hit to B causes a write-back of the modified line from Write B before the line from Write A is written back.

Here, the line modified by Write B is written to memory before the data from Write A, causing a re-ordering of CPU writes. This scenario creates a potential operating system problem if Write A writes to a location locked by a semaphore which Write B unlocks prematurely.

The reordering does not take place if Write B unlocks the semaphore using a read-modify-write sequence.

When Sampled

WWOR# is sampled during RESET as shown in the Initialization and Configuration chapter. Following the falling edge of RESET, WWOR# becomes the MALE input.

Relation to Other Signals

Pin Symbol	Relation to Other Signals
RESET	WWOR# is sampled when RESET is active. Refer to Chapter 4 for specific timing requirements with respect to RESET.
EWBE#	If the 82496 Cache Controller is configured in the weak write ordering mode, EWBE# is always driven active to the CPU.
MALE	WWOR# shares a pin with MALE.

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6

Memory Bus Functional Description

CHAPTER 6
MEMORY BUS FUNCTIONAL DESCRIPTION

The 82496 Cache Controller/82491 Cache SRAM core supports a wide variety of bus transfers to meet the needs of high performance systems. Bus transfers can be single cycle or multiple cycle, cacheable or non-cacheable, 64- or 128-bit (memory bus width), and locked. Depending on the configuration, multiple cycle transfers may be either 4 or 8 transfer cycles. To support multiprocessing systems there are cache back-invalidation, inquire, snooping, read for ownership, cache to cache transfers, and locked cycles.

This chapter begins with read cycles, both cacheable and non-cacheable. It moves on to write cycles, cacheable and non-cacheable. Snooping, locked, and I/O cycles are also represented by examples in this chapter.

The cycles shown in this chapter are examples of various types of Pentium processor CPU-Cache Chip Set cycles. The purpose of these examples is to show signal relationships, and are not necessarily best case scenarios. Sample strobe mode inputs MISTB and MOSTB are indicated in the figures in this chapter for system designers implementing strobed memory bus mode.

6.1. READ CYCLES

6.1.1. Read Hit Cycles

Read Hit cycles are executed completely within the Pentium processor CPU-Cache Chip Set, and will not be seen by the MBC.

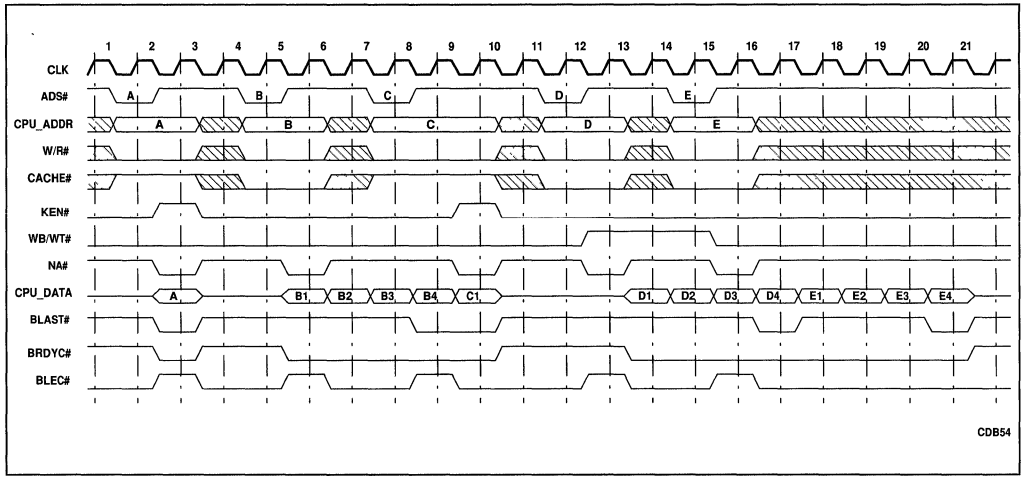


Figure 6-1. Pipelined Read Hits

Figure 6-1 illustrates a sequence of read hit cycles. It exemplifies MRU hits (A, B) and MRU misses (C, D, E). MRU (Most Recently Used) is the replacement algorithm used by the 82496 Cache Controller to determine in which set, sector, and line location a cache line will be placed.

Cycle A

Cycle A is a single transaction (length=1) non-pipelined read cycle. The 82496 Cache Controller executes a cache directory (TAGRAM) look-up and detects a cache hit with an MRU hit. Concurrently the 82491 Cache SRAM accesses the ARRAY, loads the CPU buffer with the contents of both ways corresponding to the selected set. Its internal way multiplexer selects the way pointed out by the 82491 Cache SRAM MRU bit (also corresponding to the selected set). The W/R# signal sampled low causes the 82491 Cache SRAM to drive its data pins onto the CPU data bus.

Since the 82496 Cache Controller detects an MRU hit, it activates the BRDYC# immediately after ADS# (i.e. zero wait-state access). Since CACHE# is sampled inactive (clock 1) and the BE# (byte enable) latch is empty (BLEC# active), the 82496 Cache Controller drives NA# immediately after ADS# (clock 2). Note that NA# is activated concurrently with the look-up execution (blind NA#); it is not affected by the look-up results. This NA# does not cause a pipelined cycle since it is activated with the last BRDYC#. In pipelined cycles, another ADS# is activated before or with the BLAST# and BRDYC# of the present one.

The BLAST# signal is sampled active by the 82491 Cache SRAM by the end of clock 2 (concurrently with the BRDYC#), indicating the end of the cycle. BLAST# is generated by the 82496 Cache Controller based on the CPU's burst length information (CACHE#).

Cycle B

In clock 4, the Pentium processor issues an ADS# (cycle B) with a burst length of four transactions. A CPU line-fill is executed in clocks 5-8 (burst length=4) since CACHE# was sampled active (clock 4). As a result of the blind NA# (clock 5), the CPU issues another ADS# (cycle C) in clock 7 (pipelined ADS#).

Cycle C

In clock 7 the CPU issues the ADS# for cycle D due to NA# activation in clock 5. As a result of the MRU miss, the 82496 Cache Controller the correct WAY to the 82491 Cache SRAM (using the WRARR# and WAY signals - not shown). Upon sampling WRARR# active, the 82491 Cache SRAM will update its internal MRU bit with the way information presented by the WAY signal. This information is also used by the 82491 Cache SRAM to select from its CPU buffer the data corresponding to the correct way. The 82491 Cache SRAM drives the CPU data bus by the end of clock 9. Note that the wait-state caused by the MRU miss is hidden due to the pipeline.

KEN# is driven high to the CPU in the CLK of BRDYC# active (clock 9) in response to the CACHE# signal being sampled inactive (clock 7).

Cycle D

In clock 11 (2 CLKs after the previous NA#), the CPU issues another pipelined ADS# (cycle D). In this cycle a wait-state is added (clock 12) due to the MRU miss. WB/WT# is driven high to the Pentium processor to indicate that the read hit was to a line in the Modified state.

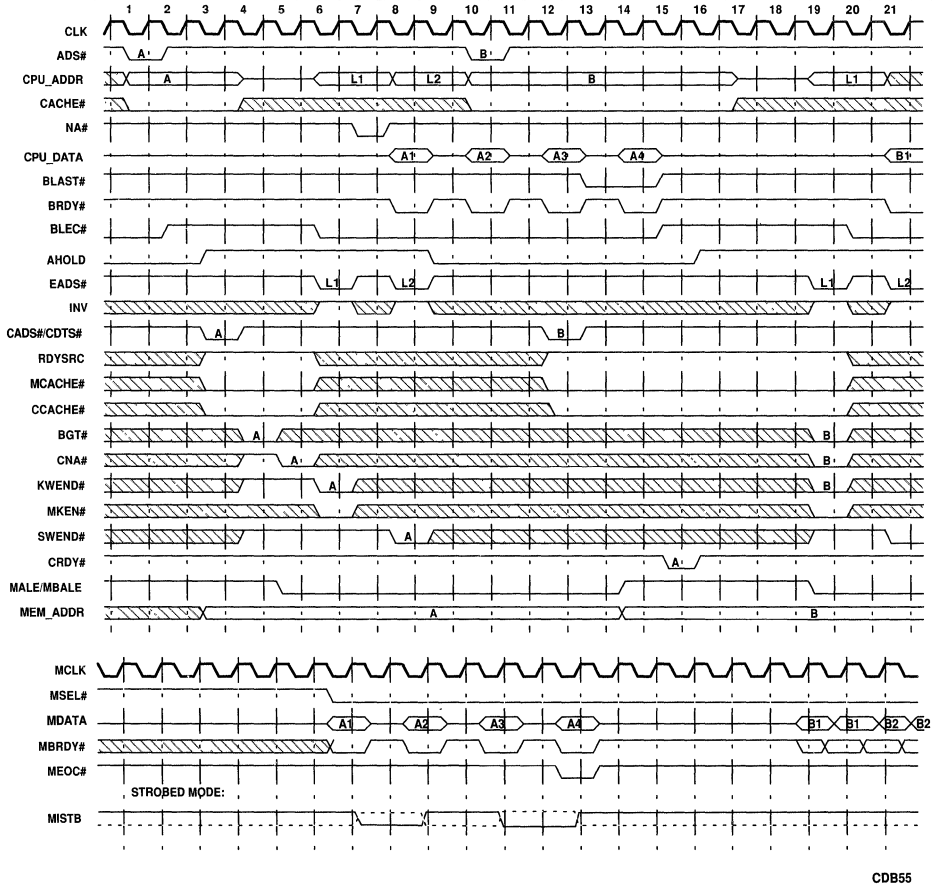
Cycle E

In clock 14 the CPU issues a pipelined ADS# (cycle E) due to a previous NA# (clock 12). CACHE# is sampled active (clock 14). Due to the 1.5 level of pipeline, the 82496 Cache Controller waits until the last BRDYC# of the previous cycle (Cycle D in clock 16) to begin the four transfers for cycle E.

Note that in all cycles BLEC# is deactivated immediately after ADS#. It activated again in the next clock, since all cycles are hits.

6.1.2. Read Miss Cycles

6.1.2.1. WITH CLEAN REPLACEMENT



NOTE: 1. In strobed mode MISTB is used in place of MBRDY to indicate data transfer onto the memory bus.

2. MCLK is asynchronous to CLK

Figure 6-2. Read Miss With Clean Replacement

Figure 6-2 illustrates CPU read cycles (A, B) that miss the 82496 Cache Controller . In such cycles, the 82496 Cache Controller will instruct the MBC (memory bus controller) to perform a cache line-fill cycle on the memory bus (a cache line-fill is a read of a complete 82496 Cache Controller line from the main memory). The line is then written into the 82491 Cache SRAM ARRAY, and data transferred to the CPU as requested). If the line fetched from the main memory replaces a valid unmodified line (i.e. [E] or [S]), then a back-invalidation cycle is

performed on the CPU bus, in order to guarantee that the replaced data is also removed from the CPU internal cache, thus maintaining the inclusion property. Note that this example shows a line ratio of 2 82496 Cache Controller cache lines to 1 Pentium processor cache line.

In clock 1, the CPU issues an ADS# of a read cycle (cycle A). The 82496 Cache Controller looks-up the cache directory (TAGRAM) and finds the CPU request to be a cache miss. It then asserts CADS# (also CDTS#) and associated cycle control signals to the MBC (CW/R#, CM/IO#, CD/C#, CCACHE#, RDYSRC, MCACHE#), in order to schedule the cache line-fill execution. MCACHE# is active, indicating that the read miss is potentially cacheable by the 82496 Cache Controller (PCD is also inactive in clock 1). RDYSRC is active (high), indicating that the MBC will supply BRDYs to the CPU.

The 82496 Cache Controller will prepare the 82491 Cache SRAM for the cache line-fill cycle, by asserting the MCYC#, WAY, and BUS# signals. MCYC# indicates to the 82491 Cache SRAM that this cycle involves the memory bus. The 82491 Cache SRAM samples and latches WAY during MCYC# activation. BUS# indicates the 82491 Cache SRAM whould switch the data source from the ARRAY to the memory-cycle buffer.

Since the cache directory look-up indicates that a line is going to be replaced, AHOLD is driven active as a preparation for the CPU back invalidation (clock 3). The CPU address lines float in clock 4. Thus, the 82496 Cache Controller starts driving the first line address to be invalidated in clock 6, so it is valid with the setup time to clock 6.

The MBC arbitrates for the memory bus and returns BGT# (clock 4), meaning that the MBC accepts ownership of the memory bus to complete the current cycle from the 82496 Cache Controller.

When the memory bus has determined the cacheability attribute of the cycle, it drives the MKEN# signal accordingly. At this point the MBC drives the KWEND# signal, indicating the end of the cacheability window. The 82496 Cache Controller samples MKEN# during KWEND# (clock 6) and realizes that the cycle in progress is cacheable. This determination triggers the start of the back-invalidation (the 82496 Cache Controller waits for the cacheability determination, in order to avoid unnecessary back-invalidations, in case the line happens to be non-cacheable). With this determination, the 82496 Cache Controller also activates MAWEA# to inform the 82491 Cache SRAM to deposit the memory-cycle buffer content into the ARRAY upon CRDY# (clock 15). The actual physical write to the ARRAY takes place during clock 16.

In clocks 6 and 8, the 82496 Cache Controller drives EADS# and INV. INV indicates the CPU to invalidate the line if it hits its internal cache directory (line address is sampled by the Pentium processor during EADS#). After completing the back-invalidation, the AHOLD signal is deactivated (clock 9) and the CPU drives the address bus with the new ADS# (clock 10).

When the snoop window ends on the memory bus, the MBC activates the SWEND# signal. The 82496 Cache Controller samples MWB/WT# during SWEND# (clock 8) and updates the cache directory according to the consistency protocol. The closure of the snoop window also enables the MBC to start providing the CPU with data that has been collected in the 82491 Cache SRAM memory-cycle buffer. The MBC supplies BRDYs to the CPU via BRDY# signal (clocks 8, 10, 12, and 14). BRDY# is an input to the 82496 Cache Controller needed to track the burst continuation.

The 82496 Cache Controller deactivates BLEC# (clock 2) immediately after the ADS# in order to keep the byte enable information latched in the external latch. BLEC# remains inactive until

CNA# is sampled active (clock 5), indicating that the MBC is ready to schedule a new memory bus cycle. In case the MBC does not support a pipelined interface with the 82496 Cache Controller (CNA# always inactive), the BLEC# will remain inactive until CRDY# is sampled active. Note that after CNA# activation, cycle control signals are not guaranteed to be valid.

NA# (of cycle A) is activated after KWEND# (clock 6), in order to determine the state of KEN# to the CPU (since KEN# is sampled by the CPU with NA# or first BRDY#). Note that the CPU delays the new ADS# due to AHOLD activation.

The CPU issues an ADS# in clock 10 (cycle B). This read cycle also misses the cache directory. Since the 82496 Cache Controller already sampled CNA# active (clock 5) it activates a new CADS# (clock 12) before the CRDY# of the current memory bus cycle, (i.e. this cycle is pipelined in the MBC).

Note that once the cycle progress signals (BGT#, CNA#, KWEND#, SWEND#) of a cycle are sampled active, the 82496 Cache Controller ignore them until the CRDY# of that cycle. The 82496 Cache Controller does not pipeline the cycle progress signals, i.e for a pipelined access (cycle B), it will start sampling them (clock 16) after the CRDY# of the current memory bus cycle (A).

6.1.2.2. WITH REPLACEMENT OF MODIFIED LINE

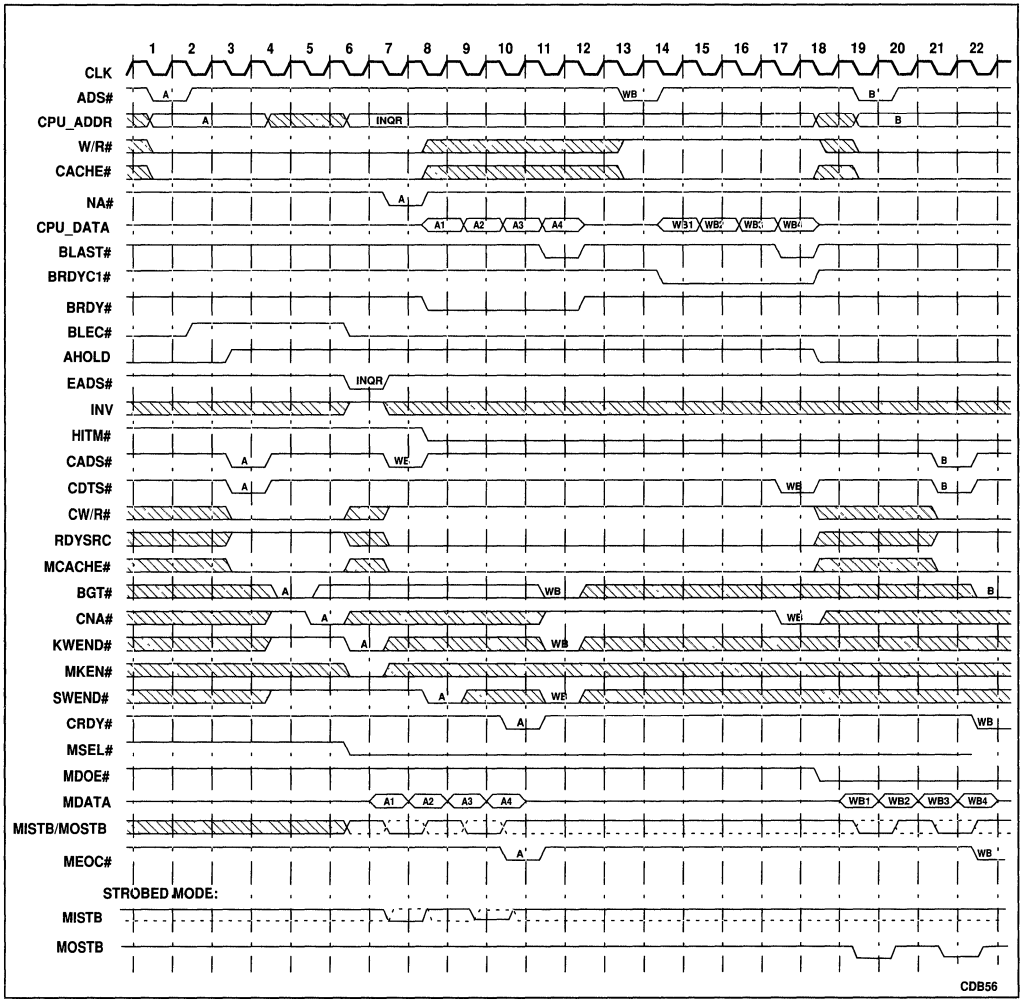


Figure 6-3. Read Miss with Replacement of Modified Line

Figure 6-3 illustrates CPU read cycles (A, B) that miss the 82496 Cache Controller cache, and require the replacement of two modified lines (tag replacement, lines/sector=1, line ratio=1).

In clock 1, the Pentium processor issues an ADS# of a memory read cycle. In clock 2, a miss is detected, so CADS# (also CDTS#) and cycle control signals are driven to the MBC on clock 3. BUS# and MCYC# are pulsed active to the 82491 Cache SRAM.

Since the cache directory look-up indicates that a modified line has to be replaced, AHOLD goes active in clock 3. After BGT# is received for the read cycle (clock 4), the 82491 Cache SRAM write-back buffer is prefilled with the contents of the ARRAY locations corresponding

to the lines to be replaced. The 82491 Cache SRAM will actually perform the reading from the ARRAY one clock after WBWE# is driven by the 82496 Cache Controller (which will be drive around clocks 5 or 6). WBTYP will be driven low to the 82491 Cache SRAM to indicate a write-back due to a replacement (WBTYP high indicates a write-back due to a snoop).

MKEN# is sampled active during KWEND# (clock 6), confirming the cacheability of the read cycle. Since the line being replaced is Modified, an inquire cycle starts. (waiting until the cacheability of the cycle is confirmed is necessary in order to avoid unneeded invalidations, i.e. if the cycle turns out to be non-cacheable).

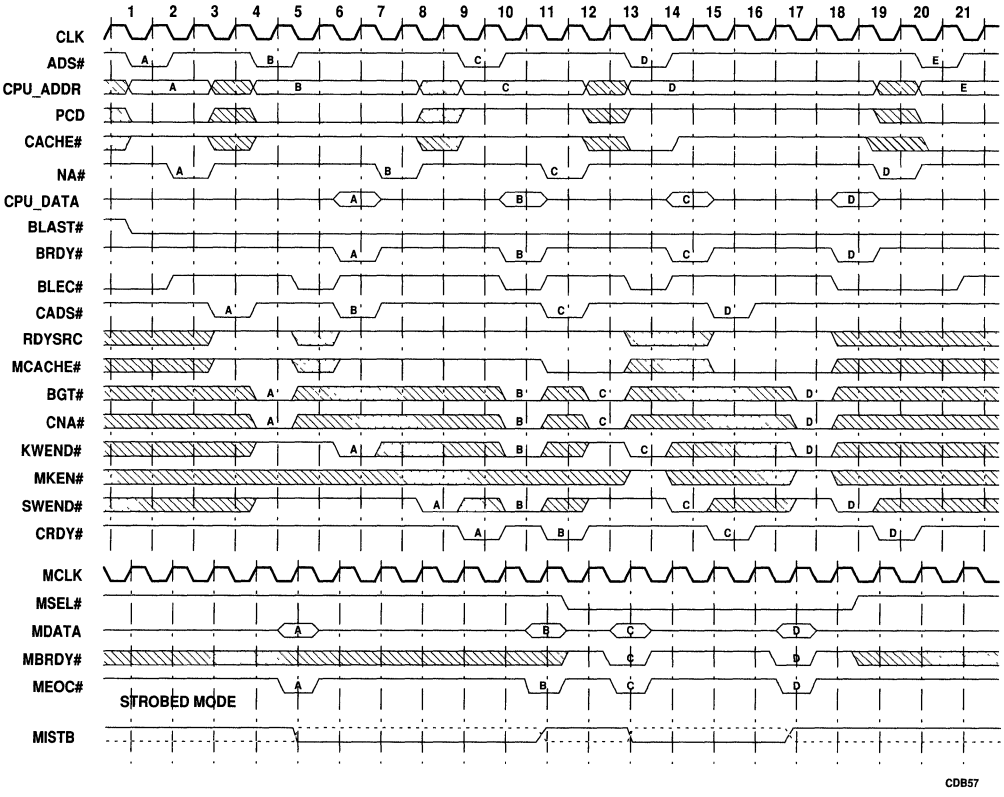
In clock 6, the line is inquired (the 82496 Cache Controller drives EADS# with active INV since it is a replacement case). In clock 8, HITM# is sampled active, indicating the line has been modified in the CPU.

After the snoop window closes, the MBC starts serving the CPU read cycle, which is completed in clock 11 (see BLAST#.BRDY#). In clock 13 the CPU starts flushing back the contents of the inquired line (WBTYP will be valid during the write back ADS# in order to inform the 82491 Cache SRAM where to load the inquired data: replacement write-back or snoop write-back buffer). The CPU data overwrites the corresponding 82491 Cache SRAM write-back buffer. With the BLAST#.BRDYC# (clock 17) of the CPU write-back cycle, the 82496 Cache Controller activates CDTS# meaning that all data is available in the 82491 Cache SRAM write-back buffer. AHOLD is deactivated (clock 18) one clock after BLAST#.BRDYC# of the CPU write-back cycle.

On the memory bus, the 82496 Cache Controller issues a write-back (WB) cycle. CNA# is sampled active in clock 5 causing the 82496 Cache Controller to issue the CADS# of the write-back (clock 7). Note that CDTS# is issued later after completing the CPU write-back cycle (clock 17). CNA# of a cycle can be activated only with or after CDTS# of that cycle. In this example, CNA# is activated together with CDTS#.

Following the completion of the write back cycle on the CPU bus (BLAST#.BRDYC1# in clock 17), a new read cycle (B) is issued in clock 19 with ADS#.

6.1.3. Non Cacheable Read Miss Cycles



NOTE:

1. In strobed mode, MISTB is used in place of MBRDY to indicate data transfer onto the memory bus.

Figure 6-4. Non Cacheable Read Miss

Figure 6-4 illustrates a sequence of pipelined read misses that are non-cacheable by the CPU. The first two cycles (A, B) are also non-cacheable by the 82496 Cache Controller (e.g. MCACHE# is inactive), while the other two (C, D) are potentially cacheable by the 82496 Cache Controller (active MCACHE#), but not cacheable by the memory bus (inactive MKEN# during KWEND#). This example assumes that cycles A and B are single transaction read misses (length=1), thus CACHE# is inactive. Cycles C and D are not cacheable due to an active cache disable bit in the current page table (PCD active).

Note the BLEC# signal. The 82496 Cache Controller deactivates BLEC# immediately upon detecting the CPU read request (clock 2) in order to keep the byte enable information latched

in the external latch. Upon receiving CNA# from the MBC (clock 4), BLEC# is activated again. This enables the sampling of a new cycle. (In case the MBC does not activate CNA#, BLEC# will be activated again only after CRDY#). Sampling the CNA# active causes the 82496 Cache Controller to drive the next read miss pending cycle (clock 6).

When the MBC drives BRDY#s to the CPU, the maximum level of pipelining is 1 since the 82496 Cache Controller has to sample the last BRDY# of the current CPU cycle in order to issue another NA#. NA# activation for the second read miss (cycle B) is delayed from clock 5 (blind NA#) to clock 7 (after sampling active BLAST#.BRDY#). This behavior of the NA# is also shown in the last cycle (D).

6.2. WRITE CYCLES

6.2.1. Write Hit to [E] or [M] State Cycles

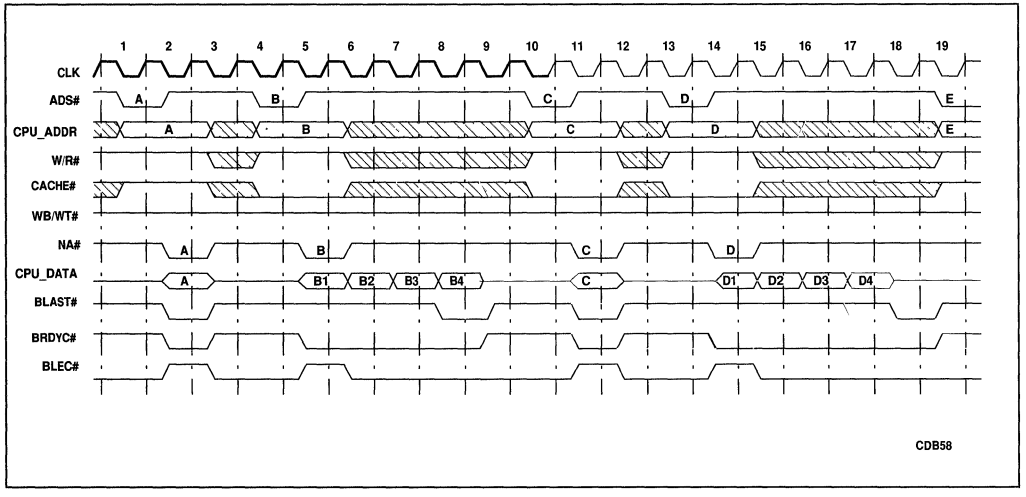


Figure 6-5. Write Hits to [E] or [M] State Cycles

Figure 6-5 illustrates a sequence of Pentium processor memory write cycles that hit 82496 Cache Controller entries marked in the [E] or [M] states. Such cycles are served by the 82496 Cache Controller by directly writing to the 82491 Cache SRAM ARRAY, without any memory bus activity. Note that the Pentium processor does not pipeline write-back cycles into previous CPU bus cycles, and will not pipeline a following CPU bus cycle into a Pentium processor data cache write-back cycle.

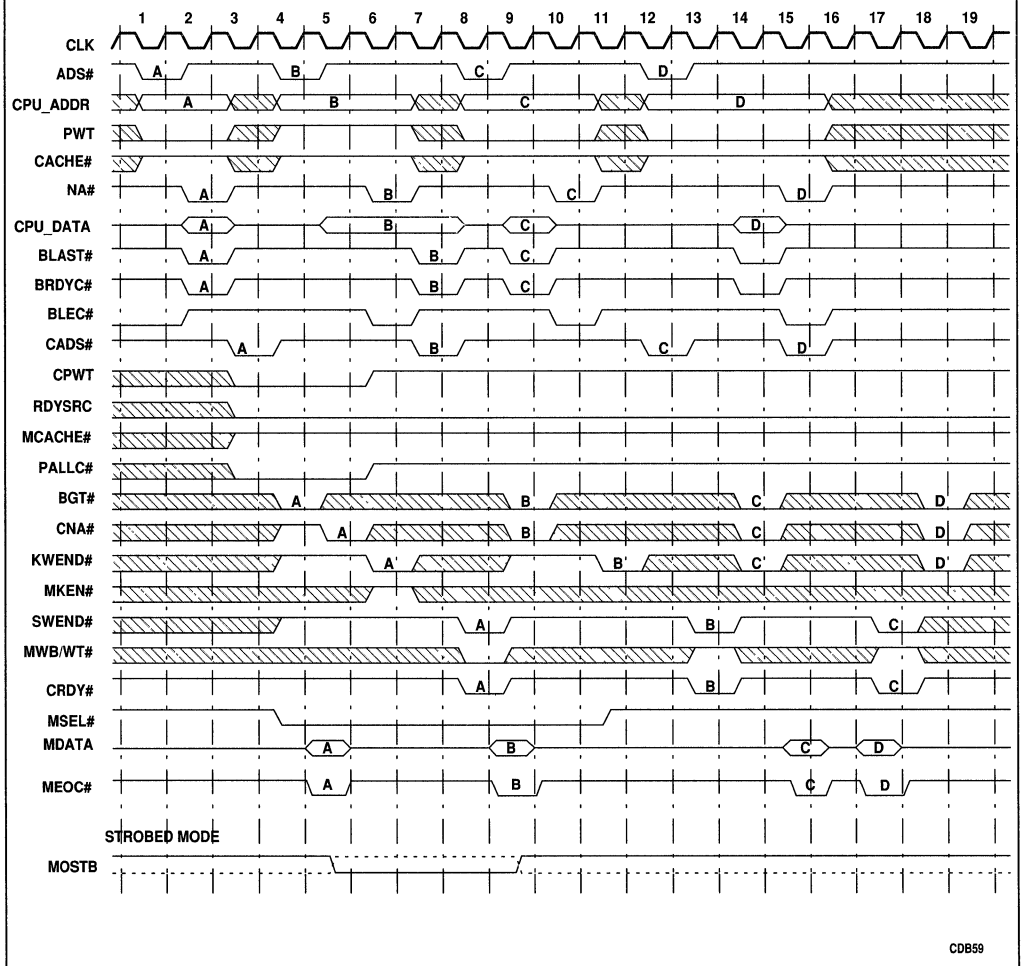
In clock 1, the first CPU write cycle (A) starts. The 82496 Cache Controller looks-up the cache directory (TAGRAM) and detects a hit to [E] or [M] states in clock 2. WRARR# is activated by the 82496 Cache Controller in preparation for the ARRAY write, and WAY points to the way to be written. The 82496 Cache Controller asserts BRDYC# in clock 2 (zero wait-state). Since the BLAST# is also active in clock 2, the 82491 Cache SRAM executes a write cycle into the ARRAY in the first half of clock 3.

In clock 4, the CPU issues a four transaction write-back (length=4). The first transfer is placed in the 82491 Cache SRAM buffer in clock 5, and the last in clock 8. BLAST# is activated with the fourth BRDYC#, indicating the completion of the cycle. Data is effectively written into the 82491 Cache SRAM ARRAY during the first half of clock 9.

Since the Pentium processor will not pipeline a new cycle into a write-back cycle, cycle C is issued in clock 10 (2 CLKs after BLAST#.BRDYC# for cycle B).

Cycles A, B, C, and D exemplify blind NA# assertion, thus the 82496 Cache Controller asserts NA# one clock after the ADS#.

6.2.2. Write Miss with No Allocation or Write Hit to [S] State Cycles



NOTE:

1. In strobed mode, MOSTB is used in place of MBRDY to indicate data transfer off of the memory bus.

Figure 6-6. Write Miss with No Allocation or Write Hit to [S] State Cycles

Figure 6-6 illustrates a sequence of pipelined posted write-through cycles. Cycles A and B exemplify memory writes that miss the 82496 Cache Controller directory, while C and D exemplify write hit to [S] state cycles in the 82496 Cache Controller tagram.

In clocks 1-3, the first write (cycle A) is posted in the 82491 Cache SRAM's memory-cycle buffer, which was empty prior to that time. The write is completed without wait-states. NA# is activated with the cache directory look-up (blind NA#), i.e. in clock 2. MCYC# is activated by the 82496 Cache Controller to indicate to the 82491 Cache SRAM that this cycle will involve the memory bus. In clock 3 CADS# and cycle control signals are issued. RDYSRC is low indicating that the 82496 Cache Controller is the source of the BRDY#s supplied to the CPU, (the MBC will not provide BRDY#s for this cycle). PALLC# is low indicating a potential allocate cycle after the write-through one. CNA# is active in clock 5 indicating that the MBC is free to accept a new CADS#. Nevertheless, the 82496 Cache Controller will not issue a new CADS# until after it resolves the allocatability of the current memory write cycle. Since MKEN# is inactive during KWEND# (clock 6), an allocation cycle will not be performed and a new write miss CADS# is issued in clock 7.

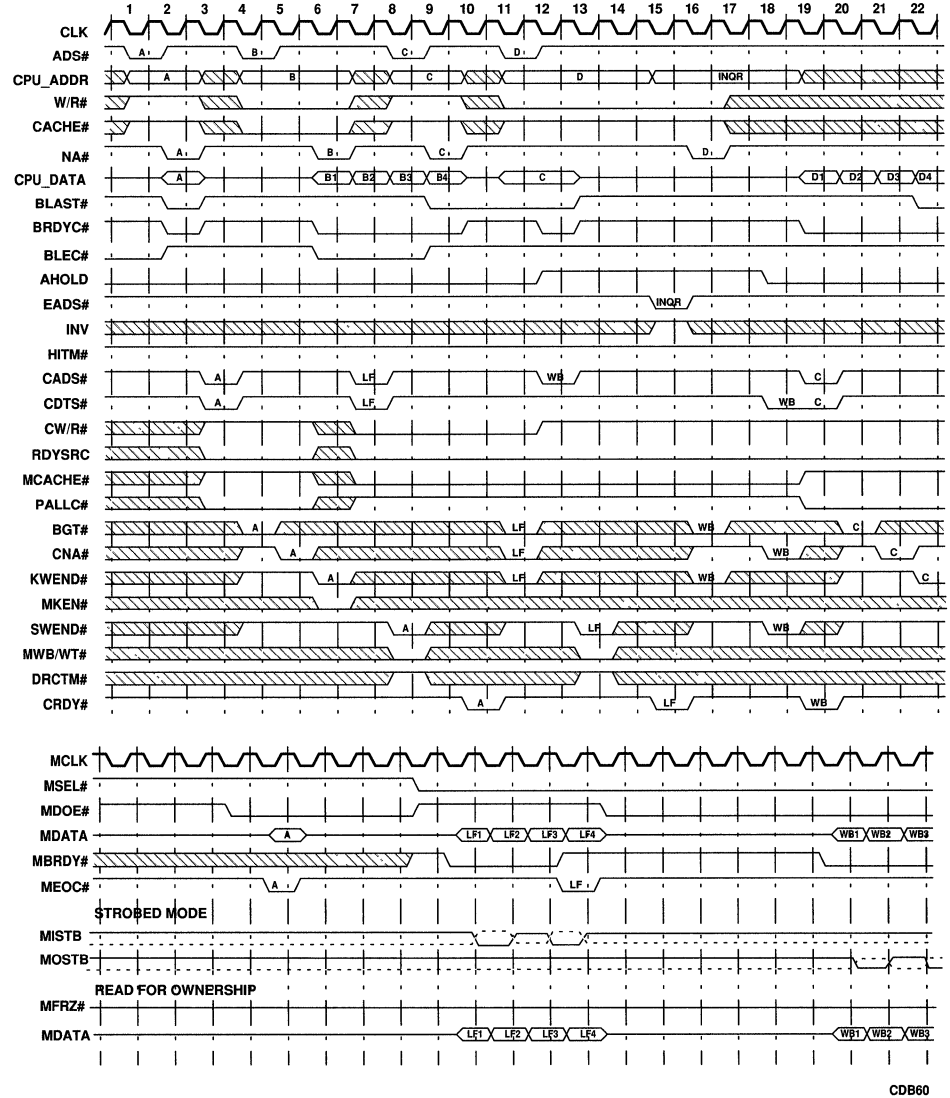
In clock 4, a new write cycle is requested by the CPU (cycle B). Since the memory-cycle buffer is busy, the first transfer is collected in the 82491 Cache SRAM's CPU buffer in clock 5. The 82496 Cache Controller posts the transfer after MKEN# is sampled inactive (during KWEND# in clock 6). If MKEN# was sampled active during KWEND#, then the transfer would be collected after the BGT# of the allocation cycle.

In clock 8, a new pipelined write is requested by the CPU (cycle C). Since this cycle is a write hit to [S] state, the data has to be written into the 82491 Cache SRAM's ARRAY. Thus, the WRARR# signal is activated by the 82496 Cache Controller to indicate to the 82491 Cache SRAMs that they must write the data at the end of the cycle, i.e. in the first half clock after sampling BLAST#.BRDYC# active. PALLC# is high indicating that an allocation cycle will not be performed (regardless of MKEN# state) since the line is already available in the cache. NA# is activated in clock 10 after sampling the CNA# of the previous memory cycle (clock 9).

In clock 12 a similar write hit to [S] state cycle is illustrated. For this cycle the 82496 Cache Controller issues the CADS# (clock 15) after sampling CNA# active (clock 14). The 82496 Cache Controller would not wait for KWEND# to provide CADS# since this is not a potential allocate cycle (PALLC# is high).

Note that the 82496 Cache Controller will drive the WB/WT# signal low for all cycles shown in this example to maintain the write once cache coherency protocol.

6.2.3. Write Miss with Allocation Cycles



NOTE:

1. In strobed mode, MISTB/MOSTB are used in place of MBRDY to indicate data transfer onto/off of the memory bus.

Figure 6-7. Write Miss with Allocation to Modified Line

Figure 6-7 illustrates a 82496 Cache Controller/82491 Cache SRAM write miss cycle which follows the write to main memory with an allocation cycle. The example assumes that allocating the new line requires the replacement of a modified line (write-back to main memory). This example displays a configuration of 1 line per sector and a line ratio of 1:1.

In clocks 1-3, the first write (cycle A) is posted in the 82491 Cache SRAM's memory-cycle buffer, which was empty prior to that time. The write is completed without wait-states. NA# is activated with the cache directory look-up (blind NA#), i.e. in clock 2. MCYC# is activated by the 82496 Cache Controller to indicate to the 82491 Cache SRAM that this cycle will involve the memory bus. In clock 3, CADS# and cycle control signals are issued. RDYSRC is low indicating that the 82496 Cache controller is the source of the BRDY#s supplied to the CPU (the MBC will not provide BRDY#s for this cycle). PALLC# is low indicating a potential allocate cycle immediately following the write-through cycle. CNA# is active in clock 5 indicating the MBC is free to accept a new CADS#. Nevertheless, the 82496 Cache Controller will not issue a new CADS# until after it resolves the allocatability of the current memory write cycle.

MKEN# is sampled active during KWEND# (clock 6), indicating that the missed line should be allocated in the 82496 Cache Controller/82491 Cache SRAM. Thus, the 82496 Cache Controller issues a second CADS# (LF) to request the line allocation (note MCACHE#, RDYSRC and CW/R#).

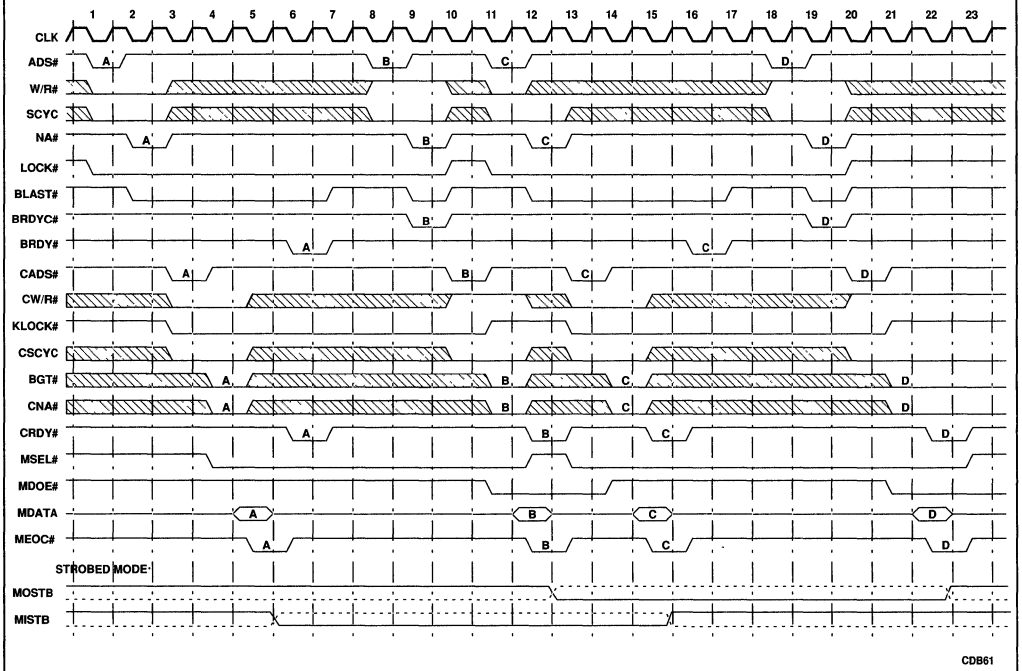
Concurrently with the memory bus write, the Cache Controller serves a CPU read hit (cycle B in clocks 4 to 9 — note the wait state in clock 10 due to the write-after-read back to back cycles on the CPU bus). In clock 8, the CPU starts a write cycle (C), but since it misses the cache, its service waits for the BGT# of the allocation. This wait is due to the fact that until BGT# activation, a snoop could happen, thus the usage of the 82491 Cache SRAM's CPU buffer is not allowed. The last BRDYC# of this cycle (C) can be issued only after the CRDY# of the allocation.

In clock 11, BGT# of the allocation is returned active. The cache controller activates AHOLD in clock 12 to inquire the CPU. The cache controller also drives WBWE#, WBTYP, and WBA to load the SRAM's write-back buffer from the ARRAY. The line is inquired in clock 15 (the 82496 Cache Controller drives the inquired address, activates INV and pulses EADS#). HITM# is sampled inactive in clock 17, so the data will come from the 82491 Cache SRAM's replacement write-back buffer. AHOLD is deactivated in clock 18 as a result of the Pentium processor cache miss (HITM# inactive).

The 82496 Cache Controller notifies the 82491 Cache SRAM on allocations by pulsing the MAWEA# signal after sampling an active MKEN# during KWEND# (clock 6). Note that the CDTS# of the write-back cycle is not asserted with CADS# since the data is not available in the 82491 Cache SRAM's write-back buffer till the BLAST#.BRDYC# of the inquire cycle or the CLK following HITM# results.

Cycle D (a read hit in the 82496 Cache Controller) is handled concurrently with the 82496 Cache Controller replacement write back and cycle C handling on the memory bus (clocks 11-22). The CPU bus data transfers for cycle D are delayed due to AHOLD assertion from the inquire cycle.

6.3. LOCKED READ-MODIFY-WRITE CYCLES



NOTE:

1. In strobed mode, MISTB/MOSTB are used in place of MBRDY to indicate data transfer onto/off of the memory bus.

Figure 6-8. Locked Read Modify Write Cycles

The 82496 Cache Controller provides a facility to allow atomic accesses (requested by the CPU, i.e. LOCK# is activated) through the KLOCK# signal. KLOCK# activation indicates to the MBC that the memory bus should not be released between the Klocked cycles. KLOCK# will remain active from the beginning of the first cycle (with CADS#) until CADS# is issued for the last cycle. This KLOCK# behavior allows the MBC to distinguish between back to back locked operations.

Figure 6-8 illustrates two back to back read-modify-write operations (A, B and C, D).

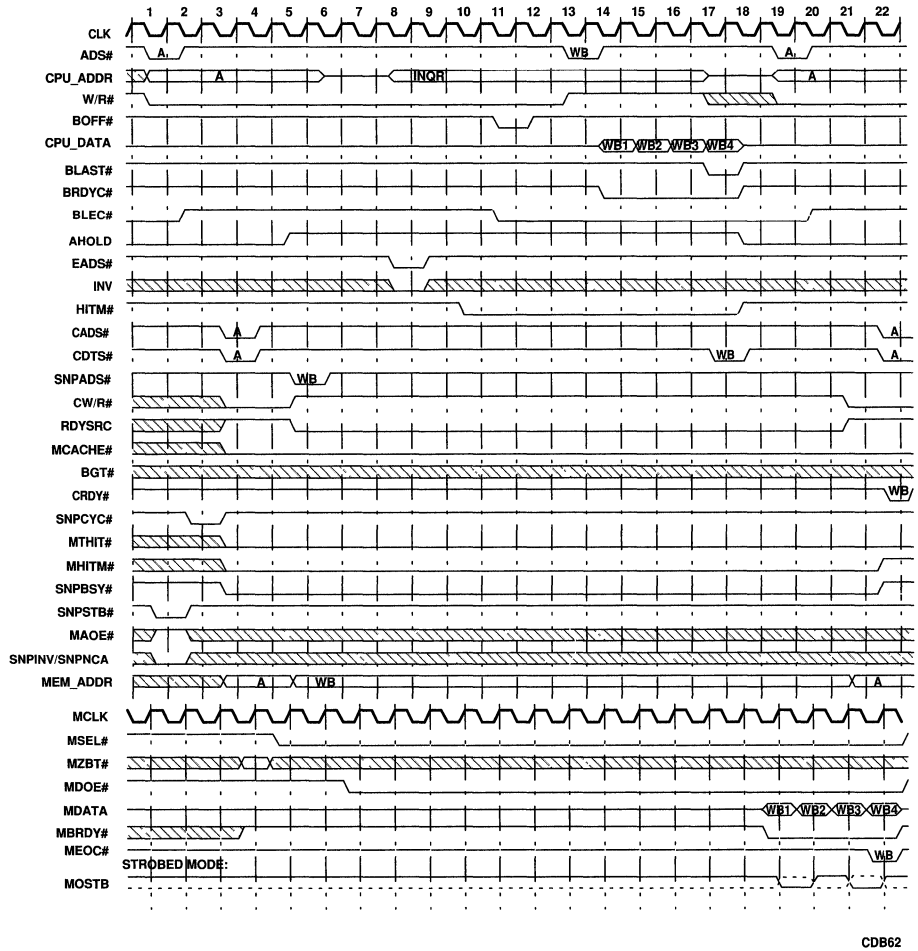
In clock 1, the Pentium processor issues a read cycle (A) with an active LOCK# signal. Since LOCK# is active, the 82496 Cache Controller issues a CADS# to the MBC with active KLOCK# (clock 3). The 82496 Cache Controller issues a request for memory bus access (CADS#) for every locked cycle (read or write) regardless of whether it hits the cache directory (TAGRAM). The MBC activates BRDY# (clock 6) and CRDY# (clock 6) but will not release the memory bus since the KLOCK# signal is active.

In clock 8, an ADS# of a write cycle is issued. Since this is the last locked cycle, LOCK# is deactivated one clock after BLAST#.BRDYC# (clock 10). The locked write is posted like any other memory write cycle, thus the 82496 Cache Controller supplies the BRDYC# to the CPU (clock 9). The 82496 Cache Controller issues CADS# with active KLOCK# for the write cycle (clock 10). Since LOCK# is deactivated, the 82496 Cache Controller deactivates KLOCK# one clock after CADS# (clock 11), indicating that the MBC can release the memory bus after completion of the current cycle.

In clock 11 a similar locked sequence starts (C,D). Since the last locked write was posted, a new ADS# is issued even before the CRDY# of that write (clock 12). The 82496 Cache Controller samples CNA# active (clock 11) and issues CADS# (clock 13). Note that the 82496 Cache Controller deactivates KLOCK# between unlocked operations for at least one clock (in this example it is inactive for two clocks: 11 and 12).

In this example, SCYC (and, correspondingly, CSCYC) would be inactive (low) with ADS# (CADS#) to indicate that the locked sequence is not split across a cache line boundary. If the cycle is split, there would be multiple read cycles followed by multiple write cycles for the split locked sequence.

6.4. SNOOP HIT TO [M] STATE - SYNCHRONOUS SNOOP MODE



NOTE:

1. In strobed mode, MOSTB is used in place of MBRDY to indicate data transfer off of the memory bus.

Figure 6-9. Snoop Hit to [M] State - Synchronous Snoop Mode

Figure 6-9 illustrates a snoop hit to [M] state sequence. This example assumes synchronous snooping mode, i.e. requests for snoop are done via SNPSTB# signal which is sampled by the 82496 Cache Controller's clock (not SNPCLK).

In clock 1, SNPSTB# is activated indicating the 82496 Cache Controller has a request for

snooping. The 82496 Cache Controller checks that MAOE# and MBAOE# are sampled inactive in order to recognize the snoop request. MAOE# is latched together with the snoop address (MSET[10:0], MTAG[11:0], MCFA[6:0], MAP), SNPINV and SNPNCA. These signals are latched by the 82496 Cache Controller's clock (not SNPCLK) rising edge, during SNPSTB# assertion. The look-up is done immediately after SNPSTB# (clocks 2-3) since snoops have the highest priority in the cache directory arbiter (TAGRAM arbitration). SNPCYC#, in clock 2, indicates that snoop look-up is in progress. The results of the look-up are driven to the memory bus via MTHIT# and MHITM# signals. Since the snoop hits a modified line, both signals are activated (clock 3). SNPBSY# is also driven active indicating the 82496 Cache Controller is busy with CPU bus inquires or the 82491 Cache SRAM's snoop buffer is full. The 82496 Cache Controller will accept snoops only when SNPBSY# is inactive.

Concurrently with the memory bus activity (snoop request), the CPU issues an ADS# of a read miss cycle (clock 1). The 82496 Cache Controller issues CADS#, CDTS# and cycle control signals to the MBC (clock 3). Note that the CPU request look-up is done with ADS# (clocks 1-2), while the snoop request look-up is done one clock after SNPSTB# (clocks 2-3). The MBC samples CADS# active and waits for the memory bus to execute the pending cycle.

In clock 5, the 82496 Cache Controller issues SNPADS# and cycle control signals to the MBC indicating a request to flush a modified line out of the cache. SNPADS# activation causes the MBC to abort the pending cycle. It is the 82496 Cache Controller's responsibility to re-issue the aborted cycle after the completion of the write back, since BGT# had not yet been activated on the CLK when SNPSTB# was sampled active.

The 82496 Cache Controller issues AHOLD (clock 5) causing the CPU to float its address lines. The 82496 Cache Controller issues WBWE#, WBTYP and WBA. WBTYP and WBA would be active (high) indicating to the 82491 Cache SRAMs that a snoop hit to the ARRAY occurred. The 82491 Cache SRAM performs an ARRAY read cycle in clock 6 and thus requires stable address and WAY at that time. Data is loaded into the 82491 Cache SRAM's snoop buffer one clock after the ARRAY read cycle.

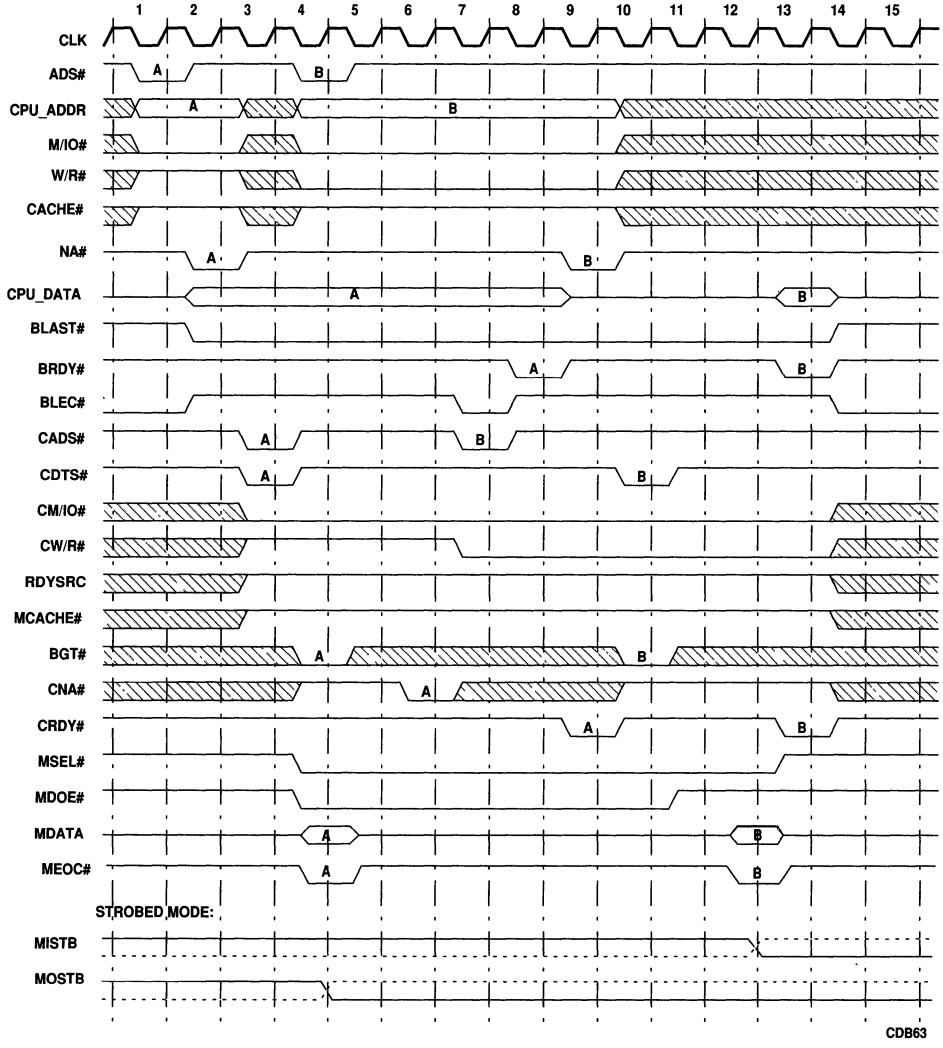
The 82496 Cache Controller drives the snoop address to the CPU bus (clocks 8-16). EADS# is activated (clock 8) in order to inquire the CPU. Since SNPINV was sampled inactive while SNPSTB# (clock 1), the 82496 Cache Controller issues an inactive INV with EADS#. Thus modified data from the CPU (clocks 14-17) will be written into both the ARRAY and snoop buffer. HITM# is activated in clock 10 indicating that the line has been modified in the CPU cache. AHOLD remains active until the inquire sequence completion. Thus AHOLD is deactivated in clock 18 after the BLAST#.BRDYC# of the Pentium processor write-back cycle. If HITM# would be sampled inactive in clock 10 then AHOLD would be deactivated one clock after that, i.e. in clock 11.

Since the CPU waits for the read miss (cycle A) to be completed in order to provide the modified data, and the MBC waits for the memory bus to execute the pending read miss (i.e. 82496 Cache Controller write-back has to be completed), a deadlock occurs. To avoid this deadlock, the 82496 Cache Controller issues BOFF# in clock 11, causing the CPU to abort the read miss cycle. After BOFF# is deactivated (clock 12), the CPU issues a write-back cycle (ADS# in clock 13) in order to flush the modified data out of the cache. The 82496 Cache Controller provides BRDY#s to the CPU in clocks 14-17. Note that WRARR# is activated, indicating to the 82491 Cache SRAM that it must write the data to the ARRAY. With the BLAST#.BRDYC#, the 82496 Cache Controller activates CDTS# (clock 17) indicating to the MBC that data is available in the snoop buffer.

The CPU does not guarantee that the same cycle which was aborted will be issued after completing the inquire sequence. Thus, BLEC# is activated together with the BOFF# (clock 11). BLEC# is deactivated again (clock 20) after sampling the re-issued (in this example) ADS# in clock 19.

After the Pentium processor write-back has completed (clock 17), the CPU issues (in this example, re-issues) the read miss cycle (clock 19). In clock 21 the MBC activates CRDY# indicating the 82496 Cache Controller the completion of the write-back cycle on the memory bus. As a result, the 82496 Cache Controller deactivates SNPBSY# (clock 22) and issues the pending read miss cycle (activates CADS#, CDTS# in clock 22).

6.5. I/O CYCLES



NOTE:

1. In strobed mode, MISTB/MOSTB are used in place of MBRDY to indicate data transfer onto/off of the memory bus.

Figure 6-10. I/O Cycles

Figure 6-10 illustrates I/O write (cycle A) and read (cycle B) accesses. An I/O write is the only write cycle that is not posted by the 82496 Cache Controller, i.e. the cycle is not fully acknowledged to the CPU until it is completed on the memory bus.

In clock 1, the Pentium processor issues an ADS# of an I/O write cycle. In clock 3 the 82496 Cache Controller issues CADS# (also CDTS#) with all cycle control signals. RDYSRC is high indicating the MBC to supply BRDY#s to the CPU. The MBC activates BRDY# (clock 8) to both the 82496 Cache Controller and the CPU. CRDY# is activated in clock 9 indicating to the 82496 Cache Controller the completion of the cycle on the memory bus. The 82496 Cache Controller can pipeline I/O cycles, i.e CNA# is recognized during all I/O cycles. Note that BLEC# is activated either after CNA# (cycle A, clock 7), or after CRDY# (cycle B, clock 14).

In clock 4, the CPU issues an ADS# of an I/O read cycle. This cycle is similar to non-cacheable read miss cycles with burst length = 1, i.e CACHE# is high. Upon completing the access on the memory bus, the MBC activates BRDY# (since RDYSRC is high) and CRDY#. Note that BRDY# of a cycle may come before (cycle A), with (cycle B), or after the CRDY# of the same cycle.

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7

Electrical Specifications

CHAPTER 7
ELECTRICAL SPECIFICATIONS

7.1. POWER AND GROUND

For clean on-chip power distribution, the Pentium processor has 50 Vcc (power) and 49 Vss (ground) inputs. The 82496 cache controller has 56 Vcc (power) and 67 Vss (ground) inputs and the 82491 cache SRAM has 9 Vcc (power) and 9 Vss (ground) inputs. Power and ground connections must be made to all external Vcc and Vss pins of the Pentium processor, 82496 cache controller, and 82491 cache SRAM. On the circuit board, all Vcc pins must be connected to a Vcc plane. All Vss pins must be connected to a Vss plane.

7.2. DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Pentium processor and 82496 cache controller/82491 cache SRAM second level cache. The CPU Cache Chip Set driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors (i.e. surface mount capacitors) and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by connecting capacitors directly to the Vcc and Vss planes, with minimal trace length between the component pads and vias to the plane. Capacitors specifically for PGA packages are also commercially available.

These capacitors should be evenly distributed among each component. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

7.3. CONNECTION SPECIFICATIONS

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to Vcc. Unused active high inputs should be connected to ground.

7.4. MAXIMUM RATINGS

Table 7-1 is a stress rating only. Functional operation at the maximums is not guaranteed. Functional operating conditions are given in the A.C. and D.C. specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor, 82496 cache controller, and 82491 cache SRAM contain

protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 7-1. Absolute Maximum Ratings

Case temperature under bias.	-65°C to 110°C
Storage temperature	-65°C to 150°C
Voltage on any pin with respect to ground	-0.5 Vcc to Vcc + 0.5 (V)
Supply voltage with respect to Vss	-0.5V to +6.5V

7.5. D.C. SPECIFICATIONS

Table 7-2 lists the D.C. specifications associated with the CPU Cache Chip Set.

Table 7-2. D.C. Specifications

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

V_{CC} = 5V ± 5%, T_{CASE} = 0 to +85 °C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	-0.3	+0.8	V	TTL Level (6) (15)
V_{IH}	Input High Voltage	2.0	Vcc+0.3	V	TTL Level (6) (15)
V_{OL}	Output Low Voltage		0.45	V	TTL Level (1) (6)
V_{OH}	Output High Voltage	2.4		V	TTL Level (2) (6)
I_{CC}	Power Supply Current		3200 2910 900 850 400 365	mA	PP 66 MHz (7) (12) PP 60 MHz (13) CC 66MHz (7), (4) CC 60 MHz (7) (4) CS 66 MHz (3), (9) CS 60 MHz (3) (9)
I_{LI}	Input Leakage Current		±15	uA	$0 \le V_{IN} \le V_{CC}$ (8)
I_{LO}	Output Leakage Current		±15	uA	$0 \le V_{OUT} \le V_{CC}$ (8) Tristate
I_{IL}	Input Leakage Current		-400	uA	V_{IN} = 0.45V, (5)
I_{IH}	Input Leakage Current		200	uA	V_{IN} = 2.4V, (10)
C_{IN}	Input Capacitance		15 11 5	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)
C_O	Output Capacitance		20 22 --	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)
$C_{I/O}$	I/O Capacitance		25 17 10	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)
C_{CLK}	CLK Input Capacitance		7 7 7	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)
C_{TIN}	Test Input Capacitance		15 9 5	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)
C_{TOUT}	Test Output Capacitance		15 14 7	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)
C_{TCK}	Test Clock Capacitance		7 9 5	pF pF pF	PP, (11) (14) CC, (11) (14) CS, (11) (14)

NOTES:

(1) Parameter measured at 4mA load.

For MCFA6-MCFA0, MSET10-MSET0, MTAG11-MTAG0, and MBT3-0, this parameter is measured at 12 mA load.

(2) Parameter measured at 1mA .

For MCFA6-MCFA0, MSET10-MSET0, MTAG11-MTAG0, and MBT3-0, this parameter is measured at 2 mA load.

(3) 82491 cache SRAM Icc may be considerably less depending on cycle mix. (For example, idle clocks only require approximately 75mA)

(4) Typical 82496 cache controller Supply current is 800 mA at 66 MHz and 750 mA at 60 MHz.

(5) This parameter is for input with pullup.

(6) TTL levels used for external interface signals.

(7) Worst case average Icc for a mix of test patterns.

(8) This parameter is for input without pullup or pulldown.

(9) Typical 82491 cache SRAM Supply current is 250 mA at 66 MHz and 230 mA at 60 MHz, assuming a typical cycle mix of: 50% Read Hit - MRU Hit Burst=4, 20% Write Hit Burst=4, 30% Idle.

(10) This parameter is for input with pulldown.

(11) For additional granularity, refer to the I/O models.

(12) (16 W max.) Typical Pentium processor supply current is 2600 mA (13 W) at 66 MHz.

(13) (14.6 W max.) Typical Pentium processor supply current is 2370 mA (11.9 W) at 60 MHz.

(14) Not 100% tested..Guaranteed by design/characterization.

(15) V_{IL} min and V_{IH} max are not 100% tested. Guaranteed by design/characterization.

7.6. A.C. SPECIFICATIONS

The A.C. specifications consist of two sections, Optimized and External interface specifications.

7.6.1. Optimized Interface

The optimized interface is the high-performance interconnect between the Pentium processor, 82496 cache controller and 82491 cache SRAM. This interface is tuned for the known configuration options of the chip set and includes specially designed (non-standard) input and output buffers optimized for the defined electrical environment of each signal path. The specification of this interface is also non-standard; this section describes the signal flight times, signal quality and buffer types parameters used throughout this interface.

The specifications that follow define the requirements of each path in the optimized interface. As outlined in Table 7-3 there are three classes of specifications: flight time to guarantee signal timing; signal quality to guarantee reliable operation; and, buffer models to specify completely flight time and signal quality. Tables 7-3 - 7-17 define the optimized interface for the **256 Kbyte and 512 Kbyte configurations of the CPU-Cache Chip Set.**

Table 7-3. Three Specification Classes, Their Purpose and the New Parameters

Specification Class	Purpose	Parameters
Flight Time	Guarantee Timing	Maximum Flight Time
Signal Quality	Guarantee Reliable Operation	Absolute Maximum Signal Overshoot (Undershoot) Maximum Group Average Overshoot (Undershoot) Absolute Maximum Time Beyond the Supply Maximum Group Average Time Beyond the Supply Maximum Signal Ring-back Maximum Settling Time
Buffer Models	Completely Specify Flight Time and Signal Quality	Cin - Input Capacitance Lp - Package Inductance Cp - Package Capacitance dV/dt - Voltage source rate of change Ro - Output impedance Co - Output Capacitance

7.6.1.1. FLIGHT TIME SPECIFICATION

The first new parameter is flight time. Flight time is the difference in output delay measured between a loaded and an unloaded output buffer.

The most straight forward definition of flight time is the time difference between the loaded and unloaded output signals at the 50% Vcc voltage level as illustrated in Figure 7-1 (50% Vcc is the normal CMOS switching threshold. The loaded delay must be measured at the last receiver to cross this threshold). This delay is called the 50% delay time.

Unfortunately, it is also necessary to measure delays to the 65% Vcc voltage level (or 35% Vcc for falling transitions). This is due to differences between waveforms generated in the actual system and for an unloaded buffer, which are caused by the transmission line nature of the system environment. Delays measured to the 65% Vcc level must be extrapolated back to the 50% Vcc level using a line with a 1V/ns slope(i.e. subtract 0.75 ns when Vcc=5V), as shown in Figure 7-2. This delay is called the 65% delay time.

Flight time is defined as the greater of the 50% delay or that obtained by extrapolation from the 65% delay.

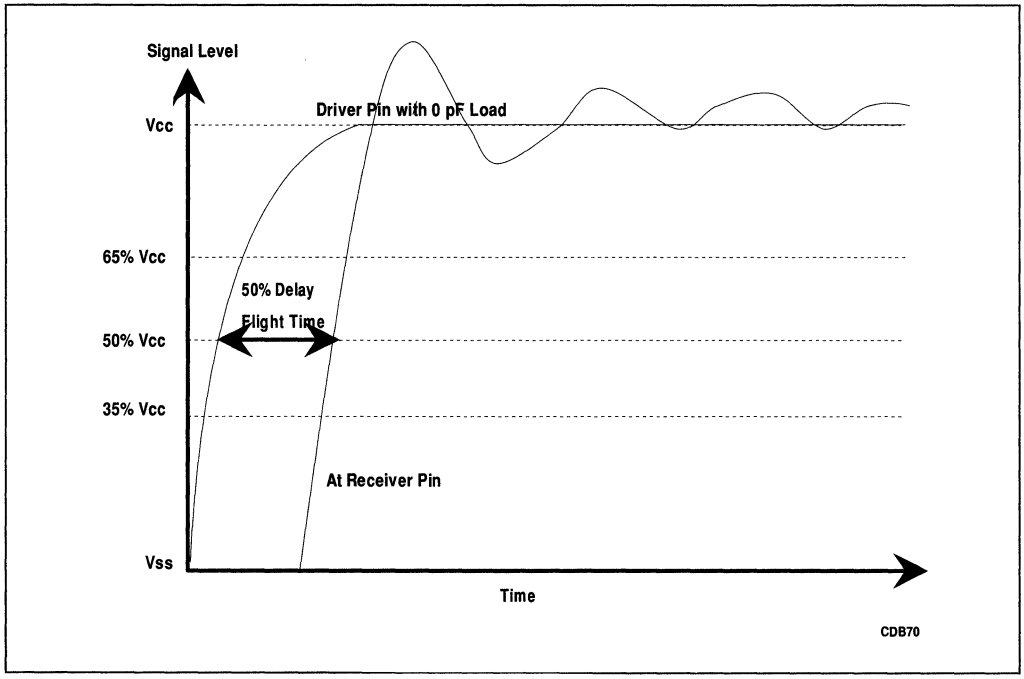


Figure 7-1. Determination of Flight Time

Figure 7-1 shows determination of flight time based on the 50% Vcc level measurement of a 0 pF load output with reference to the 50% Vcc level of at the receiver pin. The 50% Vcc to 65% Vcc rise time is faster than 1 volt/nsec in this example.

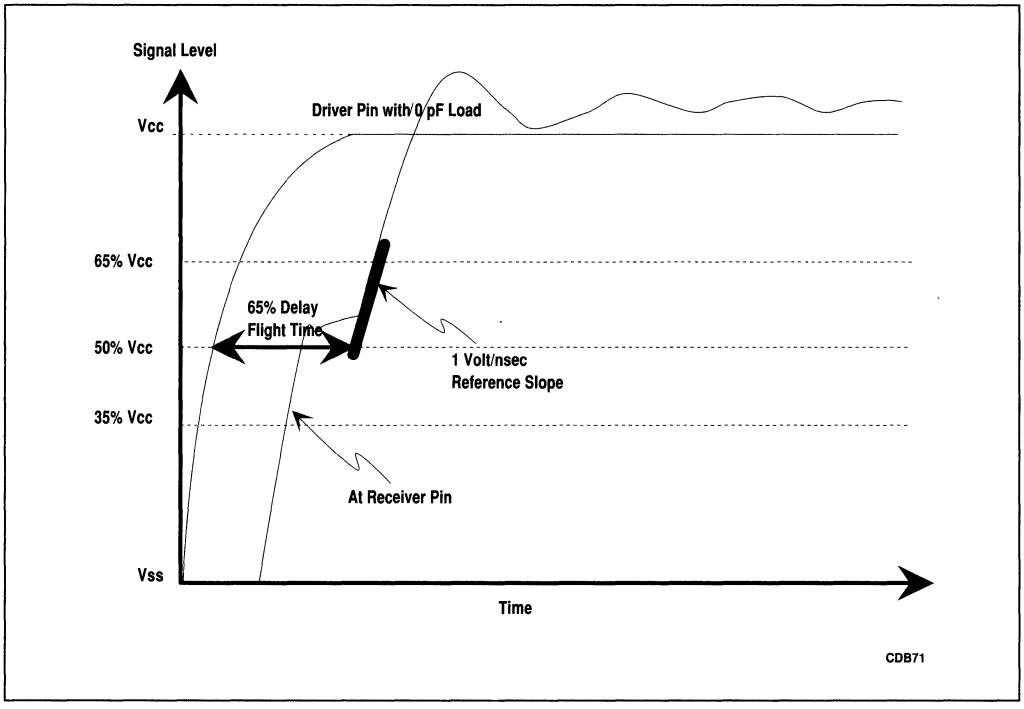


Figure 7-2. Derating the Flight Time

In a system environment it will not usually be possible to measure the delay of an unloaded driver. Figure 7-3 shows the method for measuring flight time in a system environment. As shown, the voltage measured at the pin of the loaded driver will have a ledge near the center of the transition. According to Transmission Line Theory, the time required to reach half the voltage level of the ledge is equivalent to the time required for an unloaded driver to reach the 50% Vcc level. The oscillation (if any) seen at the ledge defines the measurement uncertainty for this technique.

To measure flight time via this technique, first measure the maximum and minimum voltages of the ledge and take the average of these two values, (Vmax + Vmin) / 2, to arrive at the ledge voltage. Finally, divide the ledge voltage by two, (Vmax + Vmin) / 4. The result is the voltage level that approximately corresponds to the point in time at which an unloaded driver's signal would reach the 50% Vcc level. The flight time is determined by measuring the difference in time between the (Vmax + Vmin) / 4 point and the extrapolated 50% point on the receiver. The uncertainty of this technique is the time difference between the Vmin/2 and Vmax/2 points.

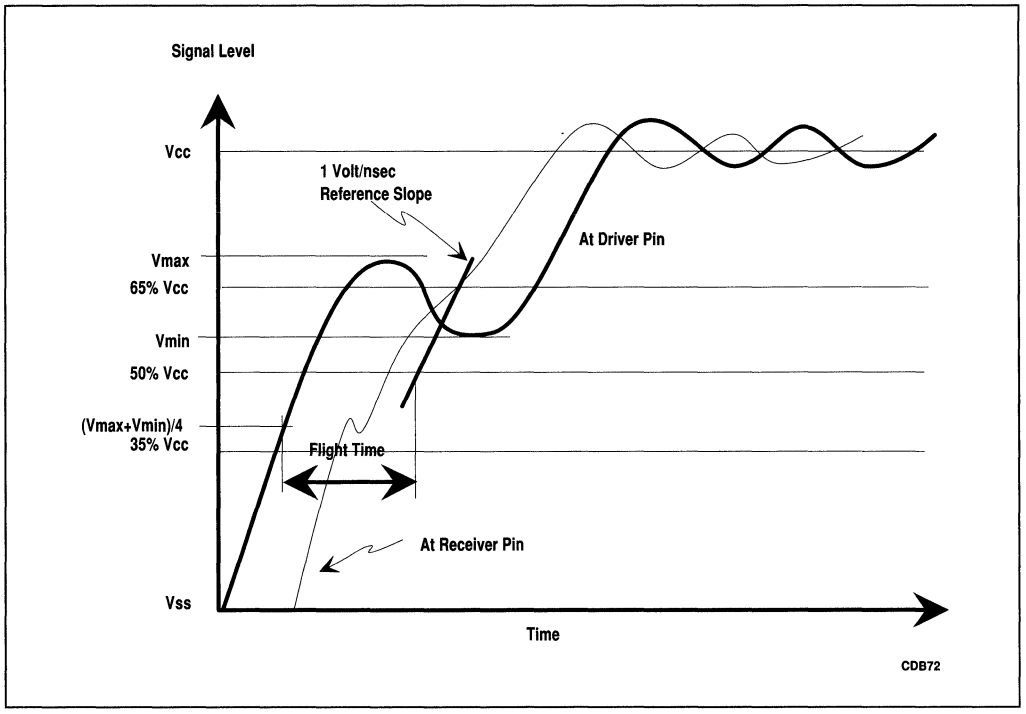


Figure 7-3. In-System Measurement of Flight Time

Table 7-4 describes the maximum flight time and clock skew specifications. Tables 7-5 to Table 7-16 list the flight time and maximum clock skew specifications for each driver-receiver network in the optimized interface. For each net, the driver first order output buffer model type and receiver input buffer model type are also listed. Some signals have **two buffer types** listed in the "Driver Buffer Type" column. These are the signals whose buffer type is **selected** using **BUSCHK#** (Pentium processor) and **CLDRV** (82496 cache controller) as described in section 4.5. The first entry corresponds to driving these configuration signals HIGH during reset and the second to driving them LOW. Tables 7-5 to 7-8 list the flight time and clock skew for the 66 MHz 256K byte CPU Cache Chip Set. Tables 7-9 to 7-12 list the flight time and clock skew for the 60 MHz 256K byte CPU Cache Chip Set. Tables 7-13 to 7-16 list the flight time and clock skew for the 60 MHz 512K byte CPU Cache Chip Set.

Table 7-4. Description of Maximum Flight Time and Clock Skew

Parameter	Description
Maximum Flight Time	Maximum time delay for a signal to reach the receiving component referenced from the driving component's pin, when the driver is unloaded. It includes the time to traverse the PC board trace and any added output delay on the output buffer due to the trace and receiving component loading and is dependent on rise time at the receiving component.
Maximum Clock Skew	Maximum clock skew is the difference in time of the clock signal arriving at different components. It is measured at 0.8V, 1.5V, and 2.0V.

7.6.1.1.1. 66-MHz 256-Kbyte Flight Times

Table 7-5. Signal Group: CPU to Cache RAM (CPU-CRAM) (66 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	CS CDATA0-7	0.7	1.0	2.2	ZD2	ZR10
PP DP0-7	CS CDATA0-3	0.7	1.0	2.2	ZD2	ZR10
CS CDATA0-7	PP D0-D63	0.7	1.0	2.2	ZD10	ZR4
CS CDATA0-3	PP DP0-7	0.7	1.0	2.2	ZD10	ZR4

Table 7-6. Signal Group: CPU to Cache (CPU-Cache) (66 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	CC CFA0-1	0.2	2.8	ZD6/ZD6a	ZR8
PP A5	CC CFA6	0.2	2.8	ZD6/ZD6a	ZR8
PP A6-A16	CC SET0-10	0.2	2.8	ZD6/ZD6a	ZR8
PP A3-A16	CS A2-A15	0.7	2.8	ZD6/ZD6a	ZR9
CC CFA0-1	PP A3-A4	0.2	9.5	ZD7	ZR6
CC CFA6	PP A5	0.2	9.5	ZD7	ZR6
CC SET0-10	PP A6-A16	0.2	9.5	ZD7	ZR6
CC CFA0-1	CS A2-A3	0.7	9.5	ZD7	ZR9
CC CFA6	CS A4	0.7	9.5	ZD7	ZR9
CC SET0-10	CS A5-A15	0.7	9.5	ZD7	ZR9
PP W/R#	CC W/R#	0.2	3.0	ZD5/ZD5a	ZR7
PP W/R#	CS W/R#	0.7	3.3	ZD5/ZD5a	ZR9
PP HITM#	CC HITM#	0.2	3.0	ZD5/ZD5a	ZR7
PP HITM#	CS HITM#	0.7	3.2	ZD5/ZD5a	ZR9
PP ADS#	CS ADS#	0.7	2.7	ZD5/ZD5a	ZR9
PP BE0-7#	CS BE#	0.7	2.3	ZD1	ZR9
PP BE0-7#	CS CDATA4-7	0.7	2.3	ZD1	ZR10

Table 7-7. Signal Group: CPU to Cache Controller (CPU-CCTL) (66 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A17-A20	CC TAG0-3	0.2	1.7	ZD6/ZD6a	ZR8
PP A21-A28	CC TAG4-11	0.2	1.7	ZD3	ZR8
PP A29-A31	CC CFA2-4	0.2	1.7	ZD3	ZR8
PP BT0-BT3	CC BT0-BT3	0.2	1.7	ZD3	ZR8
CC TAG0-3	PP A17-A20	0.2	3.2	ZD7	ZR6
CC TAG4-11	PP A21-A28	0.2	3.2	ZD7	ZR5
CC AP	PP AP	0.2	2.7	ZD7	ZR3
CC CFA2-4	PP A29-A31	0.2	3.2	ZD7	ZR5
CC BT0-BT3	PP BT0-BT3	0.2	3.2	ZD7	ZR5
PP AP	CC AP	0.2	1.6	ZD4	ZR8
PP SCYC	CC SCYC	0.2	1.6	ZD1	ZR7
PP PWT	CC PWT	0.2	1.6	ZD1	ZR7
PP PCD	CC PCD	0.2	1.6	ZD1	ZR7
PP M/IO#	CC M/IO#	0.2	1.6	ZD1	ZR7
PP D/C#	CC D/C#	0.2	1.4	ZD1	ZR7
PP LOCK#	CC LOCK#	0.2	1.6	ZD1	ZR7
PP CACHE#	CC CACHE#	0.2	1.6	ZD1	ZR7
PP ADSC#	CC ADS#	0.2	1.5	ZD1	ZR7a
CC AHOLD	PP AHOLD	0.2	1.7	ZD8	ZR1
CC EADS#	PP EADS#	0.2	1.7	ZD8	ZR1
CC KEN#	PP KEN#	0.2	1.7	ZD8	ZR1
CC BRDYC1#	PP BRDYC#	0.2	1.6	ZD8	ZR2
CC WBWT#	PP WBWT#	0.2	1.7	ZD8'	ZR1
CC INV	PP INV	0.2	1.7	ZD8	ZR1a
CC NA#	PP NA#	0.2	1.7	ZD8'	ZR1
CC EWBE#	PP EWBE#	0.2	1.7	ZD8	ZR1

Table 7-8. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (66 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
CC BOFF#	PP BOFF#	0.2	3.0	ZD9/ZD9a	ZR1
CC BOFF#	CS BOFF#	0.7	3.0	ZD9/ZD9a	ZR9
CC BLAST#	CS BLAST#	0.7	2.5	ZD9/ZD9a	ZR9
CC WRARR#	CS WRARR#	0.7	2.5	ZD9/ZD9a	ZR9
CC WAY	CS WAY	0.7	2.7	ZD9/ZD9a	ZR9
CC MCYC#	CS MCYC#	0.7	2.7	ZD9/ZD9a	ZR9
CC MAWEA#	CS MAWEA#	0.7	2.7	ZD9/ZD9a	ZR9
CC BUS#	CS BUS#	0.7	2.7	ZD9/ZD9a	ZR9
CC WBA	CS WBA	0.7	2.7	ZD9/ZD9a	ZR9
CC WBWE#	CS WBWE#	0.7	2.7	ZD9/ZD9a	ZR9
CC WBTYP	CS WBTYP	0.7	2.7	ZD9/ZD9a	ZR9
CC BRDYC2#	CS BRDYC#	0.7	2.5	ZD9/ZD9a	ZR9
CC BLEC#	CS BLEC#	0.7	2.5	ZD9/ZD9a	ZR9

7.6.1.1.2. 60-MHz 256-Kbyte Flight Times

Table 7-9. Signal Group: CPU to Cache RAM (CPU-CRAM) (60 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	CS CDATA0-7	0.8	1.0	2.7	ZD2	ZR10
PP DP0-7	CS CDATA0-3	0.8	1.0	2.7	ZD2	ZR10
CS CDATA0-7	PP D0-D63	0.8	1.0	2.7	ZD10	ZR4
CS CDATA0-3	PP DP0-7	0.8	1.0	2.7	ZD10	ZR4

Table 7-10. Signal Group: CPU to Cache (CPU-Cache) (60 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	CC CFA0-1	0.3	3.3	ZD6/ZD6a	ZR8
PP A5	CC CFA6	0.3	3.3	ZD6/ZD6a	ZR8
PP A6-A16	CC SET0-10	0.3	3.3	ZD6/ZD6a	ZR8
PP A3-A16	CS A2-A15	0.8	3.3	ZD6/ZD6a	ZR9
CC CFA0-1	PP A3-A4	0.3	10	ZD7	ZR6
CC CFA6	PP A5	0.3	10	ZD7	ZR6
CC SET0-10	PP A6-A16	0.3	10	ZD7	ZR6
CC CFA0-1	CS A2-A3	0.8	10	ZD7	ZR9
CC CFA6	CS A4	0.8	10	ZD7	ZR9
CC SET0-10	CS A5-A15	0.8	10	ZD7	ZR9
PP W/R#	CC W/R#	0.3	3.5	ZD5/ZD5a	ZR7
PP W/R#	CS W/R#	0.8	3.8	ZD5/ZD5a	ZR9
PP HITM#	CC HITM#	0.3	3.5	ZD5/ZD5a	ZR7
PP HITM#	CS HITM#	0.8	3.7	ZD5/ZD5a	ZR9
PP ADS#	CS ADS#	0.8	3.2	ZD5/ZD5a	ZR9
PP BE0-7#	CS BE#	0.8	2.8	ZD1	ZR9
PP BE0-7#	CS CDATA4-7	0.8	2.8	ZD1	ZR10

Table 7-11. Signal Group: CPU to Cache Controller (CPU-CCTL) (60 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A17-A20	CC TAG0-3	0.3	2.2	ZD6/ZD6a	ZR8
PP A21-A28	CC TAG4-11	0.3	2.2	ZD3	ZR8
PP A29-A31	CC CFA2-4	0.3	2.2	ZD3	ZR8
PP BT0-BT3	CC BT0-BT3	0.3	2.2	ZD3	ZR8
CC TAG0-3	PP A17-A20	0.3	3.7	ZD7	ZR6
CC TAG4-11	PP A21-A28	0.3	3.7	ZD7	ZR5
CC AP	PP AP	0.3	3.2	ZD7	ZR3
CC CFA2-4	PP A29-A31	0.3	3.7	ZD7	ZR5
CC BT0-BT3	PP BT0-BT3	0.3	3.7	ZD7	ZR5
PP AP	CC AP	0.3	2.1	ZD4	ZR8
PP SCYC	CC SCYC	0.3	2.1	ZD1	ZR7
PP PWT	CC PWT	0.3	2.1	ZD1	ZR7
PP PCD	CC PCD	0.3	2.1	ZD1	ZR7
PP M/IO#	CC M/IO#	0.3	2.1	ZD1	ZR7
PP D/C#	CC D/C#	0.3	1.9	ZD1	ZR7
PP LOCK#	CC LOCK#	0.3	2.1	ZD1	ZR7
PP CACHE#	CC CACHE#	0.3	2.1	ZD1	ZR7
PP ADSC#	CC ADS#	0.3	2.0	ZD1	ZR7a
CC AHOLD	PP AHOLD	0.3	2.2	ZD8	ZR1
CC EADS#	PP EADS#	0.3	2.2	ZD8	ZR1
CC KEN#	PP KEN#	0.3	2.2	ZD8	ZR1
CC BRDYC1#	PP BRDYC#	0.3	2.1	ZD8	ZR2
CC WBWT#	PP WBWT#	0.3	2.2	ZD8'	ZR1
CC INV	PP INV	0.3	2.2	ZD8	ZR1a
CC NA#	PP NA#	0.3	2.2	ZD8'	ZR1
CC EWBE#	PP EWBE#	0.3	2.2	ZD8	ZR1

Table 7-12. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (60 MHz 256 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
CC BOFF#	PP BOFF#	0.3	3.5	ZD9/ZD9a	ZR1
CC BOFF#	CS BOFF#	0.8	3.5	ZD9/ZD9a	ZR9
CC BLAST#	CS BLAST#	0.8	3.0	ZD9/ZD9a	ZR9
CC WRARR#	CS WRARR#	0.8	3.0	ZD9/ZD9a	ZR9
CC WAY	CS WAY	0.8	3.2	ZD9/ZD9a	ZR9
CC MCYC#	CS MCYC#	0.8	3.2	ZD9/ZD9a	ZR9
CC MAWEA#	CS MAWEA#	0.8	3.2	ZD9/ZD9a	ZR9
CC BUS#	CS BUS#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBA	CS WBA	0.8	3.2	ZD9/ZD9a	ZR9
CC WBWE#	CS WBWE#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBTYP	CS WBTYP	0.8	3.2	ZD9/ZD9a	ZR9
CC BRDYC2#	CS BRDYC#	0.8	3.0	ZD9/ZD9a	ZR9
CC BLEC#	CS BLEC#	0.8	3.0	ZD9/ZD9a	ZR9

7.6.1.1.3. 60-MHz 512-Kbyte Flight Times

Table 7-13 to Table 7-16 list the flight time and clock skew for the 60 MHz 512K byte CPU Cache Chip Set. Note the maximum frequency of the 512K chip set is 60 MHz. All external interface specifications remain unchanged except for the maximum frequency.

Table 7-13. Signal Group: CPU to Cache RAM (CPU-CRAM) (60 MHz 512 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	CS CDATA0-3	0.8	1.0	2.7	ZD2	ZR10
PP DP0-7	CS CDATA0-3	0.8	1.0	2.7	ZD2	ZR10
CS CDATA0-3	PP D0-D63	0.8	1.0	2.7	ZD10	ZR4
CS CDATA0-3	PP DP0-7	0.8	1.0	2.7	ZD10	ZR4

Table 7-14. Signal Group: CPU to Cache (CPU-Cache) (60 MHz 512 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	CC CFA0-1	0.3	3.3	ZD6/ZD6a	ZR8
PP A5-A6	CC CFA5-6	0.3	3.3	ZD6/ZD6a	ZR8
PP A7-A17	CC SET0-10	0.3	3.3	ZD6/ZD6a	ZR8
PP A3-A17	CS A1-A15	0.8	3.3	ZD6/ZD6a	ZR9
CC CFA0-1	PP A3-A4	0.3	10.6	ZD7	ZR6
CC CFA5-6	PP A5-A6	0.3	10.6	ZD7	ZR6
CC SET0-10	PP A7-A17	0.3	10.6	ZD7	ZR6
CC CFA0-1	CS A1-A2	0.8	10.6	ZD7	ZR9
CC CFA5-6	CS A3-A4	0.8	10.6	ZD7	ZR9
CC SET0-10	CS A5-A15	0.8	10.6	ZD7	ZR9
PP W/R#	CC W/R#	0.3	3.9	ZD5/ZD5a	ZR7
PP W/R#	CS W/R#	0.8	4.0	ZD5/ZD5a	ZR9
PP HITM#	CC HITM#	0.3	3.8	ZD5/ZD5a	ZR7
PP HITM#	CS HITM#	0.8	3.9	ZD5/ZD5a	ZR9
PP ADS#	CS ADS#	0.8	3.2	ZD5/ZD5a	ZR9
PP BE0-7#	CS BE#	0.8	2.8	ZD1	ZR9
PP BE0-7#	CS CDATA4-7	0.8	2.8	ZD1	ZR10

Table 7-15. Signal Group: CPU to Cache Controller (CPU-CCTL) (60 MHz 512 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
PP A18-A21	CC TAG0-3	0.3	2.2	ZD6/ZD6a	ZR8
PP A22-A29	CC TAG4-11	0.3	2.2	ZD3	ZR8
PP A30-A31	CC CFA2-3	0.3	2.2	ZD3	ZR8
PP BT0-BT3	CC BT0-BT3	0.3	2.2	ZD3	ZR8
CC TAG0-3	PP A18-A21	0.3	3.7	ZD7	ZR6
CC TAG4-11	PP A22-A29	0.3	3.7	ZD7	ZR5
CC AP	PP AP	0.3	3.2	ZD7	ZR3
CC CFA2-3	PP A30-A31	0.3	3.7	ZD7	ZR5
CC BT0-BT3	PP BT0-BT3	0.3	3.7	ZD7	ZR5
PP AP	CC AP	0.3	2.1	ZD4	ZR8
PP SCYC	CC SCYC	0.3	2.1	ZD1	ZR7
PP PWT	CC PWT	0.3	2.1	ZD1	ZR7
PP PCD	CC PCD	0.3	2.1	ZD1	ZR7
PP M/IO#	CC M/IO#	0.3	2.1	ZD1	ZR7
PP D/C#	CC D/C#	0.3	1.9	ZD1	ZR7
PP LOCK#	CC LOCK#	0.3	2.1	ZD1	ZR7
PP CACHE#	CC CACHE#	0.3	2.1	ZD1	ZR7
PP ADSC#	CC ADS#	0.3	2.0	ZD1	ZR7a
CC AHOLD	PP AHOLD	0.3	2.2	ZD8	ZR1
CC EADS#	PP EADS#	0.3	2.2	ZD8	ZR1
CC KEN#	PP KEN#	0.3	2.2	ZD8	ZR1
CC BRDYC1#	PP BRDYC#	0.3	2.1	ZD8	ZR2
CC WBWT#	PP WBWT#	0.3	2.2	ZD8'	ZR1
CC INV	PP INV	0.3	2.2	ZD8	ZR1a
CC NA#	PP NA#	0.3	2.2	ZD8'	ZR1
CC EWBE#	PP EWBE#	0.3	2.2	ZD8	ZR1

Table 7-16. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (60 MHz 512 Kbyte Version)

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
CC BOFF#	PP BOFF#	0.3	3.7	ZD9/ZD9a	ZR1
CC BOFF#	CS BOFF#	0.8	3.7	ZD9/ZD9a	ZR9
CC BLAST#	CS BLAST#	0.8	3.0	ZD9/ZD9a	ZR9
CC WRARR#	CS WRARR#	0.8	3.0	ZD9/ZD9a	ZR9
CC WAY	CS WAY	0.8	3.2	ZD9/ZD9a	ZR9
CC MCYC#	CS MCYC#	0.8	3.2	ZD9/ZD9a	ZR9
CC MAWEA#	CS MAWEA#	0.8	3.2	ZD9/ZD9a	ZR9
CC BUS#	CS BUS#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBA	CS WBA	0.8	3.2	ZD9/ZD9a	ZR9
CC WBWE#	CS WBWE#	0.8	3.2	ZD9/ZD9a	ZR9
CC WBTYP	CS WBTYP	0.8	3.2	ZD9/ZD9a	ZR9
CC BRDYC2#	CS BRDYC#	0.8	3.0	ZD9/ZD9a	ZR9
CC BLEC#	CS BLEC#	0.8	3.0	ZD9/ZD9a	ZR9

7.6.1.2. SIGNAL QUALITY

Acceptable signal quality must be maintained over all operating conditions. Figure 7-4 illustrates the parameters used to verify acceptable signal quality. Table 7-17 describes each of these parameters.

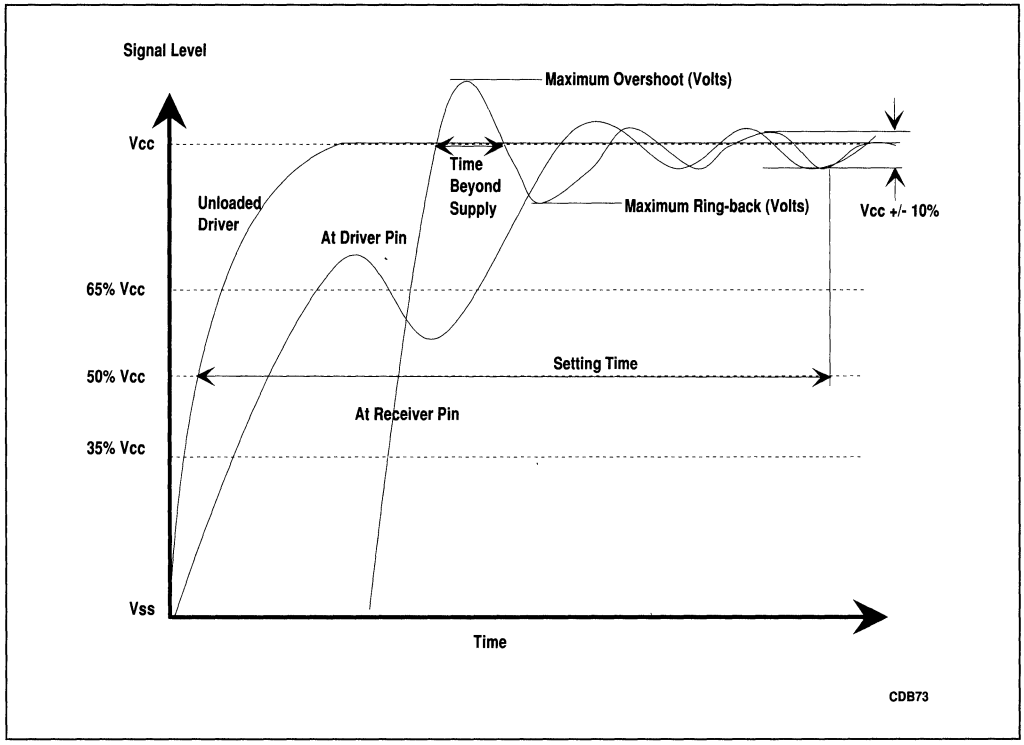


Figure 7-4. Driver and Receiver Signal Waveforms Showing Signal Quality Parameters

Beyond the absolute maximum values shown in Figure 7-4, each of the four signal groups defined by Tables 7-5 to 7-16 in the CPU-Cache Chip Set optimized interface must meet a maximum group average for Overshoot (Undershoot) and Time Beyond the Supply. Maximum group average overshoot (undershoot) is the numeric average of the maximum signal overshoot (undershoot) for each signal within the signal group. Maximum group average Time Beyond the Supply is the numeric average of the Maximum Time Beyond the Supply for each signal within the signal group.

Group average is calculated assuming one component is driving the line. For example the CPU-CRAM group includes the data bus between the Pentium processor and 82491 cache SRAM. The averages should be calculated assuming the Pentium processor is driving the data bus. A second average is calculated assuming the 82491 cache SRAM is driving. Both must be less than the specified limit.

Since the maximum value for signal overshoot and undershoot will be limited by the component's ESD diodes, both the absolute and group average specifications for overshoot and undershoot must be met under the simulation conditions described by Tables 7-5 to 7-17.

Table 7-17. Specifications for Signal Quality

Parameter	Description	Group	Specification
Absolute Maximum Signal Overshoot (Undershoot)	Absolute value of the maximum voltage at the receiving pin above Vcc (or below Vss) relative to Vcc (or Vss) level. (Assumes input diodes are not present.)	NA	3.0 Volts
Absolute Maximum Time Beyond the Supply	Maximum time a signal may exceed Vcc (or Vss). Time beyond supply can be ignored if the overshoot is less than 0.5 volts.	NA	6ns
Maximum Signal Ring-back	Absolute value of the maximum voltage at the receiving pin below Vcc (or above Vss) relative to Vcc (or Vss) level after the signal has reached its maximum voltage level.	NA	65% Vcc Volts (low to high) 35% Vcc Volts (high to low)
Maximum Settling Time	Total time required for a signal to settle within 10% of its final value referenced from the unloaded driver's initial crossing of the 50% level.	NA	12.5 nsec
Maximum Group Average Overshoot (Undershoot)	The maximum numeric average of the signal overshoot (undershoot) for all signals within a signal group.	CPU-CRAM	1.5 Volt
		CPU-Cache	2.5 Volt
		CPU-CCTL	1.5 Volt
		CCTL-CRAM	2.5 Volt
Maximum Group Average Time Beyond Supply	The maximum numeric average of the time a signal may exceed Vcc (or Vss) for all signals within a signal group. (Signals whose overshoot is less than 0.5V should be ignored in calculating this average.)	CPU-CRAM	3.0ns
		CPU-Cache	4.5ns
		CPU-CCTL	3.0ns
		CCTL-CRAM	4.5ns

7.6.2. External Interface

The external interface is the interface between the chip set components and the memory bus controller, memory address bus, and memory data bus. Intel supplies buffer models for this interface to aid system designers simulation of this section of their design. Unlike the optimized interface, Intel supplies the A.C. specifications of output valid delay and input setup and hold times.

Tables 7-18 to 7-21 list the 66 MHz A.C. specifications and Tables 7-22 to 7-25 list the 60 MHz A.C. specifications associated with the chip set's external interface signals.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor, 82496 cache controller, and 82491 cache SRAM operation.

Care should be taken to read all notes associated with a particular timing parameter. In addition, the following list of notes apply to the timing specification tables in general and are not associated with any one timing. They are 6, 13, 14, 15, 37, 47, 48, and 50.

7.6.2.1. 66 MHz A.C. SPECIFICATIONS

Table 7-18. 66 MHz CPU Cache Chip Set Common Timings

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t1	CLK Frequency	33.33	66.66	MHz		1X clock, (1), (49)
t2	CLK Period	15	30	ns	7.5	
t3	CLK High Time	4		ns	7.5	(2)
t4	CLK Low Time	4		ns	7.5	(3)
t5	CLK Rise Time	0.15	1.5	ns	7.5	(4)
t6	CLK Fall Time	0.15	1.5	ns	7.5	(4)
t7	CLK Stability		+/- 250	pS		(18), (19), (20), (21)
t8	RESET, INIT Setup Time	6		ns	7.9	To guarantee recognition on a given CLK edge. (16), (17)
t9	RESET, INIT Hold Time	1.5		ns	7.9	To guarantee recognition on a given CLK edge.
t10	RESET Pulse Width, CLK and Vcc Stable	15		CLKs	7.9	(11), (17)
t11	INIT Pulse Width, Async.	2		CLKs		To guarantee asynchronous recognition.
t12	INIT Pulse Width, CLK and Vcc Stable	1		CLKs		
t13	RESET Active After CLK and Vcc Stable	1		ms	7.9	Power Up (11), (12)
t20	TCK Frequency	--	16	MHz		
t21	TCK Period	62.5		ns	7.5	
t22	TCK High Time	25		ns	7.5	(2)
t23	TCK Low Time	25		ns	7.5	(3)
t24	TCK Rise Time		5	ns	7.5	(9), (4)
t25	TCK Fall Time		5	ns	7.5	(9), (4)

Table 7-18. 66 MHz CPU Cache Chip Set Common Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t28	TRST# Pulse Width	40		ns	7.15	(46), Asynchronous
t29	TDI, TMS Setup Time	5		ns	7.14	(7)
t30	TDI, TMS Hold Time	13		ns	7.14	(7)
t31	TDO Valid Delay	3	20	ns	7.14	(8)
t32	TDO Float Delay		25	ns	7.14	(8), (46)
t33	All Non-Test Outputs Valid Delay	3	20	ns	7.14	(8), (10)
t34	All Non-Test Outputs Float Delay		25	ns	7.14	(8), (10), (46)
t35	All Non-Test Inputs Setup Time	5		ns	7.14	(7), (8)
t36	All Non-Test Inputs Hold Time	13		ns	7.14	(7), (8)

Table 7-19. 66 MHz Pentium™ Processor Memory Bus Interface Timings

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t40	PP reset configurations Setup Time	5		ns	7.9	
t41	PP reset configurations Hold Time	1.5		ns	7.9	
t42	PP reset configurations Setup Time Referenced to Falling Edge of RESET	4		CLKs	7.9	
t43	PP reset configurations Hold Time Reference to Falling Edge of RESET	0		CLKs	7.9	
t50	HLDA Valid Delay	1.5	8	ns	7.6	(5)
t51	BREQ Valid Delay	1.5	8	ns	7.6	
t52	PCHK#, APCHK#, FERR#, IERR# Valid Delay	1.5	8.3	ns	7.6	(5)
t53	IU, IV, IBT Valid Delay	1.5	10	ns	7.6	
t54	BP0-3, PM0-1 Valid Delay	1.5	10	ns	7.6	
t55	A20M#, FLUSH#, IGNNE#, NMI, INTR, Setup Time	5		ns	7.7	(16), (17)
t56	A20M#, FLUSH#, IGNNE#, NMI, INTR, Hold Time	1.5		ns	7.7	
t57	A20M#, FLUSH#, IGNNE#, NMI, INTR, Pulse Width, Async	2		CLKs		(17)
t58	PEN#, BUSCHK# Setup Time	5		ns	7.7	
t59	PEN#, BUSCHK# Hold Time	1.5		ns	7.7	
t60	HOLD Setup Time	5		ns	7.7	
t61	HOLD Hold Time	1.5		ns	7.7	
t62	BRDY# Setup Time	5		ns	7.7	
t63	BRDY# Hold Time	1.5		ns	7.7	
t64	R/S#, SMI# Setup Time	5		ns	7.7	(16), (17)
t65	R/S#, SMI# Hold Time	1.5		ns	7.7	
t66	R/S#, SMI# Pulse Width, Async	2		CLKs		(17)
t67	PRDY, SMIACT# Valid Delay	1.5	8	ns	7.6	

Table 7-20. 66 MHz 82496 Cache Controller Memory Bus Interface Timings

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t70	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Setup Time	6		ns	7.9	(12), (22), (36)
t71	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Hold Time	1		ns	7.9	(12), (23), (36)
t72	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Setup Time Referenced to Falling Edge of RESET	10		CLKs	7.9	(12), (36)
t73	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Hold Time Referenced to Falling Edge of RESET	0		CLKs	7.9	(12), (36)
t75	FLUSH#, SYNC# Setup Time	6		ns	7.7	(34)
t76	FLUSH#, SYNC#, Hold Time	1		ns	7.7	(34)
t77	FLUSH#, SYNC#, Pulse Width, Async	2		CLKs		
t80	CADS#, CDTS# Valid Delay	1.5	8.2	ns	7.6	Glitch Free
t81	KLOCK#, MCACHE#, RDYSRC Valid Delay	1.5	8.2	ns	7.6	KLOCK# is Glitch Free
t82	CW/R#, CD/C#, CMI/O# Valid Delay	1.5	8.2	ns	7.6	
t83	CPWT, CPCD, CCACHE#, CSCYC Valid Delay	1.5	8.2	ns	7.6	
t84	CAHOLD, CWAY, PALLC# Valid Delay	1.5	8.2	ns	7.6	
t85	FSIOUT# Valid Delay	1.5	8.2	ns	7.6	
t86	NENE#, SMLN# Valid Delay	1.5	12	ns	7.6	
t87	APERR#, IPERR#, MAPERR# Valid Delay	1.5	8.2	ns	7.6	Glitch Free
t88	APIC# Valid Delay	1.5	12	ns	7.6	
t89	BLE# Valid Delay	1.5	8.2	ns	7.6	(35)

Table 7-20. 66 MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t90	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	11	ns	7.6	(25), (43)
t91	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	11	ns	7.10	(26), (43)
t92	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	10	ns	7.10	(27), (43)
t93	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Float Delay		11	ns	7.10	(28), (46)
t95	BRDY#, CRDY# Setup Time	6.5		ns	7.7	
t96	BRDY#, CRDY# Hold Time	1		ns	7.7	
t97	BGT#, CNA#, KWEND#, SWEND# Setup Time	6		ns	7.7	
t98	BGT#, CNA#, KWEND#, SWEND# Hold Time	1		ns	7.7	
t100	DRCTM#, MRO#, MWB/WT# Setup Time	6		ns	7.7	(24)
t100a	MKEN# Setup Time	6.5		ns	7.7	(24)
t101	DRCTM#, MKEN#, MRO#, MWB/WT# Hold Time	1		ns	7.7	(24)
t110	SNPCLK Frequency	8.3	66.66	MHz		1X clock
t111	SNPCLK Period	15	120	ns	7.5	
t112	SNPCLK High Time	4		ns	7.5	
t113	SNPCLK Low Time	4		ns	7.5	
t114	SNPCLK Rise Time		1.5	ns	7.5	(38)
t115	SNPCLK Fall Time		1.5	ns	7.5	(38)
t118	SNPADS#, SNPCYC# Valid Delay	1.5	8.2	ns	7.6	Glitch Free.
t120	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6		ns	7.7	(29)
t121	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7.7	(29)
t122	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6		ns	7.7	(30)

Table 7-20. 66 MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t123	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7.7	(30)
t124	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	1		ns	7.8	(31)
t125	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	6		ns	7.8	(31)
t130	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6		ns	7.7	(29)
t131	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7.7	(29)
t132	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6		ns	7.7	(30)
t133	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7.7	(30)
t134	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	1		ns	7.8	(31)
t135	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	6		ns	7.8	(31)
t140	SNPSTB# Setup Time	6		ns	7.7	(29)
t141	SNPSTB# Hold Time	1		ns	7.7	(29)
t142	SNPSTB# Setup Time	6		ns	7.7	(30)
t143	SNPSTB# Hold Time	1		ns	7.7	(30)
t144	SNPSTB# Active Time	6		ns	7.16	(32)
t145	SNPSTB# Inactive Time	6		ns	7.16	(32)
t148	MHITM#, MTHIT#, SNPBSY# Valid Delay	1.5	10	ns	7.6	

Table 7-21. 66 MHz 82491 Cache SRAM Memory Bus Interface Timings

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t150	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time	5		ns	7.9	(22), (42)
t151	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time	1		ns	7.9	(23), (42)
t152	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time Refernced to Falling Edge of RESET	4		CLKs	7.9	(41), (42)
t153	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time Referenced to Falling Edge of RESET	0		CLKs	7.9	(41), (42)
t155	BRDY#, CRDY# Setup Time	5		ns	7.7	
t156	BRDY#, CRDY# Hold Time	1		ns	7.7	
t160	MDATA Setup to CLK (CLK before BRDY# Active)	5		ns	7.7	(44)
t161	MDATA Valid Delay From CLK (CLK from CDTS# Valid, MDOE# Active)		13	ns	7.6	(49)
t162	MDATA Valid Delay From MDOE# Active		8	ns	7.10	
t163	MDATA Float Delay From MDOE# Inactive		10	ns	7.10	
t165	MBE# Valid Delay	1.5	8	ns	7.6	(39)
Clocked Mode						
t170	MCLK, MOCLK Frequency		66.66	MHz		1X clock, (49)
t171	MCLK, MOCLK Period	15		ns	7.5	
t172	MOCLK High Time	4		ns	7.5	
t173	MOCLK Low Time	4		ns	7.5	
t174	MCLK High Time	5		ns	7.5	(40)
t175	MCLK Low Time	5		ns	7.5	(40)
t176	MCLK, MOCLK Rise Time		1.5	ns	7.5	
t177	MCLK, MOCLK Fall Time		1.5	ns	7.5	

Table 7-21. 66 MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Clocked Mode						
t180	MOCLK Falling Edge To MCLK Rising Edge	2		ns		
t181	MFRZ#, MZBT# Setup Time	5		ns	7.7	Referenced to MCLK
t182	MFRZ#, MZBT# Hold Time	1		ns	7.7	Referenced to MCLK
t183	MBRDY#, MSEL#, MEOC# Setup Time	5		ns	7.7	Referenced to MCLK
t184	MBRDY#, MSEL#, MEOC# Hold Time	1		ns	7.7	Referenced to MCLK
t185	MDATA Setup Time	5		ns	7.7	Referenced to MCLK
t186	MDATA Hold Time	1		ns	7.7	Referenced to MCLK
t187	MDATA Valid Delay From MCLK•MBRDY#	2	12	ns	7.6	
t188	MDATA Valid Delay From MCLK•MEOC#	2	20	ns	7.6	
t189	MDATA Valid Delay From MCLK•MSEL#	2	18	ns	7.6	(45)
t190	MDATA Valid Delay From MOCLK	1.5	10	ns	7.6	
Strobed Mode						
t195	MEOC# High Time	8		ns	7.16	(49)
t196	MEOC# Low Time	8		ns	7.16	
t197	MISTB, MOSTB High Time	12		ns	7.16	(49)
t198	MISTB, MOSTB Low Time	12		ns	7.16	
t199	MEOC#, MISTB, MOSTB Rise Time		2	ns		

Table 7-21. 66 MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Strobed Mode						
t200	MEOC#, MISTB, MOSTB Fall Time		2	ns		
t201	MSEL# High Time for Restart	8		ns	7.16	
t202	MSEL# Setup Before Transition on MISTB or MOSTB	5		ns	7.12	(49)
t203	MSEL# Hold After Transition on MISTB or MOSTB	10		ns	7.12	
t204	MSEL# Setup Before Transition on MEOC#	5		ns	7.12	
t205	MSEL# Hold After Transition on MEOC#	1		ns	7.12	
t206	MISTB, MOSTB Transition to/from MEOC# Falling Transition	10		ns		
t207	MZBT# Setup To MSEL# or MEOC# Falling Edge	5		ns	7.11	
t208	MZBT# Hold From MSEL# or MEOC# Falling Edge	1		ns	7.11	
t209	MFRZ# Setup To MEOC# Falling Edge	5		ns	7.11	
t210	MFRZ# Hold From MEOC# Falling Edge	1		ns	7.11	
t211	MDATA Setup To MISTB transition or MEOC# Falling Edge	5		ns	7.11	
t212	MDATA Hold From MISTB transition or MEOC# Falling Edge	1		ns	7.11	
t213	MDATA Valid Delay From Transition on MOSTB	2	12	ns	7.13	
t214	MDATA Valid Delay From MEOC# Falling Transition or MSEL# Deactivation	2	20	ns	7.13	

NOTES:

1. Below 66 MHz only functionality is guaranteed, the following equations provide the change in A.C. specifications required to operate at lower frequencies:

   Pentium™ processor: no effect

   82496 cache controller: (signals: SET0-10, ADS#, CFA2-6, and TAG0-11)
   Δ setup = 0.57 (Δ cycle time) +/- 0.5ns

   82491 cache SRAM: no effect
2. High times are measured between 2.0 V crossing points.
3. Low times are measured between 0.8 V crossing points.
4. Rise and Fall times are measured between 0.8 V and 2.0 V.
5. APCHK#, FERR#, HLDA, IERR#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e. glitches).
6. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/ns rise and fall times.

7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 16 MHz. 1ns must be added to t30 and t36 for every 10 MHz of frequency below 16 MHz.
10. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
11. FRCMC# should be tied to Vcc (high) to ensure proper operation of the Pentium processor as a master Pentium processor.
12. If configuration signals with internal pullup resistors are left floating in the system, RESET pulse width must be at least 10 microseconds.
13. CLK skew between Pentium processor and 82496 cache controller assumed to be less than 0.2ns. CLK skew is measured at 0.8V, 1.5V, and 2.0V of the rising edge of CLK.
14. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
15. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
16. This input may be driven asynchronously.
17. When driven asynchronously, NMI, FLUSH#, R/S#, INIT, and SMI must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
18. Functionality is guaranteed by design/characterization.
19. Measured on rising edge of adjacent CLKs at 1.5V.
20. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency.
21. The amount of jitter present must be accounted for as a component of CLK skew between devices.
22. Setup time is required to guarantee recognition on a specific clock.
23. Hold time is required to guarantee recognition on a specific clock.
24. Only need to meet setup and hold times during the KWEND and SWEND sample times.
25. Valid delay from CLK only if MALE or MBALE, MAOE#, MBAOE# are active.
26. Valid delay from MALE or MBALE going active, if both MAOE# and MBAOE# are active.
27. Valid delay from MAOE#, MBAOE# going active.
28. Float delay from MAOE#, MBAOE# going inactive.
29. In Synchronous mode, referenced to CLK.
30. In Clocked mode, referenced to SNPCLK.
31. In Strobed mode, referenced to SNPSTB# falling edge.
32. In Strobed mode, must meet active/inactive times.
34. To guarantee recognition on a given CLK edge.
35. This signal is not used when using the 82496 cache controller with the 82491 cache SRAM.
36. For proper configuration, t70, t71, t72, and t 73 must all be met.
37. Glitch free signals monotonically transition without false transitions (i.e. glitches).
38. 1ns can be added to maximum SNPCLK rise/fall time for every 10 MHz of frequency below 66 MHz. 1ns must be added to t123 and t133 for every 10 MHz of frequency below 66 MHz.
39. From CLK in which BLEC# sampled active.
40. Tighter symmetry required since MCLK input does not use a PLL.
41. Timing is referenced to falling edge of RESET.
42. For proper configuration, t150, t151, t152, and t153 must all be met.
43. A.C. timings assume MALDRV=low on reset. If MALDRV=high on reset, add .7ns to t90, t91, and t92.

44. Must meet MDATA setup to CLK one full CLK before BRDY# active for first transfer on line fills and all non-cacheable transfers.
45. MSEL# sampled inactive resets burst counter. Data is re-driven beginning with data corresponding to first address requested.
46. Not 100% Tested. Guaranteed by design/characterization.
47. Float and Enable times measured at Vcc/2 level at gate of output device are guaranteed by design. (Not 100% tested)
48. CLK Skew between 82491 cache SRAM and other devices (Pentium processor, 82496 cache controller, and other C8Cs) assumed to be less than 0.7 ns.
49. Signal Restrictions
    a. For proper operation the following signals must have monotonic transitions:
       - CLK,
       - MCLK in clocked mode,
       - MISTB, MOSTB, and MEOC# in strobed mode.
    b. For proper operation the following signals must remain stable (must not glitch) throughout a cycle.
       - MDOE#,
       - MSEL#, when active during strobed mode.
50. All TTL timings are referenced from 1.5 V.

7.6.2.2. 60 MHz A.C. SPECIFICATIONS

Table 7-22. 60 MHz CPU Cache Chip Set Common Timings

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t1	CLK Frequency	33.33	60	MHz		1X clock, (1), (49)
t2	CLK Period	16.67	30	ns	7.5	
t3	CLK High Time	4		ns	7.5	(2)
t4	CLK Low Time	4		ns	7.5	(3)
t5	CLK Rise Time	0.15	1.5	ns	7.5	(4)
t6	CLK Fall Time	0.15	1.5	ns	7.5	(4)
t7	CLK Stability		+/- 250	pS		(18), (19), (20), (21)
t8	RESET, INIT Setup Time	6		ns	7.9	To guarantee recognition on a given CLK edge. (16), (17)
t9	RESET, INIT Hold Time	1.5		ns	7.9	To guarantee recognition on a given CLK edge.
t10	RESET Pulse Width, CLK and Vcc Stable	15		CLKs	7.9	(11), (17)
t11	INIT Pulse Width, Async.	2		CLKs		To guarantee asynchronous recognition.
t12	INIT Pulse Width, CLK and Vcc Stable	1		CLKs		
t13	RESET Active After CLK and Vcc Stable	1		ms	7.9	Power Up (11), (12)
t20	TCK Frequency	--	16	MHz		
t21	TCK Period	62.5		ns	7.5	
t22	TCK High Time	25		ns	7.5	(2)
t23	TCK Low Time	25		ns	7.5	(3)
t24	TCK Rise Time		5	ns	7.5	(9), (4)
t25	TCK Fall Time		5	ns	7.5	(9), (4)
t28	TRST# Pulse Width	40		ns	7.15	(46), Asynchronous
t29	TDI, TMS Setup Time	5		ns	7.14	(7)

Table 7-22 60 MHz CPU Cache Chip Set Common Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t30	TDI, TMS Hold Time	13		ns	7.14	(7)
t31	TDO Valid Delay	3	20	ns	7.14	(8)
t32	TDO Float Delay		25	ns	7.14	(8), (46)
t33	All Non-Test Outputs Valid Delay	3	20	ns	7.14	(8), (10)
t34	All Non-Test Outputs Float Delay		25	ns	7.14	(8), (10), (46)
t35	All Non-Test Inputs Setup Time	5		ns	7.14	(7), (8)
t36	All Non-Test Inputs Hold Time	13		ns	7.14	(7), (8)

Table 7-23. 60 MHz Pentium™ Processor Memory Bus Interface Timings

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t40	PP reset configurations Setup Time	5.5		ns	7.9	
t41	PP reset configurations Hold Time	1.5		ns	7.9	
t42	PP reset configurations Setup Time Referenced to Falling Edge of RESET	4		CLKs	7.9	
t43	PP reset configurations Hold Time Reference to Falling Edge of RESET	0		CLKs	7.9	
t50	HLDA Valid Delay	1.5	9	ns	7.6	(5)
t51	BREQ Valid Delay	1.5	9	ns	7.6	
t52	PCHK#, APCHK#, FERR#, IERR# Valid Delay	1.5	9.3	ns	7.6	(5)
t53	IU, IV, IBT Valid Delay	1.5	11	ns	7.6	
t54	BP0-3, PM0-1 Valid Delay	1.5	11	ns	7.6	
t55	A20M#, FLUSH#, IGNNE#, NMI, INTR, Setup Time	5.5		ns	7.7	(16), (17)
t56	A20M#, FLUSH#, IGNNE#, NMI, INTR, Hold Time	1.5		ns	7.7	
t57	A20M#, FLUSH#, IGNNE#, NMI, INTR, Pulse Width, Async	2		CLKs		(17)
t58	PEN#, BUSCHK# Setup Time	5.5		ns	7.7	
t59	PEN#, BUSCHK# Hold Time	1.5		ns	7.7	
t60	HOLD Setup Time	5.5		ns	7.7	
t61	HOLD Hold Time	1.5		ns	7.7	
t62	BRDY# Setup Time	5.5		ns	7.7	
t63	BRDY# Hold Time	1.5		ns	7.7	
t64	R/S#, SMI# Setup Time	5.5		ns	7.7	(16), (17)
t65	R/S#, SMI# Hold Time	1.5		ns	7.7	
t66	R/S#, SMI# Pulse Width, Async	2		CLKs		(17)
t67	PRDY, SMIACT# Valid Delay	1.5	9	ns	7.6	

Table 7-24. 60 MHz 82496 Cache Controller Memory Bus Interface Timings

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t70	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Setup Time	6.5		ns	7.9	(12), (22), (36)
t71	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Hold Time	1		ns	7.9	(12), (23), (36)
t72	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Setup Time Referenced to Falling Edge of RESET	10		CLKs	7.9	(12), (36)
t73	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[Vcc] Hold Time Referenced to Falling Edge of RESET	0		CLKs	7.9	(12), (36)
t75	FLUSH#, SYNC# Setup Time	6.5		ns	7.7	(34)
t76	FLUSH#, SYNC#, Hold Time	1		ns	7.7	(34)
t77	FLUSH#, SYNC#, Pulse Width, Async	2		CLKs		
t80	CADS#, CDTS# Valid Delay	1.5	9.2	ns	7.6	Glitch Free
t81	KLOCK#, MCACHE#, RDYSRC Valid Delay	1.5	9.2	ns	7.6	KLOCK# is Glitch Free
t82	CW/R#, CD/C#, CMI/O# Valid Delay	1.5	9.2	ns	7.6	
t83	CPWT, CPCD, CCACHE#, CSCYC Valid Delay	1.5	9.2	ns	7.6	
t84	CAHOLD, CWAY, PALLC# Valid Delay	1.5	9.2	ns	7.6	
t85	FSIOUT# Valid Delay	1.5	9.2	ns	7.6	
t86	NENE#, SMLN# Valid Delay	1.5	13	ns	7.6	
t87	APERR#, IPERR#, MAPERR# Valid Delay	1.5	9.2	ns	7.6	Glitch Free
t88	APIC# Valid Delay	1.5	13	ns	7.6	
t89	BLE# Valid Delay	1.5	9.2	ns	7.6	(35)

Table 7-24. 60 MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t90	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	12	ns	7.6	(25), (43)
t91	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	12	ns	7.10	(26), (43)
t92	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Valid Delay	1.5	11	ns	7.10	(27), (43)
t93	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Float Delay		12	ns	7.10	(28), (46)
t95	BRDY# Setup Time	6.75		ns	7.7	
t95a	CRDY# Setup Time	7.5		ns	7.7	
t96	BRDY#, CRDY# Hold Time	1		ns	7.7	
t97	BGT#, CNA#, KWEND#, SWEND# Setup Time	6.5		ns	7.7	
t98	BGT#, CNA#, KWEND#, SWEND# Hold Time	1		ns	7.7	
t100	DRCTM#, MRO#, MWB/WT# Setup Time	6.5		ns	7.7	(24)
t100a	MKEN# Setup Time	6.75		ns	7.7	(24)
t101	DRCTM#, MKEN#, MRO#, MWB/WT# Hold Time	1		ns	7.7	(24)
t110	SNPCLK Frequency	8.3	60	MHz		1X clock
t111	SNPCLK Period	16.67	120	ns	7.5	
t112	SNPCLK High Time	4		ns	7.5	
t113	SNPCLK Low Time	4		ns	7.5	
t114	SNPCLK Rise Time		1.5	ns	7.5	(38)
t115	SNPCLK Fall Time		1.5	ns	7.5	(38)
t118	SNPADS#, SNPCYC# Valid Delay	1.5	9.2	ns	7.6	Glitch Free.

Table 7-24. 60 MHz 82496 Cache Controller Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t120	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6.5		ns	7.7	(29)
t121	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7.7	(29)
t122	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	6.5		ns	7.7	(30)
t123	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	1		ns	7.7	(30)
t124	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Setup Time	1		ns	7.8	(31)
t125	MCFA0-6, MSET0-10, MTAG0-11, MAP, MBT0-3 Hold Time	6.5		ns	7.8	(31)
t130	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6.5		ns	7.7	(29)
t131	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7.7	(29)
t132	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6.5		ns	7.7	(30)
t133	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	7.7	(30)
t134	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	1		ns	7.8	(31)
t135	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	6.5		ns	7.8	(31)
t140	SNPSTB# Setup Time	6.5		ns	7.7	(29)
t141	SNPSTB# Hold Time	1		ns	7.7	(29)
t142	SNPSTB# Setup Time	6.5		ns	7.7	(30)
t143	SNPSTB# Hold Time	1		ns	7.7	(30)
t144	SNPSTB# Active Time	6.5		ns	7.16	(32)
t145	SNPSTB# Inactive Time	6.5		ns	7.16	(32)
t148	MHITM#, MTHIT#, SNPBSY# Valid Delay	1.5	11	ns	7.6	

Table 7-25. 60 MHz 82491 Cache SRAM Memory Bus Interface Timings

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t150	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time	5.5		ns	7.9	(22), (42)
t151	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time	1		ns	7.9	(23), (42)
t152	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time Refernced to Falling Edge of RESET	4		CLKs	7.9	(41), (42)
t153	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time Referenced to Falling Edge of RESET	0		CLKs	7.9	(41), (42)
t155	BRDY#, CRDY# Setup Time	5.5		ns	7.7	
t156	BRDY#, CRDY# Hold Time	1		ns	7.7	
t160	MDATA Setup to CLK (CLK before BRDY# Active)	5.5		ns	7.7	(44)
t161	MDATA Valid Delay From CLK (CLK from CDTS# Valid, MDOE# Active)		13	ns	7.6	(49)
t162	MDATA Valid Delay From MDOE# Active		8	ns	7.10	
t163	MDATA Float Delay From MDOE# Inactive		11	ns	7.10	
t165	MBE# Valid Delay	1.5	9	ns	7.6	(39)
Clocked Mode						
t170	MCLK, MOCLK Frequency		60	MHz		1X clock, (49)
t171	MCLK, MOCLK Period	16.67		ns	7.5	
t172	MOCLK High Time	4		ns	7.5	
t173	MOCLK Low Time	4		ns	7.5	
t174	MCLK High Time	5		ns	7.5	(40)
t175	MCLK Low Time	5		ns	7.5	(40)
t176	MCLK, MOCLK Rise Time		1.5	ns	7.5	
t177	MCLK, MOCLK Fall Time		1.5	ns	7.5	

Table 7-25. 60 MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
Clocked Mode						
t180	MOCLK Falling Edge To MCLK Rising Edge	2		ns		
t181	MFRZ#, MZBT# Setup Time	5		ns	7.7	Referenced to MCLK
t182	MFRZ#, MZBT# Hold Time	1		ns	7.7	Referenced to MCLK
t183	MBRDY#, MSEL#, MEOC# Setup Time	5		ns	7.7	Referenced to MCLK
t184	MBRDY#, MSEL#, MEOC# Hold Time	1		ns	7.7	Referenced to MCLK
t185	MDATA Setup Time	5		ns	7.7	Referenced to MCLK
t186	MDATA Hold Time	1		ns	7.7	Referenced to MCLK
t187	MDATA Valid Delay From MCLK•MBRDY#	2	13	ns	7.6	
t188	MDATA Valid Delay From MCLK•MEOC#	2	20	ns	7.6	
t189	MDATA Valid Delay From MCLK•MSEL#	2	18	ns	7.6	(45)
t190	MDATA Valid Delay From MOCLK	1.5	10	ns	7.6	

Table 7-25. 60 MHz 82491 Cache SRAM Memory Bus Interface Timings (Contd.)

Vcc = 5 V +/- 5%, Tcase = 0 to 85 °C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
	Strobed Mode					
t195	MEOC# High Time	8		ns	7.16	(49)
t196	MEOC# Low Time	8		ns	7.16	
t197	MISTB, MOSTB High Time	12		ns	7.16	(49)
t198	MISTB, MOSTB Low Time	12		ns	7.16	
t199	MEOC#, MISTB, MOSTB Rise Time		2	ns		
t200	MEOC#, MISTB, MOSTB Fall Time		2	ns		
t201	MSEL# High Time for Restart	8		ns	7.16	
t202	MSEL# Setup Before Transition on MISTB or MOSTB	5		ns	7.12	(49)
t203	MSEL# Hold After Transition on MISTB or MOSTB	10		ns	7.12	
t204	MSEL# Setup Before Transition on MEOC#	5		ns	7.12	
t205	MSEL# Hold After Transition on MEOC#	1		ns	7.12	
t206	MISTB, MOSTB Transition to/from MEOC# Falling Transition	10		ns		
t207	MZBT# Setup To MSEL# or MEOC# Falling Edge	5		ns	7.11	
t208	MZBT# Hold From MSEL# or MEOC# Falling Edge	1		ns	7.11	
t209	MFRZ# Setup To MEOC# Falling Edge	5		ns	7.11	
t210	MFRZ# Hold From MEOC# Falling Edge	1		ns	7.11	
t211	MDATA Setup To MISTB transition or MEOC# Falling Edge	5		ns	7.11	
t212	MDATA Hold From MISTB transition or MEOC# Falling Edge	1		ns	7.11	
t213	MDATA Valid Delay From Transition on MOSTB	2	12	ns	7.13	
t214	MDATA Valid Delay From MEOC# Falling Transition or MSEL# Deactivation	2	20	ns	7.13	

NOTES:

1. Below 60 MHz only functionality is guaranteed, the following equations provide the change in A.C. specifications required to operate at lower frequencies:

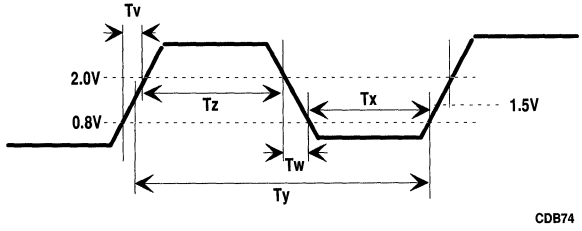
   Pentium™ processor: no effect

   82496 cache controller: (signals: SET0-10, ADS#, CFA2-6, and TAG0-11)
   Δ setup = 0.57 (Δ cycle time) +/- 0.5ns

   82491 cache SRAM: no effect
2. High times are measured between 2.0 V crossing points.
3. Low times are measured between 0.8 V crossing points.
4. Rise and Fall times are measured between 0.8 V and 2.0 V.
5. APCHK#, FERR#, HLDA, IERR#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e. glitches).
6. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/ns rise and fall times.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 16 MHz. 1ns must be added to t30 and t36 for every 10 MHz of frequency below 16 MHz.
10. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
11. FRCMC# should be tied to Vcc (high) to ensure proper operation of the Pentium processor as a master Pentium processor.
12. If configuration signals with internal pullup resistors are left floating in the system, RESET pulse width must be at least 10 microseconds.
13. CLK skew between Pentium processor and 82496 cache controller assumed to be less than 0.2ns. CLK skew is measured at 0.8V, 1.5V, and 2.0V of the rising edge of CLK.
14. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
15. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
16. This input may be driven asynchronously.
17. When driven asynchronously, NMI, FLUSH#, R/S#, INIT, and SMI must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
18. Functionality is guaranteed by design/characterization.
19. Measured on rising edge of adjacent CLKs at 1.5V.
20. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency.
21. The amount of jitter present must be accounted for as a component of CLK skew between devices.
22. Setup time is required to guarantee recognition on a specific clock.
23. Hold time is required to guarantee recognition on a specific clock.
24. Only need to meet setup and hold times during the KWEND and SWEND sample times.
25. Valid delay from CLK only if MALE or MBALE, MAOE#, MBAOE# are active.
26. Valid delay from MALE or MBALE going active, if both MAOE# and MBAOE# are active.
27. Valid delay from MAOE#, MBAOE# going active.
28. Float delay from MAOE#, MBAOE# going inactive.
29. In Synchronous mode, referenced to CLK.
30. In Clocked mode, referenced to SNPCLK.
31. In Strobed mode, referenced to SNPSTB# falling edge.
32. In Strobed mode, must meet active/inactive times.
34. To guarantee recognition on a given CLK edge.

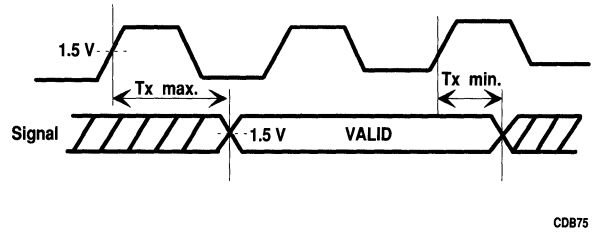
35. This signal is not used when using the 82496 cache controller with the 82491 cache SRAM.
36. For proper configuration, t70, t71, t72, and t 73 must all be met.
37. Glitch free signals monotonically transition without false transitions (i.e. glitches).
38. 1ns can be added to maximum SNPCLK rise/fall time for every 10 MHz of frequency below 60 MHz. 1ns must be added to t123 and t133 for every 10 MHz of frequency below 60 MHz.
39. From CLK in which BLEC# sampled active.
40. Tighter symmetry required since MCLK input does not use a PLL.
41. Timing is referenced to falling edge of RESET.
42. For proper configuration, t150, t151, t152, and t153 must all be met.
43. A.C. timings assume MALDRV=low on reset. If MALDRV=high on reset, add .7ns to t90, t91, and t92.
44. Must meet MDATA setup to CLK one full CLK before BRDY# active for first transfer on line fills and all non-cacheable transfers.
45. MSEL# sampled inactive resets burst counter. Data is re-driven beginning with data corresponding to first address requested.
46. Not 100% Tested. Guaranteed by design/characterization.
47. Float and Enable times measured at Vcc/2 level at gate of output device are guaranteed by design. (Not 100% tested)
48. CLK Skew between 82491 cache SRAM and other devices (Pentium processor, 82496 cache controller, and other C8Cs) assumed to be less than 0.7 ns.
49. Signal Restrictions
    a. For proper operation the following signals must have monotonic transitions:
       - CLK,
       - MCLK in clocked mode,
       - MISTB, MOSTB, and MEOC# in strobed mode.

    b. For proper operation the following signals must remain stable (must not glitch) throughout a cycle.
       - MDOE#,
       - MSEL#, when active during strobed mode.
50. All TTL timings are referenced from 1.5 V.



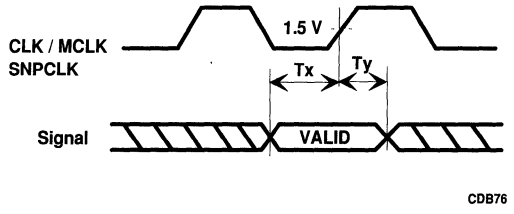
Tv = t5, t24, t114, t174
Tw = t6, t25, t115, t175
Tx = t4, t23, t113, t173
Ty = t2, t20, t111, t171
Tz = t3, t22, t112, t172

Figure 7-5. Clock Waveform



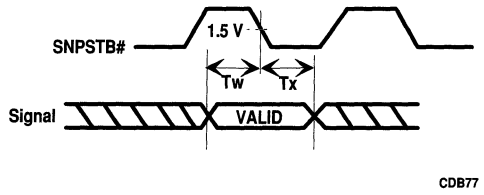
Tx = t50-t54, t66, t80-90, t118, t148, t161, t165, t187-190

Figure 7-6. Valid Delay Timings



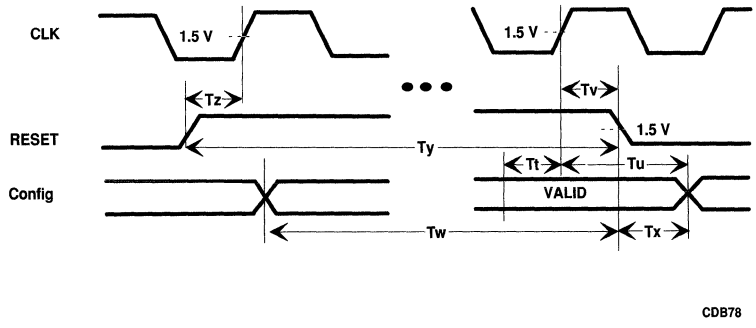
Tx = t55, t58, t60, t62, t64, t75, t95, t97, t100, t120,. t122, t130, t132, t140, t155, t160, t181, t183, t185
Ty = t56, t59, t61, t63, t65, t75, t96, t98, t101, t121, t123, t131, t133, t141, t143, t156, t182, t184, t186

Figure 7-7. Setup and Hold Timings



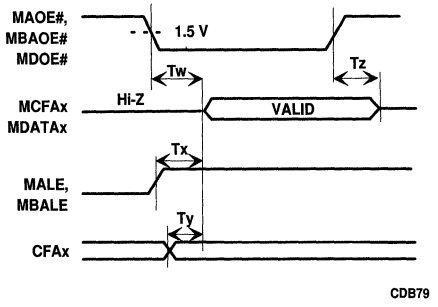
Tw = t124, t134
Tx = t125, t135

Figure 7-8. Setup and Hold Timings in Strobed Snooping Mode



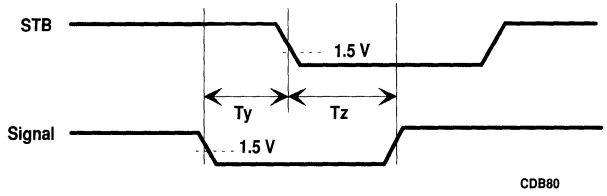
Tt = t40, t70, t150
Tu = t41, t71, t151
Tv = t9
Tw = t42, t72, t152
Tx = t43, t73, t153
Ty = t10, t13
Tz = t8

Figure 7-9. Reset and Configuration Timings



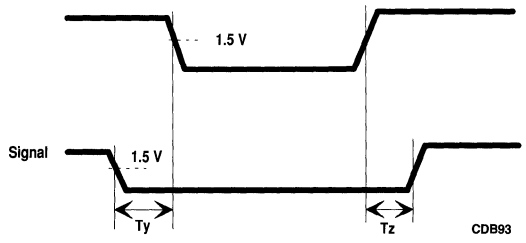
Tw = t92, t162
Tx = t91
Ty =
Tz = t93, t163

Figure 7-10. Memory Interface Timings



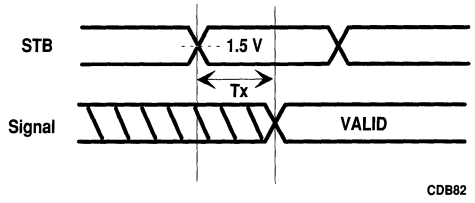
Ty = t207, t209, t211
Tz = t208, t210, t212

Figure 7-11. Setup and Hold Timings to Strobes



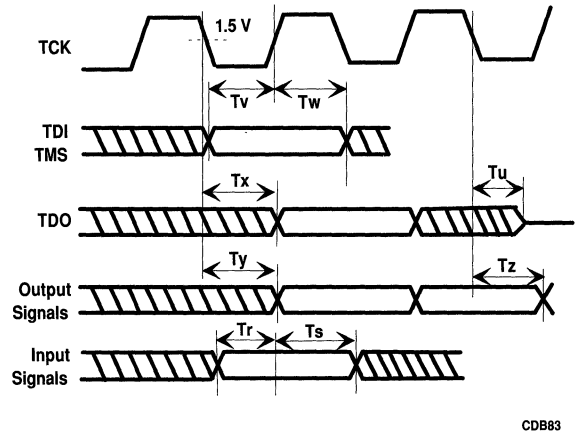
Ty = t202, t204
Tz = t203, t205

Figure 7-12. Setup and Hold Timings M_XST



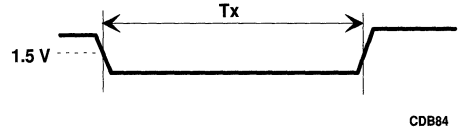
Tx = t213, t214

Figure 7-13. Valid Delay Timings from Strobes



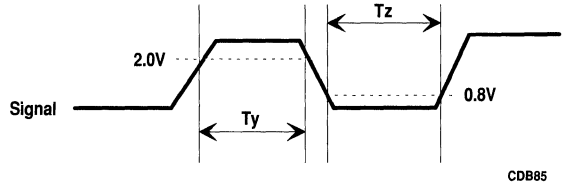
Tr = t35
Ts = t36
Tu = t32
Tv = t29
Tw = t30
Tx = t31
Ty = t33
Tz = t34

Figure 7-14. Test Timings



Tx = t28

Figure 7-15. Test Reset Timings



Ty = t145, t195, t197, t201
Tz = t144, t196, t198

Figure 7-16. Active/Inactive Timings

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays. Table 7-26 lists the buffer type to be used for each signal in the external interface.

Table 7-26. External Interface Signal Buffer Assignment

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Device	Signals	Type	Driver Buffer Type	Receiver Buffer Type
PP	A20M#, FLUSH#, FRCMC#, HOLD, IGNNE#, INIT, INTR, NMI, PEN#, R/S#, RESET, SMI#, TDI, TMS,	I	N/A	ER1
	BRDY#, BUSCHK#, TRST#	I	N/A	ER2
	CLK	I	N/A	ER3
	TCK	I	N/A	ER4
	APCHK#, BP3-0#, PM1, PM0, FERR#, HLDA, IBT, IERR#, IU, IV, PCHK#, PRDY, SMIACT#, TDO	O	ED1	N/A
CC	BRDY#, CNA#, FLUSH#, MALE, MAOE#, MBALE, MBAOE#, MKEN#, RESET, SNPCLK, SNPINV, SNPNCA, SNPSTB#, SWEND#, SYNC#, TCK, TDI, TMS, TRST#	I	N/A	ER5
	BGT#, CRDY#, KWEND#	I	N/A	ER6
	DRCTM#, MRO#, MWB/WT#	I	N/A	ER7
	CLK	I	N/A	ER8
	MAP (IN: MAOE#=1, OUT: MAOE#=0) MCFA6:0, MSET10:0, MTAG11:0 , MBT3:0 (IN:MAOE#/MBAOE#=1, OUT: MAOE#/MBAOE#=0) For MALDRV = 1 For MALDRV = 0	I/O	 ED2 ED3	 ER9 ER9
	APERR#, APIC#, BLE#, CADS#, CAHOLD, CCACHE#, CD/C#, CM/IO#, CPCD, CPWT, CSCYC, CW/R#, FSIOUT#, IPERR#, KLOCK#, MAPERR#, MCACHE#, PALLC#, RDYSRC, SNPADS#,SNPCYC#,TDO	O	ED4	N/A
	CWAY	O	ED4'	N/A
	CDTS#, MHITM#, MTHIT#, NENE#, SMLN#, SNPBSY#	O	ED5	N/A
CS	BRDY#, CRDY#, MBRDY#(MISTB), MCLK, MDOE#, MEOC#, MFRZ#, MOCLK(MOSTB), MSEL#, MZBT#, RESET, TCK, TDI, TMS	I	N/A	ER10
	MBE#	I/O	ED6	ER10'
	MDATA7-0(IN: READ CYCLE, OUT: WRITE CYCLE) For MDLDRV = 1 For MDLDRV = 0	I/O	 ED7 ED8	 ER12 ER12
	TDO	O	ED6	N/A
	CLK	I	N/A	ER11

7.7. OVERSHOOT/UNDERSHOOT GUIDELINES

The overshoot/undershoot guideline is provided to limit signals transitioning beyond Vcc or Vss due to the fast signal switching at these frequencies. Excessive ringback is the dominant harmful effect resulting from overshoot/undershoot.

Overshoot (Undershoot) is the absolute value of the maximum voltage above Vcc (below Vss). The guideline assumes the absence of diodes on the input. This guideline should be used in simulations, without the diodes present, to ensure overshoot (undershoot) is within the acceptable range.

Maximum Overshoot/Undershoot on Inputs = 1.6 Volts
(without diodes)

Ringback is the absolute value of the maximum voltage at the receiving pin below Vcc (or above Vss) relative to Vcc (or Vss) level after the signal has reached its maximum voltage level. The input diodes are assumed present. This guideline is provided to allow system designers to verify, in an actual system, the decisions made based on simulation using the overshoot (undershoot) guideline. Ringback only applies if the signal crossed above Vcc (below Vss).

Maximum Ringback on Inputs = 0.8 Volts
(with diodes)

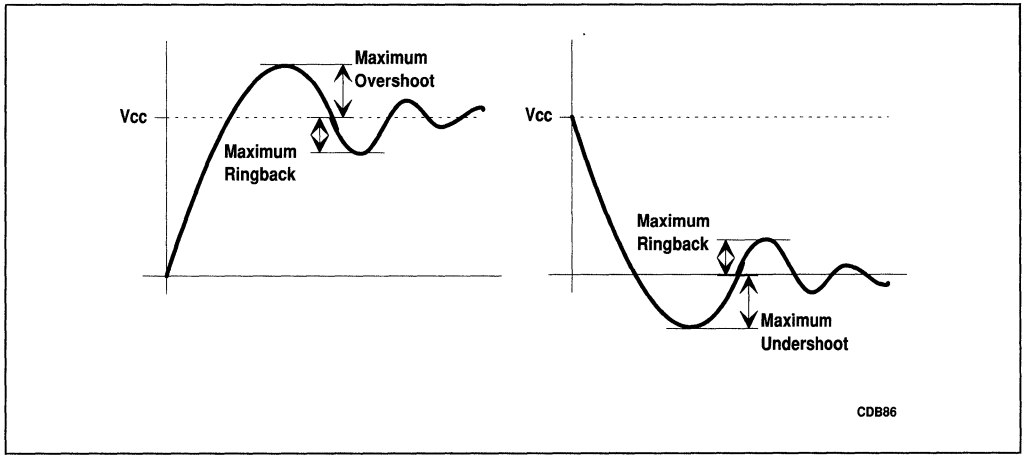


Figure 7-17. Overshoot/Undershoot and Ringback Guidelines

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8

I/O Buffer Models

CHAPTER 8
I/O BUFFER MODELS

The first order I/O buffer model is a simplified representation of the complex input and output buffers used in the Pentium processor, 82496 cache controller, and 82491 cache SRAM. Figure 8-1 shows the structure of the input buffer model and Figure 8-2 shows the output buffer model. Tables 8-1 and 8-2 shows the parameters used to specify these models.

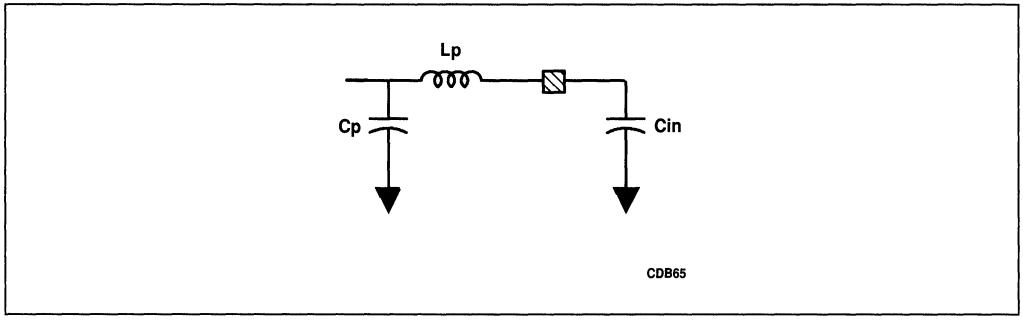

Figure 8-1. First Order Input Buffer

Table 8-1. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
Cin	Minimum and Maximum value of the capacitance of the input buffer model.
Lp	Minimum and Maximum value of the package inductance.
Cp	Minimum and Maximum value of the package capacitance.

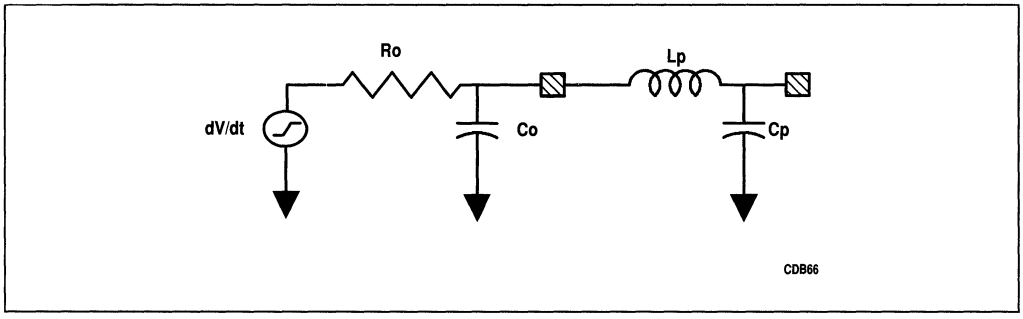

Figure 8-2. First Order Output Buffer

Table 8-2. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model.
Ro	Minimum and maximum value of the output impedance of the output buffer model.
Co	Minimum and Maximum value of the capacitance of the output buffer model.
Lp	Minimum and Maximum value of the package inductance.
Cp	Minimum and Maximum value of the package capacitance.

8.1. OPTIMIZED INTERFACE BUFFERS

Tables 8-3 and 8-4 lists the minimum and maximum parameters for each buffer type of the optimized interfaces. These parameters supply the information to use in the circuits shown in Figures 8-1 and 8-2 to model the chip sets behavior in a given environment.

Table 8-3. Specification of Input Optimized Interface Buffer Model Parameters

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Buffer Type	Device	Cp (pF)		Lp (nH)		Cin (pF)	
		min	max	min	max	min	max
ZR1	PP	1.1	1.8	6.2	11.3	2.6	3.5
ZR1a	PP	7.3	9.9	14.9	20.1	2.6	3.5
ZR2	PP	2.2	2.9	7.0	9.4	1.4	1.8
ZR3	PP	0.5	6.6	5.3	15.2	3.6	4.8
ZR4	PP	0.7	7.8	5.4	17.0	3.4	4.7
ZR5	PP	0.5	6.6	5.3	15.2	4.2	5.6
ZR6	PP	1.3	5.6	6.5	13.5	12.7	17.1
ZR7	CC	1.2	6.9	6.4	16.0	1.4	2.3
ZR7a	CC	3.9	5.3	6.4	16.0	3.6	4.8
ZR8	CC	0.5	6.5	5.3	16.0	6.0	8.0
ZR9	CS	0.5	1.5	8.0	10.0	1.3	2.4
ZR10	CS	0.5	1.5	8.0	10.0	3.3	4.5

Table 8-4. Specification of Output Optimized Interface Buffer Model Parameters

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Buffer Type	Transition	Device	dV/dt (V/nsec)		Ro (Ohms)		Co (pF)		Lp (nH)		Cp (pF)	
			min	max	min	max	min	max	min	max	min	max
ZD1	Rising	PP	4.5/3.6	5.5/1.1	21	59	3.6	4.8	6.8	18.9	1.4	9.1
	Falling	PP	4.5/2.6	5.5/1.1	18	54	3.6	4.8	6.8	18.9	1.4	9.1
ZD2	Rising	PP	4.5/3.6	5.5/1.1	21	59	3.4	4.7	5.4	17.0	0.7	7.8
	Falling	PP	4.5/2.6	5.5/1.1	18	54	3.4	4.7	5.4	17.0	0.7	7.8
ZD3	Rising	PP	4.5/3.6	5.5/1.1	21	59	4.2	5.6	5.3	15.2	0.5	6.6
	Falling	PP	4.5/2.6	5.5/1.1	18	54	4.2	5.6	5.3	15.2	0.5	6.6
ZD4	Rising	PP	4.5/3.6	5.5/1.1	21	59	3.6	4.8	5.3	15.2	0.5	6.6
	Falling	PP	4.5/2.6	5.5/1.1	18	54	3.6	4.8	5.3	15.2	0.5	6.6
ZD5	Rising	PP	4.5/3.3	5.5/0.7	11.8	26.7	12.1	16.3	6.3	10.2	1.4	2.6
	Falling	PP	4.5/2.6	5.5/0.7	9.4	25.5	12.1	16.3	6.3	10.2	1.4	2.6
ZD5a	Rising	PP	4.5/2.9	5.5/0.6	6.4	14	12.1	16.3	6.3	10.2	1.4	2.6
	Falling	PP	4.5/2.6	5.5/0.6	5	13.2	12.1	16.3	6.3	10.2	1.4	2.6
ZD6	Rising	PP	4.5/3.3	5.5/0.7	11.8	26.7	12.7	17.1	6.5	13.5	1.3	5.6
	Falling	PP	4.5/2.6	5.5/0.7	9.4	25.5	12.7	17.1	6.5	13.5	1.3	5.6
ZD6a	Rising	PP	4.5/2.9	5.5/0.6	6.4	14	12.7	17.1	6.5	13.5	1.3	5.6
	Falling	PP	4.5/2.6	5.5/0.6	5	13.2	12.7	17.1	6.5	13.5	1.3	5.6
ZD7	Rising	CC	4.5/3.6	5.5/1.1	21	59	6.0	8.0	5.3	16.0	0.5	6.5
	Falling	CC	4.5/2.6	5.5/1.1	18	54	6.0	8.0	5.3	16.0	0.5	6.5
ZD8	Rising	CC	4.5/3.6	5.5/1.1	21	59	3.2	4.4	6.8	17.3	1.5	7.3
	Falling	CC	4.5/2.6	5.5/1.1	18	54	3.2	4.4	6.8	17.3	1.5	7.3
ZD8'	Rising	CC	4.5/3.6	5.5/1.1	21	59	3.7	5.1	6.6	11.3	1.3	4.1
	Falling	CC	4.5/2.6	5.5/1.1	18	54	3.7	5.1	6.6	11.3	1.3	4.1
ZD9	Rising	CC	4.5/3.3	5.5/0.7	11.8	26.7	11.7	15.9	5.0	14.6	0.9	6.2
	Falling	CC	4.5/2.6	5.5/0.7	9.4	25.5	11.7	15.9	5.0	14.6	0.9	6.2
ZD9a	Rising	CC	4.5/2.9	5.5/0.6	6.4	14	11.7	15.9	5.0	14.6	0.9	6.2
	Falling	CC	4.5/2.6	5.5/0.6	5	13.2	11.7	15.9	5.0	14.6	0.9	6.2
ZD10	Rising	CS	4.5/3.6	5.5/1.1	21	59	3.3	4.5	8.0	10.0	0.5	1.5
	Falling	CS	4.5/2.6	5.5/1.1	18	54	3.3	4.5	8.0	10.0	0.5	1.5

When simulating the optimized interface for either Flight Time or Signal Quality, it is critical to use the appropriate buffer model specification. Table 8-5 shows the correct specifications to use in the Flight Time or Signal Quality simulations.

Table 8-5. Specifications to be Used for Simulation of Flight Time or Signal Quality

		Flight Time	Signal Quality
Driver:	dV/dt	min	max
	Co	max	min
	Ro	max	min
	Cp	max	min
	Lp	max	min
Receiver:	Cin	max	min
	Cp	max	min
	Lp	max	min
Other:	Temp.	max	min
	Vcc	min	max
	Board Zo	min	max
	tpd	max	min
	Via Capacitance	max	min

8.2. EXTERNAL INTERFACE BUFFERS

Tables 8-6 and 8-7 lists the minimum and maximum parameters for each buffer type of the external interfaces. These parameters supply the information to use in the circuits shown in Figures 8-1 and 8-2 to model the chip sets behavior in a given environment.

Table 8-6. Specification of Input External Interface Buffer Model Parameters

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Buffer Type	Device	Cp (pF)		Lp (nH)		Cin (pF)	
		min	max	min	max	min	max
ER1	PP	0.8	10.2	5.2	20.6	1.1	1.5
ER2	PP	1.4	6.8	6.7	16.5	1.7	2.3
ER3	PP	1.6	2.2	6.2	8.4	1.7	2.3
ER4	PP	2.2	2.9	7.2	9.7	1.9	2.5
ER5	CC	1.5	6.0	6.8	14.8	1.4	2.3
ER6	CC	1.7	3.5	6.2	11.5	2.6	3.5
ER7	CC	1.6	4.7	6.2	13.4	3.6	5.3
ER8	CC	1.4	1.9	5.8	7.9	2.4	3.3
ER9	CC	0.7	8.5	5.1	18.0	6.0	8.1
ER10	CS	0.5	1.5	8.0	10.0	1.3	2.4
ER10'	CS	0.5	1.5	8.0	10.0	1.3	2.4
ER11	CS	0.5	1.5	6.9	9.3	2.9	3.9
ER12	CS	0.5	1.5	8.0	10.0	5.6	7.6

Table 8-7. Specification of Output External Interface Buffer Model Parameters

Legend: PP=Pentium™ Processor, CC=82496 Cache Controller, CS=82491 Cache SRAM

Buffer Type	Transition	Device	dV/dt (V/nsec)		Ro (Ohms)		Co (pF)		Lp (nH)		Cp (pF)	
			min	max	min	max	min	max	min	max	min	max
ED1	Rising	PP	4.5/3.6	5.5/1.1	21	59	3.6	4.8	5.6	19.9	0.7	9.7
	Falling	PP	4.5/2.6	5.5/1.1	18	54	3.6	4.8	5.6	19.9	0.7	9.7
ED2	Rising	CC	4.5/3.6	5.5/1.1	21	59	6.0	8.1	5.1	18.0	0.7	8.5
	Falling	CC	4.5/2.6	5.5/1.1	18	54	6.0	8.1	5.1	18.0	0.7	8.5
ED3	Rising	CC	4.5/3.3	5.5/0.7	11.8	26.7	6.0	8.1	5.1	18.0	0.7	8.5
	Falling	CC	4.5/2.6	5.5/0.7	9.4	25.5	6.0	8.1	5.1	18.0	0.7	8.5
ED4	Rising	CC	4.5/3.6	5.5/1.1	21	59	3.2	4.4	5.4	18.7	0.8	8.2
	Falling	CC	4.5/2.6	5.5/1.1	18	54	3.2	4.4	5.4	18.7	0.8	8.2
ED4'	Rising	CC	4.5/3.6	5.5/1.1	21	59	3.9	5.3	7.2	9.8	1.7	2.3
	Falling	CC	4.5/2.6	5.5/1.1	18	54	3.9	5.3	7.2	9.8	1.7	2.3
ED5	Rising	CC	4.5/3.3	5.5/0.7	11.8	26.7	5.4	7.4	4.9	16.1	0.8	7.2
	Falling	CC	4.5/2.6	5.5/0.7	9.4	25.5	5.4	7.4	4.9	16.1	0.8	7.2
ED6	Rising	CS	4.5/3.6	5.5/1.1	21	59	3.2	4.4	8.0	10.0	0.5	1.5
	Falling	CS	4.5/2.6	5.5/1.1	18	54	3.2	4.4	8.0	10.0	0.5	1.5
ED7	Rising	CS	4.5/3.6	5.5/1.1	21	59	5.6	7.6	8.0	10.0	0.5	1.5
	Falling	CS	4.5/2.6	5.5/1.1	18	54	5.6	7.6	8.0	10.0	0.5	1.5
ED8	Rising	CS	4.5/3.3	5.5/0.7	11.8	26.7	5.6	7.6	8.0	10.0	0.5	1.5
	Falling	CS	4.5/2.6	5.5/0.7	9.4	25.5	5.6	7.6	8.0	10.0	0.5	1.5

8.3. INPUT DIODE MODELS

In addition to the input and output buffer parameters, input protection diode models are provided for the external interface I/O buffer models. These diodes have been optimized to provide ESD protection and provide some level of clamping. Note however, the signal quality specifications for both the optimized and external interfaces are defined assuming the diodes are not present in the simulation. It is important that these specifications are met because there is a limit to the amount of clamping the diode can attain. The diode model is provided because it may be useful in modeling the behavior of other devices driving transmission lines with the Pentium processor as the receiving device.

Figure 8-3 shows the components of the diode model. It consists of two diodes, one connected to Vcc, D2, and one to Vss, D1. Each diode is modeled by the combination of an ideal diode in series with a resistance.

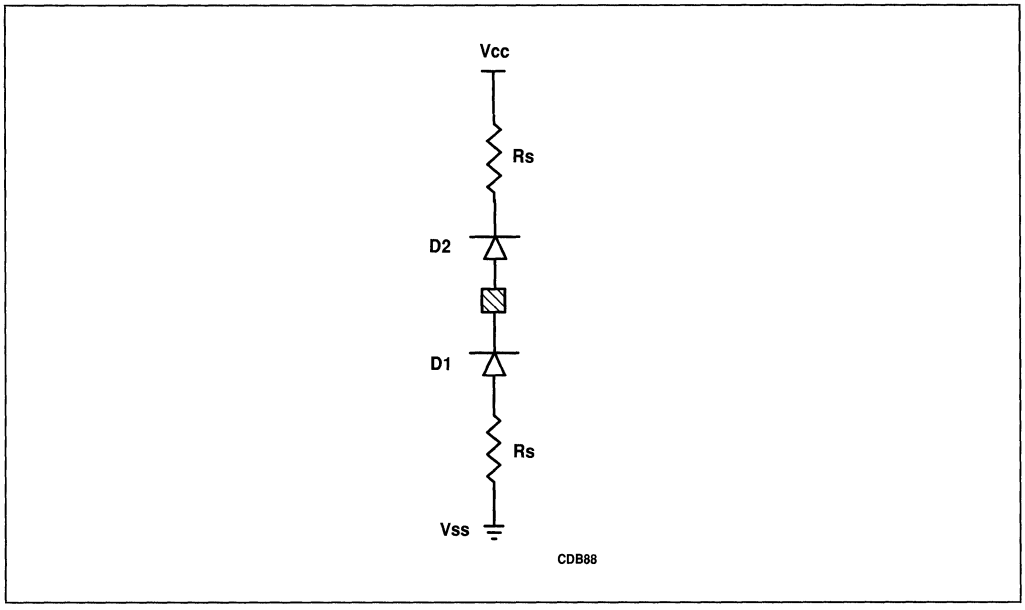

Figure 8-3. Input Diode Model

The diode model should be added to the input model for both inputs and I/O signals when desired. Figure 8-4 shows the complete input model with the diodes added.

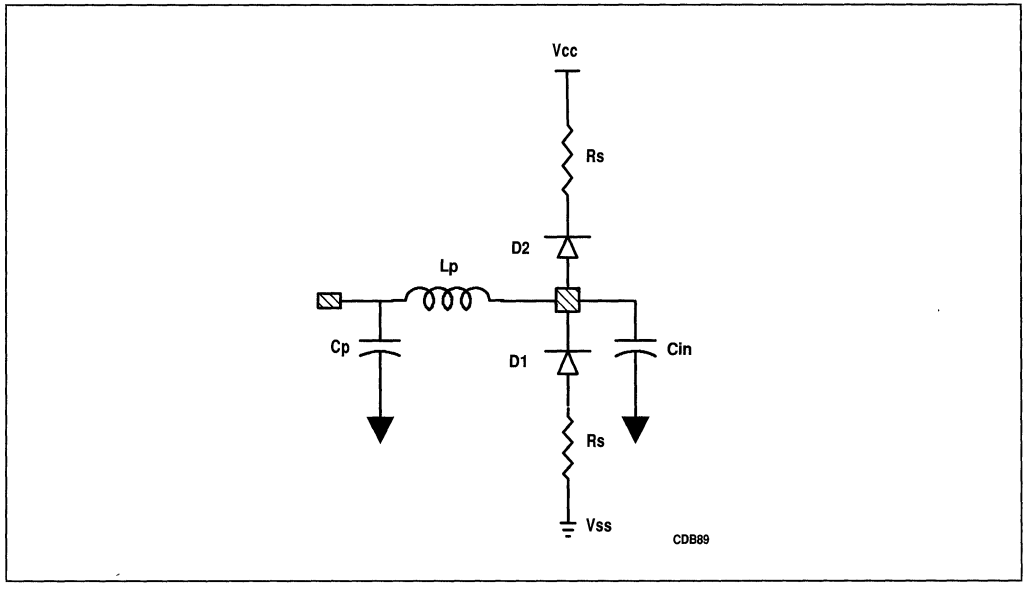

Figure 8-4. Complete Input Model Including Diode

The specific parameters associated with each diode are listed below. Table 8-8 lists the buffer types with their corresponding diode I-V curve and series resistance. Table 8-9 provides the diode I-V curve data for both D1 and D2 for each buffer type.

Table 8-8. Diode Parameter List

Input Model Type	Buffer Type	DriverMode	Diode	Diode I-V Curve Type	Rs (Ohms)
ER10'	I/O	std	D1	IV1	6.5
			D2	IV2	6.5
ER9, ER12	I/O	lg	D1	IV3	6.5
			D2	IV4	6.5
ER1, ER2, ER3, ER4, ER5, ER6, ER7, ER8, ER10, ER11	I	N/A	D1	IV5	6.5
			D2	IV6	6.5

Table 8-9. Data for Diode I-V Curves

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0v	0a	0v	0a
25mv	.0053pa	25mv	.0037pa
50mv	.0062pa	50mv	.0038pa
75mv	.0083pa	75mv	.0039pa
100mv	.0134pa	100mv	.0041pa
0.125v	.0260pa	0.125v	.0046pa
0.15v	.0572pa	0.15v	.0062pa
0.175v	0.13pa	0.175v	.0107pa
0.2v	0.33pa	0.2v	.0237pa
0.225v	0.8pa	0.225v	.0621pa
0.25v	1.98pa	0.25v	0.18pa
0.275v	4.91pa	0.275v	0.51pa
0.3v	12.18pa	0.3v	1.49pa
0.325v	30.22pa	0.325v	4.4pa
0.35v	74.98pa	0.35v	12.96pa
0.375v	0.19na	0.375v	38.22pa
0.4v	0.46na	0.4v	0.11na
0.425v	1.15na	0.425v	0.33na
0.45v	2.84na	0.45v	0.98na
0.475v	7.26na	0.475v	2.89na
0.5v	18.02na	0.5v	8.95na
0.525v	44.72na	0.525v	26.4na
0.55v	0.11ua	0.55v	77.85na
0.575v	0.28ua	0.575v	0.23ua
0.6v	0.68ua	0.6v	0.68ua
0.625v	1.69ua	0.625v	1.99ua
0.65v	4.18ua	0.65v	5.82ua

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.674v	10.26ua	0.674v	16.79ua
0.699v	24.81ua	0.698v	46.58ua
0.722v	58.06ua	0.719v	0.12ma
0.744v	0.13ma	0.737v	0.26ma
0.762v	0.25ma	0.751v	0.47ma
0.778v	0.44ma	0.762v	0.76ma
0.79v	0.69ma	0.772v	0.76ma
0.8v	1ma	0.779v	1.07ma
0.809v	0.99ma	0.784v	1.49ma
0.817v	1.32ma	0.788v	1.91ma
0.822v	1.73ma	0.792v	2.3ma
0.826v	2.13ma	0.795v	2.7ma
0.83v	2.52ma	0.798v	3.13ma
0.834v	2.93ma	0.801v	3.57ma
0.837v	3.35ma	0.803v	4.01ma
0.84v	3.79ma	0.806v	4.46ma
0.843v	4.22ma	0.808v	4.91ma
0.845v	4.67ma	0.809v	5.37ma
0.848v	5.11ma	0.811v	5.83ma
0.85v	5.57ma	0.813v	6.3ma
0.852v	6.02ma	0.814v	6.76ma
0.854v	6.48ma	0.816v	7.23ma
0.856v	6.94ma	0.817v	7.7ma
0.857v	7.4ma	0.819v	8.17ma
0.859v	7.87ma	0.82v	8.64ma
0.86v	8.34ma	0.821v	9.12ma
0.862v	8.81ma	0.822v	9.59ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.867v	10.7ma	0.826v	11.51ma
0.868v	11.17ma	0.827v	11.99ma
0.869v	11.65ma	0.828v	12.47ma
0.87v	12.13ma	0.829v	12.95ma
0.871v	12.61ma	0.83v	13.43ma
0.872v	13.09ma	0.83v	13.92ma
0.873v	13.56ma	0.831v	14.4ma
0.874v	14.05ma	0.832v	14.89ma
0.875v	14.53ma	0.833v	15.37ma
0.876v	15.01ma	0.833v	15.86ma
0.877v	15.49ma	0.834v	16.34ma
0.878v	15.97ma	0.835v	16.83ma
0.878v	16.46ma	0.835v	17.32ma
0.879v	16.94ma	0.836v	17.8ma
0.88v	17.43ma	0.836v	18.29ma
0.881v	17.91ma	0.837v	18.78ma
0.881v	18.39ma	0.838v	19.27ma
0.882v	18.88ma	0.838v	19.75ma
0.883v	19.37ma	0.839v	20.24ma
0.883v	19.85ma	0.839v	20.73ma
0.884v	20.34ma	0.84v	21.22ma
0.885v	20.83ma	0.84v	21.71ma
0.885v	21.31ma	0.841v	22.2ma
0.886v	21.8ma	0.841v	22.69ma
0.886v	22.29ma	0.842v	23.18ma
0.887v	22.78ma	0.842v	23.67ma
0.888v	23.26ma	0.843v	24.16ma

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.888v	23.75ma	0.843v	24.65ma
0.889v	24.24ma	0.844v	25.14ma
0.889v	24.73ma	0.844v	25.63ma
0.89v	25.22ma	0.845v	26.12ma
0.89v	25.71ma	0.845v	26.61ma
0.891v	26.2ma	0.845v	27.11ma
0.891v	26.69ma	0.846v	27.6ma
0.892v	27.18ma	0.846v	28.09ma
0.892v	27.67ma	0.847v	28.58ma
0.893v	28.16ma	0.847v	29.07ma
0.893v	28.65ma	0.847v	29.57ma
0.894v	29.14ma	0.848v	30.06ma
0.894v	29.63ma	0.848v	30.55ma
0.895v	30.12ma	0.848v	31.04ma
0.895v	30.61ma	0.849v	31.53ma
0.895v	31.1ma	0.849v	32.03ma
0.896v	31.59ma	0.849v	32.52ma
0.896v	32.09ma	0.85v	33.01ma
0.897v	32.58ma	0.85v	33.51ma
0.897v	33.07ma	0.85v	34ma
0.898v	33.56ma	0.851v	34.49ma
0.898v	34.05ma	0.851v	34.99ma
0.898v	34.54ma	0.851v	35.48ma
0.899v	35.04ma	0.852v	35.97ma
0.899v	35.53ma	0.852v	36.47ma
0.899v	36.02ma	0.852v	36.96ma
0.9v	36.51ma	0.853v	37.45ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.9v	37.01ma	0.853v	37.95ma
0.901v	37.5ma	0.853v	38.44ma
0.901v	37.99ma	0.854v	38.94ma
0.901v	38.49ma	0.854v	39.43ma
0.902v	38.98ma	0.854v	39.92ma
0.902v	39.47ma	0.854v	40.42ma
0.902v	39.96ma	0.855v	40.91ma
0.903v	40.46ma	0.855v	41.41ma
0.903v	40.95ma	0.855v	41.9ma
0.903v	41.44ma	0.856v	42.4ma
0.904v	41.94ma	0.856v	42.89ma
0.904v	42.43ma	0.856v	43.39ma
0.904v	42.92ma	0.856v	43.88ma
0.904v	43.42ma	0.857v	44.38ma
0.905v	43.91ma	0.857v	44.87ma
0.905v	44.41ma	0.857v	45.37ma
0.905v	44.9ma	0.857v	45.86ma
0.906v	45.39ma	0.858v	46.36ma
0.906v	45.89ma	0.858v	46.85ma
0.906v	46.38ma	0.858v	47.35ma
0.907v	46.88ma	0.858v	47.84ma
0.907v	47.37ma	0.859v	48.34ma
0.907v	47.86ma	0.859v	48.83ma
0.907v	48.36ma	0.859v	49.33ma
0.908v	48.85ma	0.859v	49.82ma
0.908v	49.35ma	0.859v	50.32ma
0.908v	49.84ma	0.86v	50.81ma

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.909v	50.34ma	0.86v	51.31ma
0.909v	50.83ma	0.86v	51.8ma
0.909v	51.33ma	0.86v	52.3ma
0.909v	51.82ma	0.861v	52.79ma
0.91v	52.32ma	0.861v	53.29ma
0.91v	52.81ma	0.861v	53.79ma
0.91v	53.3ma	0.861v	54.28ma
0.91v	53.8ma	0.861v	54.78ma
0.911v	54.29ma	0.862v	55.27ma
0.911v	54.79ma	0.862v	55.77ma
0.911v	55.28ma	0.862v	56.27ma
0.911v	55.78ma	0.862v	56.76ma
0.912v	56.27ma	0.862v	57.26ma
0.912v	56.77ma	0.863v	57.75ma
0.912v	57.27ma	0.863v	58.25ma
0.912v	57.76ma	0.863v	58.74ma
0.913v	58.26ma	0.863v	59.24ma
0.913v	58.75ma	0.863v	59.74ma
0.913v	59.25ma	0.864v	60.23ma
0.913v	59.74ma	0.864v	60.73ma
0.913v	60.24ma	0.864v	61.23ma
0.914v	60.73ma	0.864v	61.72ma
0.914v	61.23ma	0.864v	62.22ma
0.914v	61.72ma	0.864v	62.71ma
0.914v	62.22ma	0.865v	63.21ma
0.915v	62.71ma	0.865v	63.71ma
0.915v	63.21ma	0.865v	64.2ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.915v	63.71ma	0.865v	64.7ma
0.915v	64.2ma	0.865v	65.2ma
0.915v	64.7ma	0.866v	65.69ma
0.916v	65.19ma	0.866v	66.19ma
0.916v	65.69ma	0.866v	66.69ma
0.916v	66.18ma	0.866v	67.18ma
0.916v	66.68ma	0.866v	67.68ma
0.916v	67.18ma	0.866v	68.18ma
0.917v	67.67ma	0.867v	68.67ma
0.917v	68.17ma	0.867v	69.17ma
0.917v	68.66ma	0.867v	69.67ma
0.917v	69.16ma	0.867v	70.16ma
0.917v	69.66ma	0.867v	70.66ma
0.918v	70.15ma	0.867v	71.16ma
0.918v	70.65ma	0.868v	71.65ma
0.918v	71.14ma	0.868v	72.15ma
0.918v	71.64ma	0.868v	72.65ma
0.918v	72.14ma	0.868v	73.14ma

Curve Type			
IV1		IV2	
Vd	Id	Vd	Id
0.919v	72.63ma	0.868v	73.64ma
0.919v	73.13ma	0.868v	74.14ma
0.919v	73.63ma	0.868v	74.63ma
0.919v	74.12ma	0.869v	75.13ma
0.919v	74.62ma	0.869v	75.63ma
0.919v	75.11ma	0.869v	76.12ma
0.92v	75.61ma	0.869v	76.62ma
0.92v	76.11ma	0.869v	77.12ma
0.92v	76.6ma	0.869v	77.62ma
0.92v	77.1ma	0.87v	78.11ma
0.92v	77.6ma	0.87v	78.61ma
0.921v	78.09ma	0.87v	79.11ma
0.921v	78.59ma	0.87v	79.6ma
0.921v	79.09ma	0.87v	80.1ma
0.921v	79.58ma	0.87v	80.6ma
0.921v	80.08ma	0.87v	81.09ma
0.921v	80.58ma	0.871v	81.59ma
0.922v	81.07ma	0.871v	82.09ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0v	0a	0v	0a
25mv	.0098pa	25mv	.0066pa
50mv	.0113pa	50mv	.0067pa
75mv	.0149pa	75mv	.0069pa
100mv	.0238pa	100mv	.0073pa
0.125v	.0456pa	0.125v	.0083pa
0.15v	.0997pa	0.15v	.011pa
0.175v	0.23pa	0.175v	.0189pa
0.2v	0.57pa	0.2v	.0421pa
0.225v	1.39pa	0.225v	0.11pa
0.25v	3.44pa	0.25v	0.31pa
0.275v	8.51pa	0.275v	0.9pa
0.3v	21.11pa	0.3v	2.65pa
0.325v	52.38pa	0.325v	7.81pa
0.35v	0.13na	0.35v	23.01pa
0.375v	0.32na	0.375v	67.84pa
0.4v	0.8na	0.4v	0.2na
0.425v	1.99na	0.425v	0.59na
0.45v	5.07na	0.45v	1.74na
0.475v	12.59na	0.475v	5.39na
0.5v	31.24na	0.5v	15.89na
0.525v	77.52na	0.525v	46.85na
0.55v	0.19ua	0.55v	0.14ua
0.575v	0.48ua	0.575v	0.41ua
0.6v	1.18ua	0.6v	1.2ua
0.625v	2.92ua	0.625v	3.52ua

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.65v	7.2ua	0.649v	10.24ua
0.674v	17.55ua	0.674v	29.06ua
0.698v	41.74ua	0.696v	77.53ua
0.72v	94.34ua	0.716v	0.18ma
0.74v	0.2ma	0.732v	0.36ma
0.757v	0.36ma	0.744v	0.62ma
0.771v	0.59ma	0.754v	0.93ma
0.782v	0.87ma	0.762v	0.93ma
0.791v	0.87ma	0.769v	1.26ma
0.799v	1.18ma	0.773v	1.69ma
0.805v	1.58ma	0.777v	2.11ma
0.809v	1.98ma	0.781v	2.51ma
0.814v	2.37ma	0.784v	2.93ma
0.817v	2.77ma	0.786v	3.36ma
0.821v	3.19ma	0.789v	3.8ma
0.824v	3.62ma	0.791v	4.25ma
0.827v	4.05ma	0.793v	4.7ma
0.829v	4.49ma	0.795v	5.16ma
0.832v	4.94ma	0.797v	5.62ma
0.834v	5.39ma	0.799v	6.08ma
0.836v	5.84ma	0.8v	6.54ma
0.838v	6.3ma	0.802v	7.01ma
0.84v	6.76ma	0.803v	7.48ma
0.841v	7.22ma	0.805v	7.95ma
0.843v	7.69ma	0.806v	8.42ma
0.845v	8.15ma	0.807v	8.9ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.846v	8.62ma	0.808v	9.37ma
0.847v	9.09ma	0.809v	9.85ma
0.849v	9.56ma	0.81v	10.32ma
0.85v	10.04ma	0.811v	10.8ma
0.851v	10.51ma	0.812v	11.28ma
0.852v	10.99ma	0.813v	11.76ma
0.854v	11.46ma	0.814v	12.24ma
0.855v	11.94ma	0.815v	12.73ma
0.856v	12.42ma	0.816v	13.21ma
0.857v	12.9ma	0.817v	13.69ma
0.858v	13.38ma	0.817v	14.17ma
0.859v	13.86ma	0.818v	14.66ma
0.86v	14.34ma	0.819v	15.14ma
0.86v	14.82ma	0.82v	15.63ma
0.861v	15.3ma	0.82v	16.11ma
0.862v	15.78ma	0.821v	16.6ma
0.863v	16.27ma	0.822v	17.09ma
0.864v	16.75ma	0.822v	17.57ma
0.864v	17.23ma	0.823v	18.06ma
0.865v	17.72ma	0.823v	18.55ma
0.866v	18.2ma	0.824v	19.04ma
0.867v	18.69ma	0.825v	19.52ma
0.867v	19.17ma	0.825v	20.01ma
0.868v	19.66ma	0.826v	20.5ma
0.869v	20.15ma	0.826v	20.99ma
0.869v	20.63ma	0.827v	21.48ma

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.87v	21.12ma	0.827v	21.97ma
0.87v	21.61ma	0.828v	22.46ma
0.871v	22.1ma	0.828v	22.95ma
0.872v	22.58ma	0.829v	23.44ma
0.872v	23.07ma	0.829v	23.93ma
0.873v	23.56ma	0.83v	24.42ma
0.873v	24.05ma	0.83v	24.91ma
0.874v	24.54ma	0.831v	25.4ma
0.874v	25.03ma	0.831v	25.89ma
0.875v	25.52ma	0.831v	26.38ma
0.875v	26.01ma	0.832v	26.87ma
0.876v	26.49ma	0.832v	27.37ma
0.876v	26.98ma	0.833v	27.86ma
0.877v	27.47ma	0.833v	28.35ma
0.877v	27.96ma	0.833v	28.84ma
0.878v	28.46ma	0.834v	29.33ma
0.878v	28.95ma	0.834v	29.83ma
0.879v	29.44ma	0.835v	30.32ma
0.879v	29.93ma	0.835v	30.81ma
0.88v	30.42ma	0.835v	31.3ma
0.88v	30.91ma	0.836v	31.8ma
0.881v	31.4ma	0.836v	32.29ma
0.881v	31.89ma	0.836v	32.78ma
0.881v	32.38ma	0.837v	33.28ma
0.882v	32.88ma	0.837v	33.77ma
0.882v	33.37ma	0.837v	34.26ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.883v	33.86ma	0.838v	34.75ma
0.883v	34.35ma	0.838v	35.25ma
0.883v	34.84ma	0.838v	35.74ma
0.884v	35.33ma	0.839v	36.24ma
0.884v	35.83ma	0.839v	36.73ma
0.885v	36.32ma	0.839v	37.22ma
0.885v	36.81ma	0.84v	37.72ma
0.885v	37.3ma	0.84v	38.21ma
0.886v	37.8ma	0.84v	38.7ma
0.886v	38.29ma	0.84v	39.2ma
0.886v	38.78ma	0.841v	39.69ma
0.887v	39.28ma	0.841v	40.19ma
0.887v	39.77ma	0.841v	40.68ma
0.887v	40.26ma	0.842v	41.18ma
0.888v	40.76ma	0.842v	41.67ma
0.888v	41.25ma	0.842v	42.16ma
0.888v	41.74ma	0.842v	42.66ma
0.889v	42.24ma	0.843v	43.15ma
0.889v	42.73ma	0.843v	43.65ma
0.889v	43.22ma	0.843v	44.14ma
0.89v	43.72ma	0.843v	44.64ma
0.89v	44.21ma	0.844v	45.13ma
0.89v	44.7ma	0.844v	45.63ma
0.89v	45.2ma	0.844v	46.12ma
0.891v	45.69ma	0.844v	46.62ma
0.891v	46.19ma	0.845v	47.11ma

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.891v	46.68ma	0.845v	47.61ma
0.892v	47.17ma	0.845v	48.1ma
0.892v	47.67ma	0.845v	48.6ma
0.892v	48.16ma	0.846v	49.09ma
0.892v	48.66ma	0.846v	49.59ma
0.893v	49.15ma	0.846v	50.08ma
0.893v	49.65ma	0.846v	50.58ma
0.893v	50.14ma	0.847v	51.08ma
0.894v	50.64ma	0.847v	51.57ma
0.894v	51.13ma	0.847v	52.07ma
0.894v	51.63ma	0.847v	52.56ma
0.894v	52.12ma	0.847v	53.06ma
0.895v	52.61ma	0.848v	53.55ma
0.895v	53.11ma	0.848v	54.05ma
0.895v	53.6ma	0.848v	54.54ma
0.895v	54.1ma	0.848v	55.04ma
0.896v	54.59ma	0.848v	55.54ma
0.896v	55.09ma	0.849v	56.03ma
0.896v	55.58ma	0.849v	56.53ma
0.896v	56.08ma	0.849v	57.02ma
0.897v	56.57ma	0.849v	57.52ma
0.897v	57.07ma	0.849v	58.02ma
0.897v	57.56ma	0.85v	58.51ma
0.897v	58.06ma	0.85v	59.01ma
0.898v	58.56ma	0.85v	59.5ma
0.898v	59.05ma	0.85v	60ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.898v	59.55ma	0.85v	60.5ma
0.898v	60.04ma	0.851v	60.99ma
0.898v	60.54ma	0.851v	61.49ma
0.899v	61.03ma	0.851v	61.99ma
0.899v	61.53ma	0.851v	62.48ma
0.899v	62.02ma	0.851v	62.98ma
0.899v	62.52ma	0.852v	63.47ma
0.9v	63.01ma	0.852v	63.97ma
0.9v	63.51ma	0.852v	64.47ma
0.9v	64.01ma	0.852v	64.96ma
0.9v	64.5ma	0.852v	65.46ma
0.9v	65ma	0.852v	65.96ma
0.901v	65.49ma	0.853v	66.45ma
0.901v	65.99ma	0.853v	66.95ma
0.901v	66.49ma	0.853v	67.45ma
0.901v	66.98ma	0.853v	67.94ma
0.901v	67.48ma	0.853v	68.44ma
0.902v	67.97ma	0.853v	68.94ma
0.902v	68.47ma	0.854v	69.43ma
0.902v	68.96ma	0.854v	69.93ma
0.902v	69.46ma	0.854v	70.43ma
0.902v	69.96ma	0.854v	70.92ma
0.903v	70.45ma	0.854v	71.42ma

Curve Type			
IV3		IV4	
Vd	Id	Vd	Id
0.903v	70.95ma	0.854v	71.92ma
0.903v	71.45ma	0.855v	72.41ma
0.903v	71.94ma	0.855v	72.91ma
0.903v	72.44ma	0.855v	73.41ma
0.904v	72.93ma	0.855v	73.9ma
0.904v	73.43ma	0.855v	74.4ma
0.904v	73.93ma	0.855v	74.9ma
0.904v	74.42ma	0.855v	75.39ma
0.904v	74.92ma	0.856v	75.89ma
0.904v	75.42ma	0.856v	76.39ma
0.905v	75.91ma	0.856v	76.88ma
0.905v	76.41ma	0.856v	77.38ma
0.905v	76.9ma	0.856v	77.88ma
0.905v	77.4ma	0.856v	78.38ma
0.905v	77.9ma	0.856v	78.87ma
0.905v	78.39ma	0.857v	79.37ma
0.906v	78.89ma	0.857v	79.87ma
0.906v	79.39ma	0.857v	80.36ma
0.906v	79.88ma	0.857v	80.86ma
0.906v	80.38ma	0.857v	81.36ma
0.906v	80.88ma	0.857v	81.86ma
0.907v	81.37ma	0.857v	82.35ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0v	0a	0v	0a
25mv	.0009pa	25mv	.0008pa
50mv	.0012pa	50mv	.0008pa
75mv	.0022pa	75mv	.0008pa
100mv	.0044pa	100mv	.0009pa
0.125v	.0100pa	0.125v	.001pa
0.15v	.0239pa	0.15v	.0013pa
0.175v	.0584pa	0.175v	.0022pa
0.2v	0.14pa	0.2v	.0047pa
0.225v	0.36pa	0.225v	.0124pa
0.25v	0.88pa	0.25v	.0348pa
0.275v	2.19pa	0.275v	0.1pa
0.3v	5.44pa	0.3v	0.3pa
0.325v	13.49pa	0.325v	0.87pa
0.35v	33.48pa	0.35v	2.57pa
0.375v	83.09pa	0.375v	7.59pa
0.4v	0.21na	0.4v	22.37pa
0.425v	0.51na	0.425v	65.99pa
0.45v	1.27na	0.45v	0.19na
0.475v	3.15na	0.475v	0.57na
0.5v	8.05na	0.5v	1.69na
0.525v	19.97na	0.525v	5.24na
0.55v	49.56na	0.55v	15.46na
0.575v	0.12ua	0.575v	45.58na
0.6v	0.31ua	0.6v	0.13ua
0.625v	0.76ua	0.625v	0.4ua
0.65v	1.87ua	0.65v	1.17ua

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.675v	4.63ua	0.675v	3.43ua
0.699v	11.35ua	0.7v	9.97ua
0.724v	27.37ua	0.724v	28.32ua
0.747v	63.69ua	0.746v	75.71ua
0.768v	0.14ma	0.766v	0.18ma
0.787v	0.27ma	0.782v	0.36ma
0.802v	0.47ma	0.795v	0.61ma
0.814v	0.73ma	0.804v	0.92ma
0.823v	1.03ma	0.812v	0.92ma
0.832v	1.03ma	0.819v	1.25ma
0.839v	1.36ma	0.824v	1.68ma
0.845v	1.77ma	0.828v	2.1ma
0.849v	2.18ma	0.831v	2.5ma
0.853v	2.57ma	0.834v	2.92ma
0.857v	2.98ma	0.837v	3.35ma
0.86v	3.4ma	0.84v	3.79ma
0.863v	3.84ma	0.842v	4.24ma
0.865v	4.27ma	0.844v	4.69ma
0.868v	4.72ma	0.846v	5.14ma
0.87v	5.17ma	0.848v	5.6ma
0.872v	5.62ma	0.849v	6.07ma
0.874v	6.07ma	0.851v	6.53ma
0.876v	6.53ma	0.853v	7ma
0.878v	6.99ma	0.854v	7.47ma
0.88v	7.46ma	0.855v	7.94ma
0.881v	7.92ma	0.857v	8.41ma
0.883v	8.39ma	0.858v	8.88ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.884v	8.86ma	0.859v	9.36ma
0.885v	9.33ma	0.86v	9.83ma
0.887v	9.8ma	0.861v	10.31ma
0.888v	10.28ma	0.862v	10.79ma
0.889v	10.75ma	0.863v	11.27ma
0.89v	11.23ma	0.864v	11.75ma
0.891v	11.7ma	0.865v	12.23ma
0.892v	12.18ma	0.866v	12.71ma
0.894v	12.66ma	0.867v	13.2ma
0.894v	13.14ma	0.867v	13.68ma
0.895v	13.62ma	0.868v	14.16ma
0.896v	14.1ma	0.869v	14.65ma
0.897v	14.58ma	0.87v	15.13ma
0.898v	15.06ma	0.87v	15.62ma
0.899v	15.55ma	0.871v	16.1ma
0.9v	16.03ma	0.872v	16.59ma
0.901v	16.51ma	0.872v	17.07ma
0.901v	17ma	0.873v	17.56ma
0.902v	17.48ma	0.874v	18.05ma
0.903v	17.96ma	0.874v	18.54ma
0.904v	18.45ma	0.875v	19.02ma
0.904v	18.94ma	0.875v	19.51ma
0.905v	19.42ma	0.876v	20ma
0.906v	19.91ma	0.876v	20.49ma
0.906v	20.39ma	0.877v	20.98ma
0.907v	20.88ma	0.877v	21.47ma

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.907v	21.37ma	0.878v	21.96ma
0.908v	21.86ma	0.878v	22.45ma
0.909v	22.34ma	0.879v	22.94ma
0.909v	22.83ma	0.879v	23.43ma
0.91v	23.32ma	0.88v	23.92ma
0.91v	23.81ma	0.88v	24.41ma
0.911v	24.3ma	0.881v	24.9ma
0.911v	24.79ma	0.881v	25.39ma
0.912v	25.27ma	0.882v	25.88ma
0.913v	25.76ma	0.882v	26.37ma
0.913v	26.25ma	0.883v	26.86ma
0.914v	26.74ma	0.883v	27.35ma
0.914v	27.23ma	0.883v	27.85ma
0.915v	27.72ma	0.884v	28.34ma
0.915v	28.21ma	0.884v	28.83ma
0.915v	28.7ma	0.885v	29.32ma
0.916v	29.19ma	0.885v	29.81ma
0.916v	29.69ma	0.885v	30.31ma
0.917v	30.18ma	0.886v	30.8ma
0.917v	30.67ma	0.886v	31.29ma
0.918v	31.16ma	0.886v	31.78ma
0.918v	31.65ma	0.887v	32.28ma
0.919v	32.14ma	0.887v	32.77ma
0.919v	32.63ma	0.887v	33.26ma
0.919v	33.12ma	0.888v	33.76ma
0.92v	33.62ma	0.888v	34.25ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.92v	34.11ma	0.888v	34.74ma
0.921v	34.6ma	0.889v	35.24ma
0.921v	35.09ma	0.889v	35.73ma
0.921v	35.58ma	0.889v	36.22ma
0.922v	36.08ma	0.89v	36.72ma
0.922v	36.57ma	0.89v	37.21ma
0.922v	37.06ma	0.89v	37.7ma
0.923v	37.56ma	0.891v	38.2ma
0.923v	38.05ma	0.891v	38.69ma
0.923v	38.54ma	0.891v	39.19ma
0.924v	39.03ma	0.891v	39.68ma
0.924v	39.53ma	0.892v	40.17ma
0.924v	40.02ma	0.892v	40.67ma
0.925v	40.51ma	0.892v	41.16ma
0.925v	41.01ma	0.893v	41.66ma
0.925v	41.5ma	0.893v	42.15ma
0.926v	41.99ma	0.893v	42.65ma
0.926v	42.49ma	0.893v	43.14ma
0.926v	42.98ma	0.894v	43.64ma
0.927v	43.47ma	0.894v	44.13ma
0.927v	43.97ma	0.894v	44.63ma
0.927v	44.46ma	0.894v	45.12ma
0.928v	44.96ma	0.895v	45.62ma
0.928v	45.45ma	0.895v	46.11ma
0.928v	45.94ma	0.895v	46.61ma
0.929v	46.44ma	0.895v	47.1ma

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.929v	46.93ma	0.896v	47.6ma
0.929v	47.43ma	0.896v	48.09ma
0.929v	47.92ma	0.896v	48.59ma
0.93v	48.41ma	0.896v	49.08ma
0.93v	48.91ma	0.896v	49.58ma
0.93v	49.4ma	0.897v	50.07ma
0.93v	49.9ma	0.897v	50.57ma
0.931v	50.39ma	0.897v	51.06ma
0.931v	50.89ma	0.897v	51.56ma
0.931v	51.38ma	0.898v	52.05ma
0.932v	51.88ma	0.898v	52.55ma
0.932v	52.37ma	0.898v	53.04ma
0.932v	52.87ma	0.898v	53.54ma
0.932v	53.36ma	0.898v	54.04ma
0.933v	53.86ma	0.899v	54.53ma
0.933v	54.35ma	0.899v	55.03ma
0.933v	54.85ma	0.899v	55.52ma
0.933v	55.34ma	0.899v	56.02ma
0.934v	55.84ma	0.899v	56.52ma
0.934v	56.33ma	0.9v	57.01ma
0.934v	56.83ma	0.9v	57.51ma
0.934v	57.32ma	0.9v	58ma
0.934v	57.82ma	0.9v	58.5ma
0.935v	58.31ma	0.9v	59ma
0.935v	58.81ma	0.901v	59.49ma
0.935v	59.3ma	0.901v	59.99ma

Table 8-9. Data for Diode I-V Curves (Contd.)

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.935v	59.8ma	0.901v	60.48ma
0.936v	60.29ma	0.901v	60.98ma
0.936v	60.79ma	0.901v	61.48ma
0.936v	61.28ma	0.902v	61.97ma
0.936v	61.78ma	0.902v	62.47ma
0.937v	62.28ma	0.902v	62.97ma
0.937v	62.77ma	0.902v	63.46ma
0.937v	63.27ma	0.902v	63.96ma
0.937v	63.76ma	0.902v	64.45ma
0.937v	64.26ma	0.903v	64.95ma
0.938v	64.75ma	0.903v	65.45ma
0.938v	65.25ma	0.903v	65.94ma
0.938v	65.75ma	0.903v	66.44ma
0.938v	66.24ma	0.903v	66.94ma
0.938v	66.74ma	0.904v	67.43ma
0.939v	67.23ma	0.904v	67.93ma
0.939v	67.73ma	0.904v	68.43ma
0.939v	68.22ma	0.904v	68.92ma
0.939v	68.72ma	0.904v	69.42ma
0.939v	69.22ma	0.904v	69.92ma
0.94v	69.71ma	0.905v	70.41ma
0.94v	70.21ma	0.905v	70.91ma

Curve Type			
IV5		IV6	
Vd	Id	Vd	Id
0.94v	70.7ma	0.905v	71.41ma
0.94v	71.2ma	0.905v	71.9ma
0.94v	71.7ma	0.905v	72.4ma
0.941v	72.19ma	0.905v	72.9ma
0.941v	72.69ma	0.905v	73.39ma
0.941v	73.19ma	0.906v	73.89ma
0.941v	73.68ma	0.906v	74.39ma
0.941v	74.18ma	0.906v	74.88ma
0.941v	74.67ma	0.906v	75.38ma
0.942v	75.17ma	0.906v	75.88ma
0.942v	75.67ma	0.906v	76.38ma
0.942v	76.16ma	0.907v	76.87ma
0.942v	76.66ma	0.907v	77.37ma
0.942v	77.16ma	0.907v	77.87ma
0.943v	77.65ma	0.907v	78.36ma
0.943v	78.15ma	0.907v	78.86ma
0.943v	78.65ma	0.907v	79.36ma
0.943v	79.14ma	0.907v	79.85ma
0.943v	79.64ma	0.908v	80.35ma
0.943v	80.14ma	0.908v	80.85ma
0.944v	80.63ma	0.908v	81.35ma

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9

Mechanical Specifications

CHAPTER 9
MECHANICAL SPECIFICATIONS

The Pentium processor is packaged in a 273 pin ceramic pin grid array (PGA). The pins are arranged in a 21 by 21 matrix and the package dimensions are 2.16" X 2.16" (5.49cm X 5.49cm). The 82496 Cache Controller is packaged in a 280 pin ceramic pin grid array (PGA). The pins are arranged in a 19 by 19 matrix and the package dimensions are 1.95" X 1.95" (4.95cm X 4.95cm). The 82491 Cache SRAM is packaged in a 84 pin plastic quad flat pack (PQFP). The package dimensions are 0.8" X 0.8" (2.03cm X 2.03cm).

Table 9-1. CPU Cache Chip Set Package Information Summary

	Package Type	Total Pins	Pin Array	Package Size	Estimated Wattage (66Mhz)
Pentium™ Processor	PGA	273	21 x 21	2.16"x2.16" 5.49cm X 5.49cm	16
82496	PGA	280	19 x 19	1.95"x1.95" 4.95cm X 4.95cm	4.5
82491	PQFP	84	N/A	0.80"x0.80" 2.03cm X 2.03cm	2.0 1.3 (typ)

NOTE: See D.C. Specifications for more detailed power specifications.

Table 9-2. Pentium™ Processor Mechanical Specificatons

Family: Ceramic Pin Grid Array Package						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
A	2.84	3.51	Solid Lid	0.112	0.138	Solid Lid
A1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A2	2.51	3.07		0.099	0.121	
B	0.43	0.51		0.017	0.020	
D	54.61	55.11		2.150	2.170	
D1	50.67	50.93		1.995	2.005	
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	273			273		
S1	1.65	2.16		0.065	0.085	

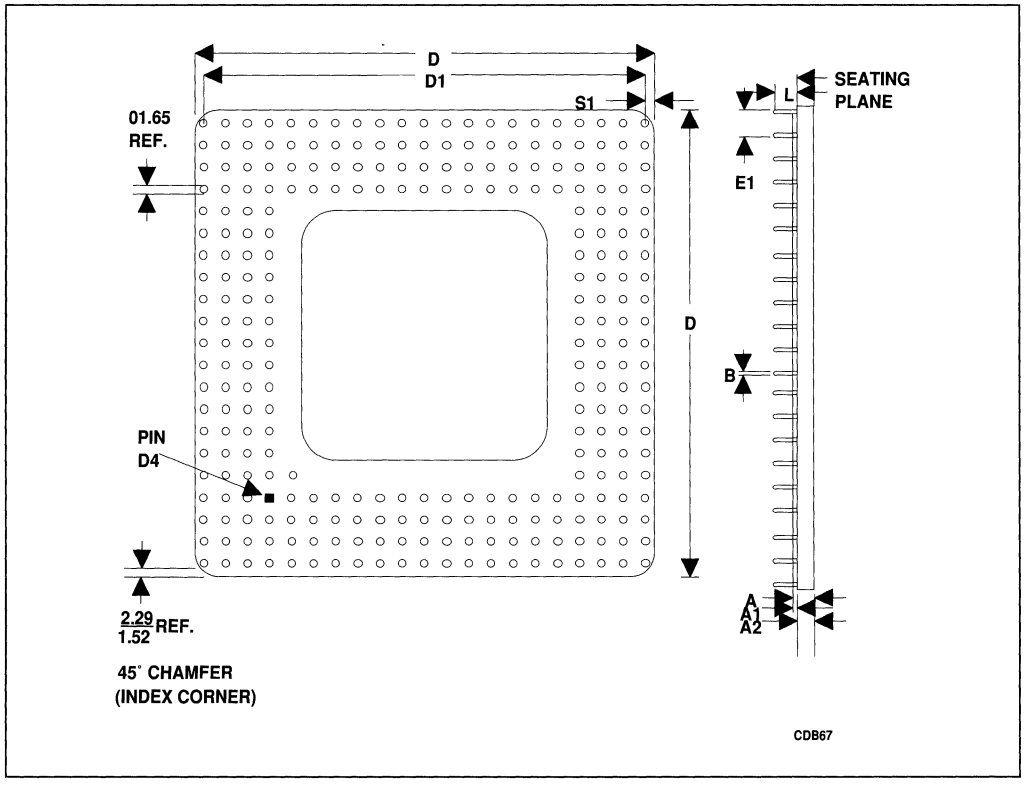

Figure 9-1. Pentium™ Processor Mechanical Specifications

Table 9-3. 82496 Cache Controller Mechanical Specificatons

Family: Ceramic Pin Grid Array Package						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
A	2.84	3.51	Solid Lid	0.112	0.138	Solid Lid
A1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A2	2.51	3.07		0.099	0.121	
B	0.43	0.51		0.017	0.020	
D	49.53	50.17		1.940	1.975	
D1	45.59	45.85		1.795	1.805	
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	280			280		
S1	1.65	2.16		0.065	0.085	

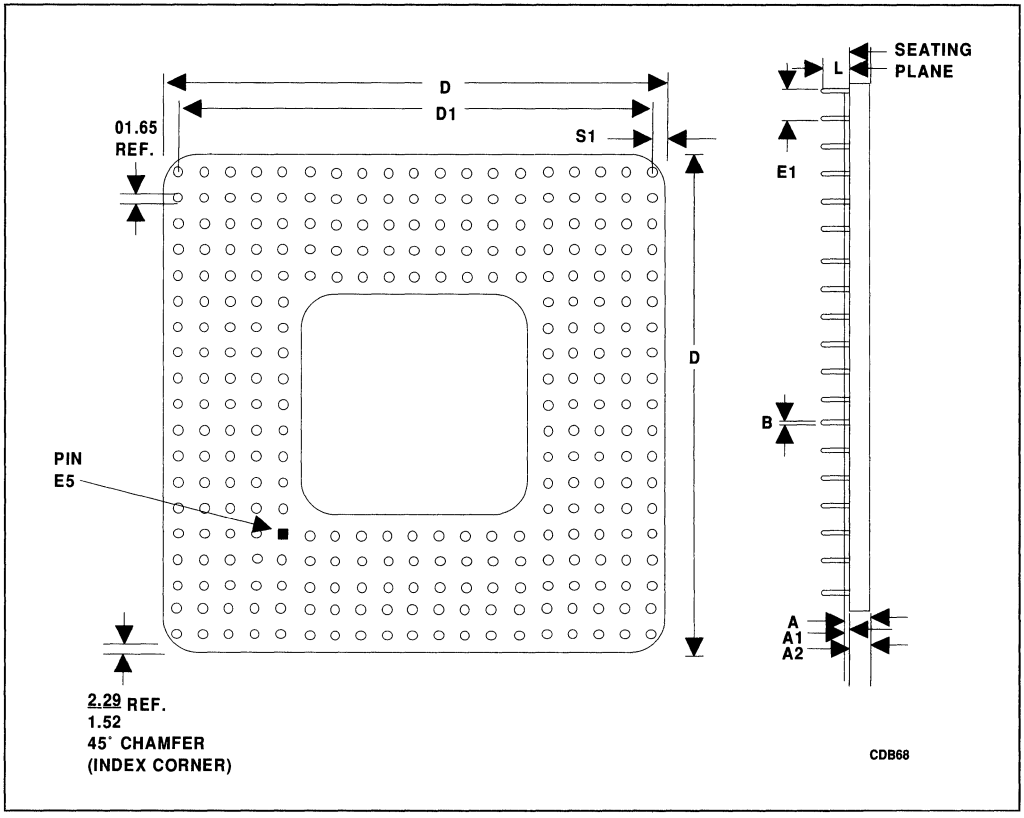

Figure 9-2. 82496 Cache Controller Mechanical Specifications

Table 9-4. 82491 Cache SRAM Mechanical Specificatons

Family: Plastic Quad Flatpack (PQFP) 0.025 in (0.635 mm) Pitch					
Symbol	**Description**	**Millimeters**		**Inches**	
		Min	**Max**	**Min**	**Max**
N	Leadcount	84		84	
A	Package Height	4.06	4.57	0.160	0.180
A1	Standoff	0.51	1.02	0.020	0.040
D, E	Terminal Dimension	19.56	20.07	0.770	0.790
D1, E1	Package Body	16.43	16.59	0.647	0.653
D2, E2	Bumper Distance	20.24	20.39	0.797	0.803
D3, E3	Lead Dimension	12.70 REF		0.500 REF	
D4, E4	Foot Radius Location	18.36	18.71	0.723	0.737
L1	Foot Length	0.51	0.76	0.020	0.030

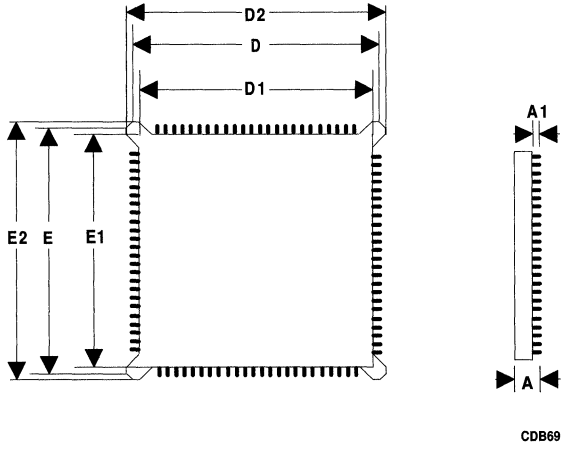

Figure 9-3. 82491 Cache SRAM Mechanical Specifications

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Thermal Specifications

CHAPTER 10
THERMAL SPECIFICATIONS

The CPU Cache Chip Set is specified for proper operation when T_C (case temperature) is within the specified range of 0°C to 85°C. To verify that the proper T_C is maintained, it should be measured at the center of the top surface (opposite of the pins) of the device in question. To ensure accurate and consistent T_C measurements, the following approach is recommended:

- Use 36 gauge or finer diameter k, t, or j type thermocouples. The laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number: OB-100).
- The thermocouple should be attached at a 90° angle as shown in the following figure. When a heat sink is attached a hole should be drilled through the heat sink to allow probing the center of the package as shown below.
- If the case temperature is measured with a heat sink attached to the package, provide a shallow grove on the contact surface of the heat sink to route the thermocouple wire out.

The measurement is made in the same way with or without a heatsink attached as shown in Figure 10-1.

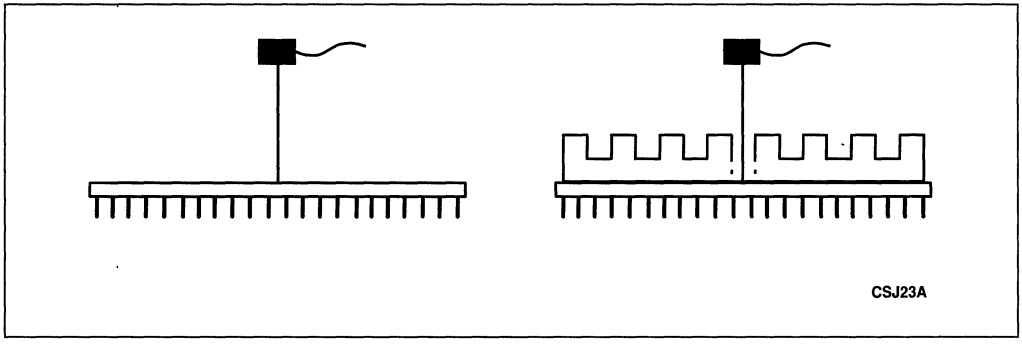

Figure 10-1. Technique For Measuring Tcase

An ambient temperature T_A is not specified directly. The only restriction is that T_C is met. To determine the allowable T_A values, the following equations may be used:

$$T_J = T_C + (P \bullet \Theta_{JC})$$

$$T_A = T_J - (P \bullet \Theta_{JA})$$

$$T_C = T_A + (P \bullet (\Theta_{JA} - \Theta_{JC}))$$

$$\Theta_{CA} = \Theta_{JA} - \Theta_{JC}$$

$$T_A = T_C - (P \bullet \Theta_{CA}).$$

Table 10-1 lists the Θ_{JC} and Θ_{CA} values for the Pentium processor.

Table 10-1. Junction-to-Case and Case-to-Ambient Thermal Resistances for the Pentium™ Processor (With and Without a Heat Sink)

	Θ_{JC}	Θ_{CA} vs Airflow (ft/min)					
		0	200	400	600	800	1000
With 0.25" Heat Sink	0.6	8.3	5.8	3.9	3.0	2.5	2.2
With 0.35" Heat Sink	0.6	7.9	5.0	3.4	2.6	2.2	2.0
With 0.65" Heat Sink	0.6	6.4	3.4	2.3	1.8	1.5	1.3
Without Heat Sink	1.2	11.6	9.4	6.7	5.4	4.6	4.2

Heat Sink: 2.05 sq. in. omni-directional fin Aluminum heat sink with 0.050 in. pin width, 0.143 in pin-to-pin center spacing and 0.150 in. base thickness.

Table 10-2 lists the Θ_{JC} and Θ_{CA} values for the 82496 cache controller.

Table 10-2. Junction-to-Case and Case-to-Ambient Thermal Resistances for the 82496 Cache Controller (With and Without a Heat Sink)

	Θ_{JC}	Θ_{CA} vs Airflow (ft/min)					
		0	200	400	600	800	1000
With 0.35" Heat Sink	1.1	9.1	6.1	4.1	3.1	2.6	2.3
Without Heat Sink	1.1	14.7	11.9	9.2	7.6	6.7	6.1

Heat Sink: 1.91 sq. in. omni-directional fin Aluminum heat sink with 0.050 in. pin width, 0.143 in pin-to-pin center spacing and 0.150 in. base thickness.

Table 10-3 lists the Θ_{JC} and Θ_{CA} values for the 82491 cache SRAM.

Table 10-3. Junction-to-Case and Caes-to-Ambient Thermal Resistances for the 82491 Cache SRAM (With and Without a Heat Sink)

	Θ_{JC}	Θ_{CA} vs Airflow (ft/min)					
		0	200	400	600	800	1000
With 0.35" Heat Sink	8.5	27.1	16.0	12.5	10.7	9.4	8.5
Without Heat Sink	8.5	34.5	26.7	22.6	19.1	16.0	14.2

Heat Sink: 0.62 sq. in. omni-directional fin Aluminum heat sink with 0.050 in. pin width, 0.143 in pin-to-pin center spacing and 0.100 in. base thickness.

NOTE

Additional heat sink and thermal information will be added as it becomes available. Contact your local Intel Sales Office for the latest information.

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11

Testability

CHAPTER 11
TESTABILITY

Two special testability features are offered in Pentium processor CPU-Cache Chip Set: Built-In Self Test (BIST) and Boundary Scan. BIST will test the Pentium processor CPU, micro-code ROM, TLB, and 82496 Cache Controller. Boundary scan test will test the interfaces among components of the Pentium processor CPU-Cache Chip Set. Normal functional testing of CPU core, 82496 Cache Controller controller logic, and 82491 Cache SRAMs can be performed by using the test data registers within the Pentium processor CPU-Cache Chip Set and external connections. The 82491 cache SRAMs can be tested using standard cache memory testing techniques to flush, write, and read the 82491 cache Controller.

The 'IEEE Standard 1149.1 Test Access Port (TAP) and Boundary Scan Architecture' is implemented to access the Pentium processor CPU-Cache Chip Set testability features, e.g. BIST and boundary scan interconnect test. There are more testability features designed around TAP and boundary scan architecture in each component. For a tutorial or details about boundary scan architecture, the user may also refer to the IEEE 1149.1 standard.

11.1. BUILT-IN SELT TEST (BIST)

The BIST tests the internal functionality of the chip set components: approximately 70% of the Pentium microprocessor, 80% of the 82496 Cache Controller cache controller, and 98% of the 82491 Cache Controller Memory devices (100% of the SRAM Array). BIST will test the Pentium processor CPU, micro code ROM, cache controller, TLB, and 82496 Cache Controller/82491 caches.

There are two ways to activate BIST of the Pentium processor and 82496 Cache Controller. The first, or conventional method, is to initialize and perform BIST is as follows:

1. Drive CRDY#[SLFTST#] LOW and MBALE[HIGHZ#] HIGH at least 10 CLKs before RESET goes inactive to initiate 82496 Cache Controller BIST.
2. Drive INIT HIGH during reset to initiate Pentium processor CPU BIST (refer to the Pentium processor CPU EDS for details).
3. Clock at least 512K cycles at normal operating frequency for Pentium processor and 90K CLKs for 82496 Cache Controller to finish the BIST. The results of Pentium processor CPU and 82496 Cache Controller BIST are indicated by the Pentium processor EAX register contents and the 82496 Cache Controller CAHOLD signal, respectively. If the BIST was successful, the Pentium processor CPU EAX register contains "0". If the 82496 Cache Controller BIST passed, CAHOLD is HIGH and can be sampled 1 CLK after FSIOUT# goes inactive.

The second way to perform Pentium processor or 82496 Cache Controller BIST, and the only way to perform 82491 Cache Controller BIST, is to activate BIST through TAP controllers and boundary scan architecture. The user needs to refer to the next section of this section and IEEE 1149.1 standard for the test mode and instruction to activate Pentium processor BIST. The

procedure is as follows:

1. Set up and initiate Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM BIST mode
   a. Ensure that all cycles are complete prior to entering BIST.
   b. Put Pentium processor, 82496 Cache Controller, or 89491 Cache SRAM TAP controllers in SHIFT-IR state (by shifting in test mode data through TMS pin).
   c. Shift in RUNBIST instructions into Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM TAP controllers instruction registers.
2. Start RUNBIST test
   a. Put Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM TAP controllers and test circuits in RUN-TEST-IDLE state (by shifting in test mode data through TMS pin).
   b. Clock CLK at least 512K cycles at normal operating frequency for Pentium processor, 90K cycles for the 82496 cache controller, and 250K cycles for the 82491 cache SRAM to complete the BIST.
   c. JTAG must remain in the RUN-TEST-IDLE state until BIST completion.
   d. RESET may not be asserted to the 82496 Cache Controller during execution of the RUNBIST instruction.
3. Examination of the RUNBIST results
   a. Set Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM component TAP controllers and test circuits in SHIFT-DR state (by shifting in test mode data through TMS pin).
   b. Shift out and examine the data of Pentium processor, 82496 Cache Controller or 82491 Cache SRAM RUNBIST registers. If BIST is successful, the contents of the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM RUNBIST registers are "0".
   c. Results must be observed via the TDO output prior to system reset or the pass/fail value will be lost.
4. If the BIST is passed, perform CPU or cache reset and then begin normal operation.

On the Pentium processor, 82496 Cache Controller, or 82491 Cache SRAM, BIST only indicates that a failure did or did not occur. BIST cannot indicate where a failure occurred.

11.2. BOUNDARY SCAN

The 'IEEE Standard 1149.1 Test Access Port (TAP) and Boundary Scan Architecture' has been implemented in the Pentium processor CPU-Cache Chip Set to test the connections between components. By implementing this feature, 100% of the Pentium processor CPU-Cache Chip Set interconnectivity can be tested. This is one method of ensuring product integrity.

The boundary scan architecture in Pentium processor CPU-Cache Chip Set is a fully boundary-scannable type design. Each component of Pentium processor CPU-Cache Chip Set has its own TAP controller, boundary scan register, bypass register, etc. The boundary scan chain

may be connected from one of the Pentium processor CPU-Cache Chip Set components' TDI signal pin to the 82496 Cache Controller, Pentium processor, eight (or more) 82961 Cache SRAMs, and then back to the original components TDO signal pin. This approach is a single-chain design. There are 403 scan cells in the Pentium processor CPU-Cache Chip Set boundary scan chain (eg. the Pentium processor contains 175 cells, the 82496 Cache Controller contains 160 cells, and the 82491 Cache SRAM contains 68 cells). System designers may add other components which have boundary scan capability to the scan chain.

11.2.1. Boundary Scan Architecture

The Pentium processor CPU-Cache Chip Set boundary scan test logic contains the following elements and features:

1. TAP - Five dedicated signal pins consisting of TMS, TCK, TDI, and TRST# input pins and TDO output pin. (Note: the 82491 Cache SRAM does not utilize the TRST# input signal.)
2. TAP controllers - All TAP circuitry is IEEE 1149.1 standard compatible.
3. Test Data Registers - There are at least four test data registers in each Pentium processor CPU-Cache Chip Set component. These are: Bypass Register, Device Identification Register, RUNBIST register, and Boundary Scan Register.
4. Instructions and Instruction Registers - Every 82496 Cache Controller and 82491 Cache SRAM component has a 4-bit instruction register which supports all public instructions. The Pentium processor has a 13-bit instruction register. The public instructions supported by the Pentium processor CPU-Cache Chip Set are: BYPASS, SAMPLE/PRELOAD, RUNBIST, and EXTEST; and optional IDCODE instruction.
5. The maximum operating frequency of boundary scan test CLK is 16 MHz.

11.2.2. Test Data Registers

The two required test data registers, Bypass and Boundary scan registers, a Device Identification register, and a RUNBIST register are provided in Pentium processor CPU-Cache Chip Set boundary scan design. The test data registers can be selected by shifting the appropriate instruction into the TAP controllers instruction registers. Table 11-1 lists the lengths of Pentium processor CPU-Cache Chip Set boundary scan test data registers.

Table 11-1. 82496 Cache Controller/82491 Cache SRAM Boundary Scan Test Data Register Length

	Pentium™ CPU	Cache Controller	Cache SRAM
Boundary scan Register	175 bits	160 bits	68 bits
BYPASS Register	1 bit	1 bit	1 bit
ID Register	32 bits	32 bits	32 bits
RUNBIST Register	1 bit	1 bit	1 bit

11.2.2.1. BYPASS REGISTER

The Bypass Register is a one-bit shift register that can be selected to reduce the length of the scan path selected within Pentium processor CPU-Cache Chip Set. This path can be selected when no test operation is being performed to allow rapid movement of test data to and from other components on the board.

11.2.2.2. BOUNDARY SCAN REGISTER

The Boundary Scan Register is a shift register containing the boundary scan cells that are built within all input and output buffers of the Pentium processor/82496 Cache Controller/82491 Cache SRAM components. Figure 11-1 shows the logical structure of the boundary scan register within each component. The data is driven out by output cells and the value of the signal is captured and compared on the corresponding input cell of a input pin. The boundary scan register is utilized for the EXTEST and SAMPLE tests. The lists and their sequence of boundary scan register of Pentium processor CPU-Cache Chip Set components are described in a later section.

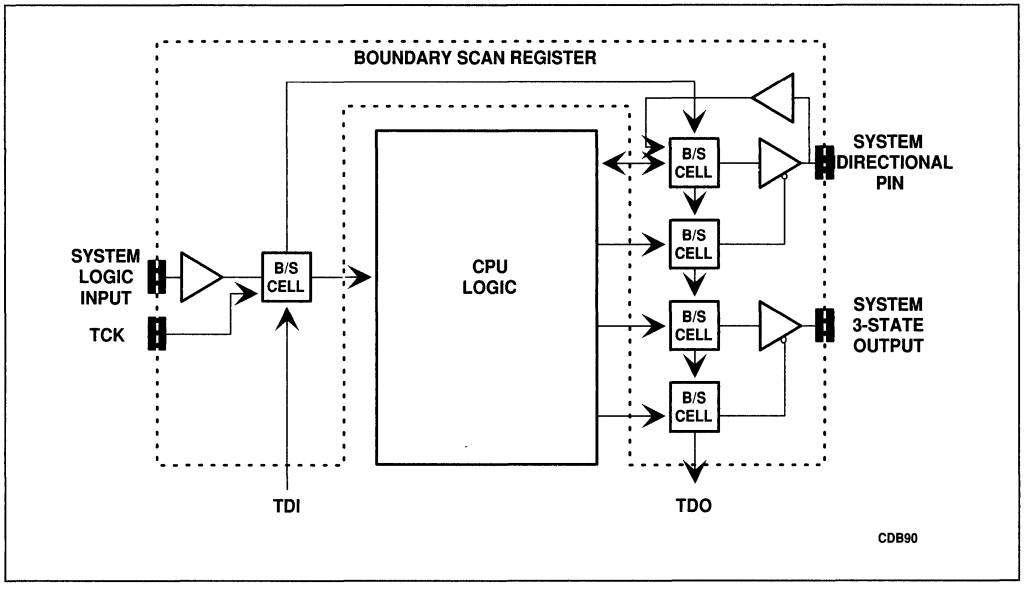

Figure 11-1. Boundary Scan Register Structure of a Component

11.2.2.3. DEVICE IDENTIFICATION REGISTER

The Device Identification Register contains the manufacturer's identification code, part number code, and version code in the format shown in Figure 11-2. The content of the Device Identification Register changes with the stepping of the 82496 Cache Controller, 82491 Cache SRAM, or Pentium processor used. Table 11-2 lists the codes for the components (Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM) used in the Pentium processor CPU-Cache Chip Set chip set.

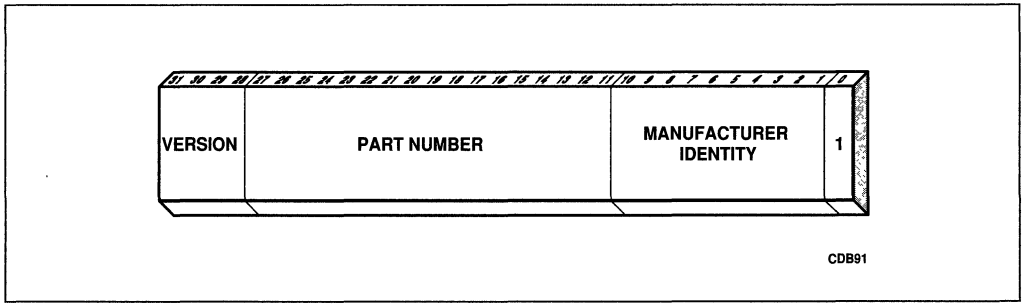

Figure 11-2. Device ID Register

Table 11-2. Pentium™ Processor CPU-Cache Chip Set Component Device Identification Code

Component	Version Code (4 bits)	Part Number Code			Manufacturer Identity (11 bits)	LSB (1 bit)	Entire ID Code (32 bits)
		(7 bits) Product Type	(9 bits) Product Specific				
			Family	Model			
Pentium™ Processor	0000	0000 001	0 101	0 0001	0000 0001 001	1	
82496 Cache Controller	0000	0000 010	0 101	0 0001	0000 0001 001	1	
82491 Cache SRAM	0000	0000 010	0 101	0 0010	0000 0001 001	1	

11.2.2.4. RUNBIST REGISTER

The RUNBIST Registers are one-bit registers used to store and report the results of the Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM BIST. The Pentium processor, 82496 Cache Controller and 82491 Cache SRAM RUNBIST registers are loaded with "0" upon successful completion and "1" upon an unsuccessful completion.

11.2.3. Instruction Register

The instruction registers of Pentium processor CPU-Cache Chip Set components are used to select the test mode and the test data register to be accessed within each Pentium processor CPU-Cache Chip Set component for one test task. The instruction registers are four bits wide for the 82496 Cache Controller and 82491 Cache SRAM. The instruction register is 13 bits wide in the Pentium processor. The MSB is connected to TDI and the LSB is connected to TDO. Upon entering the Capture-IR TAP controller state, all instruction registers within the Pentium processor CPU-Cache Chip Set are loaded with the default "0001" instruction for SAMPLE/PRELOAD.

11.2.3.1. PENTIUM PROCESSOR CPU-CACHE CHIP SET BOUNDARY SCAN INSTRUCTION SET

The Pentium processor CPU-Cache Chip Set supports all three mandatory boundary scan instructions (BYPASS, SAMPLE/PRELOAD and EXTEST) as well as two optional instructions (IDCODE and RUNBIST). Table 11-3 lists the boundary scan instruction codes of Pentium processor CPU-Cache Chip Set components. Execution of the PRIVATE instructions may cause hazardous operation and the breakage of the scan chain in the Pentium processor CPU-Cache Chip Set. Thus, it is not recommended. RESERVED instructions are not used by Intel.

Table 11-3. 82496 Cache Controller/82491 Cache SRAM Boundary Scan Instruction Codes

	Pentium™ CPU	Cache Controller	Cache SRAM
0000	EXTEST	EXTEST	EXTEST
0001	SAMPLE/PRELOAD	SAMPLE/PRELOAD	SAMPLE/PRELOAD
0010	IDCODE	IDCODE	IDCODE
0011	PRIVATE	PRIVATE	RESERVED
0100	PRIVATE	PRIVATE	PRIVATE
0101	PRIVATE	PRIVATE	RESERVED
0110	PRIVATE	PRIVATE	RESERVED
0111	RUNBIST	RUNBIST	RUNBIST
1000	PRIVATE	PRIVATE	RESERVED
1001	PRIVATE	RESERVED	RESERVED
1010	PRIVATE	RESERVED	RESERVED
1011	PRIVATE	RESERVED	RESERVED
1100	PRIVATE	RESERVED	RESERVED
1101	PRIVATE	RESERVED	RESERVED
1110	PRIVATE	RESERVED	RESERVED
1111	BYPASS	BYPASS	BYPASS

EXTEST

The instruction code is "0000". The EXTEST instruction and test mode is used to test component board interconnections. Its use is to drive test data, which is loaded into the boundary scan register output cells, through component output pins. It then allows the test data to propagate and to be captured on the corresponding boundary scan input cells. I/O pins are selected according to the types of I/O buffers and boundary scan cells designed in the boundary scan register. Values shifted into input latches in the boundary scan register should not be used to drive the internal logic of any component. Thus, when ANY individual chip set component preforms EXTEST, it must be reset before normal (non-boundary scan) operation.

SAMPLE/PRELOAD

The instruction code is "0001". SAMPLE/PRELOAD performs two functions. The test mode activated by SAMPLE/PRELOAD instruction will cause the Pentium processor CPU-Cache Chip Set components to capture a "snap-shot" of the input and output states of the component. It also allows the loading of scan cells with pre-determined data to set up component input and output conditions.

IDCODE

The instruction code is "0010". This IDCODE instruction selects the device identification register and causes the devices identification code to be loaded into ID register which can be shifted out of the components for examination. Since the device identification is coded by hardware, the data being shifted in on TDI while shifting out identification will not alter device identification.

The IDCODE instruction is forced into the Pentium processor CPU-Cache Chip Set components to allow the devices identifications to be selected whenever the TAP controller has been reset or powered-on.

BYPASS

The instruction code is "1111". The BYPASS instruction selects the bypass register for shifting the data to and from other components rapidly by reducing the shift register length to one bit when no test operation of that component is required.

RUNBIST

The instruction code is "0111". The RUNBIST instruction selects the one-bit RUNBIST register and initiates the Pentium processor CPU-Cache Chip Set BIST. The BIST of Pentium processor 82496 Cache Controller and 82491 Cache SRAM begins on the first rising edge of TCK after entering the Run-Test/Idle state. It requires at least 512K CLK (CLK) cycles at normal operating frequency in the Run-Test/Idle state to complete BIST and store the result to the RUNBIST register. After the BIST has been performed, the value in the RUNBIST register can be shifted out through TDO pin for examination. A value of "0" for Pentium processor, 82496 Cache Controller, and 82491 Cache SRAM indicates that BIST completed successfully. After executing the RUNBIST instruction, the Pentium processor CPU-Cache Chip Set must be reset before normal (non-boundary scan) operation. Note that the pass/fail indication must be read via the TDO output prior to system reset or the result will be lost. Also note that the RESET signal may not be active when the RUNBIST instruction is being executed in the JTAG controller.

11.2.4. Test Access Port (TAP) Controller

The TAP controller is a synchronous, finite state machine. It controls the sequence of operations of the test logic. The state diagram and some features for the TAP controller is shown in Figure 11-3 and this section for reference. The user should refer to IEEE 1149.1 standard for more details.

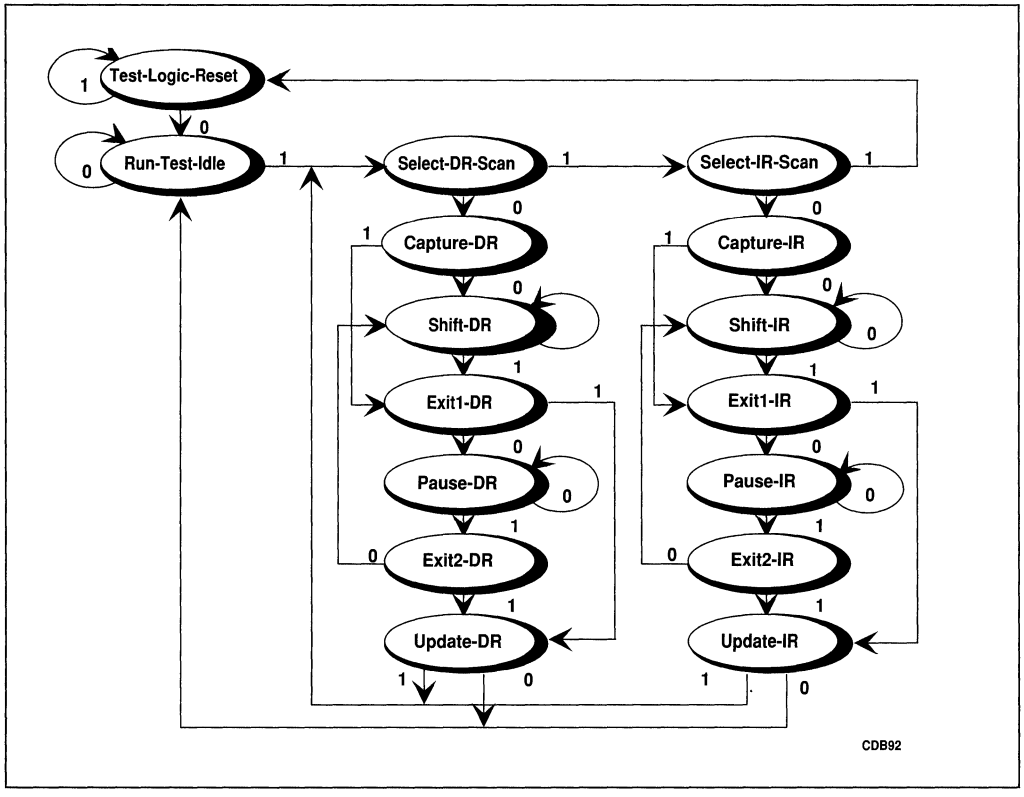

Figure 11-3. TAP Controller State Diagram

11.2.4.1. TEST-LOGIC-RESET STATE

TRST# is a test logic control pin. When asserted, it will force the TAP controller into the Test Logic Reset State (see the TAP controller state diagram, Figure 11-3).

When in Test-Logic-Reset State, the test logic is disabled so that normal operation of the device can continue unhindered. During initialization, the Pentium processor or 82496 Cache Controller initializes the instruction register such that the IDCODE instruction is loaded.

On power up, the TAP controller is automatically initialized to the test logic reset state (test logic disabled), so normal Pentium processor, 82496 Cache Controller or 82491 Cache SRAM behavior is the default. The TAP controller can also be reset by holding TMS input pin HIGH for at least five TCK clock cycles or by asserting the TRST# pin.

11.2.4.2. CAPTURE-IR STATE

The fixed binary pattern "0001" is loaded into the instruction register of the 82496 Cache Controller and 82491 Cache SRAM in Capture-IR state. The fixed binary pattern "0000000000001" is loaded into the instruction register of the Pentium processor in the Capture-IR state. This fixed pattern and the device ID can be used to isolate the fault in the Pentium processor CPU-Cache Chip Set scan chain and control mechanism.

11.2.5. Boundary Scan Register Cell

The boundary scan register for each component contains a cell for each pin, as well as cells for controlling and enabling bi-directional and tri-state cells/pins.

11.2.5.1. PENTIUM PROCESSOR BOUNDARY SCAN REGISTER CELL

The Boundary Scan Register for the Pentium processor contains a cell for each pin. There are a total of 175 cells. The following is the bit order of the Pentium processor Boundary Scan Register (left to right, top to bottom):

TDI -->

Reserved,	Reserved,	Reserved,	RESET,	FRCMC#,	PEN#,	R/S#,
NMI,	INTR,	IGNNE#,	SMI#,	INIT,	Reserved,	CLK,
Reserved,	A3,	A4,	A5,	A6,	A7,	A8,
A9,	A10,	A11,	A12,	A13,	A14,	A15,
A16,	A17,	A18,	A19,	A20,	A21,	A22,
A23,	A24,	A25,	A26,	A27,	A28,	A29,
A30,	A31,	BT0,	Disabus*,	BT1,	BT2,	BT3,
BE7#,	BE6#,	BE5#,	BE4#,	BE3#,	BE2#,	BE1#,
BE0#,	SCYC,	D/C#,	PWT,	PCD,	W/R#,	ADS#,
ADSC#,	PRDY,	AP,	LOCK#,	HLDA,	APCHK#,	PCHK#,
HIT#,	HITM#,	Disbus*,	BREQ,	SMIACT#,	A20M#,	FLUSH#,
HOLD,	WB/WT#,	EWBE#,	EADS#,	BUSCHK#,	AHOLD,	BRDYC#,
BRDY#,	KEN#,	NA#,	INV,	BOFF#,	IU,	IV,
CACHE#,	M/IO#,	BP3,	BP2,	PM1/BP1,	PM0/BP0,	Dismisc*,
FERR#,	IERR#,	Disfrc*,	DP0,	D0,	D1,	D2,
D3,	D4,	D5,	D6,	D7,	DP1,	D8,
D9,	D10,	D11,	D12,	D13,	D14,	D15,
DP2,	D16,	D17,	D18,	D19,	D20,	D21,
D22,	D23,	DP3,	D24,	D25,	D26,	D27,
D28,	D29,	D30,	D31,	DP4,	D32,	D33,
D34,	D35,	D36,	Diswr*,	D37,	D38,	D39,
DP5,	D40,	D41,	D42,	D43,	D44,	D45,
D46,	D47,	DP6,	D48,	D49,	D50,	D51,
D52,	D53,	D54,	D55,	DP7,	D56,	D57,
D58,	D59,	D60,	D61,	D62,	D63,	IBT

--> TDO

"Reserved" includes the no connect "NC" signals on the Pentium processor.

The cells marked with * are control cells that are used to select the direction of bidirectional pins or tristate the output pins. If "1" is loaded into the control cell, the associated pin(s) are tristated or selected as input. The following lists the control cells and their corresponding pins:

Disabus:	A31-A3, AP, BT3-BT0
Disbus:	ADS#, BE7-0#, CACHE#, SCYC, M/IO#, D/C#, W/R#, PWT, PCD, LOCK#
Dismisc:	BREQ, APCHK#, SMIACT#, PRDY, IU, IV, IBT, BP3, BP2, PM1/BP1, PM0/BP0, FERR#, HITM#, HIT#, PCHK#, HLDA
Disfrc:	IERR#
Diswr:	D63-D0, DP7-0

11.2.5.2. 82496 CACHE CONTROLLER BOUNDARY SCAN REGISTER CELL

The following is the listing and sequence of scan cells of the 82496 Cache Controller boundary scan register (left to right, top to bottom). There are a total of 160 cells.

TDI -->	MKEN#	KWEND#,	SWEND#,	BGT#,	CNA#,	BRDY#,
CRDY#,	MAPERR#,	APERR#,	IPERR#,	SNPBSY#,	MHITM#,	MTHIT#,
KLOCK#,	MWBWT#,	DRCTM#,	MRO#,	CWAY,	Reserved,	SMLN#,
NENE#,	EWBE#,	APIC#,	SNPCYC#,	CAHOLD,	FSIOUT#,	PALLC#,
SNPADS#,	CADS#,	CDTS#,	CWR#,	CSCYC,	CCACHE#,	CPWT,
CPCD,	CDC#,	CMIO#,	RDYSRC,	MCACHE#,	AP,	CFA3,
CFA2,	TAG11,	TAG10,	TAG9,	TAG8,	TAG7,	TAG6,
TAG5,	TAG4,	TAG3,	TAG2,	TAG1,	TAG0,	SET10,
SET9,	SET8,	SET7,	SET6,	SET5,	SET4,	SET3,
SET2,	SET1,	SET0,	CLK,	CFA6,	CFA10,	CFA9,
CFA8,	CFA7,	CFA5,	CFA4,	CFA1,	CFA0,	ADS#,
SCYC,	BLAST#,	CACHE#,	LOCK#,	BLE#,	BLEC#,	BOFF#,
KEN#,	AHOLD,	WR#,	MIO#,	DC#,	PWT,	PCD,
HITM#,	Reserved,	EADS#,	NA#,	INV,	BRDYC1#,	BRDYC2#,
WBWT#,	WAY,	WRARR#,	MCYC#,	BUS#,	MAWEA#,	WBWE#,
WBA,	WBTYP,	MCFA0,	MCFA1,	MCFA4,	MCFA5,	MCFA6,
MCFA7,	MCFA8,	MCFA9,	MCFA10,	MSET0,	MSET1,	MSET2,
MSET3,	MSET4,	MSET5,	MSET6,	MSET7,	MSET8,	MSET9,
MSET10,	MAP,	MTAG0,	MTAG1,	MTAG2,	MTAG3,	MTAG4,
MTAG5,	MTAG6,	MTAG7,	MTAG8,	MTAG9,	MTAG10,	MTAG11,
MCFA2,	MCFA3,	RESET,	MAOE#,	MBAOE#,	SNPCLK,	SNPSTB#,
SNPINV,	FLUSH#,	SYNC#,	SNPNCA,	MBALE,	MALE,	jmaoe#,
jooe#,	jcfa4oe#,	jcfa5oe#,	jcaoe#,	Reservedoe#,	jwbwtoe#,	jnaoe#,
--> TDO						

The following cells are control cells that are used to select the direction of bidirectional pins or tristate the output pins. If "1" is loaded into the control cell, the associated pin(s) are tristated or selected as input. The following lists the control cells and their corresponding pins:

jnaoe# controls	NA#
jwbwtoe# controls	WBWT#
jcaoe# controls	CFA0-CFA3, CFA6-CFA10, SET0-SET10, TAG0-TAG11, AP
jcfa5oe# controls	CFA5
jcfa4oe# controls	CFA4
jooe# controls	WBTYP, WBA, WBWE#, MAWEA#, BUS#, MCYC#, WRARR#, WAY, BRDYC2#, BRDYC1#, INV, AHOLD, KEN#, BOFF#, BLEC#, BLE#, MCACHE#, RDYSRC, CMIO#, CDC#, CPCD, CPWT, CCACHE#, CSCYC, CWR#, CDTS#, CADS#, SNPADS#, PALLC#, FSIOUT#, CAHOLD, SNPCYC#, APIC#, EWBE#, NENE#, SMLN#, CWAY, KLOCK#, MTHIT#, MHITM#, SNPBSY#, IPERR#, APERR#, MAPERR#
jmaoe# controls	MCFA0-MCFA10, MSET0-MSET10, MTAG0-MTAG11,MAP
Reservedoe# controls	Reserved (Note: Reservedoe# must be '1')

11.2.5.3. 82491 CACHE SRAM BOUNDARY SCAN REGISTER CELL

The following is the listing and order of the 82491 Cache SRAM boundary scan register (left to right, top to bottom). There are a total of 68 cells.

TDI -->						
MDATA7,	MDATA3,	MDATA6,	MDATA2,	MDATA5,	MDATA1,	MDATA4,
MDATA0,	mdataoe01,	mdataoe23,	mdataoe47,	MDOE#,	MZBT#,	MBRDY#,
MEOC#,	MFRZ#,	MSEL#,	MCLK,	MOCLK,	RESET,	CLK,
MBE#[PAR#],	mbeoe,	BLEC#,	BOFF#,	WBTYP,	WBA,	WBWE#,
BUS#,	MAWEA#,	MCYC#,	CRDY#,	WRARR#,	WAY,	cdataoe01,
cdataoe23,	cdataoe47,	CDATA4,	CDATA0,	CDATA2,	CDATA5,	CDATA6,
CDATA1,	CDATA3,	CDATA7,	WR#,	BLAST#,	BRDY#,	BRDYC#,
HITM#,	ADS#,	BE#,	A0,	A1,	A2,	A3,
A4,	A5,	A6,	A7,	A8,	A9,	A10,
A11,	A12,	A13,	A14,	A15		
--> TDO						

The following cells are control cells that are used to select the direction of bidirectional pins or tristate the output pins. If "1" is loaded into the control cell, the associated pin(s) are tristated or selected as input. The following lists the control cells and their corresponding pins:

- mdataoe01, mdataoe23, and mdataoe47 control the MDATA[7:0] pins.
- cdataoe01, cdataoe23, and cdataoe47 control the CDATA[7:0] pins.
- mbeoe controls the MBE#[PAR#] pin.

11.2.6. Boundary Scan Description Language (BSDL)

The VHDL has been used to describe component boundary scan design information by IEEE as BSDL. However, component BSDL files are not included in this documentation. The user can refer to the paper "A Language for Describing Boundary-Scan Devices" by Ken Parker, (pages 222-234 of the Proceeding in 1990 International Test Conference) or contact an Intel salesperson for more information on writing a BSDL file.

11.2.7. Boundary Scan Signal Descriptions

The functionality of TDI, TMS, TDO, TRST#, and TCK are described in Chapter 5.

11.3. 82491 CACHE SRAM TESTING

The 82491 cache SRAMs of the 82496 Cache Controller/82491 Cache SRAM can be tested using standard cache memory testing techniques. One example is shown as follows:

1. Flush and reset the Pentium processor CPU-Cache Chip Set cache

2. Write 1s to every bit of a block of memory equal to the cache size
3. Read the block of memory to fill the cache, tagging the data as read only using the MRO# signal
4. Write 0s to every bit in the block of memory
5. Read the block, the cache hits should be all 1s
6. Repeat the process, exchanging 0 for 1 and 1 for 0

In this example, the code to test the cache must be non-cacheable to the 82496 Cache Controller. Also, the CPU cache must be on so that the 82496 Cache Controller will perform line-fills.

A

Supplemental Information

APPENDIX A
SUPPLEMENTAL INFORMATION

Some non-essential information regarding the Pentium processor are considered Intel confidential and proprietary and have not been documented in this publication. This information is provided in the *Supplement to the Pentium™ Processor User's Manual* once the appropriate non-disclosure agreements are in place. Please contact Intel Corporation for details.

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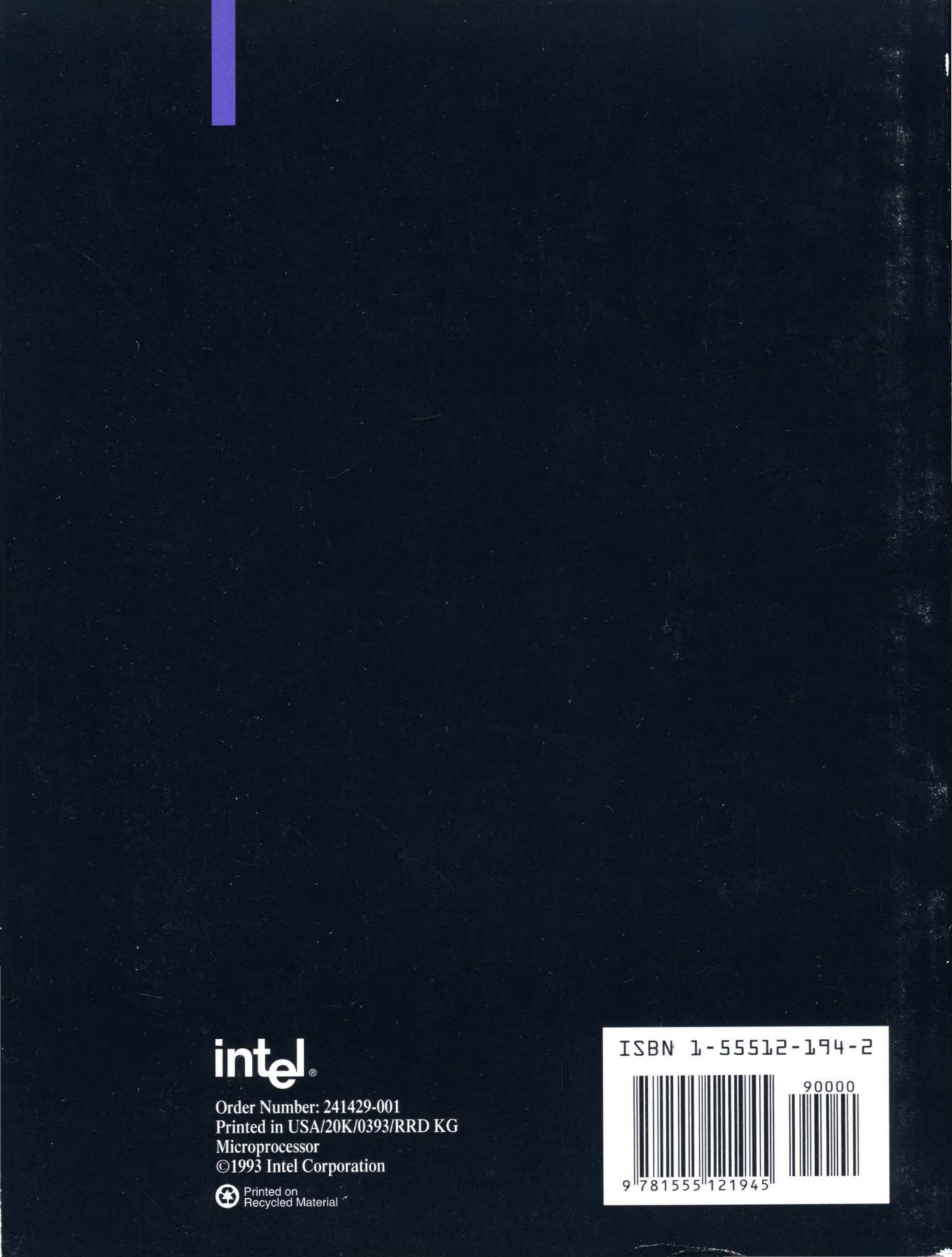

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