Intel® Pentium® 4 Processor in 478-Pin Package and Intel® 845 Chipset Platform for SDR

Design Guide

October 2002

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Revision History

Rev. No.	Description	Date
-001	Initial Release	September 2001
-002	Title changed to include SDR memory	January 2002
-003	• Updated Figure 143, "Intel® 845 Chipset Platform Using DDR-SDRAM System Memory Power Delivery Map". • Added Section 4.6.6, "Electrostatic Discharge Platform Recommendations". • Updated Table 3, "System Bus Routing Summary for the Processor". • For Intel Boxed Processor Mechanical Keep-outs, added Section 13.2 and 15.1.3. • Removed the section on 45-Watt Processor Thermal Design Power (TDP) Limitation (Section 4.6.2 in Revision –002). • Minor edits throughout for clarity.	September 2002

1 Introduction

This design guide documents Intel's design recommendations for systems based on the Intel® Pentium® 4 processor and the Intel® 845 chipset. Design issues such as thermal considerations should be addressed using specific design guides or application notes for the processor or 845 chipset.

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two following categories.

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as examples, but may not be applicable to particular designs.

Note: In this document "processor" and "Intel® Pentium® 4 processor" refer to the Intel Pentium 4 processor in the 478 pin package.

Note: The guidelines recommended in this document are based on experience and preliminary simulation work performed at Intel while developing Pentium 4 processor and 845 chipset- based systems. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics are provided in *Appendix A, Customer Reference Board Schematics*. The schematics are a reference for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 Related Documentation

Reference the following documents or models for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel. Contact the field representative for information on how to obtain Intel issued documentation.

Document	Document Number/Source
Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/design/chipsets/datashts/290725.htm
Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet	http://developer.intel.com/design/pentium4/datashts/249887.htm
Intel® Pentium® 4 Processor in the 478 Pin Package Thermal Design Guidelines	http://developer.intel.com/design/pentium4/guides/249889.htm
Intel® 845 Chipset Thermal and Mechanical Design Guidelines	http://developer.intel.com/design/chipsets/designex/298586.htm
Intel® Pentium® 4 Processor VR Down Design Guidelines	http://developer.intel.com/design/pentium4/guides/249891.htm
Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478) Design Guidelines	http://developer.intel.com/design/pentium4/guides/249890.htm
Intel® PC SDRAM Unbuffered DIMM Specification	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
Intel® PC SDRAM Specification, Revision 1.7	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
Accelerated Graphics Port Interface Specification, Revision 2.0	http://www.agpforum.org/
Low Pin Count Interface Specification, Revision 1.0	http://www.intel.com/design/chipsets/industry/lpc.htm
PCI Local Bus Specification, Revision 2.1	www.pcisig.com
PCI-PCI Bridge Specification, Revision 1.0	www.pcisig.com
PCI Bus Power Management Interface Specification, Revision 1.0	www.pcisig.com
Universal Serial Bus 1.1 Specification	http://www.usb.org/developers/docs.html
Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0b	http://www.teleport.com/~acpi/
PC'01 Specification	www.microsoft.com
PC 99 System Design Guide, Revision 1.0	http://www.microsoft.com/hwdev/pc99.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/pentium4/guides/249679.htm
Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet	http://developer.intel.com/design/chipsets/datashts/290687.htm

Document	Document Number/Source
Communication and Networking Riser (CNR) Specification, Revision 1.1	http://developer.intel.com/technology/cnr/index.htm

1.2 Conventions and Terminology

This section defines conventions and terminology that are used throughout this document.

Table 1-1. Conventions and Terminology

Convention/ Terminology	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high-logic level and termination. AGTL+ output buffers differ from GTL+ buffers by the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high-voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner means having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner means having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. Backward Crosstalk—coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. Forward Crosstalk—coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. Even Mode Crosstalk—coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. Odd Mode Crosstalk—coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Convention/ Terminology	Definition
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, and any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. Maximum and Minimum Flight Time—Flight time variations can be caused by many different variables. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions. • Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions.
GTL+	GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high-logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between one agent pin and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is observable only in simulation.
Pin	The contact point of a component package to the traces on a substrate, like the system board. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the Intel® Pentium® 4 processor. It may also be termed "system bus" in implementations where the System Bus is routed to other components. The P6 bus was the microprocessor bus of the Pentium Pro, Intel® Pentium® II, and Intel® Pentium® III processors. The System Bus is not compatible with the P6 bus.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Convention/ Terminology	Definition
SSO	Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal that falls below V_{SS} at the device pad.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VREF Guardband	A guardband defined above and below V_{REF} to provide a more realistic model accounting for noise such as V_{TT} and V_{REF} variation.

1.3 System Overview

The Pentium 4 processor with the 845 chipset delivers a high-performance and professional desktop platform solution. The processor and chipset support the System Bus protocol.

1.3.1 Intel® Pentium® 4 Processor

The Pentium 4 processor in the 478-pin package is the next generation IA-32 processor. This processor has a number of features that significantly increase its performance with respect to previous generation IA-32 processors. The Intel® NetBurst™ microarchitecture includes a number of new features as well as some improvements on existing features.

Intel NetBurst microarchitecture features include hyper-pipelined technology, rapid execution engine, 400 MHz system bus, and an execution trace cache. The hyper pipelined technology doubles the pipeline depth in the Pentium 4 processor in the 478-pin package, allowing the processor to reach much higher core frequencies. The rapid execution engine's two integer ALUs run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 400 MHz system bus is a quad-pumped bus clocked by a 100 MHz system clock, making 3.2 GB/sec data transfer rates possible. The execution trace cache is a level 1 cache that stores approximately 12K decoded micro-operations, which removes the decoder from the main execution path thereby increasing performance.

Improved features within the Intel NetBurst microarchitecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 256 KB, on-die level 2 cache with an increased bandwidth over previous microarchitectures. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. SSE2 adds 144 new instructions for double precision floating point, SIMD integer, and memory management functions.

The Pentium 4 processor in the 478-pin package supports only uni-processor configurations.

1.3.2 Intel® 845 Chipset

The 845 chipset consists of the following main components: Intel® 82045 Memory Controller Hub (MCH) and the Intel® 82801BA I/O Controller Hub 2 (ICH2). These components are interconnected via an Intel proprietary interface called Hub Interface. The hub interface is designed into the 845 chipset to provide efficient communication between components.

Additional hardware platform features include AGP 4X mode, PC 133 System memory, Ultra ATA/100, Low Pin Count interface (LPC), integrated LAN* and Universal Serial Bus. The platform is also ACPI compliant and supports Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-off power management states. Through the use of an appropriate LAN* connect, the platform supports Wake-on-LAN* for remote administration and troubleshooting.

1.3.2.1 Intel® Memory Controller Hub (MCH)

The MCH component provides the processor interface, system memory interface, AGP interface, and hub interface in an 845 chipset platform. The MCH is in a 593 ball FC-BGA package and has the following functionality:

- Supports a single processor with a data transfer rate of 400 MHz
- Supports SDR-SDRAM at 133 MHz operation. (PC133)
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5 V AGP interface with 4X SBA/data transfer and 2X/4X fast write capability
- 8-bit, 66 MHz 4X Hub Interface to the ICH2

Accelerated Graphics Port (AGP) Interface

- Supports AGP 2.0 including 1X/2X/4X AGP data transfers and 2X/4X Fast Write protocol
- Supports a single Accelerated Graphics Port (AGP) device (either via a connector or on the motherboard)
- AGP 1.5 V Connector support only. No support for 3.3 V or Universal AGP connectors.
- High-priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately

SDR–SDRAM

- Supports up to three, double-sided DIMMs (six device rows)
- Supports 64-, 128-, 256- and 512-Mb technologies for x8 and x16 devices
- All supported devices must have four banks
- Supports up to 24 simultaneous open pages
- Supports page sizes of 2 KB, 4 KB, 8 KB and 16 KB. Page size is individually selected for every row.
- 32 MB to 384 MB using 64-Mb technology; up to 1.5 GB using 256-Mb technology and up to 3 GB using 512-Mb technology
- Maximum DRAM address decode space of 4 GB
- ECC DIMM support
- 133 MHz SDRAM interface
- 64-bit data interface
- Supports only 3.3 V DIMM DRAM configurations
- No registered DIMM support
- Support for Symmetrical and Asymmetrical DRAM addressing
- Refresh Mechanism: CAS-before-RAS only
- Support for DIMM Serial Presence Detect (SPD) scheme via SMBus interface
- STR power management support via self refresh mode using CKE

1.3.2.2 Intel® I/O Controller Hub 2 (ICH2)

The ICH2 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH2 integrates:

- Upstream Hub Interface for access to the MCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- USB controller 1.1 (Expanded capabilities for 4 ports)
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- AC ’97 2.1 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Alert-on-LAN (AOL*)
- Integrated LAN Controller

The ICH2 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces. Refer to Section 8 for more information on these interfaces.

1.3.3 Bandwidth Summary

Table 1-2. lists the bandwidths of critical 845 chipset platform interfaces.

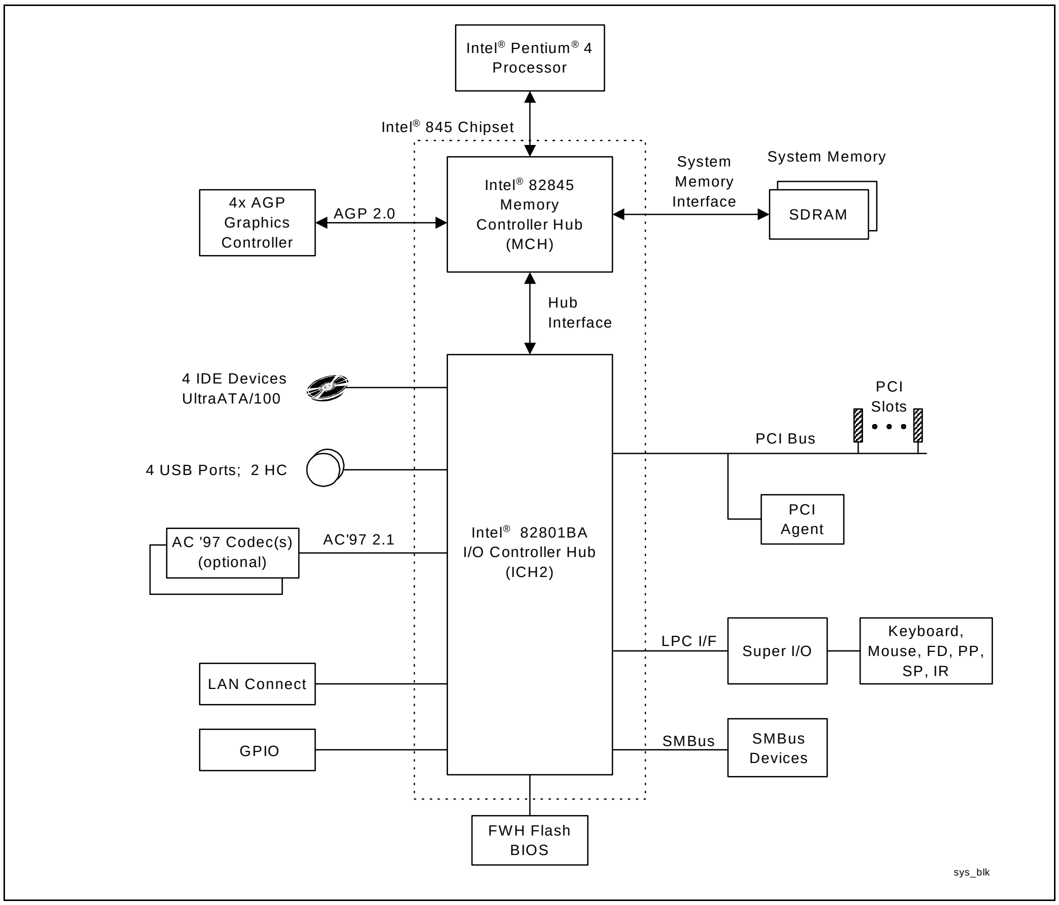
Table 1-2. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus	100	4	8	3200
AGP	66	4	4	1066
Hub Interface	66	4	1	266
PCI	33	1	4	133
SDR-SDRAM	133	1	8	1064

1.3.4 System Configurations

Figure 1-1 illustrates a typical Pentium 4 processor and 845 chipset-based system configuration for both high-performance desktop and mainstream desktop applications.

Figure 1-1. Typical System Configuration



1.4 Platform Initiatives

1.4.1 Intel® 845 Chipset

1.4.1.1 Processor/Host Interface (System Bus)

- Supports single processor
- System Bus interrupt delivery
- Supports 400 MHz System Bus
- 32-bit host bus addressing, allowing the processor to access the entire 4 GB of the MCH memory address space.

1.4.1.2 System Memory Interface

The system memory interface delivers high bandwidth to Pentium 4 processors. The MCH SDR-SDRAM interface runs at 133 MHz, delivering 1 GB/s of memory bandwidth.

The 845 chipset supports Suspend-to-RAM power management through system memory self-refresh mode using the SCKE signal.

1.4.1.3 Accelerated Graphics Port (AGP)

AGP is a high-performance, component-level interconnect that is designed for 3D graphical display applications. AGP is based on a set of performance extensions and enhancements to the PCI bus. The 845 chipset employs an AGP interface that is optimized for a point-to-point topology using 1.5 V signaling in 4X mode. The 4X mode provides a peak bandwidth of 1066 MB/s.

For additional information, refer to the *Accelerated Graphics Port Interface Specification, Rev. 2.0* located at: http://www.agpforum.org.

1.4.2 Intel® ICH2

1.4.2.1 Integrated LAN Controller

The ICH2 incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN connect components that can be used for specific market segments. The Intel® 82562EH component provides a HomePNA* 1-Mbit/sec connection. The Intel® 82562ET provides a basic Ethernet 10/100 connection. The Intel® 82562EM component provides an Ethernet 10/100 connection with the added flexibility of Alert on LAN*.

1.4.2.2 Ultra ATA/100 Support

The ICH2 supports the IDE controller with two sets of interface signals (primary and secondary) that can be independently enabled, tri-stated or driven low. The component supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33, multiword PIO modes for transfers up to 100 Mbytes/sec.

1.4.2.3 Expanded USB 1.1 Support

The ICH2 contains two USB1.1 Host Controllers. Each Host Controller includes a root hub with two separate USB ports, for a total of four USB ports.

1.4.2.4 AC ’97 6-Channel Support

The *Audio Codec ’97 (AC ’97) Specification* defines a digital interface that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC), or both an AC and an MC. The AC ’97 Specification defines the interface between the system logic and the audio or modem codec known as the “AC-link.”

The ICH2 platform’s AC ’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC-link. Using ICH2 integrated AC-link reduces cost and eases migration from ISA.

By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the ICH2 platform. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. The ICH2 integrated digital link allows several external codecs to be connected to the ICH2. The system designer can provide audio with an audio codec, a modem with a modem codec, and can provide audio or modem with an integrated audio/modem codec (Figure 1-2). The digital link is expanded to support two audio codecs or a combination of an audio and modem codec (Figure 1-3 and Figure 1-4).

Modem implementation for different countries must be considered because telephone systems vary. By using a split design, the audio codec can be on-board, and the modem codec can be placed on a riser. Intel is developing an AC-link connector. With a single integrated codec (or AMC) both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH2 is AC ’97, Revision 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high-quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

The ICH2 expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Woofer for a complete surround sound effect. The ICH2 has expanded support for two audio codecs on the AC-link.

Figure 1-2. AC ’97 with Audio/Modem Codec

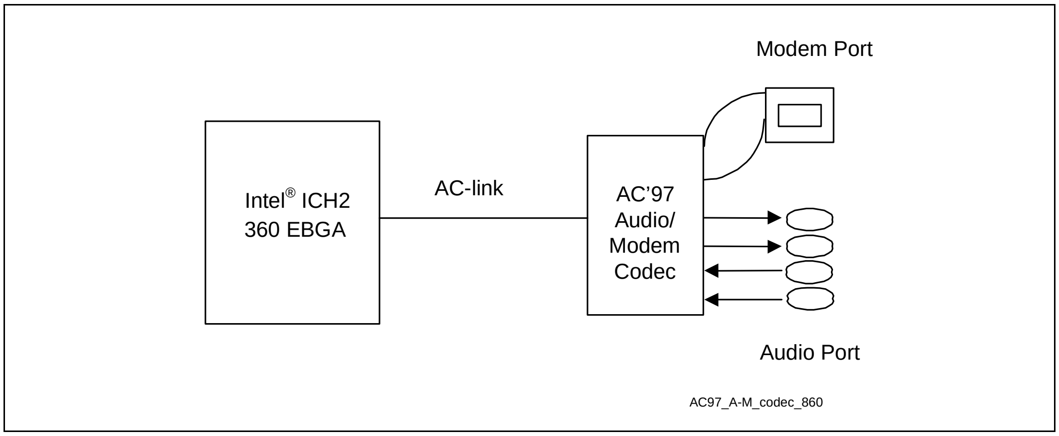


Figure 1-3. AC ’97with Audio Codecs (4 Channel Secondary)

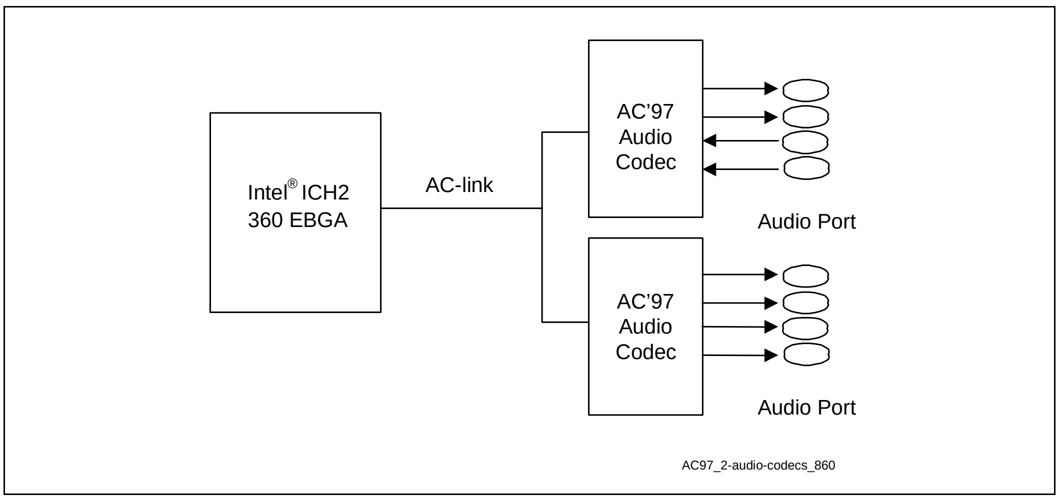
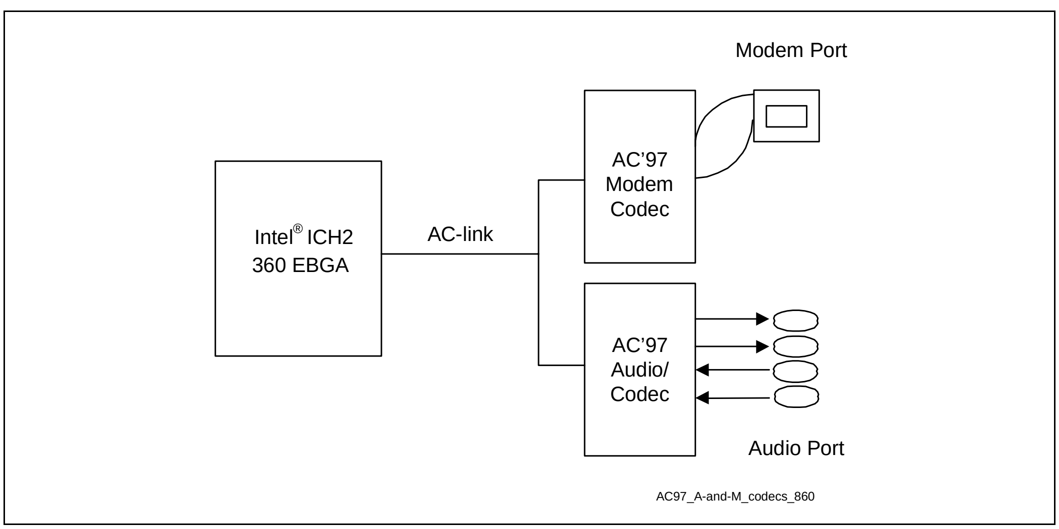


Figure 1-4. AC ’97 with Audio and Modem Codecs



1.4.3 Manageability and Other Enhancements

The ICH2 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external micro controller.

1.4.3.1 SMBus

The ICH2 integrates an SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on DIMMs, and thermal sensors. The slave interface of the SMBus controller allows an external microcontroller to access system resources.

The ICH2 platform integrates several functions designed to expand the capability of interfacing several components to the system.

1.4.3.2 Interrupt Controller

The interrupt capability of the ICH2 expands support for up to 8 PCI interrupt pins and PCI 2.2 Message-Based Interrupts. In addition, the ICH2 supports system bus interrupt delivery.

1.4.4 PC ’99/’01 Platform Compliance

PC ’99 and PC ’01 are intended to provide guidelines for hardware design that will result in optimal user experience, particularly when the hardware is used with the Microsoft Windows* family of operating systems. This document includes PC ’99 and PC ’01 requirements and recommendations for basic consumer and office implementations such as desktop, mobile, and workstation systems, and entertainment PCs. This document includes guidelines that address the following design issues:

- Design requirements for specific types of system that will run either Microsoft Windows* 98, Windows* 2000 or Windows* Me operating systems.
- Design requirements related to OnNow design initiative, including requirements related to ACPI, Plug and Play device configuration, and power management in PC systems.
- Manageability requirements that focus on improving Microsoft Windows 98, Windows 2000 and Windows Me, with the end goal of reducing TCO.
- Clarification and additional design requirements for devices supported by Microsoft Windows 98, Windows 2000 and Windows Me, including new graphics and video device capabilities, DVD, scanners and digital cameras, and other devices.

Refer to the PC ’99 System Design Guide and PC ’01 System Design Guide at http://www.pcdesguide.org/ for additional information.

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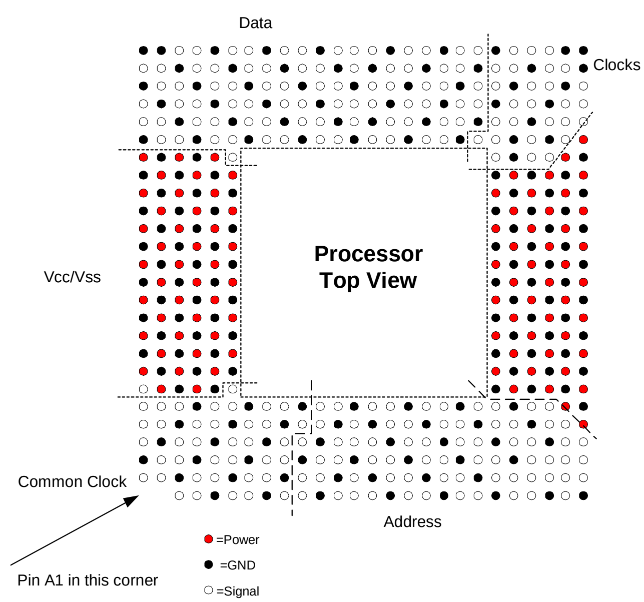
2 Component Quadrant Layout

The quadrant layout figures do not show the exact component ball count. The figures show only general quadrant information that is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Reference the following documents for pin or ball assignment information.

- *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet*
- *Intel® 845 Chipset: Intel® 82845 Memory Controller Hub (MCH) For SDR Datasheet*
- *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet*

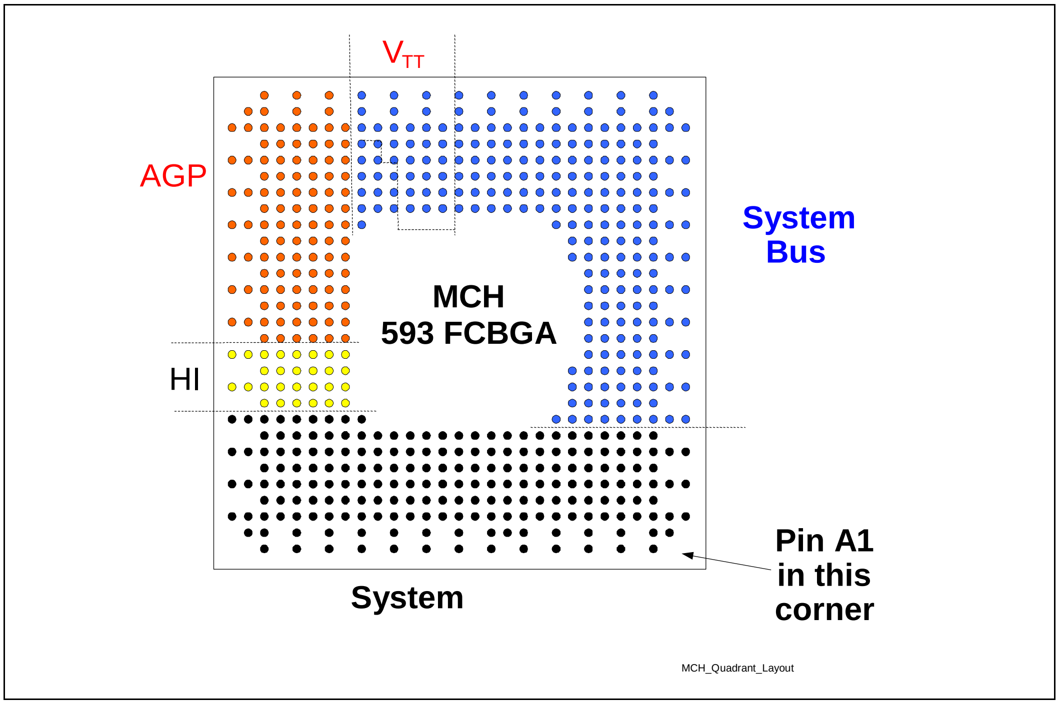
2.1 Intel® Pentium® 4 Processor Component Quadrant Layout

Figure 2-1. Pentium® 4 Processor Component Quadrant Layout (Top View–478 Pin Package)



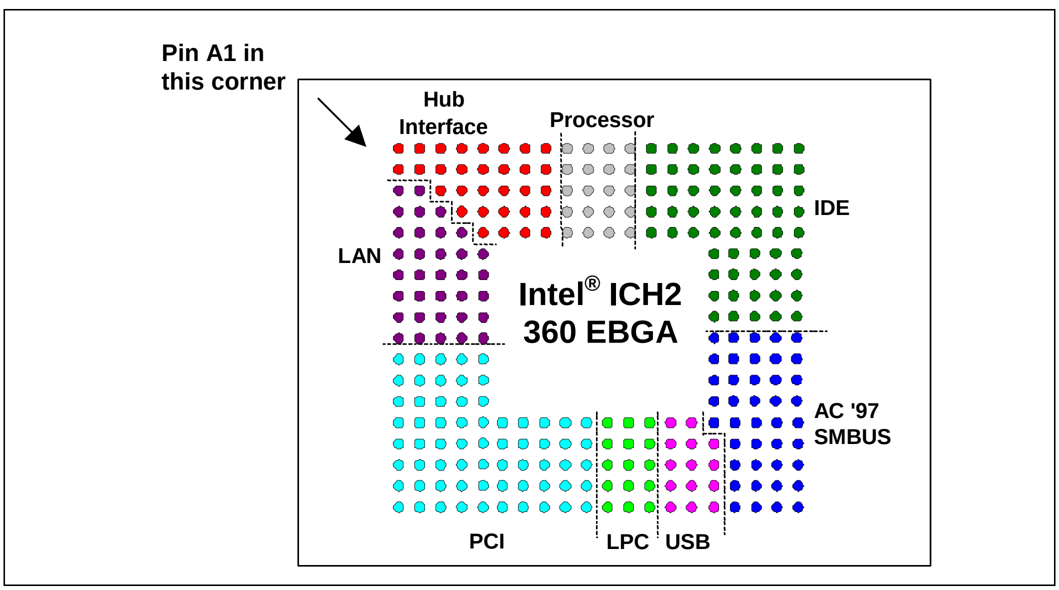
2.2 Intel® 845 Chipset Component Quadrant Layout

Figure 2-2. MCH Component Quadrant Layout (Top View)



2.3 Intel® ICH2 Component Quadrant Layout

Figure 2-3. Intel® ICH2 Quadrant Layout (Top View)

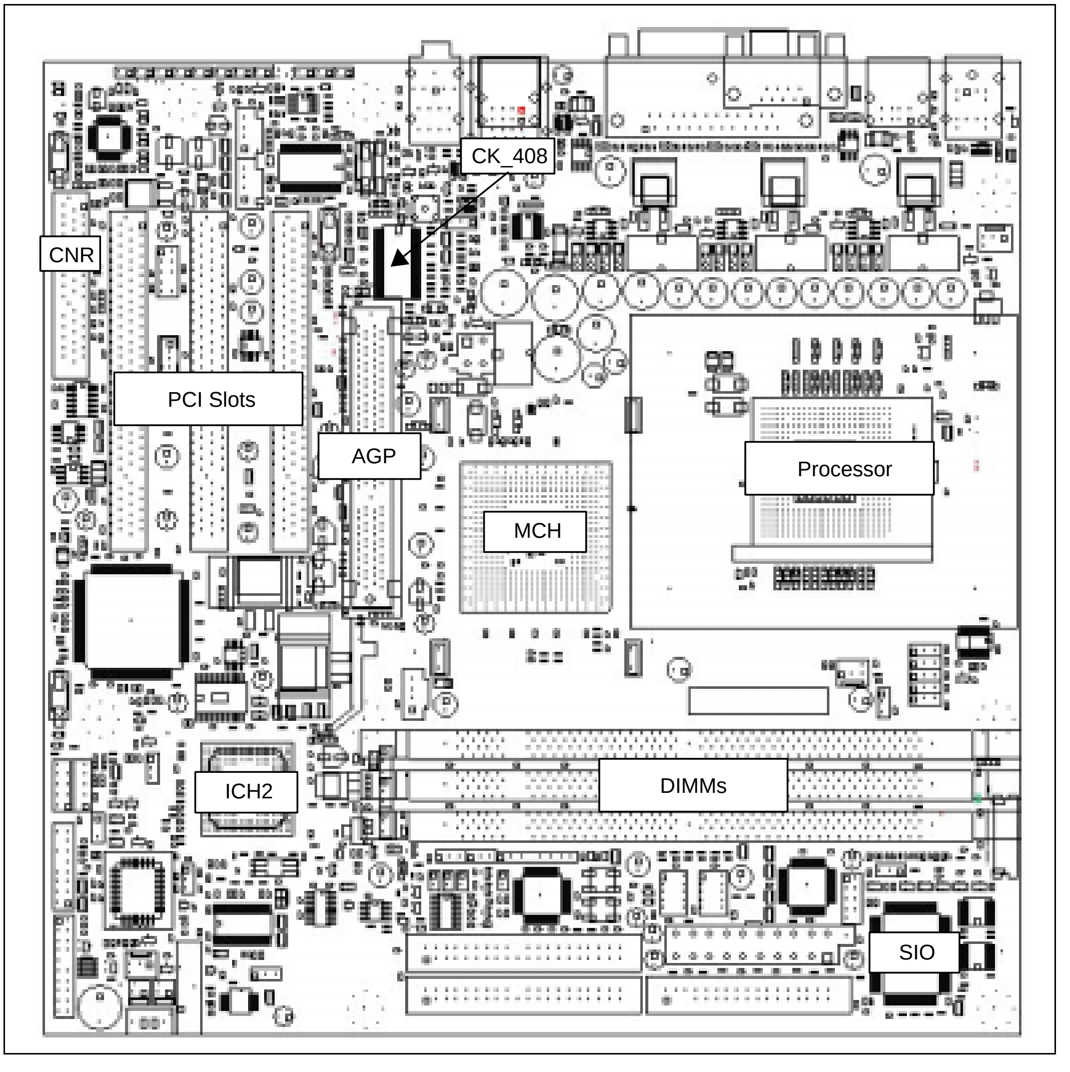


3 Platform Placement and Stack-Up Overview

In this chapter, an example of 845 chipset platform component placement and stack-up is described for a desktop system in µATX board form factor for PC133 SDRAM.

3.1 Platform Component Placement (PC133 SDRAM)

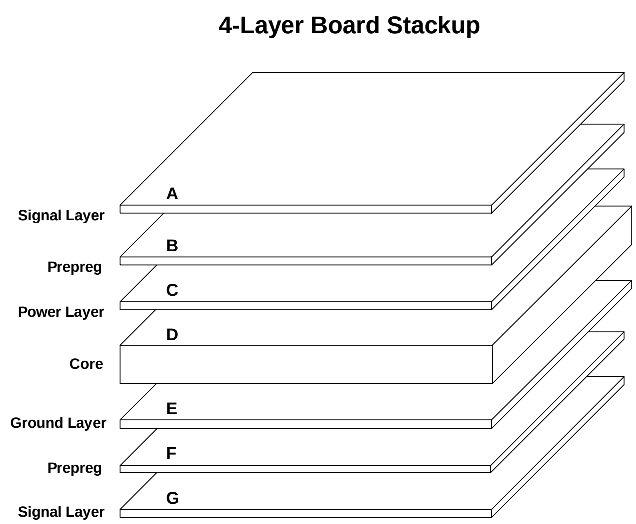
Figure 3-1. Component Placement Example Using Three PC133 SDRAM DIMMs



3.2 Nominal 4-Layer Board Stack-Up

The 845 chipset platform requires a board stack-up yielding a target board impedance ± 15% of 50 Ω for the System Bus and 60 Ω for the AGP interface, system memory, and hub interface. Recommendations in this design guide are based on the following a 4-layer board stack-up.

Figure 3-2. Four-Layer PCB Stack-Up



Description	Target Value
Target Board Impedance Z_0	50 Ω ± 15% with a 7-mil nominal trace width 60 Ω ± 15% with a 5-mil nominal trace width
Micro-stripline Er	4.2–4.5
Er @ 1 MHz	4.5
Er @ 1 GHz	4.35

Description	Typical Values
Trace Thickness	1.3–1.42 mils
Board Thickness	62 mils total 0.062 + 0.008 - 0.005
Material	Fiberglass made of FR4
Fab Construction	4 layer

Layer	Description	Nominal Thickness	Tolerance (± mils)
A	Signal Layer	0.7 mil (0.5 oz Cu) (See note 1)	(See note 2)
B	Prepreg	4.0 mil	0.3
C	Power Layer	1.4 mil (1.0 oz Cu)	0.2
D	Core	48 mil	5
E	Ground Layer	1.4 mil (1.0 oz Cu)	0.2
F	Prepreg	4.0 mil	0.3
G	Signal Layer	0.7 mil (0.5 oz Cu) (See note 1)	(See note 2)

NOTES:

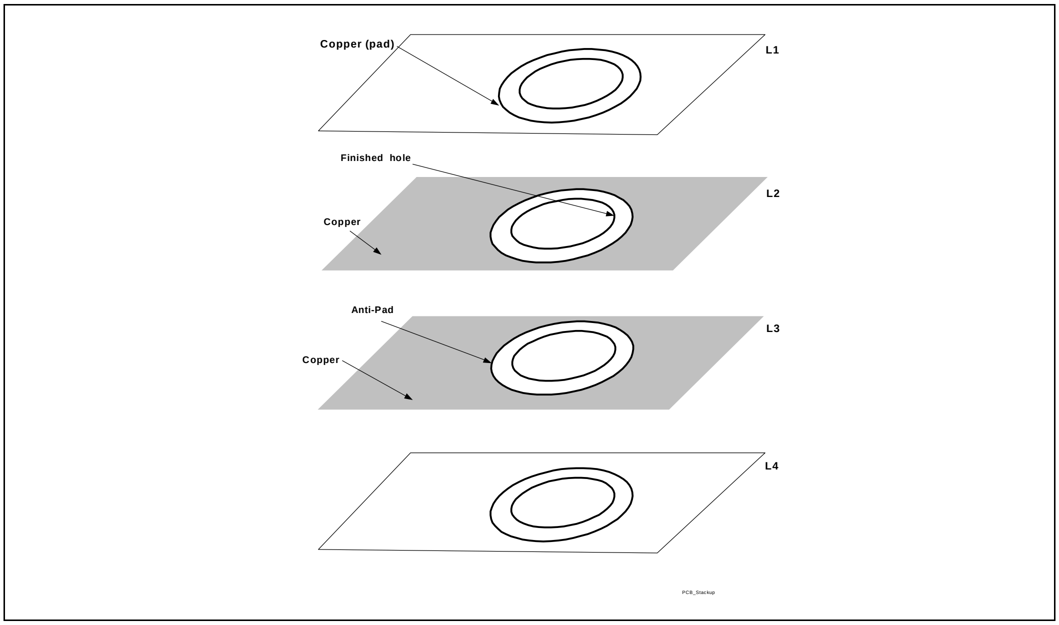
1. Thickness before Plating
2. Final Plating Thickness varies 1.3 mils—1.42 mils

3.3 PCB Technologies

3.3.1 Design Considerations

Intel has found that the following recommendation aids in the design of an 845 chipset-based platform. Simulations and reference platform are based on the following technology and is recommended that designers adhere to these guidelines.

Figure 3-3. PCB Technologies—Stack-Up



Number of Layers	
Stack-Up	4 Layer
Cu Thickness	0.5 oz Outer; (before Plating) 1 oz inner
Final Board Thickness	0.062 inch +0.008—0.005 inch
Signal and Power Via Stack /Processor / MCH / Intel® ICH2 / Memory Breakout	
Via Pad	0.026 inch
Via Anti-Pad	0.040 inch
Via Finished Hole	0.014 inch
Solder Mask Opening (top side only) [1]	0.020 inch
Signal Pad (BGA)	0.020 inch

NOTE: [1]For solder bridge avoidance these pads are to be partially covered by solder mask on the primary side. Solder mask residue must not be left in the holes.

4 Processor System Bus Guidelines

4.1 Processor System Bus Design Guidelines

Table 4-1 summarizes the layout recommendations for Pentium 4 processor configurations and expands on specific design issues and recommendations.

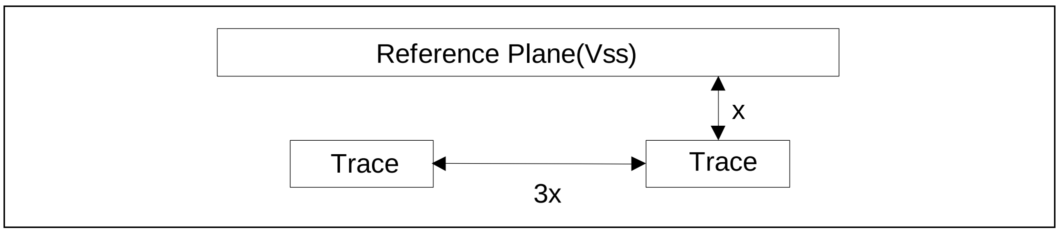
Table 4-1. System Bus Routing Summary for the Processor

Parameter	Processor Routing Guidelines
Line to line spacing	Data and common clock system bus must be routed at 7-mil wide traces and with 13 mils spacing.
Breakout Guidelines (Processor and MCH)	7-mil wide with 5-mil spacing for a maximum of 250 mils from the component ball.
Data Line lengths (agent to agent spacing)	2 inches—10 inches from pin-to-pin. Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to V_{SS}.
DSTBN/P[3:0]#	A layer transition may occur if the reference plane remains the same (V_{SS}) and the layers are of the same configuration (all stripline or all microstrip). A data strobe and its complement should be routed within ± 25 mils of the same pad-to-pad length. If one strobe switches layers, its complement must switch layers in the same manner. DSTBN/P# should be referenced to V_{SS}.
Address line lengths (agent to agent spacing) ADSTB[1:0]#	2 inches—10 inches from pin to pin. Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (V_{SS}), and the layers are of the same configuration (all stripline or all microstrip).
Common Clock line lengths	2.5 inches—10 inches pin to pin. No length compensation is necessary.
Topology	Point-to-point (chipset to processor).

Parameter	Processor Routing Guidelines
Routing priorities	All signals should be referenced to V_{SS}. Ideally, layer changes should not occur for any signals. If a layer change must occur, the reference plane must be V_{SS} and the layers must all be of the same configuration (all stripline or all microstrip for example). The data bus must be routed first, then the address bus, then common clock.
Clock keep-out zones	Refer to Table 11-3. BCLK [1:0]# Routing Guidelines.
Trace Impedance	50 Ω ± 15%

Note: Refer to the *Intel® 845 Chipset: Intel® 82845 Memory Controller Hub (MCH) Datasheet* for MCH package dimensions, and refer to *Intel Pentium 4 Processor in the 478 pin package Processor Signal Integrity Models* for processor package dimensions.

Figure 4-1. Cross-Sectional View of 3:1 Ratio



The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, and vias, VRMs, etc. It is useful to think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

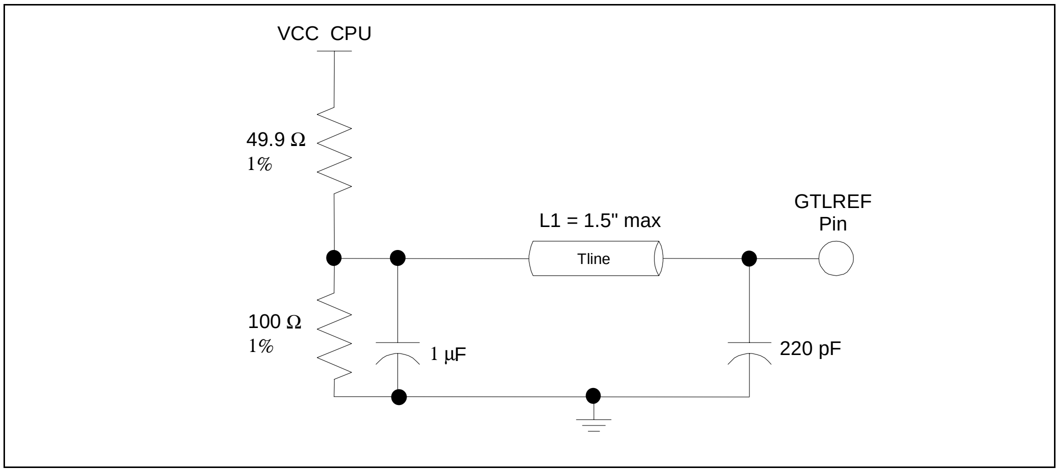
The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Maintain V_{SS} as a reference plane for all system bus signals.
- Do not route over via anti-pads or socket anti-pads.

4.1.1 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage must be supplied to only one of the four pins.

Figure 4-2. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1 µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin.
- Decouple the pin with a high-frequency capacitor (such as a 220 pF 603) as close to the pin as possible.
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use at least a 7-mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the front side bus signals).

4.1.2 HVREF, HSWNG, HRCOMP Layout and Routing Recommendations at the MCH

The HVREF signals must be tied to a resistor divider network that supplies 2/3*V_{CC_CPU}. Use one 49.9 Ω 1% resistor to the V_{CC_CPU} plane and one 100 Ω 1% resistor to ground for the divider. Decouple with one 0.1 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12 mils wide. Keep this trace at a minimum of 10 mils away from other signals.

The HSWNG signals must be tied to a resistor divider network that supplies 1/3* V_{CC_CPU}. Use one 300 Ω 1% resistor to the V_{CC_CPU} plane and one 150 Ω 1% resistor to ground for the divider. Decouple with one 0.01 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12 mils wide. Keep this trace at a minimum of 10 mils away from other signals.

Each HRCOMP signal must be tied to ground through a 24.9 Ω 1% resistor. The trace to each resistor should be routed a maximum of 0.5 inch at 10 mils wide. Keep each trace a minimum of 7 mils away from other signals.

4.2 Processor Configuration

4.2.1 Intel® Pentium® 4 Processor Configuration

This section provides more details for routing Pentium 4 processor based systems. Both recommendations and considerations are presented.

For proper operation of the processor and the 845 chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation based on assumptions that may not apply to an OEM's system design. The most accurate way to understand the signal integrity and timing of the system bus in a platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stack-up and other parameters can be made that improve system performance.

Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet* for a system bus signal list, signal types, and definitions.

4.2.2 Topology and Routing

Table 4-2. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Design recommendations are presented first, followed by design considerations.

4.2.2.1 Design Recommendations

The following are the design recommendations for the data, address, strobes, and common clock signals. Based on the example of Figure 3-2 the data, address, strobe and common clock should be routed 7 mils with 13-mil spacing. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

Data

The pad-to-pad distance for the data signals from the processor to the chipset should be between 2.0 inches and 10 inches (i.e., 2.0 inches < L1 < 10 inches). Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Data signals may change layers if the reference plane remains V_{SS}.

The following equation is used to calculate package delta addition to motherboard length for UP systems.

$$\text{delta}_{\text{net,strobe}} = (\text{cpu\_pkglen}_{\text{net}} - \text{cpu\_pkglen}_{\text{strobe*}}) + (\text{cs\_pkglen}_{\text{net}} - \text{cs\_pkglen}_{\text{strobe}})$$

NOTES:
1. Refer to Section 4.6.7 for package lengths.
2. * Strobe package length is the average of the strobe pair.

Address

Address signals follow the same rules as data signals except they should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. Address signals may change layers if the reference plane remains V_{SS}.

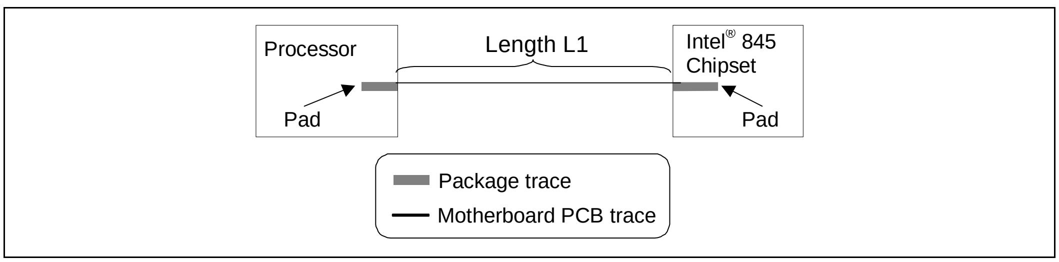
Data Strobes

A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed to ± 25 mils of the same length. It is recommended to simulate skew to determine the length that best centers the strobe for a given system.

Common Clock

Common clock signals should be routed to a minimum pin-to-pin motherboard length of 2.5 inches and a maximum motherboard length of 10 inches.

Figure 4-3. Processor Topology



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4.3 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe, and address. Table 4-3 lists the signals covered in this section.

Table 4-3. Miscellaneous Signals (Signals That Are Not Data, Address, or Strobe)

Signal Name	Type	Direction	Topology	Driven By
A20M#	Asynchronous GTL+	I	2A	ICH2
BR0#	AGTL+	I/O	4	Processor
COMP[1:0]	Analog	I	5	
FERR#	Asynchronous GTL+ Open Drain	O	1A	Processor
IGNNE#	Asynchronous GTL+	I	2A	ICH2
INIT#	Asynchronous GTL+	I	2B	ICH2
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2A	ICH2
PROCHOT#	Asynchronous GTL+ Open Drain	O	1B	Processor
PWRGOOD	Asynchronous GTL+ Open Drain	I	2C	ICH2
RESET#	AGTL+ Open Drain	I	4	MCH
SLP#	Asynchronous GTL+	I	2A	ICH2
SMI#	Asynchronous GTL+	I	2A	ICH2
STPCLK#	Asynchronous GTL+	I	2A	ICH2
THERMTRIP#	Asynchronous GTL+ Open Drain	O	1C	Processor
V_{CCA}	Power	I	3	External logic
$V_{CCIOPLL}$	Power	I	3	External logic
V_{CC_SENSE}	Other	O		Processor
VID[4:0]	Open Drain 3.3 V Tolerant	O	8	Processor
V_{SSA}	Power	I	3	Ground
V_{SS_SENSE}	Other	O		Processor
THERMDA/THERMDC	Other	I/O	6	External logic
TESTHI	Other	I/O	7	External logic

NOTE: Refer to Section 14, Schematic Checklist, for Debug Port signals.

All signals must meet the AC and DC specifications as documented in the *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet*.

4.3.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

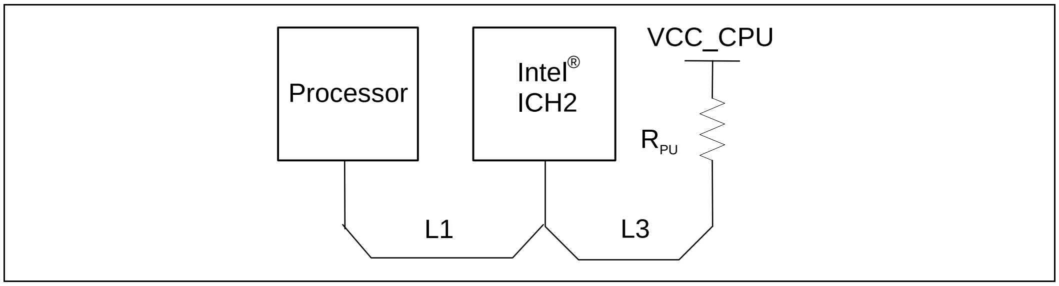
4.3.1.1 Topology 1A: Asynchronous GTL+ Signal Driven by the Processor—FERR#

FERR# should adhere to the routing and layout recommendations described and illustrated in Table 4-4 and Figure 4-4.

Table 4-4. Layout Recommendations for FERR# Signal—Topology 1A

Trace Zo	Trace Spacing	L1	L3	Rpu
60 Ω	7 mil	1 inch—12 inches	3 inches max	62 Ω ± 5%

Figure 4-4. Routing Illustration for FERR#



4.3.1.2 Topology 1B: Asynchronous GTL+ Signal Driven by the Processor—PROCHOT#

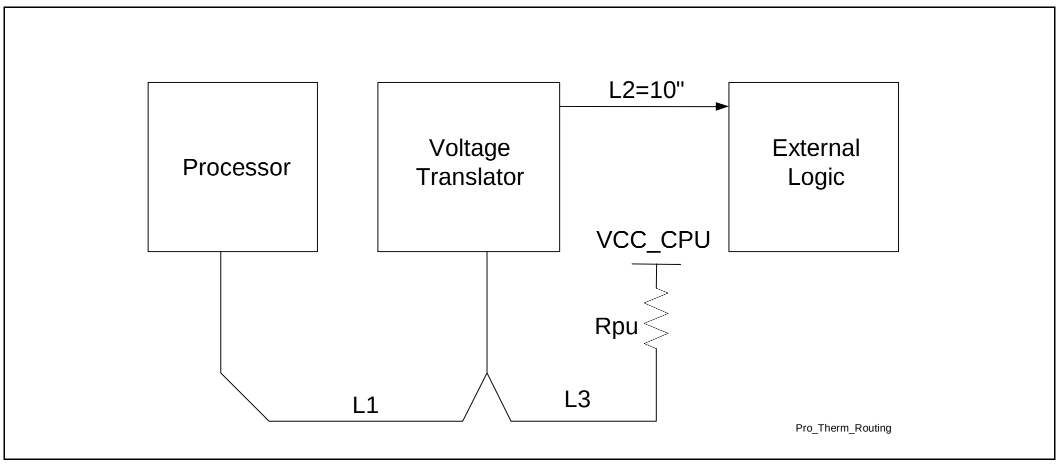
PROCHOT# should adhere to the routing and layout recommendations described and illustrated in Table 4-5 and Figure 4-5.

If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 4-5. Layout Recommendations for PROCHOT# Signal—Topology 1B

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
60 Ω	7 mil	1 inch—17 inches	10 inches max	3 inches max	62 Ω ± 5%

Figure 4-5. Routing Illustration for PROCHOT#



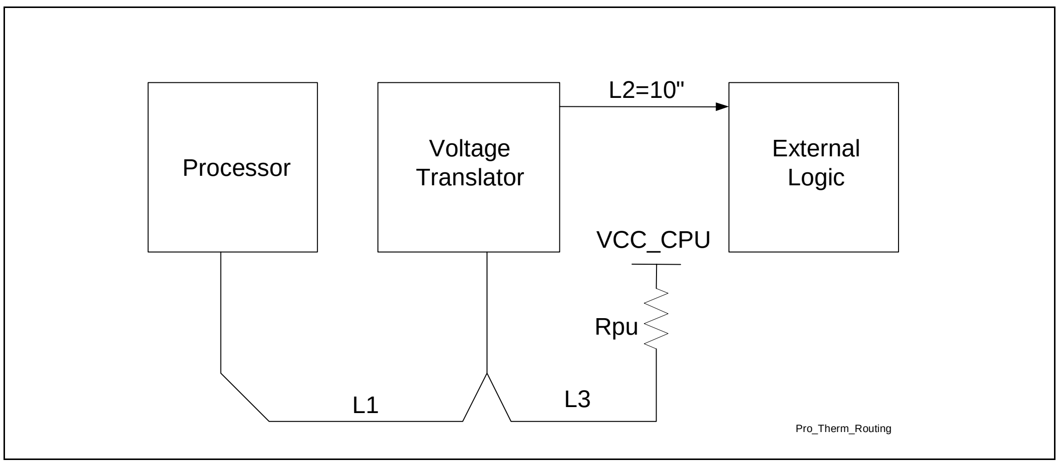
4.3.1.3 Topology 1C: Asynchronous GTL+ Signal Driven by the Processor—THERMTRIP#

THERMTRIP# should adhere to the routing and layout recommendations described and illustrated in Table 4-6 and Figure 4-6. If THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 4-6. Layout Recommendations for THERMTRIP# Signal—Topology 1C

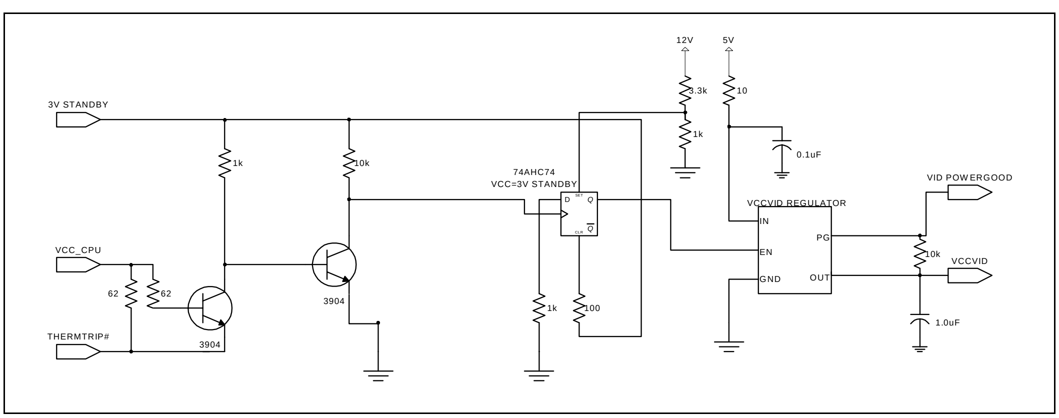
Trace Zo	Trace Spacing	L1	L2	L3	Rpu
60 Ω	7 mil	1 inch—17 inches	10 inches max	3 inches max	62 Ω ± 5%

Figure 4-6. Routing Illustration for THERMTRIP#



It is required that power is removed from the processor core within 0.5 seconds of the assertion of the THERMTRIP# signal. Figure 4-7 is an example circuit that powers down the processor voltage regulator when THERMTRIP# is asserted.

Figure 4-7. THERMTRIP# Power Down Circuit



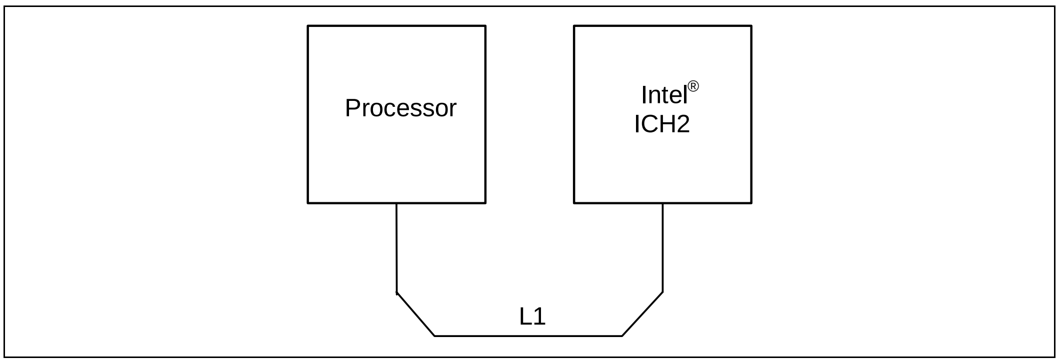
4.3.1.4 Topology 2A: Asynchronous GTL+ Signals Driven by the Intel® ICH2—A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

These signals should adhere to the routing and layout recommendations described and illustrated in Table 4-7 and Figure 4-8.

Table 4-7. Layout Recommendations for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#—Topology 2A

Trace Zo	Trace Spacing	L1	Rpu
60 Ω	7 mils	12 inches max	None

Figure 4-8. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#



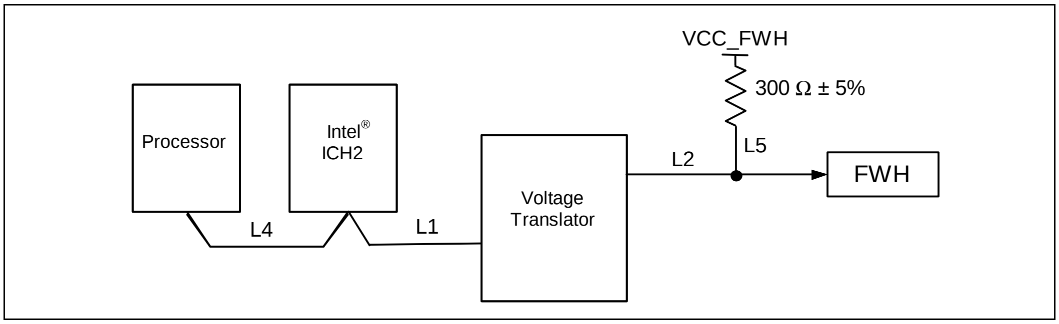
4.3.1.5 Topology 2B: Asynchronous GTL+ Signal Driven by the Intel® ICH2—INIT#

INIT# should adhere to the routing and layout recommendations described and illustrated in Table 4-8 and Figure 4-9.

Table 4-8. Layout Recommendations for INIT#—Topology 2B

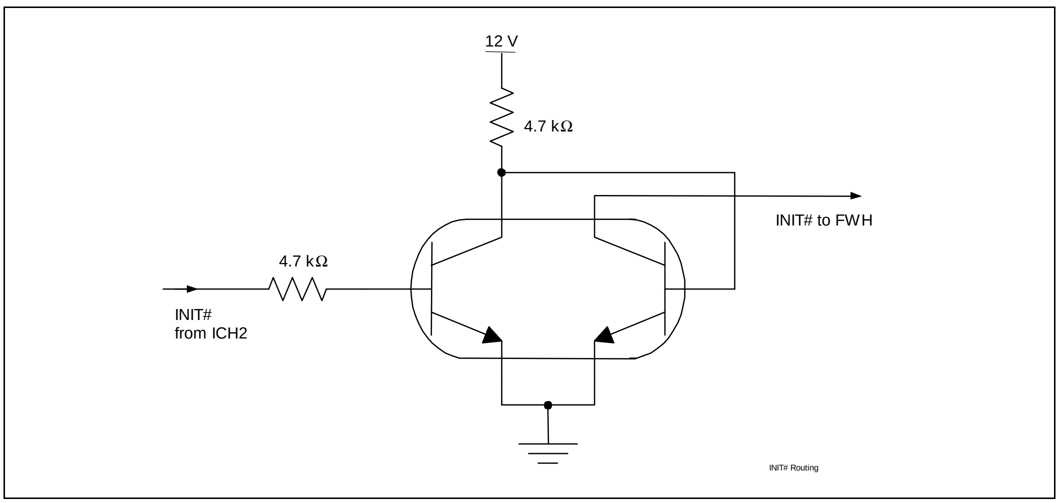
Trace Zo	Trace Spacing	L1	L2	L4	L5	Rpu
60 Ω	7 mils	2 inches max	10 inches max	17 inches max	3 inches max	300 Ω 5%

Figure 4-9. Routing Illustration for INIT#



Level shifting is required for the INIT# signal to the FWH to meet the input logic levels of the FWH. Figure 4-10 illustrates one method of level shifting.

Figure 4-10. Voltage Translation of INIT#



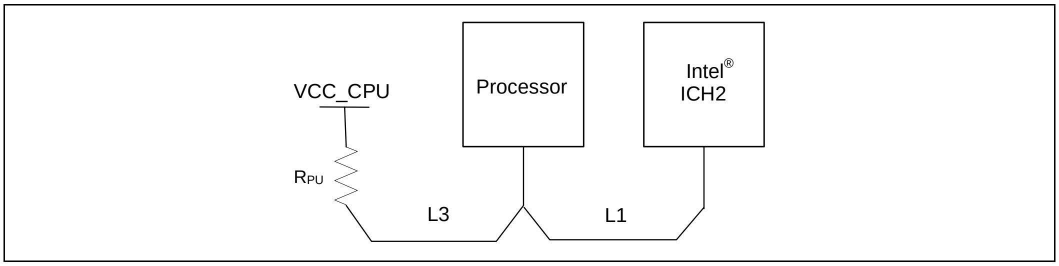
4.3.1.6 Topology 2C: Asynchronous GTL+ Signal Driven by the Intel® ICH2 Open Drain—PWRGOOD

PWRGOOD should adhere to the routing and layout recommendations described and illustrated in Table 4-9 and Figure 4-11.

Table 4-9. Layout Recommendations for Miscellaneous Signals—Topology 2C

Trace Zo	Trace Spacing	L1	L3	Rpu
60 Ω	7 mil	1 inch–12 inches	3 inches max	300 Ω ± 5%

Figure 4-11. Routing Illustration for PWRGOOD



4.3.1.7 Topology 3—$V_{CCIOPLL}$, V_{CCA} and V_{SSA}

$V_{CCIOPLL}$ and V_{CCA} are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. Further details can be found in Section 4.6.6.1.

4.3.1.8 Topology 4—BR0# and RESET#

Because the processor does not have on-die termination on the BR0# and RESET# signals, it is necessary to terminate the signals using discrete components on the system board. Connect the signals between the components as shown in Figure 4-12. The 845 chipset has on-die termination; therefore it is necessary to terminate only at the processor end. The value of Rt should be 51 Ω ± 5% for RESET#. The value of Rt should be 150–220 Ω ± 5% for BR0#.

Figure 4-12. Routing Illustration for BR0# and RESET#

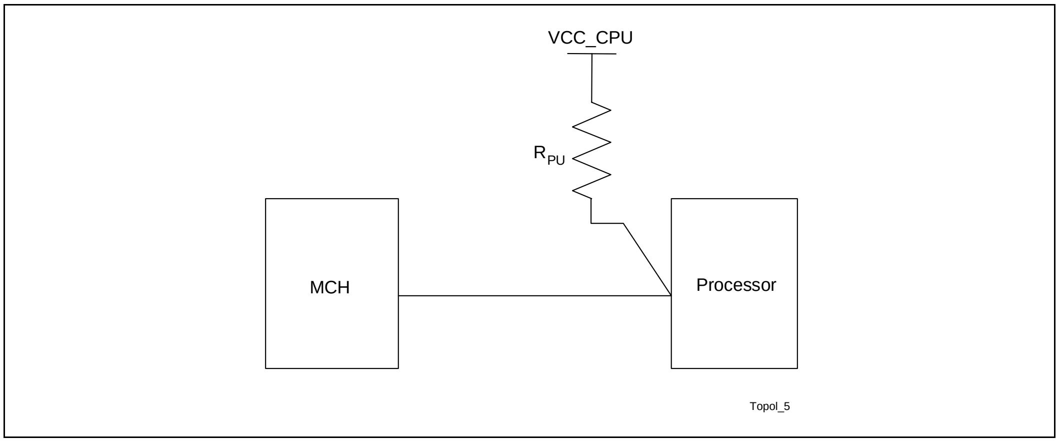


Table 4-10 BR0# and RESET# Lengths

Signal	Rt	L1	L2
RESET#	51 Ω	≤ 1–2 inches	2 inches – 10 inches pin-to-pin
BR0#	150 Ω – 220 Ω	≤ 1–2 inches	2 inches – 10 inches pin-to-pin

4.3.1.9 Topology 5: COMP[1:0] Signals

Terminate the COMP[1:0] pins to ground through a 51 Ω ± 1% resistor as close as possible to the pin. Do not wire COMP pins together; connect each pin to its own termination resistor. RCOMP value can be adjusted to set external drive strength of I/O and to control the edge rate.

4.3.1.10 Topology 6: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. The following are some guidelines:

- The remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources such as clock generators, data buses, and address buses, etc., are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

4.3.1.11 Topology 7: TESTHI and RESERVED Pins

The TESTHI pins should be tied to the processor V_{CC} using a matched resistor, where the matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, If the trace impedance is 50 Ω, a value between 40 Ω and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or may be grouped together as detailed below. A matched resistor should be used for each group:

1. TESTHI[1:0]
2. TESTHI[5:2]
3. TESTHI[10:8]
4. TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used, they can be connected individually to V_{CC} using matched resistors, or can be grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 kΩ resistors is acceptable. Tying ITPCLKOUT[1:0] directly to V_{CC} or sharing a pull-up resistor to V_{CC} will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

As an alternative, group 2 (TESTHI [5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor V_{CC}. This has no impact on system functionality. TESTHI[0] and TESTHI[12] may also be tied directly to processor V_{CC} if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0], direct tie to V_{CC} is strongly discouraged for system boards that do not implement an onboard debug port.

4.3.1.12 Topology 8: Processor Voltage Regulator Sequencing Requirements

- The output of the voltage regulator used to generate V_{CC}VID should be no more than 1.5 inches from processor pin AF4
- The trace connecting the voltage regulator output to pin AF4 should be as wide as practical, but not less than 0.025 inch wide.
- The trace connecting the voltage regulator output to pin AF4 should have both a 0.1 µF, and a 1.0 µF capacitor for decoupling. The 0.1 µF capacitor should be located as close as possible to processor pin AF4. The 1.0 µF capacitor should be located as close as possible to the output of the voltage regulator.

If an integrated voltage regulator such as the MIC5248 is used, the voltage input (pin 1) should be connected to the system board V_{CC} or 3.3 V rail through a zero ohm resistor. The input of the voltage regulator should also be decoupled with a 0.1 µF capacitor at the pin. The trace connecting the voltage regular input to the zero resistor should be equal to or greater than the voltage regulator output trace connected to the processor (i.e., if the connection to the processor is 0.025 inch, the trace width to the input of the voltage regulator should be 0.025 inch or greater). The voltage regulator power good signal (pin 4) should be connected to the voltage regulator output (pin 5) through a 10 kΩ resistor.

During power-on, the rising edge of the V_{CC}VID power supply must be monotonic. Examples of acceptable monotonic and unacceptable non-monotonic rising edges are shown in Figure 4-13 and Figure 4-14 for reference.

Figure 4-13. Passing Monotonic Rising Edge Voltage Waveform

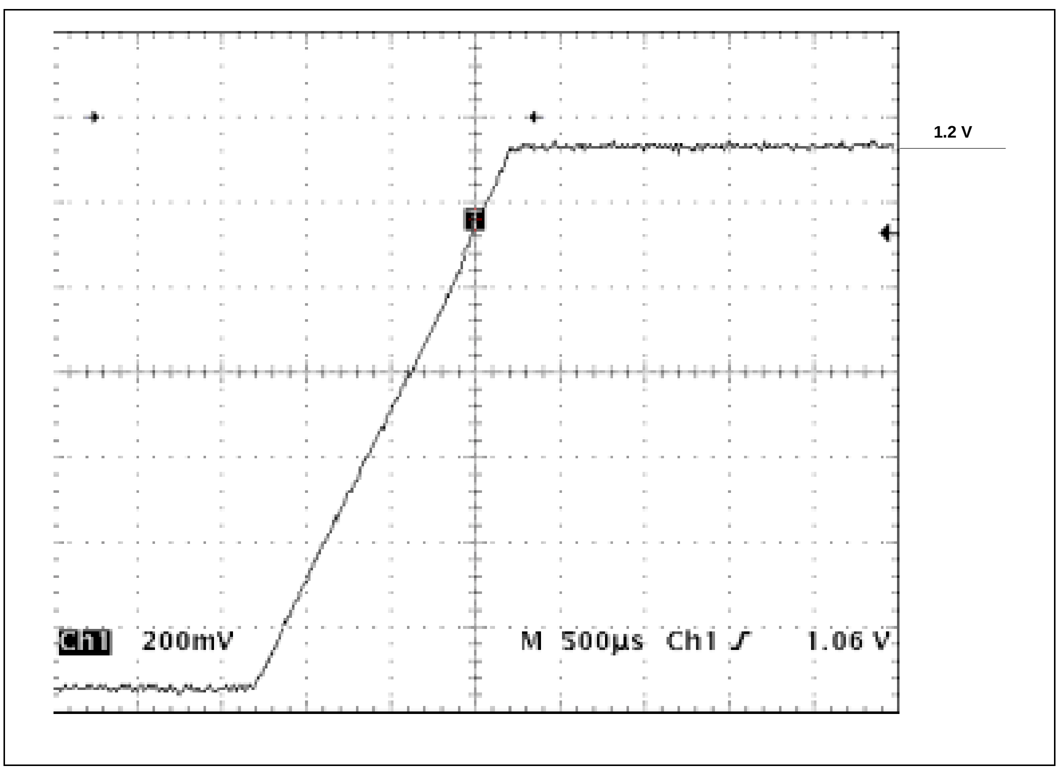
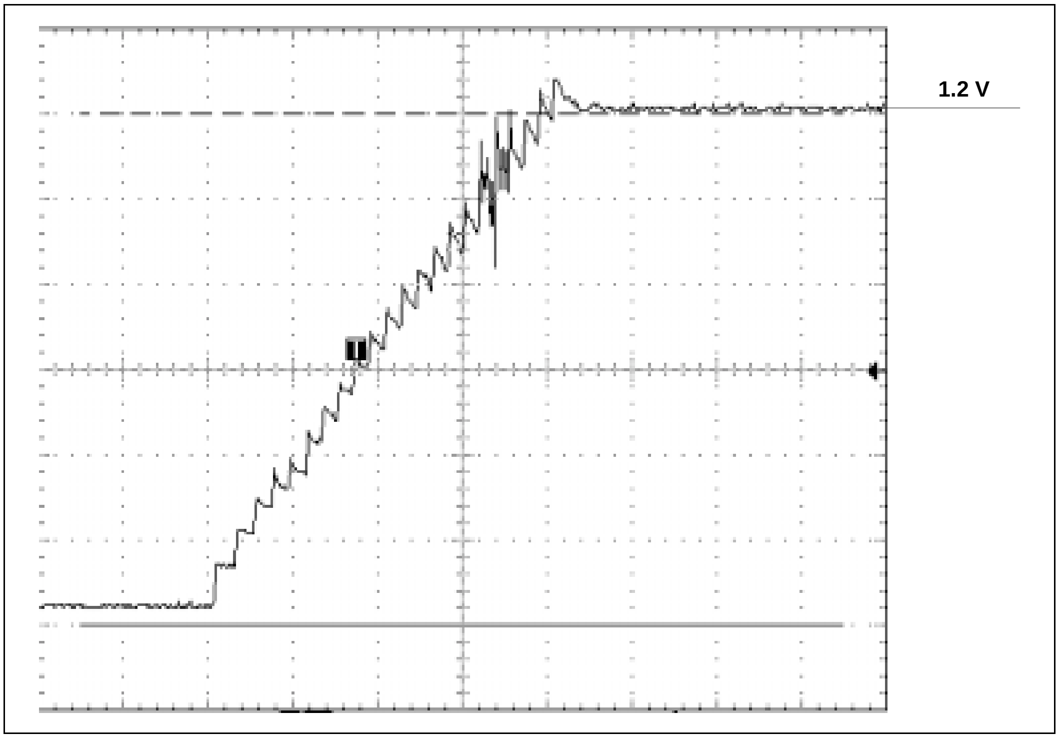
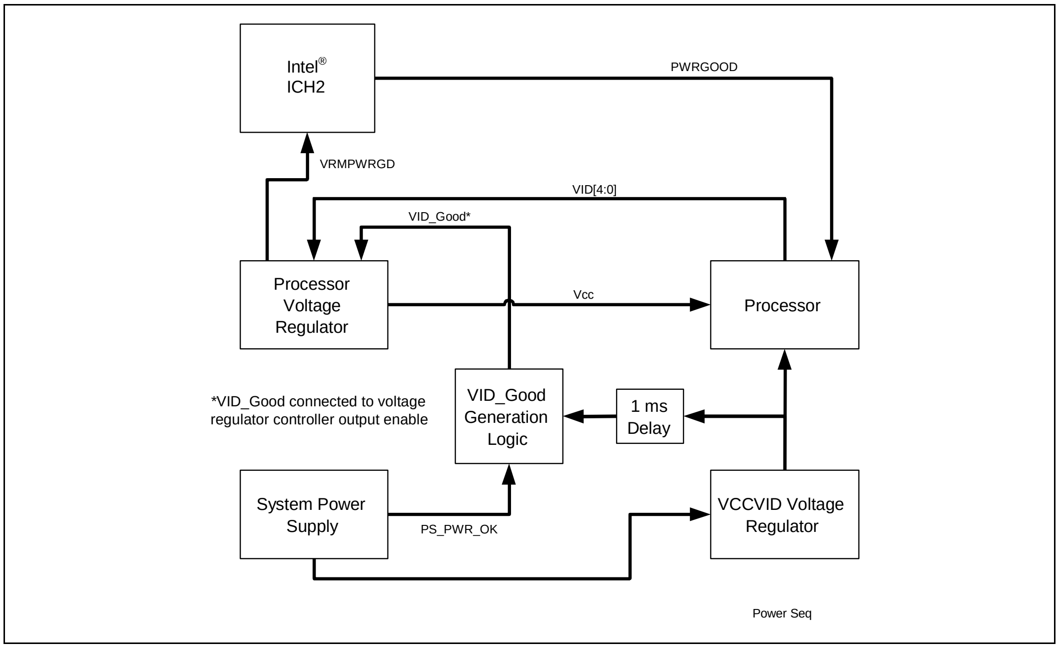


Figure 4-14. Failing Non-Monotonic Rising Voltage Waveform



The platform requires a 1.2 V supply to the V_{CC}VID pins to support the on-die VID generation circuitry. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry has some power sequencing requirements. Figure 4-15 shows a block diagram of a power sequencing implementation.

Figure 4-15. Power Sequencing Block Diagram



4.4 Additional Processor Design Considerations

This section documents system design considerations not addressed in previous sections.

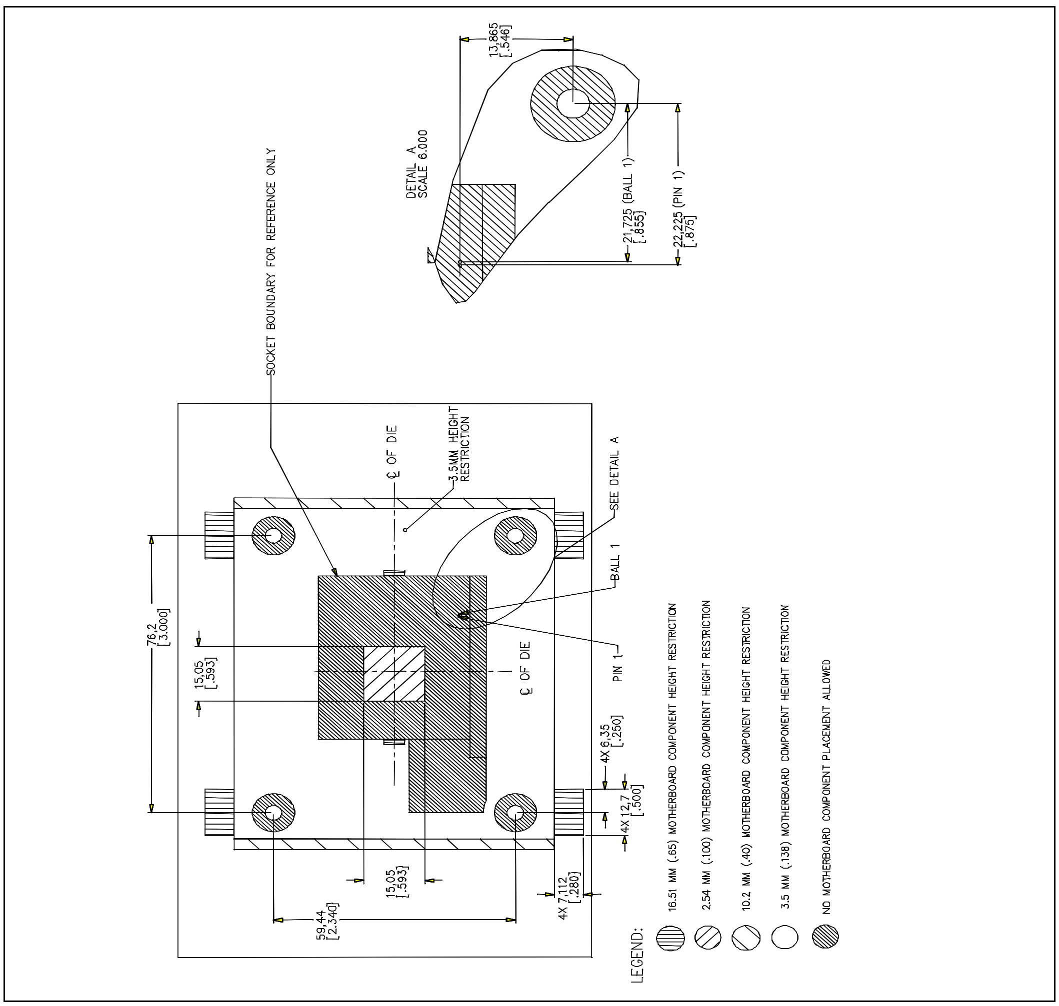
4.4.1 Retention Mechanism Placement and Keep-Outs

The RM requires a keep-out zone for a limited component height area under the RM as shown in Figure 4-16 and Figure 4-17. The figures show the relationship between the RM mounting holes, and pin one of the socket. In addition it also documents the keep-outs.

The retention holes should be a non-plated hole. The retention holes should have a primary and secondary side route keep-out area of 0.409 inches diameter.

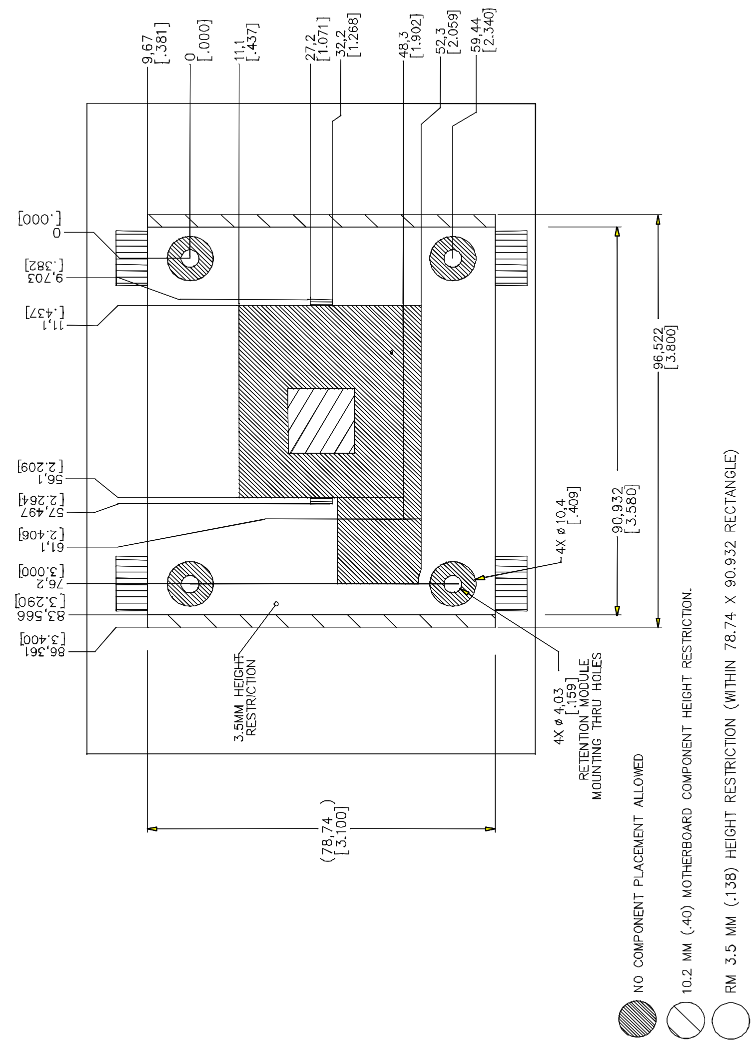
For heatsink volumetric information refer to the *Intel® Pentium® 4 Processor in the 478-pin package Thermal Design Guidelines*.

Figure 4-16. RM Keep-Out Drawing 1



NOTE: Dimensions are in millimeters with inch dimensions in brackets.

Figure 4-17. RM Keep-Out Drawing 2



NOTE: Dimensions are in millimeters with inch dimensions in brackets.

4.4.2 Power Header for Active Cooling Solutions

The Intel reference-design heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden/Molex 22-01-3037, AMP 643815-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described Table 4-11

Table 4-11. Reference Solution Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel boxed processor heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden/Molex 22-23-2037, AMP 640456-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 4-12

Table 4-12. Boxed Processor Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	Sense

The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate V_{OH} level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to GND.

For more information on boxed processor requirements, refer to the *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet.*

4.5 Debug Port Routing Guidelines

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port.

4.5.1 Debug Tools Specifications

4.5.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Pentium 4 processor systems. Tektronix and Agilent should be contacted for specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Pentium 4 processor systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor system that can make use of an LAI: mechanical and electrical.

4.5.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium 4 processor. The LAI pins plug into the socket, while the Pentium 4 processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Pentium 4 processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system. Note that it is possible that the keep-out volume reserved for the LAI may include space normally occupied by the Pentium 4 processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

4.5.1.3 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models for each of the logic analyzers to be able to run system level simulations to prove that they will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

4.6 Intel® Pentium® 4 Processor Power Distribution Guidelines

4.6.1 Power Requirements

Intel recommends using a Pentium 4 processor in the 478-pin package VR Down Design Guidelines-compliant regulator for the processor system board designs. A Pentium 4 processor and VR Down Design Guidelines -compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure that voltage fluctuations remain within *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet* specifications. See Table 4-13 for recommendations on the amount of decoupling required.

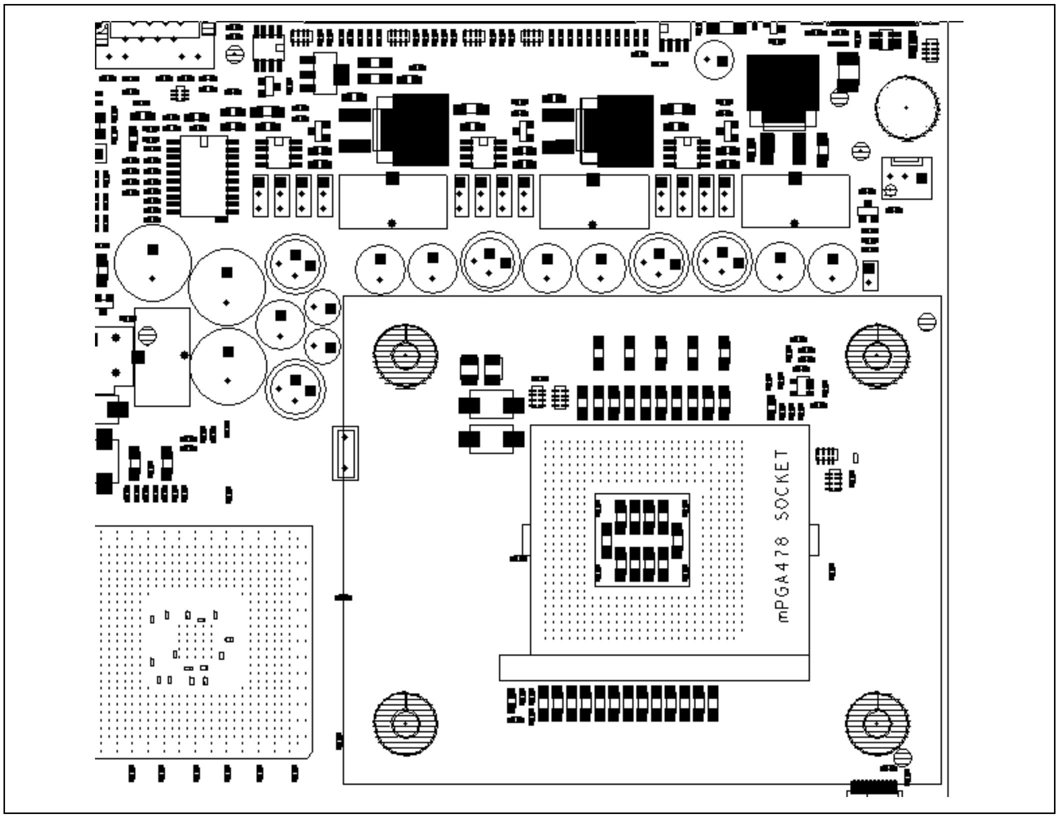
Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the socket loadlines in the *Intel® Pentium® 4 Processor in the 478 Pin Package VR Down Design Guidelines*.

The voltage tolerance of the loadlines contained in these documents helps the system designer achieve a flexible motherboard design solution for all processor frequencies. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation because of its higher current requirements, and to maintain power supply tolerance. For example, an onboard DC-to-DC converter converts a higher DC voltage to a lower level using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More important, however, an onboard regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 4-18 shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 3-1 North refers to the side of the processor closest to the back panel, and South refers to the side of the processor closest to the system memory.

Figure 4-18. VR Component Placement



4.6.2 45-Watt Processor Thermal Design Power (TDP) Limit

The Pentium 4 processors with 512-KB cache on the 0.13 micron process limited to a TDP of 45 Watts allow for a cost-optimized, high-performance VR down solution. A regulator switching at 400 KHz/phase allows the regulator designer to apply two phases when the processor is inserted into the socket, and to provide a minimum amount of output bulk capacitance. However, considerations must be made when using a 2-phase regulator at this high-switching frequency and with roughly 20 A of current going through each phase. Intel recommends placing plenty of copper on the board to dissipate FET and other conversion component losses, and to pay special attention to VR transient performance and tuning to maintain regulator stability and meet processor minimum and maximum voltages. A minimum 10 square inches of board space should be used on layer 1 as well as layer 4 for the entire regulator design. For exact details and layout guidelines, contact your voltage regulator manufacturer. Refer to the schematics for an implementation of the design.

4.6.3 Decoupling Requirements

For the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in Table 4-13.

Table 4-13. Decoupling Requirements

Capacitance	ESR (Each)	ESL (Each)	Ripple Current Rating (Each)
9 OSCONs, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A_{rms}
3 Al, Electolytic, 3300 µF	12 mΩ, max	5 nH, max	
38 1206 package, 10 µF	3.5 mΩ, typ	1.15 nH, typ	

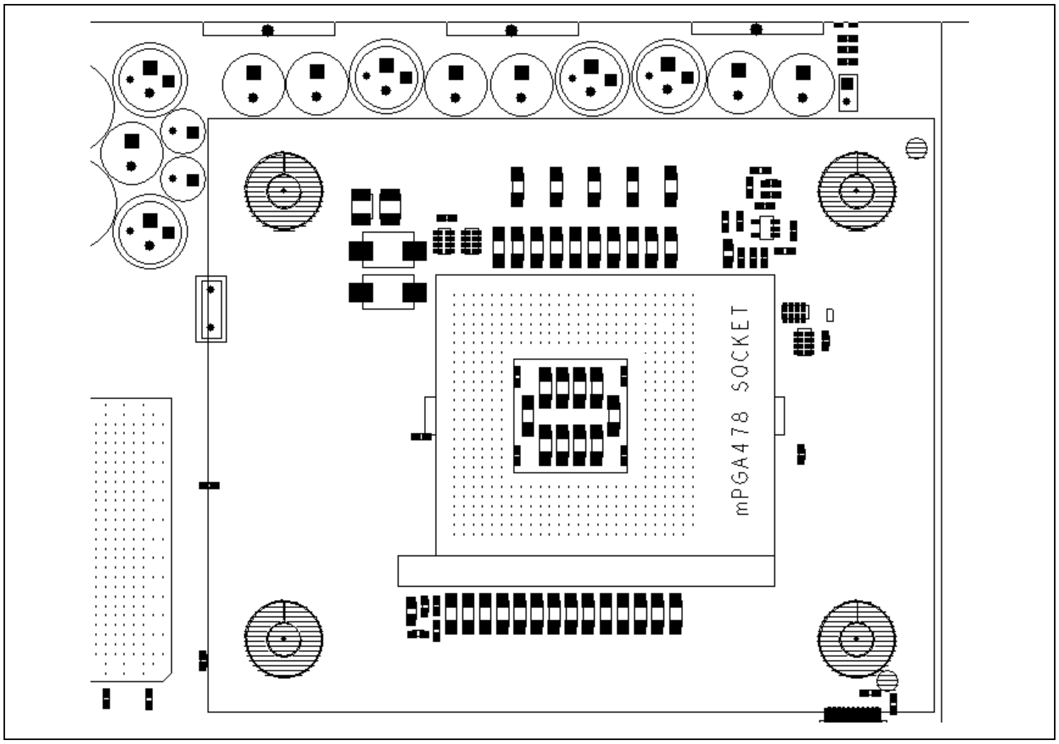
NOTES:
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel, and are not vendor specifications.

The decoupling should be placed as close as possible to the processor power pins. Table 4-14 and Figure 4-19 describe and illustrate the recommended placement.

Table 4-14. Decoupling Locations

Type	Number	Location
560 µF OS-CONs	9	North side of the processor as close as possible to the keep-out area for the retention mechanism
3 Al, Electolytic, 3300 µF	3	North side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 µF	14	North side of the processor as close as possible to the processor socket
1206 package, 10 µF	10	Inside the processor socket cavity
1206 package, 10 µF	14	South side of the processor as close as possible to the processor socket

Figure 4-19. Decoupling Placement



4.6.4 Layout

All four layers in the processor area should be used for power delivery. Two layers should be used for V_{CC_CPU}, and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high-current and low resistance required to meet the processor voltage specifications. To satisfy these requirements, shapes that encompass the power delivery part of the processor pin field are required. Figure 4-20 through Figure 4-23 show examples of how to use shapes to deliver power to the processor.

Figure 4-20. Top Layer Power Delivery Shape (V_{CC_CPU})

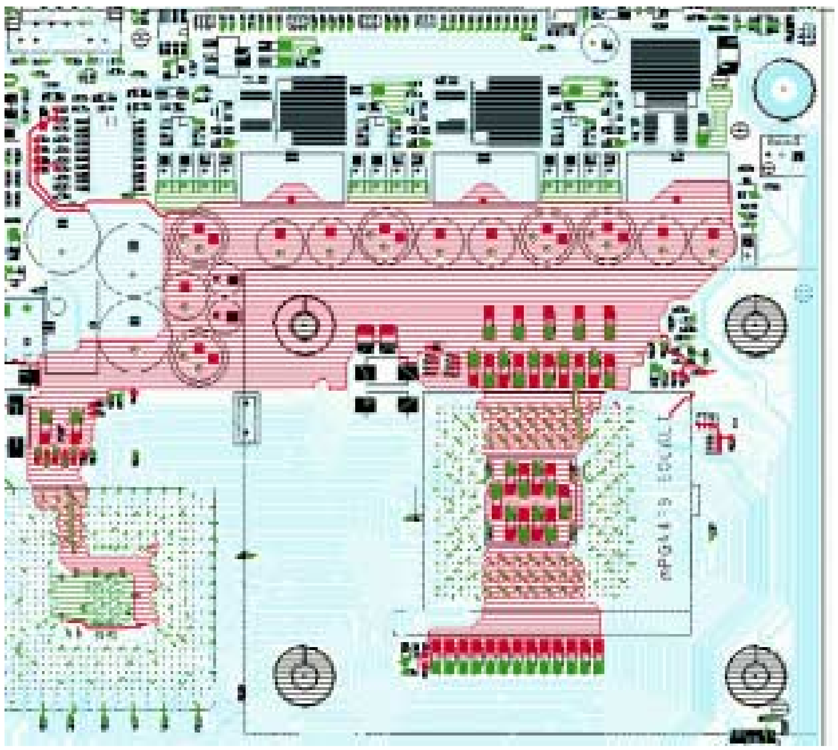


Figure 4-21. Layer 2 Power Delivery Shape (V_{SS})

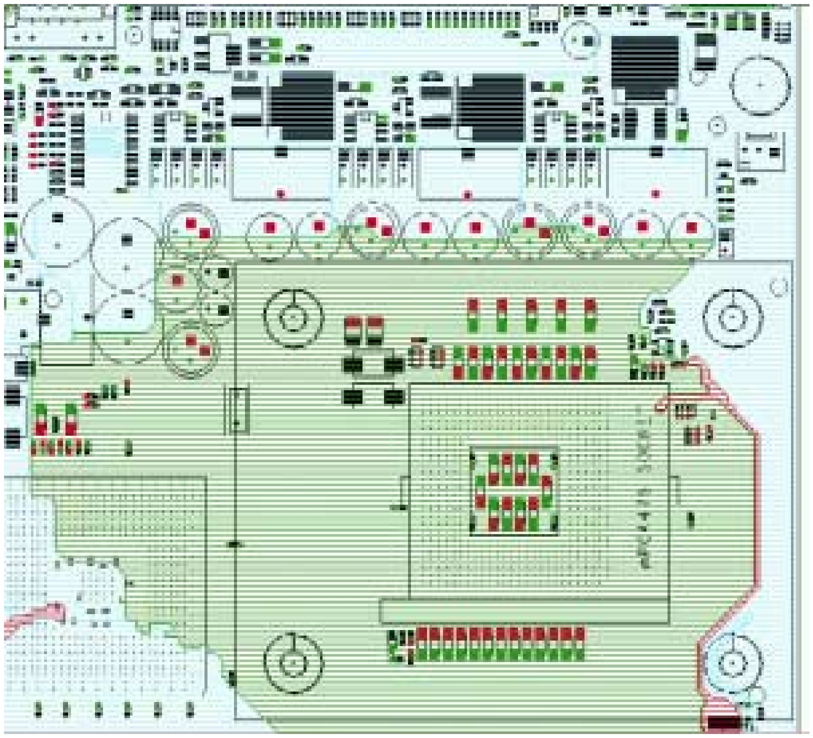


Figure 4-22. Layer 3 Power Delivery Shape (V_{SS})

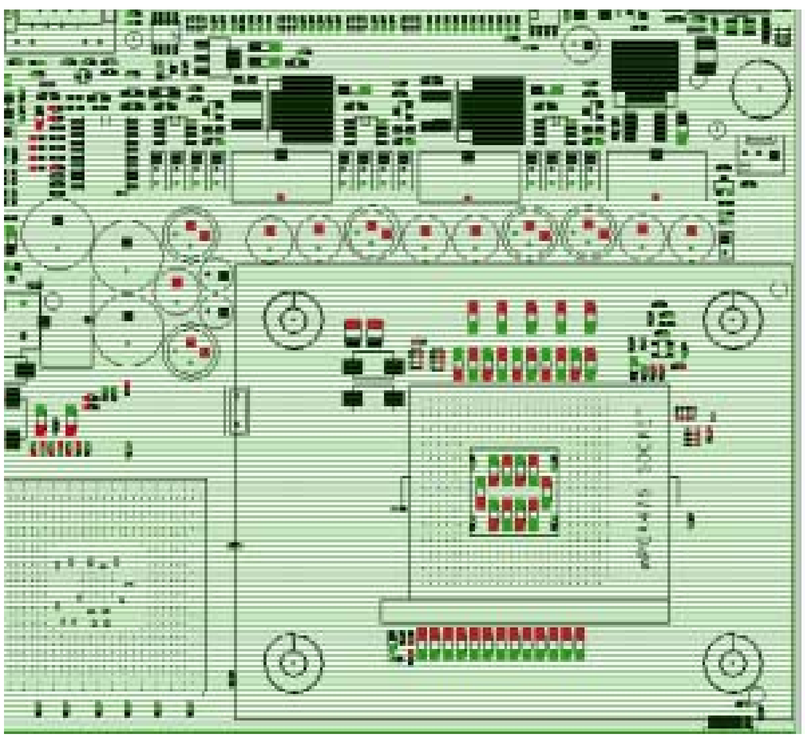
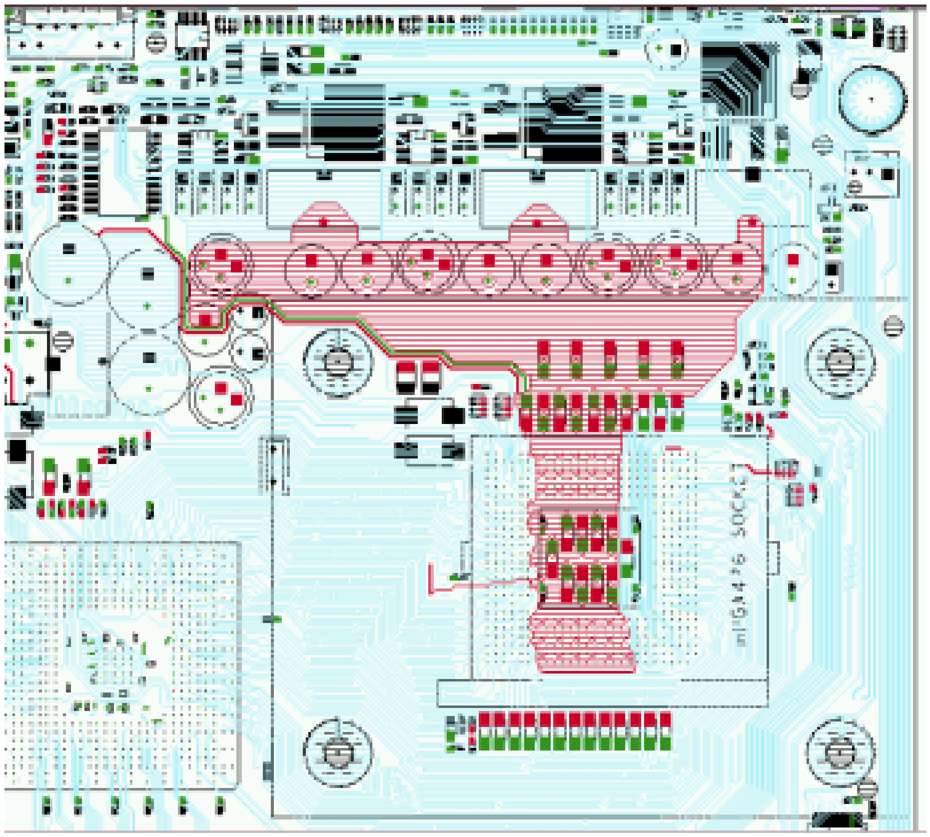
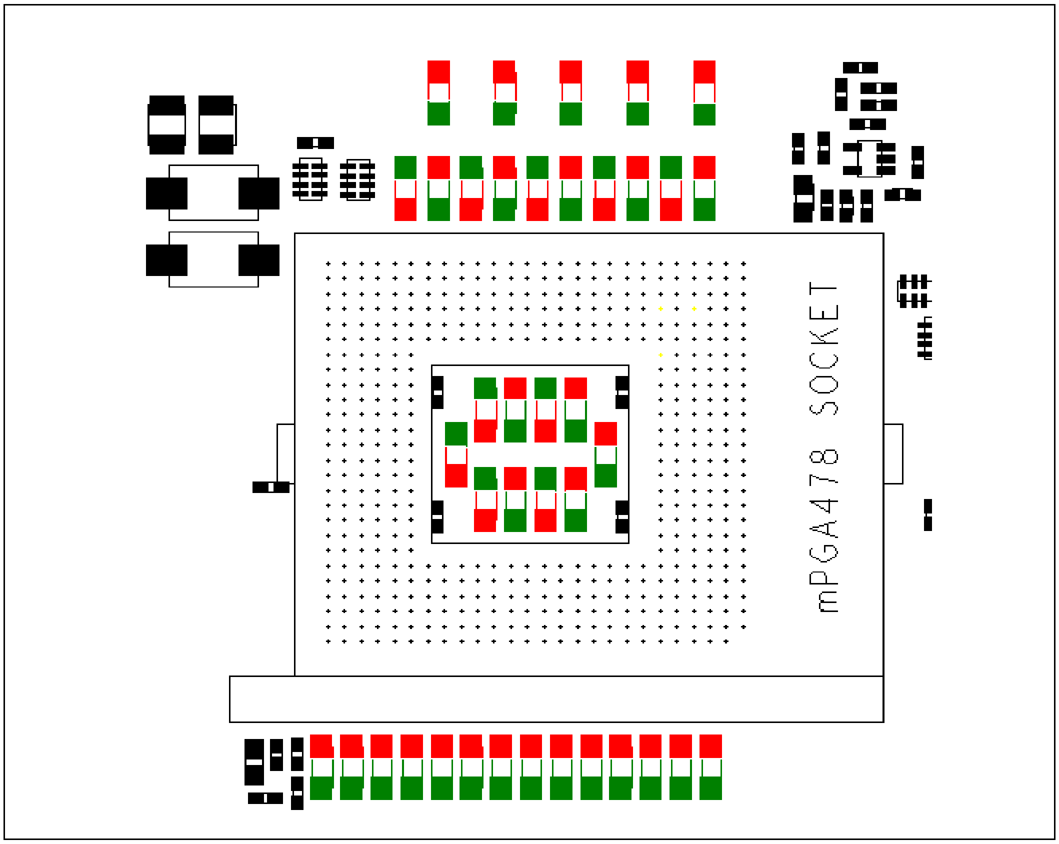


Figure 4-23. Bottom Layer Power Delivery Shape (V_{CC_CPU})



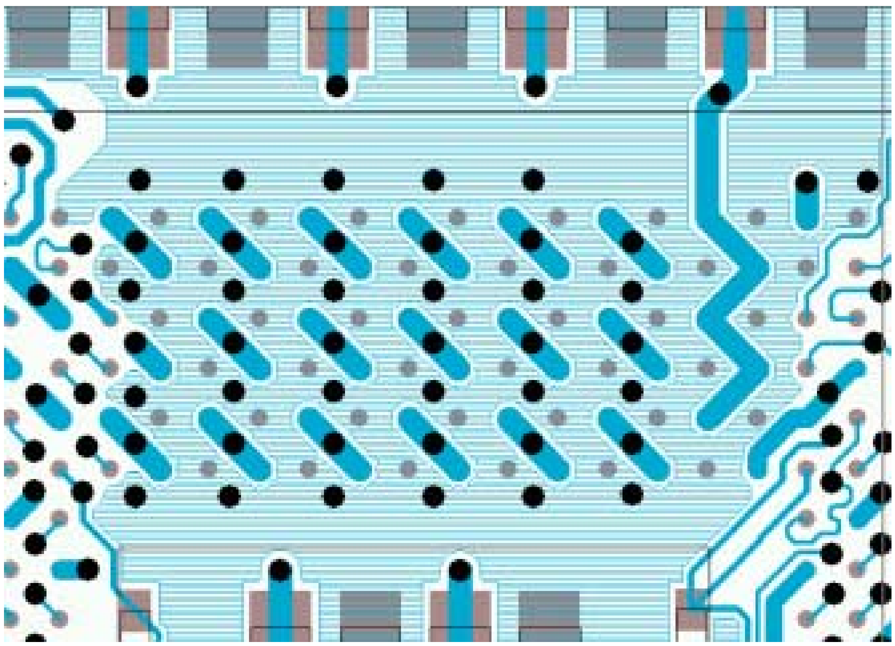
The high-frequency decoupling capacitors on the North side and within the socket cavity should be placed with alternating V_{CC_CPU} and V_{SS} to provide a better path for power delivery through the capacitor field. An example of this placement is shown in Figure 4-24.

Figure 4-24. Alternating V_{CC_CPU}/V_{SS} Capacitor Placement



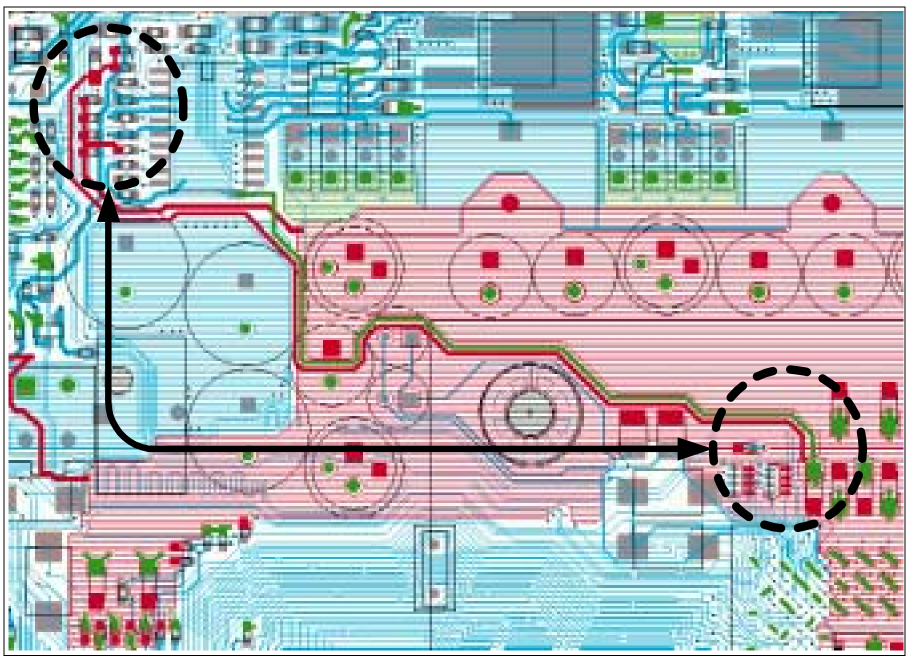
The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias be shared for two processor ground pins and for two processor power pins. Figure 4-25 illustrates this via sharing.

Figure 4-25. Shared Power and Ground Vias



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The V_{CC_SENSE} and V_{SS_SENSE} pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor VR Down Design Guidelines* is defined from pins AC14 (V_{CC_CPU}) and AC15 (V_{SS}) and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. Figure 4-26 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

Figure 4-26. Routing of VR Feedback Signal



4.6.5 Thermal Considerations

For a power delivery solution to meet the flexible motherboard (FMB) requirements, it must be able to deliver a high amount of current. This high amount of current also requires that the solution be able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

4.6.6 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 4-27.

Figure 4-27. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

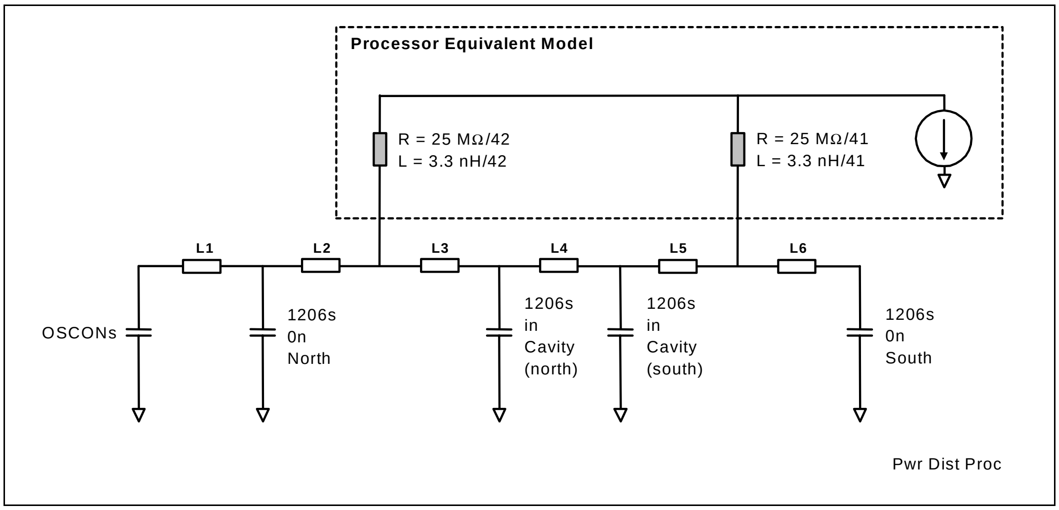


Table 4-15 lists model parameters for the system board shown in Figure 3-1.

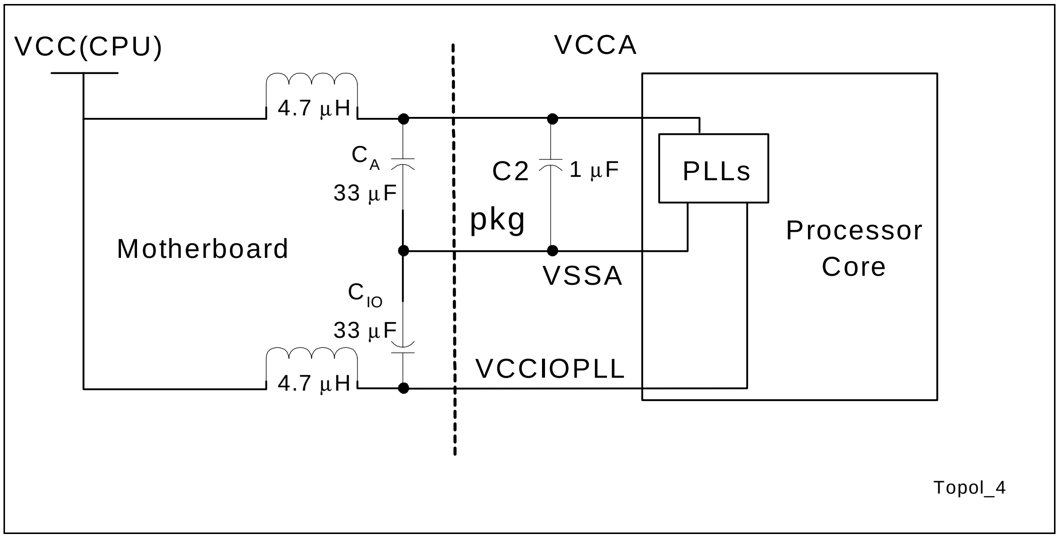
Table 4-15. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	113 pH
L3	0.392 mΩ	104 pH
L4	0.196 mΩ	52 pH
L5	0.392 mΩ	104 pH
L6	0.64 mΩ	200 pH

4.6.6.1 Filter Specifications for V_{CCA}, $V_{CCIOPLL}$, and V_{SSA}

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the processor silicon. Because these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system. It degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. The general desired filter topology is shown in Figure 4-28. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 4-28. Typical $V_{CCIOPLL}$, V_{CCA} and V_{SSA} Power Distribution



The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity this document will address the recommendation for the V_{CCA} filter design. The same characteristics and design approach is applicable for the $V_{CCIOPLL}$ filter design.

The AC low-pass recommendation, with input at V_{CC} and output measured across the capacitor (CA or CIO in Figure 4-28), is as follows:

$<$ 0.2 dB gain in pass band.

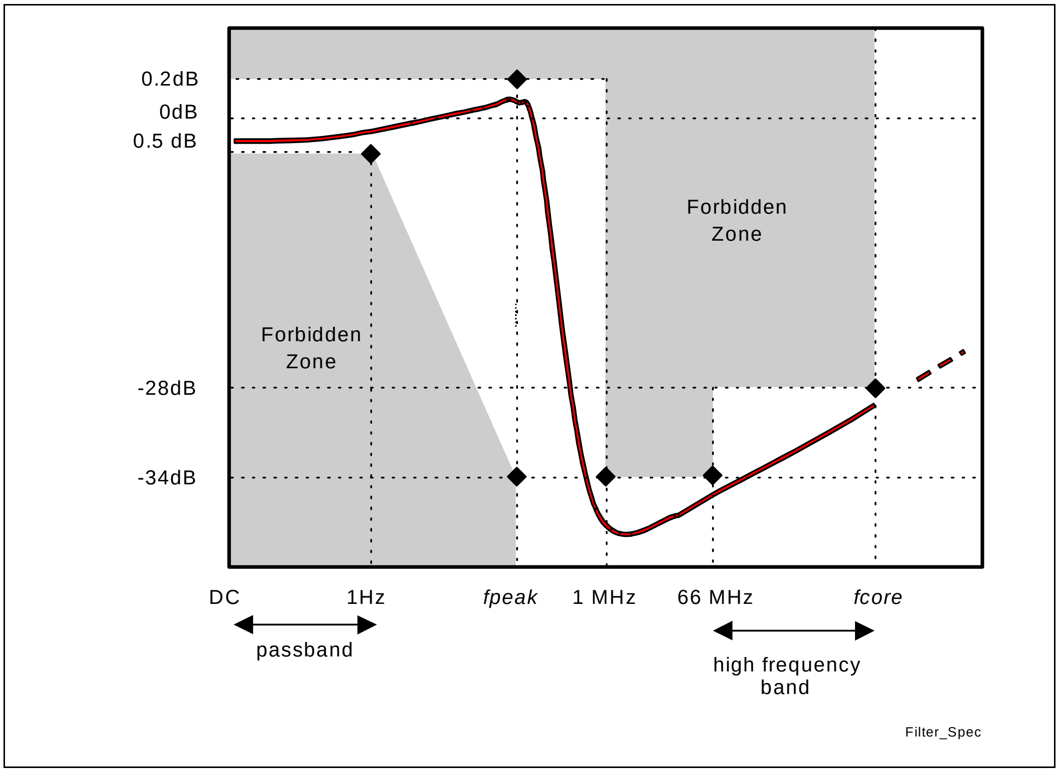
$<$ 0.5 dB attenuation in pass band $<$ 1 Hz (see DC drop in next set of requirements).

$>$ 34 dB attenuation from 1 MHz to 66 MHz.

$>$ 28 dB attenuation from 66 MHz to core frequency.

The filter recommendation (AC) is graphically shown in Figure 4-29.

Figure 4-29. Filter Recommendation

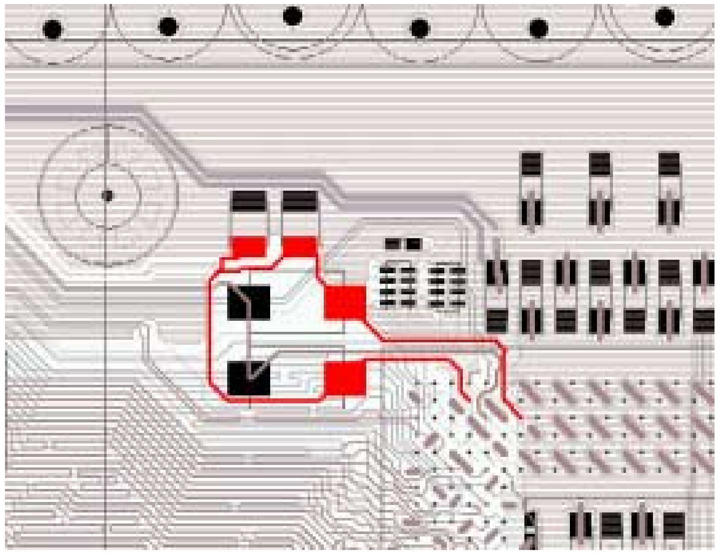


NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. Fpeak, if existent, should be less than 0.05 MHz.

Other Recommendations

1. Use shielded type inductors to minimize magnetic pickup.
2. Capacitors for the filters can have any value between 22 µF and 100 µF as long as components with ESL ≤ 5 nH and ESR <0.3 Ω are used.
3. Values of either 4.7 µH or 10 µH may be used for the inductor.
4. Filter should support DC current > 60 mA.
5. DC voltage drop from V_{CC} to V_{CCA} should be < 60 mV.
6. To maintain a DC drop of less than 60 mV, the total DC resistance of the filter from V_{CC_CPU} to the processor socket should be a maximum of 1 Ω.
7. Other routing requirements:
   a. C should be within 600 mils of the V_{CCA} and V_{SSA} pins. An example of the component placement is shown in Figure 4-30.
   b. V_{CCA} route should be parallel and next to V_{SSA} route (minimize loop area).
   c. A minimum 12-mil trace should be used to route from the filter to the processor pins.
   d. L should be close to C.

Figure 4-30. Example Component Placement of PLL Filter



4.6.7 Electrostatic Discharge Platform Recommendations

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that, when followed, can lead to higher ESD immunity. Electromagnetic fields, due to ESD, are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in Figure 4-31 through Figure 4-34. In addition, a ground fill cutout should be placed on the Vcc layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as seen in Figure 4-32). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100–150 mils apart or less.

In conclusion, Intel recommends the following:

- Fill the I/O area with the ground fill in all layers including signal layers whenever possible
- Extend the ground fill along the entire back I/O area
- Connect the ground fill to mounting holes
- Place stitching vias 100–150 mils apart in the entire ground fill

Figure 4-31. Top Signal Layer before the Ground Fill near the I/O Area

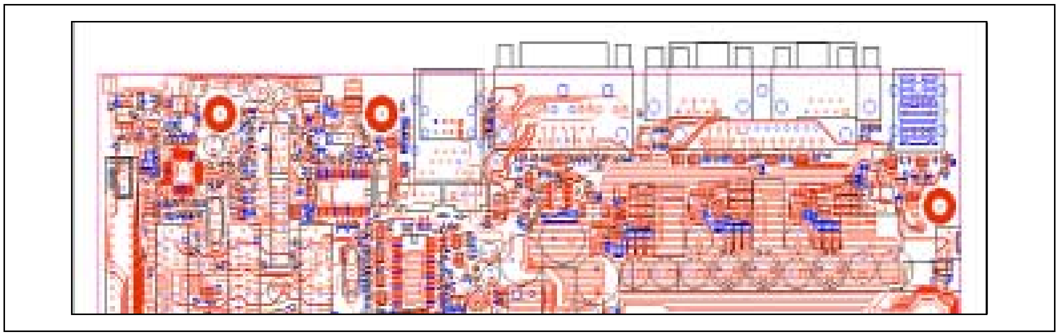


Figure 4-32. Top Signal Layer after the Ground Fill near the I/O Layer

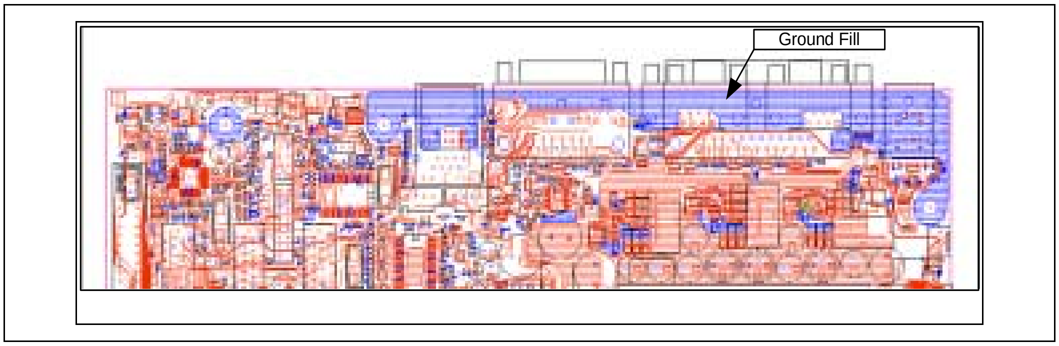


Figure 4-33. Bottom Signal Layer before The Ground Fill near the I/O Area

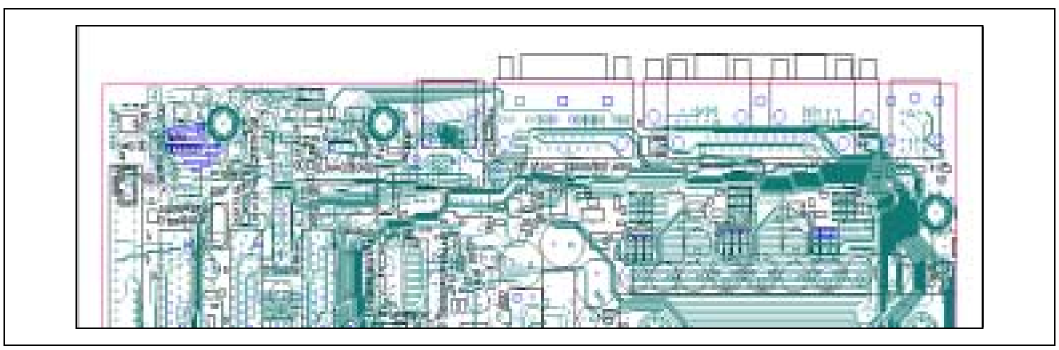
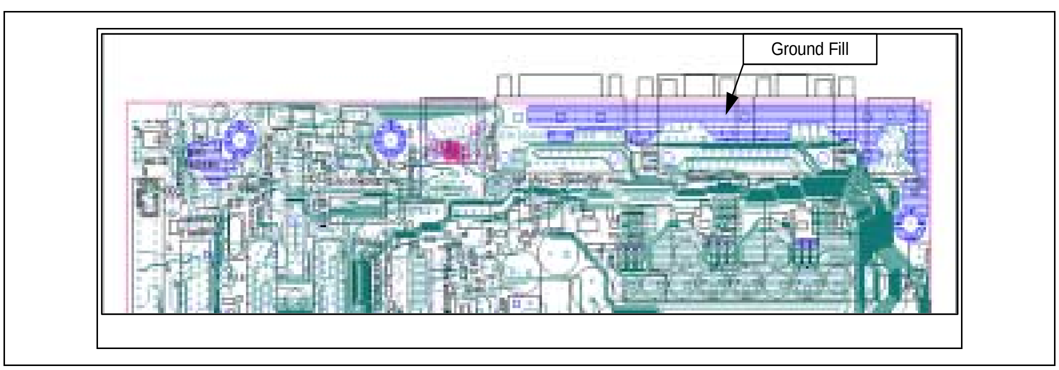


Figure 4-34. Bottom Signal Layer after the Ground Fill near the I/O Area



4.7 Intel® Pentium® 4 Processor and Intel® 845 Chipset Package Lengths

Processor Lengths			MCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	MCH Ball	Length (inches)
Address Group 0					
ADSTB0#	L5	0.210	HADSTB0#	R5	0.530
A3#	K2	0.368	HA3#	T4	0.518
A4#	K4	0.265	HA4#	T5	0.434
A5#	L6	0.155	HA5#	T3	0.728
A6#	K1	0.415	HA6#	U3	0.577
A7#	L3	0.304	HA7#	R3	0.551
A8#	M6	0.144	HA8#	P7	0.359
A9#	L2	0.372	HA9#	R2	0.643
A10#	M3	0.327	HA10#	P4	0.533
A11#	M4	0.246	HA11#	R6	0.397
A12#	N1	0.394	HA12#	P5	0.463
A13#	M1	0.408	HA13#	P3	0.576
A14#	N2	0.349	HA14#	N2	0.660
A15#	N4	0.241	HA15#	N7	0.407
A16#	N5	0.198	HA16#	N3	0.570
REQ0#	J1	0.427	HREQ0#	U6	0.402
REQ1#	K5	0.207	HREQ1#	T7	0.350
REQ2#	J4	0.270	HREQ2#	R7	0.393
REQ3#	J3	0.337	HREQ3#	U5	0.475
REQ4#	H3	0.356	HREQ4#	U2	0.599
Address Group 1					
ADSTB1#	R5	0.214	HADSTB1#	N6	0.438
A17#	T1	0.470	HA17#	K4	0.550
A18#	R2	0.404	HA18#	M4	0.580
A19#	P3	0.303	HA19#	M3	0.648
A20#	P4	0.246	HA20#	L3	0.604
A21#	R3	0.334	HA21#	L5	0.521
A22#	T2	0.388	HA22#	K3	0.624

Processor Lengths			MCH Lengths		
Signal	**Processor Ball**	**Length (inches)**	**Signal**	**MCH Ball**	**Length (inches)**
A23#	U1	0.458	HA23#	J2	0.685
A24#	P6	0.156	HA24#	M5	0.509
A25#	U3	0.379	HA25#	J3	0.636
A26#	T4	0.281	HA26#	L2	0.648
A27#	V2	0.417	HA27#	H4	0.634
A28#	R6	0.166	HA28#	N5	0.472
A29#	W1	0.493	HA29#	G2	0.792
A30#	T5	0.217	HA30#	M6	0.449
A31#	U4	0.285	HA31#	L7	0.365
Data Group 0					
DSTBN0#	E22	0.338	HDSTBN0#	AD4	0.759
DSTBP0#	F21	0.326	HDSTBP0#	AD3	0.801
D0#	B21	0.414	HD0#	AA2	0.649
D1#	B22	0.475	HD1#	AB5	0.564
D2#	A23	0.538	HD2#	AA5	0.531
D3#	A25	0.608	HD3#	AB3	0.678
D4#	C21	0.386	HD4#	AB4	0.628
D5#	D22	0.386	HD5#	AC5	0.635
D6#	B24	0.535	HD6#	AA3	0.623
D7#	C23	0.464	HD7#	AA6	0.468
D8#	C24	0.515	HD8#	AE3	0.802
D9#	B25	0.590	HD9#	AB7	0.495
D10#	G22	0.274	HD10#	AD7	0.609
D11#	H21	0.203	HD11#	AC7	0.548
D#12	C26	0.589	HD12#	AC6	0.579
D13#	D23	0.462	HD13#	AC3	0.709
D14#	J21	0.183	HD14#	AC8	0.590
D15#	D25	0.550	HD15#	AE2	0.856
DBI0#	E21	0.309	DBI0#	AD5	0.637
Data Group 1					
DSTBN1#	K22	0.301	HDSTBN1#	AE6	0.693
DSTBP1#	J23	0.306	HDSTBP1#	AE7	0.638
D16#	H22	0.272	HD16#	AG5	0.845
D17#	E24	0.480	HD17#	AG2	0.904

Processor Lengths			MCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	MCH Ball	Length (inches)
D18#	G23	0.358	HD18#	AE8	0.663
D19#	F23	0.418	HD19#	AF6	0.759
D20#	F24	0.443	HD20#	AH2	0.965
D21#	E25	0.508	HD21#	AF3	0.798
D22#	F26	0.513	HD22#	AG3	0.898
D23#	D26	0.597	HD23#	AE5	0.709
D24#	L21	0.176	HD24#	AH7	0.863
D25#	G26	0.524	HD25#	AH3	0.904
D26#	H24	0.412	HD26#	AF4	0.794
D27#	M21	0.171	HD27#	AG8	0.789
D28#	L22	0.245	HD28#	AG7	0.785
D29#	J24	0.401	HD29#	AG6	0.785
D30#	K23	0.313	HD30#	AF8	0.711
D31#	H25	0.473	HD31#	AH5	0.892
DBI1#	G25	0.458	DBI1#	AG4	0.888
Data Group 2					
DSTBN2#	K22	0.252	HDSTBN2#	AE11	0.595
DSTBP2#	J23	0.266	HDSTBP2#	AD11	0.532
D32#	M23	0.300	HD32#	AC11	0.514
D33#	N22	0.226	HD33#	AC12	0.565
D34#	P21	0.178	HD34#	AE9	0.652
D35#	M24	0.371	HD35#	AC9	0.566
D36#	N23	0.271	HD36#	AE10	0.605
D37#	M26	0.454	HD37#	AD9	0.635
D38#	N26	0.437	HD38#	AG9	0.724
D39#	N25	0.383	HD39#	AC10	0.543
D40#	R21	0.165	HD40#	AE12	0.558
D41#	P24	0.343	HD41#	AF10	0.666
D42#	R25	0.381	HD42#	AG11	0.703
D43#	R24	0.329	HD43#	AG10	0.705
D44#	T26	0.420	HD44#	AH11	0.754
D45#	T25	0.380	HD45#	AG12	0.669
D46#	T22	0.221	HD46#	AE13	0.563
D47#	T23	0.279	HD47#	AF12	0.596
DBI2#	P26	0.441	DBI2#	AH9	0.775

Processor Lengths			MCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	MCH Ball	Length (inches)
Data Group 3					
DSTBN3#	W22	0.298	HDSTBN3#	AC15	0.443
DSTBP3#	W23	0.300	HDSTBP3#	AC16	0.395
D48#	U26	0.419	HD48#	AG13	0.668
D49#	U24	0.324	HD49#	AH13	0.712
D50#	U23	0.270	HD50#	AC14	0.412
D51#	V25	0.384	HD51#	AF14	0.548
D52#	U21	0.167	HD52#	AG14	0.621
D53#	V22	0.252	HD53#	AE14	0.520
D54#	V24	0.341	HD54#	AG15	0.612
D55#	W26	0.447	HD55#	AG16	0.610
D56#	Y26	0.454	HD56#	AG17	0.619
D57#	W25	0.426	HD57#	AH15	0.703
D58#	Y23	0.336	HD58#	AC17	0.399
D59#	Y24	0.386	HD59#	AF16	0.580
D60#	Y21	0.222	HD60#	AE15	0.534
D61#	AA25	0.426	HD61#	AH17	0.672
D62#	AA22	0.268	HD62#	AD17	0.419
D63#	AA24	0.394	HD63#	AE16	0.503
DBI3#	V21	0.202	DBI3#	AD15	0.431

5 PC133 System Memory Design Guidelines

5.1 SDRAM Signal Groups

The 845 chipset PC133 Synchronous DRAM (SDRAM) memory interface consists of 122 CMOS signals. These CMOS signals can be divided into six signal group categories: Data, Address and Control, Chip Select, Clock Enable, Clock, and Feedback.

Table 5-1. CMOS Signals and Signal Groups for the Intel® 845 Chipset

Data	Address/ Control	Chip Select	Clock Enable	Clock	Feedback
SDQ[63:0] SCB[7:0]	SMA[12:0] SBS[1:0] SRAS# SCAS# SWE#	SCS[11:0]#	SCKE[5:0]	SCK[11:0]	RDCLKO RDCLKIN

5.2 PC133 System Memory Topology and Layout Design Guidelines

To provide a good current return path and limit noise on system memory signals, all system memory signals should reference a single contiguous plane from the MCH to the DIMM connectors, and from DIMM connector to DIMM connector. Based on the four-layer stack-up example in Section 3.2, the MCH system memory signal ball field, and the MCH system memory package referencing, the following PC133 system memory guidelines should be followed in 845 chipset-based systems.

5.2.1 3 DIMM Topology and Layout Guidelines

5.2.1.1 Data—SDQ[63:0], SCB[7:0]

The MCH provides one pin per data bus signal. This signal group includes the 64-bit wide data bus and the eight bits for Error Checking and Correction (ECC) bus signals. The data group signals should break out of the MCH on the top signal layer and be routed from the MCH to the middle DIMM. Then they should stub to the first DIMM and last DIMM on the bottom signal routing layer. To provide an adequate current return path, bypass capacitors should be added. For system memory bypass capacitor guidelines, see Section 5.3.

Figure 5-1 and Table 5-2 illustrate and describe the recommended topology and layout routing guidelines for the SDRAM data signal group.

Figure 5-1. 3-DIMM Routing Topology for Data Signals

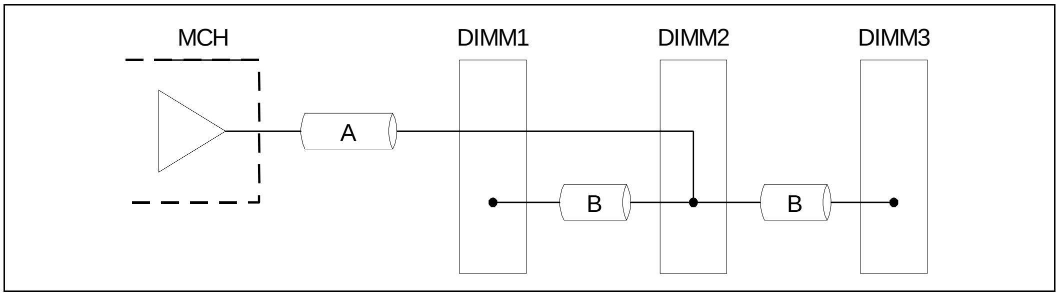


Table 5-2. 3-DIMM Routing Guidelines for Data Signals

Parameter	Routing Guidelines
Signal Group	Data—SDQ[63:0], SCB[7:0]
Topology	Balanced “T”
Reference Plane	Single plane referenced from MCH to middle DIMM. Single plane referenced from middle DIMM to first and last DIMM.
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	12 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	2.5 inches to 4.5 inches
Trace Length—B	0.4 inch to 0.6 inch
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch 5 mil width with 8 mil spacing for a max of 1.50 inches

Figure 5-2. Routing Example, Top Layer—SDQ[63:0], SCB[7:0]

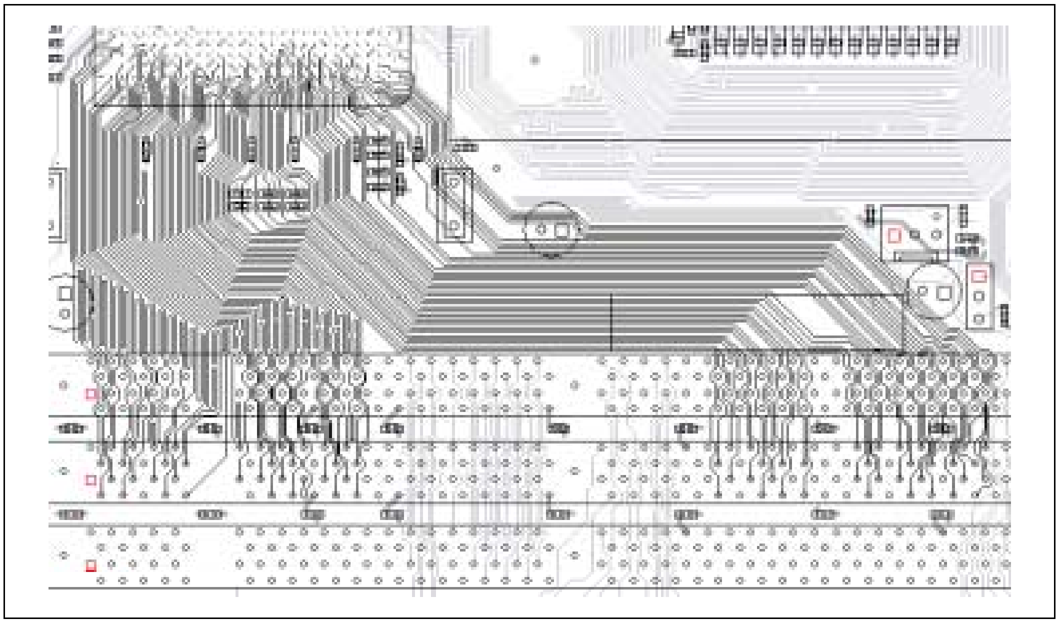
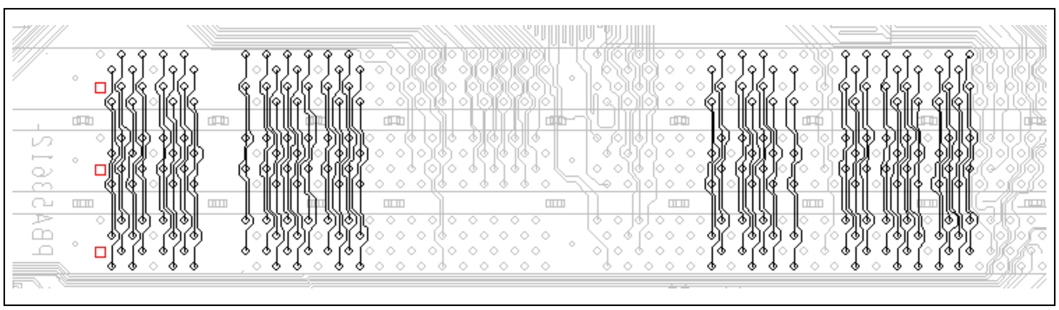


Figure 5-3. Routing Example, Bottom Layer—SDQ[63:0], SCB[7:0]



5.2.1.2 Chip Select and Clock Enable—SCS[11:0]#, SCKE[5:0]

The MCH provides two chip select outputs and one clock enable output signal per PC133 DIMM device Row. These signals should transition from the top signal layer to the bottom signal layer under the MCH and be routed on the same layer for the entire length to all DIMMs. The trace lengths from the signal balls to their vias at the MCH should be kept as short as possible.

The following figures and tables describe the recommended topology and layout routing guidelines for a single PC133 DIMM socket. These topologies and layout routing guidelines should be repeated for all three PC133 DIMM slots.

Figure 5-4. 3-DIMM Routing Topology for SCS# Signals

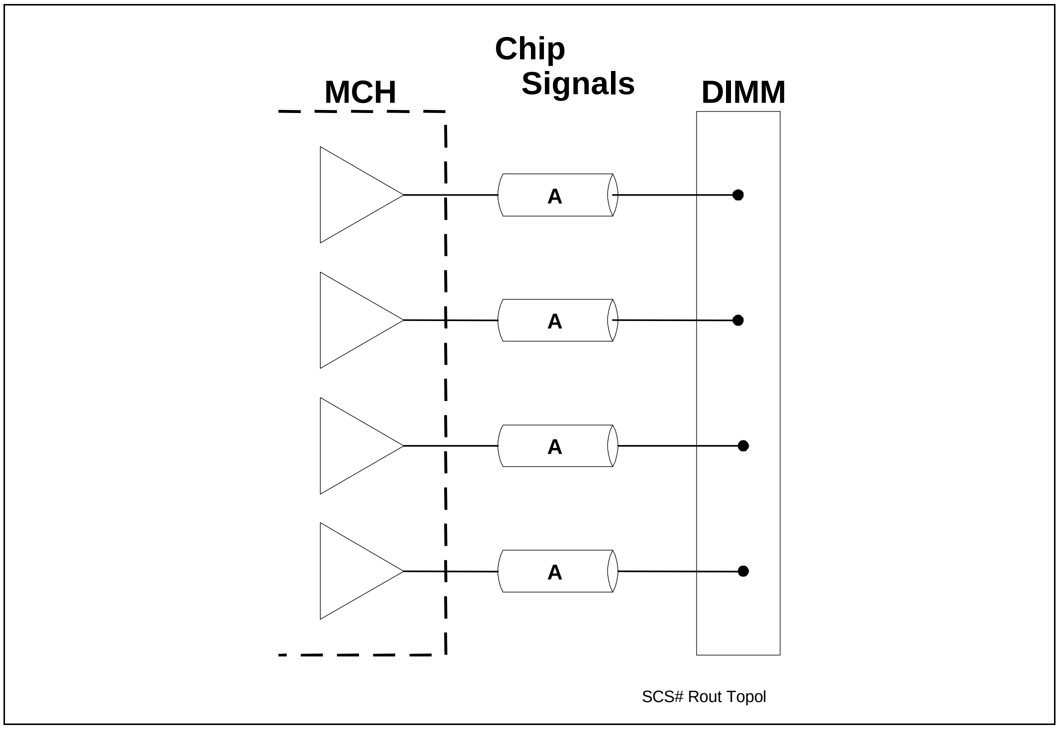


Table 5-3. 3-DIMM Routing Guidelines for SCS# Signals

Parameter	Routing Guidelines
Signal Group	SCS[11:0]#
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	10 mils (Recommend 12 mils if possible)
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	3.0 inches to 4.0 inches
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch

Figure 5-5. 3-DIMM Routing Topology for SCKE# Signals

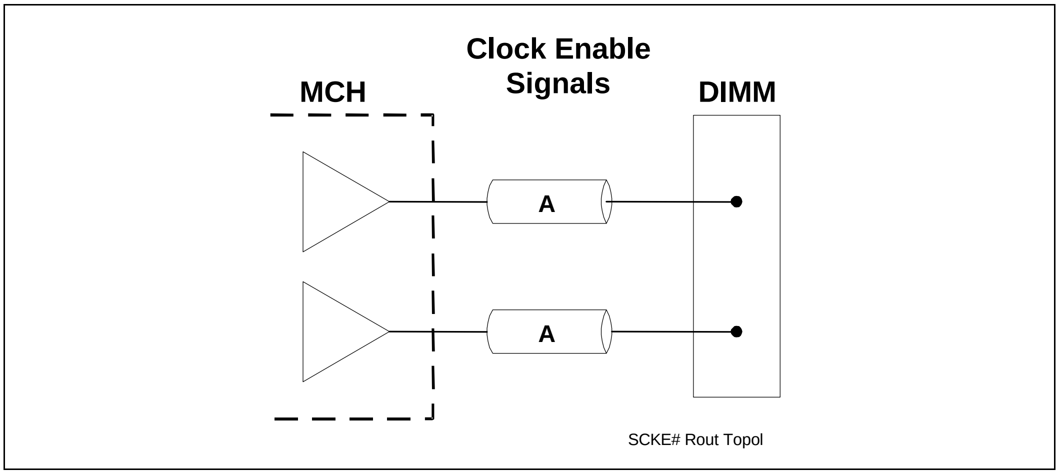
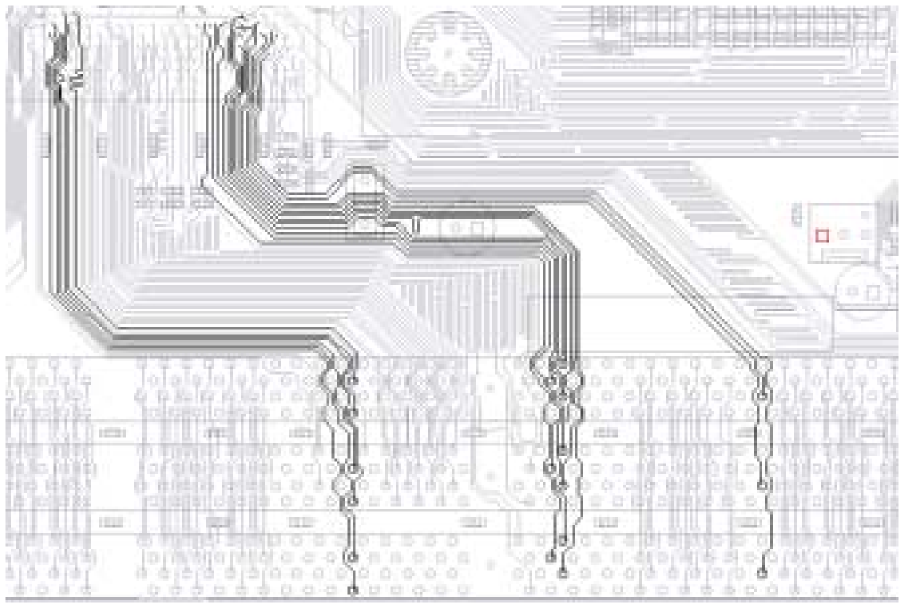


Table 5-4. 3-DIMM Routing Guidelines for SCKE# Signals

Parameter	Routing Guidelines
Signal Group	SCKE[5:0]
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	40 Ω ± 15%
Trace Width	10 mils
Minimum Trace Spacing	10 mils (Recommend 12 mils if possible)
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	3.0 inches to 4.4 inches
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch

Figure 5-6. Routing Example, Bottom Layer—SCS [11:0]#, SCKE[5:0]



5.2.1.3 Address and Control—SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#

The MCH provides one pin per address signal, one pin for RAS#, one pin for CAS#, one pin for WE#, and one pin per bank address signal. These signals should transition from the top signal layer to the bottom signal layer under the MCH and be routed from the MCH to the middle DIMM. Then they should stub to the first DIMM and last DIMM on the top signal routing layer. The trace lengths from the signal balls to their signal vias at the MCH should be kept as short as possible. To provide a clean current return path, bypass capacitors should be added. For system memory bypass capacitor guidelines, refer to Section 5.3.

Figure 5-7 and Table 5-5 illustrate and describe the recommended topology and layout routing guidelines for the PC133 Address and Control signals.

Figure 5-7. 3-DIMM Routing Topology for Address and Control Signals

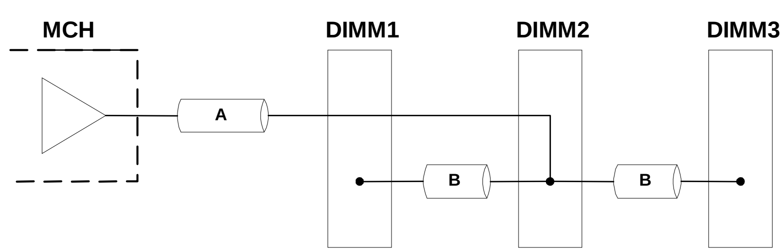


Table 5-5. 3-DIMM Routing Guidelines for Address and Control Signals

Parameter	Routing Guidelines
Signal Group	SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#
Topology	Balanced "T"
Reference Plane	Single plane referenced from MCH to middle DIMM. Single plane referenced from middle DIMM to first and last DIMM.
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	10 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	2.5 inches to 4.0 inches
Trace Length—B	0.40 inch to 0.60 inch
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch 5 mil width with 8 mil spacing for a max of 1.0 inch

Figure 5-8. Routing Example, Bottom Layer—SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#

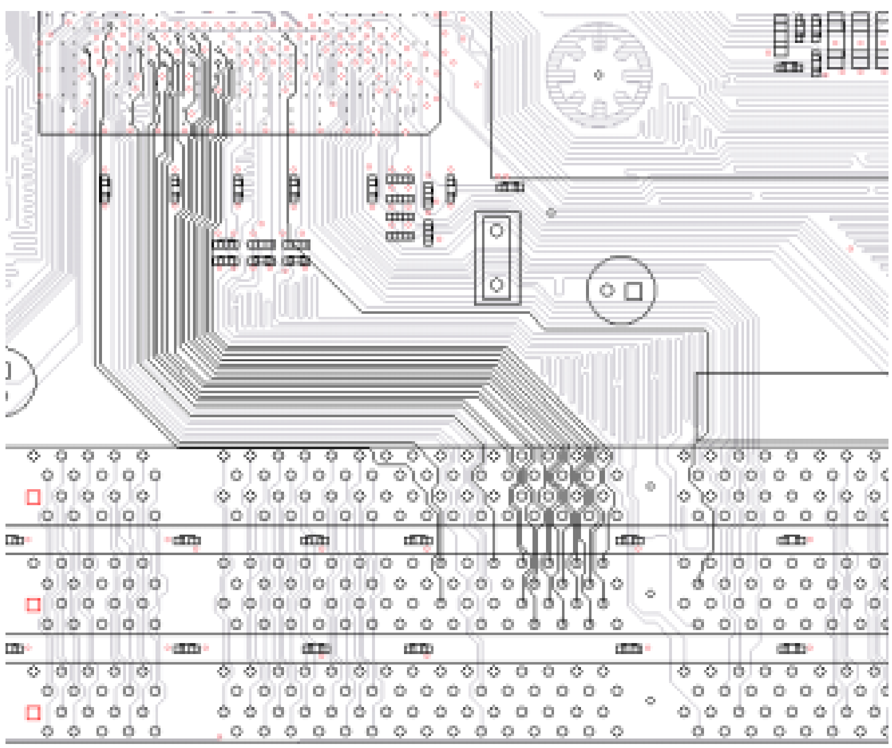
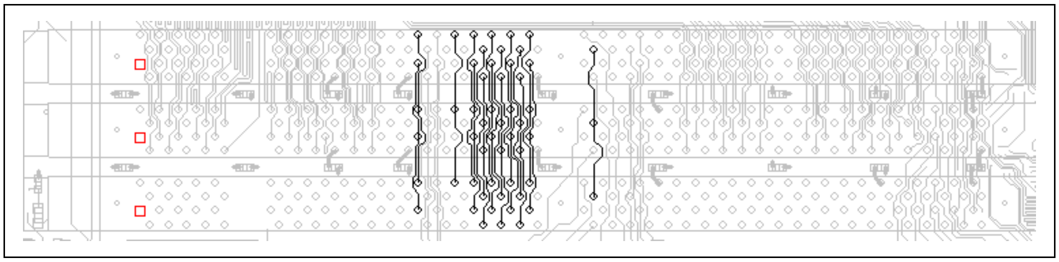


Figure 5-9. Routing Example, Top Layer—SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#



5.2.1.4 Clocks—SCK[11:0]

The 845 chipset MCH provides two clock signals per PC133 DIMM device row. The clock signals should transition from the top signal layer to the bottom signal layer and be routed to the DIMMs on the bottom signal layer. The clocks should be length matched from MCH die pad to the DIMM pin. For example, the total trace length from the MCH die pad to the DIMM pin should be 5.9 inches ± 0.05 inch. Refer to Table 5-14 for package trace length data.

Figure 5-10 and Table 5-6 illustrate and describe the recommended topology and layout routing guidelines for the PC133 clocks. This topology and this set of layout routing guidelines should be repeated for all three PC133 DIMM slots.

Figure 5-10. 3-DIMM Routing Topology for Clock Signals

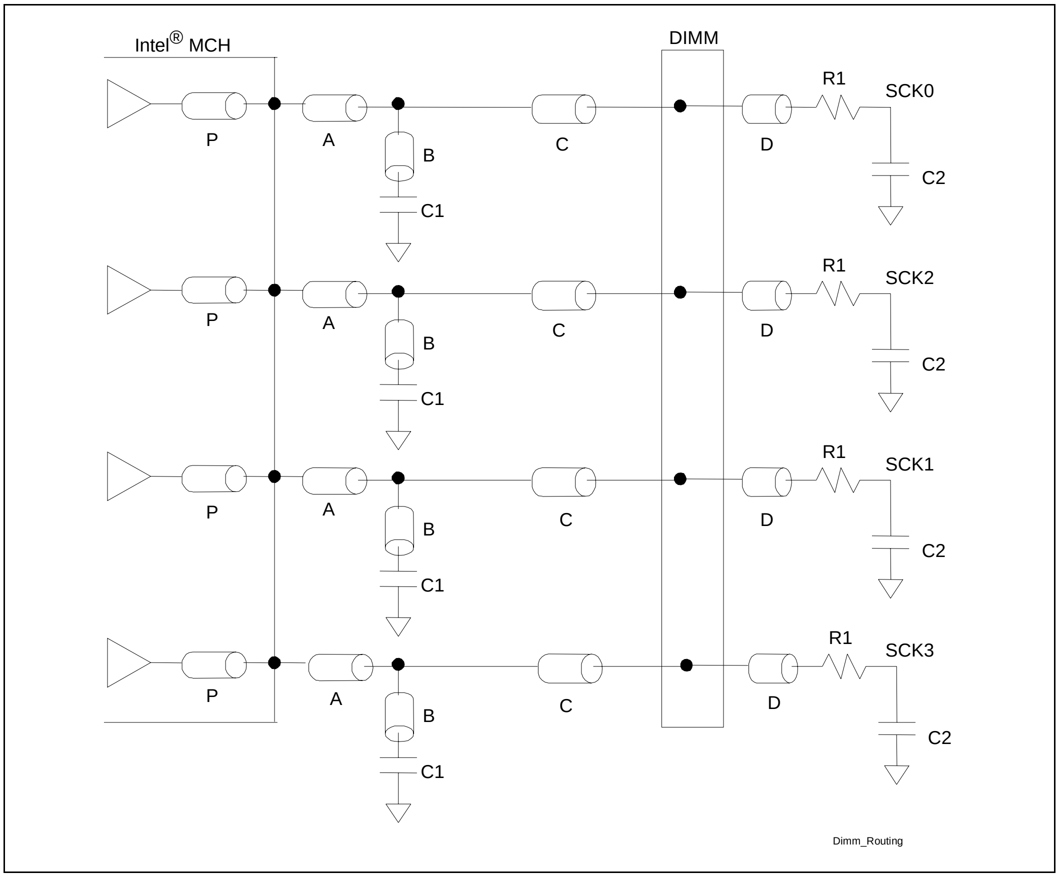


Table 5-6. 3-DIMM Routing Guidelines for Clock Signals

Parameter	Routing Guidelines
Signal Group	SCK[11:0]
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	50 Ω ± 15%
Trace Width	7 mils
Minimum Trace Spacing	15 mils
Minimum Group Spacing (spacing from other signal groups)	15 mils
Trace Length—P (package trace length)	See Table 5-14
Trace Length—A	0.0 inch to 1.0 inch from MCH ball to EMI capacitor stub
Trace Length—B	0.0 inch to 0.25 inch.
Trace Length—C	4.0 inches to 5.0 inches
Trace Length—D	0 inch to 1.5 inches
Total Length Limits (P + A + C)	5.9 inches ± 0.05 inch from MCH die pad to DIMM pin
Breakout Guidelines	7 mil width with 5 mil spacing for a max of 0.50 inch 7 mil width with 10 mil spacing for a max of 1.0 inch

Note: The value of the AC termination network, R1 and C2, is 51 Ω and 270 pF ± 5%.
The value of the EMI filter capacitor C1 is 22 pF ± 5%.

Figure 5-11. Routing Example, Bottom Layer—SCK[11:0]

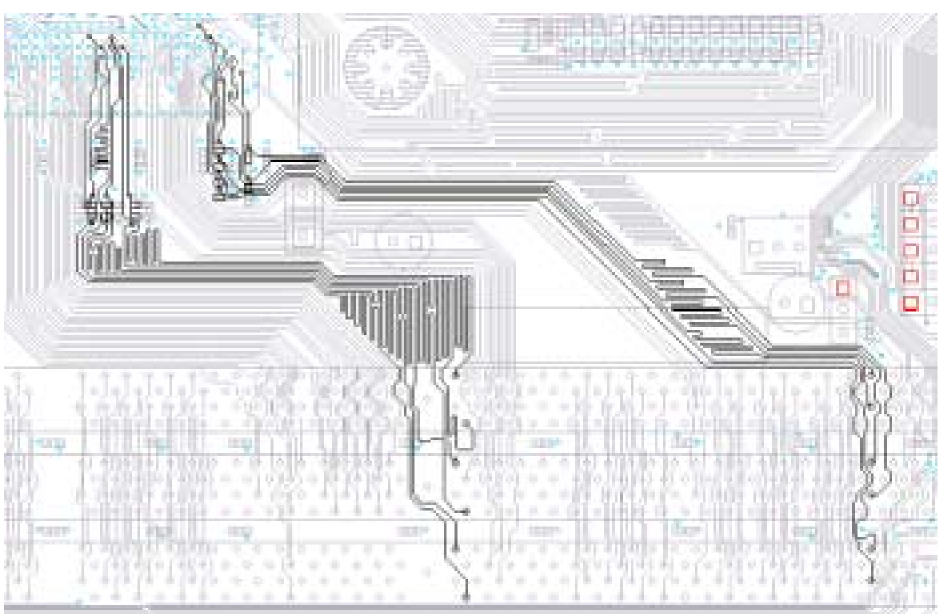
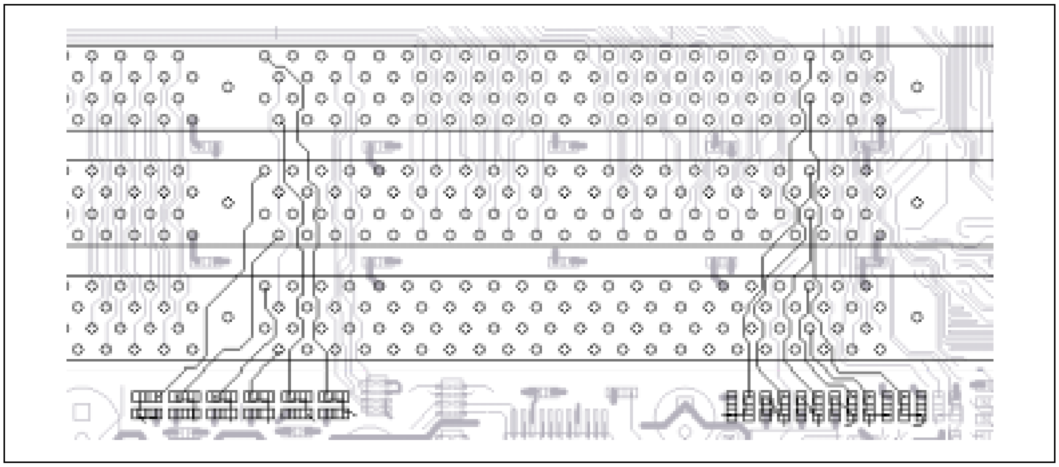


Figure 5-12. Routing Example, Top Layer—SCK[11:0] Termination



5.2.1.5 Feedback—RDCLKO, RDCLKIN

The MCH provides a feedback reference clock output (RDCLKO) and reference clock input (RDCLKIN), which is used during SDRAM reads. The RDCLKO ball is connected directly to the RDCLKIN ball through a very short trace on the motherboard. A test point should be added to this net for probing. Figure 5-13 and Table 5-7 illustrate and describe the recommended topology and layout routing guidelines for the SDRAM feedback signal.

Figure 5-13. 3-DIMM Routing Topology for Feedback Signals

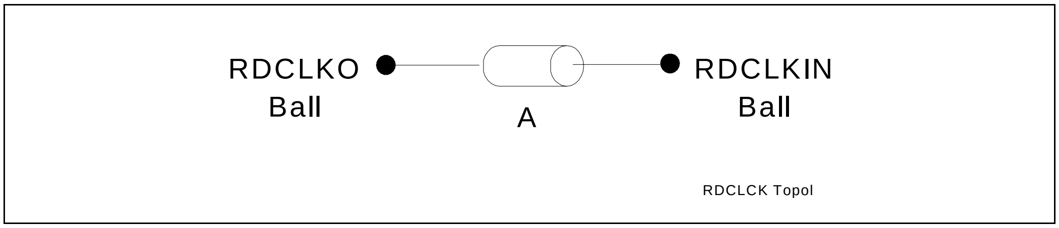


Table 5-7. 3-DIMM Routing Guidelines for Feedback Signals

Parameter	Routing Guidelines
Signal Group	RDCLKO, RDCLKIN
Topology	Point-to-point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	50 Ω ± 15%
Trace Width	7 mils
Minimum Group Spacing (spacing from other signal groups)	5 mils
Trace Length—A	50 mils

5.2.2 2-DIMM Topology and Layout Guidelines

5.2.2.1 Data—SDQ[63:0], SCB[7:0]

The MCH provides one pin per data bus signal. This signal group includes the 64-bit data bus and the 8 bits for Error Checking and Correction (ECC) bus signals. These signals should break out of the MCH and be routed to the DIMMs on the top layer in a daisy chain topology. Figure 5-14 and Table 5-8 illustrate and describe the recommended topology and layout routing guidelines for the SDRAM data signals.

Figure 5-14. 2-DIMM Routing Topology for Data Signals

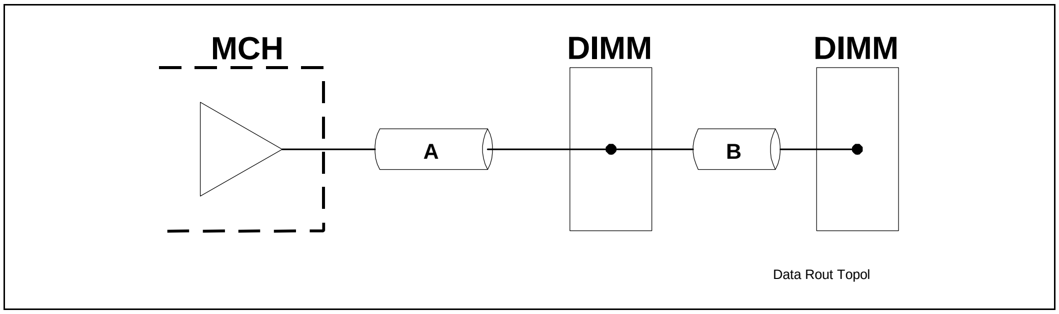


Table 5-8. 2-DIMM Routing Guidelines for Data Signals

Parameter	Routing Guidelines
Signal Group	SDQ[63:0], SCB[7:0]
Topology	Daisy Chain
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	12 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	2.0 n to 4.0 n
Trace Length—B	0.4 inch to 0.6 inch
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch 5 mil width with 8 mil spacing for a max of 1.50 inches

5.2.2.2 Chip Select and Clock Enable—SCS[7:0]#, SCKE[3:0]

The MCH provides two chip select outputs and one clock enable output signal per PC133 DIMM device Row. These signals are single plane referenced and should transition from the top signal layer to the bottom signal layer under the MCH and be routed to the DIMMs. The trace lengths from these signal balls to their signal vias at the MCH should be kept as short as possible. The unused chip selects and clock enables, SCS[8:11] and SCKE[4:5], should be left floating. They are disabled on a 2-DIMM platform.

The following diagrams and tables illustrate and describe the recommended topology and layout routing guidelines for a single PC133 DIMM socket. This topology and layout routing guidelines should be repeated for both PC133 DIMM slots.

Figure 5-15. 2-DIMM Routing Topology for SCS# Signals

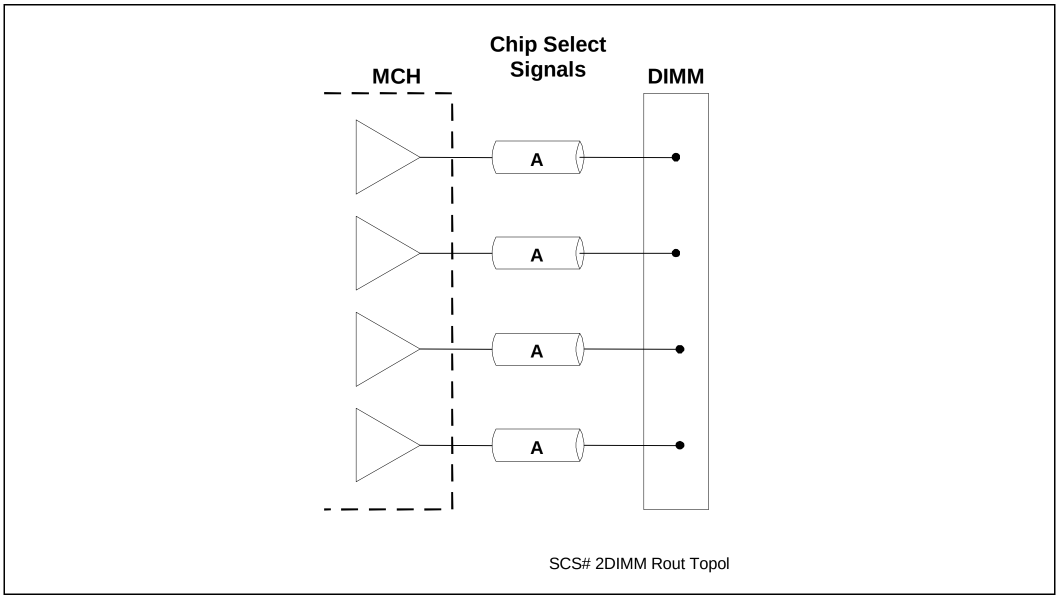


Table 5-9. 2-DIMM Routing Guidelines for SCS# Signals

Parameter	Routing Guidelines
Signal Group	SCS[7:0]#
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	10 mils (Recommend 12 mils if possible)
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	3.0 inches to 4.0 inches
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch

Figure 5-16. 2-DIMM Routing Topology for SCKE# Signals

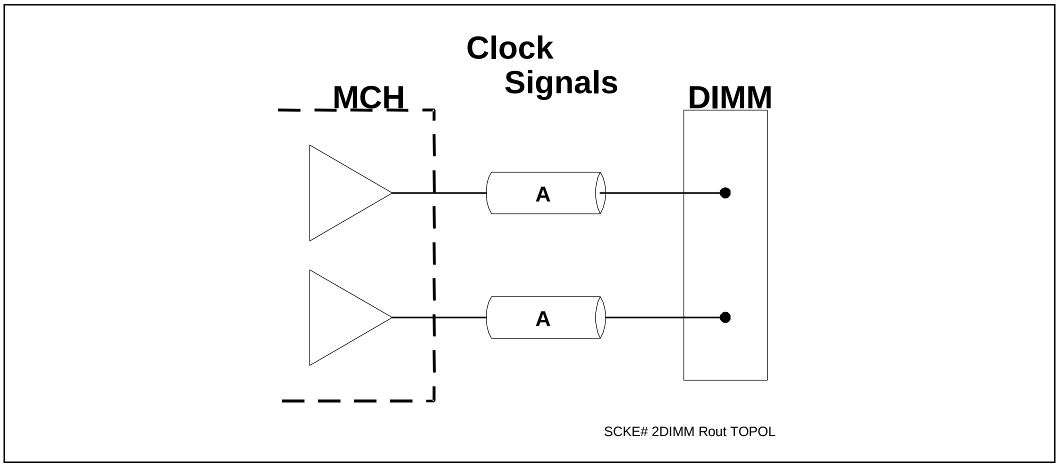


Table 5-10. 2-DIMM Routing Guidelines for SCKE# Signals

Parameter	Routing Guidelines
Signal Group	SCKE[3:0]
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	40 Ω ± 15%
Trace Width	10 mils
Minimum Trace Spacing	10 mils (Recommend 12 mils if possible)
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	3.0 inches to 4.0 inches
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch

5.2.2.3 Address and Control—SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#

The MCH provides one pin per address signal, one pin for RAS#, one pin for CAS#, one pin for WE#, and one pin per bank address signal. These signals are single plane referenced. They should transition from the top signal layer to the bottom signal layer under the MCH, and should be routed to the first DIMM, then to the second DIMM in a daisy chain topology. The trace lengths from the signal balls to their signal vias at the MCH should be kept as short as possible. Figure 5-17 and Table 5-11 illustrate and describe the recommended topology and layout routing guidelines for the SDRAM address and control signals.

Figure 5-17. 2-DIMM Routing Topology for Address and Control Signals

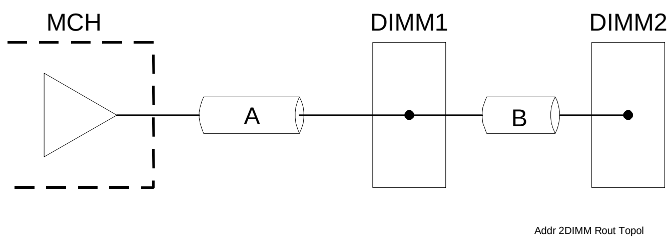


Table 5-11. 2-DIMM Routing Guidelines for Address and Control Signals

Parameter	Routing Guidelines
Signal Group	SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#
Topology	Daisy Chain
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	10 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length—A	2.0 inches to 3.0 inches
Trace Length—B	0.4 inch to 0.6 inch
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50 inch 5 mil width with 8 mil spacing for a max of 1.50 inches

5.2.2.4 Clocks—SCK[7:0]

The MCH provides two clock signals per SDRAM DIMM device Row. The clock signals should transition from the top signal layer to the bottom signal layer, and should be routed to the DIMMs on the bottom signal layer. The clocks should be length matched from MCH die pad to DIMM pin. For example, the total trace length from the MCH die pad to the DIMM pin should be 5.3 inches ± 0.05 inches Refer to Table 5-14 for package trace length data. The unused clocks, SCK[9:11], should be left floating—they are disabled on a 2-DIMM platform.

Figure 5-18 and Table 5-12 illustrate and describe the recommended topology and layout routing guidelines for the PC133 clocks. This topology and layout routing guidelines should be repeated for both PC133 DIMM slots.

Figure 5-18. 2-DIMM Routing Topology for Clock Signals

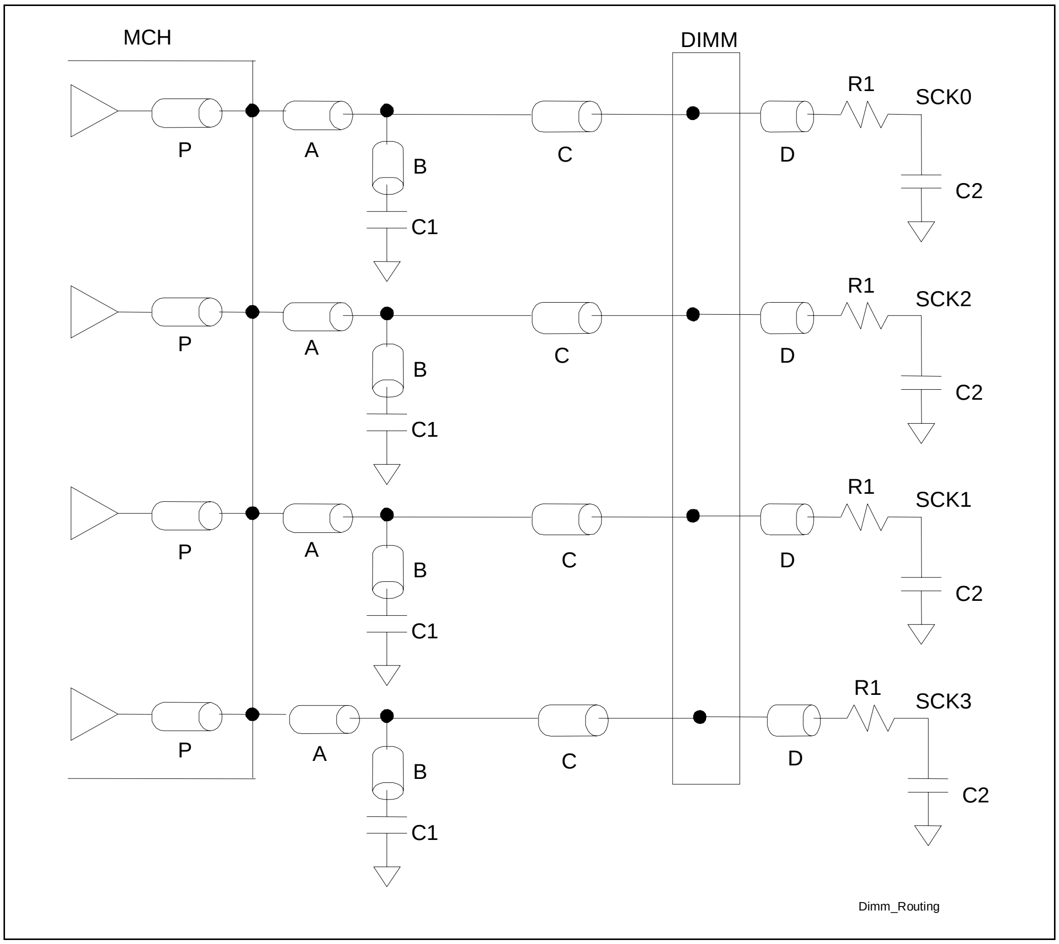


Table 5-12. 2-DIMM Routing Guidelines for Clock Signals

Parameter	Routing Guidelines
Signal Group	SCK[7:0]
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	50 Ω ± 15%
Trace Width	7 mils
Minimum Trace Spacing	15 mils
Minimum Group Spacing (spacing from other signal groups)	15 mils
Trace Length—P (package trace length)	See Table 5-14
Trace Length—A	0.0 inch to 1.0 inch from MCH ball to EMI capacitor stub
Trace Length—B	0.0 inch to 0.25 inch
Trace Length—C	4.0 inches to 5.0 inches
Trace Length—D	0 inch to 1.5 inches
Total Length Limits (P + A + C)	5.3 inches ± 0.05 inch from MCH die pad to DIMM pin
Breakout Guidelines	7 mil width with 5 mil spacing for a max of 0.50 inch 7 mil width with 10 mil spacing for a max of 1.0 inch

Note: The value of the AC termination network, R1 and C2, is 51 Ω and 270 pF ± 5%.
The value of the EMI filter capacitor C1 is 22 pF ± 5%.

5.2.2.5 Feedback—RDCLKO, RDCLKIN

The MCH provides a feedback reference clock output (RDCLKO) and reference clock input (RDCLKIN), which are used during SDRAM reads. The RDCLKO ball is connected directly to the RDCLKIN ball through a very short trace on the motherboard. A test point should be added to this net for probing. Figure 5-19 and Table 5-13 illustrate and describe the recommended topology and layout routing guidelines for the SDRAM feedback signal.

Figure 5-19. 2-DIMM Routing Topology for Feedback Signals

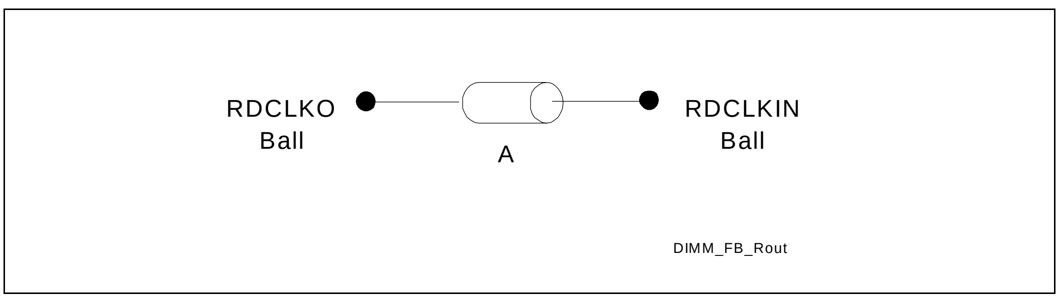


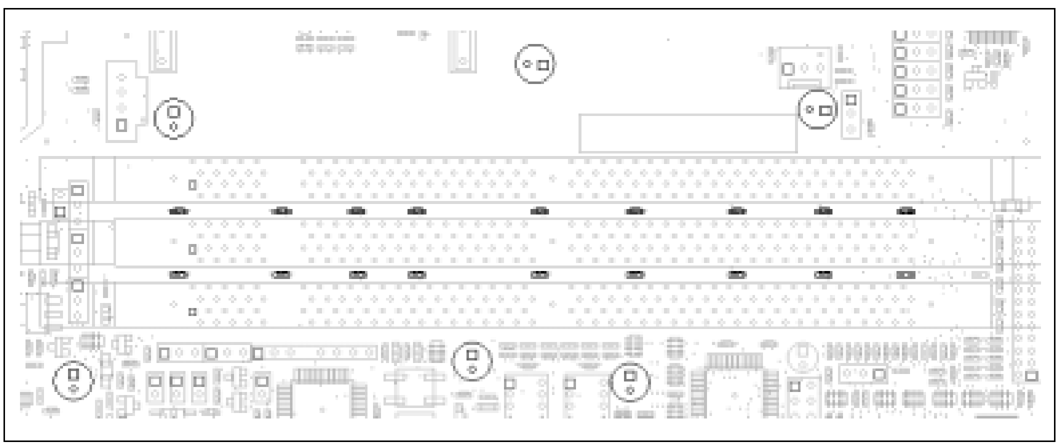
Table 5-13. 2-DIMM Routing Guidelines for Feedback Signals

Parameter	Routing Guidelines
Signal Group	RDCLKO, RDCLKIN
Topology	Point-to-Point
Reference Plane	Single plane referenced (contiguous over entire length)
Characteristic Trace Impedance (Zo)	50 Ω ± 15%
Minimum Trace Width	7 mils
Minimum Group Spacing (spacing from other signal groups)	5 mils
Trace Length—A	50 mils

5.3 DIMM Decoupling Guidelines

Bypass capacitors should be added between the V_{CCSM} voltage rail and ground, where V_{CCSM} is the 3.3 V power plane. Place nine evenly spaced 0.1 µF capacitors between each DIMM. This should ensure a clean current return path. (See Figure 5-20). For bulk decoupling, place six ,100 µF bulk capacitors around the DIMMs. (See Figure 5-20).

Figure 5-20. DIMM Decoupling Example

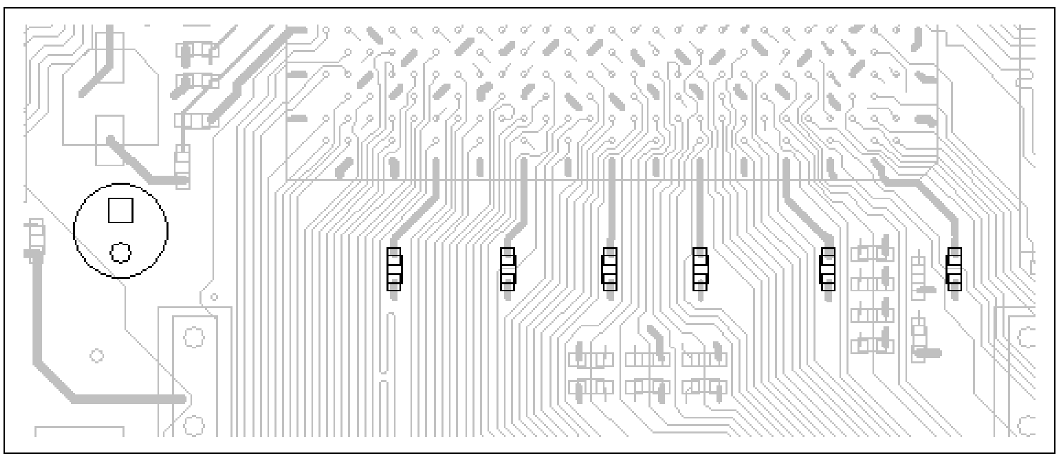


5.4 MCH V_{CCSM} Decoupling Guidelines

The MCH requires both high-frequency and bulk decoupling for V_{CCSM}. Every MCH power and ground ball in the system memory interface should have its own via. For 3.3 V high-frequency decoupling, a minimum of six, 0603 0.1 µF capacitors are required. These capacitors should be evenly distributed along the MCH SDR interface as shown in Figure 5-21. The trace from the ground end of the capacitor should be as wide as possible and must connect to an outer row ground ball on the on the MCH. The power ball of the capacitor should via down directly to the 3.3 V power plane. The via should be as close to the capacitor pad as possible, within 25 mils, with as thick a trace as possible.

For low-frequency decoupling, one 22 µF capacitor at the MCH is recommended. See Figure 5-21 for a placement example.

Figure 5-21. MCH V_{CCSM} Decoupling Example



5.5 Compensation

A system memory compensation resistor, SMRCOMP is used by the MCH to adjust buffer characteristics for specific board and environment variables. This is a 20 Ω 1% resistor to ground placed near the MCH. This trace should be routed a maximum of 0.5 inch at a minimum of 10 mils wide. Keep this trace a minimum of 7 mils away from other signals.

5.6 System Memory Reference Voltage

The SDREF signals are to be tied to a resistor divider network capable of supplying at least 10 mA of current. The output of this voltage divider is ½ V_{CCSM}. Use 1% resistors and decouple with one, 0.1 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches in length and a minimum of 12 mils wide. Keep this trace a minimum of 10 mils away from other signals.

5.7 DQM Signals

The 845 chipset does not support data masking. The DQM[7:0] pins on the DIMMs should be tied to ground.

5.8 Signal Mapping

Table 5-14 and Table 5-15 list both the necessary package trace lengths, and the signal mapping for the SCK, SCS#, and SCKE signals.

Table 5-14. SCK[11:0] DIMM Mapping and MCH Package Trace Lengths

Clock	DIMM	DIMM Pin	Package Trace Length (inches)
SCK0	0	42	0.404
SCK1	0	125	0.353
SCK2	0	79	0.865
SCK3	0	163	0.893
SCK4	1	42	0.371
SCK5	1	125	0.349
SCK6	1	79	0.814
SCK7	1	163	0.821
SCK8	2	42	0.483
SCK9	2	125	0.432
SCK10	2	79	0.589
SCK11	2	163	0.689

NOTE: DIMM0 is closest to the MCH and DIMM2 is furthest from the MCH.

Table 5-15. SCS#, SCKE DIMM Mapping

Signal	DIMM	DIMM Pin
SCS0#	0	30
SCS1#	0	114
SCS2#	0	45
SCS3#	0	129
SCS4#	1	30
SCS5#	1	114
SCS6#	1	45
SCS7#	1	129
SCS8#	2	30
SCS9#	2	114
SCS10#	2	45
SCS11#	2	129
SCKE0	0	128
SCKE1	0	63
SCKE2	1	128
SCKE3	1	63
SCKE4	2	128
SCKE5	2	63

NOTE: DIMM0 is closest to the MCH and DIMM2 is farthest from the MCH.

6 AGP Interface Design Guidelines

For detailed AGP Interface functionality (protocols, rules, signaling mechanisms, etc.) refer to the *AGP Interface Specification, Version. 2.0*, which is located at: http://www.agpforum.org.

This design guide focuses only on specific 845 chipset-based platform recommendations.

The *AGP Interface Specification, Version. 2.0* enhances the functionality of the original *AGP Interface Specification, Revision. 1.0* by allowing 4X data transfers and 1.5 V operation. In addition to these enhancements, additional performance enhancement and clarifications, such as fast write capability, are featured in the *AGP Interface Specification, Version. 2.0*. The 845 chipset supports these enhanced features and 1.5 V signaling only.

The 4X mode of operation on the AGP interface provides for "quad-sampling" of the AGP address/data and sideband address buses. This means data is sampled four times during each 66 MHz AGP clock cycle, or each data cycle is ¼ of 15 ns or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X mode, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5 ns. These high-speed data transfers are accomplished using source synchronous data strobing for 2X mode, and differential source synchronous data strobing for 4X mode.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, it is important to minimize noise and propagation delay mismatch. Noise on the data lines will cause the settling time to be high. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled.

The AGP signals are broken into three groups: 1X timing domain, 2X/4X timing domain, and miscellaneous signals. In addition, the 2X/4X timing domain signals are divided into three sets of signals (#1–#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are applicable only between the 2X/4X timing domain signal sets.

Table 6-1. AGP 2.0 Signal Groups

1X Timing Domain	2X/4X Timing Domain	Miscellaneous Signals
AGPCLK PIPE# RBF# WBF# ST[2:0] G_FRAME# G_IRDY# G_TRDY# G_STOP# G_DEVSEL# G_REQ# G_GNT# G_PAR	**SET 1** G_AD[15:0] G_C/BE[1:0]# AD_STB0 AD_STB0# **SET 2** G_AD[31:16] G_C/BE[3:2]# AD_STB1 AD_STB1# **SET 3** SBA[7:0] SB_STB SB_STB#	USB+ USB- OVRCNT# PME# TYPDET# PERR# SERR# INTA# INTB#

Strobe signals are not used in the 1X AGP mode. In 2X AGP mode, G_AD[15:0] and G_C/BE[1:0]# are associated with AD_STB0, G_AD[31:16] and G_C/BE[3:2]# are associated with AD_STB1, and SBA[7:0] is associated with SB_STB. In 4X AGP mode, G_AD[15:0] and G_C/BE[1:0]# are associated with AD_STB0 and AD_STB0#, G_AD[31:16] and G_C/BE[3:2]# are associated with AD_STB1 and AD_STB1#, and SBA[7:0] is associated with SB_STB and SB_STB#.

6.1 AGP Routing Guidelines

The following section documents the recommended routing guidelines for 845 chipset-based designs. All aspects of the interface will be covered from signal trace length to decoupling. These trace length guidelines apply to **all** of the signals listed as 2X/4X timing domain signals. These signals should be routed using 5-mil traces for a 60 Ω impedance, using the stack-up described in Figure 3-2.

These guidelines are not intended to replace thorough system simulations and validation. These guidelines are subject to change as simulation data is gathered.

6.1.1 1X Timing Domain Signal Routing Guidelines

The 1X signals should adhere to the follow routing guidelines:

- All 1X timing domain signal maximum trace lengths are 7.5 inches.
- 1X timing domain signals can be routed with 5 mil minimum trace separation.
- There are no trace length matching requirements for 1X timing domain signals.

6.1.2 2X/4X Timing Domain Signal Routing Guidelines

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 inches) and the long AGP interfaces (e.g., > 6 inches and < 7.25 inches) are documented separately. The maximum length allowed for the AGP interface is 7.25 inches.

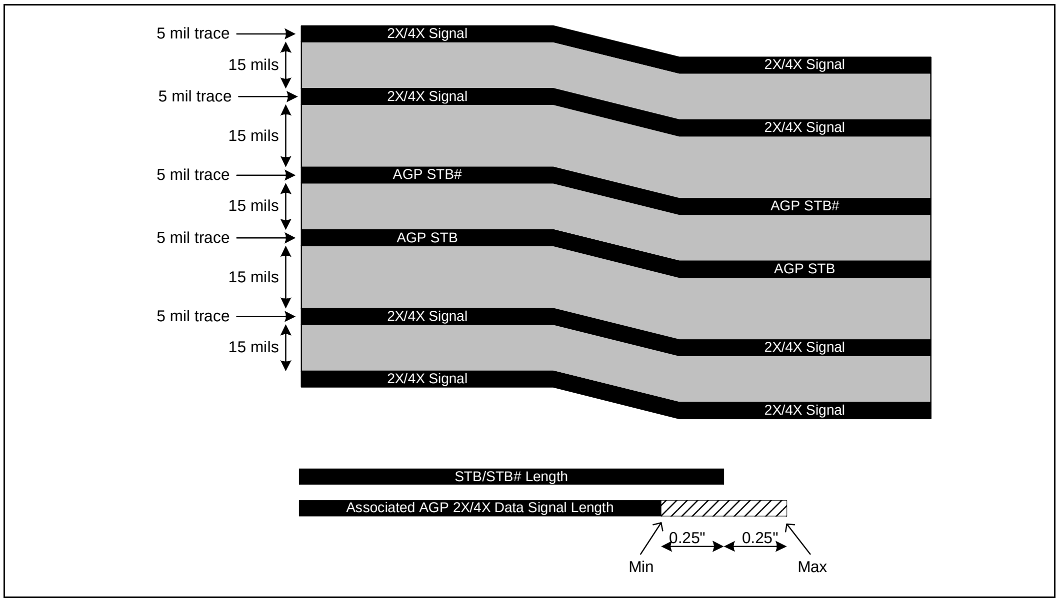
6.1.2.1 Trace Lengths Less Than 6 Inches

If the AGP interface is less than 6 inches with 60 Ω ±15% board impedance, at least 5-mil traces with at least 15 mils of space (1:3) between signals is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ± 0.25 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated with those strobe signals (e.g., G_AD[15:0] and G_C/BE[3:0]#), can be 5.05 inches to 5.55 inches long. While another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long and the data signals associated to those strobe signals (e.g., SBA[7:0]) can be 3.95 inches to 4.45 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface. Special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from all other signals by at least 15 mils. The strobe pair must be length matched to less than ± 0.1 inch (that is, a strobe and its compliment must be the same length within 0.1 inch).

Figure 6-1. AGP 2X/4X Routing Example for Interfaces Less Than 6 Inches



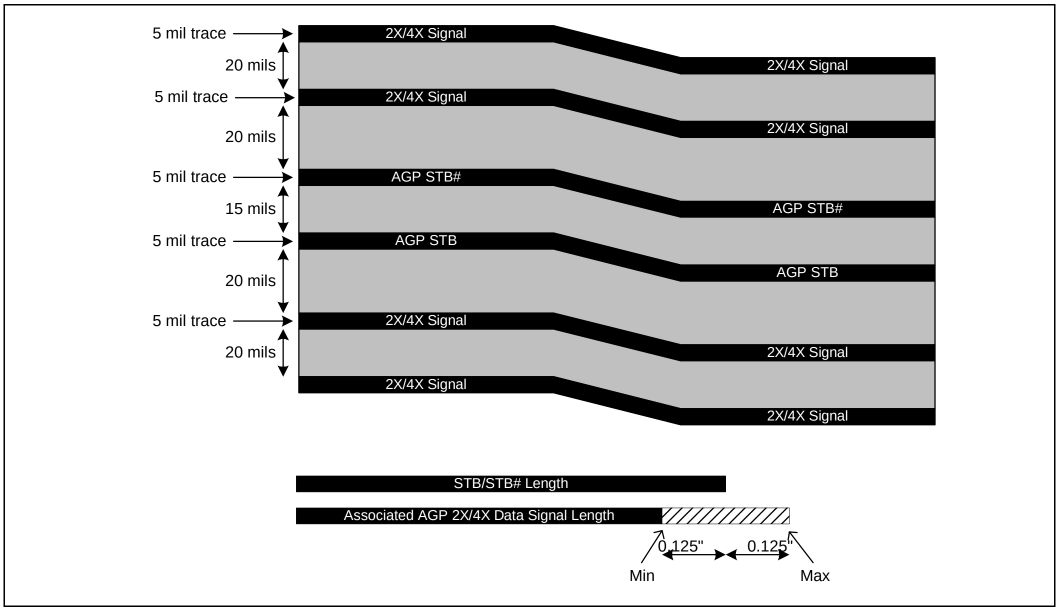
6.1.2.2 Trace Lengths Greater Than 6 Inches and Less Than 7.25 Inches

If the AGP interface is greater than 6 inches and less than 7.25 inches with 60 Ω ± 15% board impedance then at least 5-mil traces with at least 20 mils of space (1:4) between signals is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ± 0.125 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5 inches long, the data signals that are associated with those strobe signals (e.g., G_AD[15:0] and G_C/BE[2:0]#), can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2 inches long, and the data signals that are associated with those strobe signals (e.g., SBA[7:0]), can be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface. Special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from all other signals by at least 20 mils. The strobe pair must be length matched to less than ± 0.1 inches (i.e., a strobe and its compliment must be the same length within 0.1 inches).

Figure 6-2. AGP 2X/4X Routing Example for Interfaces between 6 Inches and 7.25 Inches



6.1.3 AGP Interfaces Trace Length Summary

The 2X/4X Timing Domain Signals can be routed with 5-mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.15 inch of the MCH package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

Table 6-2. AGP 2.0 Routing Summary

Signal	Maximum Length	Trace Spacing (5-mil traces)	Length Mismatch	Relative To
1X Timing Domain	7.5 inches	5 mils	No requirement	N/A
2X/4X Timing Domain Set 1	7.25 inches	20 mils	± 0.125 inches	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set 2	7.25 inches	20 mils	± 0.125 inches	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set 3	7.25 inches	20 mils	± 0.125 inches	SB_STB and SB_STB#
2X/4X Timing Domain Set 1	6 inches	15 mils	± 0.25 inches	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set 2	6 inches	15 mils	± 0.25 inches	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set 3	6 inches	15 mils	± 0.25 inches	SB_STB and SB_STB#

NOTES:

1. All trace widths are 5 mils.
2. Each strobe pair must be separated from other signals by at least 15 mils for signal maximum lengths of 6 inches, and at least 20 mils for signal maximum lengths of 7.25 inches
3. Strobe and strobe bar pairs must be separated from each other by 15 mils and must be the same length.
4. These guidelines apply to board stack-ups described in Section 3.

Table 6-3. AGP Signal Routing Guidelines

Parameter	Routing Guidelines
Breakout Guidelines	5-mil width with 5 mil-spacing for a max of 0.15 inch

6.1.4 Signal Power/Ground Referencing Recommendations

It is strongly recommended that signals do not change referencing. If a signal is power referenced it should stay referenced to power, and if it is referenced to ground it should stay referenced to ground. It is strongly recommended that AGP signals have a maximum of 1 via. All signals in a signal group should be routed on the same layer. If a signal is power referenced, it **must** stay referenced to power.

6.1.5 V_{DDQ} and TYPEDET#

AGP specifies two separate power planes: V_{CC} and V_{DDQ}. V_{CC} is the core power for the graphics controller and is always 3.3 V.V_{DDQ} is the interface voltage. The 845 chipset supports only an interface voltage of 1.5 V.

AGP Interface Specification, Version 2.0. requires V_{CC} and V_{DDQ} to be tied to separate power planes, and implements a TYPEDET# (type detect) signal on the AGP connector that determines the interface operating voltage (V_{DDQ}). Designs based on the 845 chipset do not require TYPEDET# detection because the 845 chipset supports 1.5 V AGP add-in cards. 3 V AGP add-in cards are not supported.

6.1.6 V_{REF} Generation

For 1.5 V add-in cards, the graphics controller and MCH generate AGP voltage reference V_{REF} and distribute it through the connector. Two signals have been defined on the 1.5 V connector to allow V_{REF} delivery:

- V_{REFGC}—V_{REF} from the graphics controller to the chipset
- V_{REFCG}—V_{REF} from the chipset to the graphics controller

However, the usage of the source generated V_{REFCG} at the MCH is not required per the *AGP Interface Specification, Version 2.0.* Given this and the fact that the MCH requires the presence of V_{REF} when an AGP add-in card is present and not present, the following circuit is recommended for V_{REF} generation.

The V_{REF} divider network should be placed near the AGP connector. The minimum trace spacing around the V_{REF} signal must be 25 mils to reduce crosstalk and maintain signal integrity, and a 0.1 µF bypass capacitor should be placed within 0.8 inches of the MCH AGPREF ball. V_{REF} voltage must be 0.5 x V_{DDQ} for 1.5 V operation.

Figure 6-3. AGP 2.0 V_{REF} Generation and Distribution for 1.5 V Cards

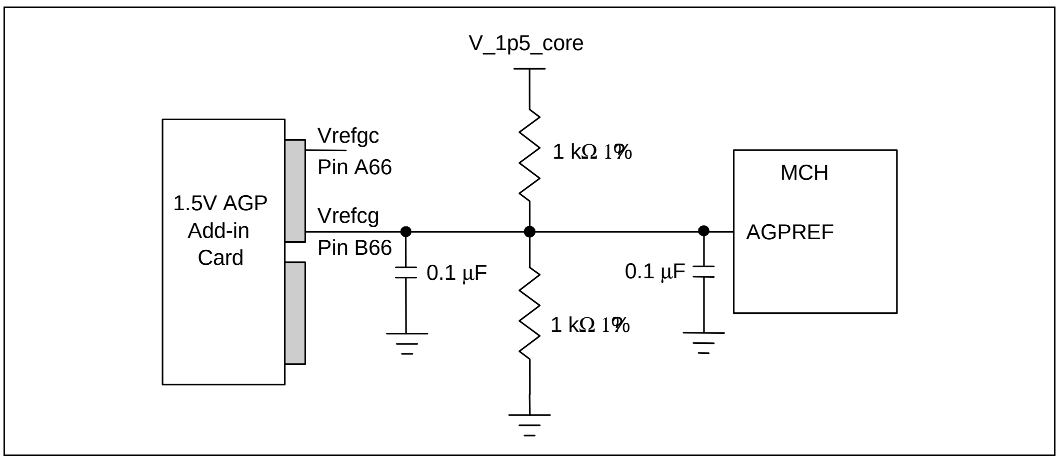


Table 6-4. AGP V_{REF} Routing Guidelines

Parameter	Routing Guidelines
AGP V_{REF} trace width	12 mils
AGP V_{REF} trace spacing to other signals	25 mils
AGP V_{REF} trace breakout guidelines	5 mil width with 5 mil spacing for a max of 0.15 inch
AGP V_{REF} decoupling—MCH max distance	0.8 inch

6.1.7 MCH AGP Interface Buffer Compensation

The MCH AGP interface supports resistive buffer compensation (GRCOMP). The GRCOMP signal must be tied to a 40 Ω 2% resistor to ground. This trace should be kept to 10 mils wide and less than 0.5 inch long.

AGP signals have integrated pull-up resistors to AGP V_{DDQ}, and pull-down resistors to ground. This is to ensure stable values are maintained when agents are not actively driving the bus. Table 6-5 lists signals that have integrated AGP pull-up/pull-down resistors. Their value is between 4 kΩ and 16 kΩ. External pull-ups and pull-downs are not needed for these signals.

Note: 1X mode, trace stub to pull-up resistor should be kept to less than 0.5 inch.
2X/4X mode, trace stub to pull-up resistor should be kept to less than 0.1 inch.

Short stub lengths help minimize signal reflections from the stub. The strobe signals require pull-up/pull-down on the motherboard to ensure stable values when there are no agents driving the bus.

Table 6-5. MCH AGP Signals with Integrated Pull-Up/Pull-Down Resistors

Signals	Pull-Up/Pull-Down
1X Timing Domain	
G_FRAME#	pull-up resistor to V_{CC1_5}
G_TRDY#	pull-up resistor to V_{CC1_5}
G_IRDY#	pull-up resistor to V_{CC1_5}
G_DEVSEL#	pull-up resistor to V_{CC1_5}
G_STOP#	pull-up resistor to V_{CC1_5}
RBF#	pull-up resistor to V_{CC1_5}
PIPE#	pull-up resistor to V_{CC1_5}
G_REQ#	pull-up resistor to V_{CC1_5}
WBF#	pull-up resistor to V_{CC1_5}
2X/4X Timing Domain	
AD_STB[1:0]	pull-up resistor to V_{DDQ}
SB_STB	pull-up resistor to V_{DDQ}
AD_STB[1:0]#	pull-down resistor to GND
SB_STB#	pull-down resistor to GND

6.1.8 MCH External AGP Pull-Up/Pull-Down Resistors

The MCH G_GNT# output signal is tri-stated during RSTIN# assertion. This signal must have an external 6.8 kΩ pull-up resistor to keep it from floating during the RSTIN# assertion.

Note: The G_GNT# signals require pull-up resistor to the MCH's V_{CC1_5}.

The MCH ST1 signal needs a site for an external pull-down resistor to ground. This resistor should not be populated, and is reserved for future use.

The MCH AGP ST0 signal is sampled by the MCH at power-on to configure MCH system memory mode. An internal MCH pull-up resistor on this signal sets the default system memory mode to PC133 SDRAM.

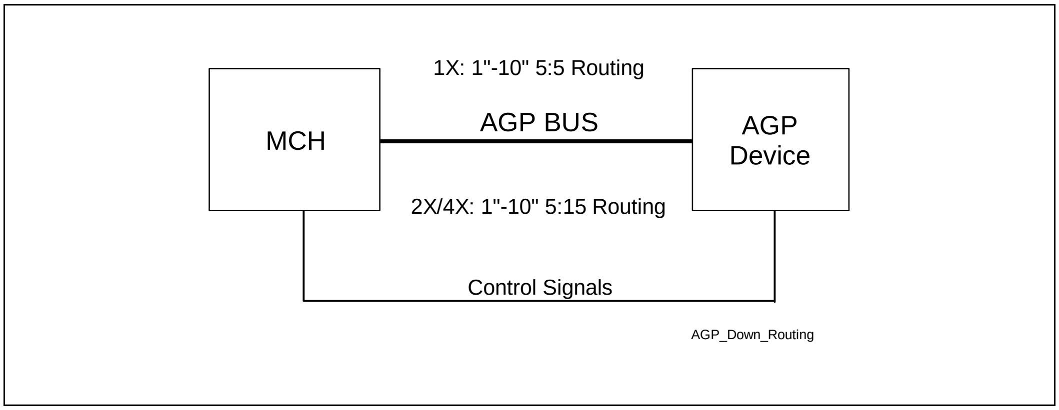
Table 6-6. MCH AGP Signals Requiring External Pull-Up/Pull-Down Resistors

Signals	Pull-Up/Pull-Down
G_GNT#	6.8 kΩ pull-up resistor to V_{CC1_5}

6.1.9 AGP Device Down Routing Guidelines

Routing guidelines for the AGP device "down" option are very similar to those used when routing to an AGP connector. For any routing/layout information that is not included in this section of design guidelines, refer to the AGP up routing/layout guidelines in this chapter. Figure 6-4 shows the on-board AGP layout.

Figure 6-4. AGP Device Down Routing Guidelines



6.1.9.1 1X Timing Domain Signal Routing Guidelines

The 1X signals should adhere to the follow routing guidelines:

- All 1X timing domain signals have a maximum trace length of 10 inches.
- 1X timing domain signals can be routed with 5-mil minimum trace separation.
- 1X timing domain signals can be routed with 5 mil minimum trace width.
- There are no trace length matching requirements for 1X timing domain signals.

In all cases it is best to reduce the line length mismatch where possible to insure added margin. It is also best to separate the traces by as much as possible to reduce the amount of trace-to-trace coupling.

Table 6-7. 1X Timing Domain Trace Length Recommendations for AGP Device Down

Width: Space	Trace	Line Length	Line Length Matching
5:5	Control	1.0 in < line length < 10 in	Not required

6.1.9.2 2X/4X Timing Domain Signal Routing Guidelines

The 2X/4X signals should adhere to the follow routing guidelines:

- All 2X/4X timing domain signals have a maximum trace length of 10 inches.
- 2X/4X timing domain signals can be routed with 15-mil minimum trace separation.
- 2X/4X timing domain signals can be routed with 5-mil minimum trace width.

Table 6-8. 2X/4X Timing Domain Trace Length Recommendations for AGP Device Down

Width:Space	Trace	Line Length	Line Length Matching
5:15	Data/Strobe	1.0 in < line length < 10 in	Refer to Section 6.1.2.2

Some of the signals require pull-up or pull-down resistors to be installed on the motherboard. Refer to Table 6-6 for a list of these signals.

6.1.10 AGP Connector

The 845 chipset supports only 1.5 V add-in cards. A 1.5 V AGP card uses the AGP 3 V connector and rotates it 180 degrees on the planar. Therefore, the key of the connector moves to the opposite side of the planar away from the I/O panel and will not allow 3 V add-in cards. A 1.5 V AGP Pro50* connector is an extension of the AGP connector. It has additional power and ground pins at each end of the connector and is back compatible with a 1.5 V AGP card. Intel recommends a 1.5 V AGP Pro50* connector for workstations, and a 1.5 V AGP connector for desktop systems.

The designer should ensure that the AGP connector is well decoupled as described in revision 1.0 of the *AGP Design Guide*, Section 1.5.3.3 (i.e., use a 0.01 µF capacitor for each power pin, a bulk 10 µF tantalum capacitor on V_{DDQ}, and 20 µF tantalum capacitor on V_{CC3_3} plane near the connector.).

6.1.11 AGP Connector Decoupling Guidelines

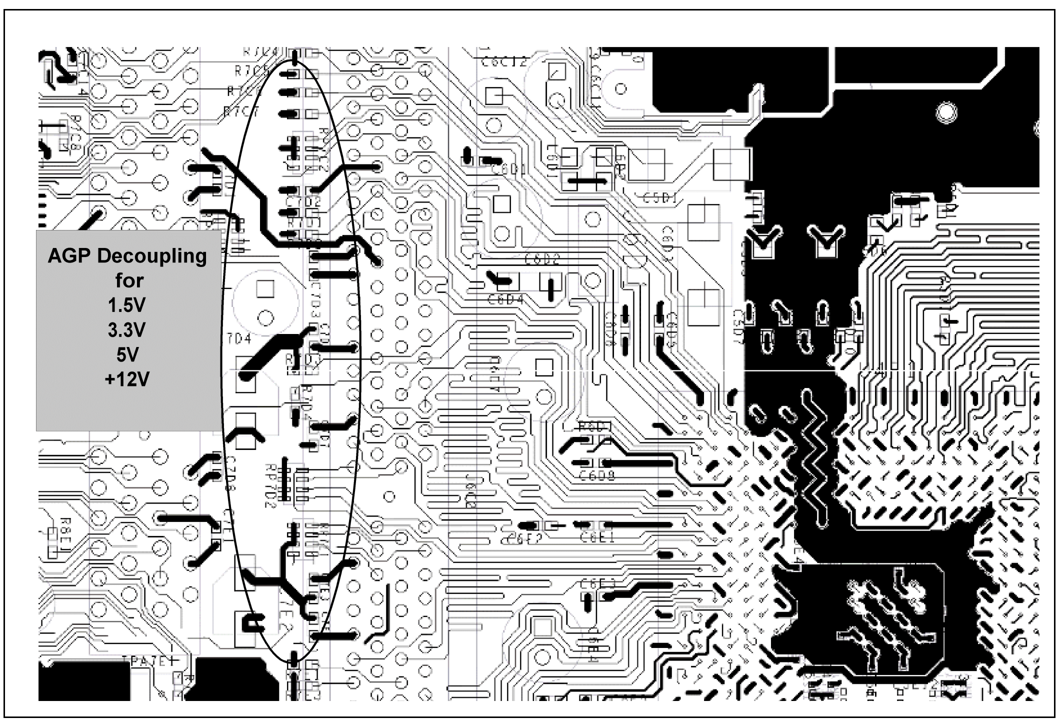
The following decoupling is suggested for decoupling the 1.5 V power plane at the AGP connector. Figure 6-5 shows the general location of AGP decoupling capacitors on layer 1. Actual component placement will depend upon how the 1.5 V, 3.3 V, 5 V, and +12 V power planes are split on layer 2.

Table 6-9. 1.5 V Decoupling at the AGP Connector

Voltage	Number of Capacitors	Component
1.5 V	6	0.1 µF ceramic capacitor, 603 body type, X7R dielectric
3.3 V	3	0.1 µF ceramic capacitor, 603 body type, X7R dielectric
	1	22 µF electrolytic capacitor
	1	100 µF electrolytic capacitor
5 V	1	0.1 µF ceramic capacitor, 603 body type, X7R dielectric
	1	10 µF aluminum electrolytic capacitor
12 V	1	0.1 µF ceramic capacitor, 603 body type, X7R dielectric

The designer should ensure that the AGP connector is well decoupled as described in revision 1.0 of the *AGP Design Guide*, Section 1.5.3.3.

Figure 6-5. AGP Decoupling on Layer 1



6.1.12 AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that, without proper retention, AGP cards may become unseated during system shipping and handling. To prevent the disengagement of AGP cards, Intel recommends that AGP-based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket used to properly locate the card with respect to the chassis, and to assist with card retention. The AGP RM is available in two different handle orientations: left-handed (Figure 6-6), and right-handed. Most system boards accommodate the left-handed AGP RM. Because the manufacturing capacity is greater for the left-handed RM, Intel recommends that customers design into their systems the left-handed AGP RM. The right-handed AGP RM is identical to the left-handed AGP RM except for the position of the actuation handle, which is located on the same end as in the primary design but extends from the opposite side, parallel to the longitudinal axis of the part. Figure 6-7 details the keep-out information for the left-handed AGP RM. Use this information to ensure that motherboard designs leave adequate space for RM installation.

The AGP interconnect design requires that the AGP card be retained to limit card back out within the AGP connector to 0.99 mm (0.039 inch) maximum. For this reason, new cards should have an additional mechanical keying tab notch that provides an anchor point on the AGP card for interfacing with the AGP RM. The RM’s round peg engages with the AGP card’s retention tab, thereby preventing the card from disengaging during dynamic loading. The additional notch in the mechanical keying tab is required for 1.5 V AGP cards, and is recommended for the new 3.3 V AGP cards.

Figure 6-6. AGP Left-Handed Retention Mechanism

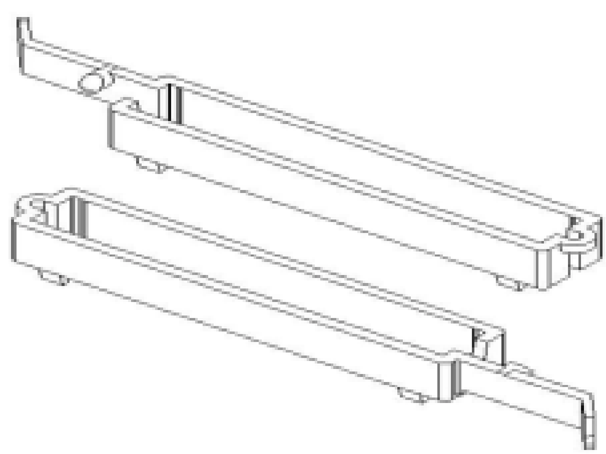
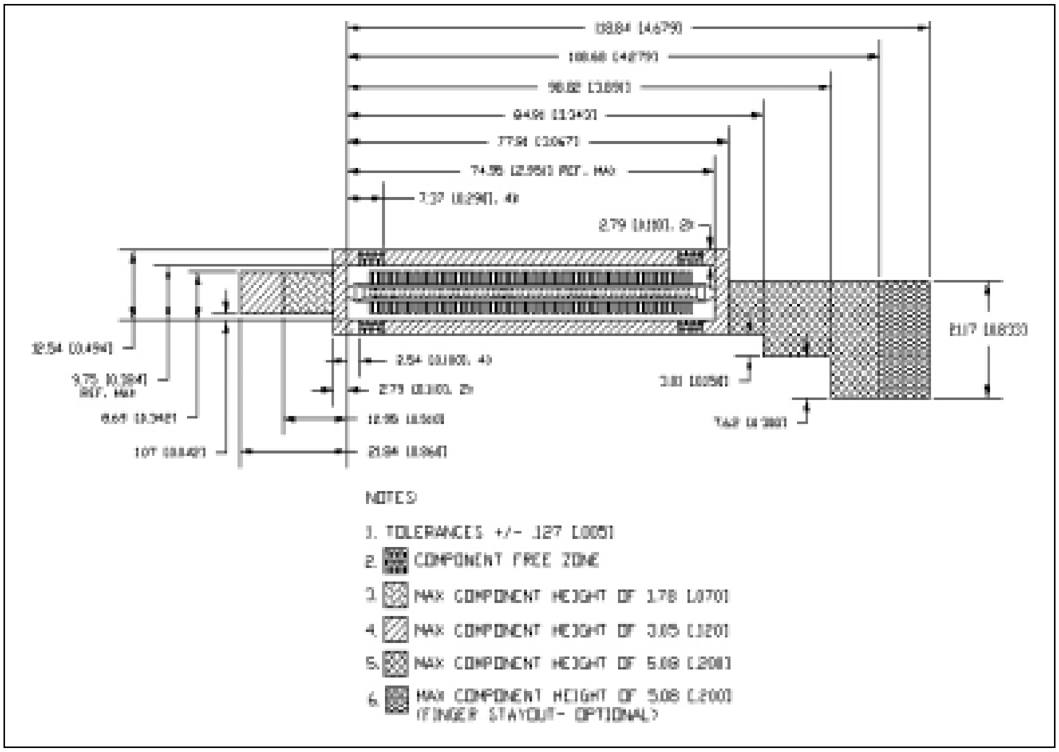


Figure 6-7. Left-Handed RM Keep-Out Information



Recommended for all AGP cards, the AGP RM is detailed in Engineering Change Request No. 48 (ECR #48), which details approved changes to the *Accelerated Graphics Port Interface Specification*, *Version 2.0*. Intel intends to incorporate the AGP RM changes into later revisions of the AGP interface specification. In addition, Intel has defined a reference design for a mechanical device utilizing the features defined in ECR #48.

ECR #48 can be viewed on the Intel Web site at:http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors:

Resin Color	Supplier	Part Number	
		Left-Handed Orientation (Preferred)	Right-Handed Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

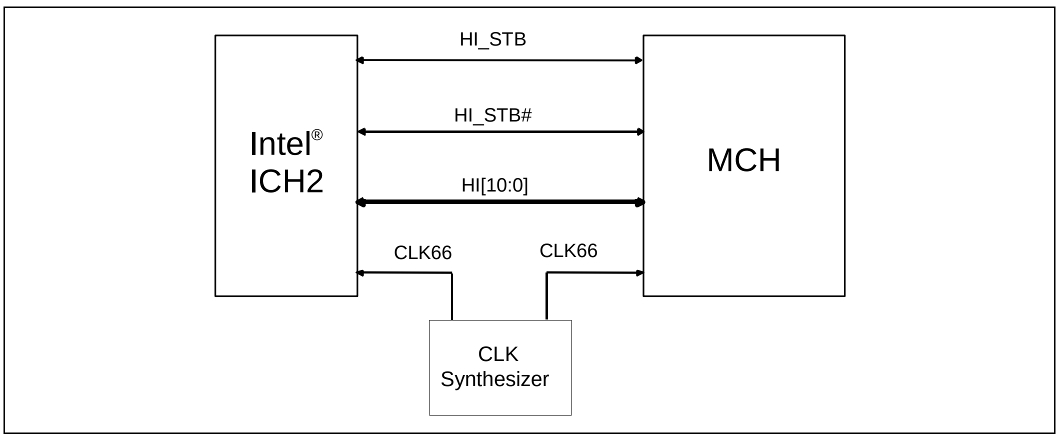
7 Hub Interface

The MCH and ICH2 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the Hub Interface signals be routed directly from the MCH to ICH2 with all signals referenced to V_{SS}. Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net, and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: data signals (HI), and strobe signals (HI_STB). For the 8-bit Hub Interface, HI[7:0] are associated with HI_STB and HI_STB#.

No pull-ups or pull-downs are required on the hub interface. HI11 on the ICH2 should be brought out to a test point for NAND Tree testing.

Figure 7-1. Bit Hub Interface Routing Example



7.1 8-Bit Hub Interface Routing Guidelines

This section documents the routing guidelines for the hub interface. This hub interface connects the ICH2 to the MCH. The trace impedance must equal 60 Ω ± 15%.

7.1.1 8-Bit Hub Interface Data Signals

The 8-bit hub interface data signal traces should be routed 5 mils wide with a minimum trace spacing of 15 mils (5 on 15). To break out of the MCH and ICH2 package, the hub interface data signals can be routed 5 on 5, and must be separated to 5 on 15 within 300 mils of the package.

The maximum hub interface data signal trace length is 8 inches. Each data signal must be matched within ± 0.1 inch of the HI_STB differential pair. There is no explicit matching requirement between the individual data signals.

7.1.2 8-Bit Hub Interface Strobe Signals

The 8-bit hub interface strobe signals should be routed 5-mils wide with a minimum trace spacing of 15 mils (5 on 15). This strobe pair should have a minimum of 15-mil spacing from any adjacent signals. The maximum length for the strobe signals is 8 inches. Each strobe signal must be the same length, and each data signal must be matched within ± 0.1 inch of the strobe signals.

7.1.3 8-Bit Hub Interface HI_REF Generation/Distribution

HI_REF is the hub interface reference voltage. The HI_REF voltage requirement must be set appropriately for proper operation. See Table 7-1 for the HI_REF voltage specifications and the associated resistor recommendations for the voltage divider circuit.

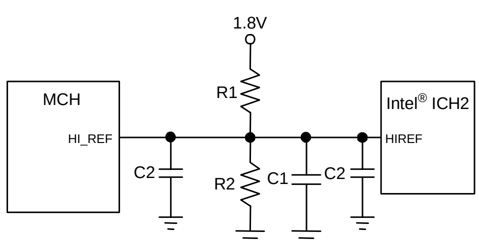
Table 7-1. HI_REF Generation Circuit Specifications

HI_REF Voltage Specification (V)	Recommended Resistor Values for the HI_REF Divider Circuit (Ω)
½ V_{CC1_8} ± 2%	R1 = R2 = 150 ± 1%

The HI_REF divider should not be located more than 4 inches from either the MCH or the ICH2. The reference divider circuit should be bypassed to ground at each component with a 0.1 µF capacitor (C2) located within 0.25 inches of the HI_REF pin.

The resistor values, R1 and R2, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the following figure) should be placed close to R1 and R2. Figure 7-2 shows an example HI_REF divider circuit.

Figure 7-2. Hub Interface with Reference Divider Circuit



7.1.4 8-Bit Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

Table 7-2. RCOMP Resistor Values

Component	RCOMP Resistor Value	RCOMP Resistor Tied to
ICH2	40.2 Ω $\pm$ 1%	V_{CC1_8}
MCH	40.2 Ω $\pm$ 2%	V_{CC1_8}

7.1.5 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors within 150 mils of the ICH2. The MCH should be decoupled with one 0.1 µF within 150 mils of the package, and one 10 µF capacitor nearby. All capacitors should be adjacent to the rows that contain the hub interface.

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8 Intel® I/O Controller Hub 2 (ICH 2)

8.1 IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH2 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Additional series terminations are not anticipated, but OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inch shorter than the longest IDE signal (on that channel).

8.1.1 Cabling

- **Length of cable**: Each IDE cable must be equal to or less than 18 inches.
- **Capacitance**: Less than 30 pF.
- **Placement**: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- **Grounding**: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH2 Placement**: The ICH2 must be placed equal to or less than 8 inches from the ATA connector(s).

8.1.1.1 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5. The ICH2 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

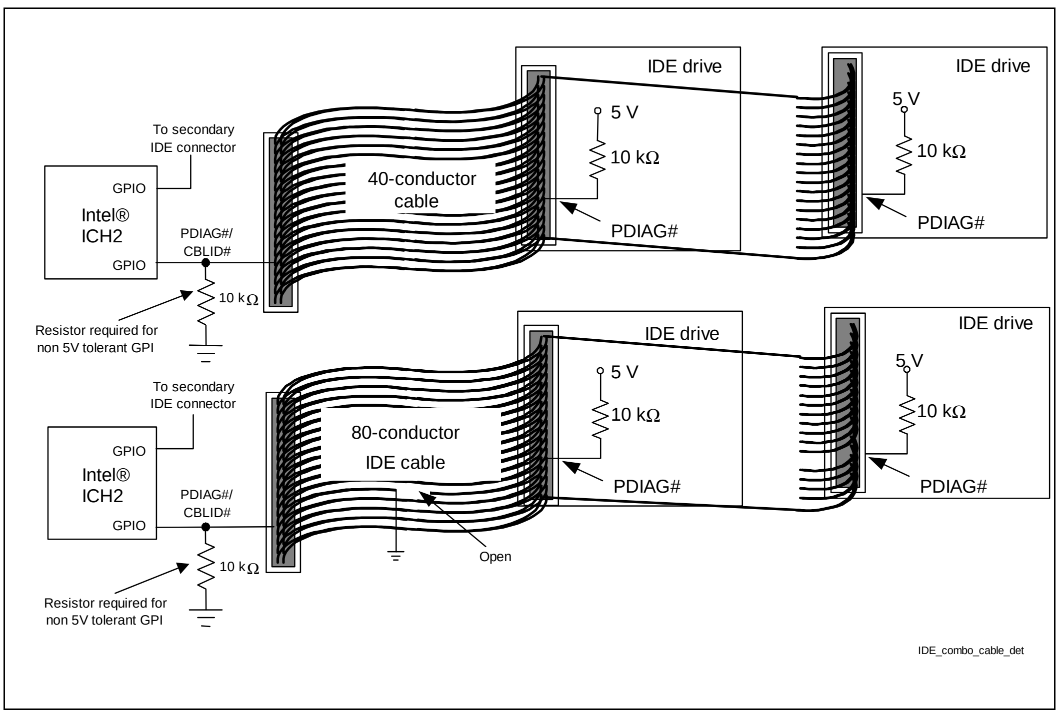
To determine if ATA/66 or ATA/100 mode can be enabled, the ICH2 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

8.1.1.2 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 8-1. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all of the GPI and GPIO pins on the ICH2 are 5 V tolerant. If non-5 V tolerant inputs are used, a resistor divider is required to prevent 5 V on the ICH2 or Intel FWH pins. This resistor also prevents the GPI pins from floating if a device is not present on the IDE interface. The proper value of the divider resistor is 10 kΩ (as shown in Figure 8-1).

Figure 8-1. Combination Host-Side/Device-Side IDE Cable Detection

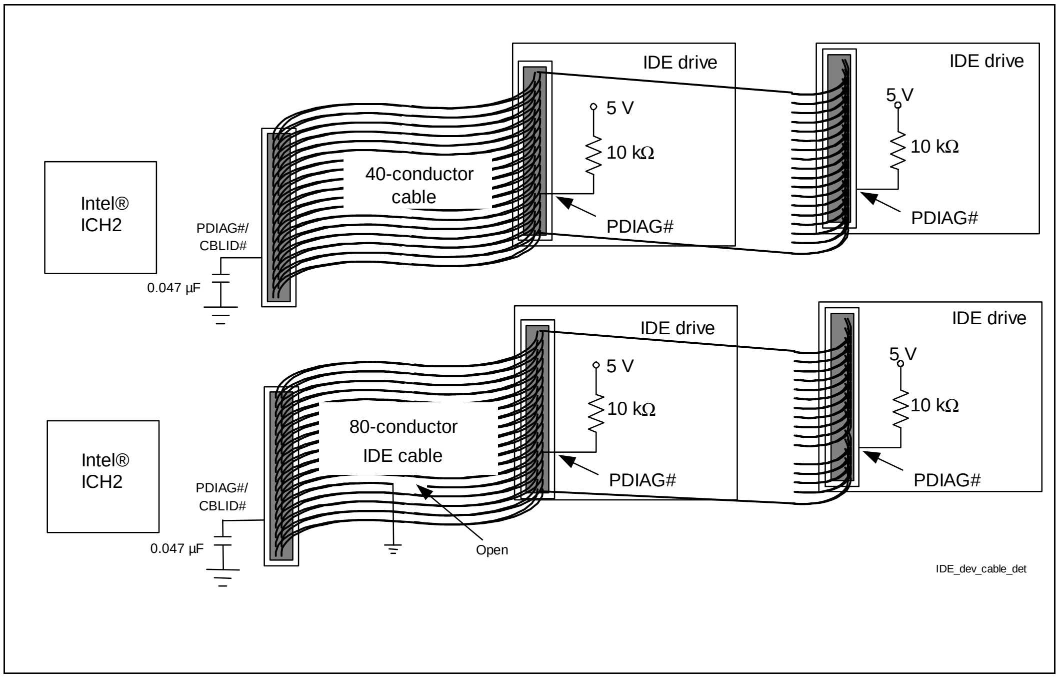


This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, there is 40-conductor cable in the system, and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and notify the user of the problem.

8.1.1.3 Device-Side Cable Detection

Figure 8-2. Device Side IDE Cable Detection

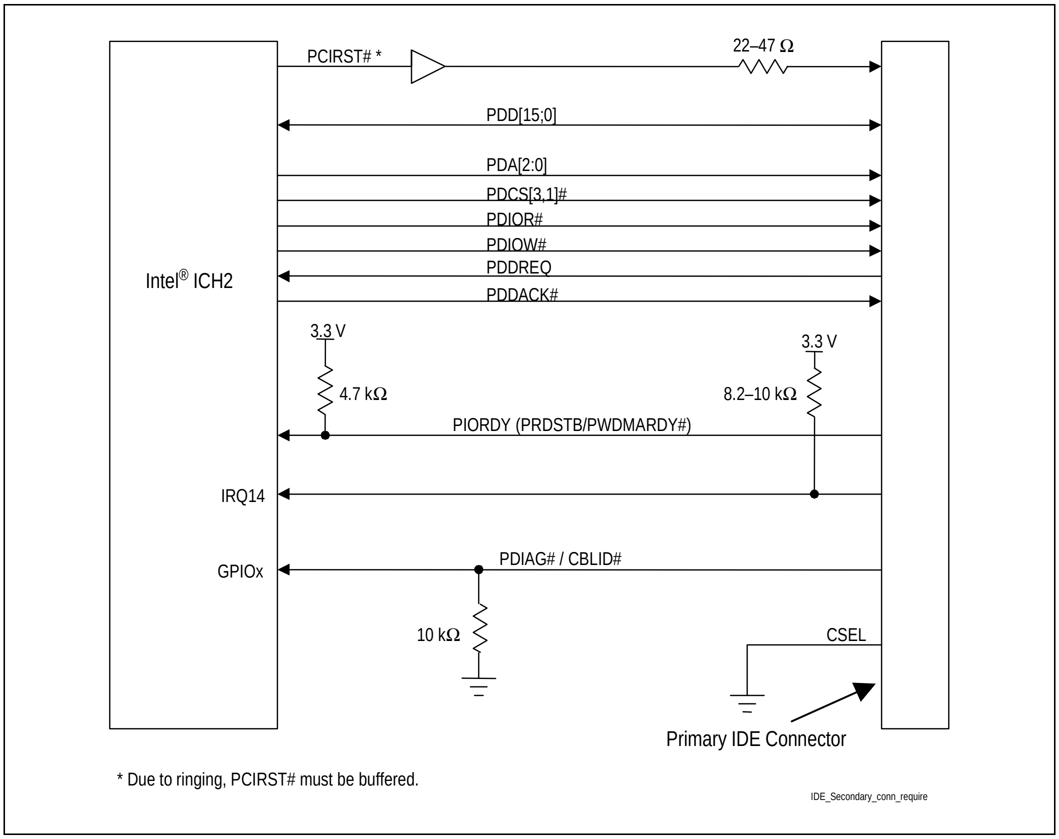


For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 8-2. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above.

This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4, or 5 drive will drive PDIAG#/CBLID# low, and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host; therefore, the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

8.1.2 Primary IDE Connector Requirements

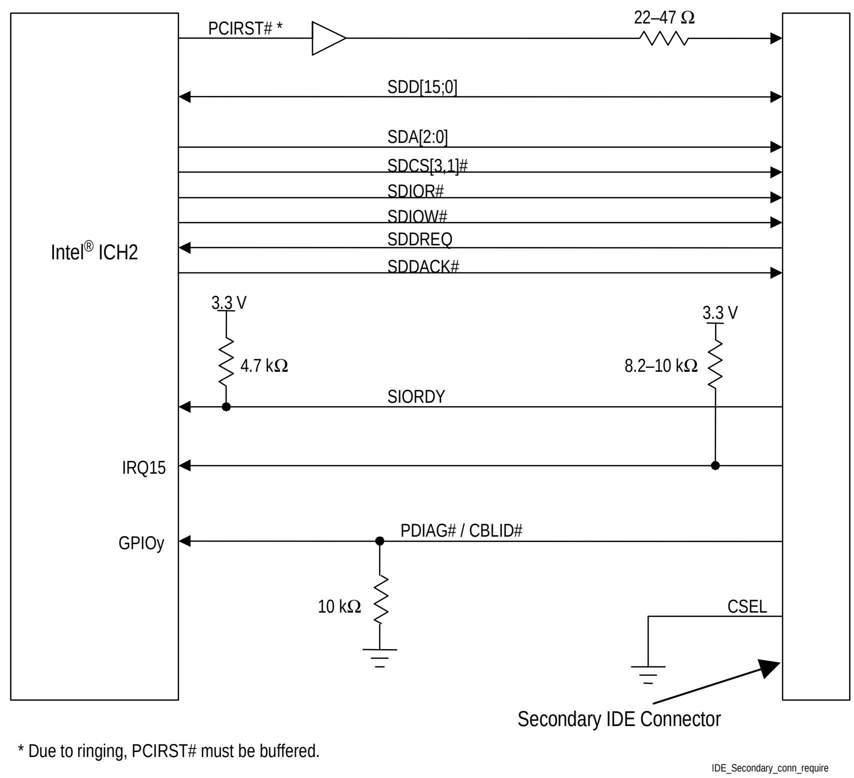
Figure 8-3. Connection Requirements for Primary IDE Connector



- A 22 Ω–47 Ω series resistor is required on PCIRST#. The correct value should be determined for each unique motherboard design based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to V_{CC3}.
- A 4.7 kΩ pull-up resistor to V_{CC3} is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the primary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

8.1.3 Secondary IDE Connector Requirements

Figure 8-4. Connection Requirements for Secondary IDE Connector



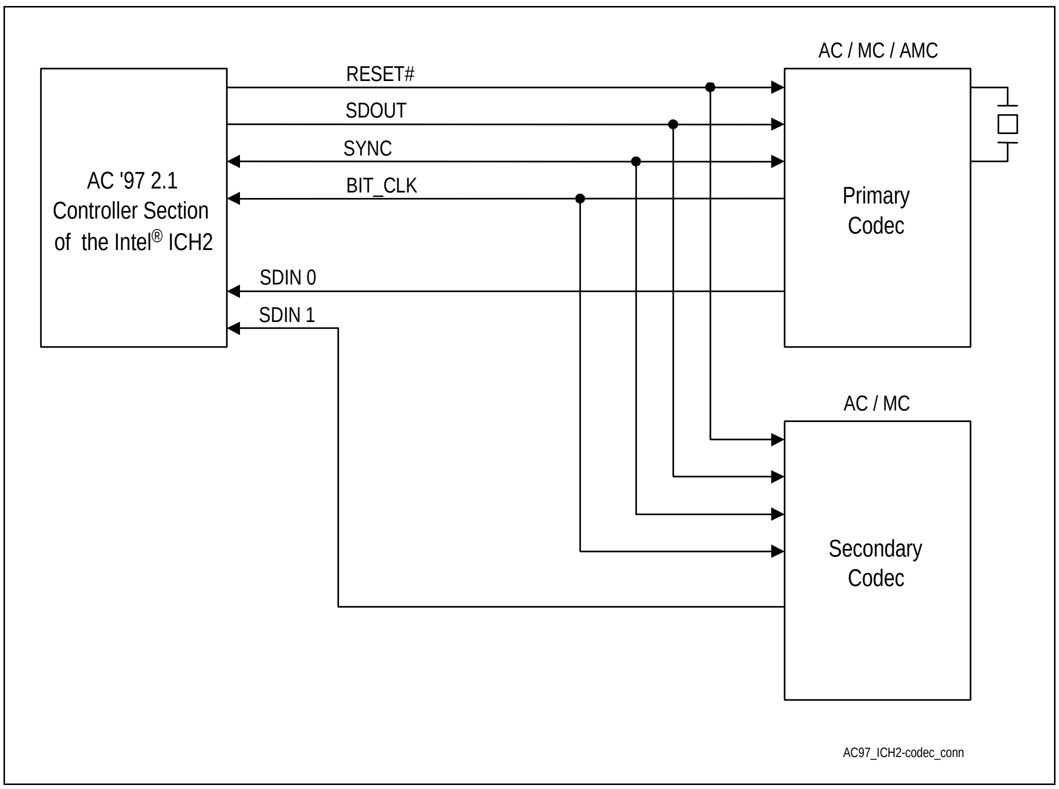
- 22 Ω–47 Ω series resistors are required on PCIRST#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to V_{CC3}.
- A 4.7 kΩ pull-up resistor to V_{CC3} is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the secondary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

8.2 AC ’97

The ICH2 implements an AC ’97, version 2.1 compliant digital controller. Any codec attached to the ICH2 AC-link must be AC ’97 2.1 compliant as well. The AC ’97 2.1 specification is on the Intel website: http://developer.intel.com/ial/scalableplatforms/audio/index.htm

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. Figure 8-5 shows a two codec topology of the AC-link for the ICH2.

Figure 8-5. Intel® ICH2 AC ’97—Codec Connection



The AC ’97 interface can be routed using 5-mil traces with 5-mil spaces between the traces. Maximum length between the ICH2 and CODEC/CNR is 14 inches in a T topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC-link. Trace impedance should be Z0 = 60 Ω ± 15%.

Clocking is provided from the primary codec on the link via AC_BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2), and any other codec present. This clock is used as the time base for latching and driving data.

The ICH2 supports wake on ring from S1–S5 via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are enabled only when the AC-Link Shut Off bit in the ICH2 is set. This keeps the link from floating when the AC-link is off or when there are no codecs present.

The Shut-off bit not set indicates that there is a codec on the link. Therefore, AC_BITCLK and AC_SDOUT will be driven by the codec and ICH2, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec. If there is one or no CODEC onboard, the unused AC_SDINx pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

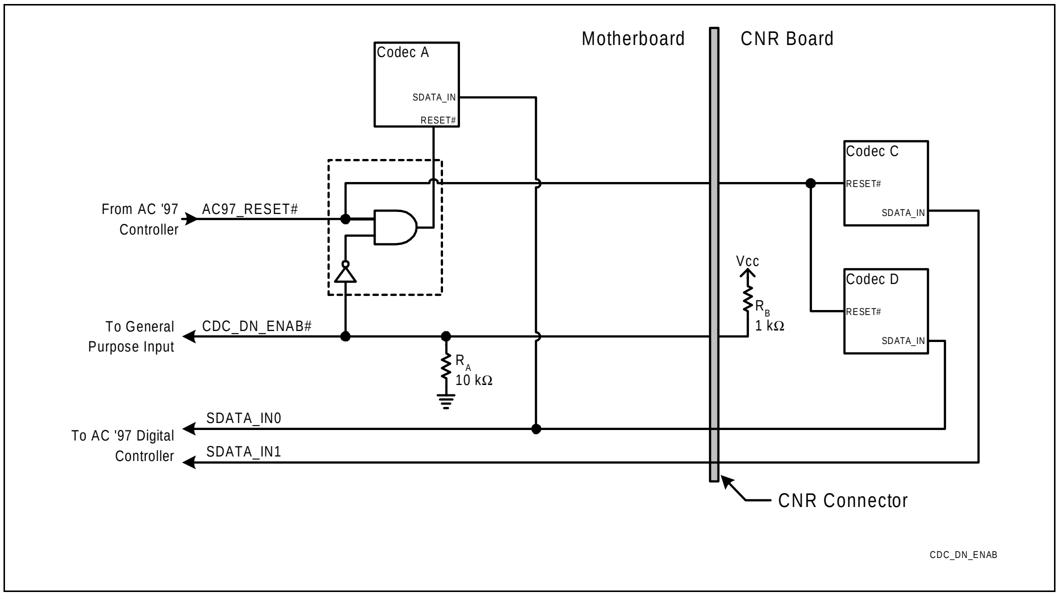
8.2.1 AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to Intel’s White Paper Recommendations for ICHx/AC ’97 Audio (Motherboard and Communication and Network Riser) for Intel’s recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration in which two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC ’97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 8-6 through Figure 8-9) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration, and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 8-6. CDC_DN_ENAB# Support Circuitry for a Single Codec Motherboard



As shown in Figure 8-6, when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented on the motherboard. This circuitry is required to disable the motherboard codec when a CNR is installed that contains two AC ’97 codecs (or a single AC ’97 codec that must be the primary codec on the AC-link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset), and the codec(s) on the CNR take control of the AC-link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 8-7 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 8-7 and Figure 8-8 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line to avoid conflict with the motherboard codec(s).

Figure 8-7. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

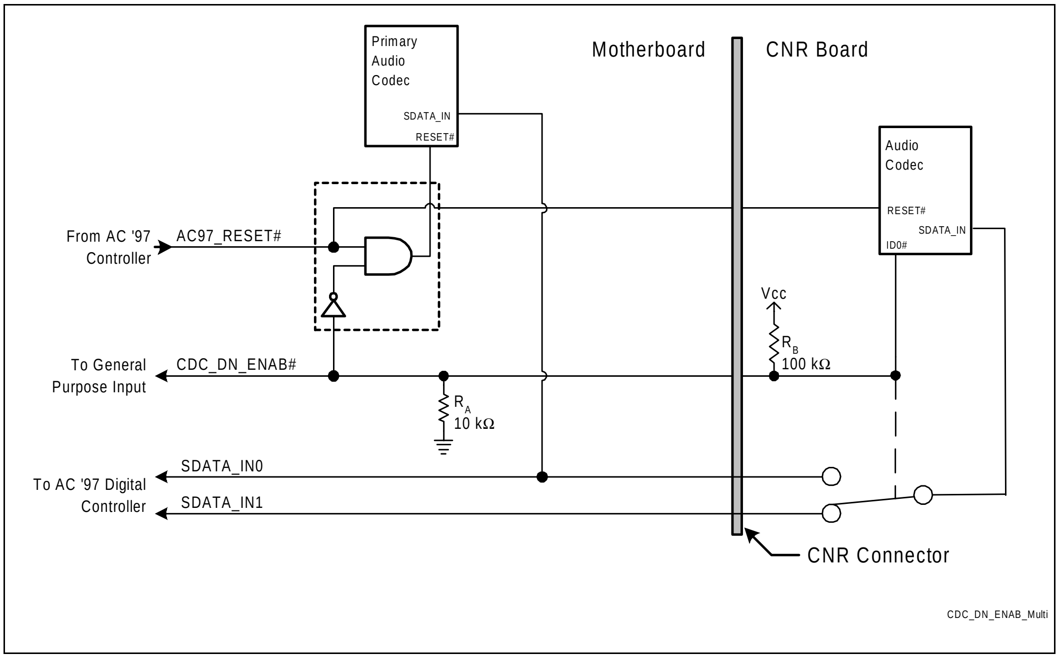


Figure 8-8 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration, the resistor R_B, has been changed to 100 kΩ.

Figure 8-8. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard/One-Codec on CNR

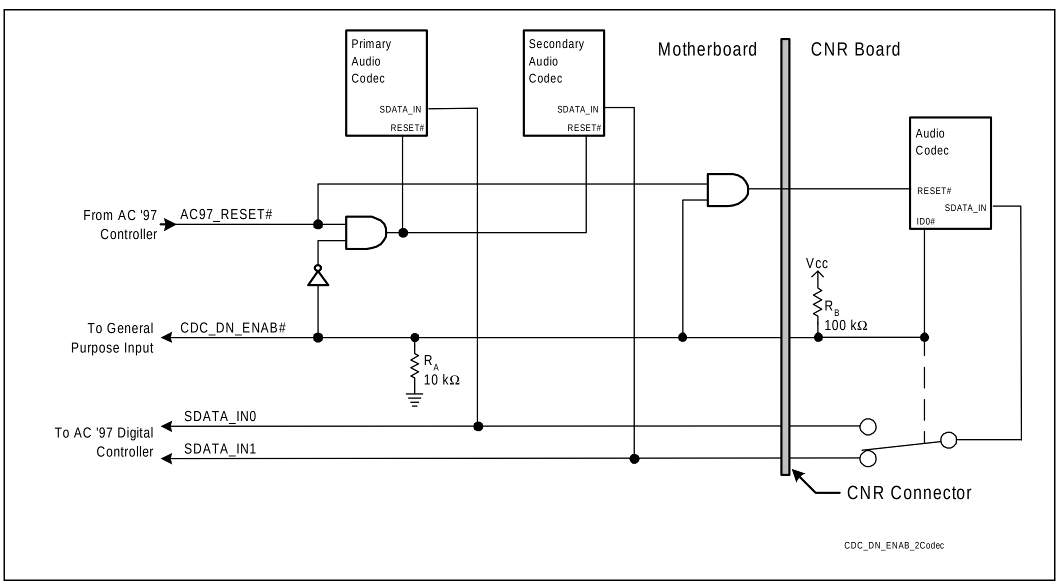
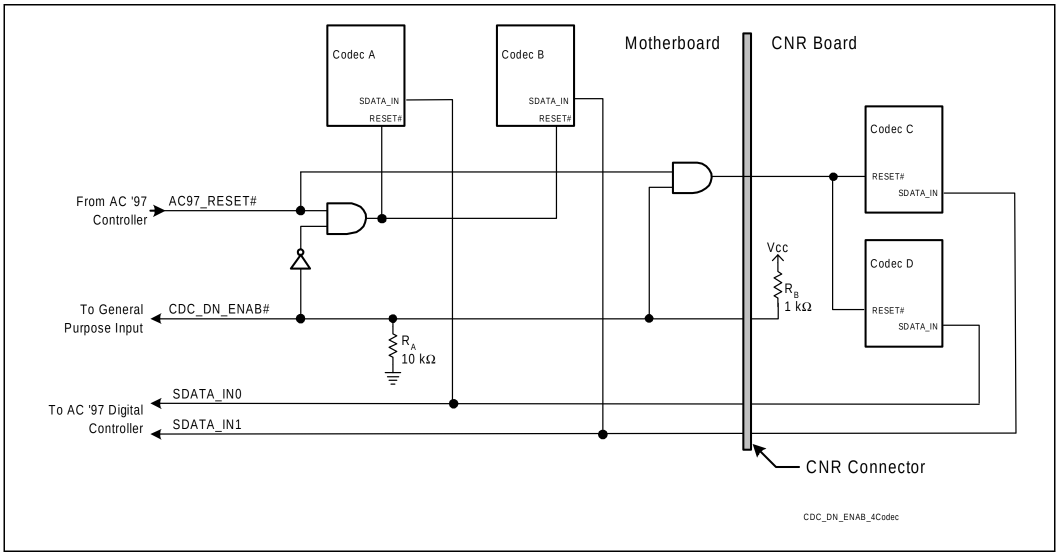


Figure 8-9 shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ

Figure 8-9. CDC_DN_ENAB# Support for Two-Codecs on Motherboard / Two-Codecs on CNR



NOTES:

1. While it is possible to disable down codecs as shown in Figure 8-6 through Figure 8-9, disabling is not recommended for reasons such as avoidance of shipping redundant and/or non-functional audio jacks, as well as reasons cited in the ICHx/AC '97 white paper.
2. All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement RB with value 1 kΩ. If there is one Codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
4. A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is required to be connected to a GPI; a connection to a GPIO is strongly recommended for testing purposes.

Table 8-1. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC '97 Digital Controller (ICH2).
SDATA_In*n*	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH2).

8.2.2 Valid Codec Configurations

Table 8-2. Codec Configurations

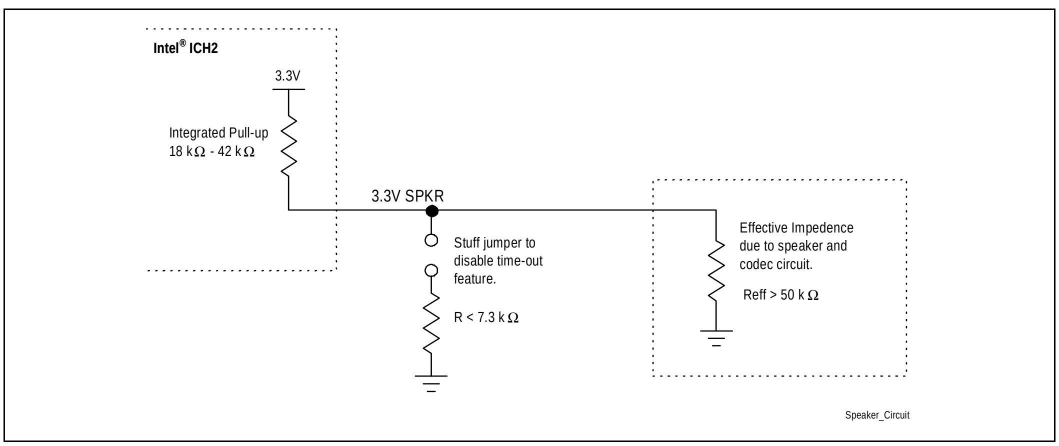
Valid Codec Configurations	Invalid Codec Configurations
AC (Primary)	MC (Primary) + X (any other type of codec)
MC (Primary)	AMC (Primary) + AMC (Secondary)
AMC (Primary)	AMC (Primary) + MC (Secondary)
AC (Primary) + MC (Secondary)	
AC (Primary) + AC (Secondary)	
AC (Primary) + AMC (Secondary)	

Note: Power management registers are in audio space for power management reasons. Therefore, if there is an audio codec in the system, it must be Primary. There cannot be two modems in a system because there is only one set of modem DMA channels.

8.2.3 SPKR Pin Consideration

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to do so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker, and as a functional strap. The strap function enables or disables the “TCO Timer Reboot function” based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-up resistor (the resistor is only enabled during boot/reset). Therefore its default state when the pin is a “no connect” is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see Figure 8-10). The value of the pull-down must be such that the voltage divider caused by the pull-down and integrated pull-up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull-up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ, and the pull-down resistor be less than 7.3 kΩ.

Figure 8-10. Example Speaker Circuit



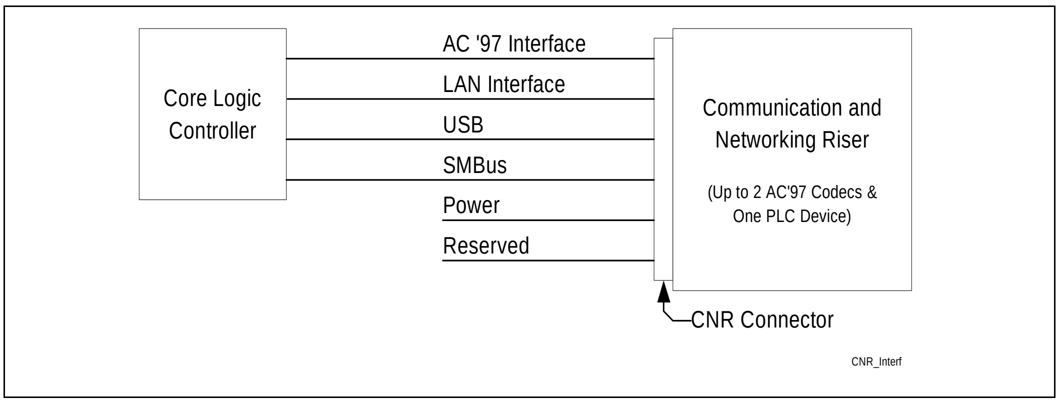
8.3 CNR

The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. Refer to *Communication and Networking Riser (CNR) Specification, Revision 1.1* (see Section 1.1).

This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Unlike the AMR (Audio Modem Riser), system designers will not sacrifice a PCI slot if they decide not to include a CNR in a particular build. It is required that the CNR A0–A2 pins be set to a unique address so that the CNR EEPROM can be accessed. See the CNR specification.

Figure 8-11 shows the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) can be either an 82562EH or an 82562EM component. Refer to the CNR specification for additional information.

Figure 8-11. CNR Interface



8.4 USB 1.1

8.4.1 Using Native USB interface

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P– data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.
- An optional 0–47 pF capacitor may be placed as close to the USB connector as possible on the USB data lines (P0±, P1±, P2±, P3±). This capacitor can be used for signal quality (rise/fall time) and to help minimize EMI radiation. Use the value in the 0–47 pF range needed to provide the best EMI immunity and best adherence to rise and fall time requirements. This capacitor is shown in the Figure 8-12.
- 15 kΩ ± 5% pull-down resistors should be placed on the USB Connector side of the series resistors on the USB data lines (P0± … P3±), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0±… P3± signals should be 45 Ω (to ground) for each USB signal P+ or P–. Using the stack-up recommended, USB requires 9-mil traces and 25-mil spacing. The impedance is 90 Ω between the differential signal pairs P+ and P– to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as critical signals. The P+/P– signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P– signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P– signal traces. The P+/P– signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 8-12 is the recommended USB schematic.

Figure 8-12. USB Data Signals

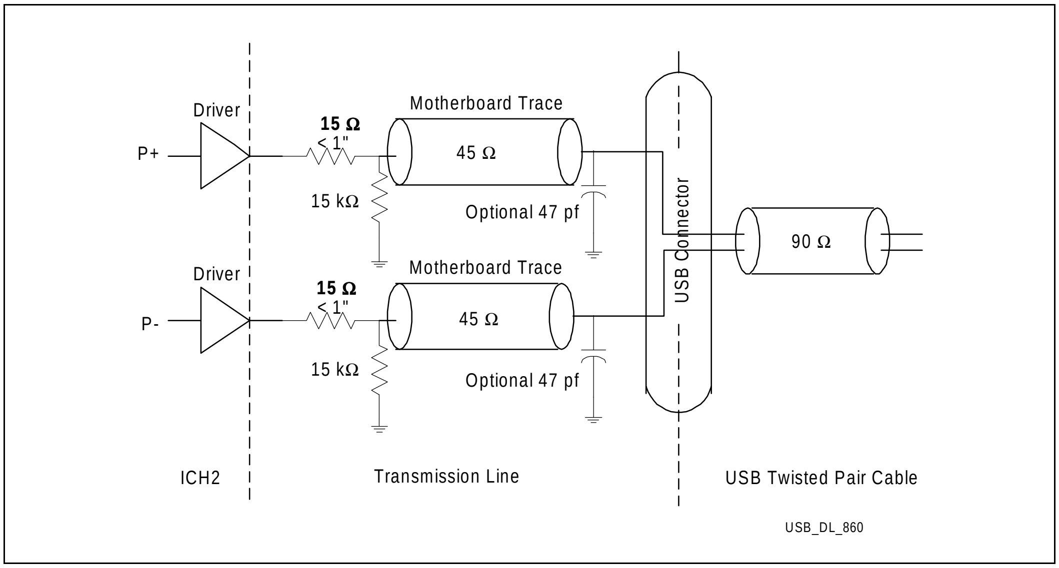


Table 8-3. Recommended USB Trace Characteristics

Impedance 'Z0' = 45.5 Ω
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Impedance 'Z0' = 45.4 Ω
Res @20°C = 53.9 mΩ

8.4.2 Disabling the Native USB Interface of the Intel® ICH2

The ICH2 native USB interface can be disabled when an external PCI based USB controller is being implemented in the platform. To disable the native USB Interface, ensure that the differential pairs are pulled down thru 15 kΩ resistors, that the OC[3:0]# signals are deasserted by pulling them up weakly to V_{CC3SBY}, and that both function 2 and function 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48 MHz USB clock is connected to the ICH2, and is kept running. This clock must be maintained even though the internal USB functions are disabled.

8.5 I/O APIC Design Recommendation

The processor does not have any I/O APIC pins that are defined. It receives interrupts for servicing via the system bus interrupt delivery mechanism. See *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet* for more details.

Intel 845 chipsets systems should incorporate the following ICH2 recommendations:

- Tie APICCLK directly to ground.
- Tie APICD [0:1] to ground through a 10 kΩ resistor.

8.5.1 PIRQ Routing Example

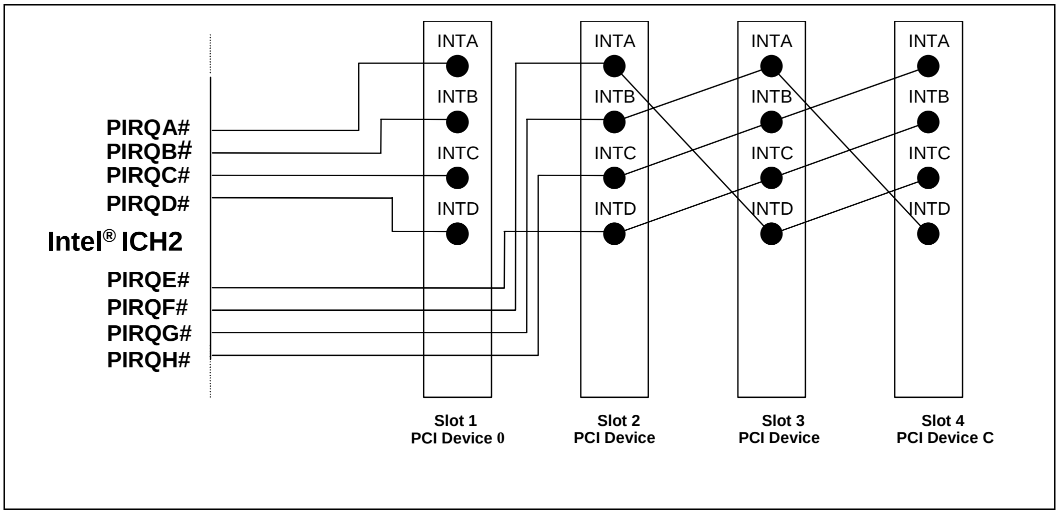
PCI interrupt request signals E-H are new to the ICH2. These signals have been added to lower the latency caused by having multiple devices on one interrupt line. With these new signals, each PCI slot can have an individual PCI interrupt request line (assuming that the system has four PCI slots). Table 8-4 shows how the ICH2 uses the PCI IRQ when the I/O APIC is active.

Table 8-4. I/O APIC Interrupt Inputs 16 Through 23 Usages

IOAPIC INTIN Pin	Function in Intel® ICH2 Using the PCI IRQ in IOAPIC
I/O APIC INTIN PIN 16 (PIRQA)	
I/O APIC INTIN PIN 17 (PIRQB)	AC’97, Modem and SMBus
I/O APIC INTIN PIN 18 (PIRQC)	
I/O APIC INTIN PIN 19 (PIRQD)	USB Controller #1
I/O APIC INTIN PIN 20 (PIRQE)	Internal LAN Device
I/O APIC INTIN PIN 21 (PIRQF)	
I/O APIC INTIN PIN 22 (PIRQG)	
I/O APIC INTIN PIN 23 (PIRQH)	USB Controller #2 (starting from ICH2 B0 silicon)

Interrupts B, D, E, and H service devices internal to the ICH2. Interrupts A, C, F, and G are unused and can be used by PCI slots. Figure 8-13 shows an example of IRQ line routing to the PCI slots.

Figure 8-13. Example PIRQ Routing



The PCI IRQ Routing shown in Figure 8-13 allows the ICH2 internal functions to have a dedicated IRQ (assuming add-in cards are single function devices and use INTA). If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI Bus, the ICH2 internal functions will start sharing IRQs.

Figure 8-13 is an example. It is up to the board designer to route the signals in the most efficient way for a particular system. A PCI slot can be routed to share interrupts with any of the ICH2 internal device/functions.

8.6 SMBus/SMLink Interface

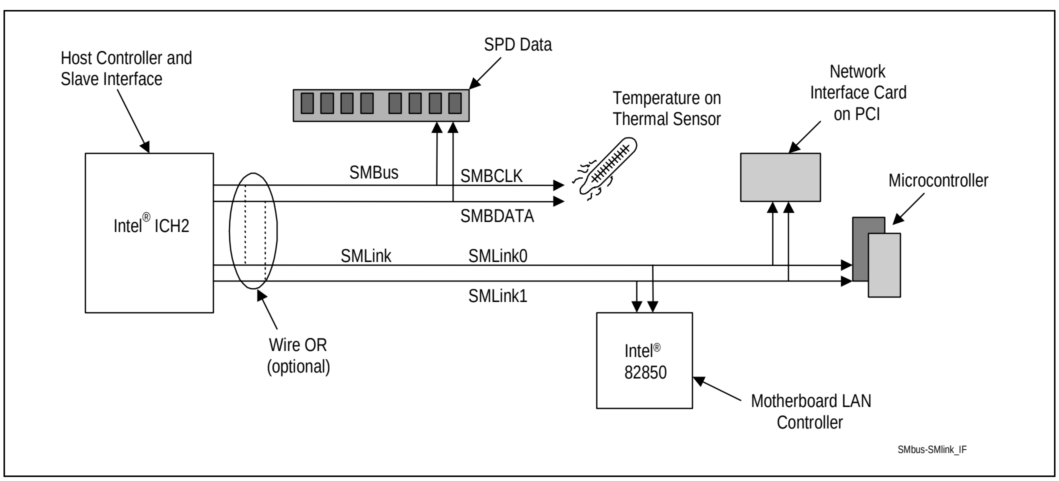
The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. The SMBus Host Controller uses these signals exclusively. The SMBus Host Controller resides inside the ICH2. If the SMBus is used only for the SDRAM SPD EEPROMs (one on each DIMM), both signals should be pulled up with a 4.7 kΩ resistor to 3.3 V.

The ICH2 incorporates a new SMLink interface that supports AOL*, AOL2*, and a slave functionality. It uses two signals, SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal, and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN (AOL) functionality, the ICH2 transmits heartbeat and event messages over the interface. When using the 82562EM LAN Connect Component, the ICH2’s integrated LAN Controller will claim the SMLink heartbeat and event messages, and send them over the network. An external, AOL2-enabled LAN Controller will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH2 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus protocol, so the two interfaces can be externally wire-OR’d together to allow an external management ASIC to access targets on the SMBus as well as the ICH2 Slave interface. This is done by connecting SMLink[0] to SMBCLK, and SMLink[1] to SMBDATA.

Figure 8-14. SMBUS/SMLink Interface



Note: Intel does not support external access to the ICH2 Integrated LAN Controller via the SMLink interface, and does not support access to the ICH2’s SMBus Slave Interface by the ICH2’s SMBus Host Controller.

8.6.1 SMBus Architecture and Design Considerations

SMBus Design Considerations

There are several possibilities for designing an SMBus using the ICH2. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs in which all devices are powered by either V_{CC_Core} or $V_{CC\_Suspend}$, and a mixed design in which some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on:

- The presence of devices that must run in STR (Suspend to RAM).
- The amount of $V_{CC\_Suspend}$ current available (i.e., minimizing load of $V_{CC\_Suspend}$).

General Design Issues and Notes

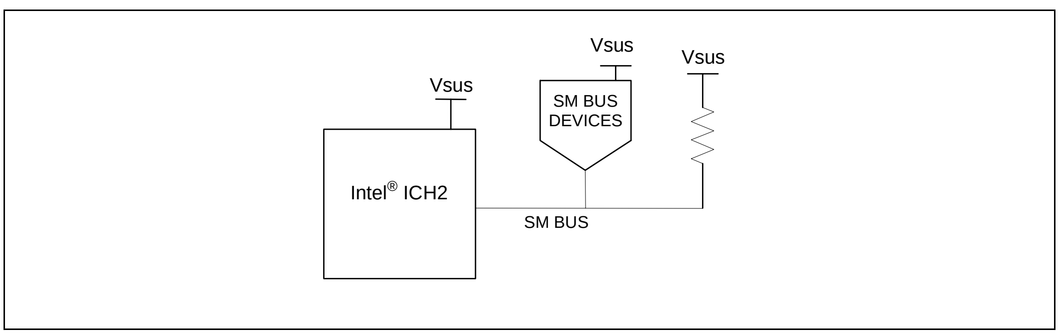
The following are general considerations for all architectures:

- The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 kΩ. This should prevent the SMBus signals from floating, which could cause leakage in the ICH2 and other devices.
- SDRAM DIMMs have their SPD device powered by the same power plane as that used for the DRAM array. Thus in a system where STR is supported, the SPD device must be powered by $V_{CC\_Suspend}$. In a system not supporting STR, this DIMM can be powered by the core supply.
- The ICH2 does not run SMBus cycles while in STR.
- SMBus devices that can operate in STR must be powered by the $V_{CC\_Suspend}$ supply.

The Unified $V_{CC\_Suspend}$ Architecture

In this design all SMBus devices are powered by the $V_{CC\_Suspend}$ supply. Consideration must be made to provide enough $V_{CC\_Suspend}$ current while in STR.

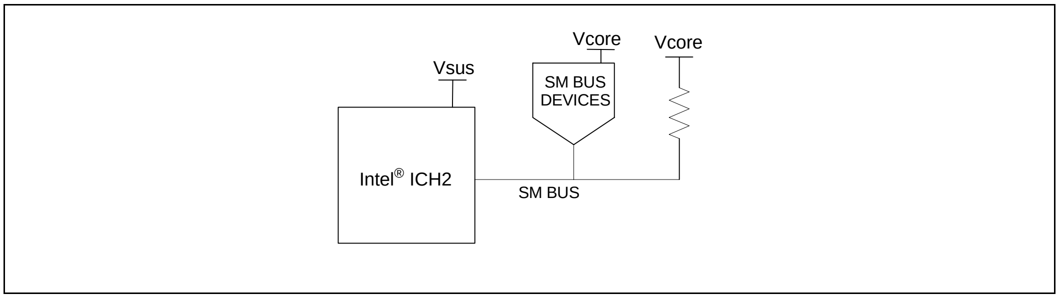
Figure 8-15. Unified $V_{CC\_Suspend}$ Architecture



The Unified V_{CC_Core} Architecture

In this design, all SMBus devices are powered by the V_{CC_Core} supply. This architecture allows none of the devices to operate in STR, but minimizes the load on $V_{CC\_Suspend}$.

Figure 8-16. Unified V_{CC_Core} Architecture

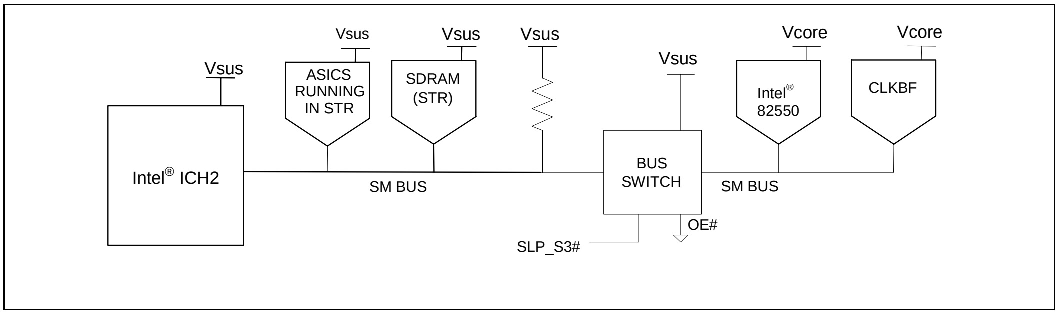


NOTES:
1. The SMBus device must be back-drive safe while its supply (V_{CORE}) is off and $V_{CC\_Suspend}$ is still powered.
2. In suspended modes in which V_{CC_Core} is off and $V_{CC\_Suspend}$ is on, the V_{CC_Core} node will be very near ground potential. In this case, the input leakage of the ICH will be approximately 10 µA.

Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes $V_{CC\_Suspend}$ leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies. (See Figure 8-17).

Figure 8-17. Mixed $V_{CC\_Suspend}$/V_{CC_Core} Architecture



Added Considerations for Mixed Architecture

- The bus switch must be powered by $V_{CC\_Suspend}$.
- If there are 5 V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3 V signal levels.
- Devices that are powered by the $V_{CC\_Suspend}$ well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.

8.7 PCI

The ICH2 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH2 supports six PCI Bus masters (excluding the ICH2) by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

The GNTA# signal on the ICH2 contains an added “top block swap” strapping function that allows the top block in the FWH to be swapped with another location. This allows for safe update up the boot block even if a power failure occurs. Refer to the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet* for more information.

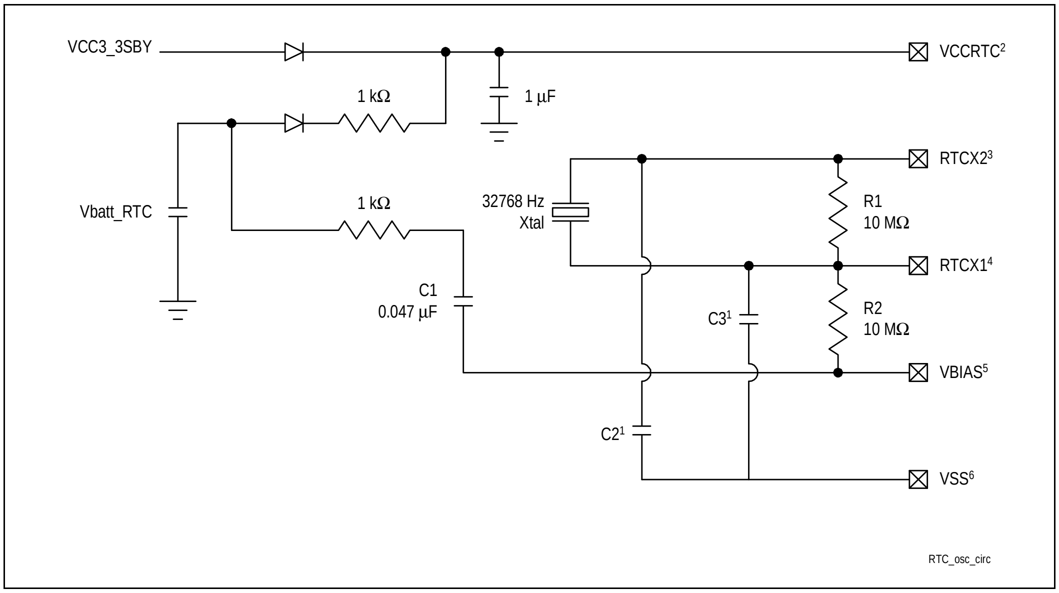
8.8 RTC

The ICH2 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down. This section describes the recommended hookup for the RTC circuit for the ICH2.

8.8.1 RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. Figure 8-18 shows the external circuitry that comprises the oscillator of the ICH2 RTC.

Figure 8-18. External Circuitry for the Intel® ICH2 RTC



NOTES:

1. The exact capacitor value must be based on the crystal maker's recommendation. (Typical values for C2 and C3 are 18 pF for a crystal with CLOAD=12.5 pF.)
2. VccRTC: Power for RTC-well.
3. RTCX2: Crystal Input 2—connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1—connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage—This pin is used to provide a reference voltage that sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground.

8.8.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 must be 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

The following equation can be used to choose the external capacitance values (C2 and C3):

Cload = (C2 * C3)/(C2+C3) + Cparasitic

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

8.8.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible (about ¼ inch is sufficient).
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator V_{CC} should be clean. Use a filter, such as an RC lowpass filter or a ferrite inductor.

8.8.4 RTC External Battery Connection

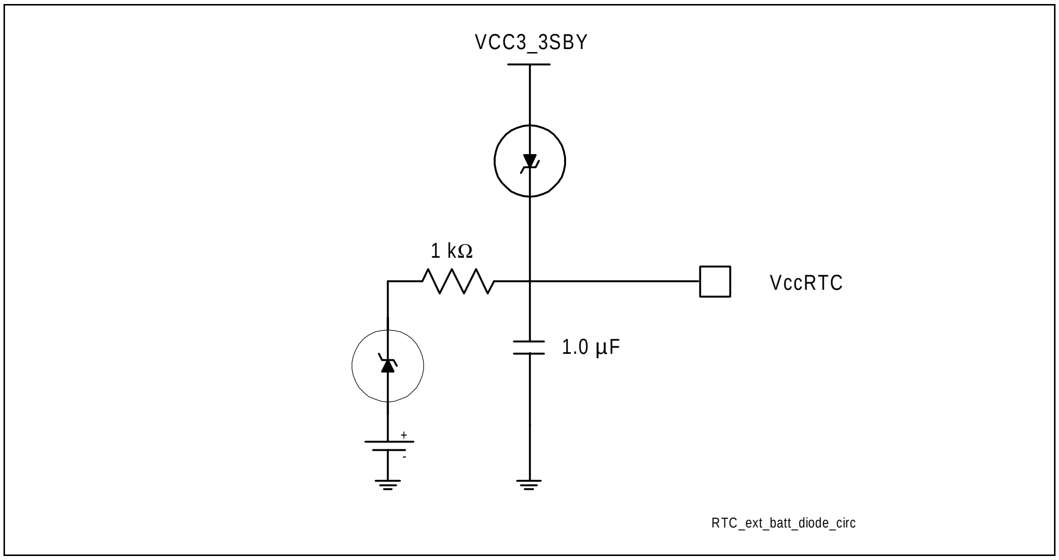
The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system. Example batteries are Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

$$170{,}000\ \mu Ah / 3\ \mu A = 56{,}666\ h = 6.4\ years$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH2 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 8-19 is an example of a diode circuit that is used.

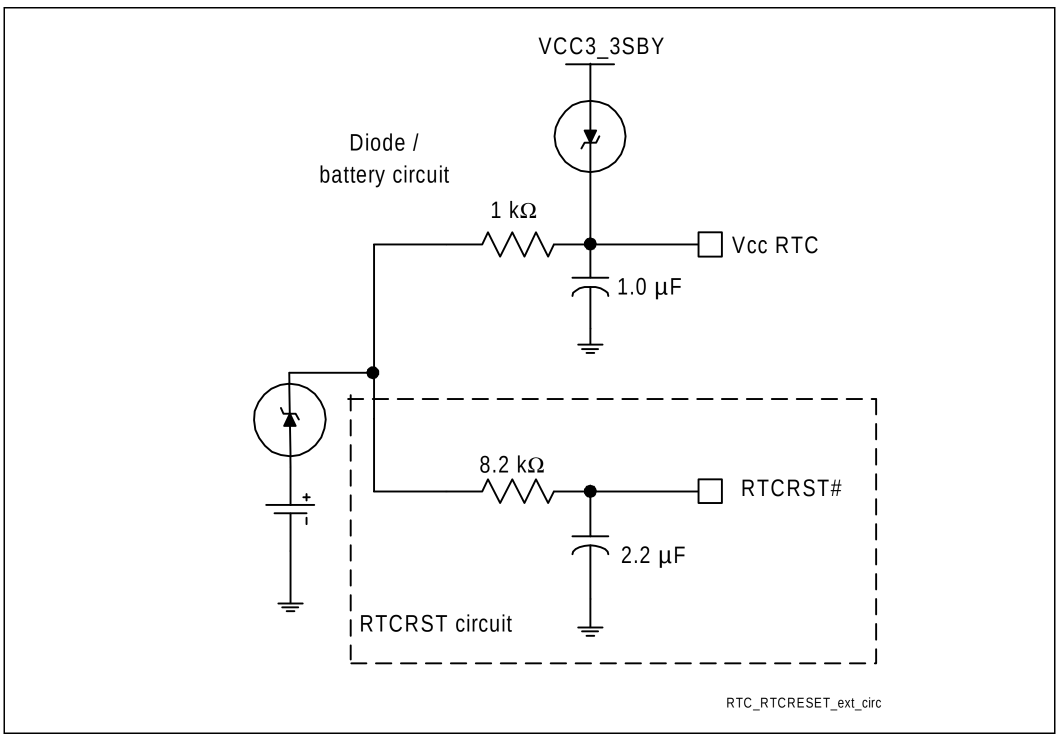
Figure 8-19. A Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

8.8.5 RTC External RTCRST Circuit

Figure 8-20. RTCRST# External Circuit for the Intel® ICH2 RTC



The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC-well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10–20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. Therefore, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit when combined with the diode circuit Figure 8-19 allows the RTC-well to be powered by the battery when the system power is not available. Figure 8-18 is and example of this circuitry that is used in conjunction with the external diode circuit.

8.8.6 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch (the shorter the better).
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

8.8.7 VBIAS DC Voltage and Noise Measurements

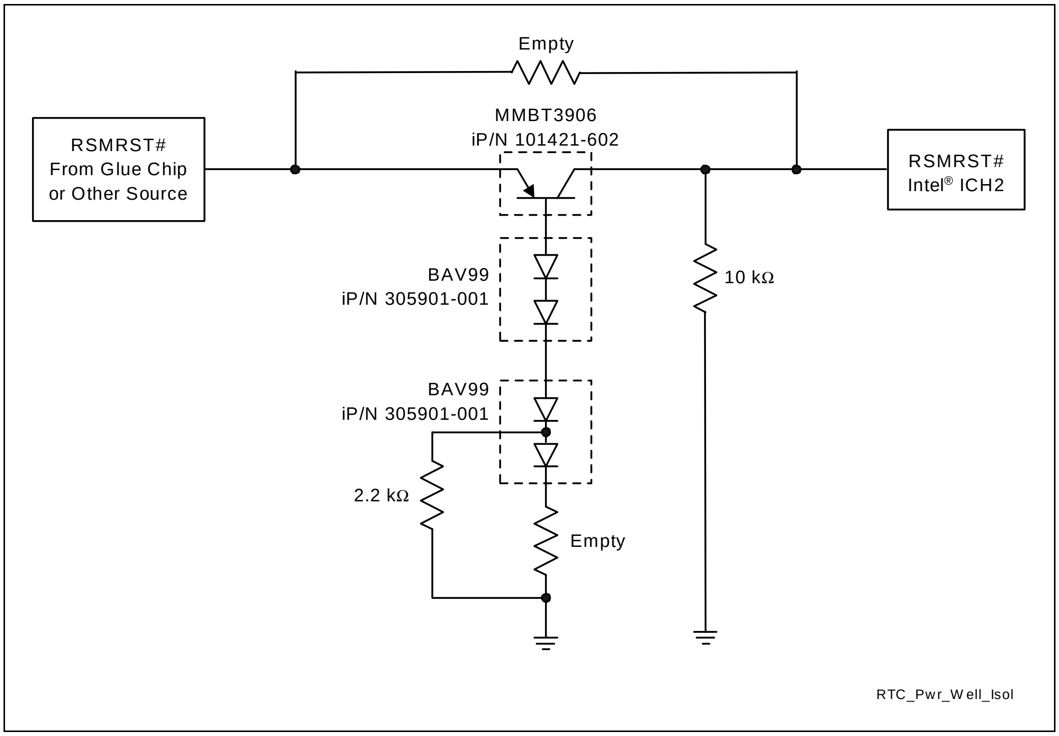
- Steady state VBIAS will be a DC voltage of at least 200 mV.
- VBIAS will be “kicked” when the battery is inserted to about 0.7 V–1.0 V, but it will come back to its DC value within a few ms.
- VBIAS is very sensitive and cannot be directly probed; it can be probed through a .01 µF capacitor.
- Excess noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize noise on VBIAS, it is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet*.

8.8.8 Power-Well Isolation Control Strap Requirements

If not using the glue chip, all RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST#, when configured as shown in Figure 8-20, meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CCRTC} leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

The circuit shown in Figure 8-21 should be implemented to control well isolation between the 3.3 V resume and the RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).

Figure 8-21. RTC Power-Well Isolation



8.9 LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 8-5. Differences between Intel® 82562EM, Intel® 82562ET, and Intel® 82562EH

LAN Connect Component	Connection	Features
Intel® 82562EM	Advanced 10/100 Ethernet	AOL* and Ethernet 10/100 Connection
Intel® 82562ET	10/100 Ethernet	Ethernet 10/100 Connection
Intel® 82562EH	1 MB HomePNA* LAN	1 MB HomePNA connection

Intel developed a dual footprint for 82562ET and 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the OEM to install the appropriate Platform LAN connect component to meet the market need. Design guidelines are provided for each required interface and connection. Refer to Figure 8-22 and Table 8-6.

Figure 8-22. Intel® ICH2/LAN Connect Section

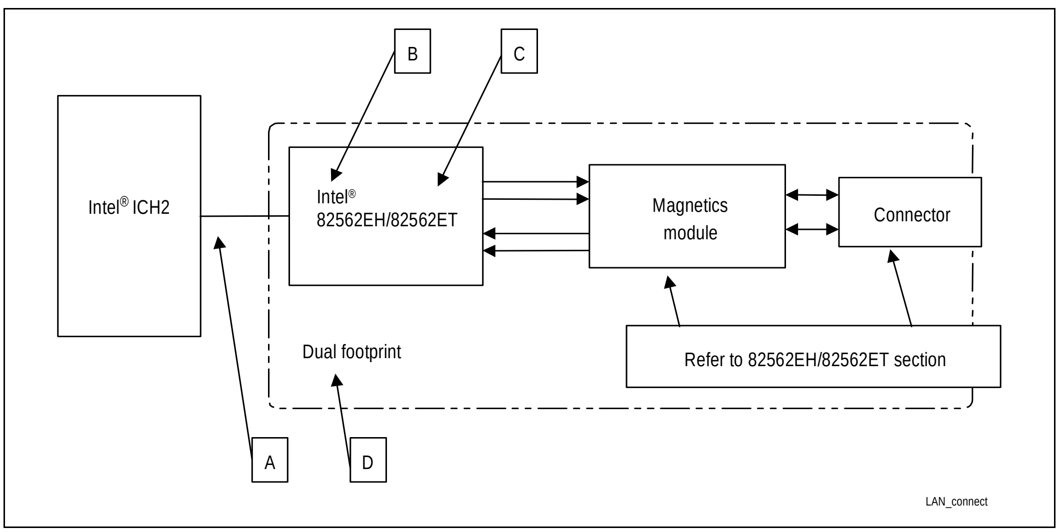


Table 8-6. LAN Design Guide Section Reference

Layout Section	Figure 8-22 Reference	Design Guide Section
Intel® ICH2—LAN Interconnect	A	8.9.1—LAN Interconnect Guidelines
General Routing Guidelines	B,C,D	8.9.2—General LAN Routing Guidelines and Considerations
Intel® 82562EH	B	8.9.3—*Intel® 82562EH Home/PNA* Guidelines*
Intel® 82562ET /82562EM	C	8.9.4—*Intel® 82562ET / 82562EM Guidelines*
Dual Layout Footprint	D	8.9.6—*Intel® 82562ET / 82562EH Dual Footprint Guidelines*

8.9.1 Intel® ICH2—Platform LAN Connect Guidelines

This section contains guidelines to the design of motherboards and riser cards to comply with the LAN Connect Interface. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH2 to LAN component interface. The following signal lines are used on the LAN Interconnect interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed. Dual Footprint guidelines are described in Section 8.9.6

8.9.1.1 Bus Topologies

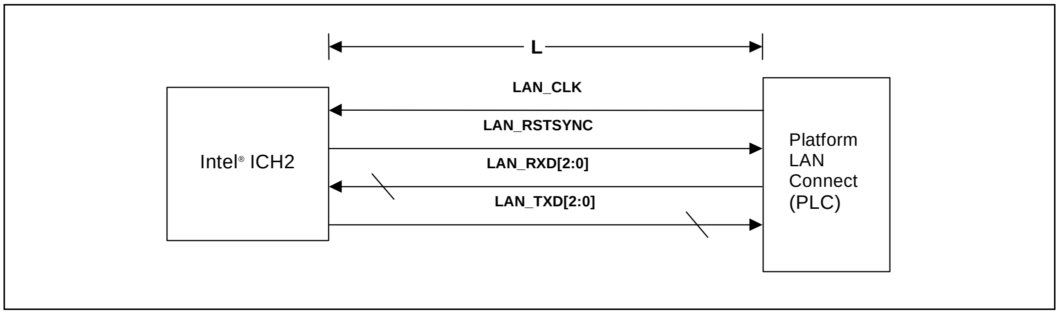
The LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual Footprint
- LOM/CNR Implementation

8.9.1.2 Point-to-Point Interconnect

The following are guidelines for a single solution motherboard; 82562EH, 82562ET, or CNR is installed.

Figure 8-23. Single Solution Interconnect



Length requirements for Figure 8-23:

- 82562EH: L = 4.5 inches to 10 inches (Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected).
- 82562ET: L = 3.5 inches to 10 inches
- CNR: L = 3 inches to 9 inches (0.5 inch to 3 inches on card).

8.9.1.3 LOM /CNR Interconnect

The following guidelines allow for an all inclusive motherboard solution. This layout combines LOM (LAN on Motherboard), dual footprint, and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time. A model of this is found in Figure 8-24. The recommended trace routing lengths are listed in Table 8-7.

Figure 8-24. LOM/CNR Interconnect

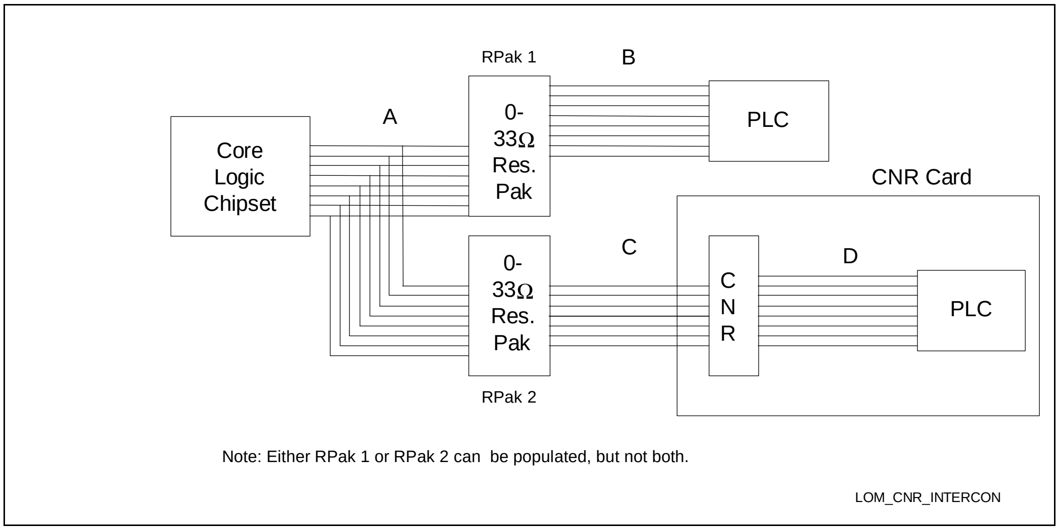


Table 8-7. Length Requirements for Figure 8-24

Configuration	A	B	C	D
Intel® 82562EH	0.5 inch to 6 inches	4 inches to (10 inches– A)		
Intel® 82562ET/82562EM	0.5 inch to 7 inches	3 inches to (10 inches– A)		
Dual Footprint	0.5 inch to 6.5 inches	3.5 inches to (10 inches– A)		
Intel® 82562ET/EH Card[1]	0.5 inch to 6.5 inches		2.5 inches to (9 inches– A)	0.5 inch to 3 inches

NOTES:

1. Total trace length should not exceed 13 inches

Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω to 33 Ω.
- LAN on motherboard PLC can be a dual footprint configuration.

8.9.1.4 Signal Routing and Layout

Platform LAN Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

8.9.1.5 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews, and is the largest part of the $t_{RMATCH.}$ parameter. This parameter is the sum of the trace length mismatch between the JCLK and other data signals. To meet this requirement, the length of each data trace on the motherboard is either equal to or as much as 0.5 inch shorter than the JCLK trace. Noise due to crosstalk from non_PLC signals should be minimized by maintaining at least 100 mils of spacing.

8.9.1.6 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ± 15% is strongly recommended. Otherwise, signal integrity requirements may be violated.

8.9.1.7 Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ring back. A 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

8.9.2 General LAN Routing Guidelines and Considerations

8.9.2.1 General Trace Routing Considerations

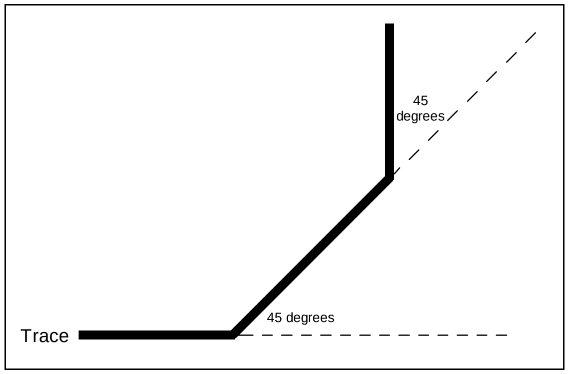
Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following to help optimize board performance.

Note: Some of the following suggestions are specific to a 4.5-mil stack-up:

- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inch.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces, and closer than 100 mils to the differential traces. 300 mils separation is recommended.
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two, 45-degree bends instead. Refer to Figure 8-25.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock.
- Place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 8-25. Trace Routing



8.9.2.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and as wide as practical. Ideally, the trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and as wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to minimize series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

8.9.2.1.2 Signal Isolation

The following rules apply to signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

8.9.2.2 Power and Ground Connections

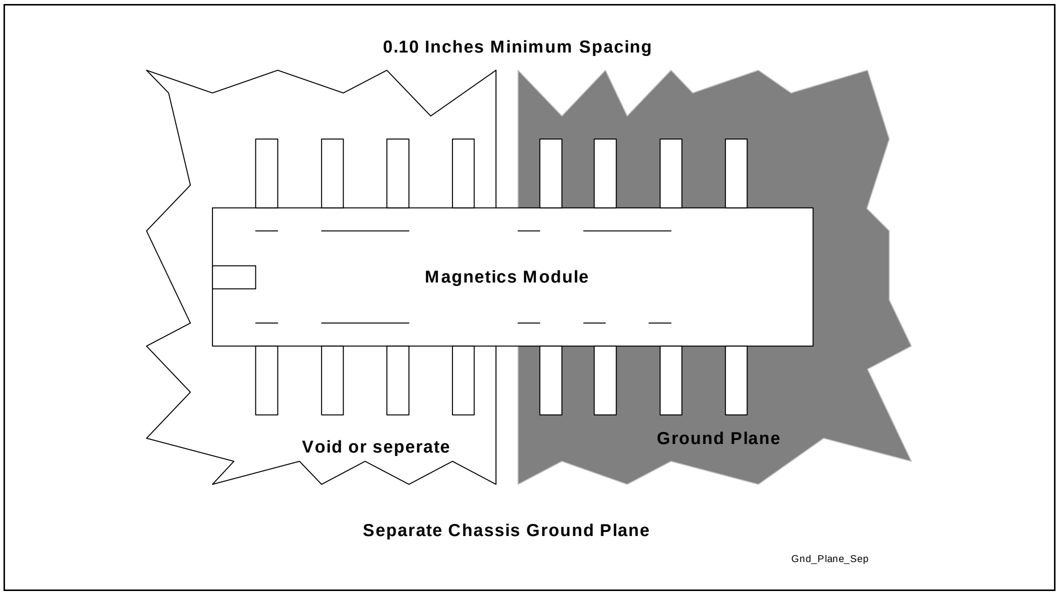
The following rules and guidelines apply to power and ground connections:

- All V_{CC} pins should be connected to the same power supply.
- All V_{SS} pins should be connected to the same ground plane.
- 4–6 decoupling capacitors, including two 4.7 µF capacitors, are recommended.
- Place decoupling as close as possible to power pins.

8.9.2.2.1 General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of at least 100 mils.

Figure 8-26. Ground Plane Separation



Proper grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. This will significantly reduce EMI radiation.

The following rules help reduce circuit inductance in both backplanes and motherboards.

- Route traces over a continuous plane with no interruptions (do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant areas, which will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath the transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.
- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6 mm (59.0 mil). This is a critical requirement needed to pass FCC part 68 testing for phoneline connection. Note that for worldwide certification, 2.5 mm is required. In North America, the spacing requirement is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

8.9.2.3 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics, or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, any impedance mismatch in the traces will be aggravated if they are longer. The magnetics should be as close to the connector as possible (less than or equal to one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk transmitted onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC), and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inch from the differential traces.

- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will induce more crosstalk onto the closest receive trace, and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45/11, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that are used have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or term plane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. Short traces will have fewer problems if the differential impedance is a little deviated.

  To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close (see note) to each other, the edge coupling can lower the effective differential impedance by 5 to 20 Ω. A 10 Ω to 15 Ω drop in impedance is common.
- Use of a capacitor between the transmit traces that is too large, and/or too much capacitance between the magnetic's transmit center-tap (on the 82562ET side of the magnetics) and ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies, and will degrade the transmit BER performance. Caution should be exercised if a capacitor is put in either of these locations. If a capacitor is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These capacitors are not necessary unless there is some overshoot in 100 Mbps mode.
- Not keeping the two traces within a differential pair close (see note) to each other. Keeping them close (see note) helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

Note: Close should be considered to be less than 0.030 inch between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

8.9.3 Intel® 82562EH Home/PNA* Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in General LAN Routing Guidelines and Considerations, Section 8.9.2. The following sections describe additional guidelines for implementing an 82562EH Home/PNA* Platform LAN connect component.

8.9.3.1 Power and Ground Connections

Do the following for power and ground connections:

- For best performance place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.
- The analog power supply pins for 82562EH (V_{CCA}, V_{SSA}) should be isolated from the digital V_{CC} and V_{SS} through the use of Ferrite beads. In addition, adequate filtering and decoupling capacitors should be used between V_{CC} and V_{SS}, and V_{CCA} and V_{SSA} power supplies.

8.9.3.2 Guidelines for Intel® 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section has guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI) that can cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

8.9.3.3 Crystals and Oscillators

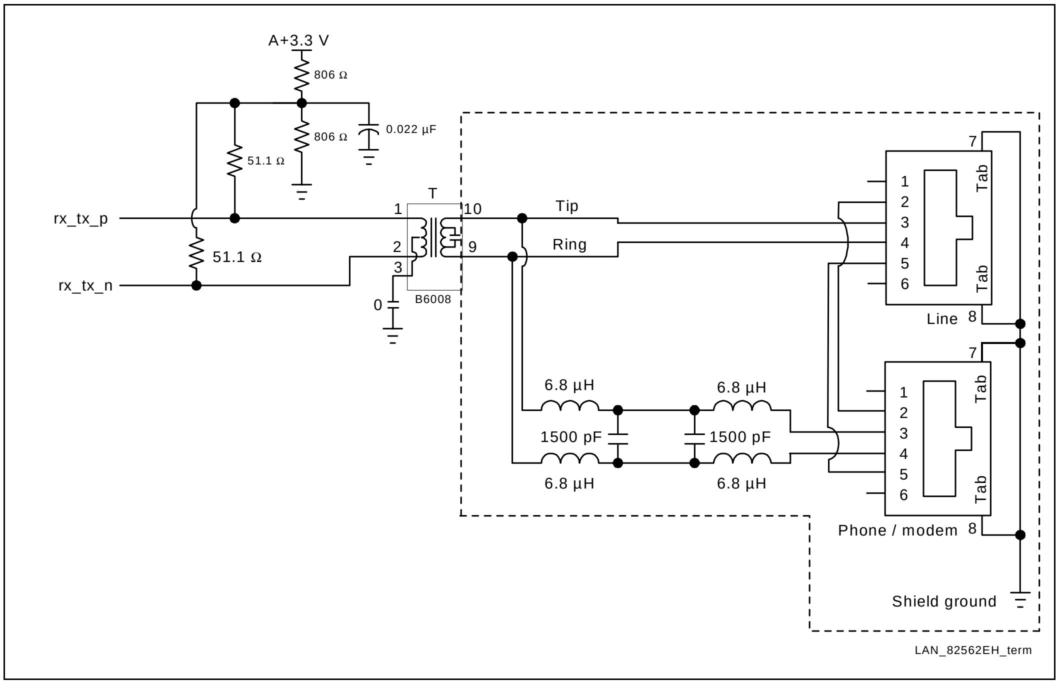
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should be kept away from the HomePNA magnetics module to prevent interference of communication. The retaining straps of the crystal (if they exist) should be grounded to prevent the possibility of radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562EH keeping the length as short as possible, and do not route any noisy signals in this area.

8.9.3.4 Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1 Ω ± 1% resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1 Ω resistors is connected to a voltage divider network. The opposite end of one 806 Ω resistor is tied to V_{CCA} (3.3 V), and the opposite end of the other 806 Ω resistor and the capacitor are connected to ground. The termination is shown in Figure 8-27.

Figure 8-27. Intel® 82562EH Termination



The filter and magnetics component T integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.

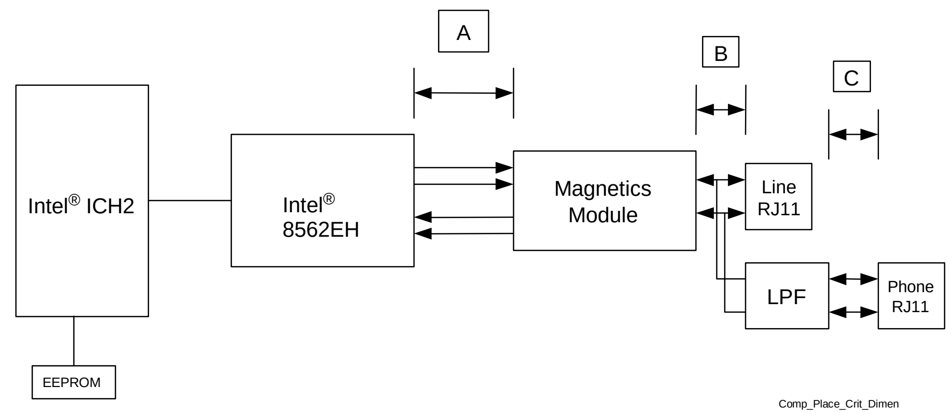
One RJ-11 jack (labeled "LINE" in Figure 8-27, 82562EH Termination) allows the node to be connected to the phoneline, and the second jack (labeled "PHONE" in Figure 8-27) allows other downline devices to be connected at the same time. This second connector is not required by HomePNA. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack, is also recommended by the HomePNA to minimize interference between the HomePNA connection and a POTs (Plain Old Telephone) voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack because the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA website, *www.homepna.org*, for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

8.9.3.5 Critical Dimensions

There are three dimensions to consider during layout. Distance 'B' from the line RJ11 connector to the magnetics module, distance 'C' from the phone RJ11 to the LPF (Low Pass Filter) if implemented, and distance 'A' from 82562EH to the magnetics module (See Figure 8-28).

Figure 8-28. Critical Dimensions for Component Placement



Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

8.9.3.5.1 Distance from Magnetics Module to Line RJ11

This distance 'B' should be given highest priority and should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise that can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

8.9.3.5.2 Distance from Intel® 82562EH to Magnetics Module

Because of the high-speed of signals present, distance 'A' between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance from connects to the magnetics module.

In general, any section of trace that is intended for use with high-speed signals should incorporate proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal can have a high-frequency component that may contribute more EMI than the original signal itself.

8.9.3.5.3 Distance from LPF to Phone RJ11

This distance 'C' should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise that can degrade the receive circuit performance and contribute to radiated emissions from the transmit side

8.9.4 Intel® 82562ET / 82562EM Guidelines

82562ET / 82562EM Guidelines Related Documents

Refer to Section 1.1, *Related Documentation*, for a list of related documents.

For correct LAN performance, designers must follow the general guidelines outlined in Section 8.9.2, General LAN Routing Guidelines and Considerations. The following sections describe additional guidelines for implementing an 82562ET or 82562EM Platform LAN connect component.

8.9.4.1 Guidelines for Intel® 82562ET / 82562EM Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI) than can cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Therefore, it is imperative that all designs be optimized to fit in a very small space.

8.9.4.2 Crystals and Oscillators

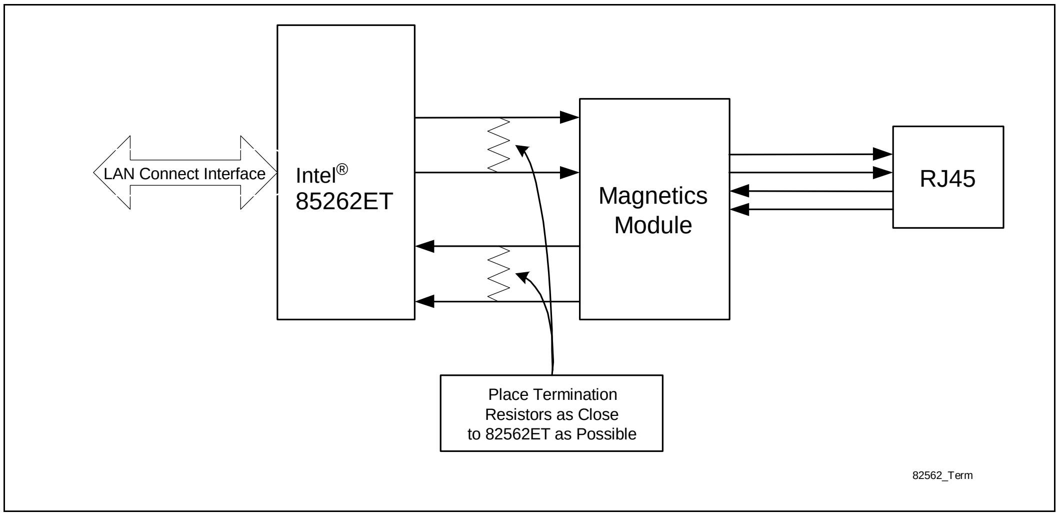
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they exist) should be grounded to prevent the possibility of radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM keeping the trace length as short as possible, and do not route any noisy signals in this area.

8.9.4.3 Intel® 82562ET / 82562EM Termination Resistors

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (82562ET or 82562EM) as possible. This is because these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

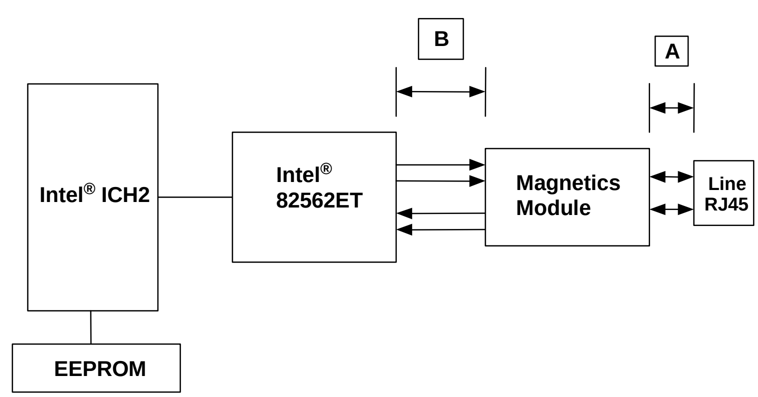
Figure 8-29. Intel® 82562ET/82562EM Termination



8.9.4.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘A’ from the line RJ45 connector to the magnetics module, and distance ‘B’ from the 82562ET or 82562EM to the magnetics module (See Figure 8-30)

Figure 8-30. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

8.9.4.4.1 Distance from Magnetics Module to RJ45

Distance 'A' in Figure 8-30: should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- **Differential Impedance—**The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- **Trace Symmetry—**Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance 'B' can be sacrificed. Keeping the total distance between the 82562ET and RJ-45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second order effects.

8.9.4.5 Distance from Intel® 82562ET to Magnetics Module

Distance 'B' should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should incorporate proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed for a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

8.9.4.6 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant areas. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane, and all power vias should be connected to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high-frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and will reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

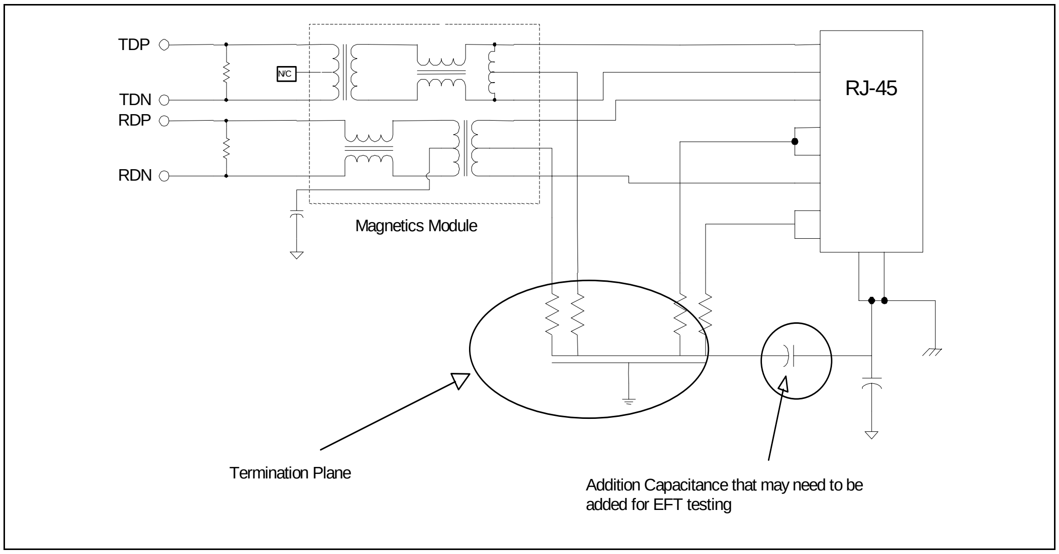
8.9.4.6.1 Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ-45 connector and on the magnetics module to ground. Depending on overall shielding and grounding design, this may be chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

8.9.4.6.2 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the term plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

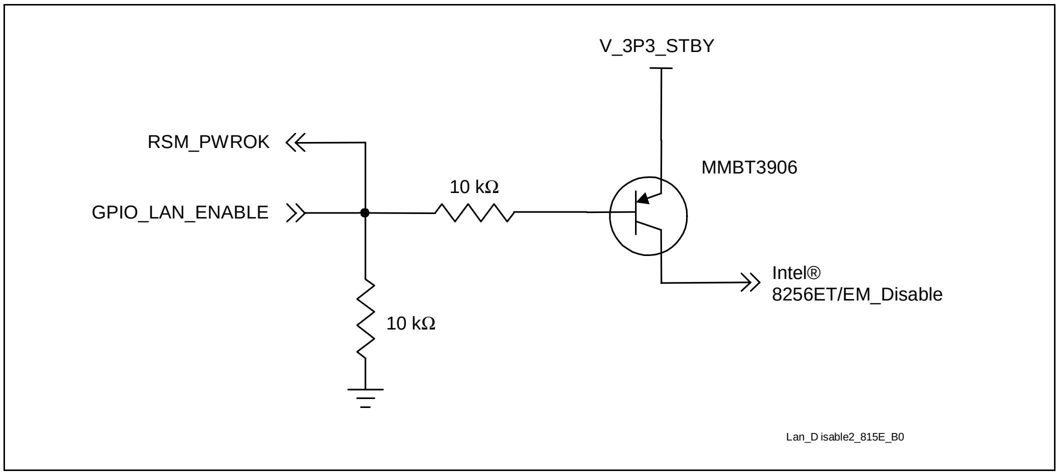
Figure 8-31. Termination Plane



8.9.5 Intel® 82562ET/82562EM Disabling Method

To disable the 82562ET/EM, the device must be isolated (disabled) before reset (RSM_PWROK) is asserted. When using a GPIO such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown in Figure 8-32 provides this operation. BIOS can disable the LAN micro controller by controlling the GPIO.

Figure 8-32. Intel® 82562ET/EM Disable Circuit



There are 4 pins that are used to put the 82562ET/EMcontroller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 8-8 describes the operational/disable features for this design

Table 8-8. Intel® 82562ET/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled with Clock (low power)
1	1	1	1	Disabled without Clock (lowest power)

Test_En (see Table 8-8) should be pulled-down through a 100 Ω resistor. The remaining 3 control signals should each be connected through 100 Ω series resistors to the common node "82562ET/EM_Disable" of the disable circuit.

8.9.6 Intel® 82562ET / 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM component in a single motherboard design. The following are guidelines for the 82562ET/82562EH Dual Footprint option. The guidelines called out in Section 8.9.1 through 8.9.4 apply to this configuration. The dual footprint for this particular solution uses an SSOP footprint for 82562ET, and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in Figure 8-33 and Figure 8-34.

Figure 8-33. Dual Footprint LAN Connect Interface

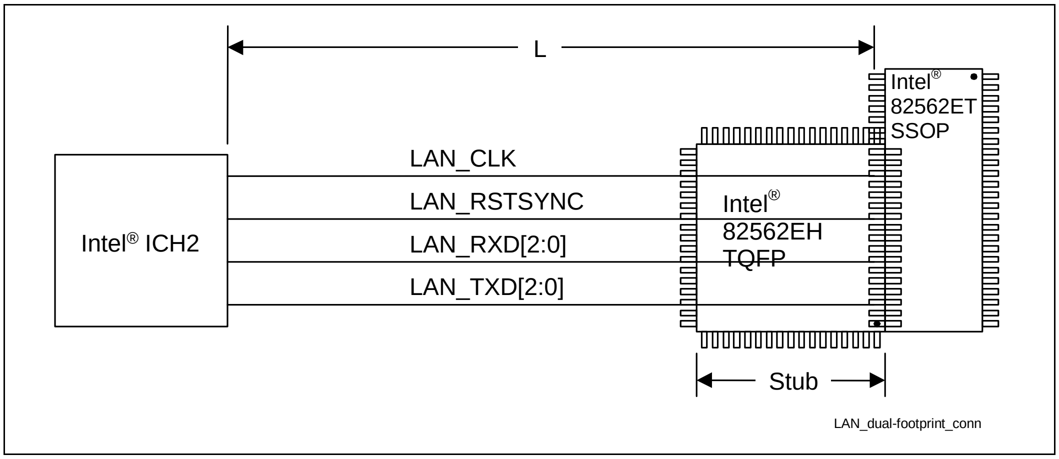
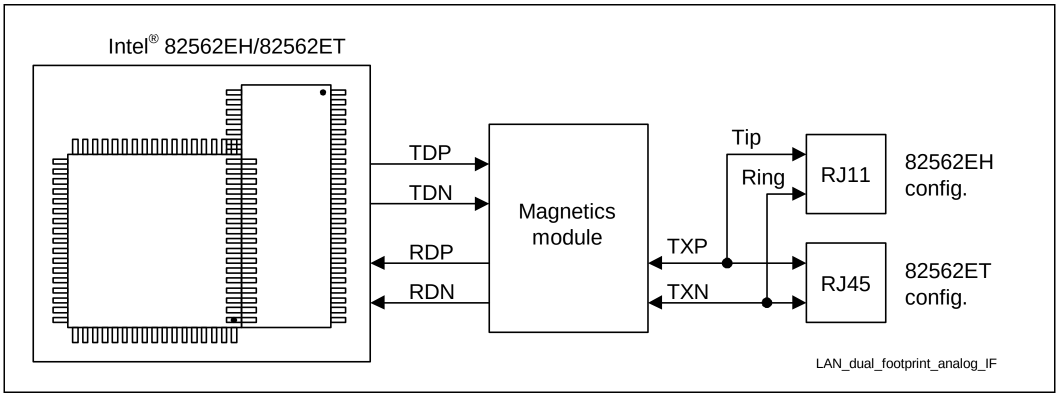


Figure 8-34. Dual Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 3.5 inches to 10 inches
- Stub < 0.5 inch
- Either 82562EH or 82562ET/82562EM can be installed, but not both.
- 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- The 82562EH and 82562ET configurations share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, LAN_TXD0, RDP, RDN, RXP/Ring, and RXN/Tip.
- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22 Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistors should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines so that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component. In an optimal layout, there should be no stubs.
- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA and Ethernet performance.

8.10 Intel® ICH2 Decoupling Recommendations

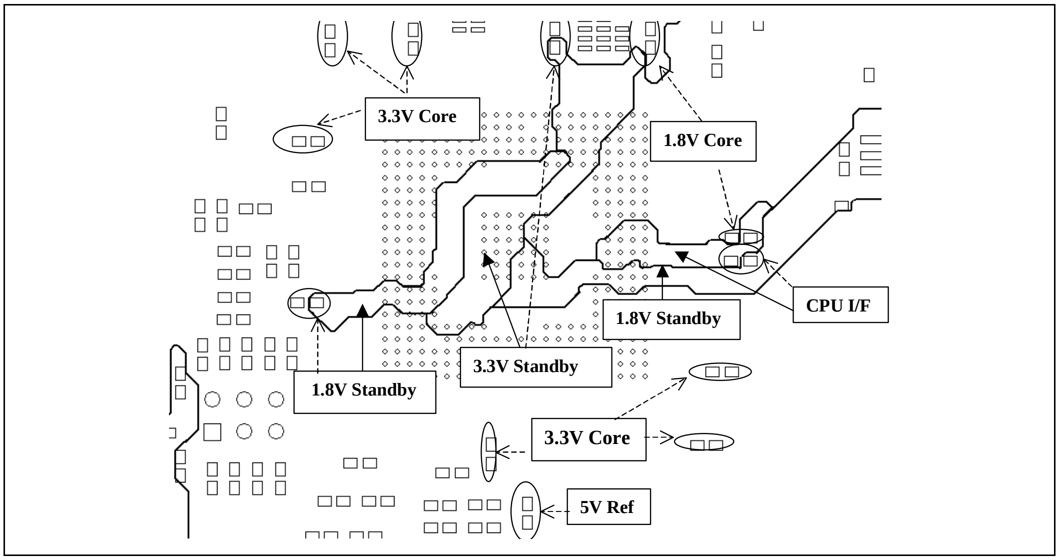
The ICH2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use decoupling capacitors specified in Table 8-9 to ensure that the components maintain stable supply voltages. The capacitors should be placed as close to the package as possible (200 mils nominal). Refer to Figure 8-35 for a layout example. It is recommended that for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Table 8-9. Decoupling Capacitor Recommendation

Power Plane/Pins	Number of Decoupling Capacitors	Capacitor Value
3.3 V Core	6	0.1 µF
3.3 V Standby	1	0.1 µF
Processor I/F (1.3 ~ 2.5 V)	1	0.1 µF
1.8 V Core	2	0.1 µF
1.8 V Standby	1	0.1 µF
5 V Reference	1	0.1 µF
5 V Reference Standby	1	0.1 µF

Figure 8-35 shows the layout of the ICH2 decoupling capacitors for various power planes around the ICH2. The decoupling capacitors are circled and have pointers that identify the power planes/traces to which they are connected.

Figure 8-35. Decoupling Capacitor Layout



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9 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device.

9.1 FWH Decoupling

A 0.1 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple high-frequency noise that may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pin to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

9.2 In-Circuit FWH Programming

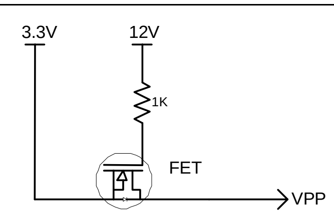
All cycles destined for the FWH will appear on PCI. The ICH2 hub interface to PCI Bridge will put all processor boot cycles on PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI. This enables the ability to boot from of a PCI card that positively decodes these memory cycles. To boot off a PCI card it is necessary to keep the ICH2 in subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, there will be two devices positively decoding the same cycle. After booting from a PCI card, it is possible to potentially program the FWH in circuit and program the ICH2 CMOS.

9.3 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. The flash cells will program about 50% faster when V_{PP} is 12 V. However, the FWH only supports 12 V V_{PP} for 80 hours. The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin **must** be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The circuit shown in Figure 9-1 allows testers to apply 12 V to the V_{PP} pin while keeping the 12 V separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 9-1. FWH VPP Isolation Circuitry



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10 Miscellaneous Logic

The ICH2 requires additional external circuitry to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip, or discrete logic.

10.1 Glue Chip

To reduce the component count and BOM (Bill of Materials) cost of the ICH2 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. By integrating much of the required glue logic, overall board cost can be reduced. The following functions are integrated into the Glue Chip.

- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers

More information regarding this component is available from the following vendors:

Vendor	Contact Information
Philips Semiconductors	6028 44th Way NE Olympia, WA 98516-2477 Phone: (360) 413-6900 Fax: (360) 438-3606
Fujitsu Microelectronics	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 Phone: 1-800-866-8600 Fax: 1-408-922-9179

Note: These vendors, devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list may be subject to change without notice.

10.2 Discrete Logic

As an alternative solution, external circuitry may be implemented into a design if not using all of the features of the Glue Chip. Refer to the Customer Reference Board schematic in Appendix A.

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11 Platform Clock Routing Guidelines

The following sections describe platform clock routing layout guidelines for 845 chipset-based systems.

11.1 Clock Generation

Only one clock generator component is required in an 845 chipset-based system. Clock synthesizers that meet the *Intel® CK408 Clock Synthesizer/Driver Specification* are suitable for 845 chipset- based systems. For more information on CK408 compliance, refer to the *Intel® CK408 Clock Synthesizer/Driver Specification*. The following tables and figure list and illustrate the 845 chipset clock groups, the platform system clock cross-reference, and the platform clock distribution.

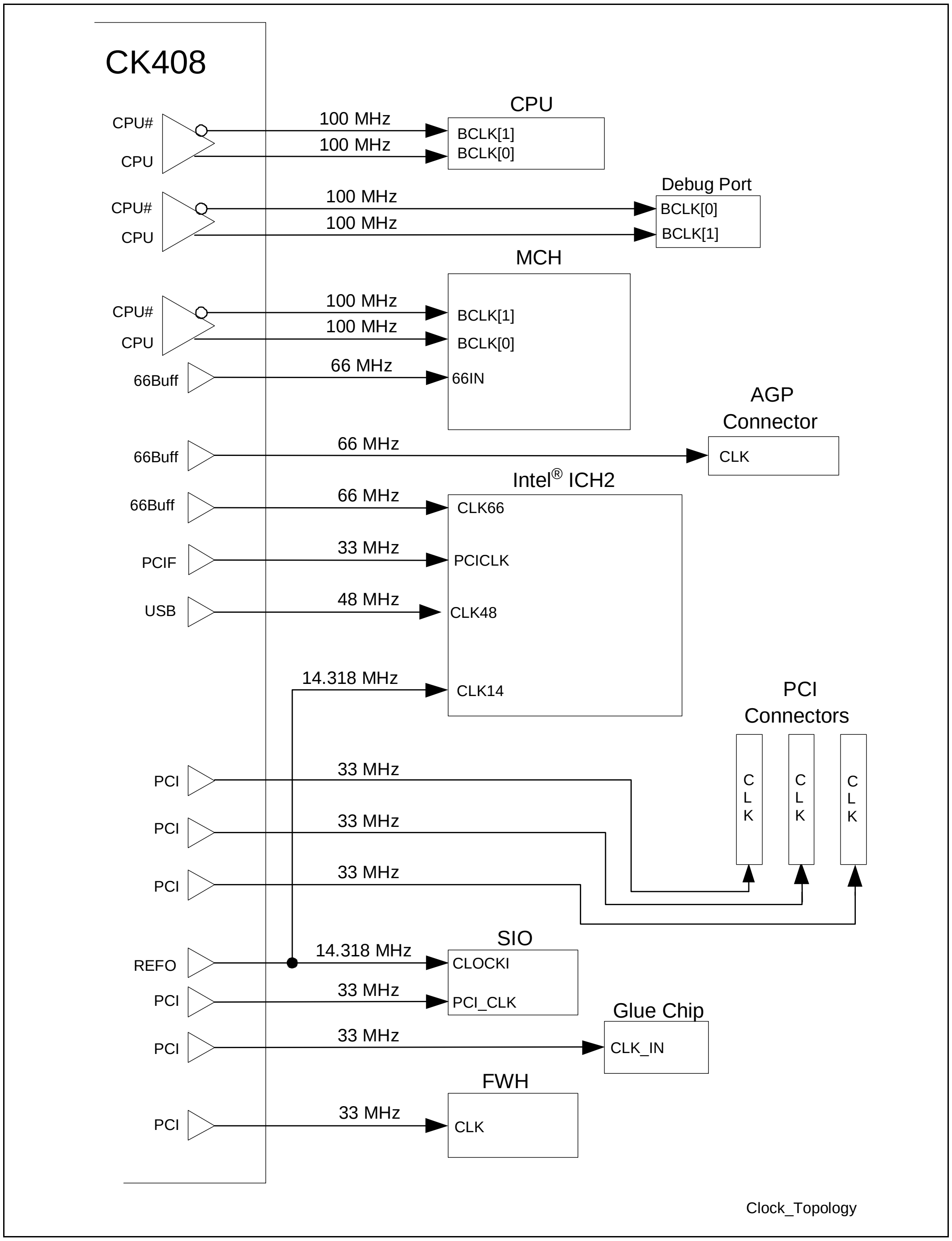
Table 11-1. Intel® 845 Chipset Clock Groups

Clock Name	Frequency	Receiver
Host_CLK	100 MHz	Processor, Debug Port, and MCH
CLK66	66 MHz	MCH and Intel® ICH2
AGPCLK	66 MHz	AGP Connector or AGP Device
CLK33	33 MHz	ICH2, SIO, Glue Chip, and FWH
CLK14	14.318 MHz	ICH2 and SIO
PCICLK	33 MHz	PCI Connector
USBCLK	48 MHz	ICH2

Table 11-2. Platform System Clock Cross-Reference

Clock Group	CK408 Pin	Component	Component Pin Name
HOST_CLK	CPU	CPU	BCLK0
	CPU#	CPU	BCLK1
	CPU	Debug Port	BCLK0
	CPU#	Debug Port	BCLK1
	CPU	MCH	BCLK0
	CPU#	MCH	BCLK1
CLK66	66BUFF	MCH	66IN
		Intel® ICH2	CLK66
AGPCLK	66BUFF	AGP Connector or AGP Device	CLK
CLK33	PCIF	ICH2	PCICLK
	PCI	SIO	PCI_CLK
	PCI	Glue Chip	CLK_IN
	PCI	FWH	CLK
CLK14	REF0	ICH2	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector 1	CLK
		PCI Connector 2	CLK
		PCI Connector 3	CLK
USBCLK	USB	ICH2	CLK48

Figure 11-1. Clock Topology



11.2 Clock Group Topology and Layout Routing Guidelines

11.2.1 HOST_CLK Clock Group

The clock synthesizer provides three sets of 100 MHz differential clock outputs. The 100 MHz differential clocks are driven to the processor, the 845 chipset, and the processor debug port as shown in Figure 11-1.

The clock driver differential bus output structure is a "Current Mode Current Steering" output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying I_{OUT} by the value of Rt. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a "Shunt Source termination." Refer to Figure 11-2 for an illustration of this termination scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage, and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board, and Rs should be between 20 and 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity and only degrade the edge rate.

Mult0 pin (pin #43) is connected to HIGH, making the multiplication factor 6.

The I_{REF} pin (pin # 42) is connected to ground through a 475 Ω ± 1% resistor, making the I_{REF} 2.32 mA.

Figure 11-2. Source Shunt Termination

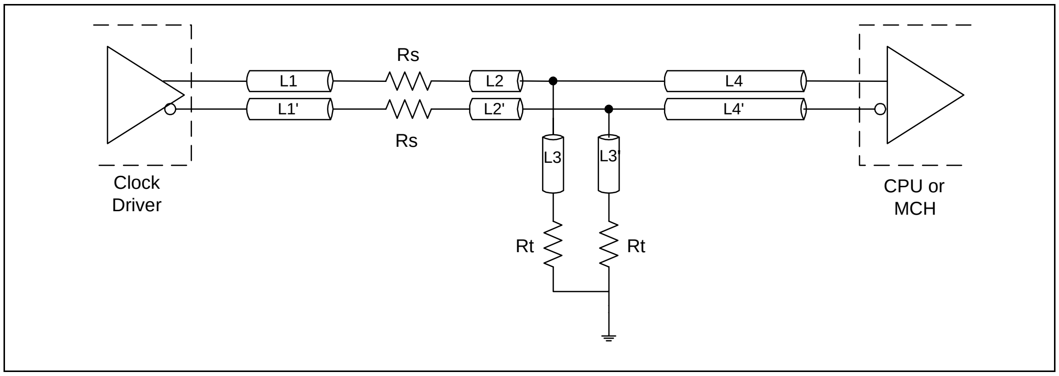


Table 11-3. BCLK [1:0]# Routing Guidelines

Layout Guideline	Value	Illustration	Notes
BCLK Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	Figure 11-1	1, 2, 3, 4
Differential pair spacing	W max.	Figure 11-4	5, 6
Spacing to other traces	4 W–5 W mils	Figure 11-4	--
Line width	7.0 mils	Figure 11-4	8
System board Impedance—Differential	100 Ω ± 15%	—	9
System board Impedance—odd mode	50 Ω ± 15%	—	10
Processor routing length— L1, L1': Clock driver to Rs	0.5 inch max	Figure 11-2	14
Processor routing length— L2, L2': Rs to RS-RT node	0–0.2 inch	Figure 11-2	14
Processor routing length— L3, L3': RS-RT node to Rt	0–0.2 inch	Figure 11-2	14
Processor routing length— L4, L4': RS-RT node to Load	2–9 inch	Figure 11-2	
MCH routing length— L1, L1': Clock Driver to Rs	0.5 inch max	Figure 11-2	14
MCH routing length— L2, L2': Rs to RS-RT node	0–0.2 inch	Figure 11-2	14
MCH routing length— L3, L3': RS-RT node to Rt	0–0.2 inch	Figure 11-2	14
MCH routing length— L4, L4': RS-RT node to Load	2–9 inches	Figure 11-2	
Clock driver to Processor and clock driver to Chipset length matching.	400 mils—600 mils	Figure 11-2	7,11
BCLK0—BCLK1 length matching	± 10 mils	Figure 11-2	—
Rs Series termination value	33 Ω ± 5%	Figure 11-2	12
Rt Shunt termination value	49.9 Ω ± 5% (for 50 Ω impedance)	Figure 11-2	13

NOTES:

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers, and are routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this will degrade the noise rejection of the network.

7. The clock driver to MCH trace length must be greater than the clock driver to processor socket trace length. This accounts for delay through the processor socket.
8. Set the line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack-up.
9. The differential impedance of each clock pair is approximately 2*Z single-ended*(1—2*Kb), where Kb is the backwards crosstalk coefficient. Kb is very small for the recommended trace spacing, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
10. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
11. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor.
12. Rs values between 20–33 Ω have been shown to be effective.
13. Rt shunt termination value should match the system board impedance.
14. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.

BCLK General Routing Guidelines

- When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. A via that is placed in one half of a differential pair must be matched by a via in the other half of the differential pair. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the V_{SS} reference plane only.

Figure 11-3. Clock Skew as Measured from Agent to Agent

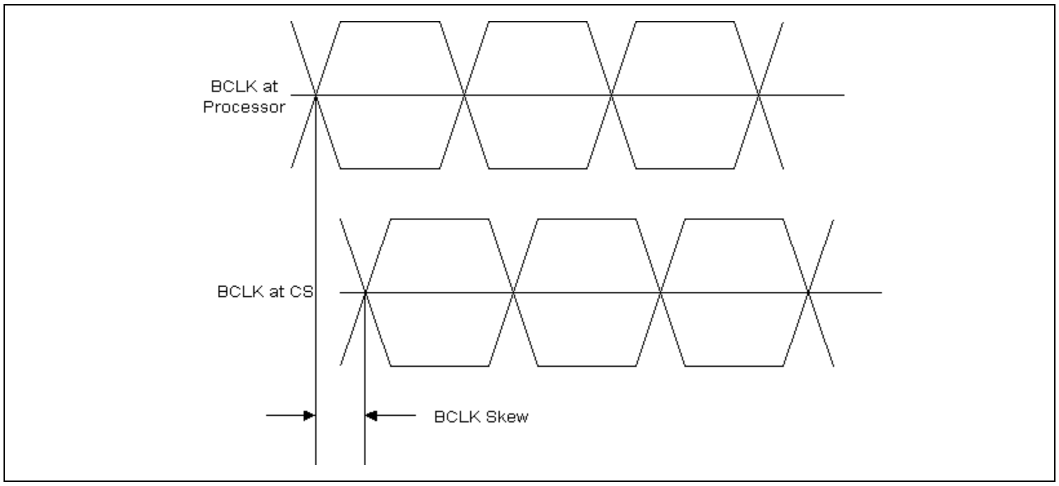
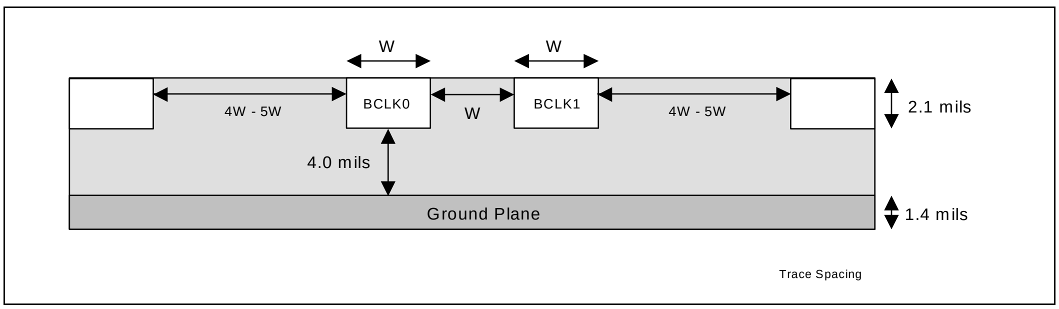


Figure 11-4. Trace Spacing



11.2.2 CLK66 Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH and the ICH2. If an AGP device is placed down on the motherboard, these guidelines should be used. Note that the goal is to have as little skew as possible between the clocks within this group.

Figure 11-5. Topology for CLK66

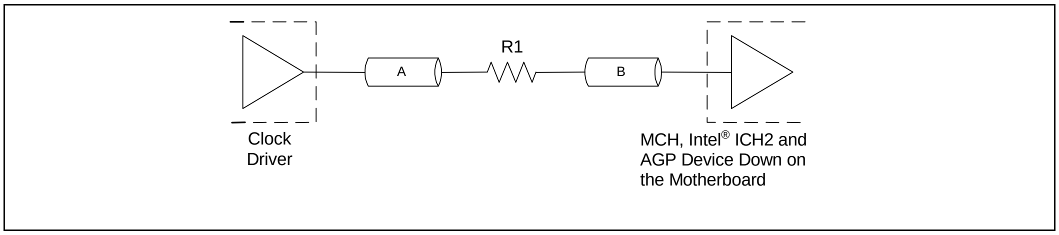


Table 11-4. CLK66 Routing Guidelines

Parameter	Routing Guidelines
Topology	Point-to-Point
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length–A	0.00 inch to 0.50 inch
Trace Length–B	4.00 inches to 8.50 inches
CLK66 Total Length (A+B)	Matched to ± 100 mils of each other
Resistor	R1 = 33 Ω ± 5%

11.2.3 AGPCLK Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the AGP device. Use these guidelines when routing to an AGP connector.

Figure 11-6. Topology for AGPCLK to AGP Connector

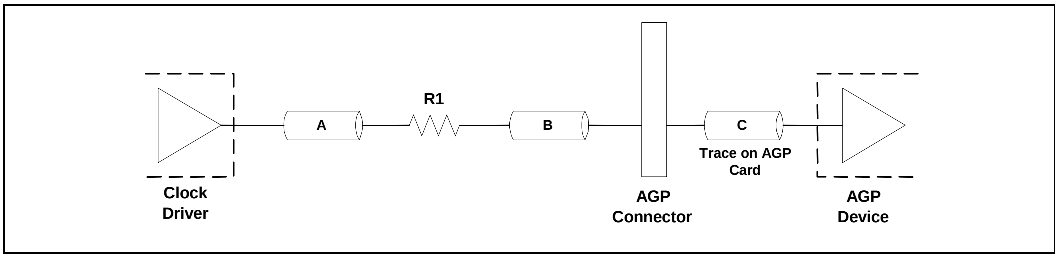


Table 11-5. AGPCLK Routing Guidelines

Parameter	Routing Guidelines
Topology	Point-to-Point
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length—A	0.00 inch to 0.50 inch
Trace Length—B	(CLK66 Trace B) – 4 inches
Trace Length—C	Trace length on AGP add-in card
AGPCLK Total Length (A+B)	Must be matched to ± 100 mils of CLK66 Total Length
Resistor	R1 = 33 Ω ± 5%

11.2.4 33 MHz Clock Group

The driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the ICH2, FWH, Glue Chip, SIO, and all PCI devices. The skew between these clocks at their respective devices must be less than 2 ns.

Figure 11-7. Topology for CLK33 to Intel® ICH2

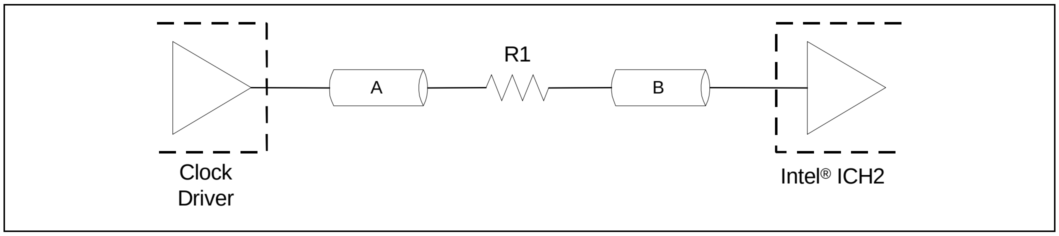


Figure 11-8. Topology for CLK33 to SIO, Glue Chip, FWH, and PCI Device Down on the Motherboard

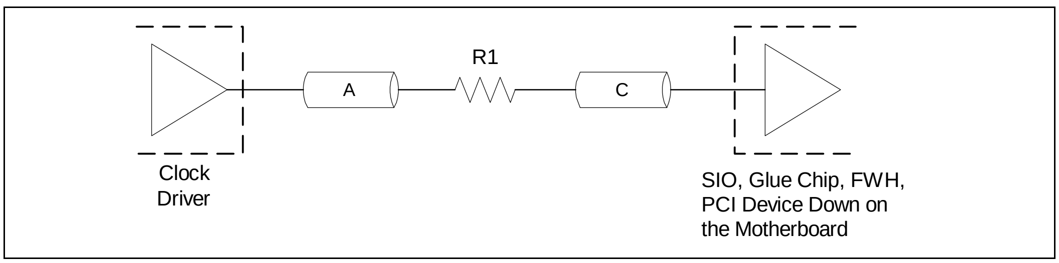


Figure 11-9. Topology for PCICLK to PCI Connector

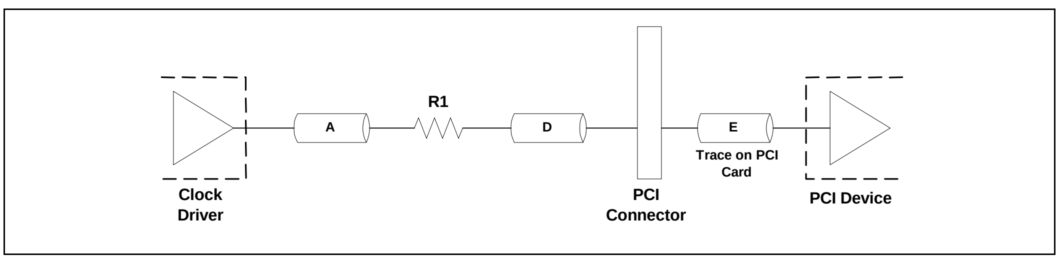


Table 11-6. 33 MHz Clock Routing Guidelines

Parameter	Routing Guidelines
Topology	Point-to-point
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length—A	0.0 inch to 0.50 inch
Total Length (A+B)	Must be matched to ± 100 mils of CLK66 Total Length. See Note 1
Total Length (A+C)	See Note 2
Total Length (A+D+E)	See Note 2
Resistor	R1 = 33 Ω ± 5%

NOTES:

1. The 33 MHz clock **must always** lag the 66 MHz clock at the ICH2 by 1–4 ns. The clock generator guarantees this phase offset. There is no need to intentionally add trace length to the 33 MHz clock. This length-matching requirement applies to the 33 MHz ICH2 clock only.
2. There should be no more than 7.5 inches of total mismatch between any two clocks in this group. If routing to a PCI connector, a 2.6 inches max trace length is assumed on the PCI card. These 2.6 inches must be included in the 7.5-inch total mismatch.

11.2.5 CLK14 Clock Group

The driver is the clock synthesizer 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the ICH2 and SIO. Note that the clocks within this group should have minimal skew (~ 0) between each other. However, each clock in this group is asynchronous to clocks in other groups.

Figure 11-10. Topology for CLK14

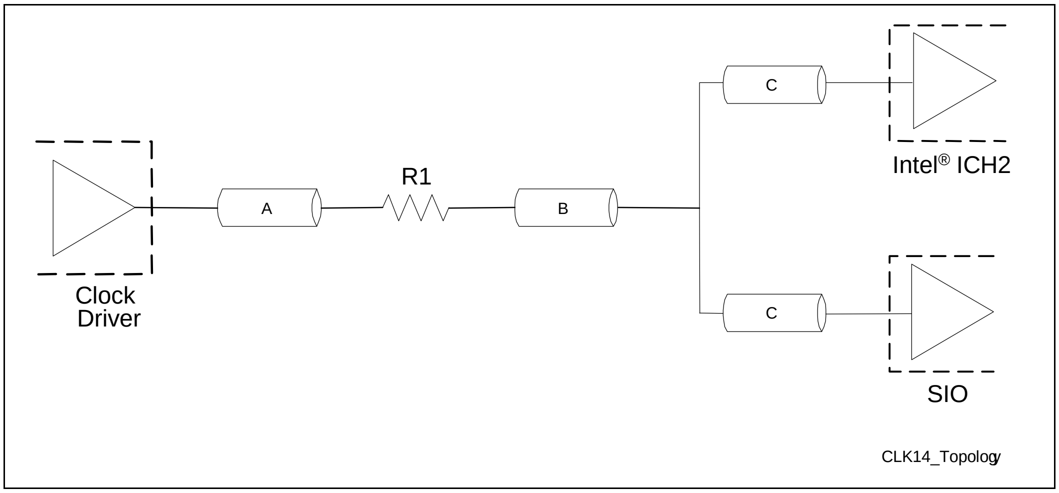


Table 11-7. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Topology	Balanced T topology
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	10 mils
Spacing to other traces	10 mils
Trace Length—A	0.00 inch to 0.50 inch
Trace Length—B	0.00 inch to 12 inches
Trace Length—C	0.00 inch to 6 inches
CLK14 Total Length (A+B+C)	Matched to ± 0.5 inch of each other
Resistor	R1 = 33 Ω ± 5%

11.2.6 USBCLK Clock Group

The driver is the clock synthesizer USB clock output buffer, and the receiver is the USB clock input buffer at the ICH2. Note that this clock is asynchronous to other clocks on the board.

Figure 11-11. Topology for USB_CLOCK

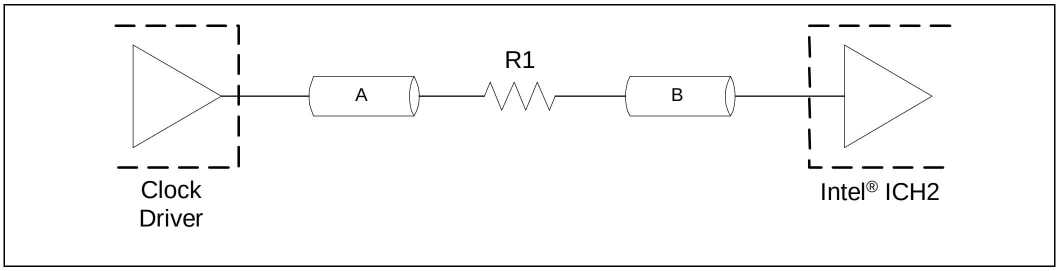


Table 11-8. USBCLK Routing Guidelines

Parameter	Routing Guidelines
Topology	Point-to-Point
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%
Trace Width	5 mils
Spacing to other traces	15 mils
Trace Length—A	0.00 inch —0.50 inch
Trace Length—B	3.00 inches—12.00 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	None—USBCLK is asynchronous to any other clock on the board

11.3 Clock Driver Decoupling

The decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- One 10 µF bulk decoupling capacitor in a 1206 package placed close to the V_{DD} generation circuitry.
- Six 0.1 µF high-frequency decoupling capacitors in a 0603 package placed close to the V_{DD} pins on the clock driver.
- Three 0.01 µF high-frequency decoupling capacitors in a 0603 package placed close to the V_{DD}A pins on the Clock driver.
- One 10 µF bulk decoupling capacitor in a 1206 package placed close to the V_{DDA} generation circuitry.

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12 Platform Power Guidelines

This chapter presents the power guidelines for an 845 chipset for SDR platform. Power delivery architecture, power supply decoupling, power sequencing, and power management are covered. Table 12-1 defines some of the terms used in this chapter.

Table 12-1. Power Terminology

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
Full-power Operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant state) state.
Suspend Operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3), and Soft-off (S5).
Core Power Rail	A power rail that is only on during full-power operation. These power rails are on when the PS_ON signal is asserted to the ATX power supply.
Standby Power Rail	A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times when the power supply is plugged into AC power. The only standby power rail that is distributed directly from the ATX power supply is $5V_{SB}$ (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived Power Rail	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, $3.3V_{SB}$ is usually derived on the motherboard from $5V_{SB}$ using a voltage regulator.
Dual Power Rail	A dual power rail is derived from different rails at different times depending on the power state of the system. Usually a dual power rail is derived from a standby supply during suspend operation, and derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

12.1 Power Delivery Map

Figure 12-1 shows the power delivery architecture for an example 845 chipset platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the *suspend-to-RAM* (STR) state.

During STR, only the necessary devices are powered. These devices include main memory, the ICH2 resume well, PCI wake devices (via 3.3 Vaux), AC ’97, and optionally USB. (USB can be powered only if sufficient standby power is available.) To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in *suspend* and in *full power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions in this design guide are only examples. Many power distribution methods achieve similar results. When deviating from these examples, it is critical to consider the effect of a change. For additional thermal characteristics, refer to the *Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet*.

Figure 12-1. Intel® 845 Chipset Platform Using PC133 SDRAM System Memory Power Delivery Map

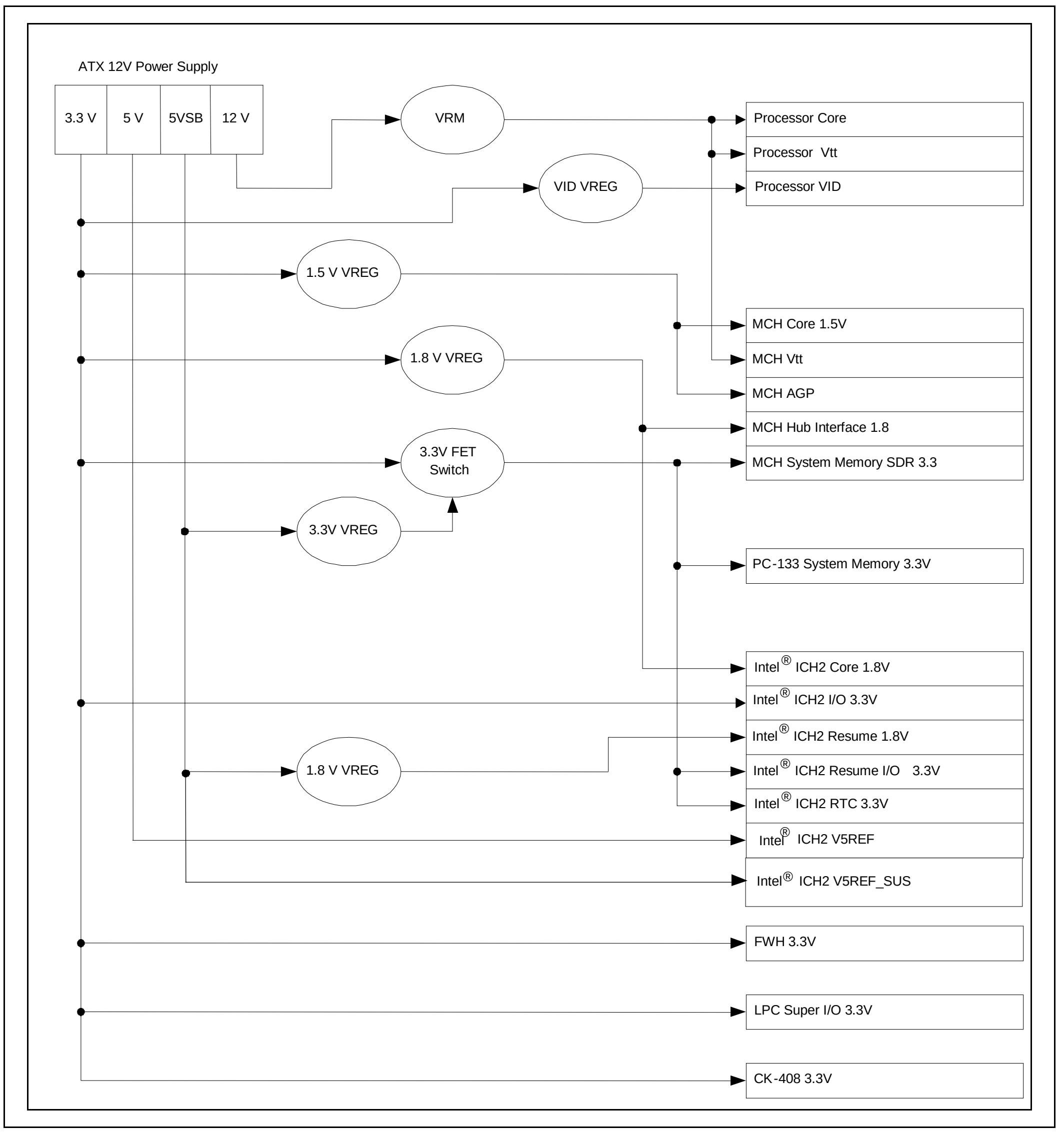
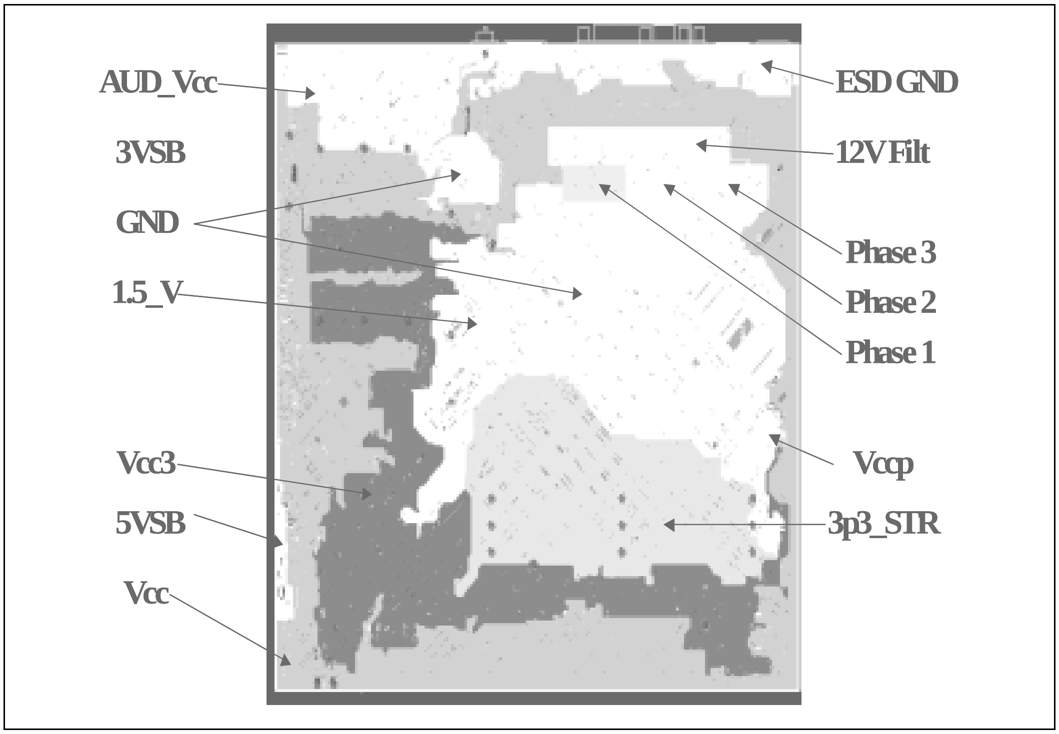


Figure 12-2. Example Platform Power Delivery—Intel® 845 Chipset Using PC133 SDRAM



12.2 MCH Power Delivery

There are no MCH power sequencing requirements. All MCH power rails should be stable before deasserting reset, but the power can be brought up in any order desired. Good design practice would have all power rails come up as close in time as practical.

12.2.1 MCH PLL Power Delivery

V_{CCA1} and V_{SSA1}, and V_{CCA0} and V_{SSA0} are power sources required by the MCH's PLL clock generators.

Figure 12-3. Intel® 845 Chipset PLL0 Filter

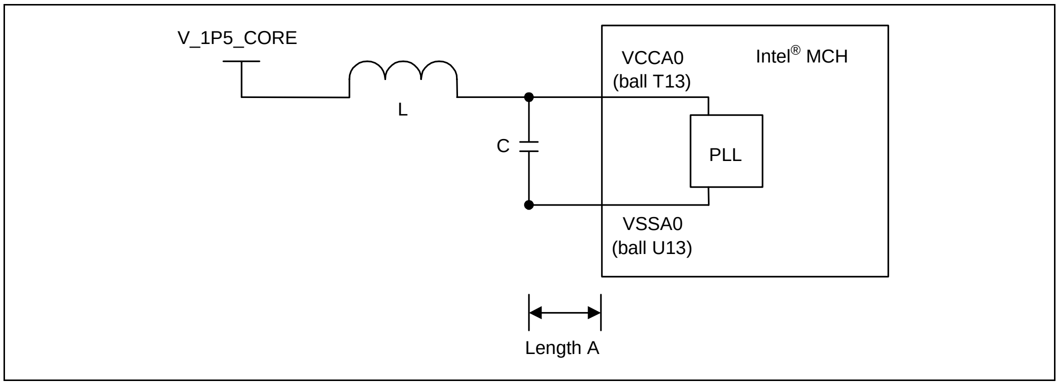


Table 12-2. PLL0 Filter Routing Guidelines

Parameter	Routing Guidelines
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length—A	1.5 inches
Capacitor—C	33 µF
Inductor—L	4.7 µH

Figure 12-4. Intel® 845 Chipset PLL1 Filter

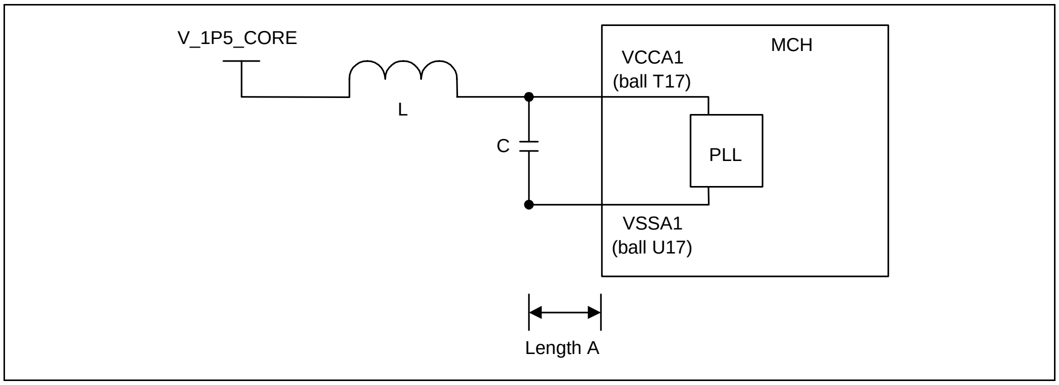


Table 12-3. PLL1 Routing Guidelines

Parameter	Routing Guidelines
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length—A	1.5 inches
Capacitor—C	33 µF
Inductor—L	4.7 µH

Table 12-4. Recommended Inductor Components for MCH PLL Filter

Value	Tolerance	SRF	Rated I	DCR
4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1Ω max)
4.7 µH	10%	47 MHz	30 mA	0.7 Ω (± 50%)
4.7 µH	30%	35 MHz	30 mA	0.3 Ω max

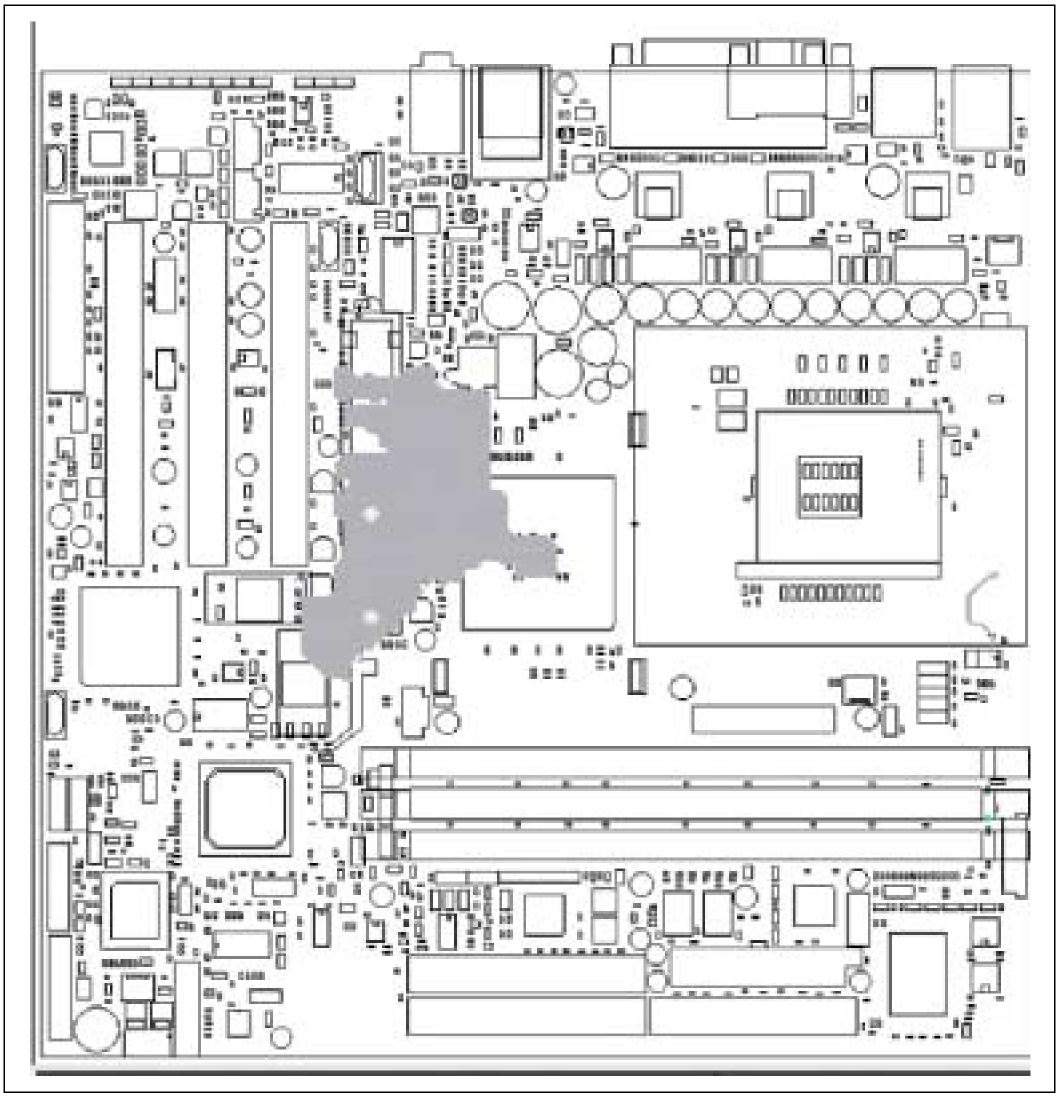
Table 12-5. Recommended Capacitor Components for MCH PLL Filter

Value	ESL	ESR
33 µF	2.5 nH	0.225 Ω
33 µF	2.5 nH	0.2 Ω

12.2.2 MCH 1.5 V Power Delivery

The MCH core and AGP I/O is supplied by 1.5 V. Adequate high-frequency decoupling is needed to ensure one does not adversely impact the other.

Figure 12-5. 1.5 V Power Plane—Board View



12.2.3 MCH 1.5 V Decoupling

The following minimum decoupling components are recommended:

- Six, 0.1 µF ceramic capacitor, 603 body type, X7R dielectric
- Two, 10 µF ceramic capacitor, 1206 body type, X7R dielectric
- Two, 100 µF electrolytic capacitor

It is recommended that low ESL ceramic capacitors, such as 0603 body types, X7R dielectric, be used. The designer should evenly distribute placement of decoupling capacitors among the AGP interface signal field, and place them as close to the MCH as possible (no further than 0.25 inch from the MCH V_{CC1_5} ball in the AGP ball field). Figure 12-6 shows an example placement of 1.5 V decoupling capacitors.

Figure 12-6. MCH 1.5 V Core and 1.5 V AGP I/O Decoupling Placement

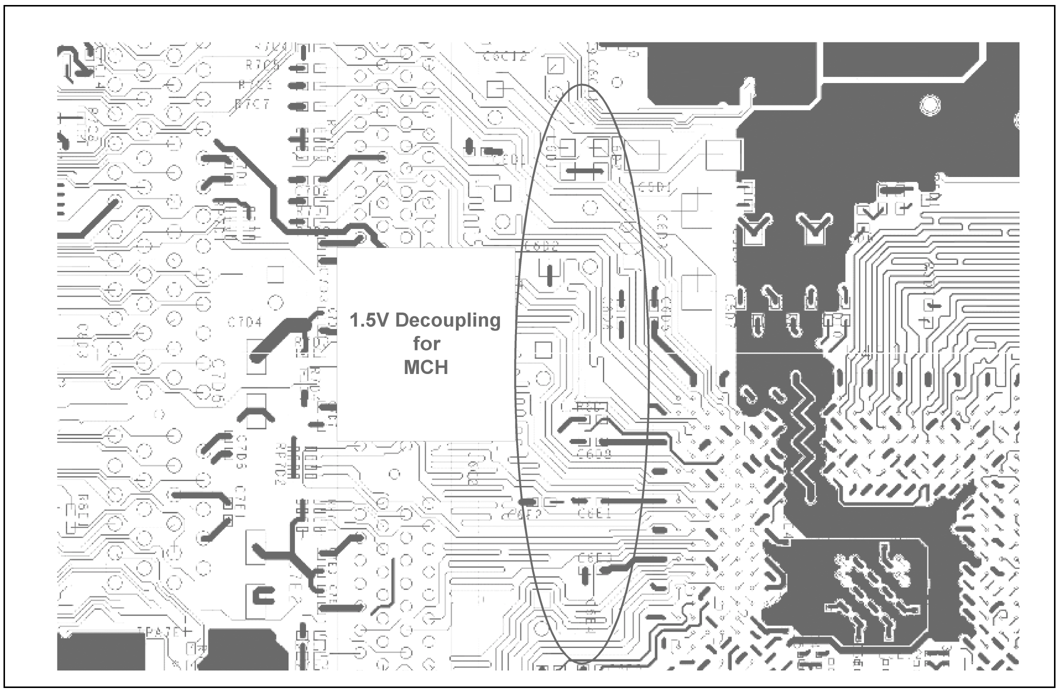
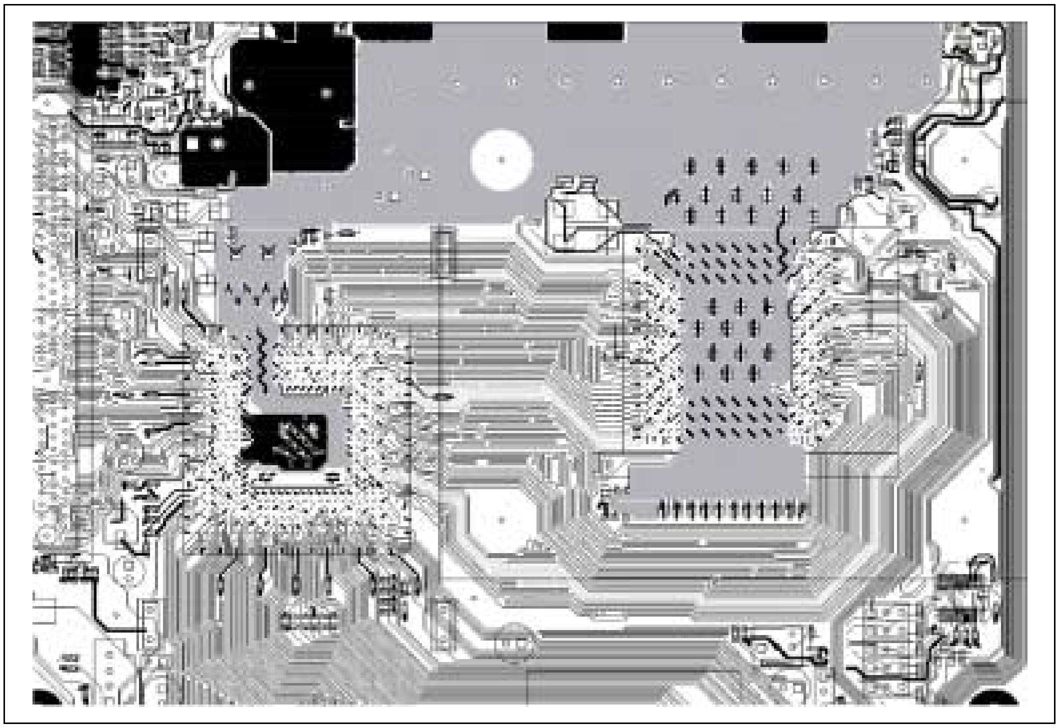


Figure 12-7. V_{TT} Power Plane—Processor and MCH



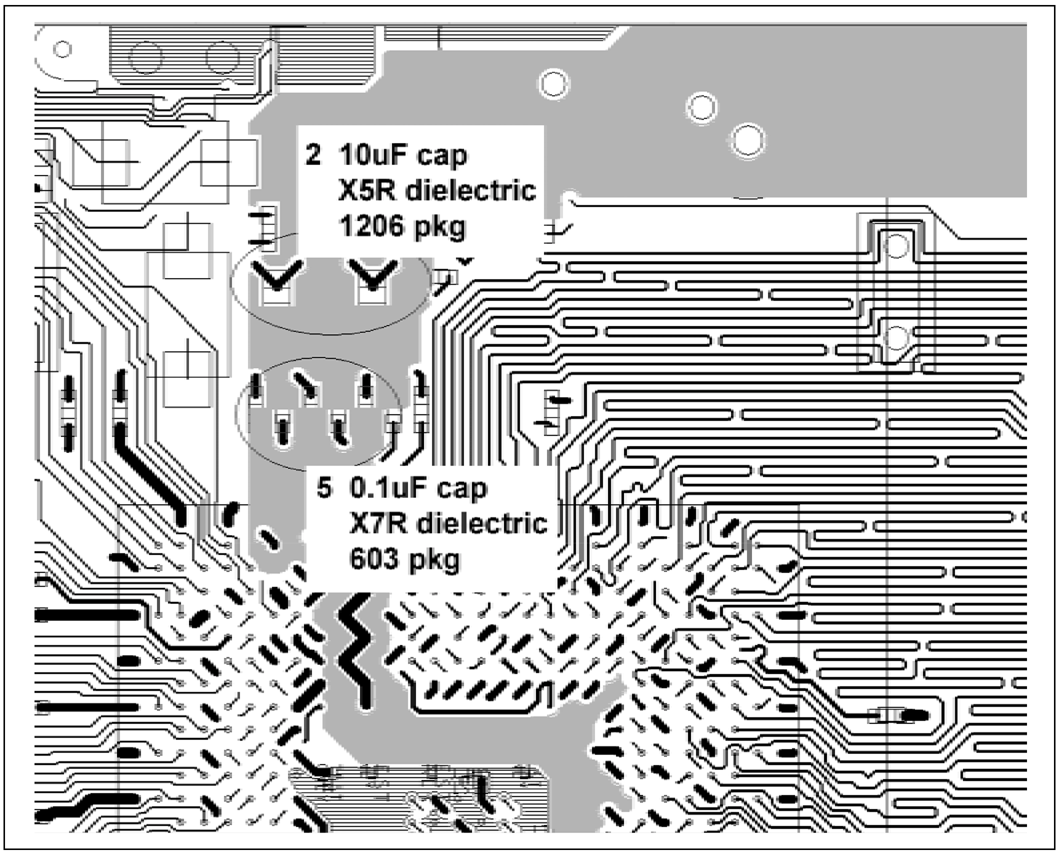
12.2.4 MCH V_{TT} Decoupling

The following minimum decoupling components are recommended:

- Two, 10 µF ceramic capacitor, 1206 body type, X5R dielectric
- Five, 0.1 µF ceramic capacitor, 1206 type, X7R dielectric

The alternating polarity of the five, 0.1 µF capacitors minimizes the area reduction caused by the vias.

Figure 12-8. V_{TT} Power Plane at MCH—V_{TT} Decoupling at MCH



12.3 Intel® ICH2 Power Delivery

Figure 12-9. Power Plane Split Example (Layer 2)

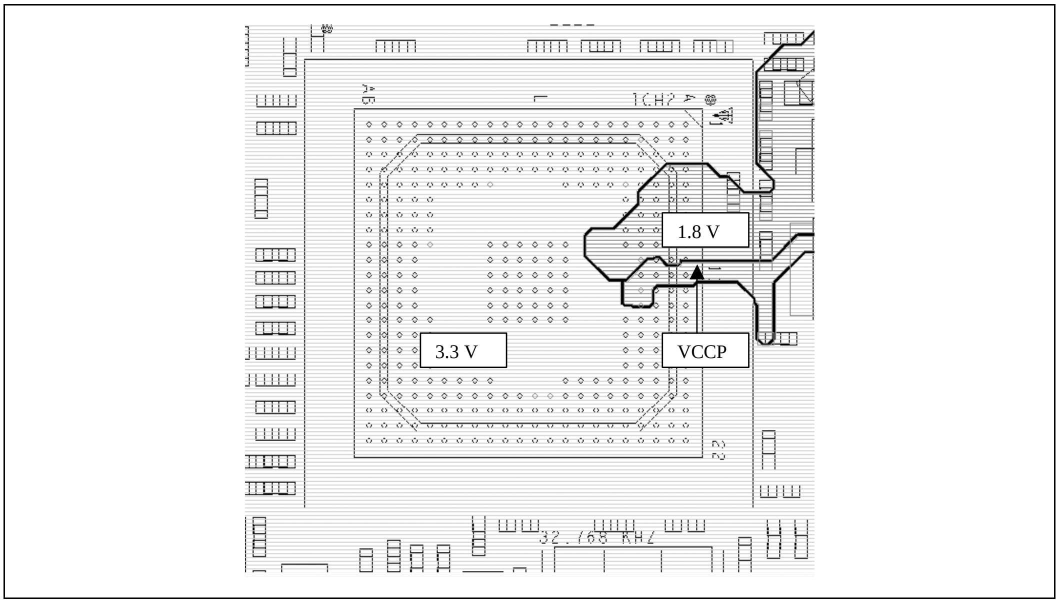
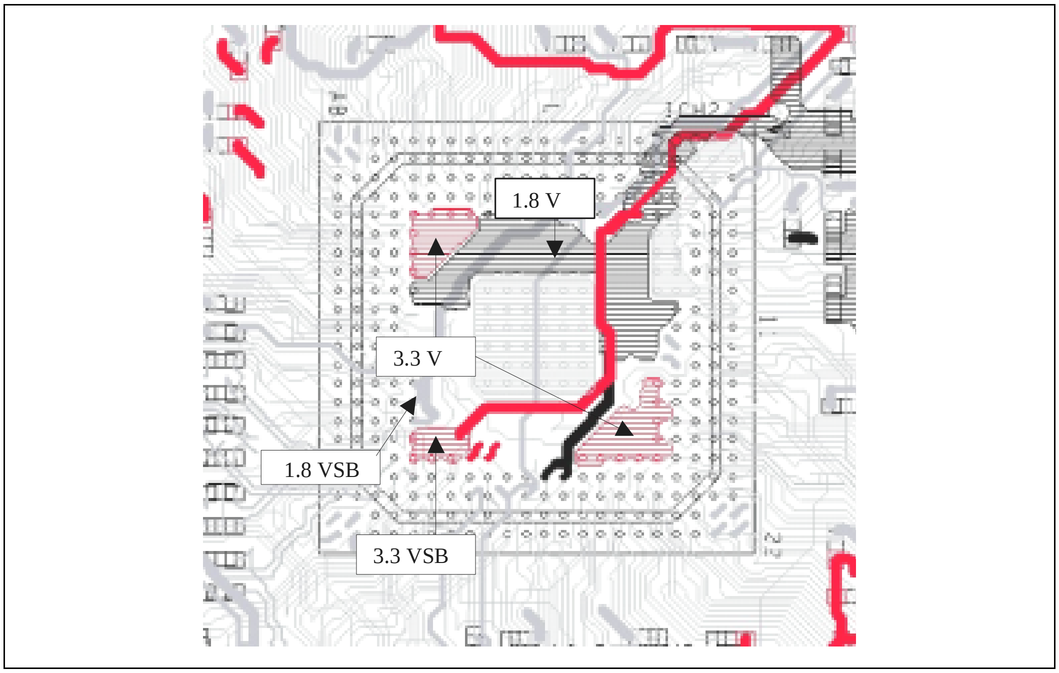


Figure 12-10. Power Plane Split Example (Layer 1)



12.3.1 1.8 V / 3.3 V Power Sequencing

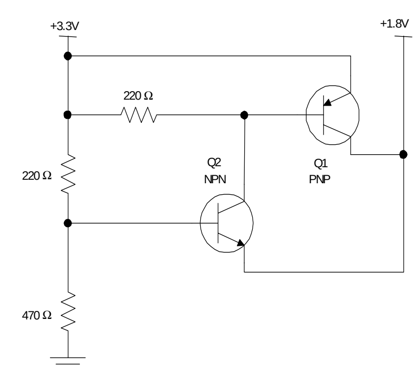
The ICH2 has two pairs of associated 1.8 V and 3.3 V supplies; these are {V_{CC1_8}, V_{CC3_3}}, and {V_{ccSus1_8}, V_{ccSus3_3}}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment because the 1.8 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violating this “2 V Rule” is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.8 V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as “Input-only” actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

Figure 12-11 is an example power-on sequencing circuit that ensures that the 2 V Rule is not violated. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

Figure 12-11. Example 1.8 V/3.3 V Power Sequencing Circuit



When analyzing systems that may be “marginally compliant” to the 2 V Rule, pay close attention to the behavior of the ICH2’s RSMRST# and PWROK signals because these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC-well and the resume wells.
- PWROK controls isolation between the resume wells and main wells.

Caution: If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging internal currents.

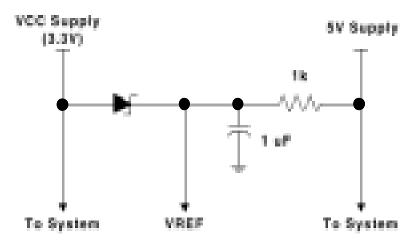
12.3.2 3.3 V / V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before V_{CC3_3}, or after V_{CC3_3}within 0.7 V. Also, V5REF must power down after V_{CC3_3}, or before V_{CC3_3}within 0.7 V. The rule must be followed to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the V_{CC3_3} rail. Figure 12-12 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the standby rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5; and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_SUS will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend, the only signals that are 5 V tolerant capable are USB OC[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5 V_Always/5V_AUX. If OC[3:0]# is needed during suspend and 5 V tolerance is required, then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5 V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

Figure 12-12. Example 3.3 V / V5REF Sequencing Circuitry



12.3.3 ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH2 sets the PWROK_FLR bit (ICH2 GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at offset A2h). If this bit is set upon resume from S3 power-down, the system will reboot, and control of the system will not be given to the program that is running when the S3 state is entered. System designers should ensure that PWROK signal designs are glitch free.

12.3.4 Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH2 integrates 16 ms debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH2 to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PS_POK logic must be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply while making sure that the input to the ICH2 is at the 3 V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed V_{CC} (RTC).
- It is recommended that 3.3 V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from V_{CC5}.
- The PWROK signal to the chipset is a 3 V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V using a 330 Ω resistor.
- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, make sure that the driver (RS232 transceiver) of the RI# signal is powered when the ICH2 suspend well is powered. This can be achieved by powering the serial port transceiver from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH2 must be inverted then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is Low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

12.4 CK408 Power Delivery

Differential Routing

- The host clock pairs must be routed differentially and on the same physical routing layer.
- **Do not** split the two halves of a differential clock pair. Route them referenced to ground for the entire length.
- The differential clock must have no more than two via transitions.

Isolation

- Special care must be taken to provide a quiet $V_{DD}A$ supply to the Ref V_{DD}, $V_{DD}A$, and the 48 MHz V_{DD}.
- These $V_{DD}A$ signals are especially sensitive to switching noise induced by the other V_{DD}s on the clock chip.
- The $V_{DD}A$ signals are also sensitive to switching noise generated elsewhere in the system such as CPU VRM. The LC Pie filter should be designed to provide the best reasonable isolation.

Referencing

- Ground referencing is strongly recommended for all platform clocks.
- Motherboard layer transitions and power plane split crossing must be kept to a minimum.

Flooding

Option 1 (Signal-Power-Ground-Signal)

For the stack-up shown in Figure 3-2 (Signal-Power-Ground-Signal), it is strongly recommended that:

- A solid ground flood be placed on layer 1 (signal layer) inside the part pads.
- A solid 3.3 V Power plane be present on layer 2 (power layer).
- A solid ground plane be present on layer 3 (ground layer).
- Signals after termination should via to the backside to be ground referenced.
- Here the host clocks will be power referenced for a small portion of time while they route from CK408 pin to their transition via.
- Keep this MB length as short as possible.

Option 2 (Signal-Ground-Power-Signal)

If using a stack-up such as **Signal-Ground-Power-Signal**, It is **strongly recommended** that:

- A ground flood be present on layer1 (signal layer) inside the part pads.
- A solid ground plane be present on layer 2 (ground layer).
- A solid 3.3 V Power plane be present on layer 3 (power layer).
- Signals after termination should remain on the top layer to be ground referenced (via to the front side).

Decoupling

- For **all** power connections to planes, decoupling capacitors, and vias, the **maximum** trace width allowable and shortest possible lengths should be used to ensure the lowest possible inductance.
- The decoupling capacitors should be connected as shown in Figure 12-14, taking care to connect the V_{DD} pins directly to the V_{DD} side of the capacitors.
- The V_{SS} pins should not be connected directly to the V_{SS} side of the capacitors. They should be connected to the ground flood under the part that is via'd to the ground plane to avoid V_{DD} glitches propagating out and getting coupled through the decoupling capacitors to the V_{SS} pins. This method has been shown to provide the best clock performance.
- The ground flood should be via'd through to the ground plane with no less than 12–16 vias under the part. It should be well connected.
- For all power connections, heavy duty and/or dual vias should be used.
- It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power and ground planes.
- V_{DDA} should be generated by using an LC filter. This V_{DDA} should be connected to the V_{DD} side of the three capacitors that require it using a hefty trace on the top layer. This trace should be routed from the LC filter.

12.4.1 CK408 Power Sequencing

Platforms need proper power sequencing of the CK408 with respect to the voltage regulators, processor, and MCH. Figure 12-13 is a schematic showing the relationship between the V_{CC}VID voltage regulator, the V_{CCP} voltage regulator, CK408, processor, and MCH.

Figure 12-13. CK408 Schematic

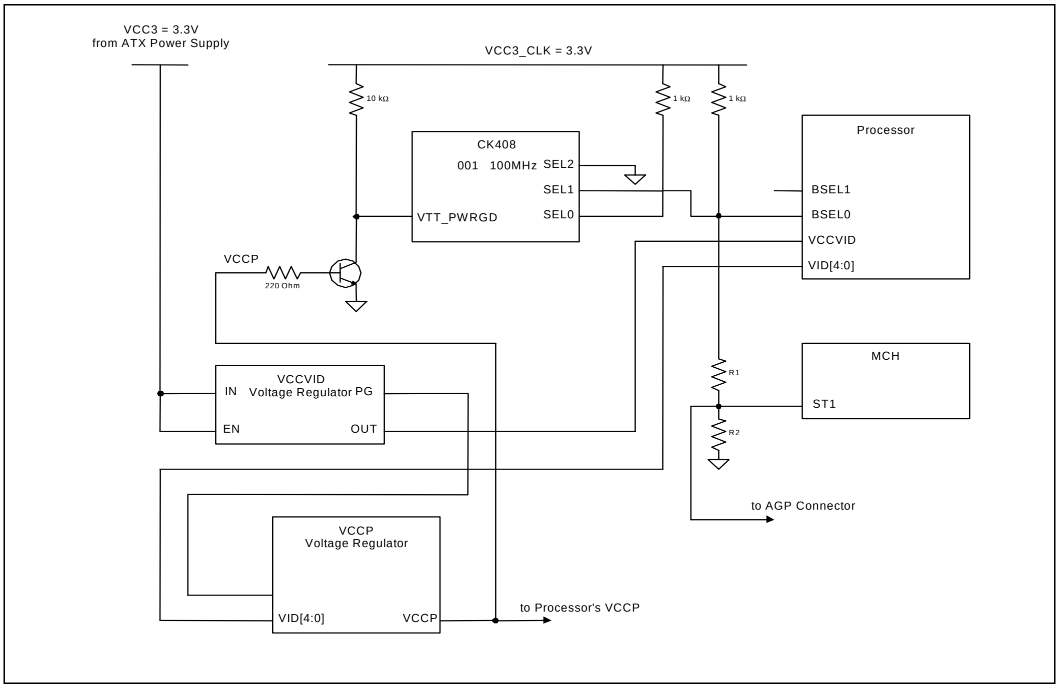


Table 12-6. PLL1 Routing Guidelines

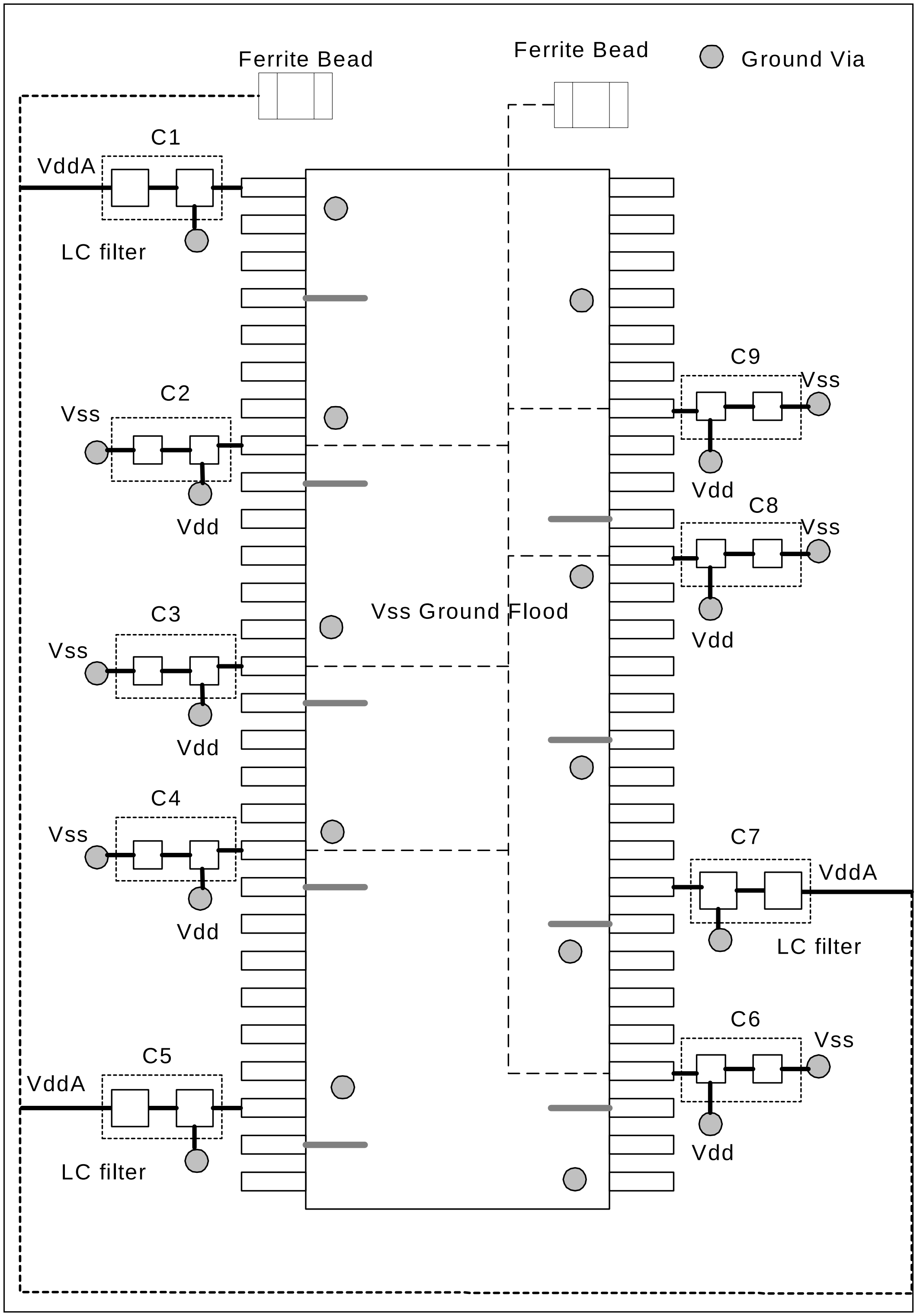
Parameter	Routing Guidelines
Resistor—R1	Not populated
Resistor—R2	Not populated

12.4.2 CK408 Decoupling

The decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- One 10 µF bulk-decoupling capacitor in a 1206 package placed close to the V_{DD} generation circuitry.
- Six 0.1 µF high-frequency decoupling capacitors in a 0603 package placed close to the V_{DD} pins on the clock driver.
- Three 0.01 µF high-frequency decoupling capacitors in a 0603 package placed close to the V_{DD}A pins on the clock driver.
- One 10 µF bulk decoupling capacitor in a 1206 package placed close to the V_{DD}A generation circuitry.

Figure 12-14. Decoupling Capacitors Placement and Connectivity



12.5 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations of both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. Refer to the *Intel® 845 Chipset Thermal and Mechanical Design Guidelines* and the *Intel® 845 Chipset: Intel® 82845 Memory Controller Hub (MCH) Datasheet* for additional thermal package characteristics.

Table 12-7. Component Thermal Design Power

Component	Power Consumption
MCH (PC-133 SDRAM)	4.1 W ± 15 %
ICH2	1.5 W ± 15%

12.6 Power_Supply PS_ON Considerations

If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and will never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with the affected power supply.

The ATX specification does not specify a minimum pulse width on PS_ON deassertion, which means that power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Because of variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this problem.

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13 Platform Mechanical Guidelines

13.1 MCH Retention Mechanism and Keep-Outs

Figure 13-1 shows the motherboard keep-out dimensions intended for the reference thermal / mechanical components for the 845 chipset.

Figure 13-1. MCH Retention Mechanism and Keep-Out Drawing

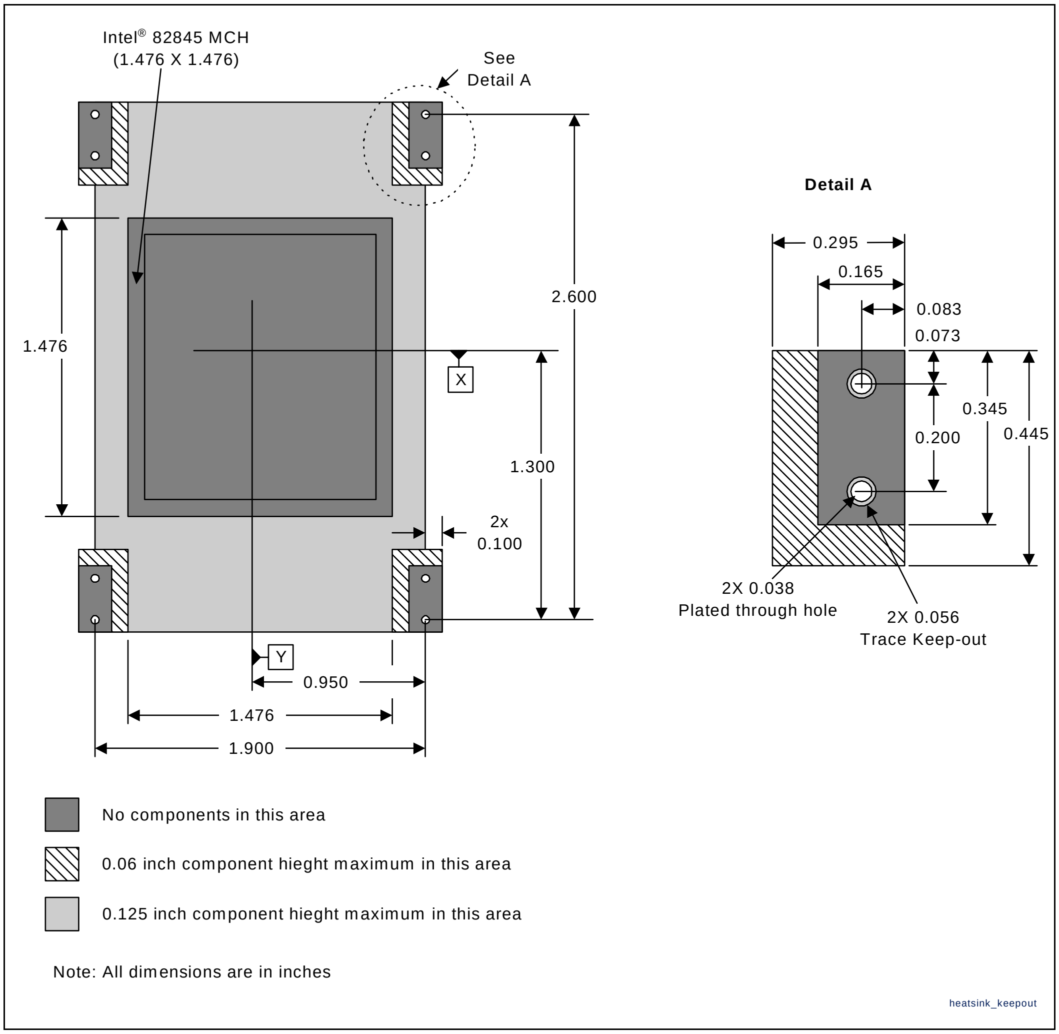
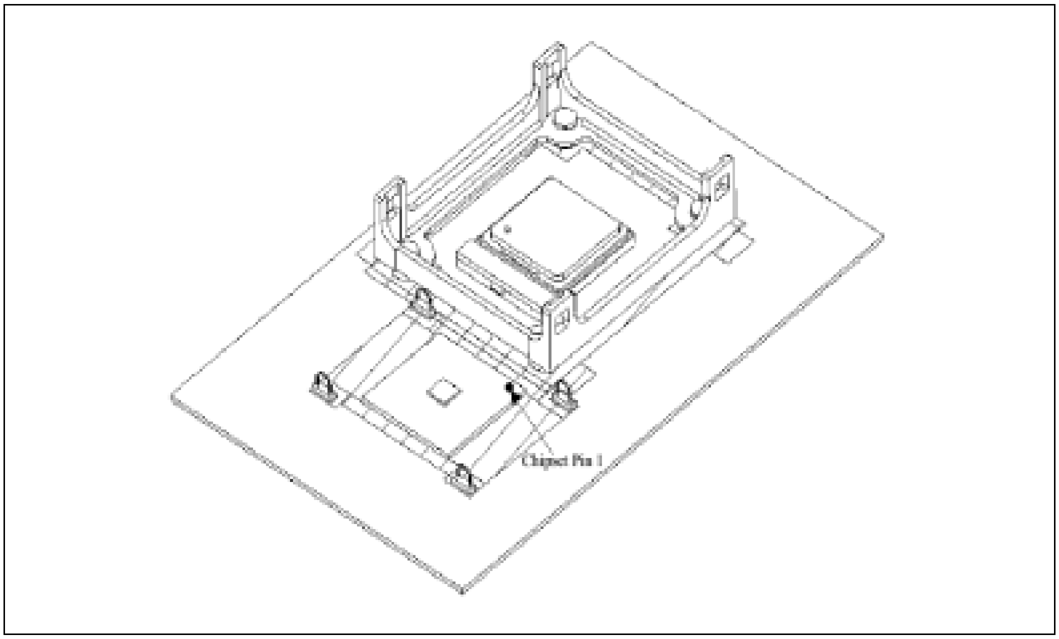


Figure 13-2 shows a typical orientation of the 845 chipset keep-out relative to the Pentium 4 processor. The 845 chipset mechanical reference design assumes this orientation, or a rotation of 180 degrees of the chipset relative to the orientation shown in this figure. Intel will not qualify other orientations.

Figure 13-2. Typical Orientation of the Chipset Relative to the Processor



13.2 Intel® Boxed Processor Mechanical Keep-Outs

Verify Intel's Boxed Processor mechanical keep-outs are marked and visible during board layout. This keep-out zone should be considered during chassis selection.

14 Schematic Checklist

14.1 Host Interface

Signal	Description	✓
	Processor / MCH Signals	
A[31:3]#	• Connect to HA[31:3] pins on MCH.	
ADS#	• Connect to the associated pin on the MCH.	
ADSTB[1:0]#	• Connect to HADSTB[1:0]# pins on MCH.	
BNR#	• Connect to the associated pin on the MCH.	
BPRI#	• Connect to the associated pin on the MCH.	
BR0#	• Connect to the associated pin on the MCH. • Terminate to V_{CC_CPU} through a 51 Ω ± 5% resistor near the processor.	
RESET#	• Connect to the associated pin on the MCH. • Terminate to V_{CC_CPU} through a 51 Ω ± 5% resistor near the processor.	
D[63:0]#	• Connect to HD[63:0] pins on MCH.	
DBI[3:0]#	• Connect to the associated pin on the MCH.	
DBSY#	• Connect to the associated pin on the MCH.	
DEFER#	• Connect to the associated pin on the MCH.	
DRDY#	• Connect to the associated pin on the MCH.	
DSTBN[3:0]#	• Connect to HDSTBN[3:0]# pins on MCH.	
DSTBP[3:0]#	• Connect to HDSTBP[3:0]# pins on MCH.	
HIT#	• Connect to the associated pin on the MCH.	
HITM#	• Connect to the associated pin on the MCH.	
LOCK#	• Connect to HLOCK# pin on MCH.	
REQ[4:0]#	• Connect to HREQ[4:0]# pins on MCH.	
RS[2:0]#	• Connect to the associated pin on the MCH.	
TRDY#	• Connect to HTRDY# pin on MCH.	
	Processor/ Intel® ICH2 Signals	
A20M#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
CPUSLP#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
FERR#	• Connect to the associated pin on the ICH2. • Terminate to V_{CC_CPU} through a 62 Ω ± 5% resistor near the processor.	

Signal	Description	✓
IGNNE#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
INIT#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required). • A voltage translator is required for FWH. • Connect to Firmware Hub.	
INTR	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
LINT[1:0]	• LINT1 connects to ICH2 NMI (No extra pull-up resistors required). • LINT0 connects to ICH2 INTR (No extra pull-up resistors required).	
NMI	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
PWRGOOD	• Connects to ICH2 CPUPWRGD pin (Weak external pull-up resistor required). • Terminate to V_{CC_CPU} through a 300 Ω ± 5% resistor.	
SLP#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
SMI#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required).	
STPCLK#	• Connect to the associated pin on the ICH2 (No extra pull-up resistors required)	
Processor Only Signals		
A[35:32]#	• No Connect.	
AP[1:0]#	• No Connect.	
BCLK[1:0]	• Connect to CK408. • Connect 20—33 Ω series resistors to each clock signal. • Connect a 49.9 Ω ± 1% shunt source termination (Rt) resistor to GND for each signal on the processor side of the series resistor (50 Ω motherboard impedance).	
BPM[5:0]#	• These signals should be terminated with a 51 Ω ± 5% resistor to V_{CC_CPU} near the processor. If a debug port is implemented termination is required near the debug port as well. Refer to the *ITP700 Debug Port Design Guide* for further information.	
BINIT#	• No Connect.	
BSEL[1:0]	• Connect to CK408. • Terminate to CK408 3.3 V supply through a 1 kΩ resistor.	
COMP[1:0]	• Terminate to GND through a 51.1 Ω ± 1% resistor. • Minimize the distance from termination resistor and processor pin.	
DBR#	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
DP[3:0]#	• No Connect.	
IERR#	• Terminate to V_{CC_CPU} through a 62 Ω ± 5% resistor near the processor.	

Signal	Description	✓
GTLREF[3:0]	• Terminate to V_{CC_CPU} through a 49.9 Ω ± 1% resistor. • Terminate to GND through a 100 Ω ± 1% resistor. • Should be 2/3 V_{CC_CPU}.	
ITP_CLK0	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
ITP_CLK1	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
MCERR#	• No Connect.	
PROCHOT#	• Terminate to V_{CC_CPU} though a 62 Ω ± 1% resistor near the processor.	
RSP#	• No Connect.	
SKTOCC#	• Connect to Glue Chip / Discrete Logic (If pin is used).	
TCK	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
TDI	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
TDO	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
TESTHI	• Refer to Section 4.3.1.11	
THERMTRIP#	• Terminate to V_{CC_CPU} through a 62 Ω ± 5% resistor near the processor.	
THERMDA	• Connect to thermal monitor circuitry if used.	
THERMDC	• Connect to thermal monitor circuitry if used.	
TMS	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
TRST#	• Refer to the *ITP700 Debug Port Design Guide* for further information.	
VCCA	• Connect with isolated power circuitry to V_{CC_CPU}.	
VCCIOPLL	• Connect with isolated power circuitry to V_{CC_CPU}.	
VCC_SENSE	• Leave as no-connect.	
VCCVID	• Connect to 1.2 V linear regulator.	
VID[4:0]	• Connect to VR or VRM. These signals must be pulled up to 3.3 V through either 1 kΩ pull-ups on the motherboard or with internal pull-ups in the VR or VRM.	
VSSA	• Connect with isolated power circuitry to V_{CC_CPU}.	
VSS_SENSE	• Leave as no-connect.	
MCH Signals Only		
HRCOMP[1:0]	• Pull-down to GND through a 24.9Ω ±1% resistor.	
HSWNG[1:0]	• Connect voltage divider circuit to V_{TT} through a 301 Ω ± 1% pull-up resistor, and to GND through a 150 Ω ± 1% pull-down resistor. • Decouple the voltage divider with a 0.01 µF capacitor to GND.	
HVREF	• Connect voltage divider circuit to V_{CC_CPU} through a 49.9 Ω ± 1% pull-up resistor and to GND through a 100 Ω ± 1% pull-down resistor • Decouple the voltage divider with a 0.1 µF capacitor.	
VTT	• Connect to V_{CC_CPU} power supply.	

14.2 Memory Interface

14.2.1 PC133 SDR SDRAM

Signal	Description	✓
MCH/DIMM Signals		
SCAS#	• Connect to CAS# pin on each DIMM.	
SCB[7:0]	• Connect to CB[7:0] pin on each DIMM.	
SCK[11:0]	• Connect to CK pins on each DIMM per Table 5-14. • Terminate each to GND at the MCH through a 22 pF ± 5% EMI capacitor. • Terminate each to GND through a 51 Ω ± 5% resistor and a 270 pF ± 5% capacitor after the DIMMs. • SCK[11:8] are left floating on a 2-DIMM platform.	
SCKE[5:0]	• Connect to CKE pins on each DIMM per Table 5-15. • SCKE[5:4] are left floating on a 2-DIMM platform.	
SCS[11:0]#	• Connect CS# pins on each DIMM per Table 5-15. • SCS[11:8] are left floating on a 2-DIMM platform.	
SDQ[63:0]	• Connect to DQ[63:0] pins on each DIMM.	
SMA[12:0]	• Connect to MA[12:0] pins on each DIMM.	
SBS[1:0]	• Connect to BA[1:0] pins on each DIMM.	
SRAS#	• Connect to RAS# pin on each DIMM.	
SWE#	• Connect to WE# pin on each DIMM.	
VCCSM	• Connect to 3.3 V system memory power plane.	
DIMM Signals Only		
DQMB[7:0]	• Connect to GND.	
MA13	• Connect to GND.	
SA[2:0]	• Connect to 3-bit address for each DIMM. • DIMM0 = 000, DIMM1 = 001, DIMM2 = 010.	
SDA	• Connect to I^2C DATA.	
SCL	• Connect to I^2C CLOCK.	
VDD	• Connect to V_{CCSM}.	
VREF[1:0]	• No Connect.	
VSS	• Connect to GND.	
MCH Signals Only		
RDCLKO	• Connect directly to MCH RDCLKI pin.	
RDCLKIN	• See RDCLKO recommendation.	
SDREF	• Connect voltage divider circuit with R1=R2=49.9 Ω ± 1%, and decouple with a 0.1 µF capacitor to ground.	
SMRCOMP	• Connect to ground through a 20 Ω ± 1% resistor.	

14.3 AGP Interface

Signal	Description	✓
	MCH/ Connector Signals	
AD_STB[1:0]	• Connect together. • Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
AD_STB[1:0]#	• Connect together. • Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_AD[31:0]	• Connect together.	
G_C/BE[3:0]#	• Connect together.	
G_DEVSEL#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_FRAME#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_GNT#	• Connect together. • Terminate to V_{DDQ} = 1.5 V through a pull-up resistor with a value between 4 kΩ and 16 kΩ. 6.8 kΩ resistor value recommended.	
G_IRDY#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_PAR	• Connect together.	
G_PIPE#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_REQ#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_STOP#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
G_TRDY#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
INTA#	• Connect together. • Terminate to 3.3 V through a pull-up resistor.	
INTB#	• Connect together. • Terminate to 3.3 V through a pull-up resistor.	
PIPE#	• Connect together.	
RBF#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	

Signal	Description	✓
SBA[7:0]	• Connect together.	
SB_STB	• Connect together. • Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
SB_STB#	• Connect together. • Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated, 6.8 kΩ resistor value recommended).	
SBA[7:0]	• Connect together.	
ST0	• Connect together.	
ST1	• Connect together. • Site required for pull-down resistor to ground but do not populate.	
ST2	• Connect together.	
WBF#	• Connect together. • Recommend site for a pull-up resistor to V_{DDQ} (4 kΩ to 16 kΩ if populated).	
VCC1_5	• Connect to 1.5 V power supply.	
Connector Signals Only		
3.3Vaux	• Connect to PCI 3.3VAUX.	
12V	• Connect to 12 V.	
AGPCLK	• Connect to CK408.	
G_PERR#	• Terminate to V_{DDQ} through a 4 kΩ to 16 kΩ resistor (6.8 kΩ resistor value recommended).	
G_SERR#	• Terminate to V_{DDQ} through a 4 kΩ to 16 kΩ resistor (6.8 kΩ resistor value recommended).	
OVRCNT	•	
PCIRST	• Connect to PCI slot PCIRST.	
PME#	• Connect to PCI PME#.	
TYPEDET#	• Not required.	
USB+	•	
USB–	•	
VCC	• Connect to V_{CC3}.	
VCC5	• Connect to V_{CC}.	
VDDQ	• Connect to $V_{1.5CORE}$.	
VREFCG	• Connect to V_{REF} divider network at the AGP connector.	
VREFGC	• Not required.	
MCH Signals Only		
AGPREF	• Connect to V_{REFCG} pin on connector. • Terminate to ground through a 0.1 µF capacitor at the MCH.	
GRCOMP	• Pull-down to GND through a 40.2 Ω ±1% resistor.	

14.4 Hub Interface

Signal	Description	✓
MCH/ Intel® ICH2 Signals		
HI[10:0]	• Connect together.	
HI_STB	• Connect together.	
HI_STB#	• Connect together.	
HI_REF	• Connect voltage divider circuit with R1=R2=150 Ω ± 1%. • Use two 0.1 µF capacitors within 150 mils of the ICH2. • The MCH should be decoupled with one 0.1 µF capacitor within 150 mils of the package and one 10 µF capacitor nearby. • Bypass to GND through a 0.1 µF capacitor located near each component's (MCH and ICH2) HI_REF pin. • Decouple with a 0.1 µF capacitor placed near the divider circuit.	
VCC1_8	• Connect to 1.8 V power supply.	
MCH Signals Only		
HLRCOMP	• Pull-up to V_{CC1_8} through a 40.2 Ω ± 1% resistor	
Intel® ICH2 Signals Only		
HI11	• No extra pull-ups required.	
HICOMP	• Terminate to V_{CC1_8} through a 40.2 Ω ± 1% resistor. • ZCOMP is no longer supported.	

14.5 Intel® ICH2 Interface

Signal	Description	✓
	LAN Signals	
LAN Connect Interface	• If not used leave all pins as NC. • For line termination, a 33 Ω series resistors can be installed at the driver side of the interface for over/undershoot problems. • **Point-to-point Interconnect:** Direct connect to Intel® 82562EH, Intel® 82562ET, or CNR. • **LOM/CNR implementation:** Add resistor pack (0–33 Ω) to ensure that either a CNR option or a LAN on motherboard option can be implemented at one time. Stubs due to the resistor pack should not be present on the interface. • **Dual Footprint:** Direct connect to 82562EH or 82562ET/EM. A 0–33 Ω resistor can be placed as close as possible to the driving side of each signal line. To improve signal quality, use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.	
LAN_CLK	• Connect to LAN device.	
LAN_RSTSYNC	• Connect to LAN device.	
LAN_RXD[2:0]	• Contains integrated pull-up resistor. • Connect to LAN device.	
LAN_TXD[2:0]	• Connect to LAN device.	
	EEPROM Signals	
EE_CS	• Refer to schematics.	
EE_DIN	• Contains an integrated pull-up resistor. • Connect to EE_DOUT of EEPROM or CNR.	
EE_DOUT	• Contains an integrated pull-up resistor. • Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. • Connect to EE_DIN of EEPROM or CNR.	
EE_SHCLK	• Refer to schematics.	
	FWH Signals	
FWH[3:0]	• Contains integrated pull-up resistors. • Connect to FWH. • Can also be used as LAD[3:0].	
FWH4	• Connect to FWH. • Can also be used as LFRAME#.	

Signal	Description	✓
	PCI Signals	
PCI Connect Interface	• All inputs to the Intel® ICH2 must not be left floating. • Note that some of these signals are mixed with GPIO signals that must be pulled up to different sources. • Pull-ups are placed to meet PCI component specification.	
AD[31:0]	• Refer to schematics.	
C/BE[3:0]#	• Refer to schematics.	
DEVSEL#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
FRAME#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
GNT[5:0]# (PCIGNT#)	• GNT5# contains an integrated pull-up resistor. • Can be left as no connect. • Terminate to V_{CC3_3} if used. • GNT5# can also be used as GNTB# or GPO17. • Actively driven by ICH2.	
GNT[A:B]#	• Contain integrated pull-up resistors. • GNTA# can also be used as GPO16. • GNTB# can also be used as GNT5# or GPO17.	
IRDY#	• Connect together • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
PAR	• Refer to schematics.	
PCICLK	• Connect together to CK408 via 33 Ω series resistor.	
PCIRST#	• Buffer to form IDERST# signal.	
PERR#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
PLOCK#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
PME#	• Contains integrated pull-up resistor. • Connect together.	
REQ[5:0]#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ. • REQ5# can also be used as REQB# or GPI1.	
REQ[A:B]#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ. • REQA# can also be used as GPI0. • REQB# can also be used as REQ5# or GPI1.	

Signal	Description	✓
SERR#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
STOP#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
TRDY#	• Connect together. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ.	
Intel® ICH2/IDE Signals		
Cable Detect	• Host Side/Device Side Detection. • Connect ICH2 GPIO pin to IDE pin PDIAG#/CBLID#. • Connect to GND through a 10 kΩ resistor. • Device Side Detection. • No ICH2 connection. • Connect a .047 µF capacitor from IDE pin PDIAG#/CBLID# to GND.	
IDERST#	• Formed by buffering PCIRST# signal. • Terminate through a series 33 Ω resistor.	
PDA[2:0]	• Contain integrated series termination resistors.	
PDCS1#	• Contains an integrated series termination resistor.	
PDCS3#	• Contains an integrated series termination resistor.	
PDD[15:0]	• Contains integrated series termination resistors. • PDD7 contains an integrated pull-down resistor. • Use a 0 Ω resistor to address possible noise issues on motherboard.	
PDDACK#	• Contains an integrated series termination resistor.	
PDDREQ	• Contains an integrated pull-down resistor. • Contains an integrated series termination resistor.	
PDIOR#	• Contains an integrated series termination resistor.	
PDIOW#	• Contains an integrated series termination resistor.	
PIORDY	• Contains an integrated series termination resistor. • Pull-up to V_{CC3_3} via a 4.7 kΩ pull-up resistor.	
SDA[2:0]	• Contains integrated series termination resistors.	
SDCS1#	• Contains an integrated series termination resistor.	
SDCS3#	• Contains an integrated series termination resistor.	
SDD[15:0]	• Contains integrated series termination resistors. • SDD7 contains an integrated pull-down resistor. • Use a 0 Ω resistor to address possible noise issues on motherboard.	
SDDACK#	• Contains an integrated series termination resistor.	

Signal	Description	✓
SDDREQ	• Contains an integrated pull-down resistor. • Contains an integrated series termination resistor.	
SDIOR#	• Contains an integrated series termination resistor.	
SDIOW#	• Contains an integrated series termination resistor.	
SIORDY	• Contains an integrated series termination resistor. • Pull-up to V_{CC3_3} via a 4.7 kΩ pull-up resistor.	
Intel® ICH2/LPC Signals		
LAD[3:0]	• Connect together. • Contains integrated pull-up resistors. • Can also be used as FWH[3:0].	
LDRQ0#	• Contains integrated pull-up resistors.	
LDRQ1#	• Contains integrated pull-up resistors. • No Connect.	
LFRAME#	• Connect together. • Can also be used as FWH4.	
Interrupt Signals		
APICCLK	• Terminate to GND.	
APICD[1:0]	• Terminate to GND through a 10 kΩ resistor.	
IRQ[15:14]	• Contain integrated series termination resistors. • Terminate to V_{CC3_3} through a 10 kΩ resistor. • Connect to IDE connector. • Open drain outputs.	
PIRQ[H:A]#	• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx#line has a separate control register. • Terminate to V_{CC3_3} through an 8.2 kΩ resistor or V_{CC5} through a 2.7 kΩ. • PIRQG# can also be used as GPI4. • PIRQF# can also be used as GPI3. • Since PIRQ[E]# and PIRQ[H]# are used internally for LAN and USB controllers respectively, they cannot be used as GPIO(s) pin. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: —PIRQ[A]# is connected to IRQ16, —PIRQ[B]# to IRQ17, —PIRQ[C]# to IRQ18, —PIRQ[D]# to IRQ19, —PIRQ[E]# to IRQ20, —PIRQ[F]# to IRQ21, —PIRQ[G]# to IRQ22, and —PIRQ[H]# to IRQ23. • This frees the ISA interrupts.	
SERIRQ	• Terminate to V_{CC3_3} through a weak 8.2 kΩ pull-up resistor. • Open drain.	

Signal	Description	✓
Intel® ICH2/USB		
Disabling	• Ensure the differential pairs are pulled down through 15 kΩ resistors. • Ensure the OC[3:0]# signals are de-asserted by pulling them up weakly to V_{CC3_3SBY}, and that both function 2 and 4 are disabled via the D31:F0;FUNC_DIS register. • Ensure that the 48 MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.	
OC[3:0]#	Refer to schematics.	
USBP[3:0]N USBP[3:0]P	• 15 Ω series resistors should be placed as close as possible to the Intel® ICH2 (<1 inch) for source termination of the reflected signal. • Terminate unused USB ports with 15 kΩ pull-down resistors on both P+/P– data lines. • For signal quality (rise/fall time) and to help minimize EMI radiation, a 47 pF capacitor may be placed as close to the USB connector as possible. • Place 15 kΩ pull-down resistors on USB Connector side of the series resistors on the USB data lines (P0± … P3±). The length of the stub should be as short as possible. Resistors are REQUIRED for signal termination by USB specification.	
Power Management Signals		
PWRBTN#	• Contains an integrated pull-up resistor.	
PWROK	• To meet timing requirements, this signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both V_{CC3_3} and V_{CC1_8} have reached their nominal voltages.	
RI#	• Recommend an 8.2 kΩ pull-up resistor to resume well.	
RSMRST#	• To meet timing requirements, this signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both V_{CC3_3} and V_{CC1_8} have reached their nominal voltages.	
RSM_PWROK	• Connect to RSMRST# on desktop platforms. • Requires weak pull-down. Also requires well isolation control as directed in Section 8.8.8.	
SLP_S3#	• If connected to clock generator's PWRDOWN pin, use an RC delay to ensure at least 5 PCICLKs after it is asserted. • No extra pull-up/pull-down resistor needed. • Driven by ICH2.	
SLP_S5#	• No extra pull-up/pull-down resistor needed. • Driven by ICH2.	
SUSCLK	• Connect to SIO. Otherwise route to a test point.	
SUSSTAT#	• Connect together.	
THRM#	• Connect to temperature sensor. • Pull-up if not used since polarity bit defaults this signal to an active low.	
VRMPWRGD	• Connect to processor's VRM power good. • Pull-up to V_{CC3} using a 10 kΩ resistor if unused.	

Signal	Description	✓
SMBUS Signals		
SMBALERT#	• See GPIO section if SMBALERT# is not implemented. • Can also be used as GPI11.	
SMBCLK SMBDATA	• Pull-up resistor required. This value is determined by the line load. • If the SMBus is used only for the SDRAM SPD EEPROMS, (one on each DIMM) pull-up with a 4.7 kΩ to 3.3 V.	
System Management Signals		
INTRUDER#	• Pull-up to V_{CC}RTC (V_{BAT}) with a weak 10 kΩ resistor. No resistor to ground on the other side of the intruder connector.	
SMLINK[1:0]	• Pull-up through an 8.2 kΩ resistor. This value is determined by the line load.	
RTC Signals		
RTCRST#	• Connect through an 8.2 kΩ series resistor and a 2.2 μF decoupling capacitor to ensure 10–20 ms RC delay.	
RTCX1 RTCX2	• Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor. • Use an 18 pF decoupling capacitor at each signal (Assuming 12.5 pF crystal capacitive load). • RTCX1may optionally be driven by an external oscillator. • These signals are 1.8 V only, and must not be driven by a 3.3 V source.	
VBIAS	• Connect through a series 1 kΩ and a 0.047 μF capacitor. • Connect to RTCX1 through a 10 MΩ series resistor.	
VCCRTC	• No “Clear” CMOS jumper on V_{CC}RTC. • Use a jumper on RTCRST#, a GPI, or use a safe mode strapping for “Clear” CMOS.	
AC ’97 Signals		
AC_RST	• Connect together.	
AC_SYNC	• No extra pull-down required. • Some implementations add termination for signal integrity.	
AC_BITCLK	• No extra pull-down required. • When nothing is connected to the link, BIOS must set a shut-off bit for the internal resistor to be enabled. At that point you don’t need pull-ups/pull-downs on any of the link signals.	
AC_SDOUT	• Requires a jumper to an 8.2 kΩ pull-up resistor (Do not stuff for default operation).	
AC_SDIN[1:0]	• Requires pads for weak 10 kΩ resistors. • Stuff resistor if unused or if going to CNR connector. • Pull-down to ground if no codec on system board.	

Signal	Description	✓
GPIO Signals		
GPIO interface	• Ensure all unconnected signals are outputs only. • Requires a 10 kΩ pull-down to ground for GPI's used for combination host-side/device-side cable detection.	
GPI[0:1]	• Reside in main power well (5 V tolerant). • Pull-up resistors must use the V_{CC3_3} plane. • Unused inputs must be pulled up to V_{CC3_3} or pulled down to ground. • GPI0 can also be used as REQA#. • GPI1 can also be used as REQB# or REQ5#.	
GPIO2	• Not implemented.	
GPI[3:4]	• Reside in main power well (5 V tolerant). • Pull-up resistors must use the V_{CC3_3} plane. • Unused inputs must be pulled up to V_{CC3_3} or pulled down to ground. • Can also be used as PIRQ[F:G]# respectively.	
GPIO5	• Not implemented.	
GPI[6:7]	• Reside in main power well (5 V tolerant). • Pull-up resistors must use the V_{CC3_3} plane. • Unused inputs must be pulled up to V_{CC3_3} or pulled down to ground.	
GPI8	• Reside in resume power well (not 5 V tolerant). • Pull-up resistors must use the V_{ccSus3_3}. • Unused resume well inputs must be pulled up. • Can be used as an ACPI compliant wake event. • Contains an associated status bits in the GPE1_STS register.	
GPI[9:10]	• Not Implemented	
GPI[11:13]	• Reside in resume power well (not 5 V tolerant). • Pull-up resistors must use the V_{ccSus3_3} plane. • Unused resume well inputs must be pulled up. • GPI11 can also be used as SMBALERT#. • Can be used as ACPI compliant wake events. • Contain associated status bits in the GPE1_STS register.	
GPI[14:15]	• Not Implemented.	
GPO[16:17]	• Reside in main power well. • Contain integrated pull-up resistors. • GPO16 can also be used as GNTA#. • GPO17 can also be used as GNT5# or GNTB#.	

Signal	Description	✓
GPO[18:23]	• Reside in main power well. • Can be left as no connect. • GPO22 is open drain.	
GPIO[24:25]	• Reside in resume power well. • Can be left as no connect.	
GPIO26	• Not Implemented.	
GPIO[27:28]	• Reside in resume power well. • Can be left as no connect.	
GPO[29:31]	• Not Implemented.	
Miscellaneous Signals		
SPKR	• Contains an integrated pull-up resistor. • The effective impedance of the Speaker and Codec circuitry must be greater than 50 kΩ; otherwise, a means to isolate the resistive load from the signal while PWROK is low should be found.	
TP_0	• Requires external pull-up resistor to V_{ccSus3_3}. • Not required for desktop.	
FS_0	• Contains an integrated pull-up resistor. • Connect to a test point.	
RCIN#	• Terminate to V_{CC3_3} through a 10 kΩ resistor. • Typically driven by open-drain external microcontroller.	
A20GATE	• Terminate to V_{CC3_3} through a 10 kΩ resistor.	

14.6 Miscellaneous MCH Signals

Signal	Description	✓
66IN	• Connect to CK408.	
RSTIN#	• Connect to PCIRST# on the ICH2.	
TESTIN#	• No Connect.	

14.7 Clock Interface CK408

Signal	Description	✓
66_BUFF0	• Connect to MCH. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	
66_BUFF1	• Connect to Intel® ICH2. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	

Signal	Description	✓
66_BUFF2	• Connect to AGP. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	
66_INPUT	• No Connect.	
CLK14	• Connect to ICH2 through a series 33 Ω resistor.	
CLK48	• Connect to ICH2 through a series 33 Ω resistor.	
CLK66	• Connect to ICH2 through a series 33 Ω resistor.	
CPU [1:0]	• Connect to processor. • Connect to a series 27 Ω ±5% resistor and terminate to GND through a 49.9 Ω ±1% resistor.	
CPU [1:0]#	• Connect to processor. • Connect to a series 27Ω ±5% resistor and terminate to GND through a 49.9Ω ±1% resistor.	
CPU2	• Connect to MCH. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.	
CPU2#	• Connect to MCH. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.	
CPU_STOP#	• Terminate to V_{CC3} through a 1 kΩ ± 1% resistor.	
DOT_48 MHz	• No Connect.	
DRCG_0	• Connect to Glue Chip/Discrete Logic. • Connect to a series 33Ω ±5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	
DRCG_1/VCH	• No Connect.	
IREF	• Terminate to GND through a 475 Ω ± 1% resistor.	
MULT0	• Connected from the V_{CC3} through a series 10 kΩ ± 5% resistor and terminate to GND through a parallel 1 kΩ ± 1% resistor.	
PCI [6:0]	• Connect to a series 33 Ω ±5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	
PCIF[2:0]	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	
PCI_STOP#	• Terminate to V_{CC3} through a 1 kΩ ± 5% resistor.	
PWRDWN#	• Terminate to V_{CC3} through a 1 kΩ ± 5% resistor.	
REF0	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.	
SEL[1:0]	• Terminate to V_{CC3CLK} through a 1 kΩ ± 5% resistor.	
SEL_2	• Terminate to GND through a 1 kΩ ± 5% resistor.	
SCLK	• Connect to DIMMs.	
SDTA	• Connect to DIMMs.	

Signal	Description	✓
USB_48 MHz	• Connect to ICH2. • Terminate to GND through a 33 Ω ± 5% resistor and a 10 pF ± 5% capacitor.	
VDD	• Terminate to V_{CC3CLK}.	
VDD_48 MHz	• Terminate to V_{CC3CLK}	
VDDA	• Terminate to GND through a 0.1 µF ± 5% capacitor.	
VSS	• Terminate to GND.	
VSS_48 MHz	• Terminate to GND.	
VSS_IREF	• Terminate to GND.	
VTT_PWRGD#	• Connect to an inverted copy of V_{CC_CPU} . Refer to the respective section of the design guide for more details.	
XTAL_IN	• Terminate to GND through a 10 pF ± 5% capacitor.	
XTAL_OUT	• Terminate to GND through a 10 pF ± 5% capacitor.	

14.8 Power and Ground

Signal	Description	✓
VCC3_3	• Requires six, 0.1 µF decoupling capacitors.	
VCC1_8	• Requires two, 0.1 µF decoupling capacitors.	
V5REF	• Connect to V_{REF}[2:1] pins.	
VCCSUS3_3	• Requires one, 0.1 µF decoupling capacitor.	
VCCSUS1_8	• Requires one, 0.1 µF decoupling capacitor.	
V5REF_SUS	• Requires one, 0.1 µF decoupling capacitor. • V5REF_SUS only affects 5 V-tolerance for USB OC[3:0]# pins and can be connected to either VccSus3_3 or 5V_Always/5V_AUX if 5V tolerance on these OC[3:0]# is not needed. If 5 V tolerance on OC[3:0]# is needed, then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.	
V_CPU_IO[1:0]	• Connected to the proper power plane for the processor's CMOS compatibility signals. • Connect one, 0.1 µF decoupling capacitor.	
VSS	• Connect to GND.	

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15 Intel® 845 Chipset Design Layout Checklist

15.1 System Bus

15.1.1 System Bus

Checklist Item	✓
Data Signals: D[63:0]#, DBI[3:0]#	
• Point-to-Point Topology.	
• Edge to edge spacing versus trace to reference plane height ratio should be 3:1.	
• 2.0 inches to 10.0 inches pin-to-pin data signal lengths.	
• Traces should be 7 mils wide with 13-mil spacing.	
• Data signals of the same source synchronous group should be routed to the same pad-to-pad length within +100 mils of the associated strobes.	
Data Strobes: DSTBn/p[3:0]	
• Traces should be 7 mils wide with 13 mil spacing.	
• Data strobes and their compliments should be routed within ± 25 mils of the same pad to pad length.	
Address Strobes: ADSTB[1:0]	
• Point-to-Point Topology.	
• Edge to edge spacing versus trace to reference plane height ratio should be 3:1.	
• 2.0 inches to 10.0 inches pin to pin address signal lengths.	
• Traces should be 7 mils wide with 13-mil spacing.	
Address Signals: A[3:31]#, REQ[4:0]	
• Traces should be 7 mils wide with 13-mil spacing.	
• 2.0 inches to 10.0 inches pin to pin address signal lengths.	
• Address signals of the same source synchronous group should be routed to the same pad-to-pad length, within ± 200 mils of the associated strobes.	
Clocks: BCLK, BCLK#	
• These should be routed as a differential pair with 7-mil traces and 7mil spacing between them.	
• 2.5 inches to 10.0 inches pin-to-pin common clock lengths.	
• 25 mil spacing should be maintained around all clocks.	

Checklist Item	✓
Processor AGTL+: FERR#, PROCHOT#, THERMTRIP#	
• Traces should be 5 mils wide with 7 mil spacing.	
• 1.0 inch to 12.0 inches max from processor to Intel® ICH2.	
• 3.0 inches max from ICH2 to V_{DD}.	
ICH2 AGTL+: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK#	
• Traces should be 5 mils wide with 7-mil spacing.	
• 12.0 inches max from ICH2 to processor.	
• Level shifting is required from the INIT# pin to FWH.	
Intel® ICH2 Open Drain AGTL+: PWRGOOD	
• 7 mil spacing.	
• 1.0 inch to 12.0 inches max from ICH2 to processor.	
• 1.1 inches max breakout length.	
• 3.0 inches max from Processor to V_{DD}.	
Miscellaneous AGTL+: BR0#, RESET#	
• Terminate using discrete components on the system board.	
• Minimize the distance between the terminating resistors and the processor.	
• Connect the signals between these components.	
Miscellaneous AGTL+: COMP[1:0]	
• Minimize the distance from terminating resistor.	
Miscellaneous AGTL+: THERMDA, THERMDC	
• 10 mils wide by 10 mil spacing.	
• Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0 inches to 8.0 inches away as long as the worst noise sources such as clock generators, data, buses and address buses, etc are avoided.	
• Route in parallel and close together with ground guards enclosed.	

15.1.2 Decoupling, V_{REF}, and Filtering

Checklist Item	✓
V_{CC_CPU} Decoupling	
• 9 OSCONs, 560 µF. • 3 Al Electrolytic, 3300 µF. • 38 1206 package, 10 µF. • Refer to Section 4.6.2.	
Processor GTLREF	
• The processor must have one dedicated voltage divider.	
• Keep the voltage divider within 1.5 inches of the first GTLREF pin.	
• Keep signal routing at least 10 mils separated from the GTLREF routes.	
• 7 mil min trace length for routing.	
• Do not allow signal lines to use the GTLREF routing as part of their return path.	
GTLREF Decoupling: • Decouple voltage divider with a 1 µF capacitor. • Decouple pin with a high-frequency capacitor (such as a 220 pF 603). • Place capacitor as close to pin as possible.	
V_{CCA}, $V_{CCIOPLL}$, and V_{SSA} Filtering for Processor	
• Use shielded type inductors.	
• Minimize the distance between V_{CCA}, V_{SSA} pins and capacitors.	
• V_{CCA} should be routed parallel and next to V_{SSA} route.	
• Filter capacitors and inductors should be routed next to each other.	
MCH HVREF	
• 12 mils wide, 3.0 inches max length	
• 10 mil group spacing	
• Place 0.1 µF decoupling capacitor at the MCH	
• Minimize the distance between the voltage divider, decoupling capacitors and MCH	
MCH HVREF	
• 12 mils wide, 3.0 inches max length.	
• 10 mil group spacing.	
• Place 0.1 µF decoupling capacitor at the MCH.	
• Minimize the distance between the voltage divider, decoupling capacitors and MCH.	
MCH HRCOMP[1:0]	
• 10 mils wide, 0.5-inch max length.	
• 7 mils group spacing.	
• Minimize the distance between HRCOMP and the MCH.	

Checklist Item	✓
MCH VTT Decoupling	
• Place five evenly 0.1 µF capacitors within 150 mils of the MCH.	
• Place two 10 µF capacitors right behind the 0.1 µF capacitors.	

15.1.3 Intel® Boxed Processor Mechanical Keep-Outs

Checklist Item	✓
Intel® Boxed Processor Mechanical Keep-Outs	
• Verify Intel's Boxed Processor mechanical keep-outs are marked and visible during board layout. This keep-out zone should be considered during chassis selection.	

15.2 System Memory (SDR)

15.2.1 3 DIMM SDR-SDRAM (PC133)

Checklist Item	✓
Data Signals: SDQ[63:0], SCB[7:0]	
• Balanced "T" Topology.	
• 5 mils wide by 12 mil spacing.	
• 12 mil group spacing.	
• 2.5 inches to 4.5 inches from MCH to middle DIMM.	
• 0.4 inch to 0.6 inch from middle DIMM to outside DIMMs.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length. • 5 mils wide by 8-mil spacing, 1.5 inches max length.	
Chip Select Signals: SCS[11:0]#	
• Point-to-Point Topology.	
• 5 mils wide by 12 mil spacing.	
• 12 mil group spacing.	
• 3.0 inches to 4.0 inches from MCH to DIMM.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length.	

Checklist Item	✓
Clock Enable Signals: SCKE[5:0]	
• Point-to-Point Topology.	
• 10 mils wide by 12 mil spacing.	
• 12 mil group spacing.	
• 3.0 inches to 4.4 inches from MCH to DIMM.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length.	
Address/Control Signals: SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#	
• Balanced "T" Topology.	
• 5 mils wide by 10 mil spacing.	
• 10 mil group spacing.	
• 2.5 inches to 4.0 inches from MCH to middle DIMM.	
• 0.4 inch to 0.6 inch from middle DIMM to outside DIMMs.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length. • 5 mils wide by 8- mil spacing, 1.0-inch max length.	
Clock Signals: SCK[11:0]	
• Point-to-Point Topology.	
• 7 mils wide by 15 mil spacing.	
• 15 mil group spacing.	
• 5.9 $\pm$ 0.05 inch from MCH die pad to DIMM pin.	
• Place EMI capacitor less than 1.0 inch from SCK ball, 0.25-inch max stub length.	
• Parallel termination placed within 1.5 inches of DIMM.	
Breakout guideline: • 7 mils wide by 5-mil spacing, 0.5-inch max length. • 7 mils wide by 10-mil spacing, 1.0-inch max length.	
Feedback Signals: RDCLKO, RDCLKIN	
• Point-to-Point Topology.	
• 7 mils wide, 50 mil length.	
• 5 mil group spacing.	

15.2.2 2 DIMM SDR-SDRAM (PC133)

Checklist Item	✓
Data Signals: SDQ[63:0], SCB[7:0]	
• Daisy Chain Topology.	
• 5 mils wide by 12 mil spacing.	
• 12 mil group spacing.	
• 2.0 inches to 4.0 inches from MCH to first DIMM.	
• 0.4 inch to 0.6 inch from first DIMM to second DIMM.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length. • 5 mils wide by 8-mil spacing, 1.5 inches max length.	
Chip Select Signals: SCS[7:0]#	
• Point-to-Point Topology.	
• 5 mils wide by 12 mil spacing.	
• 12 mil group spacing.	
• 3.0 inches to 4.0 inches from MCH to DIMM.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length.	
Clock Enable Signals: SCKE[3:0]	
• Point-to-Point Topology.	
• 10 mils wide by 12-mil spacing.	
• 12-mil group spacing.	
• 3.0 inches to 4.0 inches from MCH to DIMM.	
Breakout guideline: 5 mils wide by 5-mil spacing, 0.5-inch max length.	
Address/Control Signals: SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#	
• Daisy Chain Topology.	
• 5 mils wide by 10 mil spacing.	
• 10 mil group spacing.	
• 2.0 inches to 3.0 inches from MCH to first DIMM.	
• 0.4 inch to 0.6 inch from first DIMM to second DIMM.	
Breakout guideline: • 5 mils wide by 5-mil spacing, 0.5-inch max length. • 5 mils wide by 8-mil spacing, 1.5-inches max length.	

Checklist Item	✓
Clock Signals: SCK[7:0]	
• Point-to-Point Topology.	
• 7 mils wide by 15 mil spacing.	
• 15 mil group spacing.	
• 5.3 ± 0.05 inch from MCH die pad to DIMM pin.	
• Place EMI capacitor less than 1.0-inch max from SCK ball, 0.25-inch max stub length.	
• Parallel termination placed within 1.5 inches of DIMM.	
Breakout guideline: • 7 mils wide by 5-mil spacing, 0.5-inch max length. • 7 mils wide by 10-mil spacing, 1.0-inch max length.	
Feedback Signals: RDCLKO, RDCLKIN	
• Point-to-Point Topology.	
• 7 mils wide, 50 mil length.	
• 5 mil group spacing.	

15.2.3 Decoupling, Compensation, and V_{REF}

Checklist Item	✓
V_{CCSM} Decoupling	
• Place nine, evenly spaced, 0.1 µF 0603 capacitors between each DIMM.	
• Place six, 100 µF capacitors around the DIMMs.	
• Place six, evenly spaced, 0.1 µF X7R capacitors within 150 mils of the MCH.	
• Place one 22 µF capacitor at the MCH.	
SMRCOMP	
• 10 mils wide minimum, 0.5-inch max length.	
• 7-mil group spacing.	
• Minimize the distance between SMRCOMP resistor and the MCH.	
SDREF	
• 12 mils wide, 3.0 inches max length.	
• 10 mil group spacing	
• Place 0.1 µF decoupling capacitor at the MCH.	
• Minimize the distance between the voltage divider, decoupling capacitors and MCH.	

15.3 AGP

15.3.1 1X Signals

Checklist Item	✓
CLK, RBF#, WBF#, ST[2:0], PIPE, G_REQ#, G_GNT#, G_PAR, G_FRAME#, G_IRDY#, G_TRDY, G_STOP#, G_DEVSEL#	
• 7.25 inches max trace length.	
• 5 mils wide by 5 mil spacing.	
• No trace matching requirements.	

15.3.2 2X/4X Signals

Checklist Item	✓
G_AD [31:0], G_C/BE[3:0]#, ADSTB[1:0]#, SBA[7:0], SB_STB, SB_STB#	
• Route G_AD[15:0], G_C/BE[1:0], AD_STB0, and AD_STB0# together.	
• Route G_AD[31:16], G_C/BE[3:2], AD_STB1, and AD_STB1# together.	
• Route SBA[7:0], SB_STB, SB_STB# together.	
• ± 0.1-inch length match strobe pairs.	
Less Than 6 Inches	
• 5 mils wide by 15 mil spacing.	
• ± 0.25 inch length match from DATA and G_C/BE# to strobes.	
• Signals that require pull-up or pull-down resistors. • 0.5-inch max stub length for 1X signals.	
Greater Than 6 Inches and Less Than 7.25 Inches	
• 5 mils wide by 20-mil spacing.	
• ± 0.125 inch length match from DATA and G_C/BE# to strobes.	
• Signals that require pull-up or pull-down resistors. • 0.1-inch max stub length for 2X/4X signals.	
AGP Controller Down On Motherboard	
• 5 mils wide by 15-mil spacing.	
• 10.0 inches max trace length.	

15.3.3 Decoupling, Compensation, and V_{REF}

Checklist Item	✓
V_{CC1_5} Decoupling	
• Min of six, 0.1 µF capacitors spaced evenly among the AGP signals routed between the MCH and AGP connector to decouple MCH core and MCH AGP I/O. All capacitors must be within 0.25 inch of MCH.	
GRCOMP	
• 10 mils wide, 0.5-inch max length.	
• Minimize the distance between GRCOMP resistor and MCH.	
AGPREF	
• Minimum trace width must be 12 mils.	
• Minimum trace spacing around the AGPVREF signal must be 25 mils.	
• One 0.1 µF bypass capacitor should be placed 0.8-inch maximum from MCH's AGPREF pin.	

15.4 Hub Interface

15.4.1 Interface Signals

Checklist Item	✓
General Recommendations	
• It is recommended that all signals be referenced to V_{SS}.	
• Board impedance must be 60 Ω ± 10%.	
• Traces must be routed 5 mils wide with 15 mils spacing.	
• Max trace length is 8 inches	
Data Signals	
• Can be routed to 5 on 5 for breakout, but must be separated to 5 on 15 within 300 mils of the package.	
• Must be matched within ± 0.1 inch of the HL_STB diff pair.	
Strobe Signals	
• Strobe pair should have a minimum of 15 mils spacing from any adjacent signals.	
• Each strobe signal must be the same length.	

15.4.2 Decoupling, Compensation, and V_{REF}

Checklist Item	✓
V_{CC1_8} Decoupling	
• Decouple the Intel® ICH2 with two, 0.1 µF capacitors within 150 mils from the package.	
• Decouple the MCH with one, 0.1 µF capacitor within 150 mils of the package and one 10 µF capacitor nearby.	
• Capacitors should be adjacent to hub interface rows.	
HLRCOMP	
• Place resistor using a 10-mil wide and 0.7-inch max trace length.	
• 7-mil group spacing.	
• Minimize the distance between HLRCOMP resistor and MCH.	
HI_REF	
• Should be placed no more than 4 inches of away from MCH or ICH2.	
• Bypass to ground with a 0.1 µF capacitor located within 0.25 inch of each component's HI_REF pin.	
• Place one 0.1 µF capacitor at the divider.	

15.5 Clocks: CK408

Checklist Item	✓
Host Clock: CPU#, CPU	
• 7 mils wide.	
• Differential pair spacing should be based on a distance from BCLK1 to BCLK0.	
• Spacing to other traces should 4 times to 5 times greater than distance from BCLK1 to BCKL0.	
• Processor routing length—Clock driver to Rs should be 0.5-inch max.	
• Processor routing length—Rs to Rs-Rt should be 0 inch to 0.2 inch	
• Processor routing length—RS_RT node to Rt should be 0 inch to 0.2 inch	
• Processor routing length—RS_RT node to load should be 2 inches to 9 inches	
• MCH routing length—Clock driver to Rs should be 0.5-inch max.	
• MCH routing length—Rs to Rs-Rt should be 0.5-inch max.	
• MCH routing length—RS_RT node to Rt should be 0 inch to 0.2 inch max.	
• MCH routing length—RS_RT node to load should be 2.0 inches to 9.0 inches max.	
• Clock driver to processor and clock driver to chipset length matching should be 600 mils.	
• 10 mil length matching between BCLK0 to BCLK1.	
• Do not split up the two halves of a differential clock pair between layers.	
• Route all agents on the same physical routing layer referenced to ground of the differential clock.	
• Make sure that the skew induced by the vias is compensated in the traces to other agents.	
• Do not place vias between adjacent complementary clock traces.	

Checklist Item	✓
• Maintain uniform spacing between the two halves of differential clocks.	
• Route clocks on physical layers adjacent to the V_{SS} reference plane only.	
66 MHz Clock Group	
• Point-to-Point Topology.	
• 5 mils wide and 20 mil spacing.	
• 20 mil group spacing.	
• Series termination within 0.5 inch of the driver.	
• Trace length from series termination to receiver on the motherboard between 4.0 inches and 8.5 inches	
• The total trace lengths must be matched to ± 100 mils of each other.	
• Follow these guidelines when routing to an AGP device down on the motherboard.	
AGP Clock (When Routing to an AGP Connector)	
• Point-to-Point Topology.	
• 5 mils wide and 20 mil spacing.	
• 20 mil group spacing.	
• Series termination within 0.5 inch of the driver.	
• The total trace length must be 4.0 inches less than the CLK66 total trace lengths ± 100 mils.	
33 MHZ Clock Group	
• Point-to-Point Topology.	
• 5 mils wide and 15 mil spacing.	
• 15 mil group spacing.	
• Series termination within 0.5 inch of the driver.	
• The total mismatch between any two, 33 MHz clocks must be less than 7.5 inches. If routing to a PCI connector, 2.6 inches of routing on the PCI card must be included in the 7.5 inches total mismatch.	
• The 33 MHz clock to the Intel® ICH2 must be matched to ± 100 mils of the 66 MHz clock to the ICH2.	
14 MHz Clock Group	
• Balanced T Topology.	
• 5 mils wide and 10 mil spacing.	
• 10 mil group spacing.	
• Series termination within 0.5 inch of the driver.	
• The total trace length from the Clock driver to SIO and Clock driver must be matched to 0.5 inch	
• Signal must T within 12 inches of the series termination.	
• Max trace length of stubs is 6 inches	
• Total trace length matched to ± 0.5 inch of each other.	

Checklist Item	✓
USB Clock	
• Point-to-Point Topology.	
• 5 mils wide.	
• 15 mil group spacing.	
• Series termination within 0.5 inch of the driver.	
• Trace length from series termination to receiver on the motherboard between 3.0 inches and 12 inches	

15.5.1 Decoupling

Checklist Item	✓
V_{DD}A /V_{DD} Decoupling	
• Place one 10 µF capacitor close to the V_{DD} generation circuitry.	
• Place six 0.1 µF capacitors close to the V_{DD} pins on the clock driver.	
• Place three 0.01 µF capacitors close to the V_{DD}A pins on the clock driver.	
• Place one 10 µF bulk decoupling capacitor close to the V_{DD}A generation circuitry.	
• Host clock pairs must be differentially routed on the same physical routing layer.	
• Differential clocks must not have more than two via transitions.	
• Ground referencing is strongly recommended for all platform clocks.	
• Motherboard layer transitions and power plane splits must be kept to a minimum.	
• For flooding options, refer to Section 12.4 of the Design Guide.	

15.6 Intel® ICH2

15.6.1 IDE

Recommendations	✓
• 5 mil width and 7 mil spacing.	
• 8.0 inches max trace length from Intel® ICH2 to IDE connector.	
• Shortest IDE trace length must be 0.5 inch shorter than the longest IDE trace length.	

15.6.2 AC '97

Recommendations	✓
• Trace impedance should be 60 Ω ± 15%.	
• 5 mil width by 5 mil spacing.	
• 14.0 inches max trace length from Intel® ICH2 to Codec/CNR connector (Assuming CNR implements its audio solution with a max trace length of 4.0 inches).	

15.6.3 USB 1.1

Recommendations	✓
• The trace impedance for the P0±… P3± signals should be 45 Ω (to ground) for each USB signal P+ or P–.	
• 9 mils wide, 25 mil spacing between Differential pairs.	
• 15 Ω series resistor to be placed < 1 inch from Intel® ICH2.	
• 15 kΩ pull-down resistors must be on the connector side of the series resistor and must always be present whether or not the USB ports are used.	
• 0–47 pF parallel capacitors should be placed as close to the USB connector as possible.	
• Stub length due to 15 kΩ pull-downs should be as short as possible.	
• The series impedance of the twisted differential signal pairs P+ and P– should be 90 Ω resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.	
• USB data lines must be routed as critical signals. The P+/P– signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces. Doubling the space from the P+/P– signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P– signal traces. The P+/P– signal traces must also be the same length. Lastly, do not route over plane splits.	
• Trace Characteristics: Line Delay = 160.2 ps, Capacitance = 3.5 pF, Inductance = 7.3 nH, Res @ 20° C = 53.9 mΩ.	

15.6.4 RTC

Recommendations	✓
• 1.0 inch max RTC OSC signal trace lengths.	
• Minimize the capacitance between RTCX1 and RTCX2 in the routing.	
• Put a ground plane underneath crystal components.	
• 0.25 inch max RTC lead lengths.	
• Do not route switching signals under the external components (unless on other side of board).	
• 5 V Reference power plane—one 0.1 µF capacitor.	
• 5 V Reference Stand By power plane—one 0.1 µF capacitor.	
• To assist in RTC circuit debug, route SUSCLK to a test point if it is not used.	

15.6.5 LAN

Recommendations	✓
• Trace Spacing: 5 mils wide, 10 mil spacing.	
• LAN Max Trace Length Intel® ICH2 to CNR: L = 3 inches to 9 inches (0.5 inch to 3 inches on card).	
• Stubs due to R-pak CNR/LOM stuffing option should not be present.	
• Maximum Trace Lengths: ICH2 to Intel® 82562EH: L = 4.5 inches to 10 inches; Intel® 82562ET: L = 3.5 inches to 10 inches; Intel® 82562EM: L = 4.5 inches to 8.5 inches.	
• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace).	
• Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	
• Keep the total length of each differential pair under 4 inches.	
• Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	
• Distance between differential traces and any other signal line is 100 mils. (300 mils recommended).	
• Route 5 mils on 7 mils for differential pairs (out of LAN phy).	
• Differential trace impedance should be controlled to be ~100 Ω.	
• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45 deg. bends.	
• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	
• Do not route traces and vias under crystals or oscillators.	
• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	
• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	
• Vias to decoupling capacitors should be sufficiently large in diameter.	
• Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	
• Isolate I/O signals from high-speed signals.	
• Place the Intel® 82562ET/EM part more than 1.5 inches away from any board edge.	
• Place at least one bulk capacitor (4.7 µF or greater) on each side of the 82562ET/EM.	

Recommendations	✓
• Place decoupling capacitors (0.1 µF) as close to the 82562ET/EM as possible.	

15.6.6 Intel® ICH2 Decoupling

Recommendations	✓
• Place decoupling capacitors as close to the Intel® ICH2 as possible (less than 200 mils).	
• 3.3 V Core power plane—six 0.1 µF capacitors.	
• 3.3 V Standby power plane—one 0.1 µF capacitor.	
• Processor I/F (1.3 to 2.5 V)—one 0.1 µF capacitor.	
• 1.8 V Core power plane—two 0.1 µF capacitors.	
• 1.8 V Standby power plane—one 0.1 µF capacitor.	
• 5 V Reference power plane use one 0.1 µF capacitor.	
• 5 V Reference Standby power plane use one 0.1 µF capacitor.	
• V_{5REF_SUS} affects 5 V tolerance for all USB pins and can be connected to V_{ccSus3_3} if ICH2 USB is not supported in the platform. If USB is supported, V_{5REF_SUS} must be connected to 5V_AUX, which remains powered during S5.	

15.6.7 Power/Ground Decoupling

Recommendations	✓
• Insert 4–6 decoupling capacitors, including two, 4.7 µF capacitors for power/ground connections.	
• Minimize the distance between decoupling capacitors and power pins.	
• Route traces over a continuous plane with no interruptions.	
• Separate noisy digital grounds from analog grounds.	
• All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential.	

15.7 FWH

Recommendations	✓
• 0.1 µF capacitors should be placed between the V_{CC} supply pins and the V_{SS} ground pins and no less than 390 mils from the V_{CC} supply pins.	
• 4.7 µF capacitors should be placed between the V_{CC} supply pins and the V_{SS} ground pins and no less than 390 mils from the V_{CC} supply pins.	

15.8 Power

15.8.1 Filtering

Checklist Item	✓
MCH PLL Filter Routing Guidelines: PLL0, PLL1	
• 5 mil width by 10 mil spacing.	
• 1.5 inches max length from capacitor to MCH.	

Appendix A: Customer Reference Board Schematics

This appendix provides a set of schematics for the Intel· Pentium 4 processor in 478-pin package and 845 chipset Platform Customer Reference Board (CRB).

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INTEL (R) 845 SDR SCHEMATICS REV 1.3

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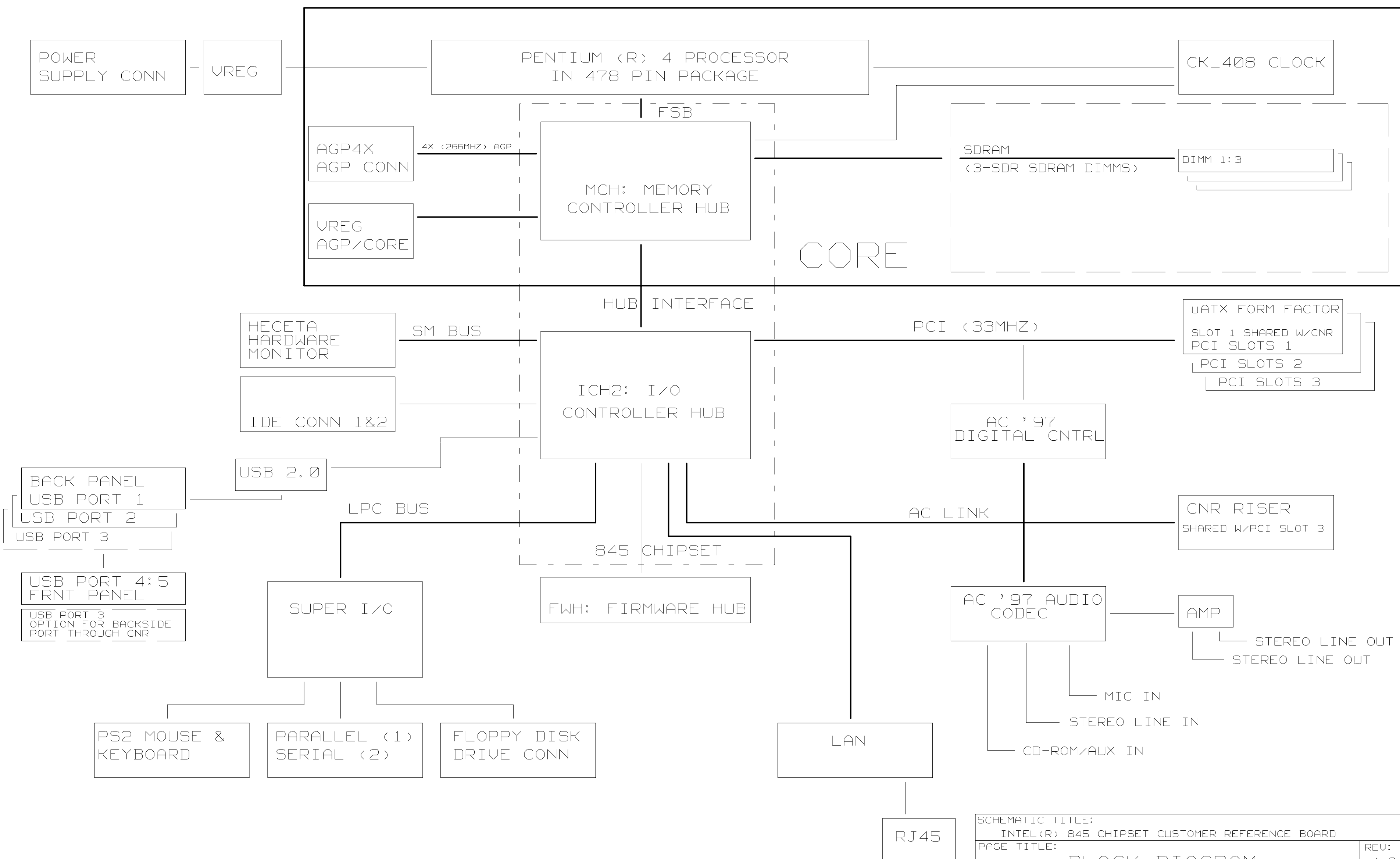

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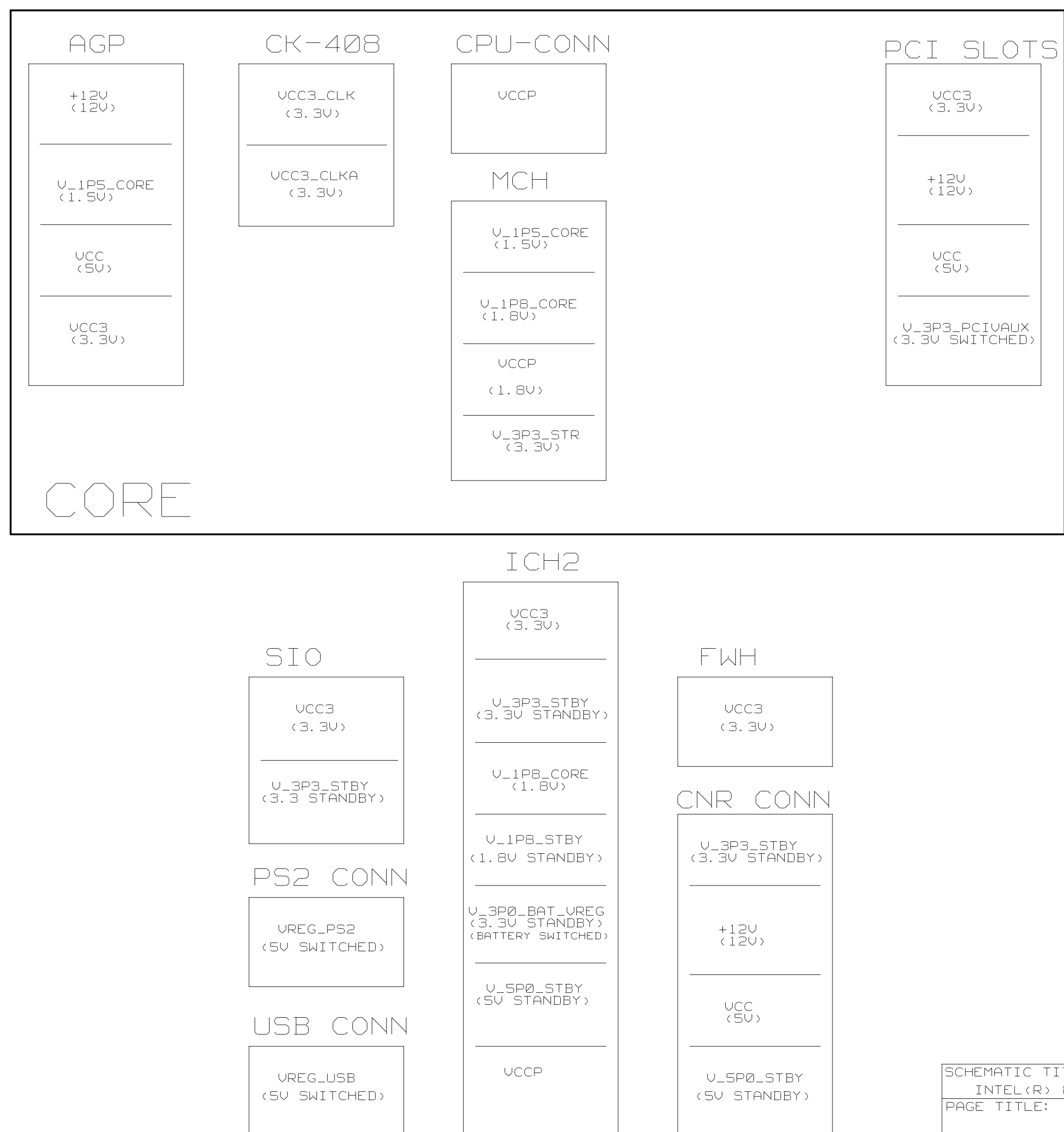

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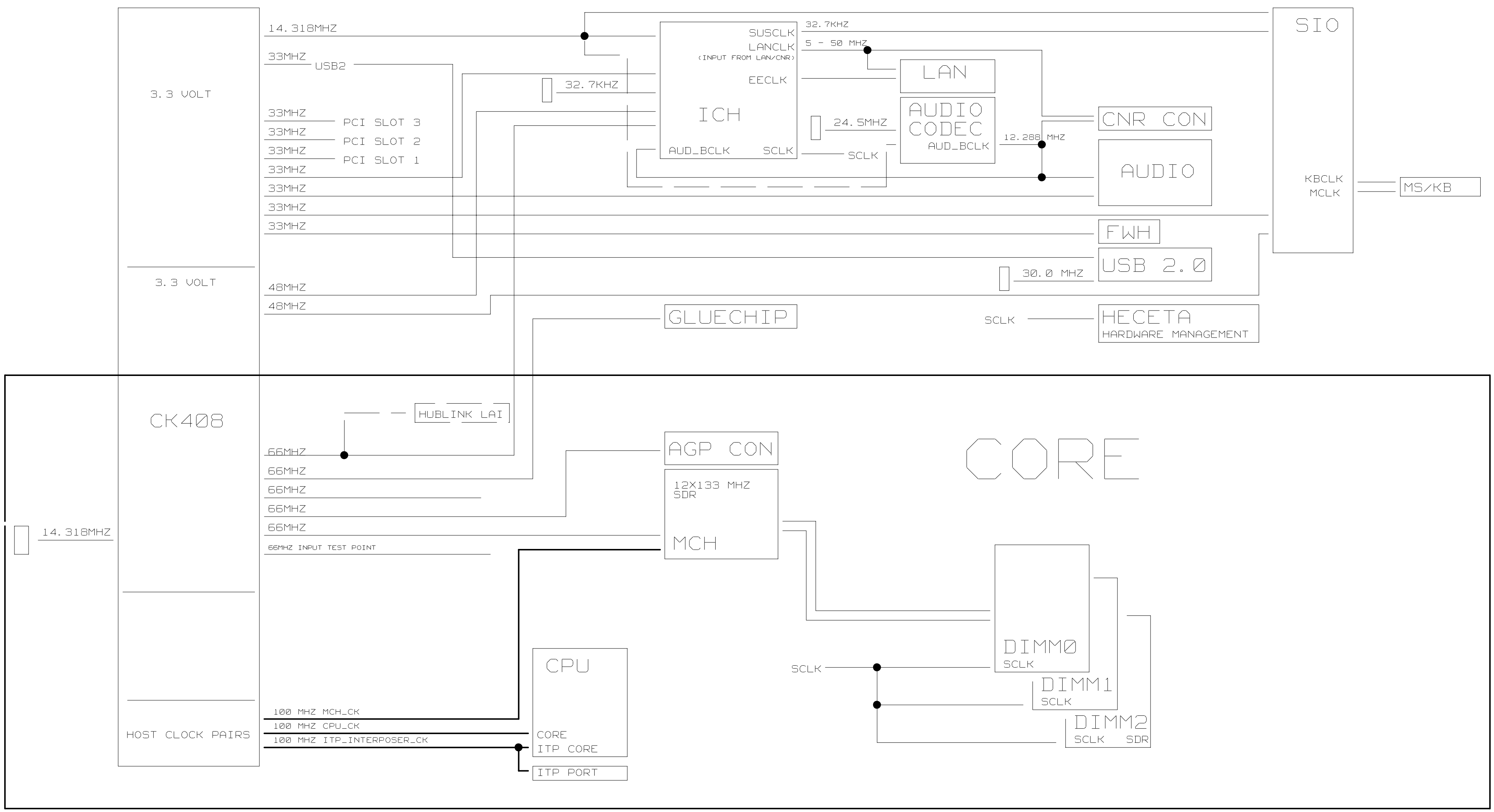

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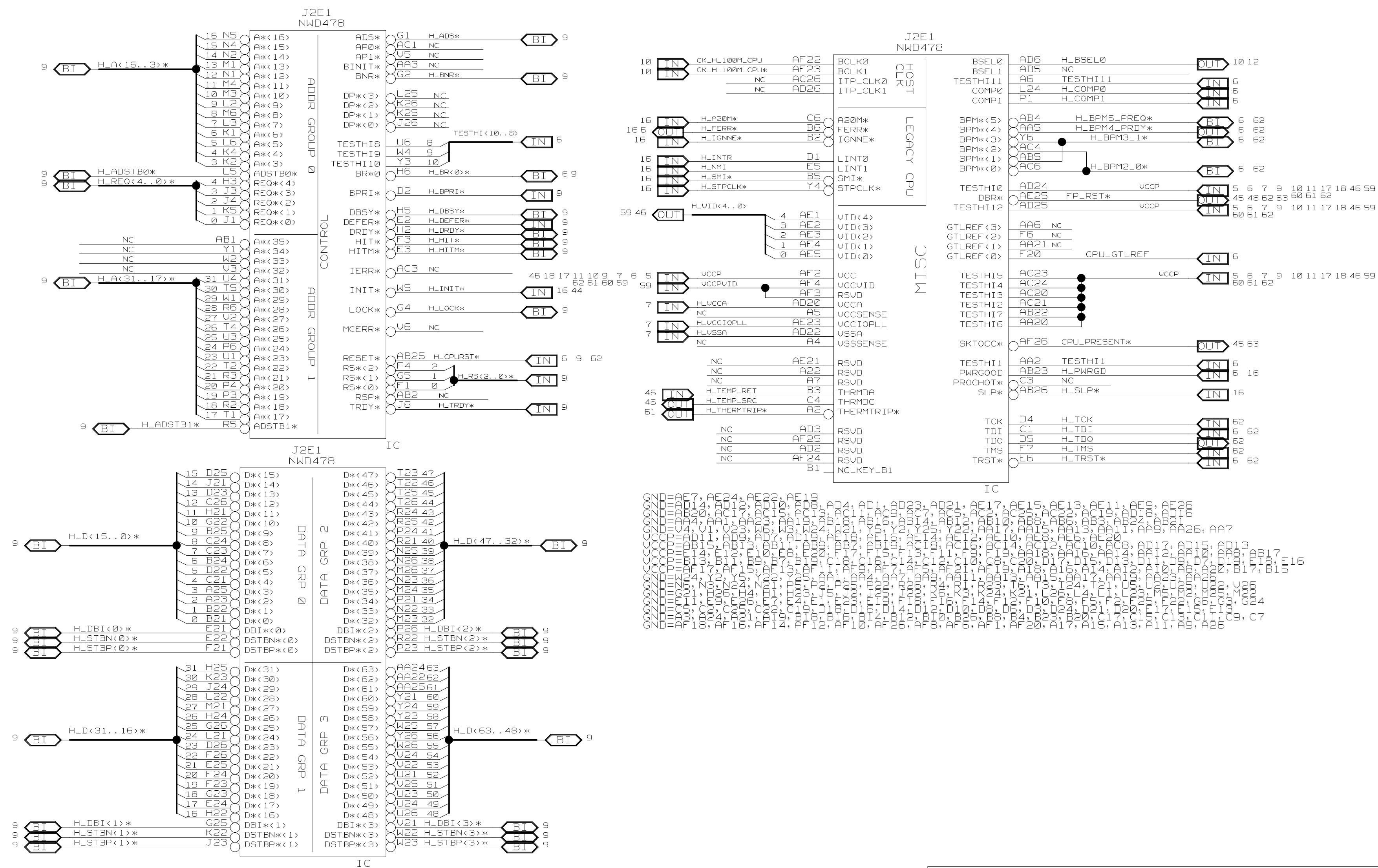

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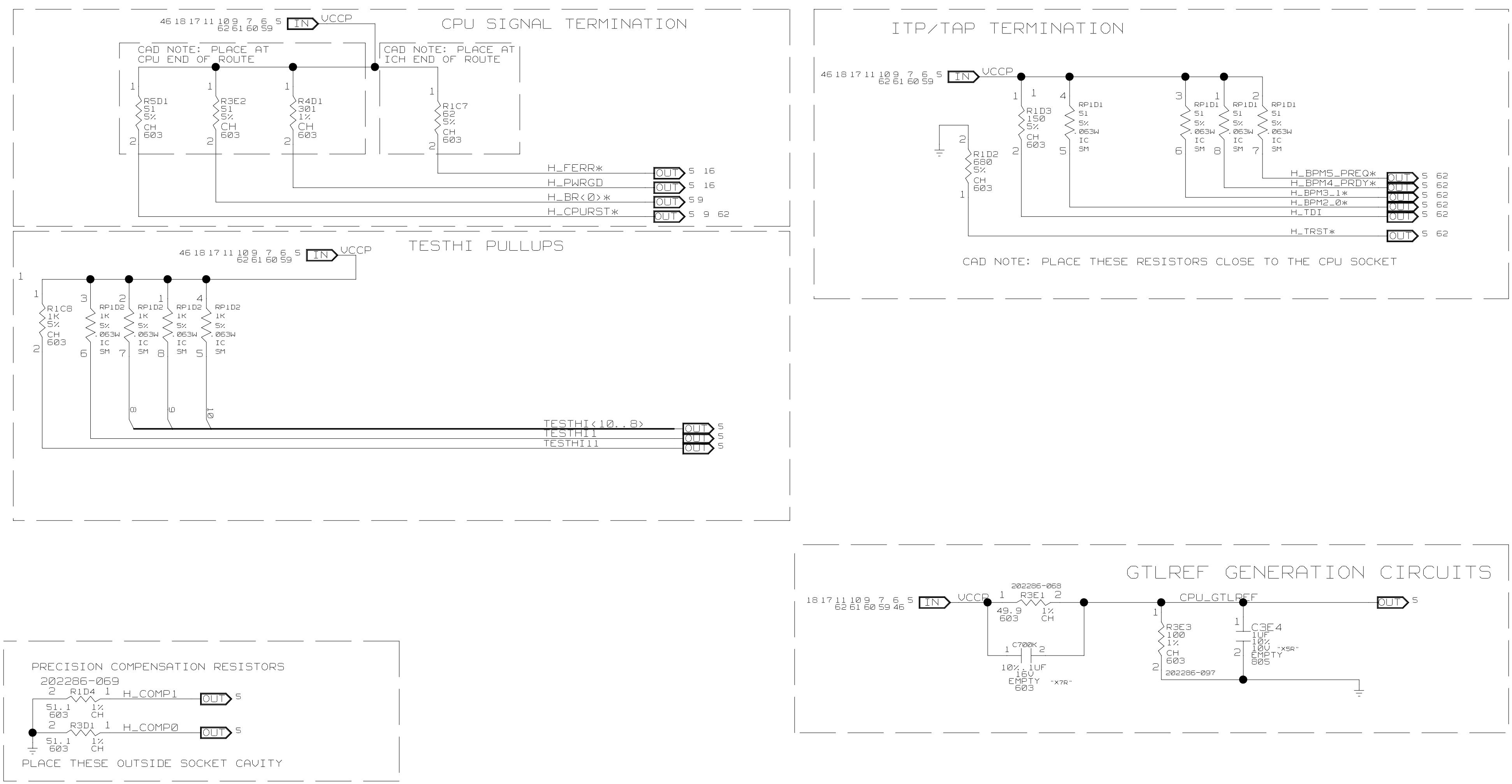

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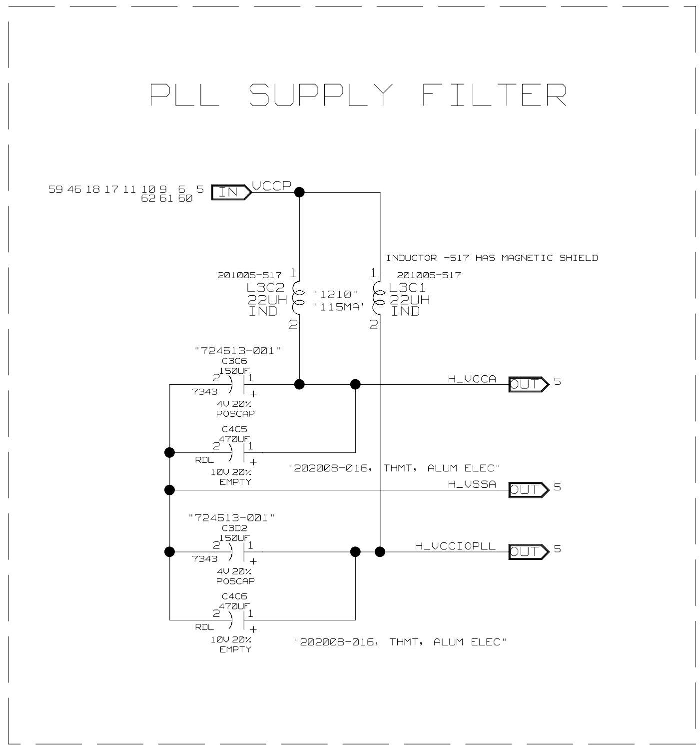

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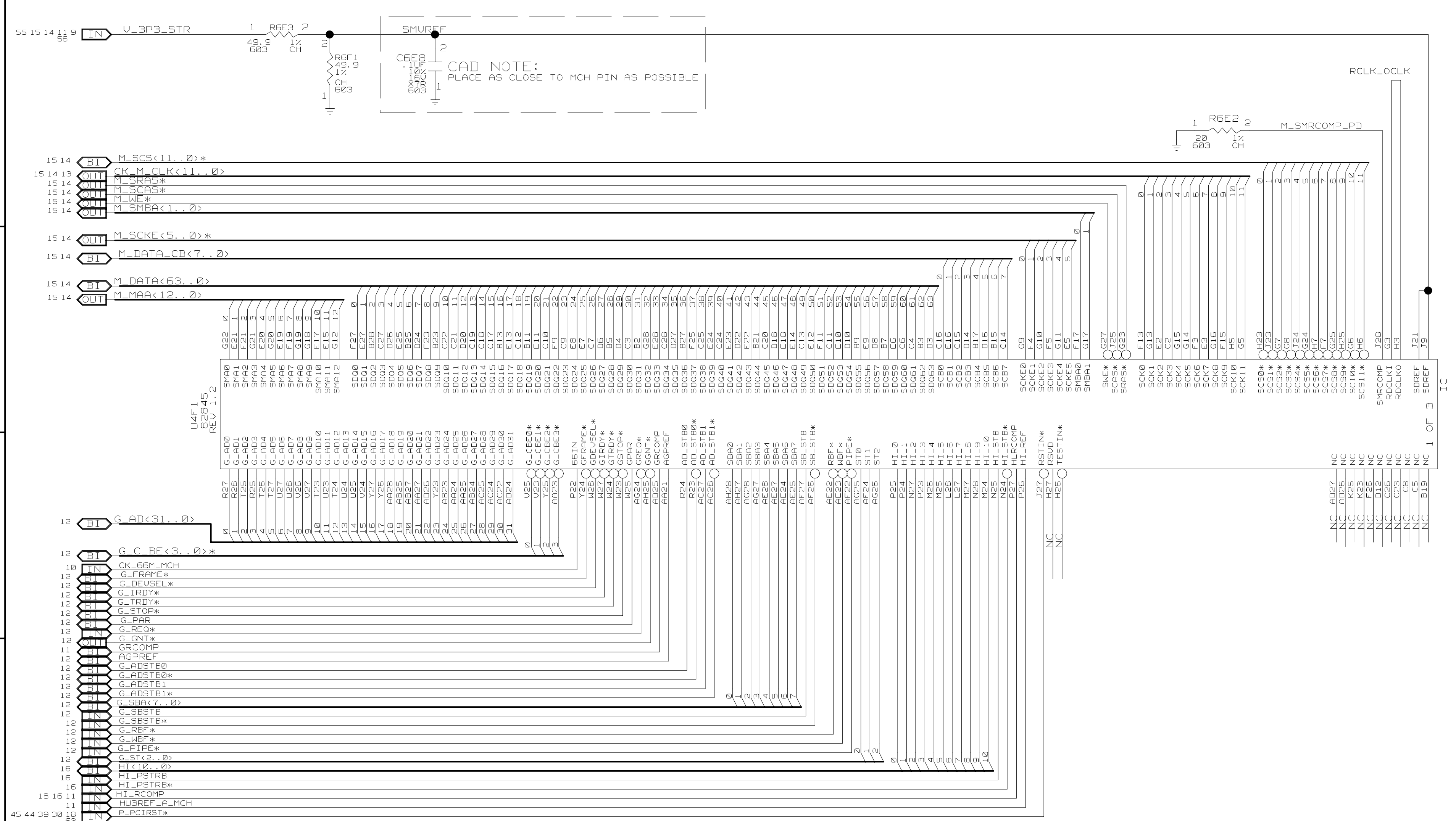

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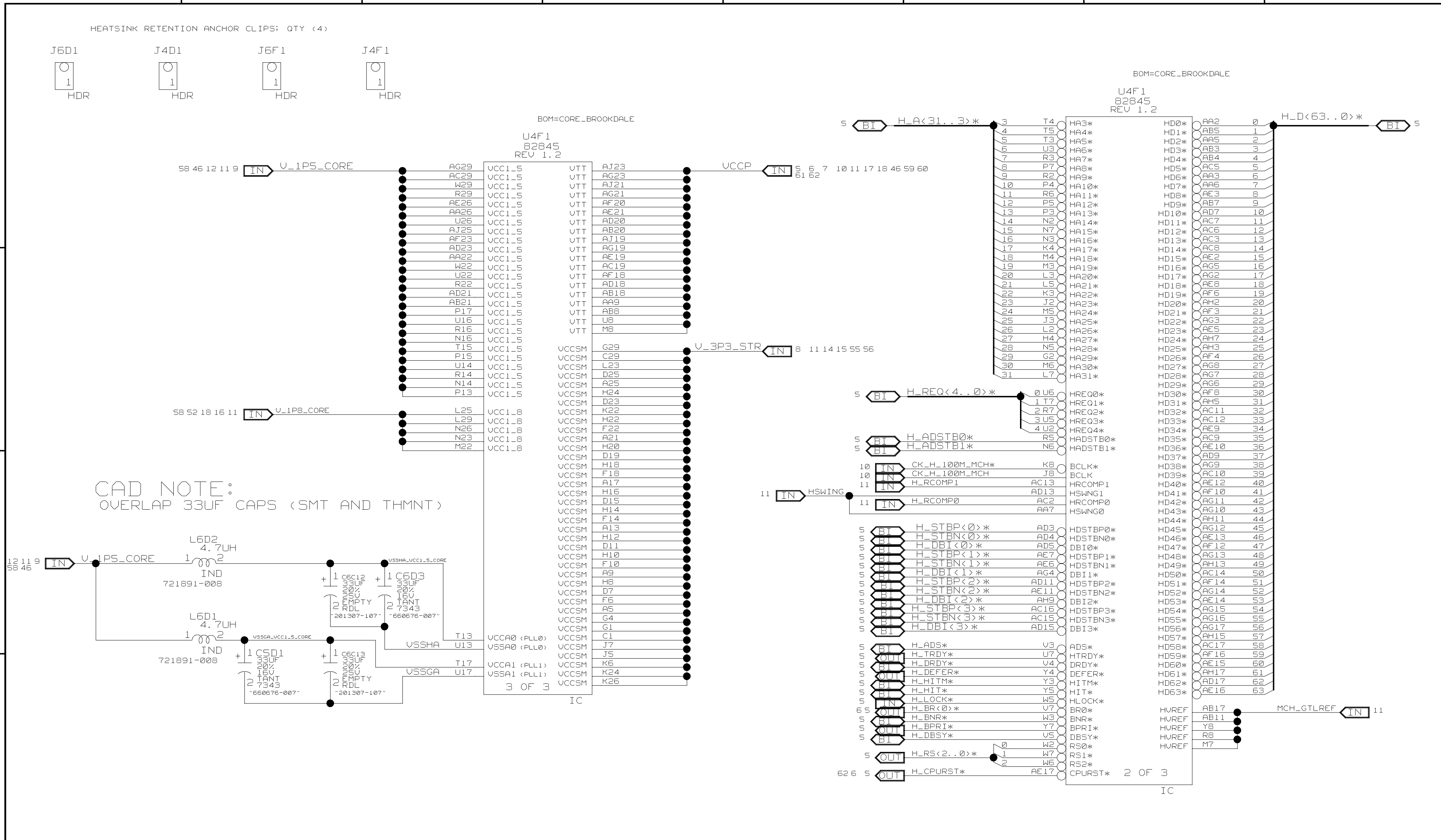

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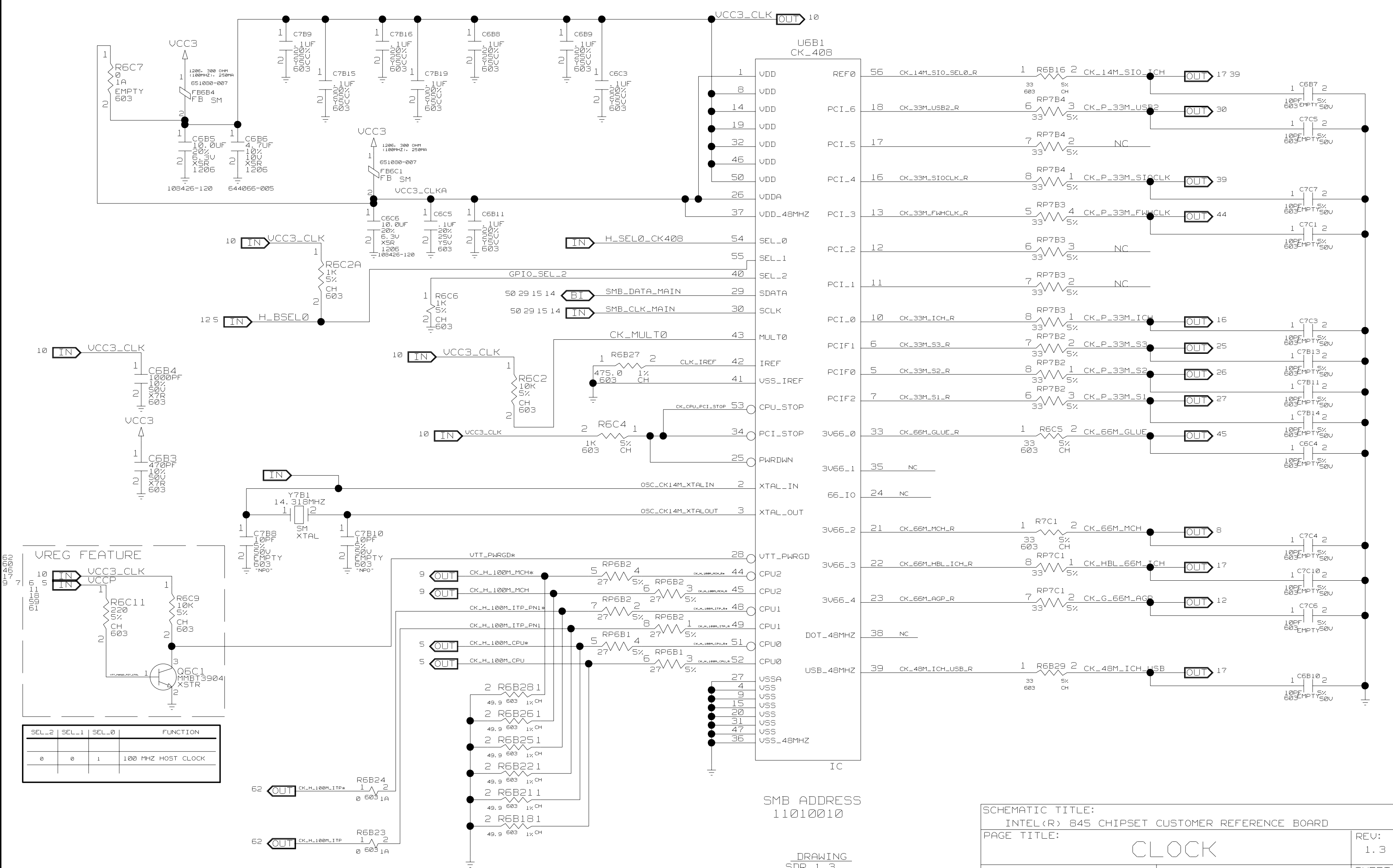

SEL_2	SEL_1	SEL_0	FUNCTION
0	0	1	100 MHZ HOST CLOCK

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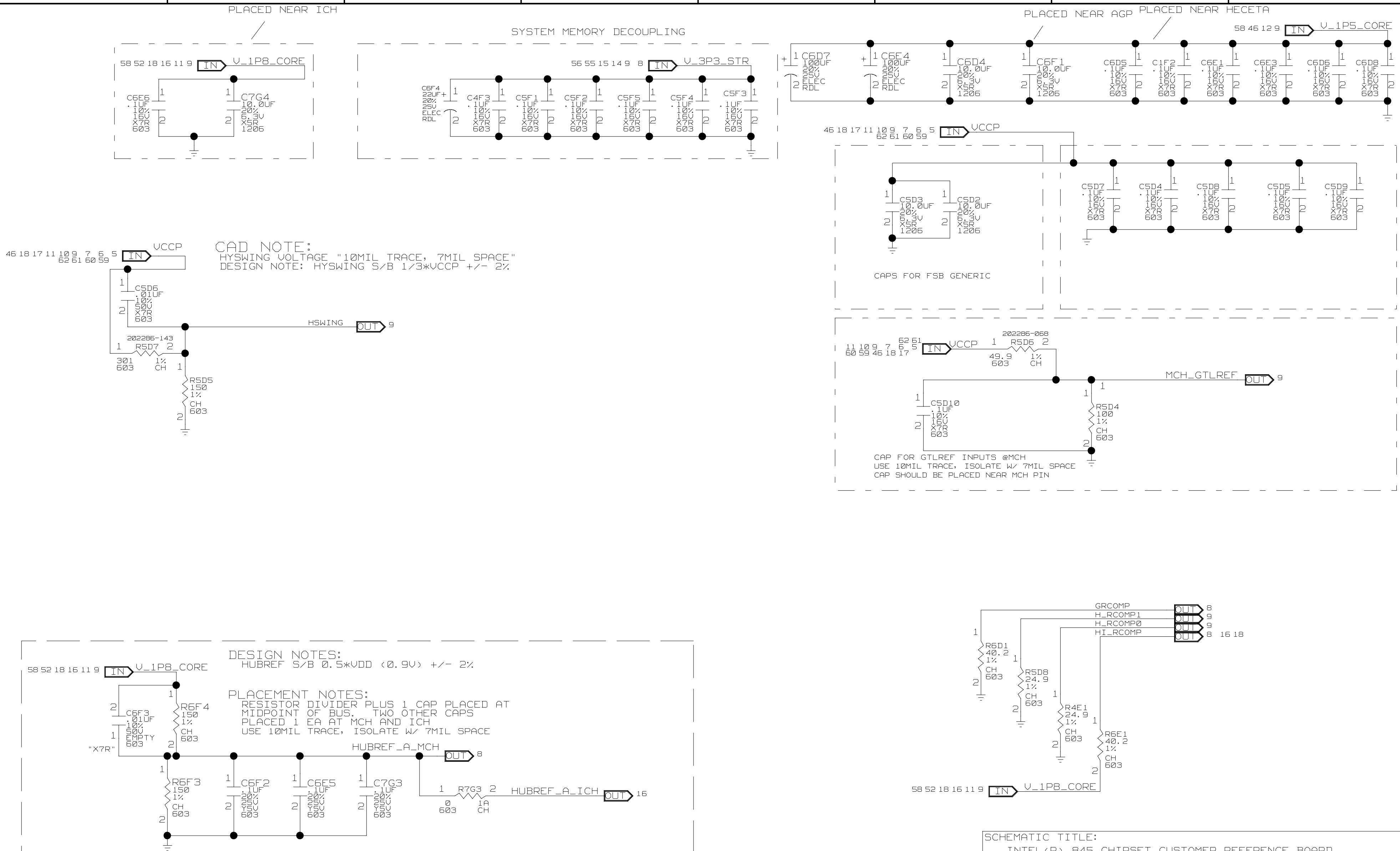


DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

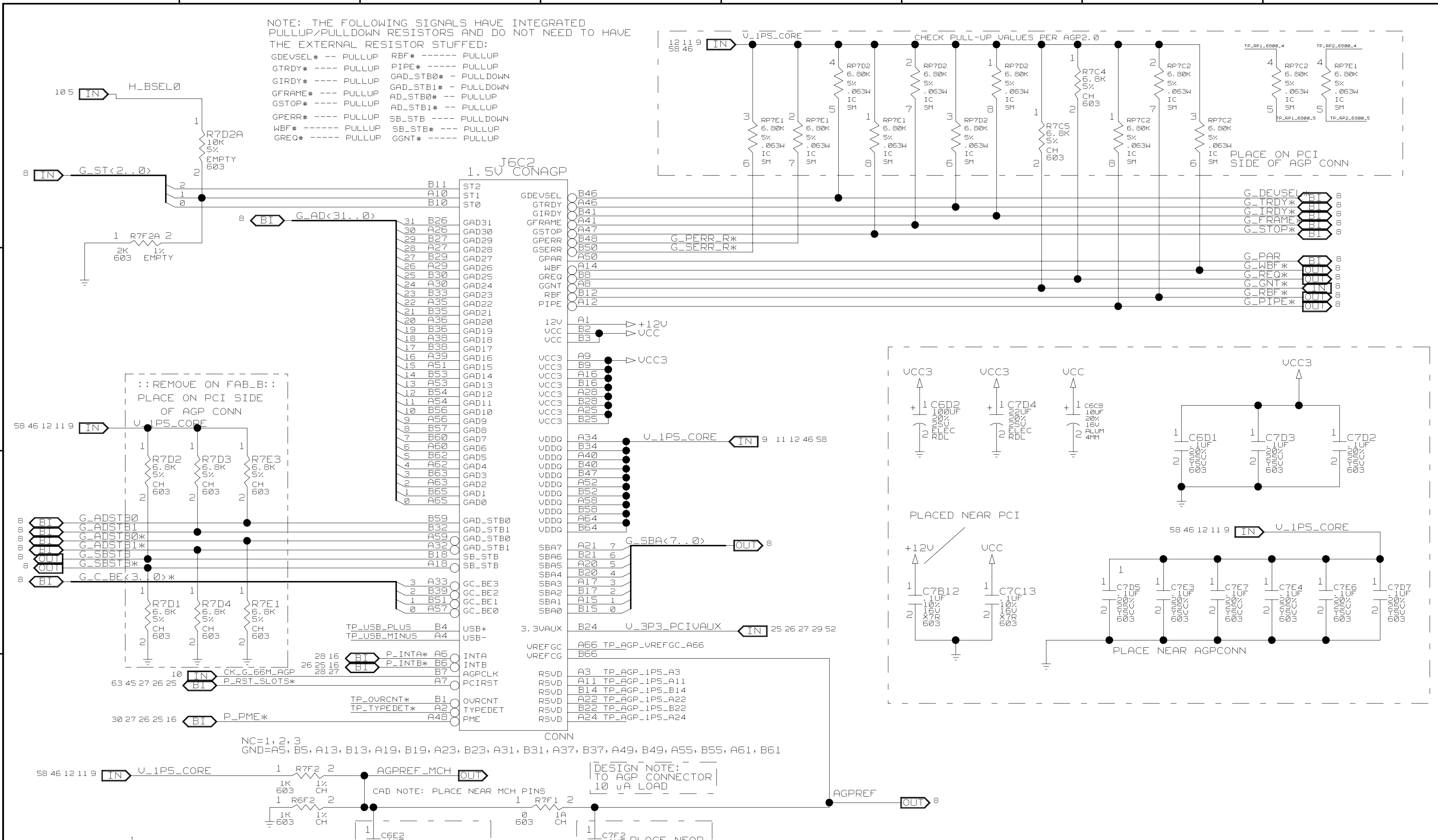
PAGE TITLE:
CHIPSET DECOUPLING, STRAPPING

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:50:21 2001

SHEET: 11



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

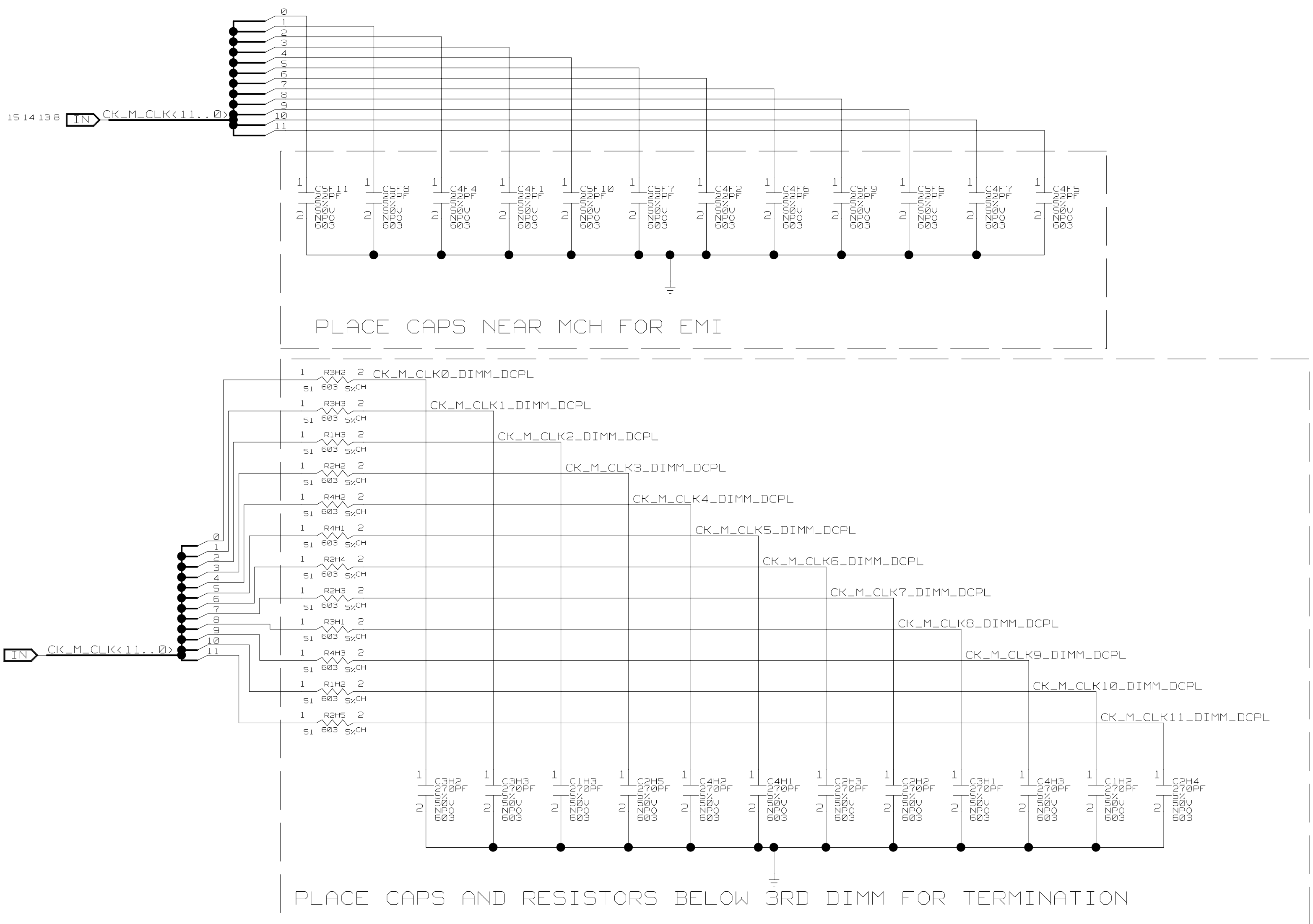
PAGE TITLE: AGP CONNECTOR

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:50:12 2001

SHEET: 12



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SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

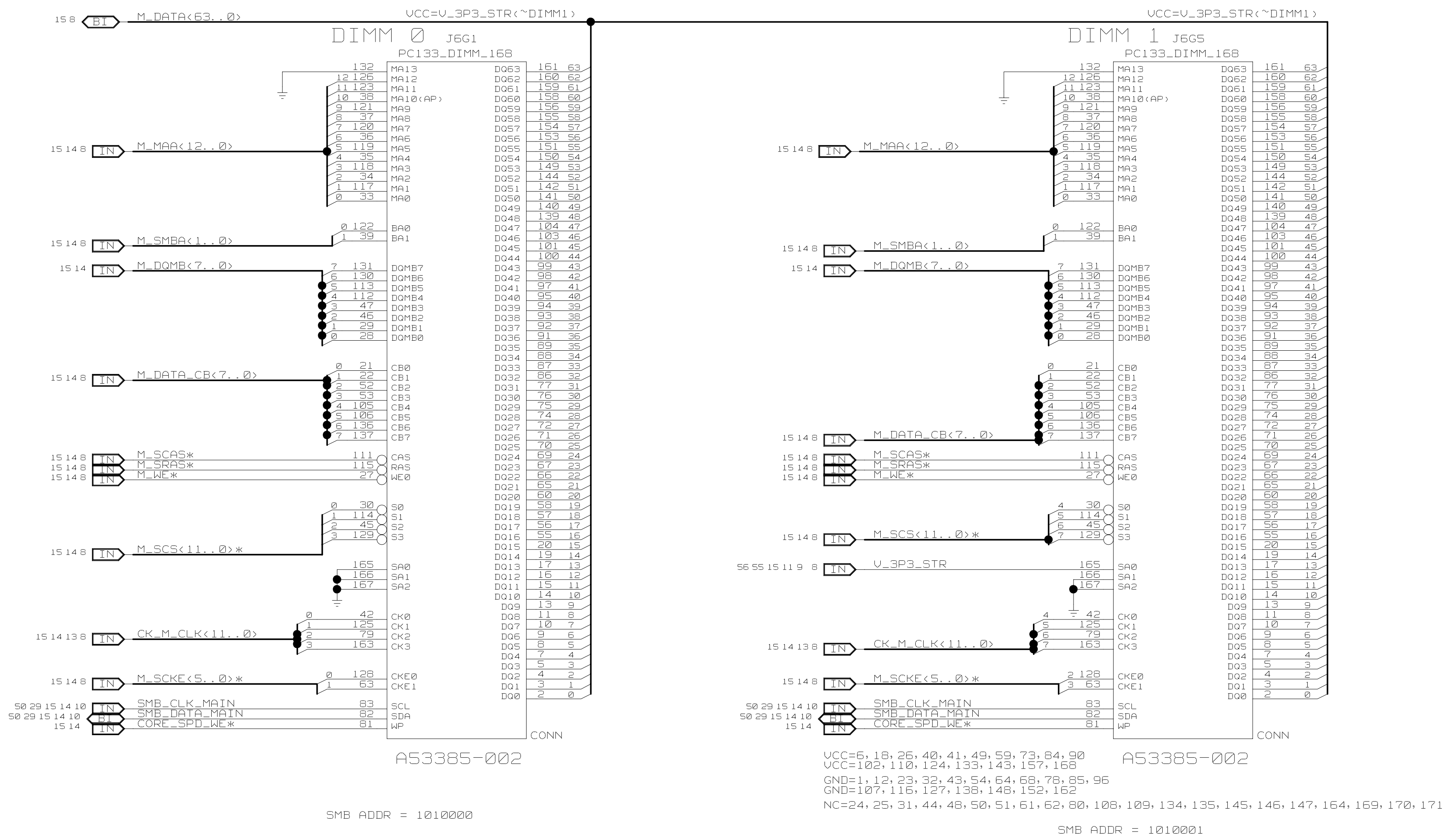
PAGE TITLE:
DIMM TERMINATION/DECOUPLING

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
Tue Aug 28 15:50:02 2001

SHEET: 13

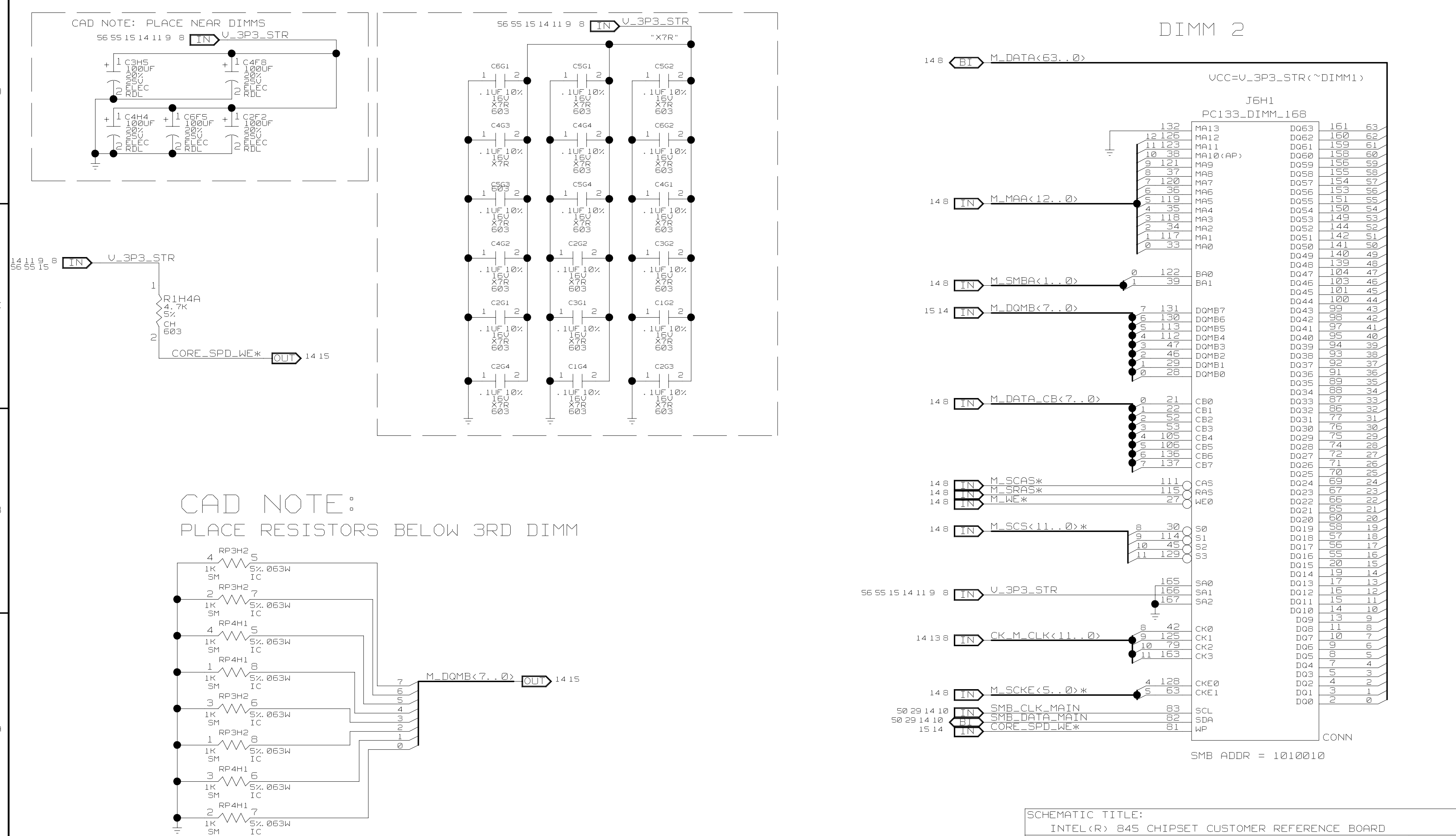


DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: SDRAM CORE		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:49:52 2001	SHEET: 14

CR-14

DIMM 2



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

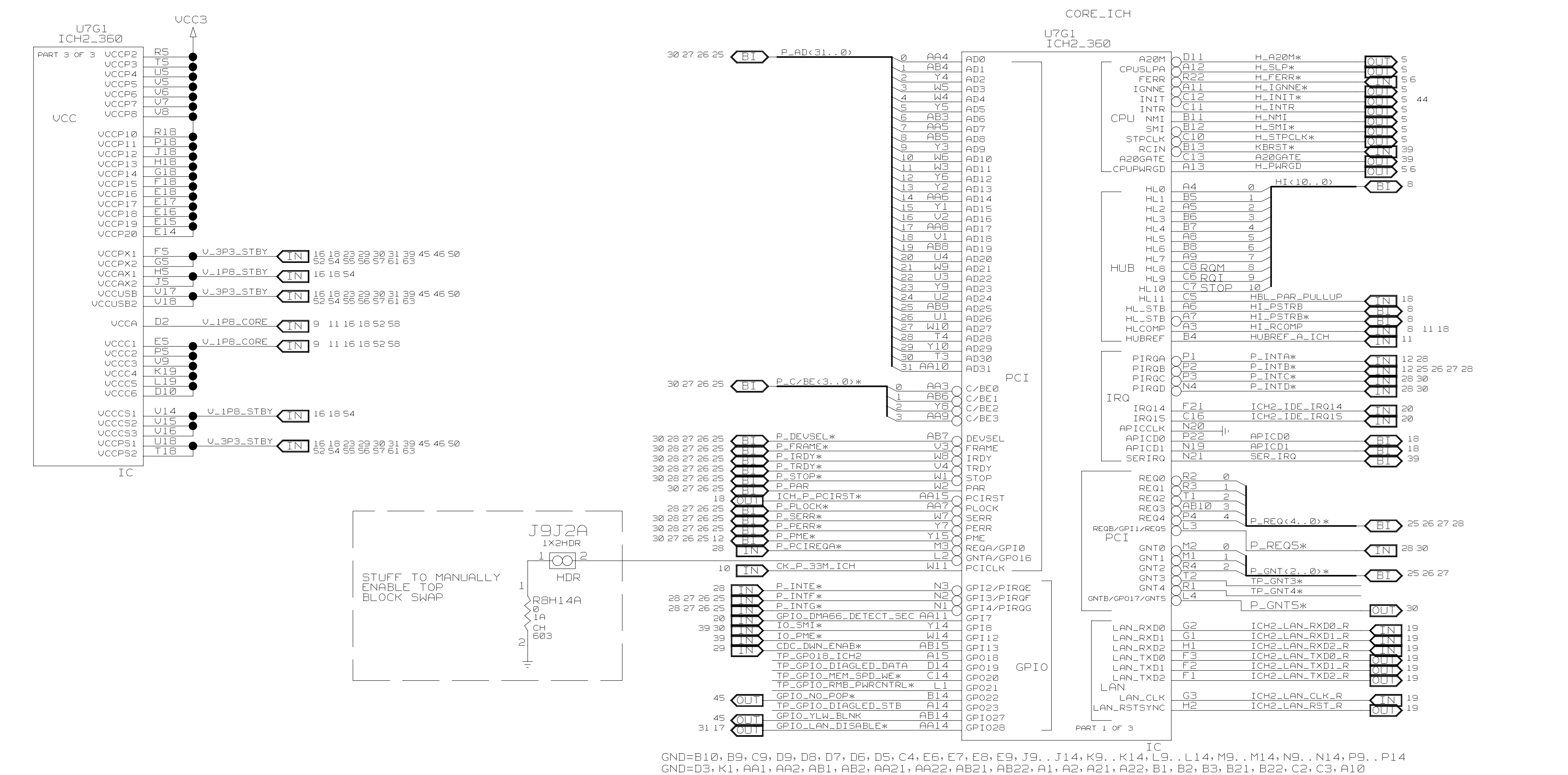
PAGE TITLE: SDRAM CORE

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:49:43 2001

SHEET: 15



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

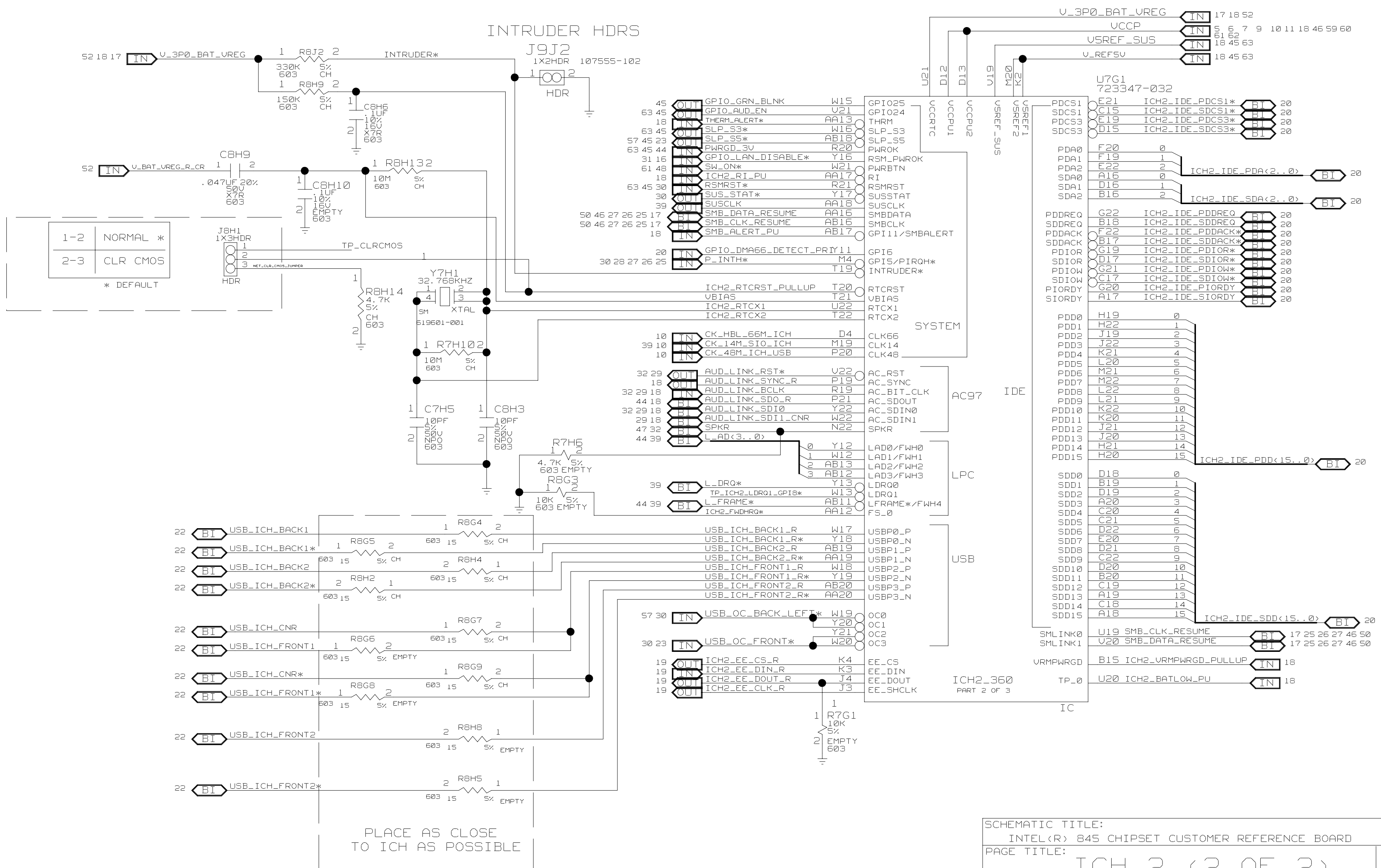
PAGE TITLE: ICH 2 (1 OF 2)

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

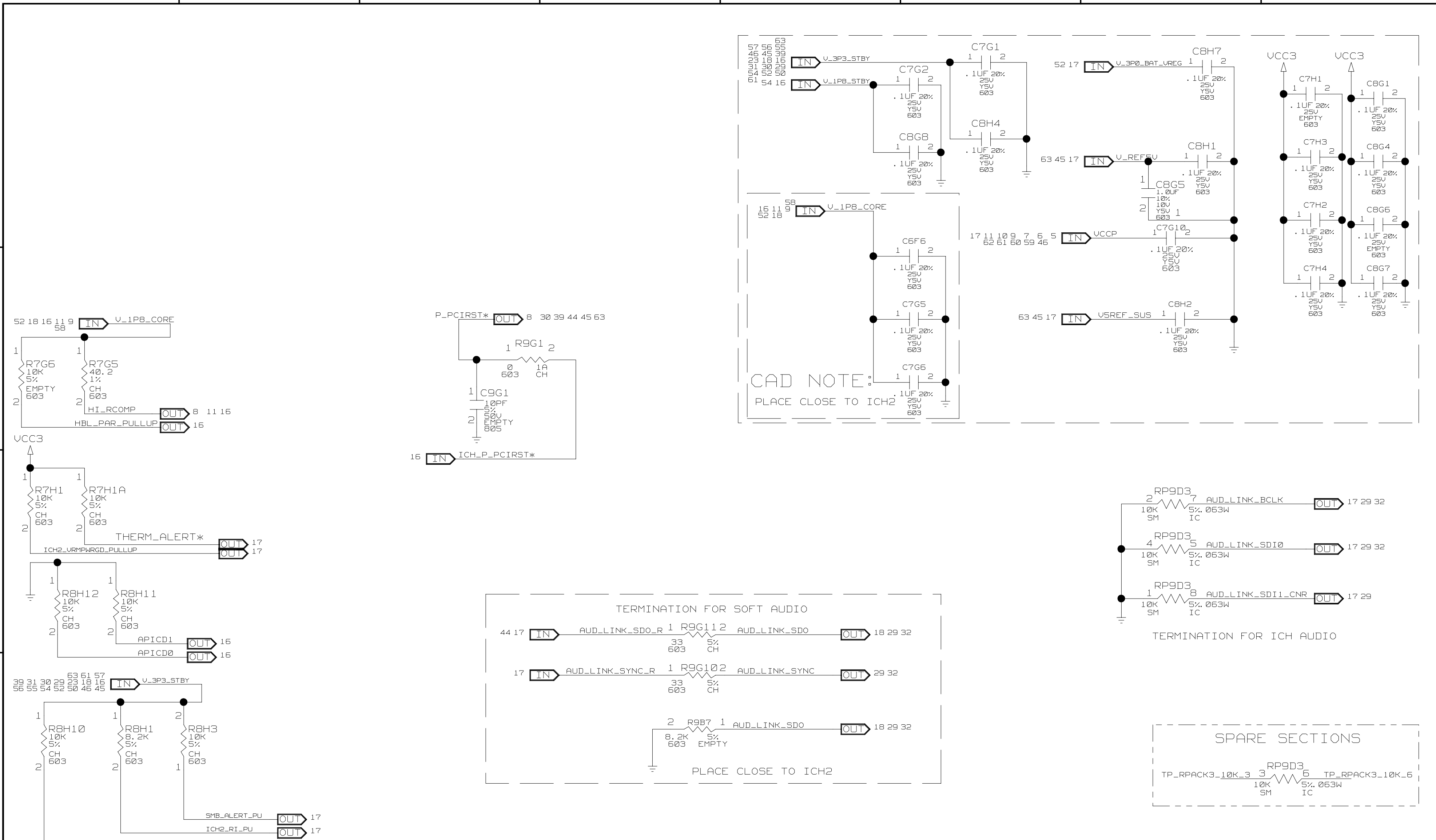
LAST REVISED: Tue Aug 28 15:49:34 2001

SHEET: 16



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: ICH 2 (2 OF 2)		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:49:24 2001	SHEET: 17



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
ICH2 PULLUPS & DECOUPLING

REV: 1.3

INTEL PLATFORM APPS ENG.
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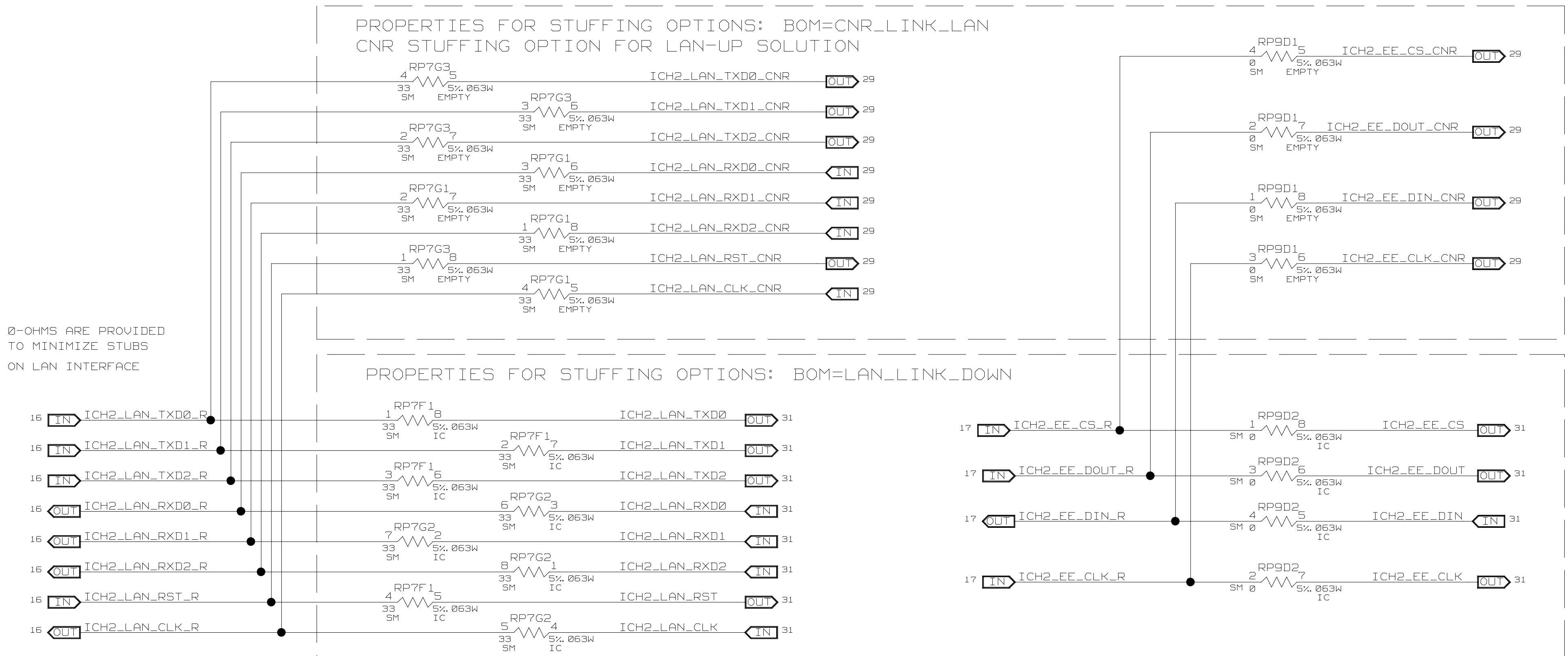
LAST REVISED: Tue Aug 28 15:49:13 2001

SHEET: 18

ICH2 AC97 AND CNR LINK STUFFING OPTION PAGE

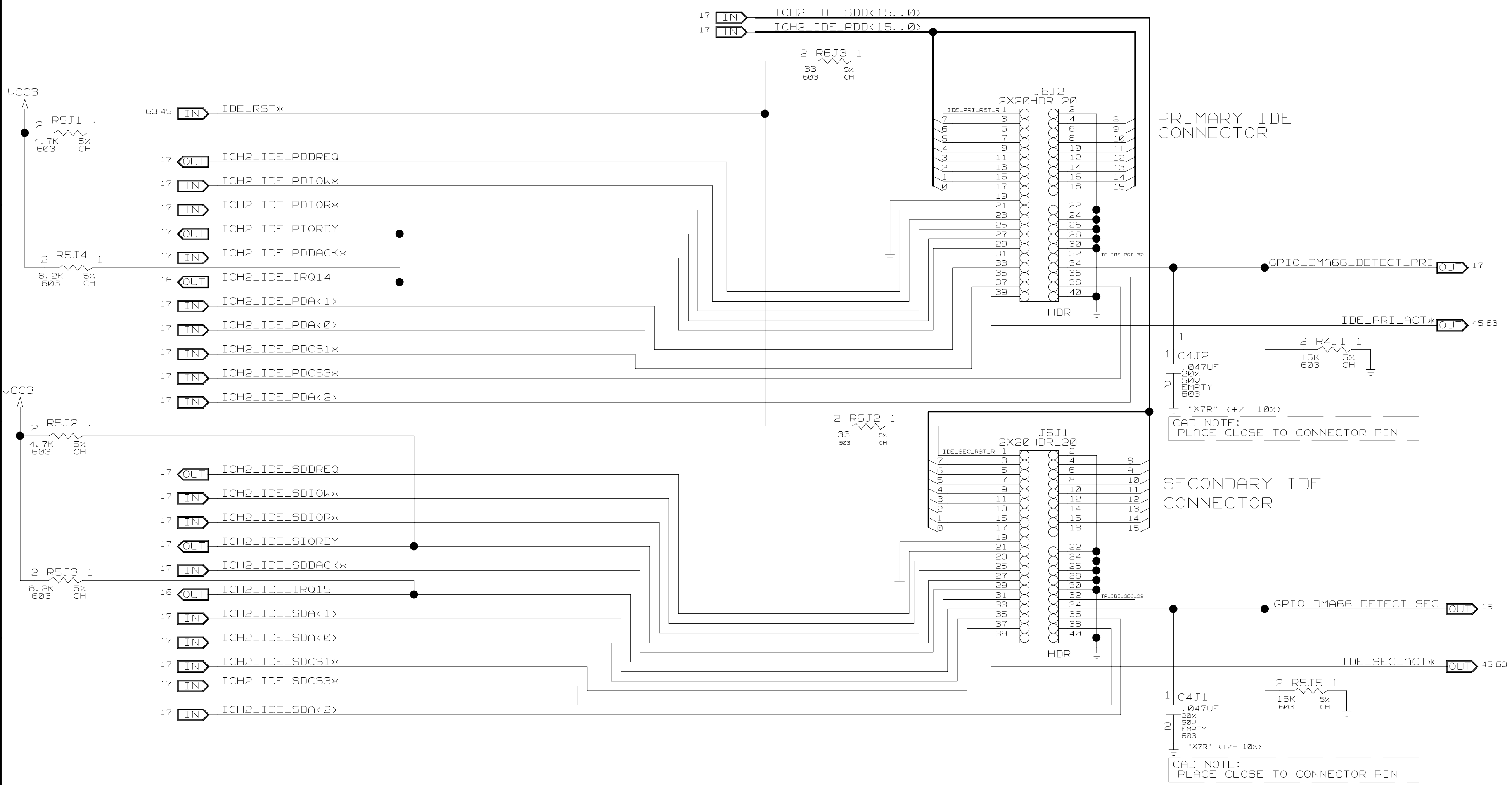
STUFF ONE OR THE OTHER NOT BOTH



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AC97/CNR LINK STUFFING OPTIONS		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:49:04 2001	SHEET: 19

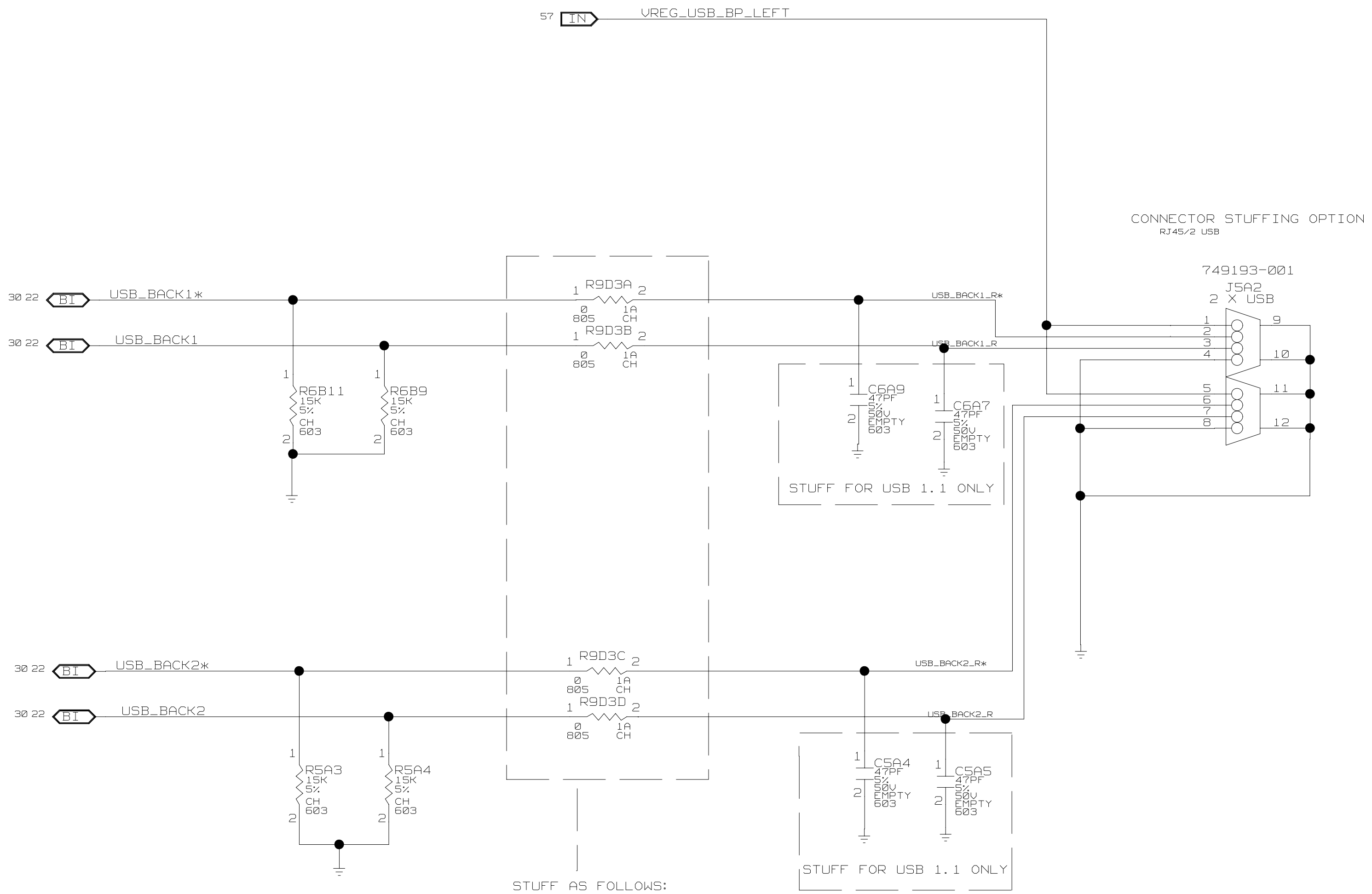
CR-19



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: IDE PORTS		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:48:55 2001	SHEET: 20

CR-21

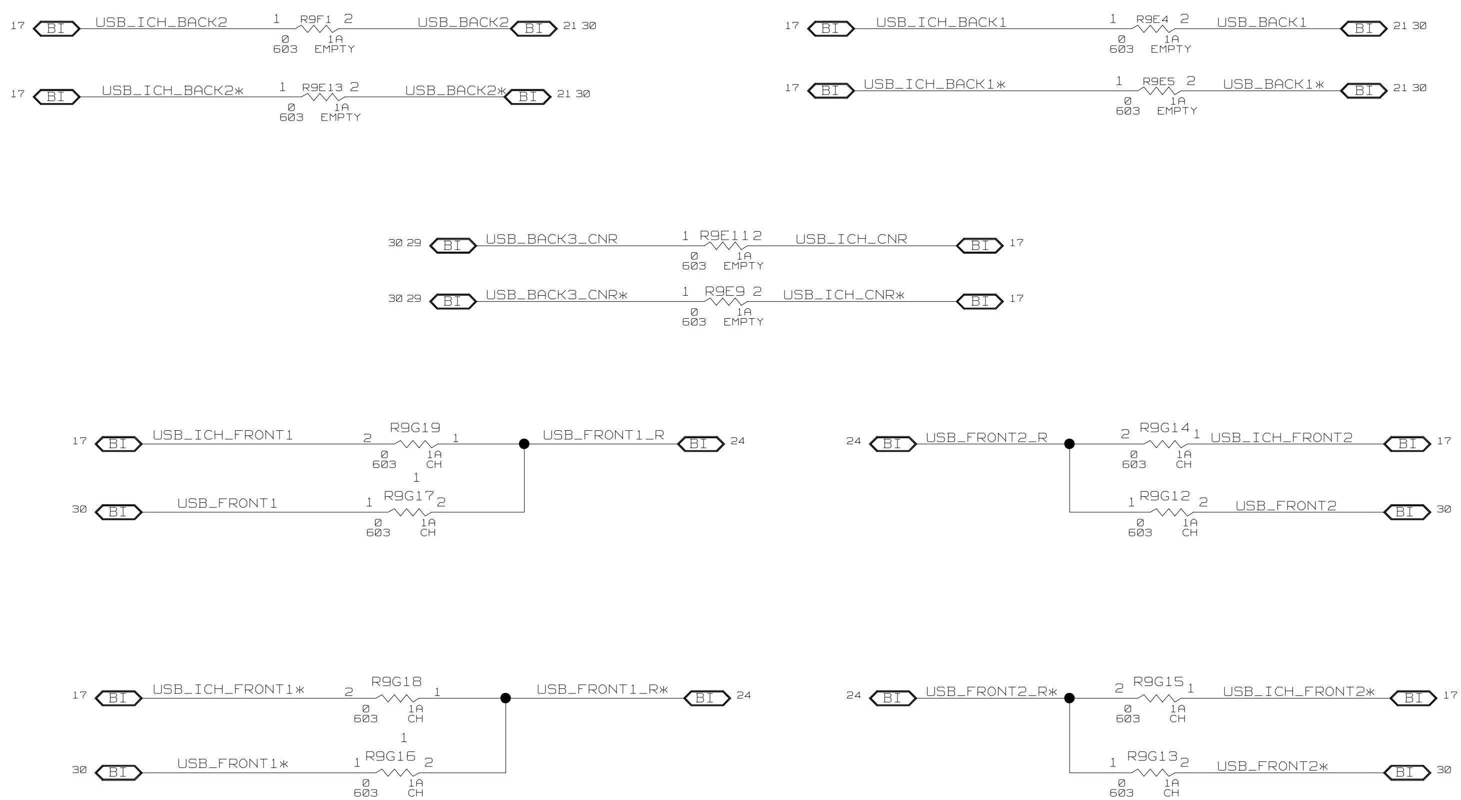


STUFF AS FOLLOWS:
USB 2.0 OR 1.1 = 0 OHM RESISTORS
USB 2.0 WITH EMI ISSUES = COMMON MODE CHOKE
USB 1.1 WITH EMI ISSUES = FERRITE BEADS

DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: USB BACKPANEL	REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630 — LAST REVISED: Tue Aug 28 15:48:46 2001	SHEET: 21

USB SWITCH PAGE



DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

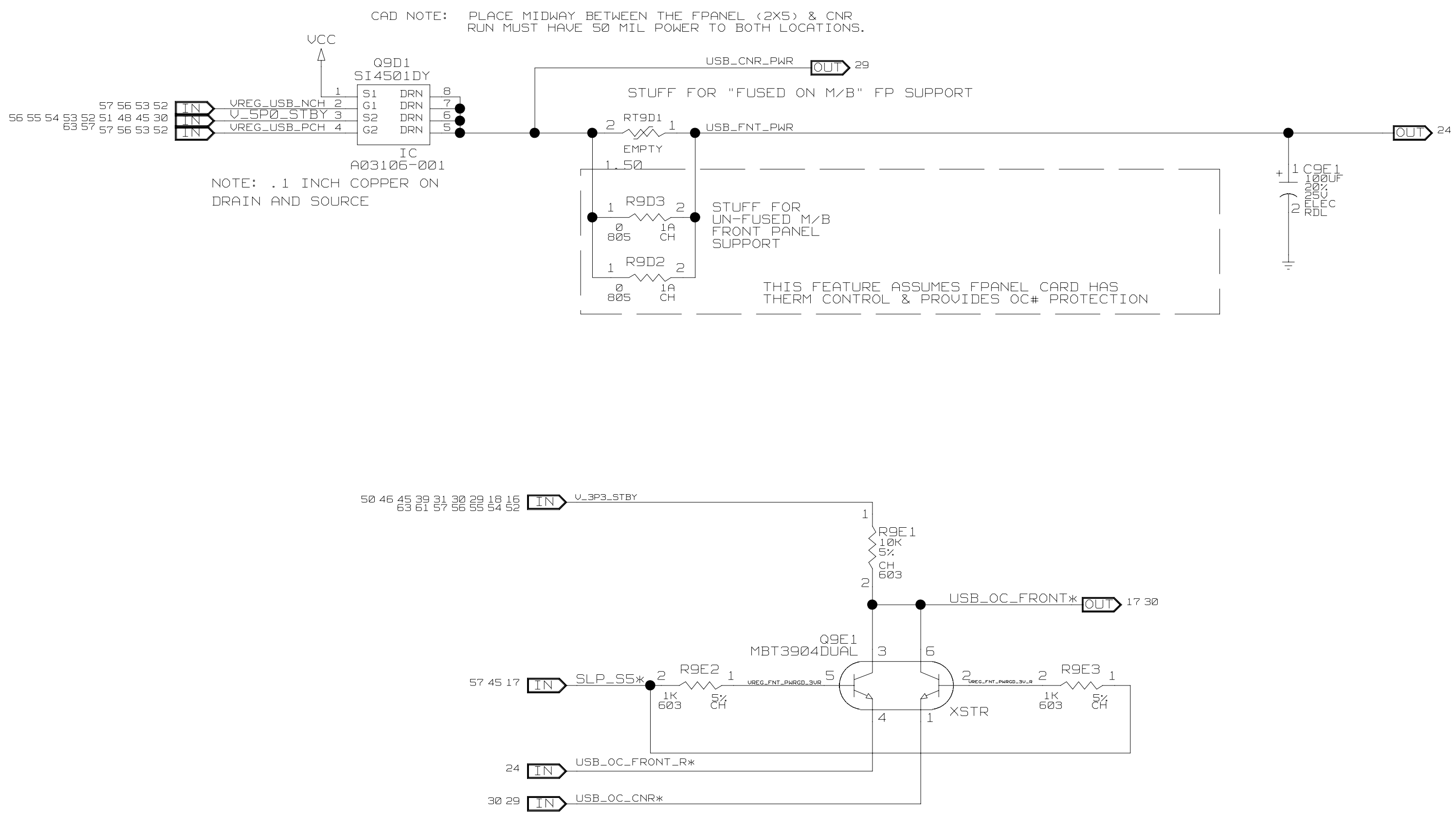
PAGE TITLE:
USB SWITCH PAGE

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:48:37 2001

SHEET: 22



DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
USB FNT PANEL POWER

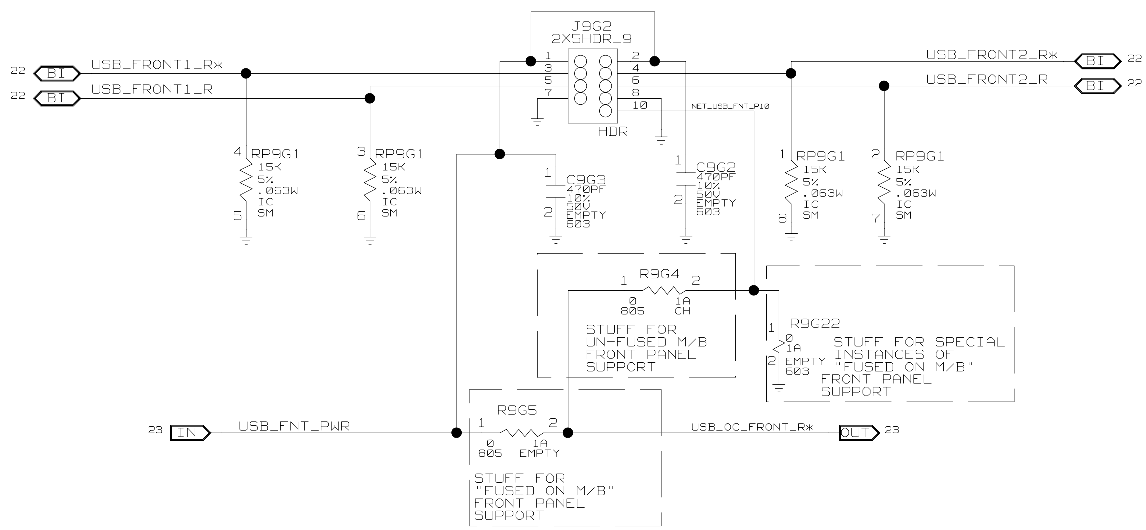
REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:48:28 2001

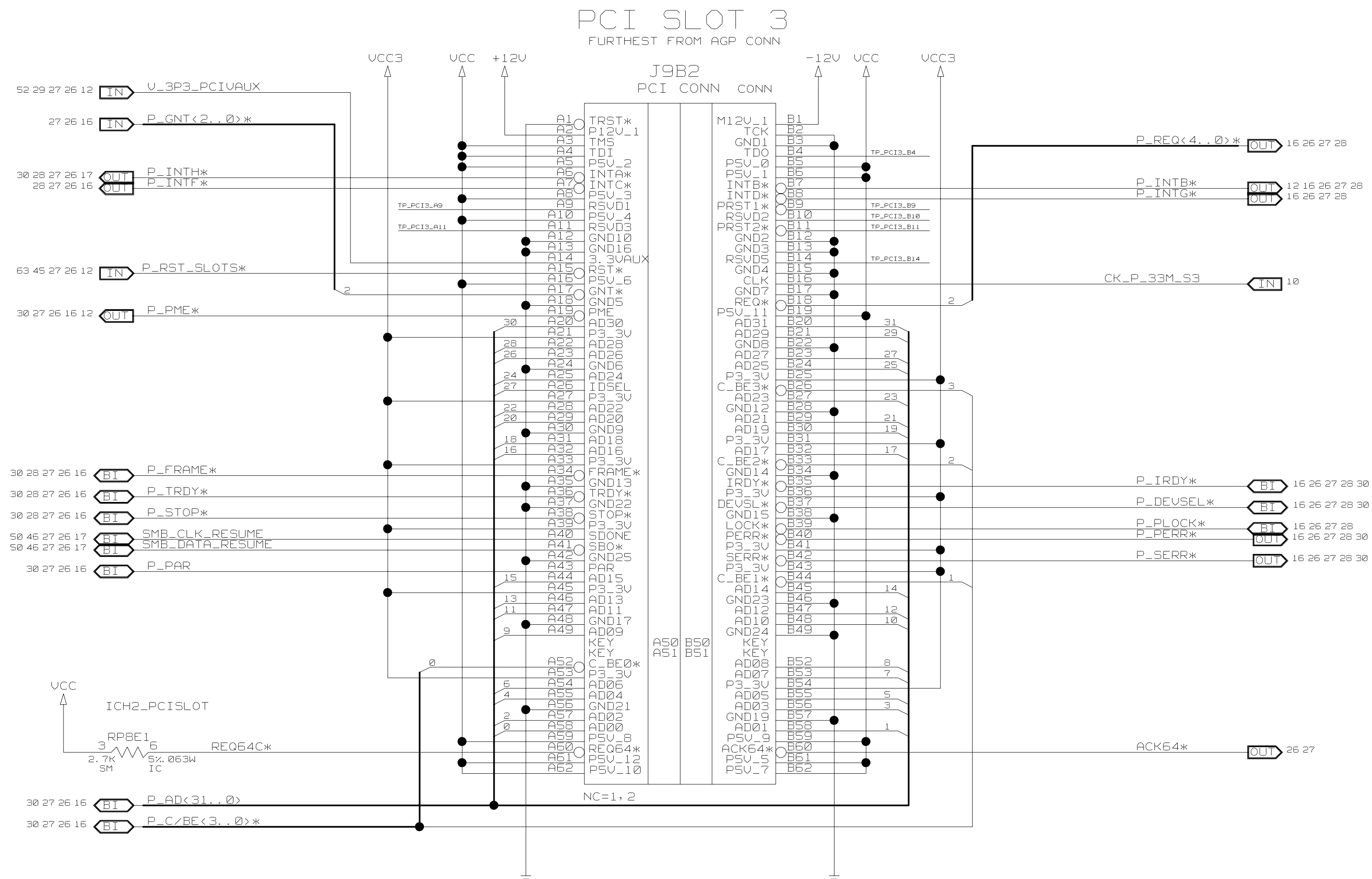
SHEET: 23

CR-23



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB FNT PANEL HEADER		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:48:20 2001	SHEET: 24



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: PCI SLOT 3

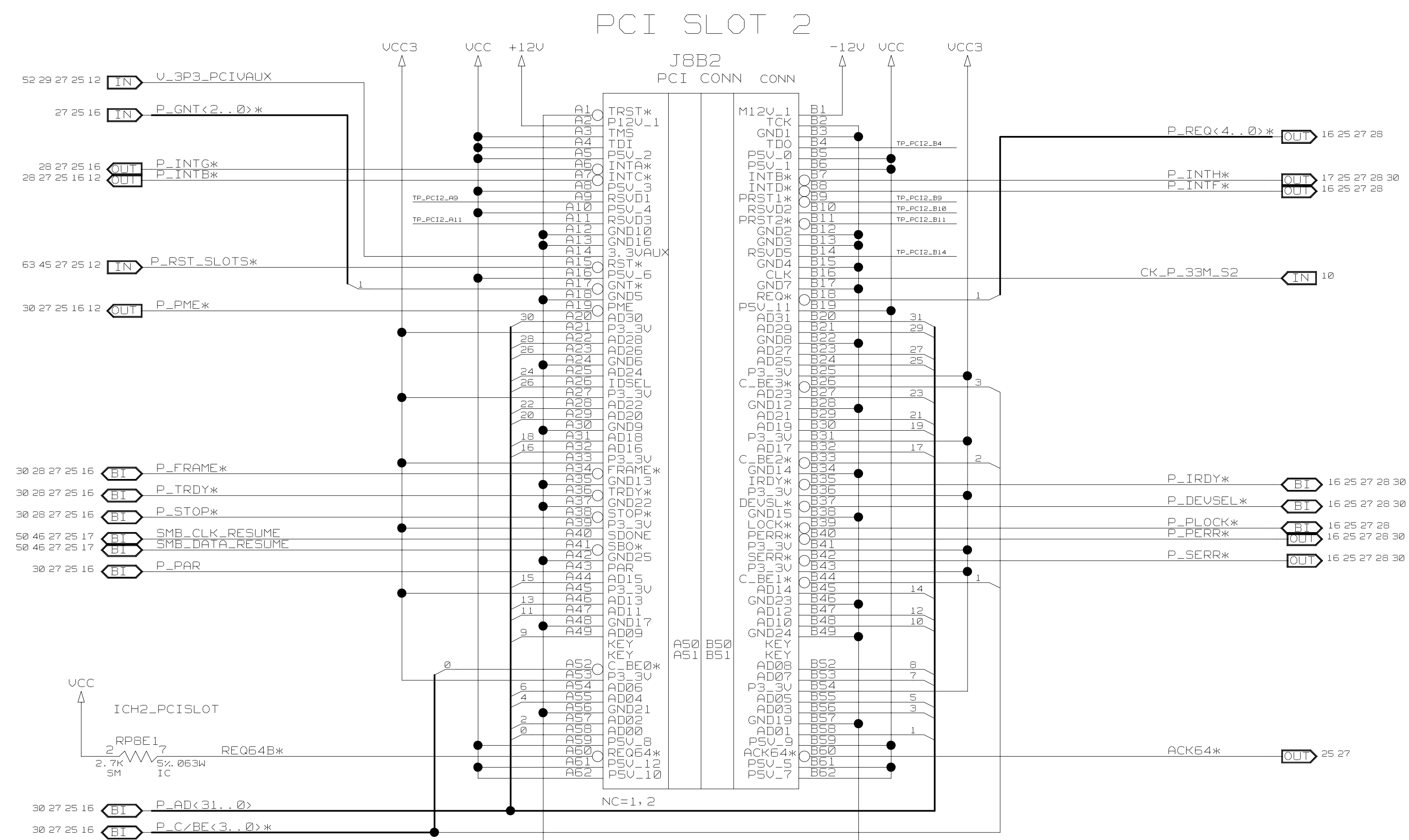
REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:48:10 2001

SHEET: 25

DRAWING
SDR_1_3



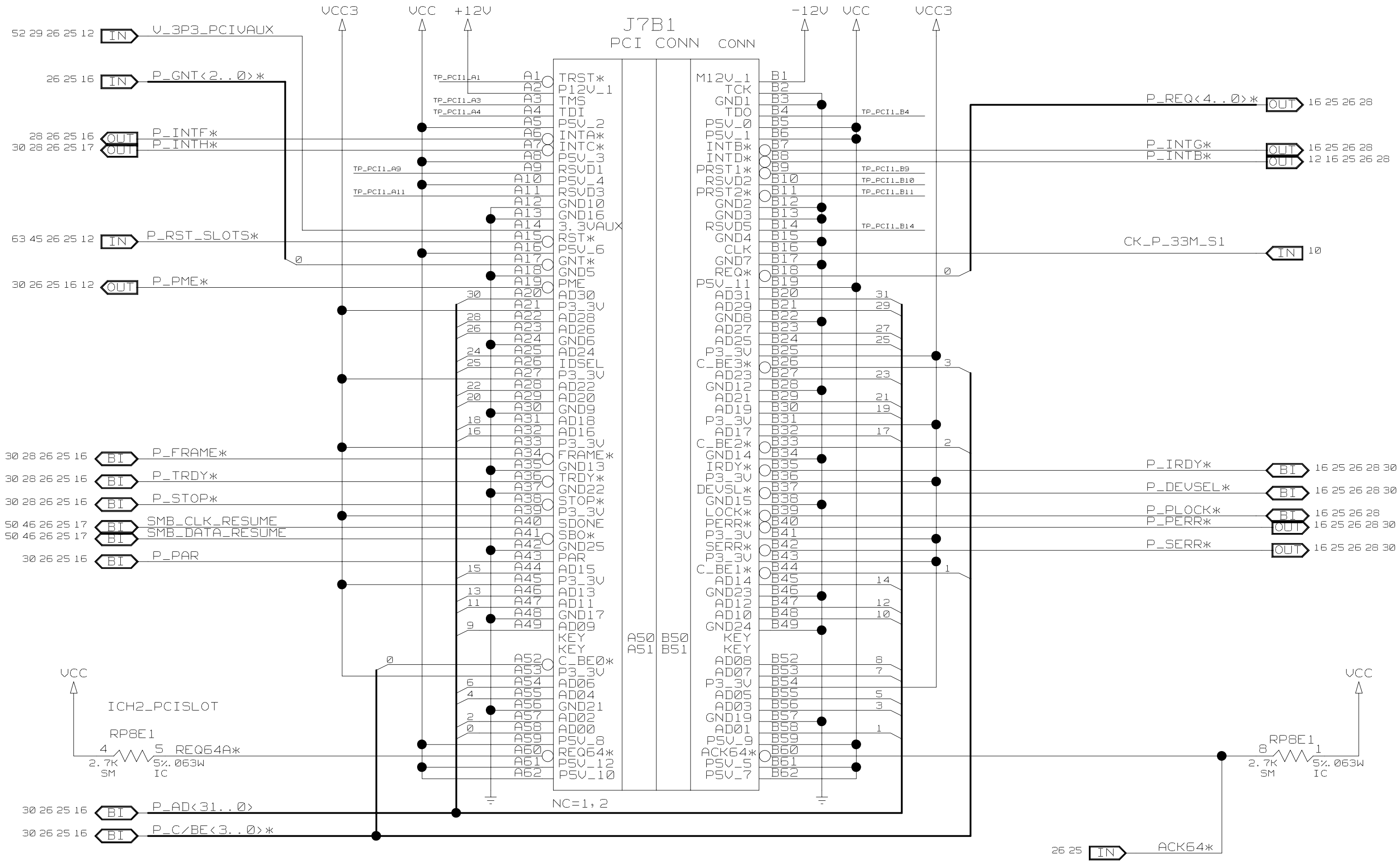
DESIGN NOTE:
PCI SLOT2 = PCI DEVICE #10
REQ/GNT PAIR = #1
IRQ MAP A : B : C : D
G : H : B : F

DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 2		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:48:02 2001	SHEET: 26

PCI SLOT 1

CLOSEST TO AGP CONN



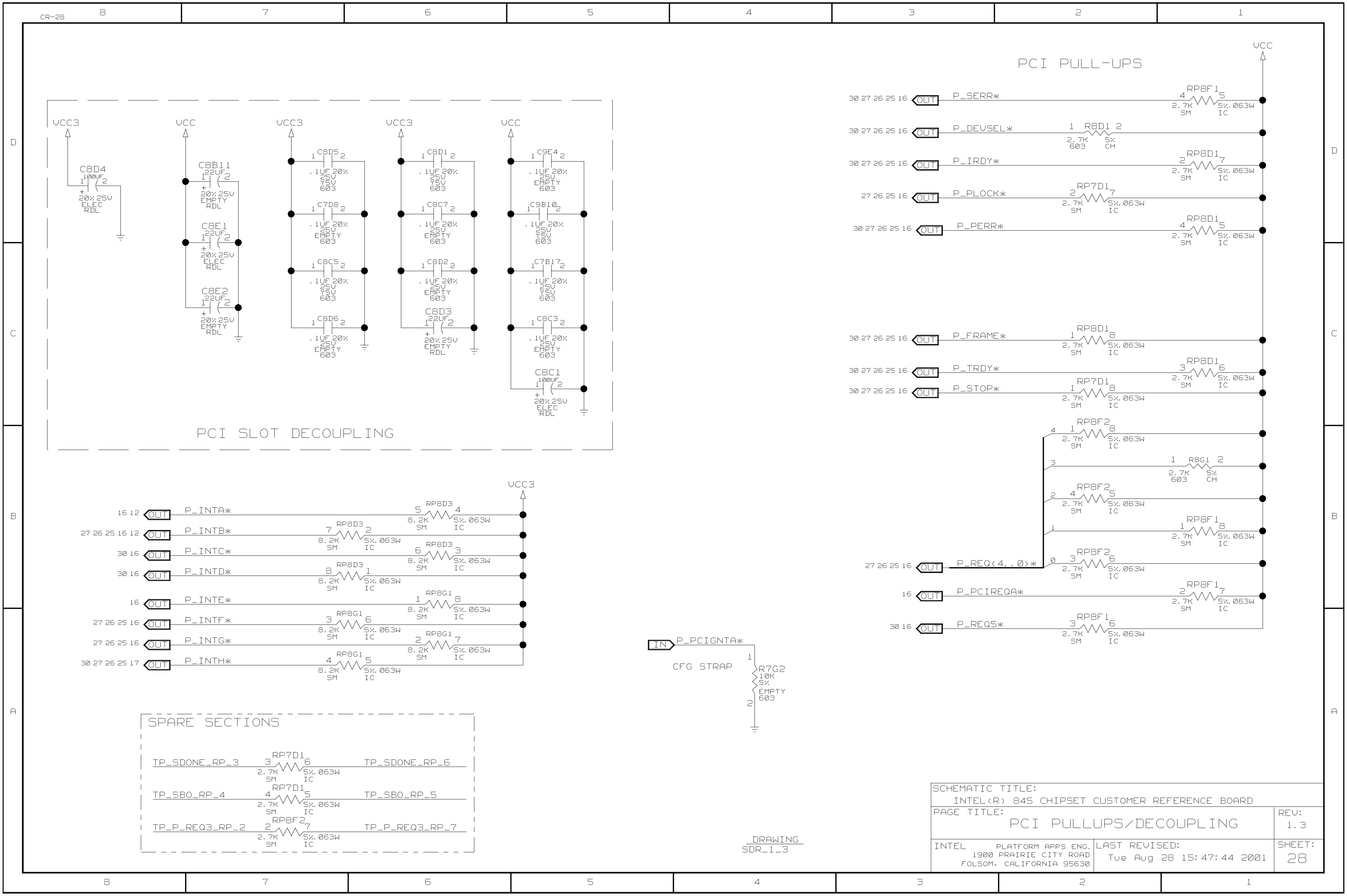
CAD NOTE:
MAKE PLACEMENT THE SAME AS ON THE EVAL BOARD
FOR TEST-POINTED, EMPTY RESISTOR SITES

DESIGN NOTE:
PCI SLOT1 = PCI DEVICE #09
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
F : G : H : B

DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 1		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:47:53 2001	SHEET: 27

CR-27



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

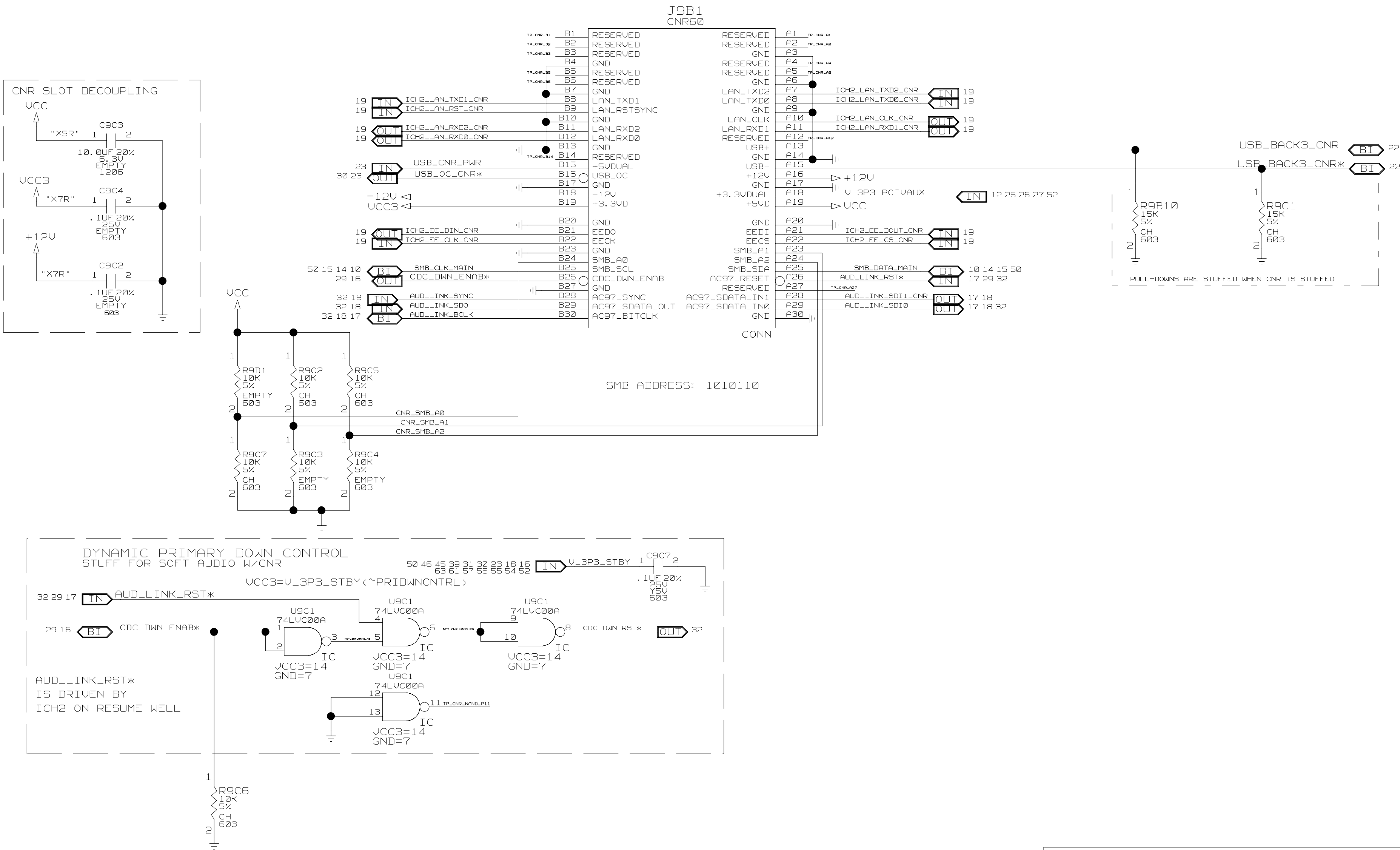
PAGE TITLE: PCI PULLUPS/DECOUPLING

REV: 1.3

INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

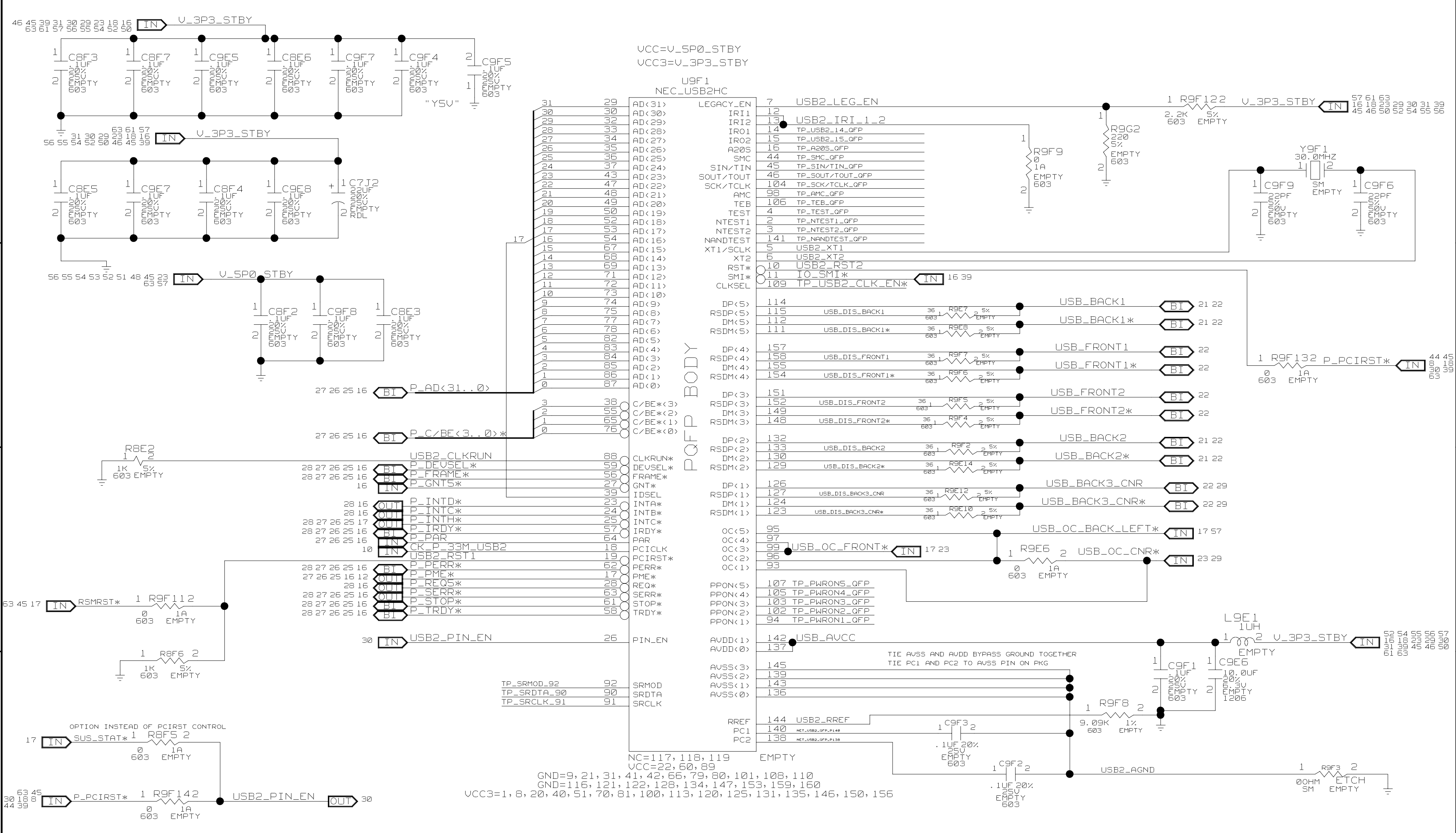
LAST REVISED: Tue Aug 28 15:47:44 2001

SHEET: 28



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CNR		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:47:35 2001	SHEET: 29



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
USB2P0 PQFP

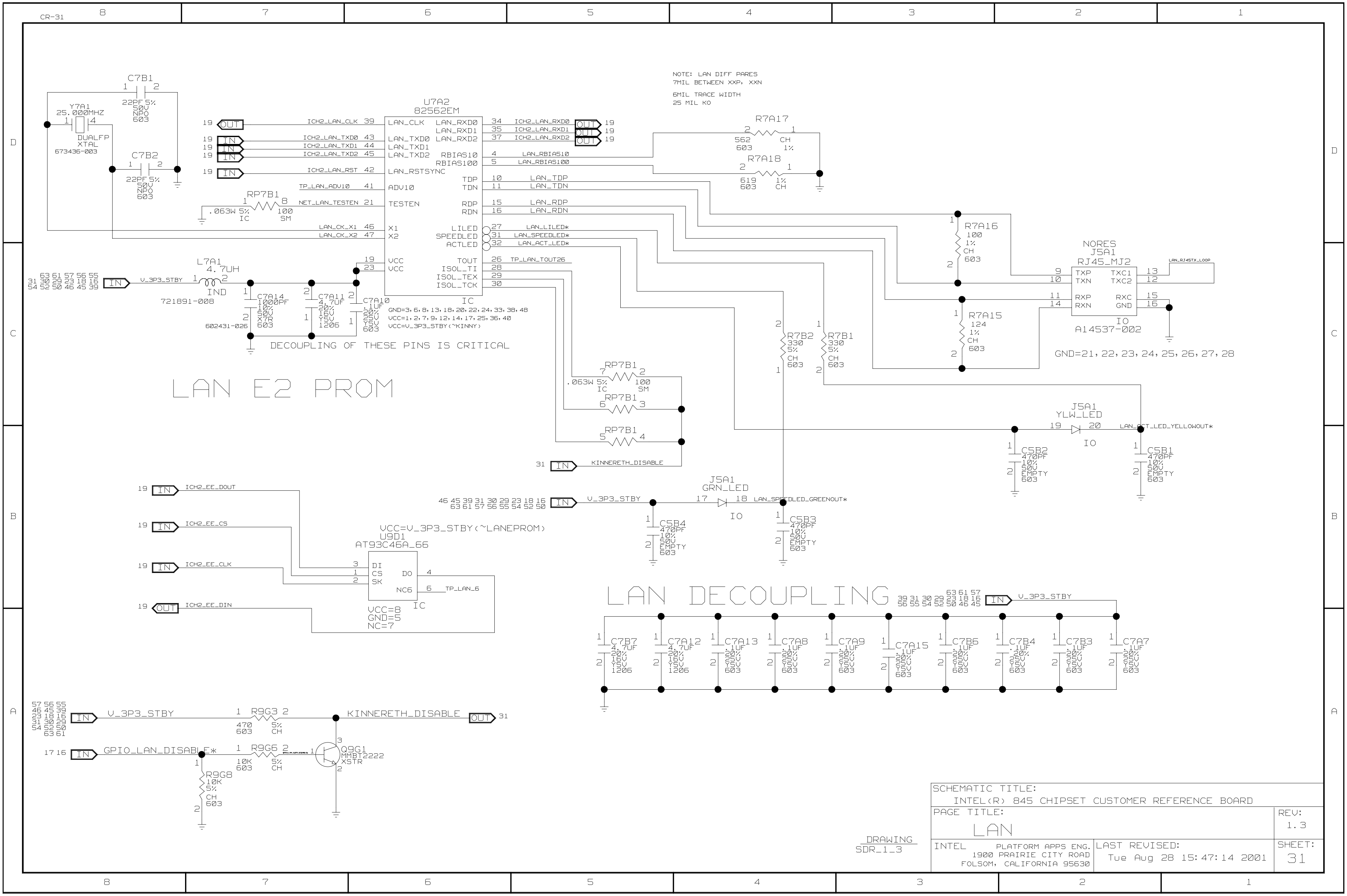
REV: 1.3

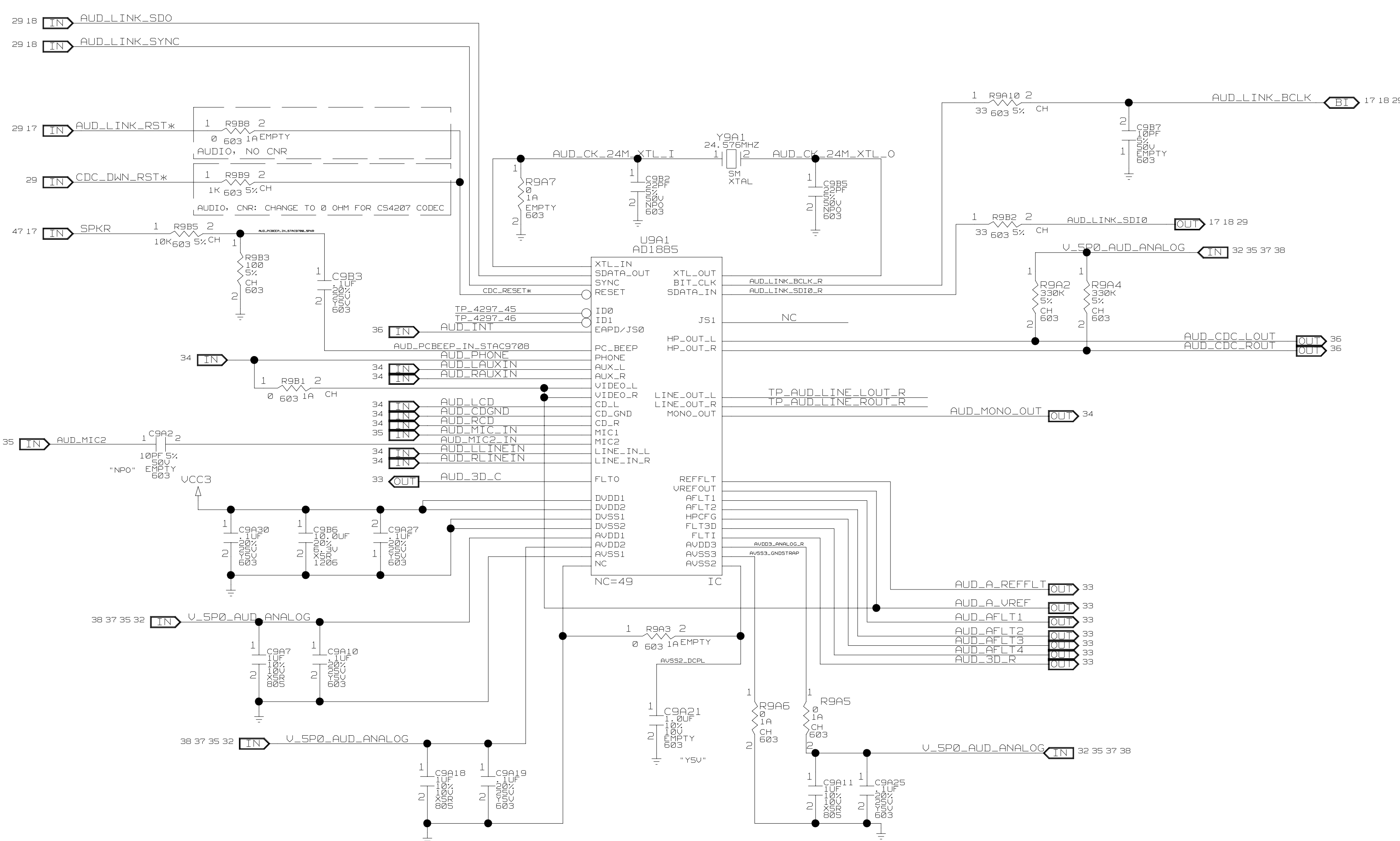
DRAWING SDR_1_3

INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:47:24 2001

SHEET: 30


LAN E2 PROM
LAN DECOUPLING
DECOUPLING OF THESE PINS IS CRITICAL
NOTE: LAN DIFF PARES
7MIL BETWEEN XXP, XXN
6MIL TRACE WIDTH
25 MIL KO
U7A2
82562EM
LAN_CLK
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_RSTSYNC
ADV10
TESTEN
X1
X2
VCC
LAN_RXD0
LAN_RXD1
LAN_RXD2
RBIAS10
RBIAS100
TDP
TDN
RDP
RDN
LILED
SPEEDLED
ACTLED
TOUT
ISOL_TI
ISOL_TEX
ISOL_TCK
GND=3,6,8,13,18,20,22,24,33,38,48
VCC=1,2,7,9,12,14,17,25,36,40
VCC=V_3P3_STBY(~KINNY)
ICH2_LAN_CLK
ICH2_LAN_TXD0
ICH2_LAN_TXD1
ICH2_LAN_TXD2
ICH2_LAN_RST
TP_LAN_ADV10
NET_LAN_TESTEN
LAN_CK_X1
LAN_CK_X2
ICH2_LAN_RXD0
ICH2_LAN_RXD1
ICH2_LAN_RXD2
LAN_RBIAS10
LAN_RBIAS100
LAN_TDP
LAN_TDN
LAN_RDP
LAN_RDN
LAN_LILED*
LAN_SPEEDLED*
LAN_ACT_LED*
TP_LAN_TOUT26
Y7A1
25.000MHZ
DUALFP
XTAL
673436-003
C7B1
22PF 5%
50V
NPO
603
C7B2
22PF 5%
50V
NPO
603
RP7B1
.063W 5%
IC
100
SM
L7A1
4.7UH
IND
721891-008
V_3P3_STBY
C7A14
1000PF
10%
50V
X7R
603
602431-026
C7A11
4.7UF
20%
16V
Y5V
1206
C7A10
.1UF
20%
25V
Y5V
603
R7A17
562
603
CH
1%
R7A18
619
603
1%
CH
R7A16
100
1%
CH
603
R7A15
124
1%
CH
603
NORES
J5A1
RJ45_MJ2
TXP
TXN
RXP
RXN
TXC1
TXC2
RXC
GND
IO
A14537-002
LAN_RJ45TX_LOOP
GND=21,22,23,24,25,26,27,28
R7B2
330
5%
CH
603
R7B1
330
5%
CH
603
KINNERETH_DISABLE
J5A1
YLW_LED
LAN_ACT_LED_YELLOWOUT*
J5A1
GRN_LED
LAN_SPEEDLED_GREENOUT*
C5B2
470PF
10%
50V
EMPTY
603
C5B1
470PF
10%
50V
EMPTY
603
C5B4
470PF
10%
50V
EMPTY
603
C5B3
470PF
10%
50V
EMPTY
603
ICH2_EE_DOUT
ICH2_EE_CS
ICH2_EE_CLK
ICH2_EE_DIN
VCC=V_3P3_STBY(~LANEPROM)
U9D1
AT93C46A_66
DI
CS
SK
DO
NC6
TP_LAN_6
VCC=8
GND=5
NC=7
C7B7
4.7UF
20%
16V
Y5V
1206
C7A12
4.7UF
20%
16V
Y5V
1206
C7A13
.1UF
C7A8
.1UF
C7A9
.1UF
C7A15
.1UF
C7B6
.1UF
C7B4
.1UF
C7B3
.1UF
C7A7
.1UF
GPIO_LAN_DISABLE*
R9G3
470
603
5%
CH
R9G6
10K
603
5%
CH
R9G8
10K
5%
CH
603
Q9G1
MMBT2222
XSTR
IN
OUT
CR-31
SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
LAN
REV:
1.3
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Aug 28 15:47:14 2001
SHEET:
31
DRAWING
SDR_1_3



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: AD1885

REV: 1.3

DRAWING SDR_1_3

INTEL PLATFORM APPS ENG.
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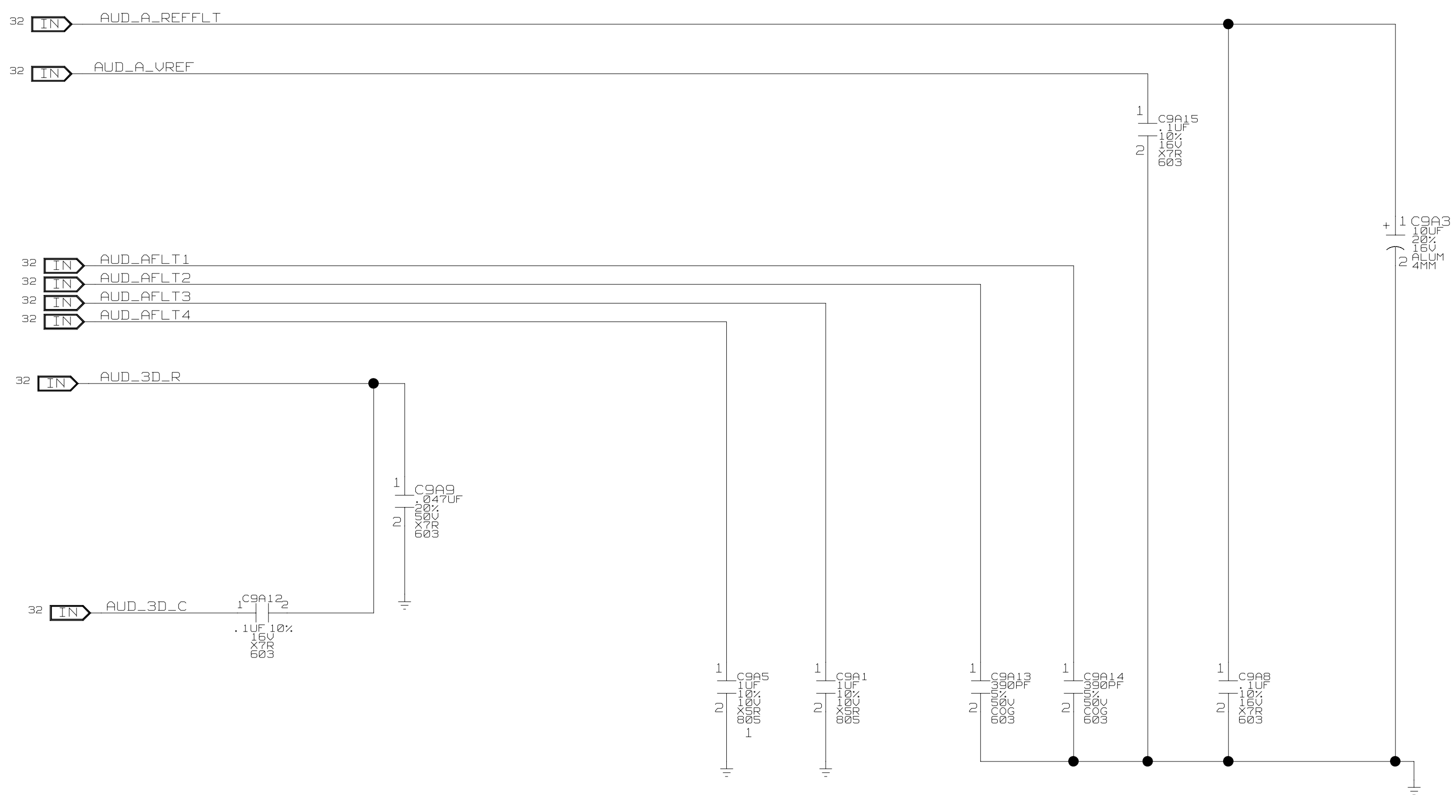
SHEET: 32

CR-32

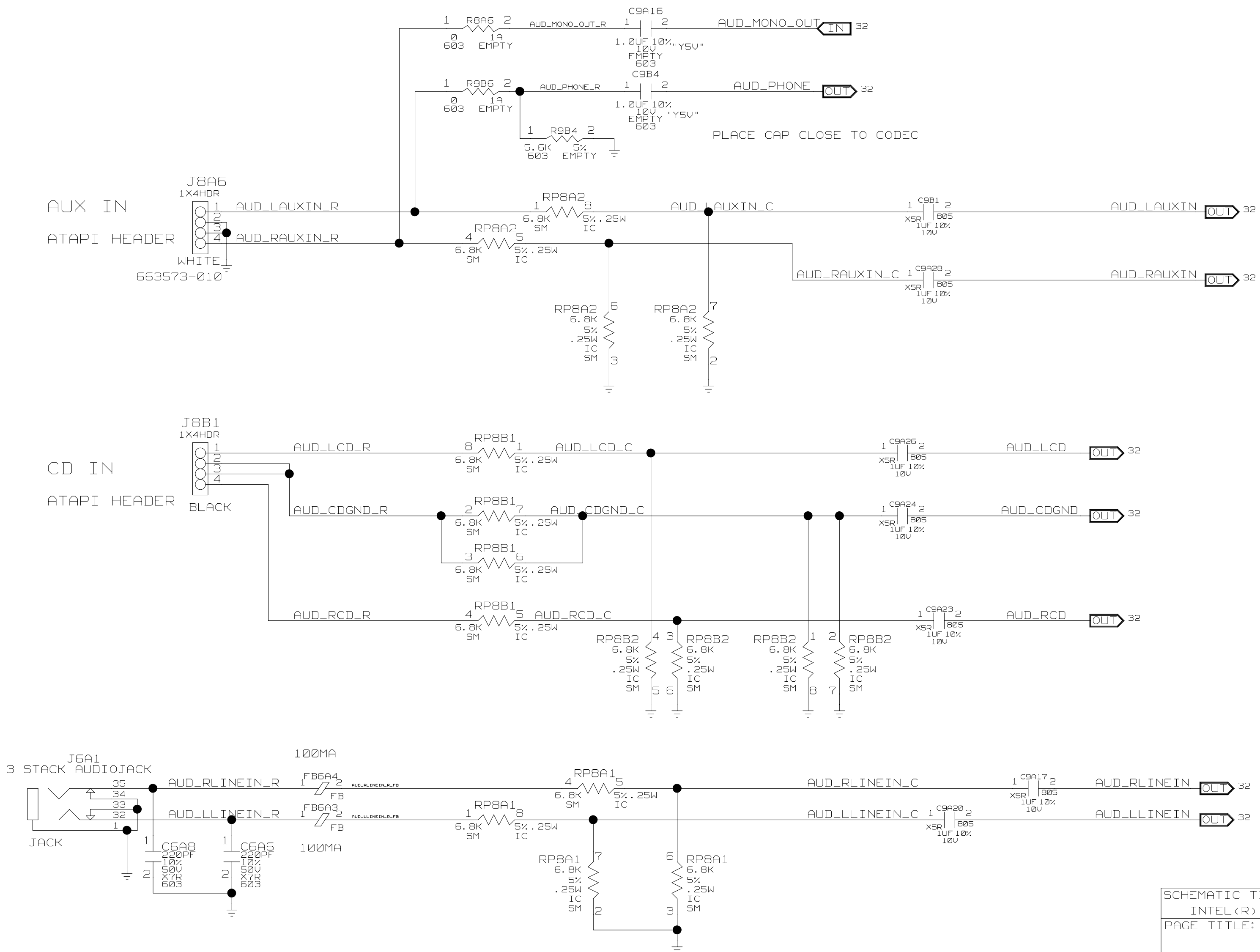
KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO SUBMODULE 2		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:46:56 2001	SHEET: 33

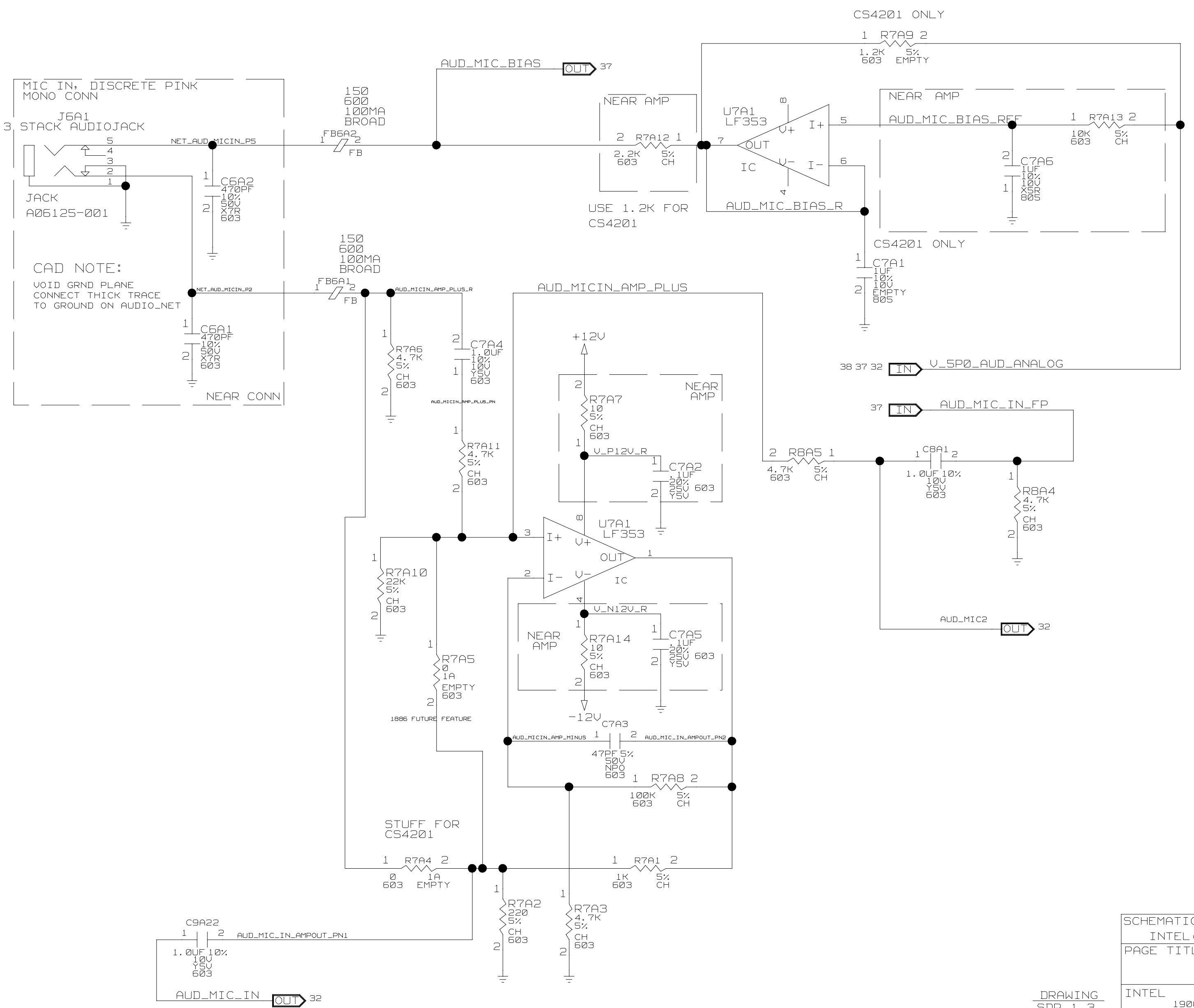
CR-33



SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO SUBMODULE 5		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:46:48 2001	SHEET: 34

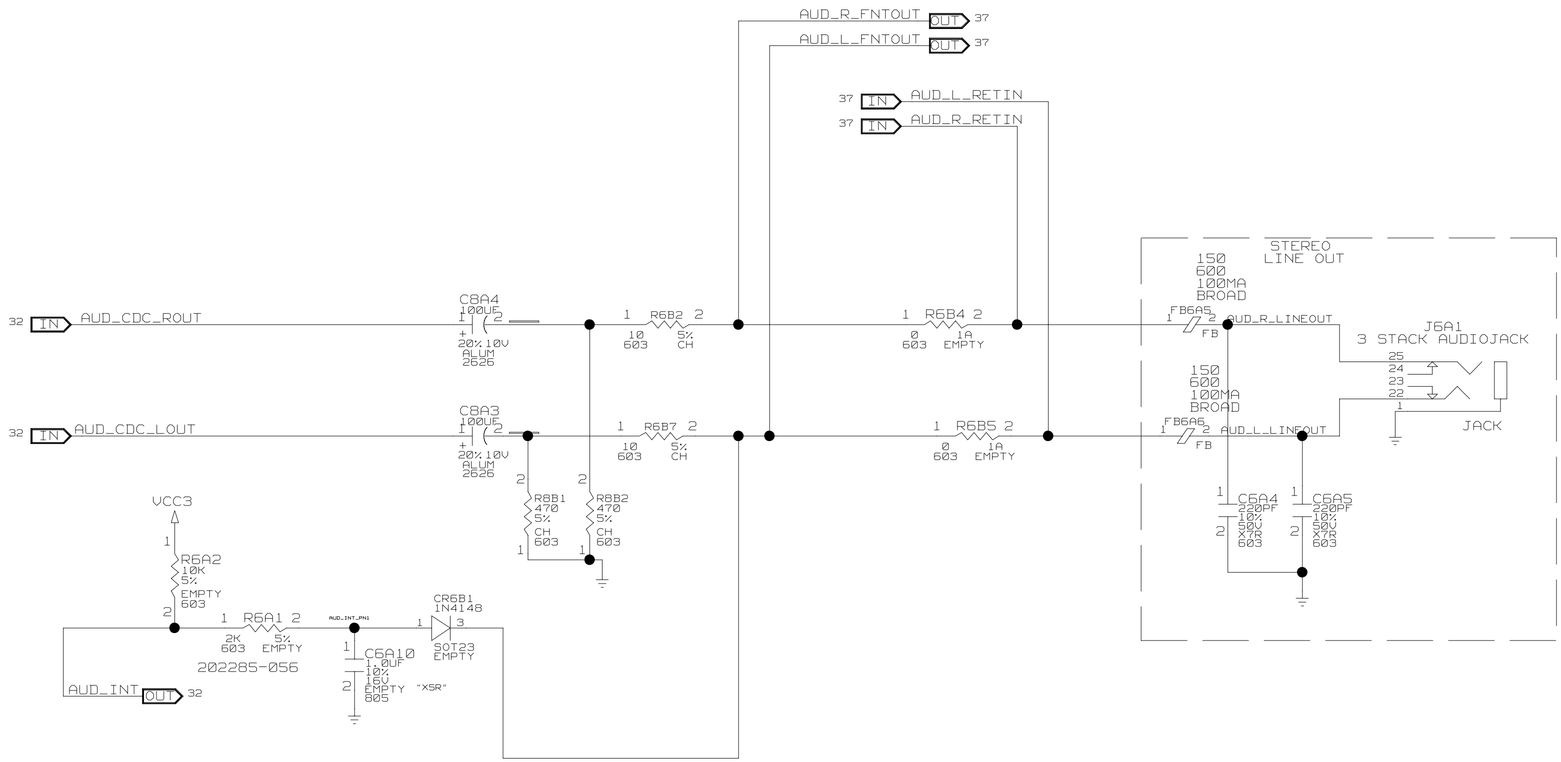
DRAWING
SDR_1_3

CR-34



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO SUBMODULE 4		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:46:38 2001	SHEET: 35



CR-36

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: AUDIO SUBMODULE 3

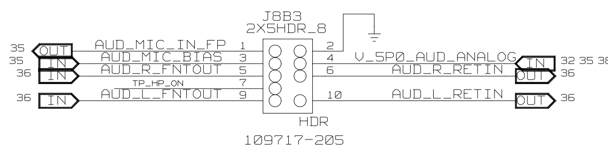
REV: 1.3

DRAWING SDR_1_3

INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

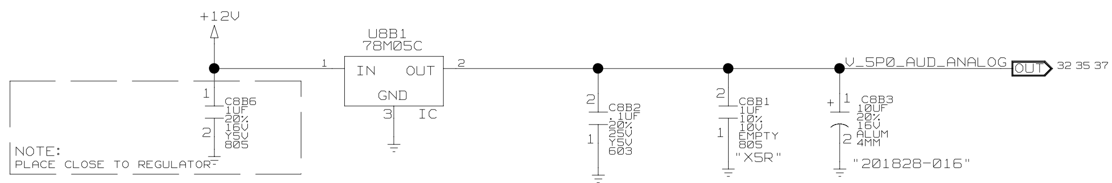
LAST REVISED: Tue Aug 28 15:46:30 2001

SHEET: 36



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AUDIO FRONT PANEL	REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630 — LAST REVISED: Tue Aug 28 15:46:20 2001	SHEET: 37



DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
AUDIO_VREG

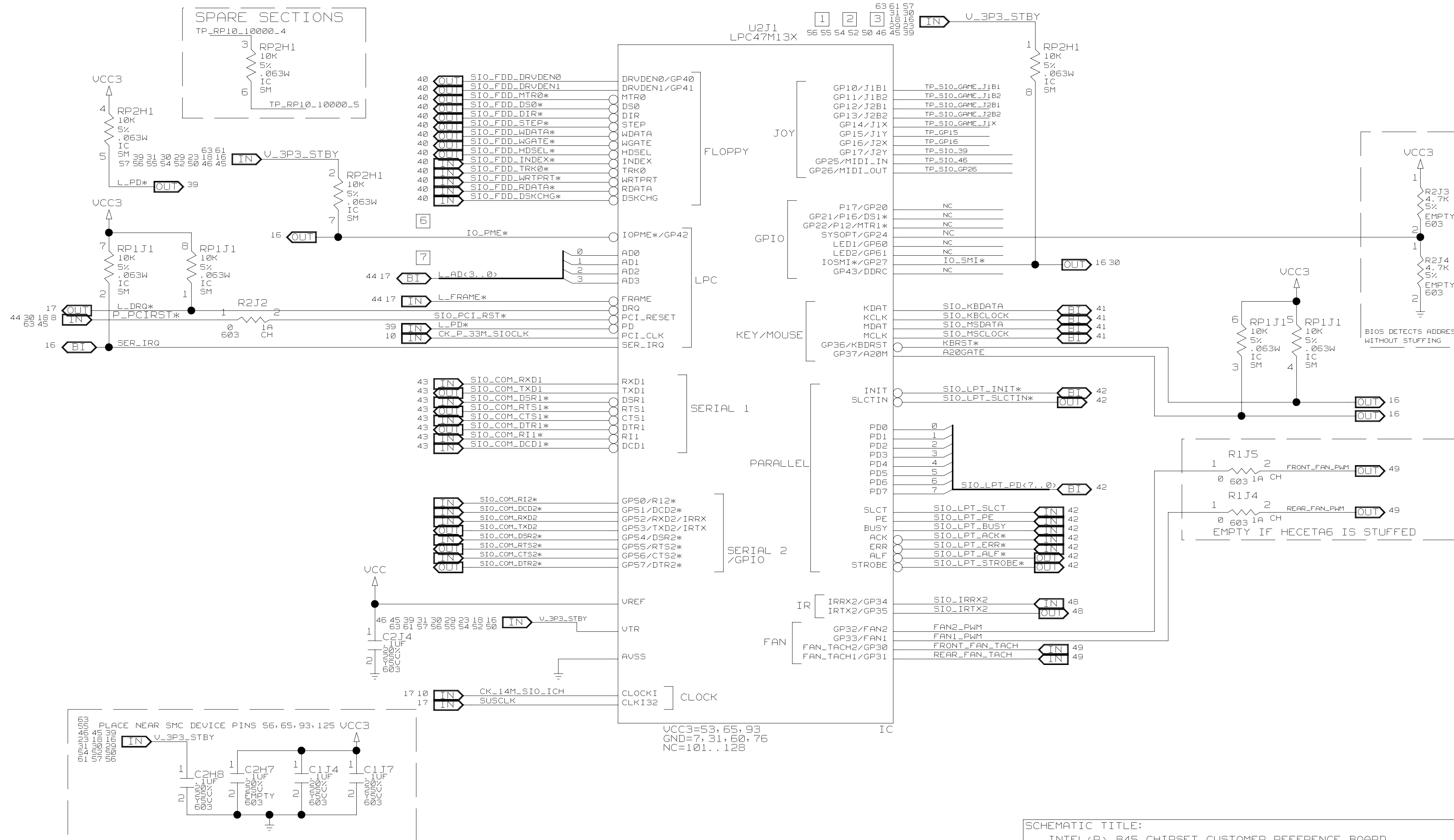
REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:46:12 2001

SHEET: 38

CR-38



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: SUPER I/O

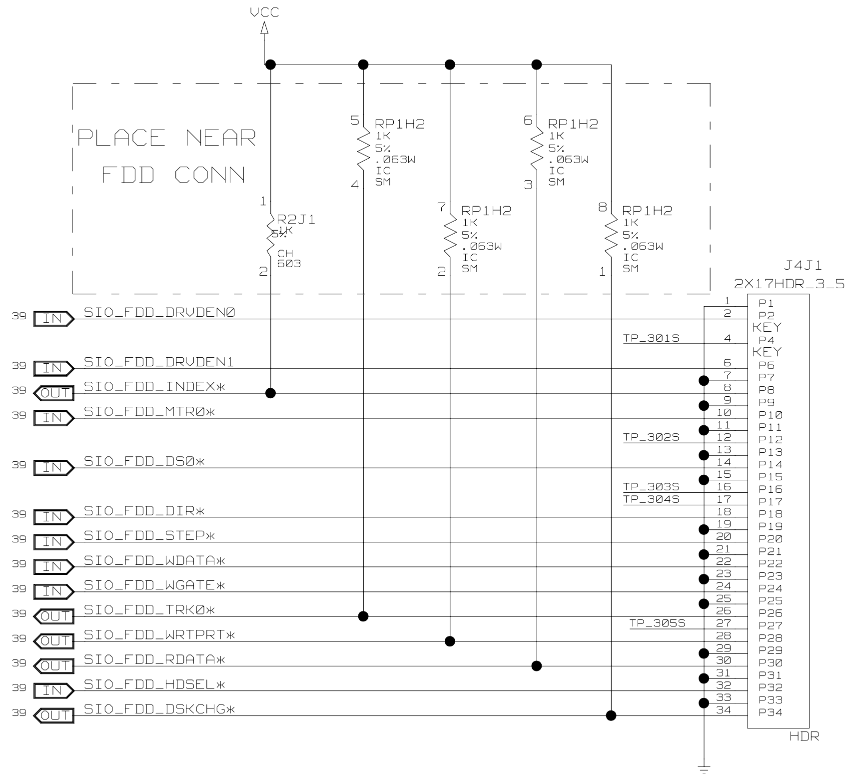
REV: 1.3

DRAWING
SDR_1_3

INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:46:03 2001

SHEET: 39



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: FLOPPY

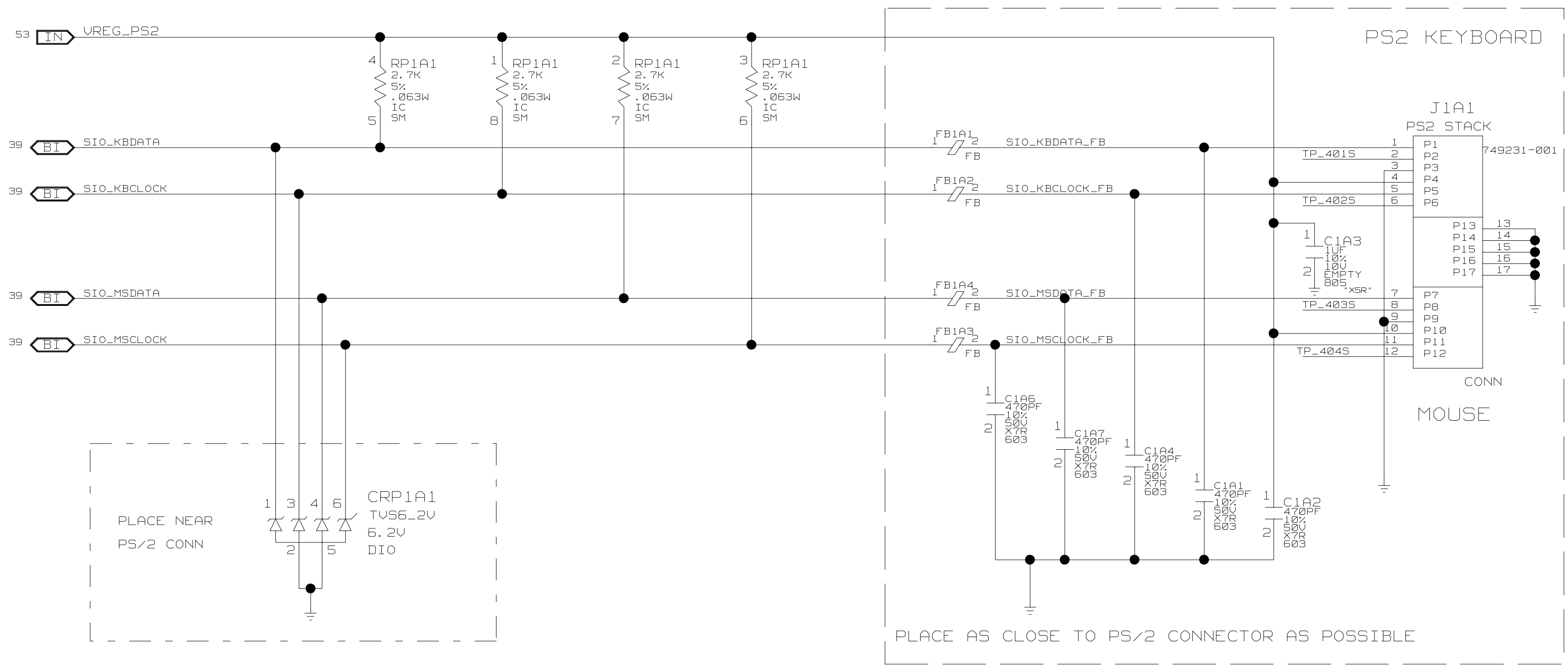
REV: 1.3

INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:45:54 2001

SHEET: 40

CR-40



CR-41

DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

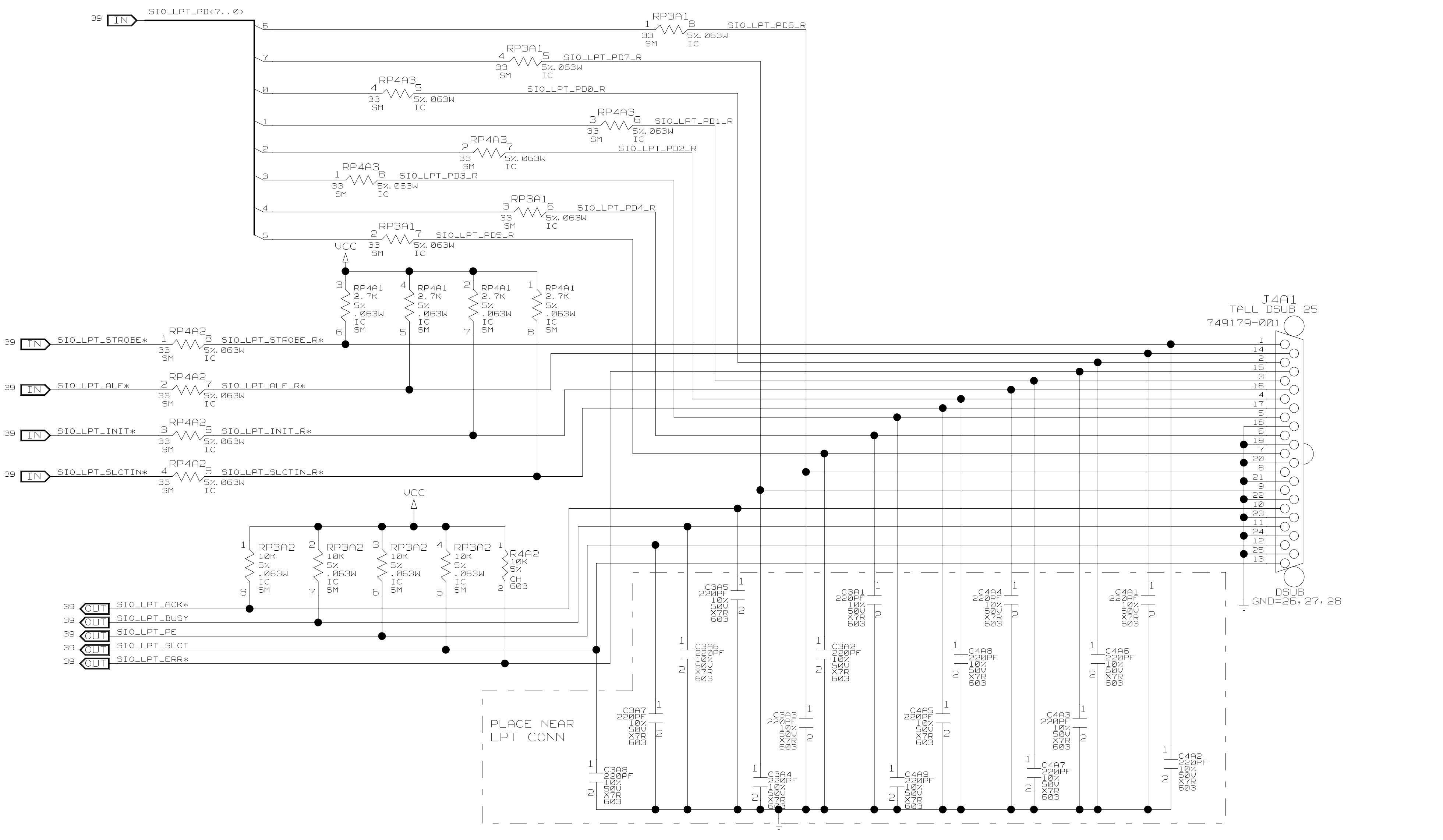
PAGE TITLE:
KEYBOARD AND MOUSE

REV:
1.3

INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

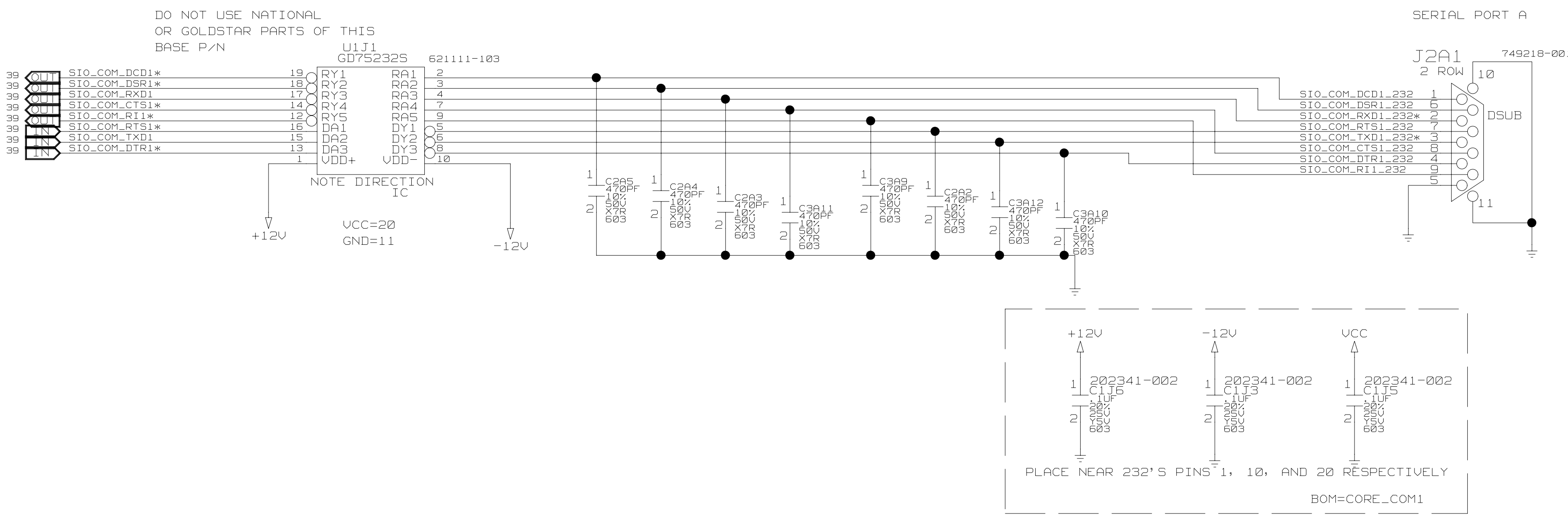
LAST REVISED:
Tue Aug 28 15:45:44 2001

SHEET:
41



SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PARRELL PORT		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:45:35 2001	SHEET: 42

DRAWING
SDR_1_3



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: SERIAL PORT

REV: 1.3

DRAWING
SDR_1_3

INTEL
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FOLSOM, CALIFORNIA 95630

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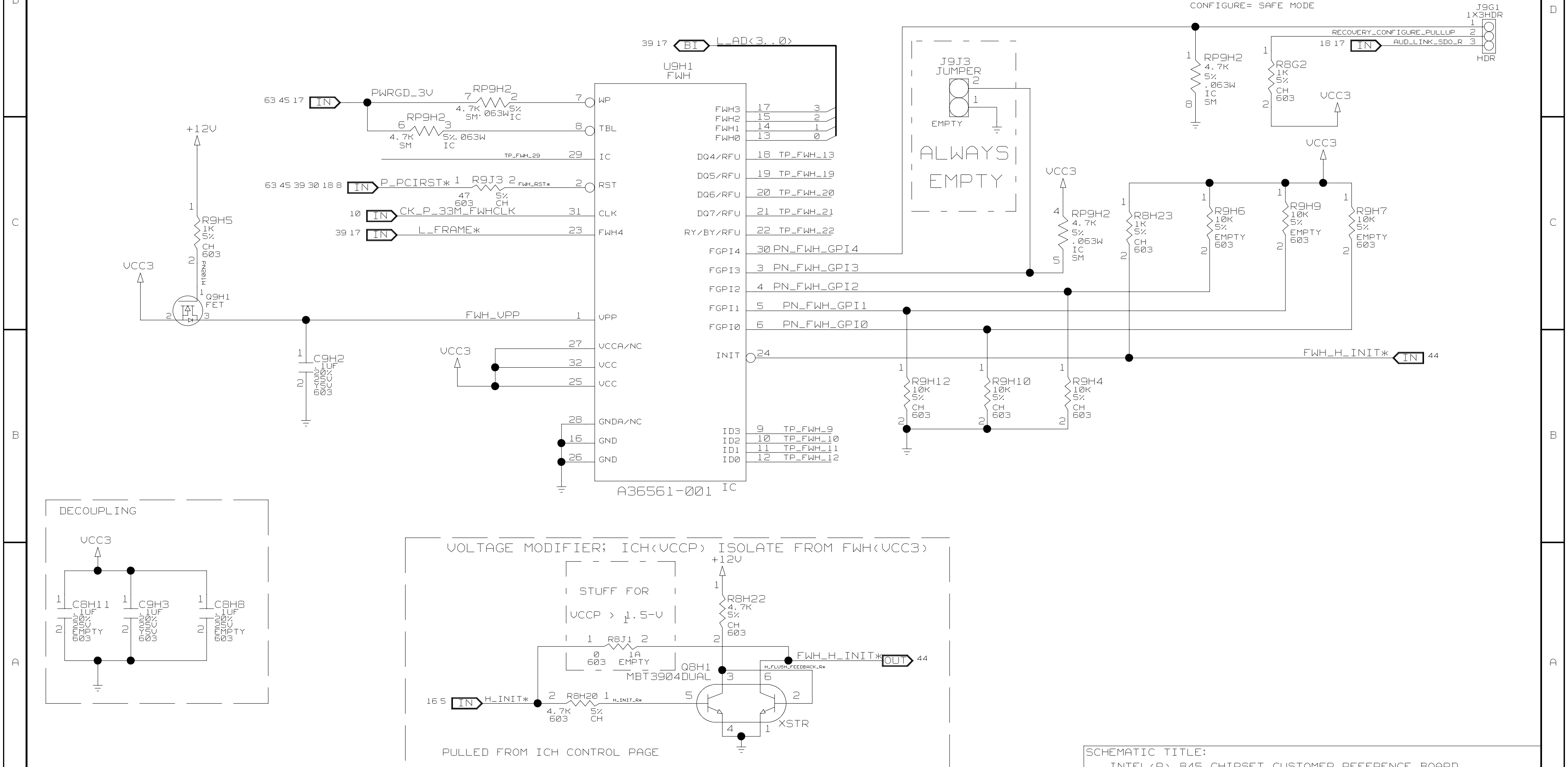
SHEET: 43

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
FIRMWARE HUB

REV: 1.3

INTEL PLATFORM APPS ENG.
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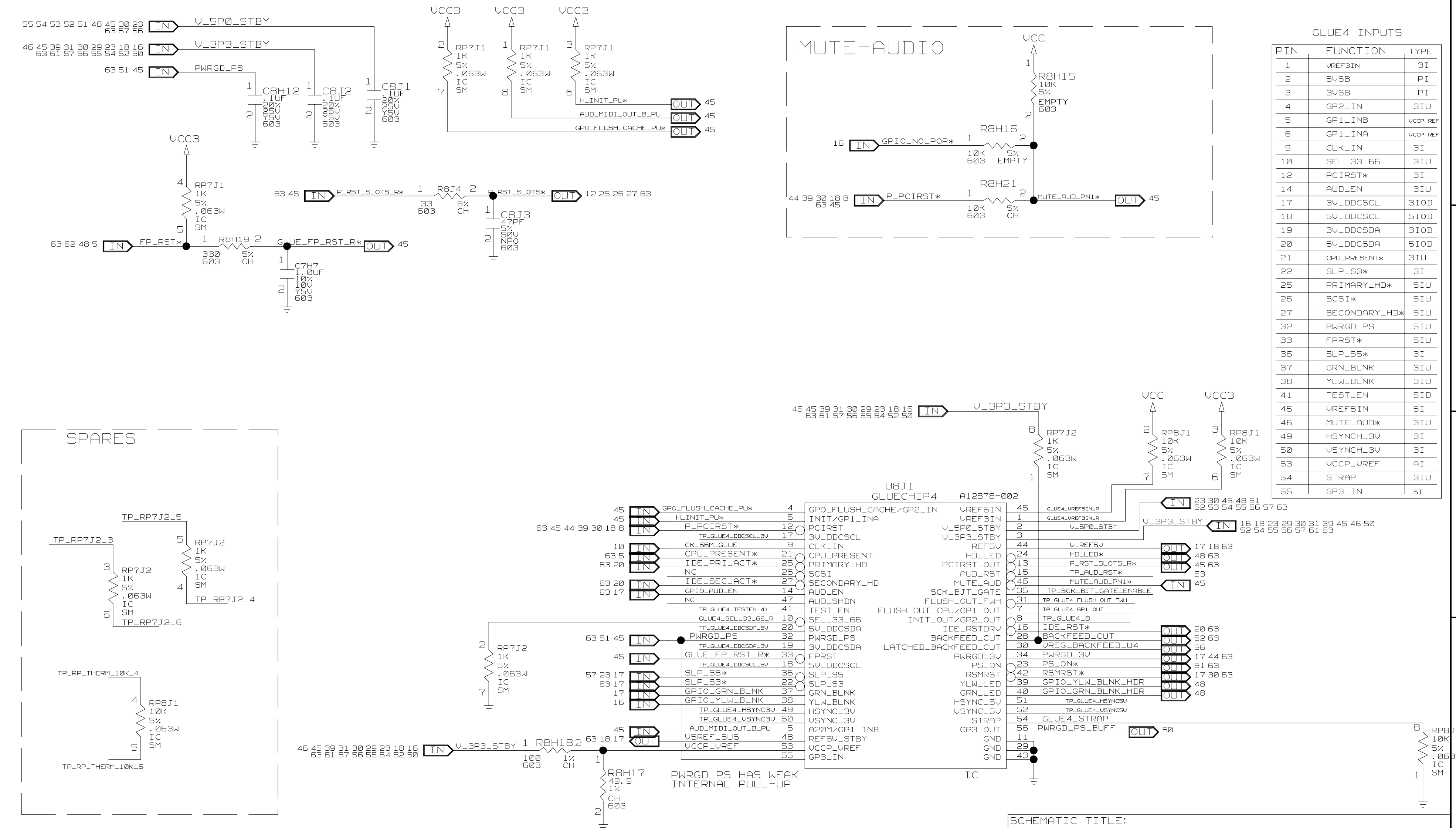
LAST REVISED: Tue Aug 28 15:45:17 2001

SHEET: 44

DRAWING SDR_1_3

CR-44

CR-45



GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I

DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: GLUECHIP4

REV: 1.3

INTEL
PLATFORM APPS ENG.
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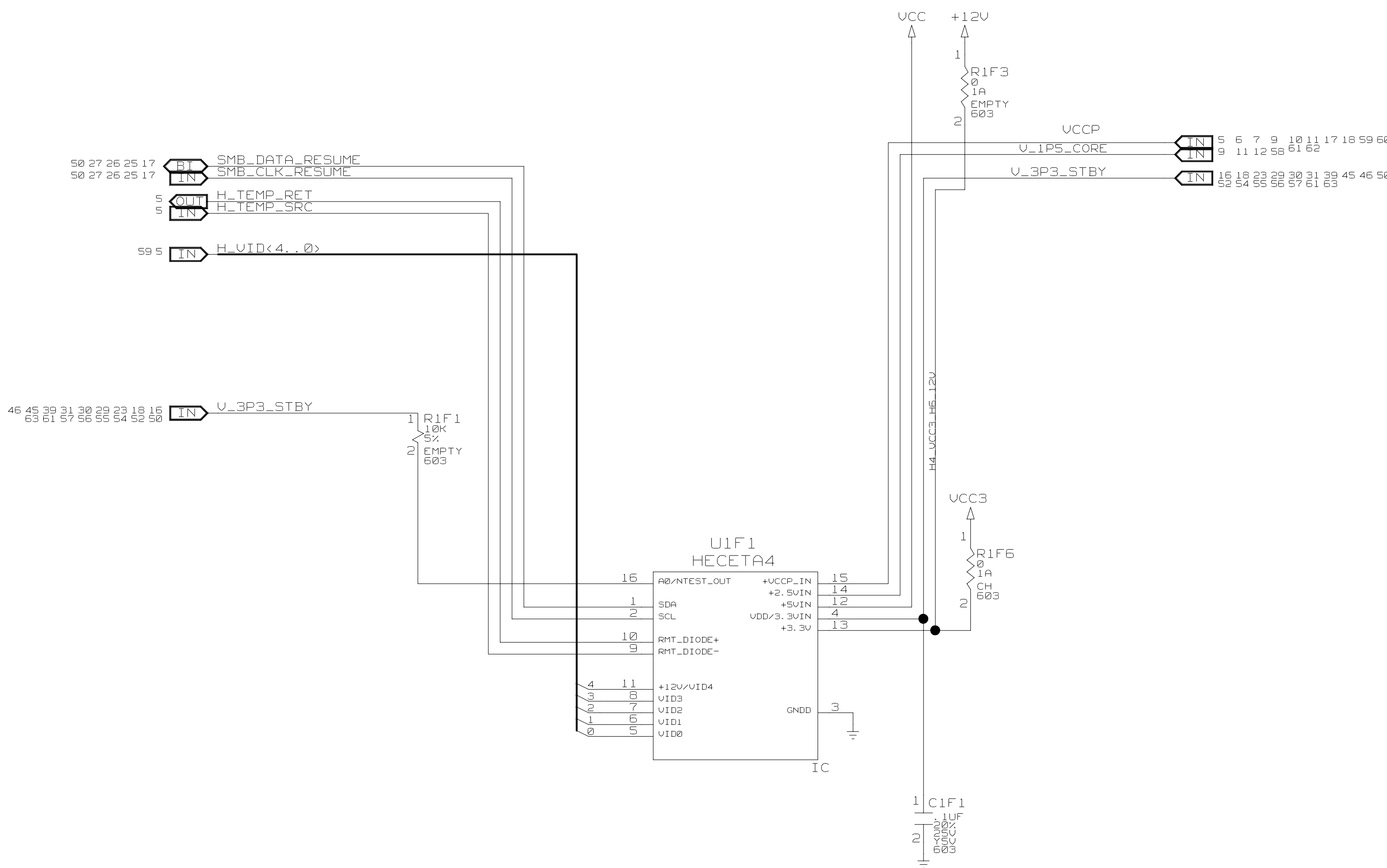
FOLSOM, CALIFORNIA 95630

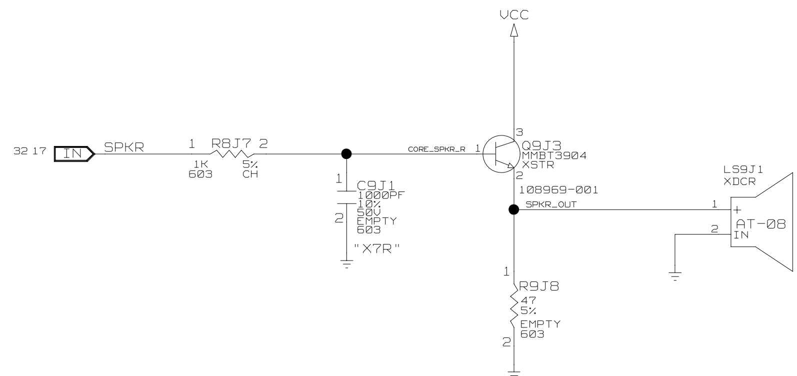
LAST REVISED:
Tue Aug 28 15:45:08 2001

SHEET: 45



DRAWING
SDR_1_2

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: HECETA4	REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630 — LAST REVISED: Tue Aug 28 15:44:58 2001	SHEET: 46



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: SPEAKER

REV: 1.3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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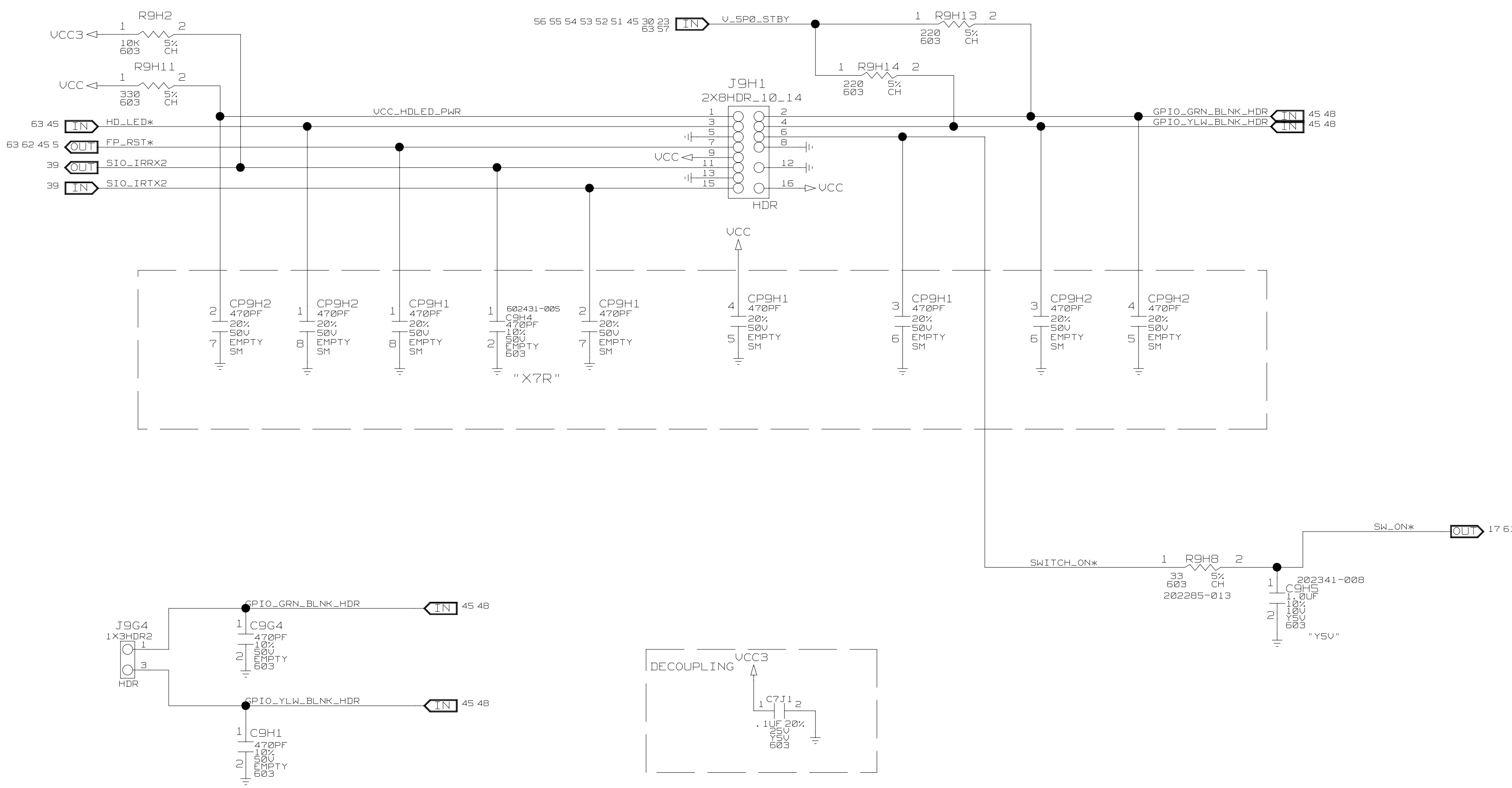
LAST REVISED: Tue Aug 28 15:44:49 2001

SHEET: 47



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: FRONT PANEL HEADER

REV: 1.3

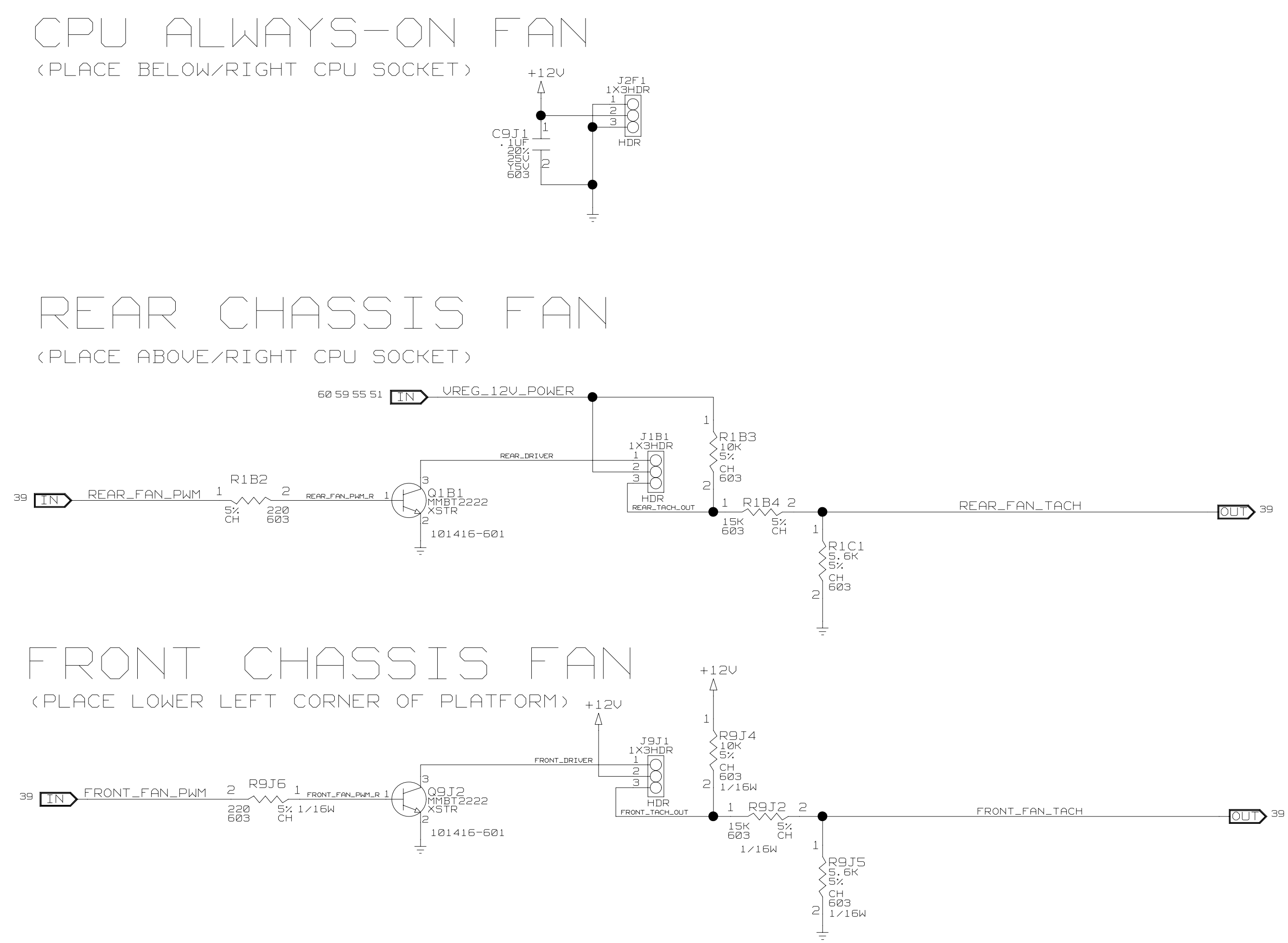
DRAWING
SDR_1_3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:44:40 2001

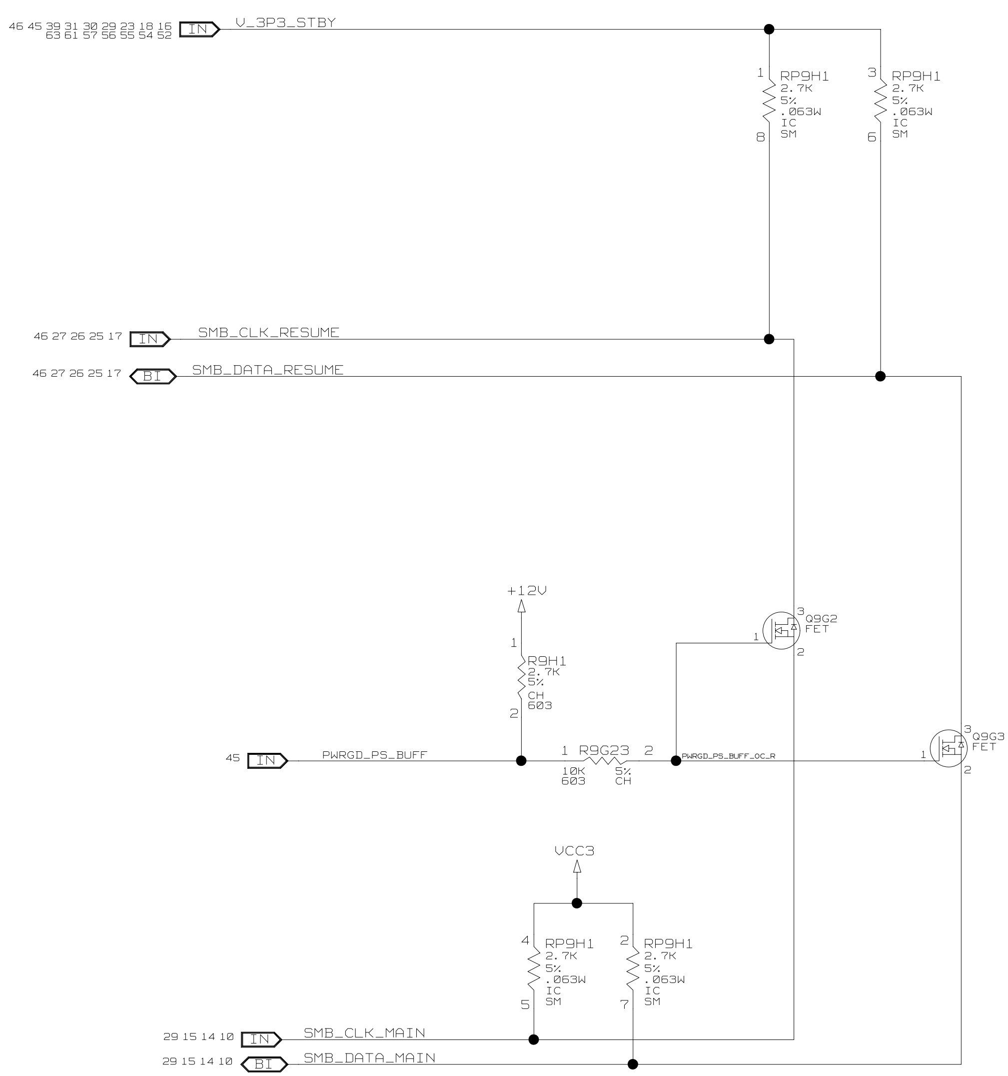
SHEET: 48

CR-48



SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: FAN CONTROL		REV: 1.3
DRAWING SDR_1_3 — INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:44:29 2001	SHEET: 49

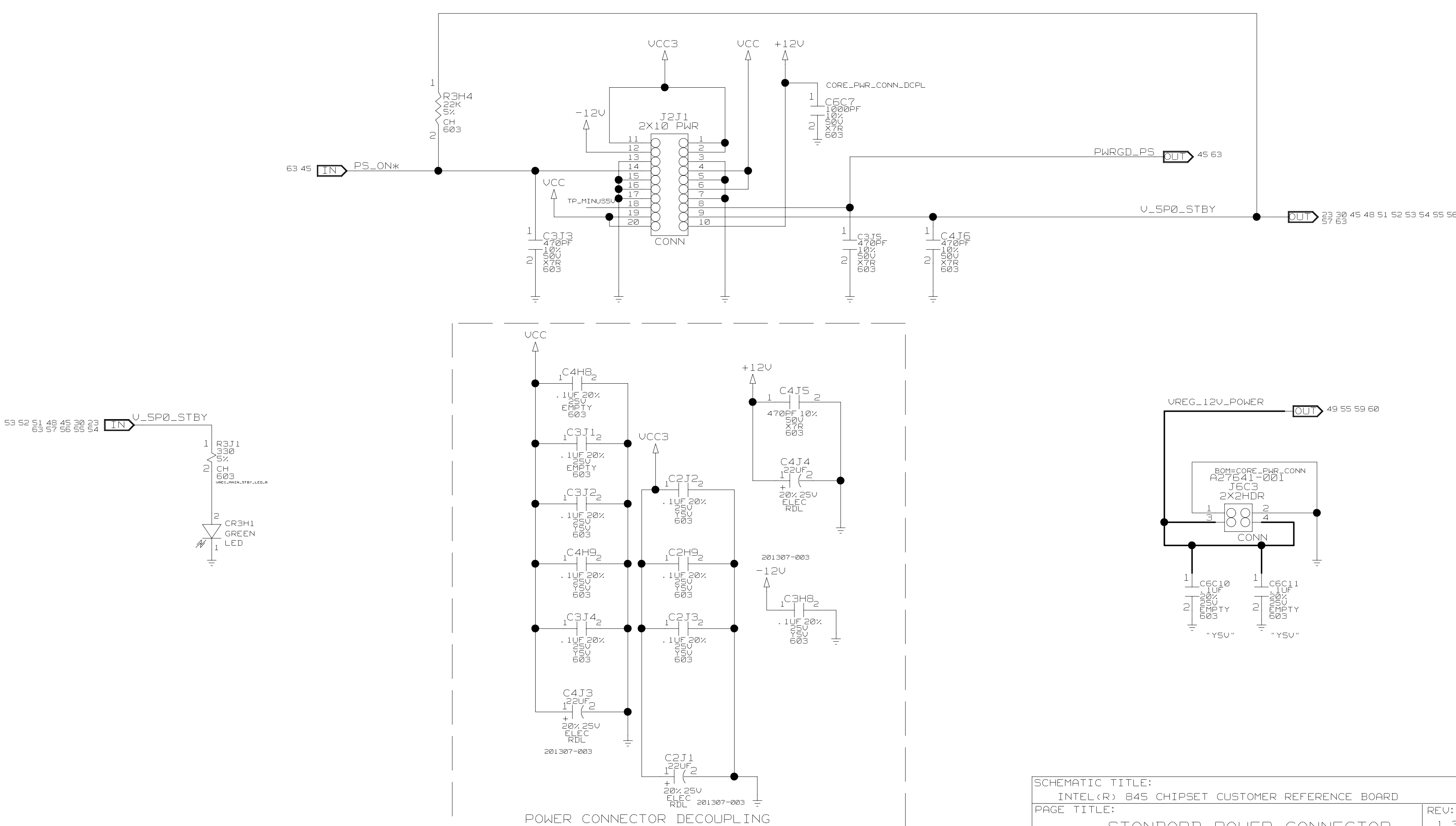
CR-49



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: SMBUS ISOLATION		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:44:20 2001	SHEET: 50

CR-50



DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
STANDARD POWER CONNECTOR

REV: 1.3

INTEL
PLATFORM APPS ENG.
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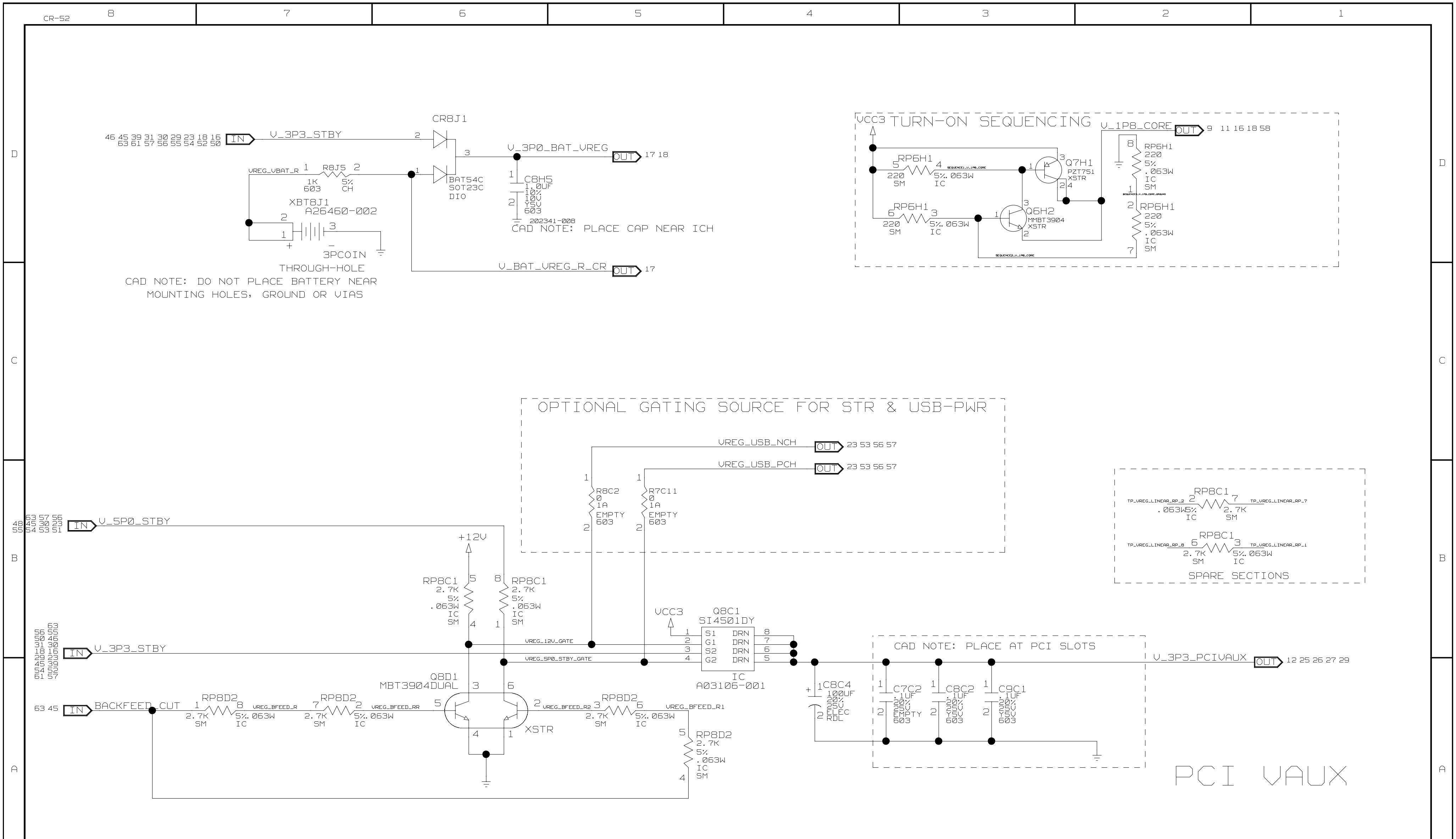
FOLSOM, CALIFORNIA 95630

LAST REVISED:
Tue Aug 28 15:44:10 2001

SHEET: 51



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: PCI VAUX

REV: 1.3

DRAWING SDR_1_3

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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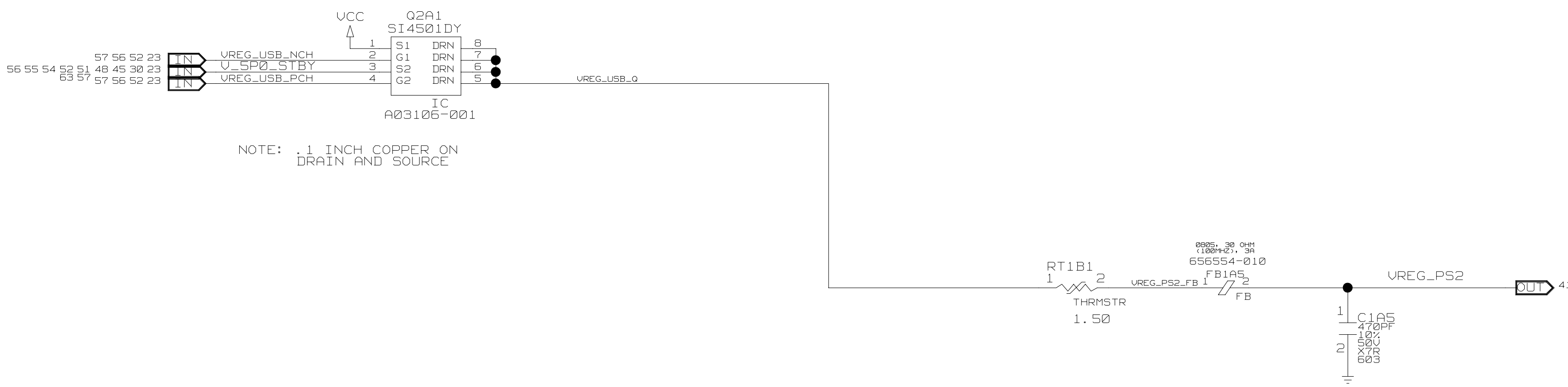
LAST REVISED: Tue Aug 28 15:44:00 2001

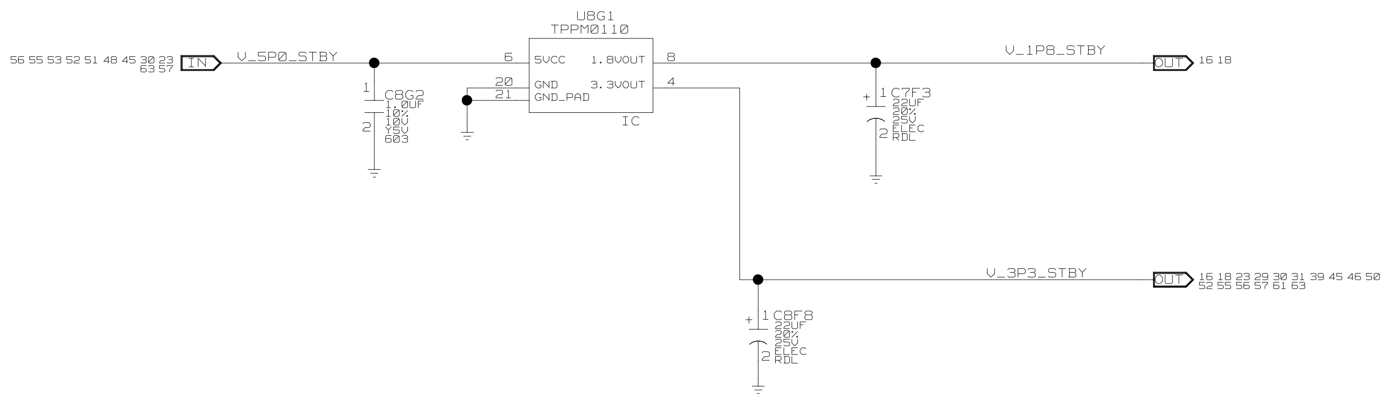
SHEET: 52



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: WAKE ON PS2		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:43:49 2001	SHEET: 53

CR-53



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
3.3V/1.8V STANDBY

REV: 1.3

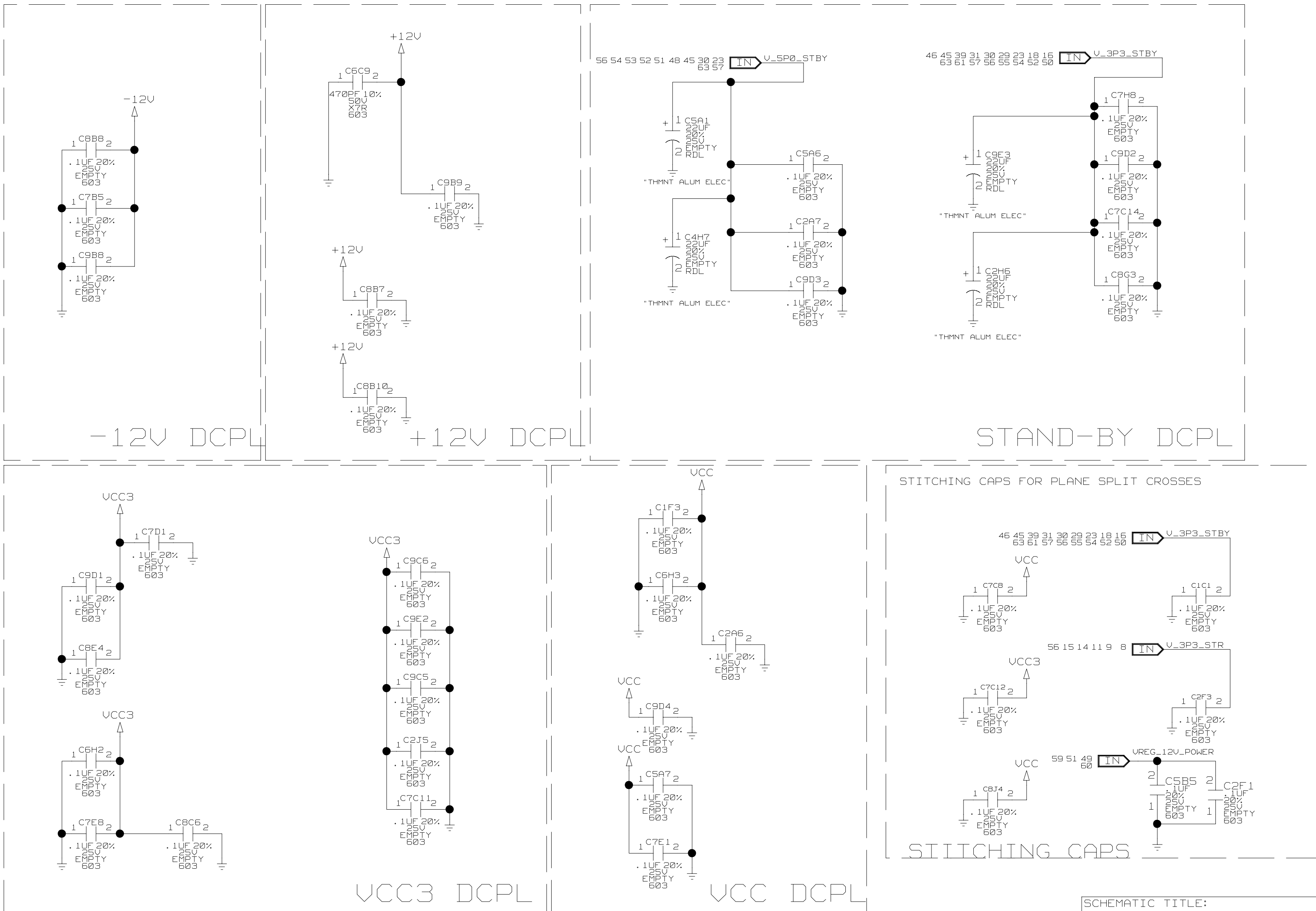
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:43:40 2001

SHEET: 54

DRAWING SDR_1_3

CR-54



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: VREG

REV: 1.3

INTEL PLATFORM APPS ENG.
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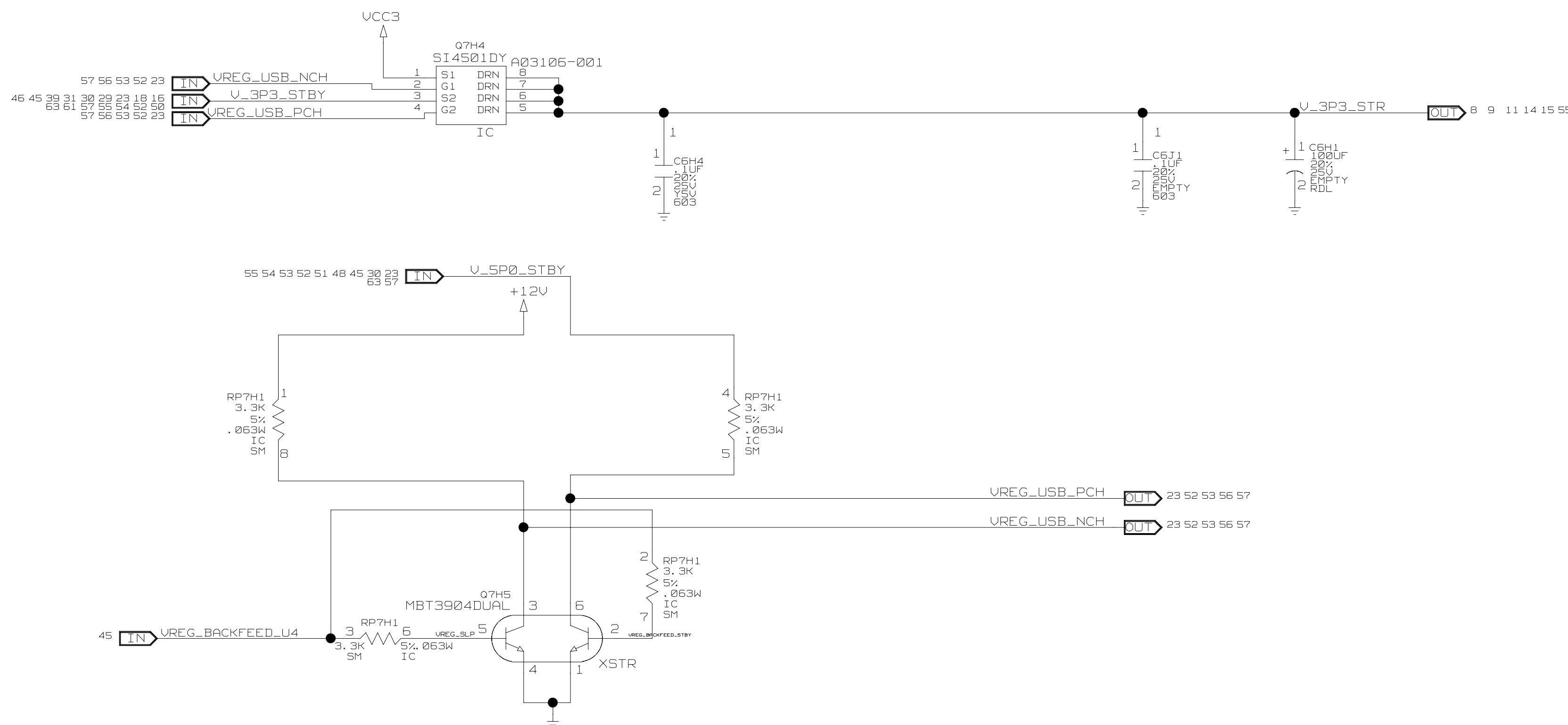
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:43:32 2001

SHEET: 55

DRAWING SDR_1_3

CR-55



DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
LINEAR REGULATION

REV: 1.3

INTEL PLATFORM APPS ENG.
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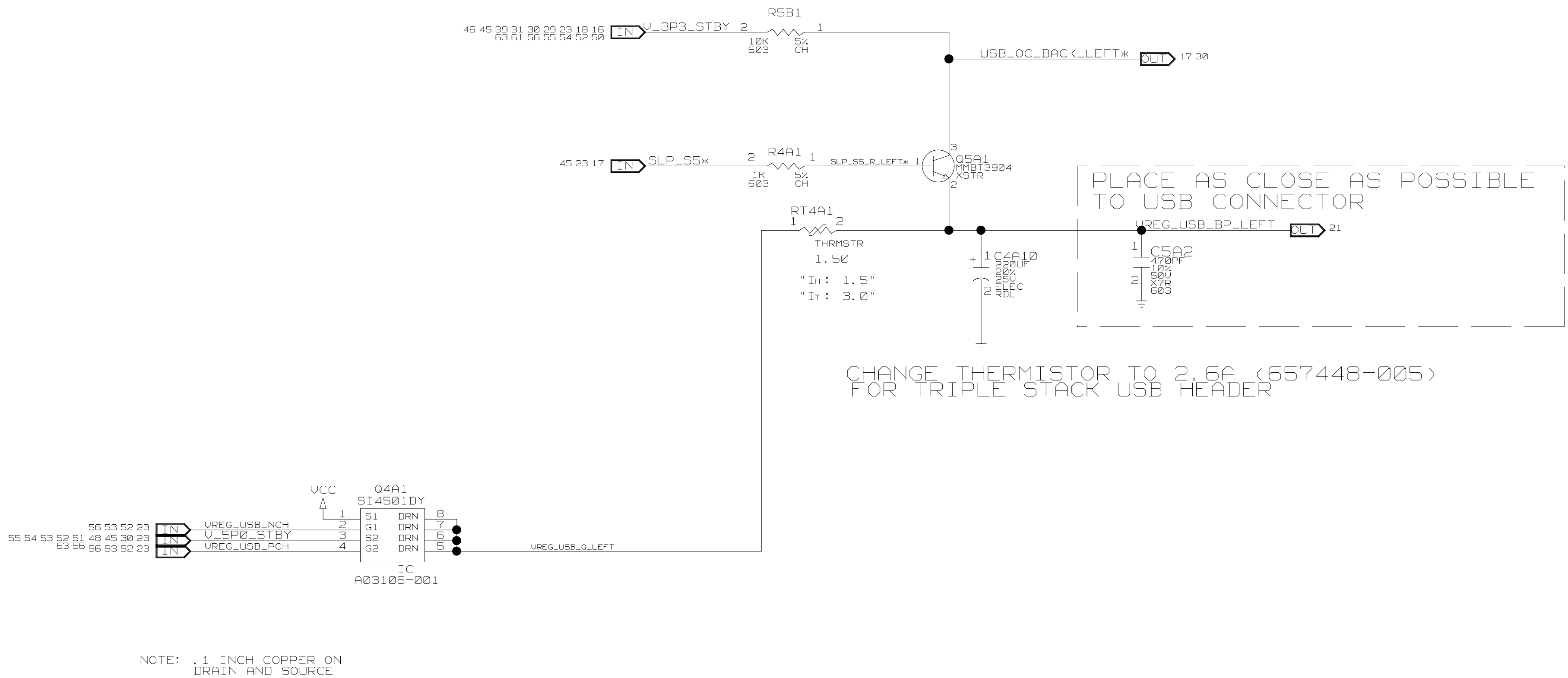
LAST REVISED:
Tue Aug 28 15:43:22 2001

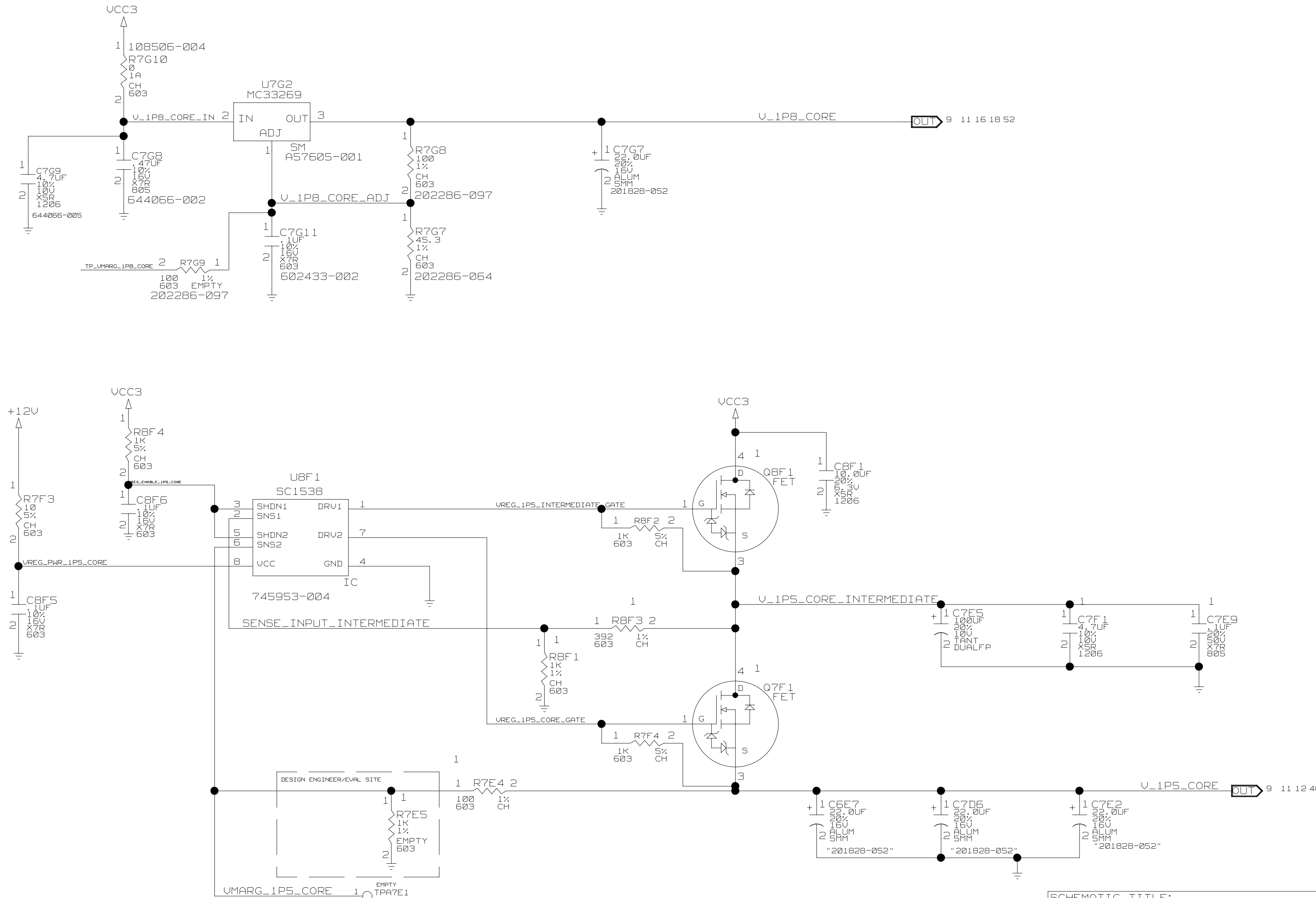
SHEET: 56



SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB REGULATION		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:43:13 2001	SHEET: 57

DRAWING SDR_1_3

CR-57



CR-58

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
1.5_&1.8 LINEAR REGULATION

REV: 1.3

DRAWING
SDR_1_3

INTEL
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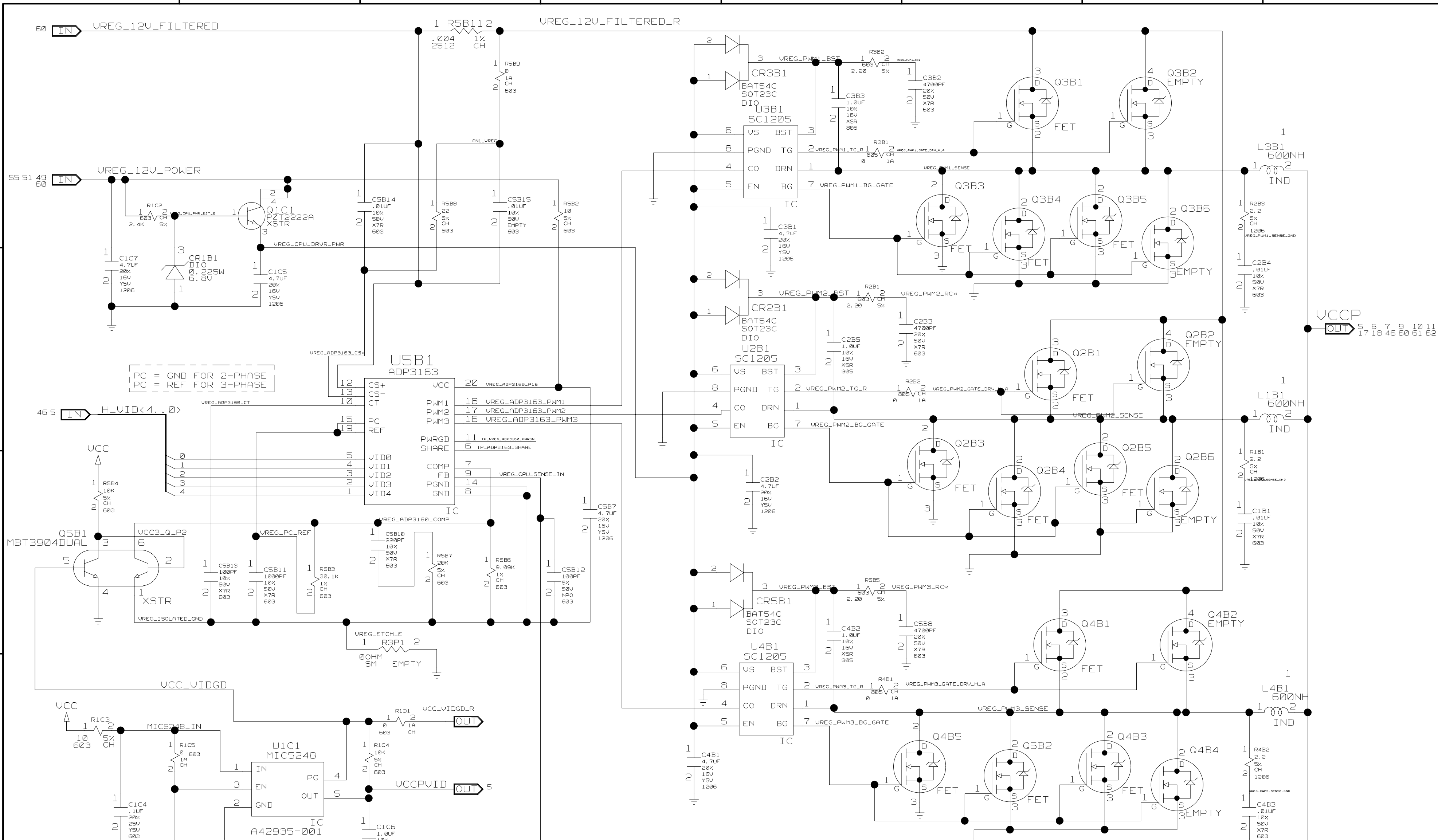
LAST REVISED:
Tue Aug 28 15:43:04 2001

SHEET: 58



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
CPU VREG

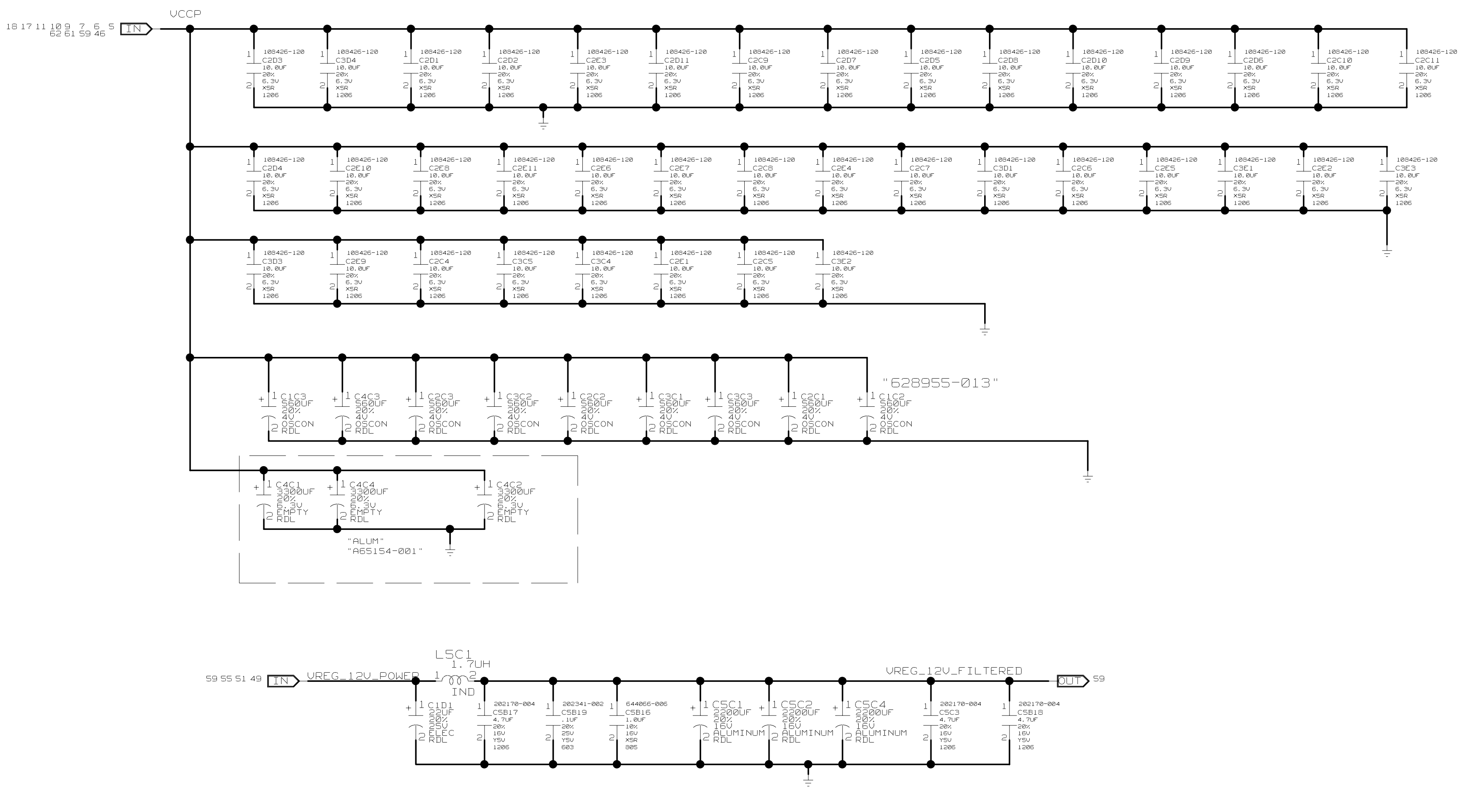
REV: 1.3

INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Aug 28 15:42:54 2001

SHEET: 59

DRAWING SDR_1_3



DRAWING
SDR_1_3

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: CAPACITORS

REV: 1.3

INTEL
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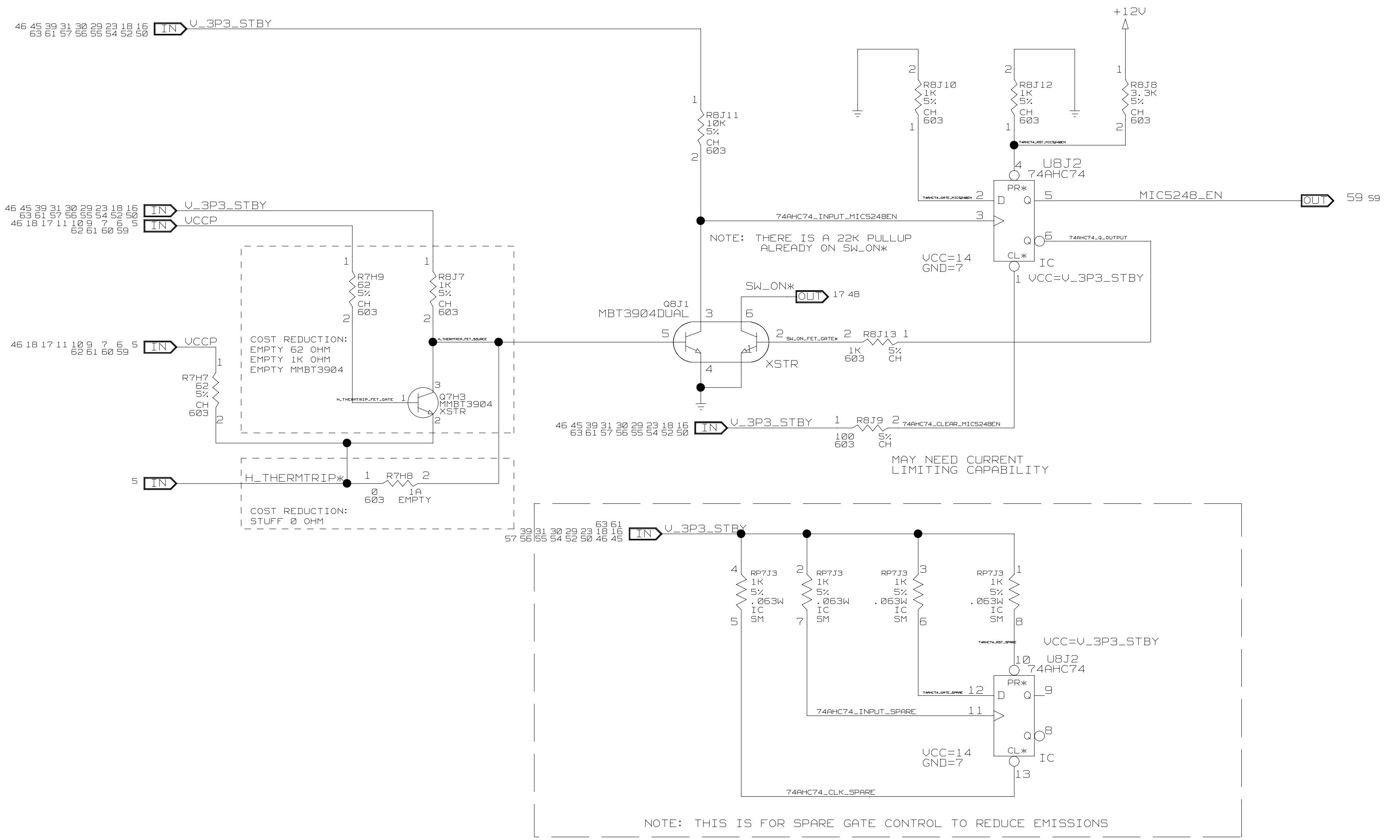
LAST REVISED:
Tue Aug 28 15:42:43 2001

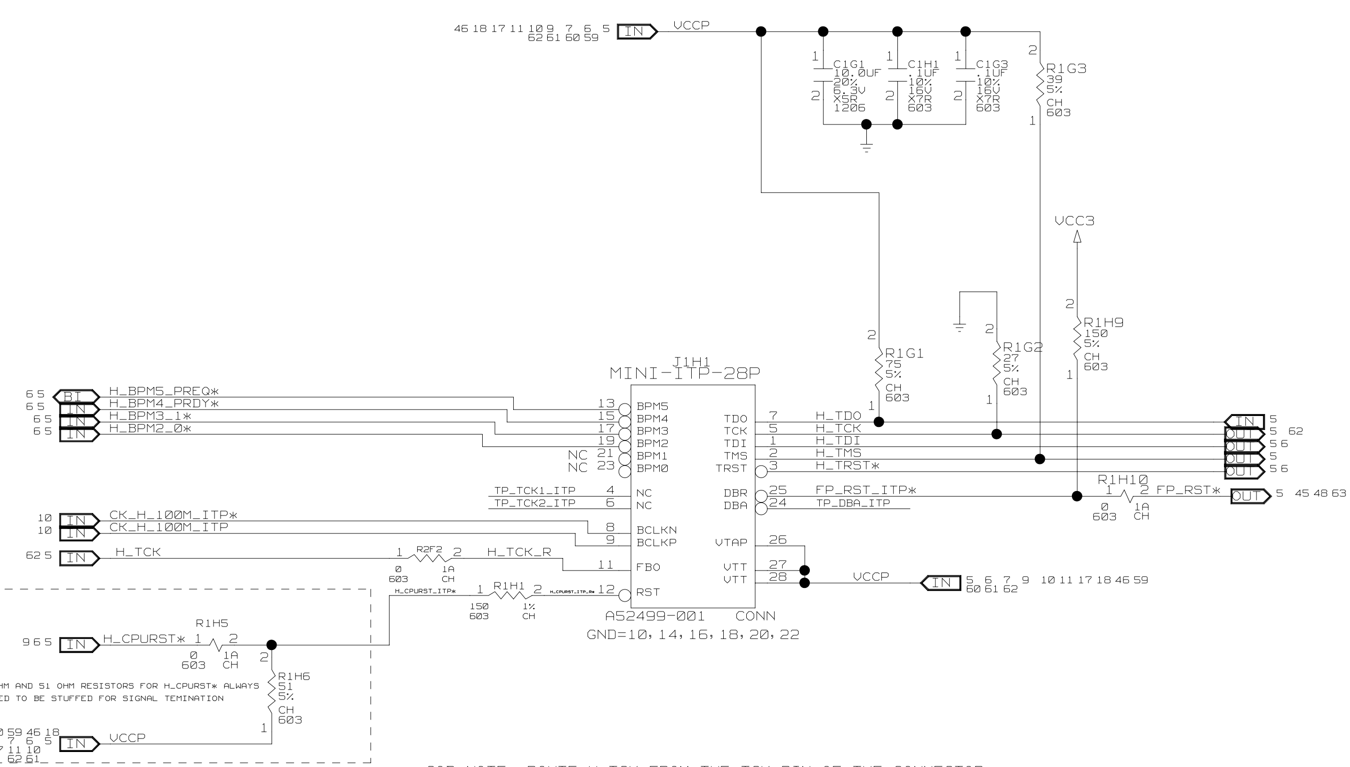
SHEET: 60



DRAWING
SDR_1_3

SCHEMATIC TITLE: INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: THERM-TRIP & POWER GOOD ENABLE CIRCUIT		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Aug 28 15:42:34 2001	SHEET: 61

ITP/DPFLEX CONNECTOR



CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR
TO THE PROCESSOR PIN. FBO TAPS INTO THE TCK PIN OF THE CONNECTOR WITH LENGTH REQUIREMENTS.

SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
ITP/DPFLEX CONNECTOR

REV: 1.3

DRAWING SDR_1_3

INTEL PLATFORM APPS ENG.
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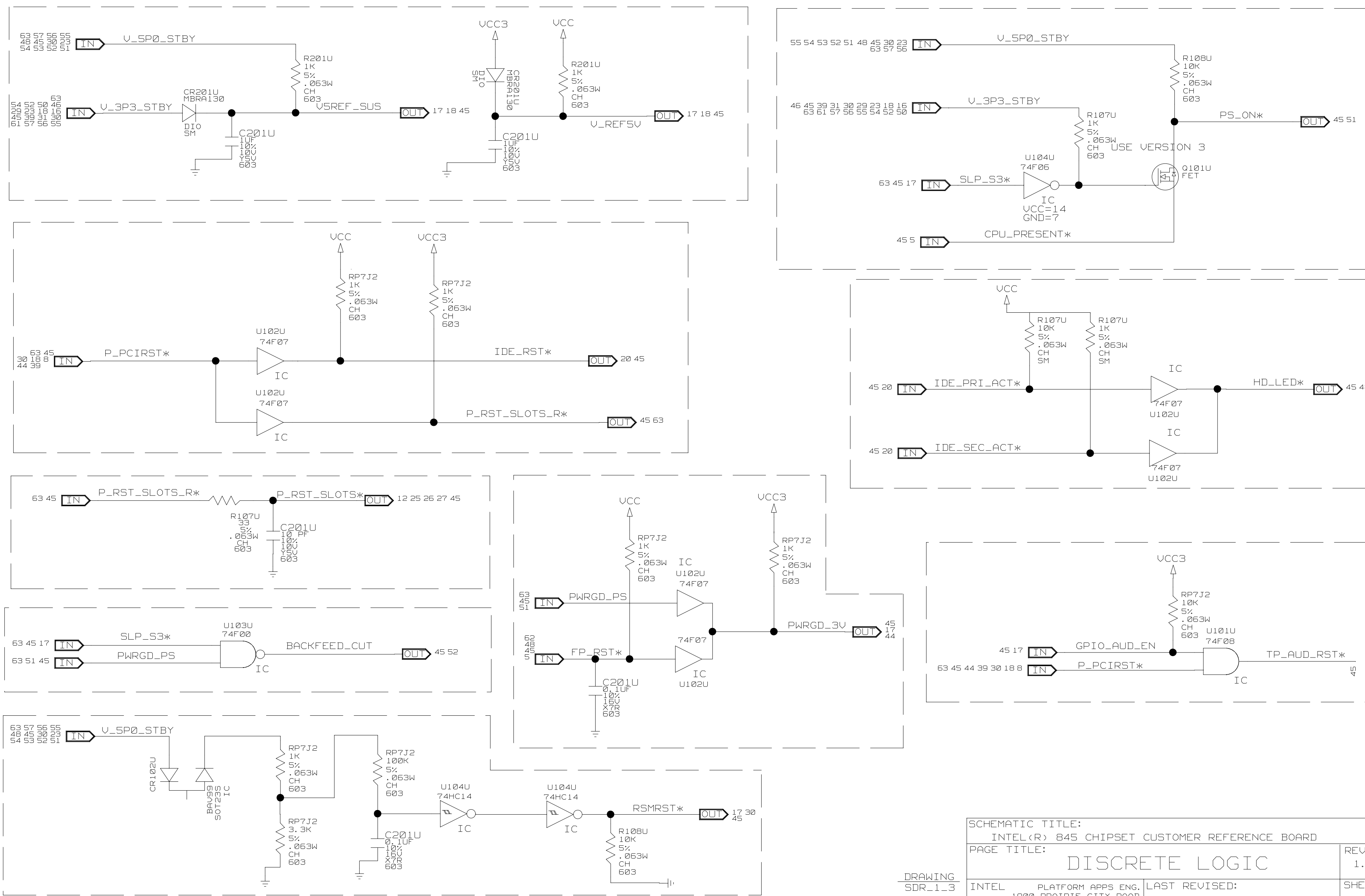
LAST REVISED: Tue Aug 28 15:42:24 2001

SHEET: 62



SCHEMATIC TITLE:
INTEL(R) 845 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
DISCRETE LOGIC

REV: 1.3

INTEL
PLATFORM APPS ENG.
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LAST REVISED: Wed Aug 29 08:59:41 2001

SHEET: 63