i.MX 93 Hardware Design Guide

Rev. 1 — 13 April 2023 User guide

Document Information

Information	Content
Keywords	IMX93HDG, i.MX 93 series of processors, i.MX93 EVK, i.MX93 QSB, design checklist, layout recommendations, power connectivity, routing, thermal considerations, stack-up information
Abstract	This document describes guidelines to design and test the i.MX 93 series of processors. It also includes board layout examples and design checklists.

1 Overview

This document aims to help hardware engineers design and test the i.MX 93 series processors. It provides examples on board layout and design checklists to ensure first-pass success, and solutions to avoid board bring-up problems.

Prerequisites include familiarity of board layouts and board hardware terminology.

This guide is released with relevant device-specific hardware documentation, such as datasheets, reference manuals, and application notes. Some of these documents are available on www.nxp.com/imx93evk.

1.1 Device supported

This document supports the i.MX 93 device. The tests described in this document are for i.MX93 EVK and i.MX93 QSB boards.

1.2 Essential references

This guide is supplementary to the i.MX 93 series chip reference manuals and data sheets. For reflow profile and thermal limits during soldering, see General Soldering Temperature Process Guidelines (document AN3300).

1.3 Supplementary references

1.3.1 General information

The following documents introduce the Arm processor architecture:

- For information about the Arm Cortex-A55 processor, see **https://www.arm.com/products/silicon-ip-cpu/cortex-a/cortex-a55**
- For information about the Arm Cortex-M33 processor, see **https://www.arm.com/products/processors/cortex-m/cortex-m33-processor.php**

For details of computer architecture refer to the following documents:

- *Computer Architecture - A Quantitative Approach (Fourth Edition)* - John L. Hennessy and David A. Patterson
- *Computer Organization and Design - The Hardware/Software Interface (Second Edition)* - David A. Patterson and John L. Hennessy

The following documents introduce the topic of high-speed board design:

- *Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II* - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936- 0-72
- *Signal and Power Integrity Simplified (2nd Edition) - Eric Bogatin (Prentice Hall)*- ISBN 0-13-703502-0
- *High Speed Digital Design- A Handbook of Black Magic* - Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1
- *High Speed Signal Propagation- Advanced Black Magic* - Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
- *High Speed Digital System Design- A handbook of Interconnect Theory and Practice* - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
- *Signal Integrity Issues and Printed Circuit Design* - Doug Brooks (Prentice Hall) ISBN 0-13-141884-X
- *PCB Design for Real-World EMI Control* - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2
- *Digital Design for Interference Specifications - A Practical Handbook for EMI Suppression* - David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X

- *Electromagnetic Compatibility Engineering* - Henry Ott (1st Edition - John Wiley and Sons) - ISBN 0-471-85068-3
- *Introduction to Electromagnetic Compatibility* - Clayton R. Paul (John Wiley and Sons) - ISBN 978-0-470-18930-6
- *Grounding & Shielding Techniques* - Ralph Morrison (5th Edition - John Wiley & Sons) - ISBN 0-471-24518-6
- *EMC for Product Engineers* - Tim Williams (Newnes Publishing) - ISBN 0-7506- 2466-3

1.4 Related documentation

For the list of current documents, refer to i.MX93/Documentation.

Additional literature would be published as and when new NXP products become available.

- For thermal management guidelines, refer to AN4579.
- Refer to the '*CCM*' chapter in the *i.MX 93 Chip Reference Manual* for details of clocks.
- For more information about general high-speed routing considerations, see *High-Frequency Design Considerations* (document AN12298).

1.5 Conventions

Table 1 lists the notational conventions used in this document.

In this document, notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follow C Language conventions.

Table 1. Conventions used in the document

Conventions	Description
Courier	Used to indicate commands, command parameters, code examples, and file and directory names.
Italics	Used to indicate command or function parameters.
Bold	Function names are written in bold.
cleared/set	When a bit takes the value zero, it means to be cleared; when it takes a value of one, it means to be set.
mnemonics	Instruction mnemonics are shown in lowercase bold. Book titles in text are set in italics.
sig_name	Internal signals are written in all lowercase.
nnnn nnnnh	Denotes hexadecimal number
0b	Denotes binary number
rA, rB	Instruction syntax used to identify a source GPR
rD	Instruction syntax used to identify a destination GPR
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.
x	An italicized x indicates an alphanumeric variable.
n, m	An italicized n indicates a numeric variable.

1.6 Acronyms and abbreviations

The table below defines the acronyms and abbreviations used in this document.

Table 2. Definitions and acronyms

Acronym	Definition
Arm	Advanced RISC Machines processor architecture
BGA	Ball Grid Array package
BOM	Bill of Materials
BSDL	Boundary Scan Description Language
BSP	Board Support Package
CAN	Flexible Controller Area Network peripheral
CCM	Clock Controller Module
CSI	MIPI Camera Serial Interface
DDR	Dual Data Rate DRAM
DDR4	DDR4 DRAM
DDRC	DDR Controller
DFP	Downstream Facing Port (USB-Type C)
DRP	Dual Role Port (USB-Type C)
ECSPI	Enhanced Configurable SPI peripheral
EIM	External Interface Module
EMI	Electromagnetic interference
ENET	10/100/1000 Mbit/s Ethernet MAC peripheral
EPIT	Enhanced Periodic Interrupt Timer peripheral
ESR	Equivalent Series Resistance
GA	General Availability
GND	Ground
GPC	General Power Controller
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	i.MX 93 chip-level I/O multiplexing
JTAG	Joint Test Action Group
KPP	Keypad Port Peripheral
LDB	LVDS Display Bridge
LDO	Low Drop-Out regulator
LPCG	Low-Power Clock Gating
LPDDR4	Low-Power DDR4 DRAM
LVDS	Low-Voltage Differential Signaling
ODT	On-Die Termination
OTP	One-Time Programmable
PCB	Printed-circuit board

Table 2. Definitions and acronyms...*continued*

Acronym	Definition
PCIe	PCI Express
PCISig	Peripheral Component Interconnect Special Interest Group
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
PTH	Plated Through Hole PCB (that is, no microvias)
QSB	Quick Start Board
RGMII	Reduced Gigabit Media Independent Interface (Ethernet)
RMII	Reduced Media Independent Interface (Ethernet)
ROM	Read-only Memory
TDP	Thermal Design Power
TIM	Thermal Interface Materials

1.7 Disclaimers

Nothing in this document relieves the design engineer/customer from ultimate responsibility in producing a proper functioning DRAM subsystem that meets JEDEC specifications. For compliance details, refer Section 3.7.

It is expected that the design engineer already has a strong understanding of PCB design using high-speed components. This is not an all-encompassing training document that can be used by beginning designers to produce reliable PCB designs using modern processors.

Design engineers should use all available design guidelines provided by the manufacturers of other high-speed components used in the system. Should a conflict arise between this document and the guidelines from other manufactures, contact NXP for resolution (community.nxp.com).

NXP strongly recommends that one of the example layouts provided for the i.MX9 designs be copied exactly for the placement of the processor, DRAM device, decoupling capacitors underneath the processor, and the interconnecting traces/vias between these parts. This includes the board stack-up design and PCB dielectric materials chosen. These designs have been tested and validated at NXP and they are proven reliable. While NXP does not expect every customer to copy our designs, customers must expect that the amount of support that can be provided for assisting a new design cannot be as great as the support provided for designs already known to NXP.

NXP provides the processor IBIS models and timing models necessary for performing complete DRAM simulations of a design. NXP strongly recommends that the end users perform simulations of any new designs before the release of a PCB layout design for manufacturing.

Processor Reference Manuals and User's Guides are continuously reviewed and revised to contain the most up-to-date information regarding the processor. In addition, Errata and Engineering bulletins may be issued to document unintended processor behavior. The design engineers should consult the official NXP website for the latest versions of these documents as a part of the final checks of a PCB design before releasing the board to manufacturing.

When a fully assembled board is returned to the design engineer, it is the engineer's responsibility to perform a complete check of the board design to ensure that all subsystems are functioning correctly. See Section 6 for recommended board bring-up guidelines.

2 i.MX 93 design checklist

This document provides a design checklist for the i.MX 93 processor. The design checklist tables recommend optimal design and provide explanations to help users understand better. All supplemental tables referenced by the checklist appear in sections following the design checklist tables.

2.1 Design checklist tables

Table 3. LPDDR4/4X recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	Connect the DRAM_ZQ ball on the processor to a 120 Ω, 1% resistor to GND.	This is a reference used during DRAM output buffer driver calibration.	☐
2	The ZQ0 ball on the LPDDR4/4X device should be connected through a 240 Ω, 1% resistor to the LPDDR4/4X VDDQ rail.	—	☐
3	Place a 10 kΩ, 5% resistor to ground on the DRAM reset signal.	This ensures adherence to the JEDEC specification until the control is configured and starts driving the DDR.	☐
4	The ODT_CA balls on the LPDDR4/4X device should be connected directly to the LPDDR4/4X VDD2 rail.	LPDDR4/4X ODT on the i.MX 93 is command-based, making processor ODT_CA output balls unnecessary.	☐
5	The architecture for each chip inside the DRAM package must be x16.	The processor does not support byte mode specified in JESD209-4B.	☐
6	The processor ball DRAM_MTEST1 should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.	☐
7	Ensure that VDDQ_DDR/VDD2_DDR power up ramp rate is less than 24 V/ms.	Too fast ramp rate on VDDQ_DDR/VDD2_DDR might trigger the ESD protection circuit.	☐

Table 4. I2C recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	Verify the target I2C interface clock rates.	The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.	☐
2	Verify that there are no I2C address conflicts on any of the I2C buses utilized.	There are multiple I2C ports available on chip, so if a conflict exists, move one of the conflicting devices to a different I2C bus. If it is impossible, use a I2C bus switch (NXP part number PCA9646).	☐
3	Do not place more than one set of pullup resistors on the I2C lines.	This could result in excessive loading and potential incorrect operation. Choose the pullup value commensurate with the bus speed being used.	☐
4	Ensure that the VCC rail powering the i.MX 93 I2C interface balls matches the supply voltage used for the pull-up resistors and the slave I2C devices.	Prevent device damage or incorrect operation due to voltage mismatch.	☐

Table 5. JTAG recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	Do not use external pull-up or pull-down resistors on JTAG_TDO.	JTAG_TDO is configured with an on-chip keeper circuit and the floating condition is actively eliminated.	☐
2	Follow the recommendations for external pull-up and pull-down resistors given in Table 12.	—	☐

Table 6. Reset and ON/OFF recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	The POR_B input must be asserted at power up and remain asserted until the last power rail for devices required for system boot is at its working voltage. The PMIC (PCA9451AHNY) on i.MX93 EVK controls this functionality.	The PMIC drives POR_B. If a reset button is used, connect it to the PMIC_RST_B pin of the PMIC instead of directly connecting it to POR_B pin of the CPU. This connection ensures that all the peripheral devices are reset along with i.MX93. ***Note:*** *When POR_B on the i.MX 93 is asserted (low), then, the output PMIC_ON_REQ remains asserted (high). Therefore only toggling POR_B does not reset the peripheral devices. Only toggling POR_B might cause the system to fail to reboot after resetting.*	☐
2	For portable applications, the ONOFF pin may be connected to an ON/OFF SPST push-button switch to ground. An external pull-up resistor is required on this pin.	A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power- down). The connection to GND for approximate 5 seconds or more causes a forced OFF.	☐
3	In order to repower the system (except SNVS), users must connect WDOG_ANY ball to external PMIC or reset IC.	In Idle mode, internal reset source cannot reset i.MX93. In such a case, the processor should be repowered. Some peripherals such as SD3.0 and QSPI should also be repowered during system reset.	☐
4	WDOG_ANY ball is used as Cold Reset. If a PMIC other than PCA9451 is used, an external pull-up resistor (100 KΩ) is required to support boundary-scan mode.	In Boundary-scan mode, WDOG_ANY is left floating. Without the external 100 KΩ pull-up, WDOG_ANY might repeatedly reset the system when entering Boundary-scan mode. The PCA9451 disables WDOG_ANY reset by default, so it is not impacted.	☐
5	While using a low power design, the wake up source should be on the I/Os within the NVCC_AON domain.	The I/Os within the NVCC_AON domain are associated with M33 core, which is supposed to be used in low power design.	

Table 7. USB recommendations

Checkbo	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	Connect a 200 Ω, 1% resistor to the ground on the USBx_TXRTUNE ball.	—	☐
2	Route all USB differential signals with 90 Ω differential impedance.	—	☐

Table 7. USB recommendations*...continued*

Checkbo	Recommendations	Explanation/Supplemental recommendations	Checkbox
3	ESD protection should be implemented at the connector pins. Choose a low capacitance device recommended for high-speed interfaces.	This prevents potential damages to board components from ESD.	☐
4	If USB connectors MicroAB or MicroB are used, USBx_VBUS must not connect directly to the 5 V VBUS voltage of connector. Instead, this pin must be isolated using an external 30 K 1% resistor.	—	☐

Table 8. Oscillator/Crystal recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	Connect a 24 MHz crystal between XTALI _24M and XTALO_24M balls.	• This crystal should have ESR not greater than 60 Ω, and be rated for a drive level of at least 100 µW. • Follow the manufacturer's recommendation for loading capacitance. • Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.	☐
2	Connect a 32.768 kHz between RTC_XTALI and RTC_XTALO balls. Alternatively, an external 32.768 kHz clock can be fed into RTC_XTALI to provide the RTC clock for the i.MX 93. See item #3.	• This crystal should have ESR not greater than 70 kΩ, and be rated for a drive level of at least 0.5 µW. • Follow the manufacturer's recommendation for loading capacitance. • Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.	☐
3	If using external 32.768 kHz clock rather than a crystal to provide the RTC clock, it should be connected to RTC_ XTALI pin. The RTC_XTALO pin must remain unconnected or driven by a complementary signal	The voltage level of this driving clock should not exceed the voltage of the NVCC_BBSM_1P8 rail, or damage/ malfunction might occur. The RTC signal should not be driven if the NVCC_BBSM_1P8 supply is OFF. For RTC V_{IL} and V_{IH} voltage levels, see the latest i.MX 93 data sheet available at www.nxp.com/i.MX93/Documentation.	☐

Table 9. i.MX 93 power/decoupling recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	Comply with the power-up sequence guidelines as described in the data sheet to guarantee reliable operations of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst case)	☐
2	Maximum ripple voltage requirements	Common requirement for ripple noise peak-to-peak value should be less than 5% of the supply voltage nominal value.	☐
3	If PCA9451AHNY PMIC is used to provide power, ensure that the output L/C components	Leaving any regulator output open will lead to malfunction of the whole PMIC.	☐

Table 9. i.MX 93 power/decoupling recommendations*...continued*

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
	of all regulators are properly connected, even if unused.		
4	Check PMIC switcher output currents and the switcher inductor current ratings are sufficient for the maximum supply currents ratings per rail as specified within the data sheet.	When using a non-NXP PMIC, or scaling down a power rail, ensure that the PMIC and inductor meet the maximum current demands of the system. ***Note:*** *Currents will be higher at hotter SoC temperatures than at room temperature.*	☐

Table 10. Decoupling capacitors recommendations

S.No	Supply	0.22 µF	1 µF	10 µF	Notes	Checkbox
1	VDD_SOC	—	6	2		☐
2	VDD2_DDR	—	6	1	—	☐
3	VDDQ_DDR	—	2	1	—	☐
4	VDD_BBSM_0P8_CAP	1	—	—	—	☐
5	NVCC_BBSM_1P8	—	1	—	—	☐
6	VDD_ANA0_1P8, VDD_ANA1_1P8, VDD_ANADET_1P8, VDD_LVDS_1P8, VDD_MIPI_1P8, VDD_USB_1P8	—	6	—	These 6 power rails are combined on EVK, and are then combined with NVCC_WAKEUP through a filter consisting of a ferrite bead and 2 x 22 µF capacitors.	☐
7	VDD_USB_0P8, VDD_MIPI_0P8, VDD_ANA_0P8	—	5	—	These 3 power rails are combined on EVK.	☐
8	NVCC_WAKEUP	—	2	—	—	☐
9	NVCC_AON	—	1	—	—	☐
10	NVCC_GPIO	—	1	—	—	☐
11	NVCC_SD2	—	1	—	—	☐
12	VDD_USB_3P3	—	1	—	—	☐
	Capacitor part number used on EVK: • 0.22 µF --- LMK063BJ224MP-F • 1 µF --- CL03A105KP3NSNC • 10 µF --- CL05A106MQ5NUNC					

Table 11. PCB design recommendations

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
1	High-speed signal traces have reference plane in adjacent layer and are impedance-controlled.	Controlled impedance is the key factor to have good signal integrity. Note that the reference plane can only be GND or the signal's own I/O power. Do not use other nets as reference.	☐
2	High-speed signal traces never cross gap or slot in reference plane.	Crossing gap in reference plane will cause reflection and increase crosstalk.	☐

Table 11. PCB design recommendations*...continued*

S.No	Recommendations	Explanation/Supplemental recommendations	Checkbox
3	Place at least one GND stitching via within 50 mils of signal via when switching reference planes.	GND stitching via can help keep impedance continuous and reduce via crosstalk.	☐
4	Appropriate delay matching is done for parallel bus.	Signals within a bus should have delay time matched to maintain timing margin.	☐
5	The true and complementary signal of a differential pair must have delay matched to within 1 ps.	The true and complementary signal within a differential pair should have delay time tightly matched.	☐
6	DDR interface passed Si simulation. Alternatively, directly copy the EVK DDR layout design.	Generally, Si simulation should be performed for DDR interface that runs at 3733 MT/s to ensure stable working. If this is not feasible, just copy the EVK DDR layout design as well as the board stack-up and materials.	☐
7	Place test point on key signals to ease debugging. While placing test points on high-speed signal traces, ensure that the diameter of the test point is no more than 20 mil. Test points should be directly placed on the trace with no stub.	Test points can bring excessive capacitance and should be carefully handled on high-speed signal traces.	☐
8	Decoupling capacitors are placed as close to IC power pins as possible.	This strategy reduces the inductance from decoupling capacitor to IC power pin. Therefore such placement improves decoupling effectiveness.	☐

2.2 JTAG signal termination

Below is a JTAG termination chart showing the terminations that should be placed on PCB designs.

Table 12. Recommended JTAG board terminations

JTAG signal	I/O type	External termination	Comments
JTAG_TCK	Input	None	Internal pull down, no external termination required.
JTAG_TMS	Input	None	Internal pull up to NVCC_WAKEUP, no external termination required.
JTAG_TDI	Input	None	Internal pull up to NVCC_WAKEUP, no external termination required.
JTAG_TDO	3-state output	None	—

2.3 General recommendations

More than one software operating environment can run on the i.MX 93 platforms concurrently. Peripherals on these SoCs are accessible to all software operating environments. A conflict can occur when more than one software operating environment reads or writes the state of the same peripheral.

Therefore, software operating environments must be isolated from each other when accessing shared resources. For instance, if two operating environments read and write the same region of DRAM without coordinating their access, results are unpredictable. The same behavior is applicable for peripheral registers, especially for the IP modules which offer multiple logical channels. For example, GPIO, I2C, SPI, SAI, and DMA.

Therefore, any sharing of an IP module between Cortex-M and Cortex-A domains must be coordinated with the system software architecture because software operating environments must be isolated from each other when accessing shared resources in order to avoid safety/reliability issues.

Consider an example. Individual GPIO pins are aggregated into groups, each group is controlled by a single GPIO module. Each GPIO module is a distinct peripheral that must be protected from conflicting access by different software operating environments. For example, GPIO1 module is assigned as a shared peripheral for Linux on the Arm Cortex-A and RTOS on the Cortex-M. Cortex-A and Cortex-M should obtain a semaphore lock before access to any pin of GPIO1 module is allowed. If Cortex-A and Cortex-M attempt to access to GPIO1 module at the same time, it can result in lack of isolation leading to safety/reliability issues.

Note:

Resource allocation should assure that peripherals have external signals pinned out and their IO resources can be synchronously controlled either by Cortex-A or Cortex-M in the corresponding software operating environment.

Not allocating correctly can result in lack of isolation leading to safety/reliability issues that can only be overcome using complex software such as virtual drivers. Use of such software can indirectly affect the hardware isolation of software domains and the peripheral performance. In this case, customer needs to implement customized software solutions such as RPMSG Client/server-style cooperative device drivers or Peripheral Exclusive Access using a Mutex solution implemented using SEMA42. Implementation on the i.MX 93 is up to the Software Architecture chosen by customer.

Under those circumstances, the Peripheral Modules should be allocated to Software Systems per module basis and not a per signal basis from board design phase.

3 i.MX 93 layout/routing recommendations

3.1 Introduction

This chapter describes how to assist design engineers with the layout of an i.MX 93-based system.

3.2 Basic design recommendations

When using the Allegro design tool, the schematic symbol and PCB footprint created by NXP is recommended. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If the export is not possible, create the footprint per the package dimensions outlined in the product data sheet.

Note: *Native Allegro layout and gerber files would be made available on www.nxp.com/imx93evk/DesignTools & Files.*

3.3 Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 or 0402 decoupling and 0603 or larger bulk capacitors should be mounted as close as possible to the power vias. The distance should be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the i.MX 93 EVK layouts for the recommended decoupling capacitor placement.

The following list describes how to choose correct decoupling scheme:

- Place the largest capacitance in the smallest package that budget and manufacturing can support.
- For high-speed bypassing, select the required capacitance with the smallest package (for example, 1.0 µF, or even 2.2 µF in a 0201 package size).
- Minimize trace length (inductance) to small caps.
- Series inductance cancels out capacitance.
- Tie caps to GND plane directly with a via.
- Place capacitors close to the power ball of the associated package from the schematic.
- A preferred BGA power decoupling design is available on the EVK board design available on www.nxp.com/imx93evk. Customers should use the NXP design strategy for power and decoupling.

3.4 Stack-up and manufacturing recommendations

3.4.1 Stack-up recommendation

Due to the number of balls on the i.MX 93 processor in the package, a minimum 6-layer PCB stack-up is recommended. For the smaller 9 mm x 9 mm package, a minimum 4-layer PCB stack-up can be achieved. For either the 6-layer or 4-layer stack-up, at least one layer should be dedicated to power on routing to meet the IR drop target of 2% for the i.MX 93 CPU power rails.

The constraints for the trace width depend on such factors as the board stack-up, the associated dielectric and copper thickness, required impedance, and required current (for power traces). The stack-up also determines the constraints for routing and spacing. Consider the following requirements when designing the stack-up and selecting board material:

- **Board stack-up is critical for high-speed signal quality.**
- **Pre-planning impedance of critical traces is required.**
- **High-speed signals must have reference planes on adjacent layers.**

- **PCB material: the material used on EVK is 185HR.**

3.4.2 Manufacturing recommendation

Since the i.MX 93 processor uses 0.5 mm-pitch BGA package, the PCB technology must meet below requirement to fully fanout all the signals of the processor using PTH (plated through holes).

- **Minimum trace width: 3.2 mil**
- **Minimum trace to trace/pad spacing: 3.2 mil**
- **Minimum via size: 8 mil diameter hole, 16 mil diameter pad**
- **Minimum via pad-to-pad spacing: 4 mil**

The figure below shows the reference routing of the i.MX 93, PTH is OK for the fanout, HDI is not needed.

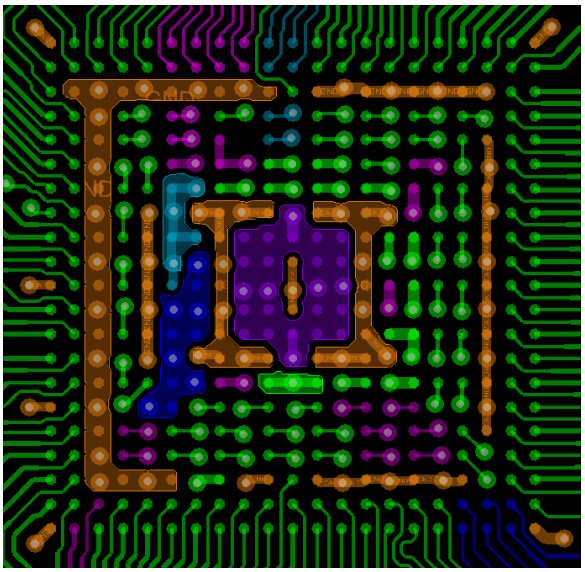

Figure 1. i.MX 93 fanout routing on EVK

3.5 PCB stack-up examples

The following sections show examples for stack-up of the i.MX93 EVK and i.MX93 QSB boards.

3.5.1 EVK PCB stack-up

The tables below show stack-up of the MCIMX93 EVK. The CPU board uses 6-layer stack-up and the BB board uses 8-layer stack-up.

Table 13. MCIMX93-SOM Board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	**Signal**	0.5+Plating			
	Dielectric		PP1080	3.67	2.8 mil
2	**GND**	1			
	Dielectric		Core 0.076 mm	3.86	3 mil
3	**Signal**	1			

Table 13. MCIMX93-SOM Board stack up information*...continued*

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
	Dielectric		PP 1080*2 Core 0.8 mm PP 1080*2	3.67	41.082 mil
4	**Power**	1			
	Dielectric		Core 0.076 mm	3.86	3 mil
5	**GND**	1			
	Dielectric		PP 1080	3.67	2.8 mil
6	**Signal**	0.5+Plating			
Finished:	62.992(6.299/-6.299) mil			1.6(+0.16/-0.16) mm	
Designed:	58.268 mil			1.48 mm	
Material:	185HR				

Table 14. MCIMX93-BB Board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	**Signal**	0.5+Plating			
	Dielectric		1080	3.85	2.646 mil
2	**GND**	1			
	Dielectric		Core 0.13 mm	4.2	5.12 mil
3	**Signal**	1			
	Dielectric		1080*2 2116	3.95	9.674 mil
4	**Power**	1			
	Dielectric		Core 0.8 mm	4.47	31.5 mil
5	**Power**	1			
	Dielectric		1080*2 2116	3.95	9.638 mil
6	**Signal**	1			
	Dielectric		Core 0.13 mm	4.2	5.12 mil
7	**GND**	1			
	Dielectric		1080	3.85	2.646 mil
8	**Signal**	0.5+Plating			
Finished:	78.74(7.874/-7.874) mil			2(+0.2/-0.2) mm	
Designed:	75.236 mil			1.911 mm	
Material:	TU768				

3.5.2 QSB PCB stack-up

The tables below shows stack-up of the Quick Start Board (QSB). It is based on i.MX93 9x9 package and a 4-layer stack-up is used.

Table 15. MCIMX93-QSB Board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.5+Plating			
	Dielectric		106H	3.52	2.072
2	GND	1			
	Dielectric		Core 1.4MM	3.76	55.12
3	Power	1			
	Dielectric		106H	3.52	2.072
4	Signal	0.5+Plating			
Finished:	62.992 (6.299/-6.299) mil			1.6 (+0.16/-0.16) MM	
Designed:	63 mil			1.57 MM	
Material:	185HR				

3.6 DDR design recommendations

3.6.1 LPDDR4/4X-3733 design recommendations

The following list provides some generic guidelines that should be adhered to when implementing an i.MX 93 design using LPDDR4/4X.

1. It is expected that the layout engineer and design team already has experience and training with DDR designs at speeds of 1.867 GHz / 3733 MT/s.
2. Use solid GND planes as reference planes for all the high-speed signal traces. The only exception that is allowed is CKE and DQS signal, for which power plane can be used as reference plane in the case of a 4-layer board design of i.MX93 9X9 package.
   Note: *Users must ensure that there is no discontinuity or slot on the reference plane underneath the traces.*
3. Keep edge to edge spacing of high-speed signal traces no less than 2 times the trace width to minimize trace crosstalk. Widen edge-to-edge spacing to 3x-4x where space is available in order to further minimize crosstalk.
4. At a speed of 3733 MT/s, signal vias can be a significant source of crosstalk. Improper design of signal vias can introduce crosstalk larger than that from the trace. To minimize via crosstalk follow the below:
   a. Make sure that the total number of vias is no more than two on each point-to-point single-ended/ differential trace.
   b. Place at least one ground stitching via within 50 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 2. The i.MX 93 is optimized to use layer 1 and layer 3 for all single-ended traces. The differential traces, CLK, DQS0,1 are often routed on the bottom layer. These require the stitching GND vias. The EVK reference design demonstrates this method.

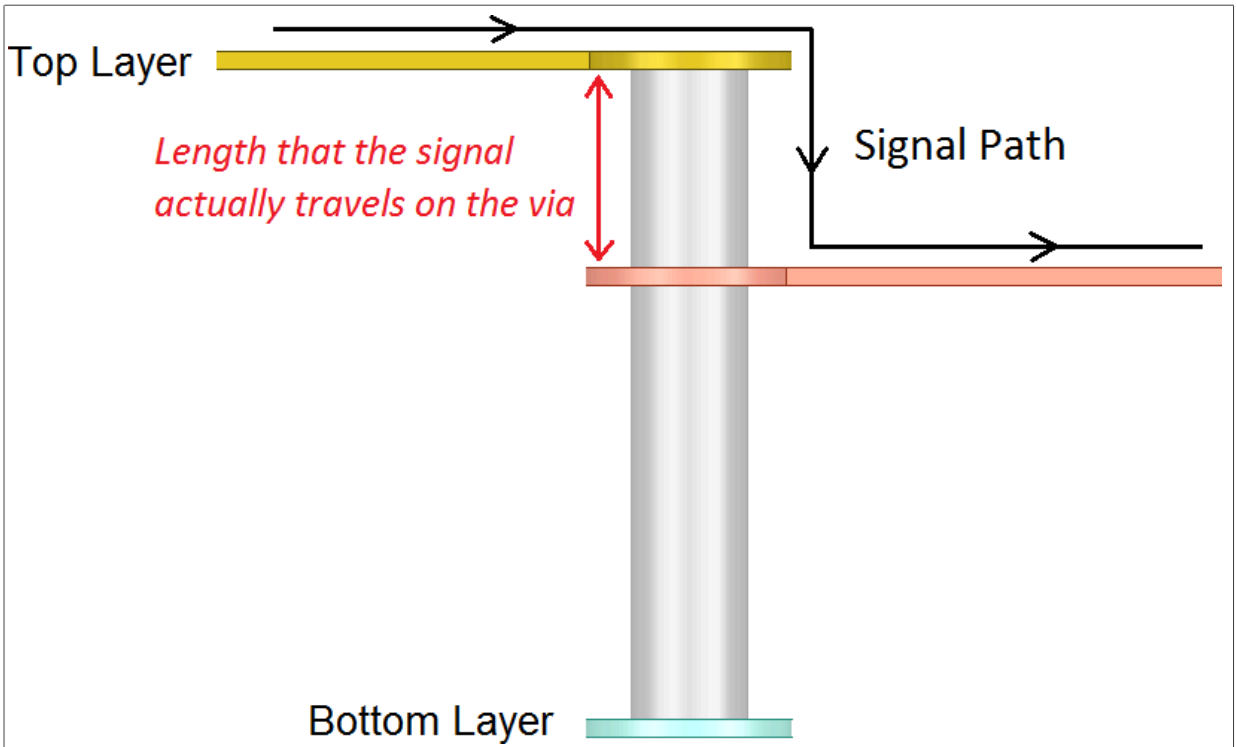

Figure 2. Length that the signal actually travels on the Via

5. CLK and DQS signal can be routed on different layer with DQ/CA signals to ease routing. When doing this, keep no less than 5 times trace width spacing from other signals.
6. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.
7. Include the delay of vias when performing delay matching. This can be realized in Allegro tool by enabling the Z Axis Delay in "**Setup** -> **Constraints** -> **Modes**".
8. Bit swapping within each slice/byte lane is OK. Byte swapping is NOT allowed.
9. Bit swapping of Command/Address (CA[5:0]) pins is NOT allowed.
10. i.MX 93 does not drive *ODT_CA* signals. The *ODT_CA* balls on the LPDDR4/4X devices should be connected directly or through a resistor to the VDD2 supply.
11. In general, the 200-ball LPDDR4/4X package should be placed ~200 mils from the i.MX 93.
12. Make sure to enable the DBI (data bus inversion) feature. This reduces power consumption and noise.

3.6.2 i.MX 93 LPDDR4/4X-3733 routing recommendations

LPDDR4/4X-3733 needs to be routed with signal fly times matched shown in Table 16. The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling the Z Axis Delay in "Setup - Constraints - Modes".

An example of the delay match calculation has been shown for the i.MX 93 EVK board design in Table 17 and Table 18. This analysis was done for the LPDDR4/4X-3733 implementation using the i.MX 93. In Table 17 and Table 18, the PCB Delay column is obtained directly from the Allegro PCB file. The Pkg Delay column is the package delay obtained from Section 3.6.6.

NXP strongly recommends that users simulate their LPDDR4/4X implementation before fabricating PCBs.

Table 16. i.MX 93 LPDDR4/4X-3733 routing recommendations

LPDDR4/4X-3733				
LPDDR4/4X signal	Group	PCB+ package prop delay		
		Min	Max	Considerations
CK_T/CK_C	Clock	Short as possible	200 ps	Match the true/complement signals within 1 ps.
CS1, CS0	Address/Command/ Control	CK_t - 1 ps	CK_t+ 1 ps	-
CA5, CA4, CA3, CA2		CK_t - 50 ps	CK_t + 50 ps	Match CA5, CA4, CA3, CA2 within 2 ps
CA1, CA0, CKE1, CKE0				Match CA1, CA0, CKE1, CKE0 within 2 ps
DQS0_T/DQS0_C	Byte0 - DQS	CK_t- 125 ps	CK_t+ 75 ps	Match the true/complement signals of DQS within 1 ps.
DMI0	Byte0 - Data	DQS0_t-50 ps	DQS0_t+50 ps	
DQ[7:0]				
DQS1_T/DQS1_C	Byte1 - DQS	CK_t- 125 ps	CK_t+ 75 ps	
DMI1	Byte1 - Data	DQS1_t-50 ps	DQS1_t+50 ps	
DQ[15:8]				

Table 17. LPDDR4/4X delay matching example (CA/CTL signals)

Net Name	PCB Delay (ps)	Pkg Delay (ps)	Total Net Delay = (PCB + Pkg) Delay	Comments
DRAM_CK_T_A	163.9	40	203.9	Vias are L1-> L6->L1
DRAM_CK_C_A	164.3	40.2	204.5	Vias are L1-> L6->L1
DRAM_CA0_A	125	36.4	161.4	Vias are L1-> L3->L1
DRAM_CA1_A	118.2	42.7	160.9	Vias are L1-> L3->L1
DRAM_CA2_A	201.4	35.8	237.2	Vias are L1-> L3->L1
DRAM_CA3_A	193.9	43.5	237.4	Vias are L1-> L3->L1
DRAM_CA4_A	197.8	39	236.8	Vias are L1-> L3->L1
DRAM_CA5_A	190.6	45.8	236.4	Vias are L1-> L3->L1
DRAM_nCS0_A	164.3	39	203.3	Vias are L1-> L3->L1
DRAM_nCS1_A	166	37.8	203.8	Vias are L1-> L3->L1
DRAM_CKE0_A	124	37.2	161.2	Vias are L1-> L3->L1
DRAM_CKE1_A	129.1	33	162.1	Vias are L1-> L3->L1

Table 18. LPDDR4/4X delay matching example (byte lane 1 signals)

Net Name	PCB Delay (ps)	Pkg Delay (ps)	Total Net Delay = (PCB + Pkg) Delay	Comments
DRAM_SDQS1_T_A	90.2	20.9	111.1	Vias are L1-> L6->L1
DRAM_SDQS1_C_A	90.8	20.7	111.5	Vias are L1-> L6->L1
DRAM_DMI1_A	47.7	29.2	76.9	Routed on top layer, no via
DRAM_DQ8_A	60	35.9	95.9	Routed on top layer, no via

Table 18. LPDDR4/4X delay matching example (byte lane 1 signals)*...continued*

Net Name	PCB Delay (ps)	Pkg Delay (ps)	Total Net Delay = (PCB + Pkg) Delay	Comments
DRAM_DQ9_A	70.1	33.9	104	Routed on top layer, no via
DRAM_DQ10_A	54.5	30.9	85.4	Routed on top layer, no via
DRAM_DQ11_A	41.8	33.7	75.5	Routed on top layer, no via
DRAM_DQ12_A	42.3	32	74.3	Routed on top layer, no via
DRAM_DQ13_A	43.7	29.4	73.1	Routed on top layer, no via
DRAM_DQ14_A	59.3	27.4	86.7	Routed on top layer, no via
DRAM_DQ15_A	60.1	33.6	93.7	Routed on top layer, no via

3.6.3 LPDDR4/4X-3733 routing example (11x11 and 14x14 package)

The figures Figure 3, Figure 4, and Figure 5 below show the placement and routing of the LPDDR4/4X signals on the i.MX 93 EVK board (MCIMX93-EVK board), based on 11x11 package. The 14x14 package uses the same ball assignment as 11x11 package, so the routing is very similar to that shown here.

The CLK and DQS signals are routed on bottom layer to save routing space on top layer and layer 3. DQ and DMI signals are routed on top layer, and CA/CTL signals are routed on layer 3. This is to minimize the distance the signal actually travels on the via to minimize via crosstalk.

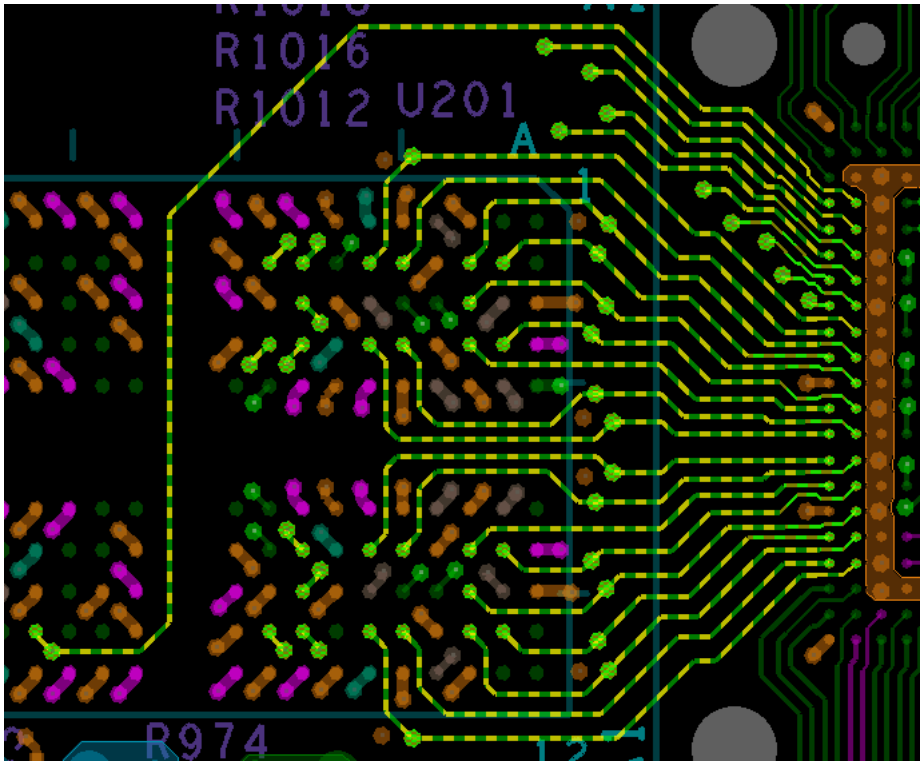

Figure 3. i.MX 93 EVK board LPDDR4/4X routing (Top Layer)

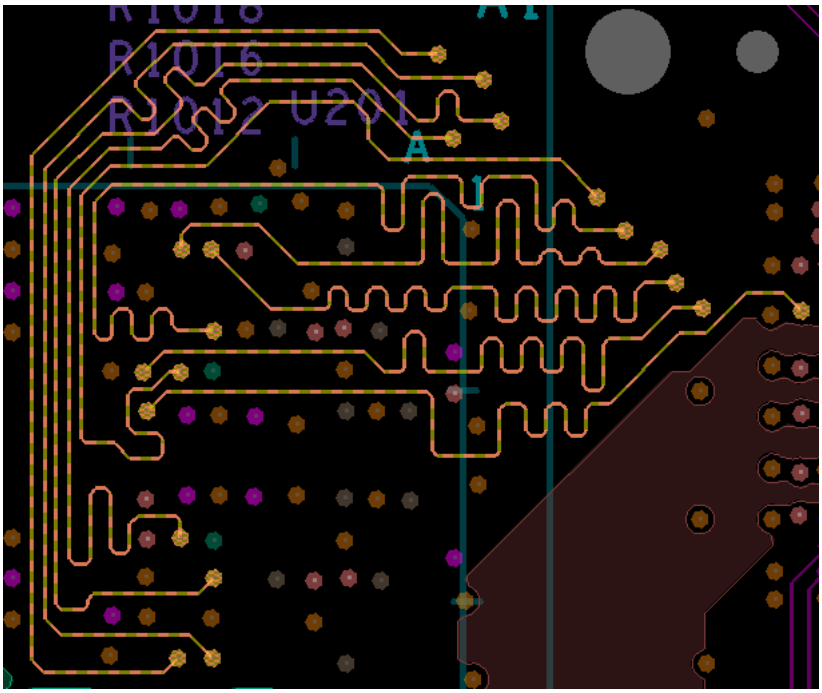

Figure 4. i.MX 93 EVK board LPDDR4/4X routing (Layer 3)

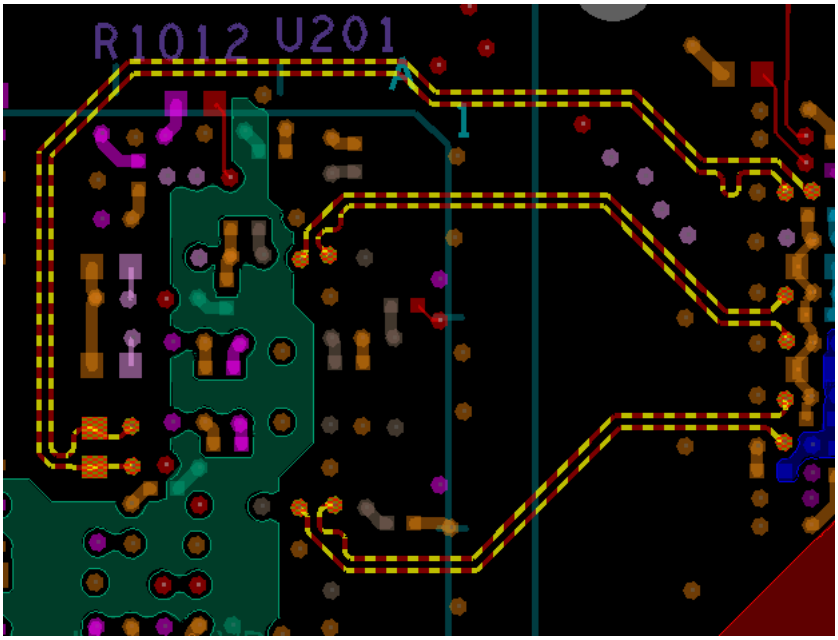

Figure 5. i.MX 93 EVK board LPDDR4/4X routing (Bottom Layer)

3.6.4 LPDDR4-3733 routing example (9x9 package)

The figures 6 and Figure 7 below show the placement and routing of the LPDDR4 signals on the i.MX 93 Quick Start Board (MCIMX93-QSB) which is based on 9x9 package. Taking advantage of the less number of I/Os on the 9x9 package, a 4-layer board design is realized. For a 4-layer board, only the signals routed on top layer will have a solid GND reference plane, so almost all the signals are routed on top layer except CKE whose toggle-

rate is very low and differential signals DQS which are not as sensitive to non-ideal reference plane as single-ended signals. The CKE and DQS signals are routed on bottom layer with power plane as reference plane. Note that there shall not be any discontinuity/slot on the reference plane underneath the traces.

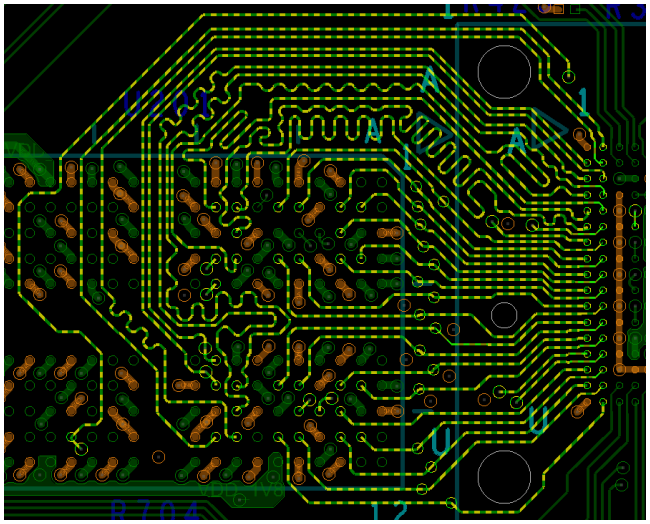

Figure 6. i.MX 93 QSB board LPDDR4 routing (Top Layer)

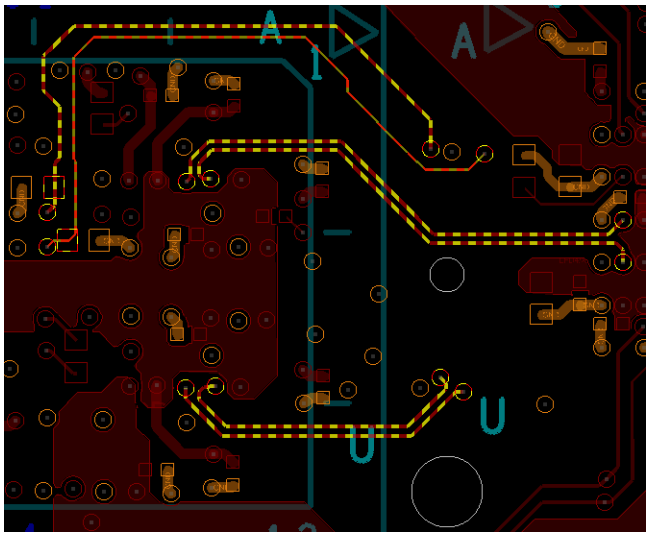

Figure 7. i.MX 93 QSB board LPDDR4 routing (Bottom Layer)

3.6.5 i.MX 93 DDR SI simulation guide

The simulation architecture includes the DDR controller (that is, the i.MX 93 processor), the PCB and the DRAM device. The IBIS model for the i.MX 93 processor is available from NXP. The DRAM device IBIS model must be obtained from the memory vendor.

This section describes how to check SI performance of the layout for a DDR design using the i.MX 93.

- Firstly, perform S-parameter extraction:
- It requires a 2.5D full-wave extraction tool, such as PowerSI from Cadence.
- Set the extraction bandwidth to 20 GHz.

- Port reference impedance: 50 Ω for signal ports, and 0.1 Ω for power ports.
- Coupled mode: Set the rise time to 20 ps and coupling coefficient to 1%.
- Secondly, perform time domain simulation:
- Stimulus pattern: 500-bit random code and different pattern for each signal within the same byte.
- Ideal power.
- Probe at the die.
- Simulation at slow corner (worst case).
- Eye waveform triggered by aligning with the timing reference (DQS/CLK).

When the simulation is done, find the simulated worst eye width and compare with following requirements to see if it can pass:

For LPDDR4/4X-3733

- **DQ Write**: Eye width @VREF ±70 mV should be over 187 ps.
- **DQ Read:** Eye width @VREF ±70 mV should be over 175 ps.
- **Cmd/Addr/Ctrl**: Eye width @VREF ±77.5 mV should be over 361 ps.
  The figure below shows an example of simulated eye width of LPDDR4/4X-3733 DQ write.

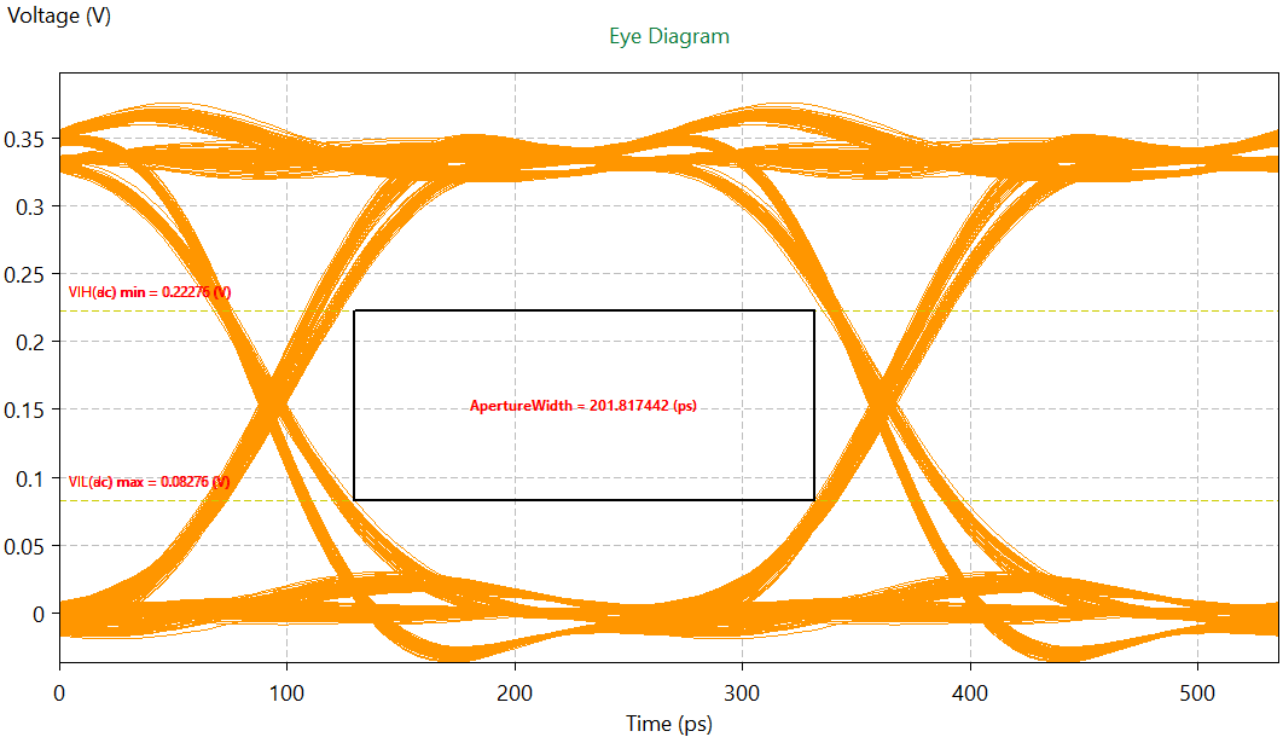

Figure 8. Example of simulated eye width

3.6.6 i.MX 93 DDR package delays

While performing the required delay matching for LPDDR4/4X routing, the substrate routing within the i.MX 93 package needs to be accounted for and included in the match calculation. The table below lists the propagation/ fly time from the die I/O to the package ball.

Table 19. i.MX 93 DDR package trace delays (11x11 package)

Ball Name	Delay (ps)	Ball Name	Delay (ps)
DRAM_CA0_A	36.4	DRAM_DQ03_A	30.3
DRAM_CA1_A	42.7	DRAM_DQ04_A	35.9
DRAM_CA2_A	35.8	DRAM_DQ05_A	33.5
DRAM_CA3_A	43.5	DRAM_DQ06_A	37.2
DRAM_CA4_A	39.0	DRAM_DQ07_A	37.0
DRAM_CA5_A	45.8	DRAM_DQ08_A	35.9
DRAM_CKE0_A	37.2	DRAM_DQ09_A	33.9
DRAM_CKE1_A	33.0	DRAM_DQ10_A	30.9
DRAM_CK_C_A	40.2	DRAM_DQ11_A	33.7
DRAM_CK_T_A	40.0	DRAM_DQ12_A	32.0
DRAM_CS0_A	39.0	DRAM_DQ13_A	29.4
DRAM_CS1_A	37.8	DRAM_DQ14_A	27.4
DRAM_DMI0_A	30.7	DRAM_DQ15_A	33.6
DRAM_DMI1_A	29.2	DRAM_DQS0_C_A	33.3
DRAM_DQ00_A	31.1	DRAM_DQS0_T_A	33.7
DRAM_DQ01_A	31.6	DRAM_DQS1_C_A	20.7
DRAM_DQ02_A	33.7	DRAM_DQS1_T_A	20.9

Table 20. i.MX 93 DDR package trace delays (14x14 package)

Ball Name	Delay (ps)
DRAM_CA0_A	45.7
DRAM_CA1_A	53.4
DRAM_CA2_A	49.7
DRAM_CA3_A	56.1
DRAM_CA4_A	53.2
DRAM_CA5_A	60.6
DRAM_CKE0_A	50.7
DRAM_CKE1_A	42.8
DRAM_CK_C_A	48.8
DRAM_CK_T_A	48.4
DRAM_CS0_A	53.6
DRAM_CS1_A	47.9
DRAM_DMI0_A	40.7
DRAM_DMI1_A	43.5
DRAM_DQ00_A	44.0
DRAM_DQ01_A	40.9
DRAM_DQ02_A	46.8

Table 20. i.MX 93 DDR package trace delays (14x14 package)*...continued*

Ball Name	Delay (ps)
DRAM_DQ03_A	40.3
DRAM_DQ04_A	47.5
DRAM_DQ05_A	43.0
DRAM_DQ06_A	49.8
DRAM_DQ07_A	46.0
DRAM_DQ08_A	52.6
DRAM_DQ09_A	48.7
DRAM_DQ10_A	45.9
DRAM_DQ11_A	49.6
DRAM_DQ12_A	45.7
DRAM_DQ13_A	42.1
DRAM_DQ14_A	40.4
DRAM_DQ15_A	47.5
DRAM_DQS0_C_A	32.6
DRAM_DQS0_T_A	32.8
DRAM_DQS1_C_A	31.7
DRAM_DQS1_T_A	31.9

Table 21. i.MX 93 DDR package trace delays (9x9 package)

Ball Name	Delay (ps)
DRAM_CA0_A	32.7
DRAM_CA1_A	45.2
DRAM_CA2_A	35.9
DRAM_CA3_A	43.2
DRAM_CA4_A	42.3
DRAM_CA5_A	50.6
DRAM_CKE0_A	37.0
DRAM_CKE1_A	34.5
DRAM_CK_C_A	48.1
DRAM_CK_T_A	47.2
DRAM_CS0_A	40.9
DRAM_CS1_A	36.3
DRAM_DMI0_A	24.5
DRAM_DMI1_A	30.9
DRAM_DQ00_A	19.1
DRAM_DQ01_A	24.7
DRAM_DQ02_A	24.4

Table 21. i.MX 93 DDR package trace delays (9x9 package)*...continued*

Ball Name	Delay (ps)
DRAM_DQ03_A	25.1
DRAM_DQ04_A	26.6
DRAM_DQ05_A	30.1
DRAM_DQ06_A	39.7
DRAM_DQ07_A	33.4
DRAM_DQ08_A	27.4
DRAM_DQ09_A	31.9
DRAM_DQ10_A	32.1
DRAM_DQ11_A	25.3
DRAM_DQ12_A	25.3
DRAM_DQ13_A	21.2
DRAM_DQ14_A	18.9
DRAM_DQ15_A	25.4
DRAM_DQS0_C_A	17.0
DRAM_DQS0_T_A	18.8
DRAM_DQS1_C_A	25.4
DRAM_DQS1_T_A	26.4

3.7 JEDEC specification compliance

The i.MX 93 processors are designed and tested to work with the JEDEC JESD209-4A–compliant LPDDR4/4X memories. Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. In this document, NXP cannot cover all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variations. The PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, via placement, ground and supply planes layout, and DDR controller/PHY register settings - all are factors affecting the performance of the memory system.

Nevertheless, this hardware user's guide contains a large amount of valuable design information that NXP believes aid the design engineers in developing a DRAM memory system compliant with the JEDEC standards. NXP has validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors, and DDR trace routing between the processor and the selected DDR memory.

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as a closure to a customer-reported DDR issue. Customers are responsible for properly designing the printed circuit board and correctly simulating and modeling the designed DDR system. They should validate the system under all expected operating conditions (temperatures and voltages) before releasing their product to the market.

3.8 High-speed routing recommendations

For more information about general high-speed routing considerations, see High-Frequency Design Considerations (document AN12298)

3.9 Reset architecture/routing

A reset button may be connected to **PMIC_RST_B** pin of the PMIC (PCA9451AHNY) for development purposes. This allows all voltages to be put to their initial default power-on state when depressing the reset button.

Pressing the reset button causes the PMIC to trigger a cold reset event. This causes all the power supplies except for the SNVS domain to be OFF. During this time, the **POR_B** driven by the PMIC is also kept asserted (low). This state remains for several hundred milliseconds to provide enough time for the power supplies to be completely powered down, and then the power supplies start ramping up again in defined sequence. When all the power supplies have reached their operating voltages, **POR_B** is de-asserted, and the CPU begins booting from reset.

3.10 Trace impedance recommendations

Table 22 is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/ trace widths.

Table 22. Trace impedance recommendations

Signal group	Impedance	PCB manufacturer tolerance (+/-)
All single-ended signals, unless specified	50 Ω Single-ended	10%
DDR DQS/CLK	85 Ω Differential	10%
USB differential signals	90 Ω Differential	10%
Differential signals, including Ethernet, MIPI (CSI and DSI), LVDS	100 Ω Differential	10%

Note:

If the customer wants to pass test 1.1.4 and 1.1.5 of the MIPI-DSI compliance test on their board, he should ensure that the parasitic capacitance of each PCB trace of MIPI-DSI data signals to be no more than 10 pF.

This is because the test requires connecting a 50 pF load board to the signal, and the capacitance load driving capability of the i.MX 93 MIPI-DSI LP driver is 70 pF. Considering that the i.MX 93 chip itself can have up to 10 pF capacitance, the final allowed maximum capacitance of the PCB trace is 10 pF. For normal function, the customer only needs to ensure that the total capacitance load seen by the i.MX 93 is no more than 60 pF.

3.11 Power connectivity/routing

Delivering clean, reliable power to the i.MX 93 internal power rails is critical to a successful board design. The PCB PDN should be designed to accommodate the maximum output current from each voltage regulator into the i.MX 93 supply balls. The table below lists the design goals for each high-current i.MX 93 power rail.

Table 23. i.MX 93 maximum current design levels

Supply input	i.MX 93 Max current (mA)
VDD_SOC	1500
VDD2_DDR	500
VDDQ_DDR	260

3.11.1 i.MX 93 Power distribution block diagram

There are companion PMICs that provide a low-cost and efficient solution for powering the i.MX 93 processor, for example, NXP PCA9451AHNY. The PCA9451AHNY features remote voltage sensing on BUCK1, BUCK2, and BUCK3. This implies that the output voltage sensing point can be on processor power pins to compensate for the IR drop of the power path from PMIC to processor.

However, this does not mean that the IR drop of the power path can be arbitrarily large. This is because resistance of the power path and capacitance of the decaps at processor power pins introduce phase lag and can lead to instability of the control loop. The 2% IR drop requirement should still be met.

The BUCK1 and BUCK3 can be combined to operate in dual phase mode to provide current up to 6A. In this mode, the R_SNSP3_CFG pin should be tied to GND.

Figure 9 shows a block diagram of the power tree of the NXP i.MX 93 EVK board. It uses a single PCA9451AHNY PMIC to power ON rails of the processor.

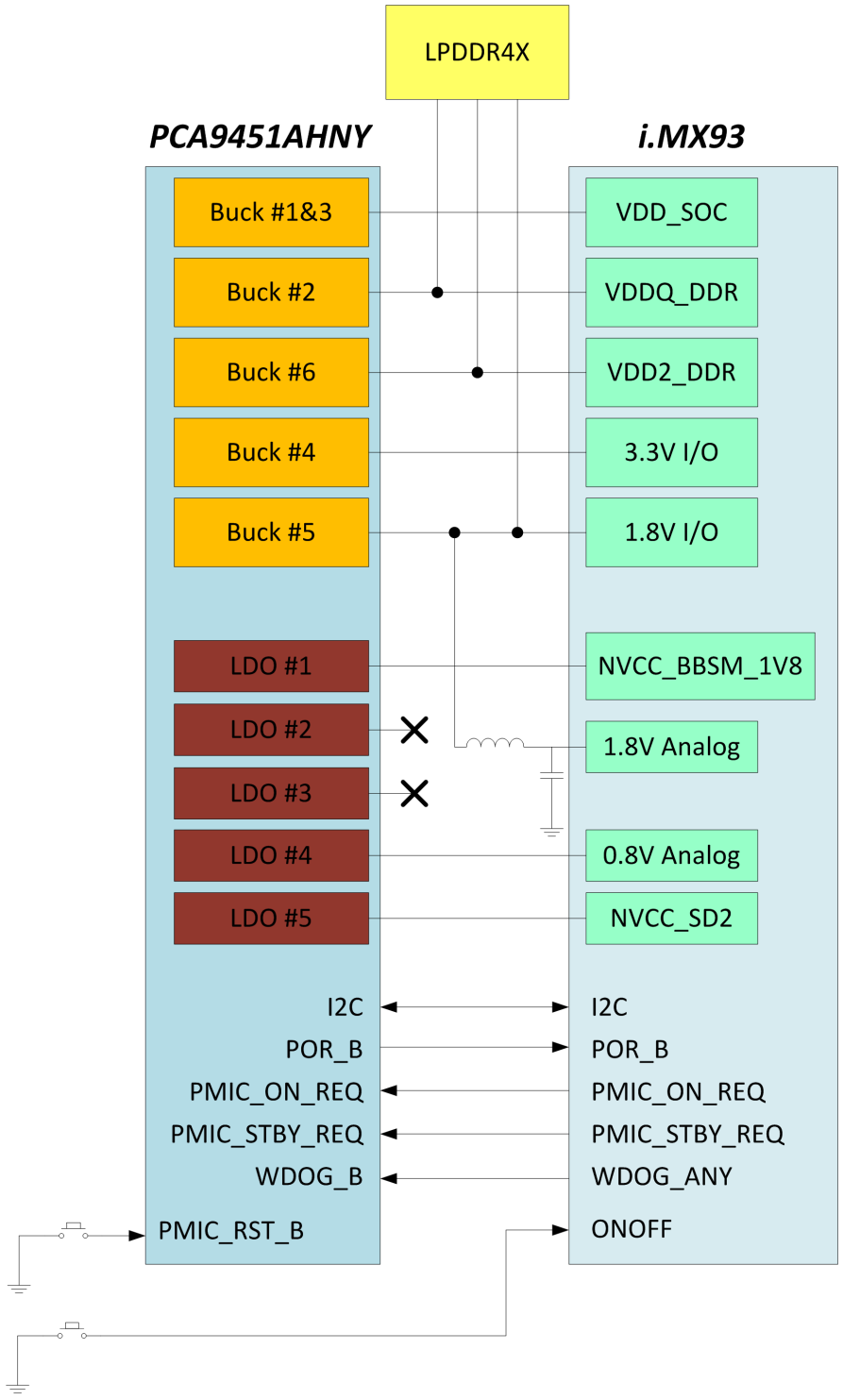

Figure 9. Power tree block diagram of i.MX 93 EVK board

3.11.2 Power routing/distribution requirements

The designing for a good Power Delivery Network (PDN) is complicated. It includes:

1. **Choose a good PCB stack-up**: Use adequate copper thickness, layer assignment, and layer utilization.

2. **Optimize the placement and routing of the PDN**: This includes good placement of the decoupling capacitors and connecting them to the power ground planes with as short and wide a trace as possible. This is recommended because the increased inductance of a longer etch degrades the effectiveness of the capacitor. Use the number/placement of capacitors on the NXP development platforms.
3. **Optimize DC IR drop**: This involves using very wide traces/plane fills to route high-current power nets and ensure an adequate number of vias on power net layer transitions. Neck down of fill areas should be minimized and current density minimized. The maximum DC IR drop on a board should be 2% (preferably 1%) of the voltage rail (that is, on a 1.1 V rail, the maximum voltage drop should be less than 0.022 V, preferably less than 0.011 V). See Table 24 for the DC IR drop requirement.
4. **AC impedance check – the target impedance at different frequencies should be below specified values.** See Table 25 for the impedance targets versus frequency for specified power rail for the i.MX 93 PCB design.

Table 24. i.MX 93 DC IR drop requirements

Supply input	Nominal voltage (V)	Max current (mA)	IR drop target	Corresponding power path resistance requirement (mΩ)
VDD_SOC	0.8/0.85/0.9	2700	<2%	< 6.7
VDD2_DDR	1.1	500	<2%	< 44
VDDQ_DDR	0.6	260	<2%	< 46

Table 25. i.MX 93 PDN target impedance

Supply Input	< 20 MHz (mΩ)	20 - 100 MHz (mΩ)
VDD_SOC	30	146
VDD2_DDR	36	165
VDDQ_DDR	62	275

3.12 USB connectivity

The i.MX 93 provides two complete USB2.0 interfaces and the following configurations (or any subset) are supported:

- **Dedicated host or device using Type-A connector or Type-B connector;**
- **Dual role using Type-C connector.**

To implement a USB Type-C interface (UFP, DFP, or DRP), external hardware must be added to manage the two configuration channel IOs (CC1 and CC2) as well as monitor the plug orientation and switch the single USB3 SS interface.

See the NXP development platform schematic for an example USB Type-C implementation.

3.13 Unused input/output terminations

3.13.1 i.MX 93 unused input/output guidance

For the i.MX 93, the I/Os and power rails of an unused function can be terminated to reduce overall board power. Table 26 lists connectivity examples for unused functions except MIPI and USB. The use case for MIPI and USB is a little more complex so the connection recommendations for these two are listed in Table 27 and Table 28 respectively.

Table 26. i.MX 93 unused function strapping recommendations

Function	Ball name	Recommendation if unused
LVDS	VDD_LVDS_1P8, LVDS_CLK_P/N, LVDS_Dx_P/N	Tie to ground through 10 KΩ resistors
Digital I/O supplies	NVCC_WAKEUP, NVCC_AON, NVCC_GPIO, NVCC_SD2	Tie to ground through 10 KΩ resistors if the entire bank is not used

Table 27. i.MX 93 MIPI strapping recommendations

Use case	Ball name	Recommendation
Only MIPI-CSI used	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	MIPI_DSI1_CLK_P/N, MIPI_DSI1_Dx_P/N	Floating
Only MPI-DSI used	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N	Floating
Neither MIPI-CSI nor DSI is used	VDD_MIPI_1P8, VDD_MIPI_0P8	Tie to ground
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N	Floating
	MIPI_DSI1_CLK_P/N, MIPI_DSI1_Dx_P/N	Floating
	MIPI_REXT	Tie to ground

Table 28. i.MX 93 USB strapping recommendations

Use case	Ball name	Recommendation
Only USB1 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB2_VBUS, USB2_D_P/N, USB2_ID, USB2_TXRTUNE	Floating
Only USB2 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P/N, USB1_ID, USB1_TXRTUNE	Floating
Neither USB1 nor USB2 is used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Tie to ground
	USB1_VBUS, USB1_D_P/N, USB1_ID, USB1_TXRTUNE	Floating
	USB2_VBUS, USB2_D_P/N, USB2_ID, USB2_TXRTUNE	Floating

4 Avoiding board bring-up problems

4.1 Introduction

This chapter describes how to avoid mistakes when bringing up a board for the first time. The recommendations below consist of basic techniques for detecting board issues and preventing/locating the three issues encountered: power, clocks, and reset.

4.2 Avoiding power pitfalls—current

Excessive current can damage the board. Use a current-limiting laboratory supply set to the expected main current draw (at most). Monitor the main supply current with an ammeter when powering up the board for the first time. You can use the supply's internal ammeter if there is. By monitoring the main supply current and controlling the current limit, any excessive current can be detected before permanent damage occurs.

Before the board test, you can connect the board power rails to the ground to verify that there are no short circuits. Then, you can power on the board. This step ensures that there is no damage to the board and/or components.

4.3 Avoiding power pitfalls—voltage

To avoid incorrect voltage rails, create a basic table called a voltage report prior to board bring up/testing. The table helps to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- **Board voltage sources**
- **Default power-up values for the board voltage sources**
- **Best location on the board to measure the voltage level of each supply**

Determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board. The drop causes inaccurate voltage values. The following guidelines help produce the best voltage measurements:

- **Measure closest to the load (in the case of the i.MX 93 processor).**
- **Make two measurements: the first after initial board power-up and the second while running a heavy use case that stresses the i.MX 93 processor.**

Ensure that the i.MX 93 power supply meets the DC electrical specifications as listed in the chip-specific data sheet. See Table 29 for a sample voltage report table.

Note: *This report table is for the i.MX 93 EVK board. Sample voltage reports for customer PCBs are different from this table. These depend on the Processor and Power Management IC (PMIC) used and the assignment of the PMIC power resources.*

Table 29. Sample voltage report table

Source	Net name	Expected (V)	Measured (V)	Measure point	Comment
PCA9451AHNY_BUCK2	LPD4/x_VDDQ_0V6	0.6	-	TP702	-
PCA9451AHNY_BUCK1/3	VDD_SOC_0V8	0.75/0.8/0.91	-	TP703	-
PCA9451AHNY_BUCK4	VDD_3V3	1.8	-	TP706	-
PCA9451AHNY_BUCK5	VDD_1V8	1.8	-	TP707	-
PCA9451AHNY_BUCK6	LPD4/x_VDD2_1V1	3.3	-	TP708	-

Table 29. Sample voltage report table*...continued*

PCA9451AHNY_LDO1	NVCC_BBSM_1V8	1.8	-	TP709	-
PCA9451AHNY_LDO4	VDD_ANA_0V8	0.8	-	TP712	-
PCA9451AHNY_LDO5	NVCC_SD	3.3/1.8	-	TP713	Can be either under SW control
MP8759GD	VSYS_5V	5.0	-	TP211	-
USB type-C connector	VBUS_IN	5.0	-	TP302	Main supply for board
Load switch from MP8759GD	VDD_5V	5.0	-	TP201	-
MP2147	VPCIe_3V3	3.3	-	TP920	-
TPS70933DBVR	VLDO_3V3	3.3	-	C412	-

1. The default output voltage of PCA9451AHNY_BUCK1 is 0.8 V. The software changes it to 0.7 V or 0.9 V depending on the drive mode.

4.4 Checking for clock pitfalls

Problems with the external clocks are another board bring-up issue. Ensure that all the clock sources run as expected.

The XTALI_24M/XTALO_24M and the RTC_XTALI/RTC_XTALO clocks are the main clock sources for 24 MHz and 32.768 kHz reference clocks. Although not required, the use of low jitter external oscillators to feed CLKIN_1/2 can be an advantage if low jitter or special frequency clock sources are required by modules driven by CLKIN_1/2. Refer to the CCM chapter in the i.MX 93 chip reference manual for details.

Use an active probe while checking crystal frequencies. This is recommended to avoid excessive loading. A passive probe might inhibit the 24 MHz oscillators from starting up. Use the following guidelines:

- **RTC_XTALI/RTC_XTALO** is running at 32.768 kHz.
- **XTALI_24M/XTALO_24M** is running at 24 MHz (used for the PLL reference).

4.5 Avoiding reset pitfalls

Follow these guidelines to ensure that you are booting correctly.

- **During initial power-on while asserting the POR_B reset signal, ensure that 24 MHz and 32.768 kHz clock is active before releasing POR_B.**
- **Follow the recommended power-up sequence specified in the i.MX 93 data sheet.**
- **Ensure the POR_B signal remains asserted (low) until all voltage rails associated with bootup are ON.**

The BOOT_MODE[3:0] balls and internal fuses control boot. For a more detailed description about the boot modes, see the system boot chapter in the chip reference manual.

4.6 Sample board bring-up checklist

The checklist incorporates the recommendations described in the previous sections. Blank cells should be filled in during the bring-up.

Table 30. Board bring-up checklist

S.No	Checklist item	Details	Owner	Findings and Status
Note: The items 1 to 5 must be completed serially.				
1	Perform a visual inspection	Check major components to make sure that no component has been misplaced or rotated before powering ON.		
2	Verify all i.MX 93 voltage rails	Confirm that the voltages match the datasheet's requirements. Be sure to check voltages as close to the i.MX 93 as possible (like on a bypass capacitor). This reveals any IR drops on the board that could cause issues later. Ideally, all the i.MX 93 voltage rails should be checked. See guidance below for important rails to check for the i.MX 93.		
		NVCC_BBSM_1V8, VDD_SOC, VDDQ_ DDR, VDD2_DDR are particularly important voltages, and must fall within the parameters provided in the i.MX 93 data sheet.		
3	Verify power-up sequence	Verify that Power On Reset (POR_B) is deasserted (at high) after all power rails have come up and are stable. See the i.MX 93 datasheet for details about power-up sequencing.		
4	Measure/probe input clocks (32.768 power-on reset, 24 MHz, others)	Without proper clocks, the i.MX 93 will not function correctly.		
5	Check JTAG connectivity	This is one of the most fundamental and basic access points to the i.MX 93 to allow the debug and execution of low level code, and probe/access processor memory.		
Note: The items 6 to 9 may be worked on in parallel with other bring-up tasks.				
6	Access internal RAM	Verify basic operation of the i.MX 93 in system. The on-chip internal RAM starts at address 0x0090 0000 and is 128 Kbytes in density. Perform a basic test by performing a write-read-verify operation to the internal RAM. No software initialization is required to access internal RAM.		
7	Verify CLKOUT1/2 outputs (measure and verify default clock frequencies for desired clock output options) if the board design supports the probing of clock output balls.	This ensures that the corresponding clock is working and that the PLLs are working. This step requires chip initialization, for example, via the JTAG debugger, to properly set up the IOMUX to output clocks to I/O balls and to set up the clock control module to output the desired clock. See the chip reference manual for more details.		
8	Measure boot mode frequencies. Set the boot configure switch for each boot mode and measure	This verifies the connectivity of signals between the i.MX 93 and boot device and that the boot mode signals are properly set. See the "System Boot" chapter in the chip		

Table 30. Board bring-up checklist*...continued*

S.No	Checklist item	Details	Owner	Findings and Status
	the following (depending on system availability): • NAND (probe CE to verify boot, measure RE frequency) • SPI-NOR (probe slave select and measure clock frequency) • MMC/SD (measure clock frequency)	reference manual for details for boot mode configurations.		
9	Run basic DDR initialization and test memory	1. Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. 2. Try writing a few words and verify if they can be read correctly. 3. If not, recheck the DDR initialization sequence and whether the DDR has been correctly soldered onto the board. Users should recheck the schematic to ensure that the DDR memory has been connected to the i.MX 93 correctly.		

5 Using BSDL for board-level testing

5.1 BSDL overview

The Boundary Scan Description Language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is contained within IEEE Std 1149.1.

5.2 How BSDL works

A BSDL file defines the internal scan chain, which is the serial linkage of the IO cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool does the following:

1. **It outputs a specific set of addresses and controls to the pins connected to the ROM.**
2. **It performs a read command and scans out the values of the ROM data pins.**
3. **It compares the values read with the known golden values.**

Based on this procedure, the tool determines whether the interface between the two parts is connected properly and does not contain shorts or opens.

5.3 Downloading the BSDL file

The BSDL file for each i.MX processor is stored at the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

5.4 Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. You can open the file with a text editor (such as Wordpad) to review how each pin functions. The BSDL file defines these functions:

Port Description Terms

- in = input only
- out = 3-state output (0, Z, 1)
- buffer = two-state output (0, 1)
- inout = bidirectional
- linkage = other (vdd, vss, analog)

The appearance of a 'linkage' in the file of a pin means that the pin cannot be used with a boundary scan. These are usually power pins or analog pins that cannot be defined by a digital logic state.

5.5 Boundary scan operation

To put i.MX93 into boundary scan mode, a certain sequence should be executed after powering up. Due to the special design of DRAM interface I/O pads in i.MX93, the sequence becomes much more complex if the user wants to enable boundary scan function on DRAM_* pins.

The sequence to be followed for boundary scan enablement on i.MX93, without and with DRAM_* pins are listed separately below. The BSDL file to be used is also different. Use `MX93_306FCCSP_11x11.bsdl` for boundary scan test with DRAM_* pins, otherwise use `MX93_306FCCSP_11x11_without_DRAM_pins.bsdl`.

It is strongly recommended that if boundary scan test on DRAM_* pins is not needed, just use the simple sequence ("**1**"):

1. **Sequence without boundary scan enablement on DRAM_* pins**:
   a. Execute a "ENABLE_TEST_CTRL" instruction, as listed in the BSDL file. This instruction carries a operand, which shall be 0xA here.
   b. Execute a "BYPASS" instruction. After these two steps are done, put the i.MX93 into boundary scan mode. Then, you can execute normal boundary instructions such as "SAMPLE" or "EXTEST". Note that DRAM_* pins cannot be sampled or toggled using this sequence.
2. **Sequence with boundary scan enablement on DRAM_* pins**:
   a. Write a series of data into corresponding addresses through JTAG interface. Note that the write operation must be executed strictly in the following sequence, and none of them can be skipped.
   address(0x44461080), data(0X20010001)
   address(0x44464004), data(0x00010105)
   address(0x44464004), data(0x00010104)
   address(0x44461020), data(0x00000010)
   address(0x44461020), data(0x00000000)
   address(0x44460010), data(0x00000040)
   address(0x44461020), data(0x00000000)
   address(0x44461020), data(0x00000004)
   address(0x44461020), data(0x00000000)
   address(0x444d0400), data(0x12345678)
   address(0x444d0410), data(0x76543210)
   b. Execute a ENABLE_TEST_CTRL instruction, as listed in the BSDL file. This instruction carries a operand, which shall be 0xC here.
   c. Execute a BYPASS instruction. After these three steps are done, the i.MX93 is put into boundary scan mode. Then, the user can execute normal boundary instructions such as SAMPLE or EXTEST.

Refer to the following references for further information:

- Refer to the "***JTAG Controller (JTAGC)***" chapter in the chip reference manual for the definitions of the JTAG interface operations.
- When trying to toggle IO logic states using EXTEST instruction, make sure that PMIC_ON_REQ is set to driving high and PMIC_STBY_REQ is set to driving low before executing EXTEST instruction. These two pins control system power and may cause system reset or power down if their logic states are not set correctly.

5.6 I/O pin power considerations

The boundary scan operation uses each of the available device pins to drive or read values within a given system. Therefore, the power supply pin for each specific module must be powered for the IO buffers to operate. This is straightforward for the digital pins within the system.

6 Thermal considerations

6.1 Introduction

This chapter introduces basic thermal considerations that need to be considered, while designing an i.MX 93 processor-based system. It also provides a few key design considerations to improve the thermal management of the final i.MX 93 processor-based system/product.

PCBs should be designed with the thermal requirements factored in early stages. In later stages, only remedial actions are possible. Factoring thermal management at the end of the design cycle would increase the cost of the overall design and delay productization.

The Thermal Design Power, (TDP), represents the maximum sustained power dissipated by the processor, across a set of realistic applications. The activity profile of the application can have a significant impact on the thermal management techniques used and on the TDP.

For customer applications that require high performance for extended periods, the usage of passive thermal management techniques is necessary. This is also required if the product is required to function in high ambient temperatures. In such cases, a heat sink can be used. For very high ambient operating environments, active thermal management techniques such a cooling fan or forced convection may also be required in addition to the heat sink.

For less demanding applications, it may be feasible to consider the PCB as one of the primary heat dissipation media if good design practices are followed. In such cases, NXP recommends passive heat sinks as a minimum to be mounted to the lid of the processor using thermal paste or appropriate Thermal Interface Materials (TIM).

6.2 PCB dimensions

The dimensions of the PCB directly affect its capability to dissipate the heat. Typically, more than 80% of the heat generated by a high-power component is dissipated through the system board, when no other thermal solution is implemented. The bigger the board is, the larger the surface area through which heat can spread away from the source component and also can be transferred more efficiently into free space.

An NXP-conducted PCB sensitivity simulation showed that a 50% reduction in PCB x-y dimensions results in an increase of between 44-65% in package thermal resistance due to the loss in conductive volume to dissipate heat. System designers therefore need to be careful while designing smaller form factor boards that have multiple high-power components.

6.3 Copper volume

Increasing the heat dissipation (reducing thermal resistance) can also be achieved by increasing the metallization in the system board. PCBs are made up of copper and dielectric material, with the copper being orders of magnitude more thermally conductive. Copper volume influences the heat capacity of the board. With higher copper volume, the board can accept more heat, so a i.MX 93 processor-based system can operate in high performance state (or near the max TDP) for longer time periods. The copper volume can be increased by increasing the dimensions of the board. This can be done by adding ground layers or increasing the thicknesses of the layers on which power and ground planes are located. Refer to Section 3.5.1 and Section 3.5.2 for stack-up information.

6.4 PCB material selection

As previously discussed, PCB material selection is extremely important for systems with high speed routing. Thermal properties should also be considered in selecting PCB materials for multilayer designs in which the system is expected to endure excessive short-term thermal steps. Specific attention should be paid to the fact that thermal properties of dielectrics are often different in horizontal and vertical directions.

Material characteristics such as the Coefficient of Thermal Expansion (CTE) should be considered. The CTE describes how a material changes dimension with temperature. Ideally, a PCB material's CTE should be closely matched to copper, which is about 17 ppm°C. CTE is a concern because as the PCB expands during heating, it can elongate plated via holes and cause fracturing.

If the CTE is closely matched to copper, expansion of the PCB material and copper will be more uniform and the plated via holes will be more robust during thermal cycling.

6.5 Thermal resistance

Reducing the thermal resistance close to the die and package is mandatory for good thermal performance. The actual semiconductor die dimensions are relatively small compared to the size of a typical PCB, which results in a very high heat flux in the die, package, and its immediate vicinity. Therefore, thermal resistance encountered early in the thermal path causes a large temperature gradient. The most effective place to focus resources to reduce thermal resistance is where the thermal gradient is the highest. To efficiently dissipate the heat through the board, thermal resistance between the SoC and the board needs to be minimized. This can be achieved by utilizing all the ground pads of the component and using board level underfill with good thermal conductivity properties.

6.5.1 Heat spreaders

Thermal resistance can be reduced when a heat spreader is mounted on the top of SoC package using a Thermal Interface Material (TIM) with good thermal conductivity properties (thermal paste). If the heat spreader is also thermally connected with the PCB, an alternative route for the heat is created, reducing the global thermal resistance. Spreading the heat at the beginning of the thermal path not only reduces the thermal resistance near the source component, but it also provides a broader area to further disseminate the heat.

The type of heat spreader to be used is dependent on the customers' application, available enclosure space, and budget considerations. Graphite heat spreaders are quite common as they match the thermal performance of copper in two directions (x, y), at a lower weight and cost. The high in-plane (basal) thermal conductivity results in spreading and evening out of the hot spots. Due to its low cost, the area that the graphite heat spreader covers, could be potentially larger, covering all heat generating components on the system board.

6.5.2 Thermal vias

Using a continuous low thermal impedance path from the processor to ambient conditions is important and a low thermal resistance has to be maintained throughout the PCB. Any small break in the low impedance path is highly detrimental. System designers should provide redundant thermal paths where possible. This can be achieved by adding an appropriate number of thermal vias to connect all the ground planes together and allow the heat to spread uniformly through other layers of the PCB. System designers should allocate enough **plated-through** vias around the ground and power balls of the i.MX 93 processor and other heat generating components.

6.6 Power net design

Modern power electronics devices can have very low on-resistances. It is quite possible that the PCB traces and connector pins that feed current to these devices contribute more ohmic losses to the system than the power transistors do. Such heating may be avoidable if traces are up-sized. Reducing trace ohmic losses may be the least expensive way to reduce the design's total power dissipation. Trace width calculators, which also predict trace temperature rise, are readily available on the Internet. Using over-sized power transistors is a way to cut total power and subsequent heat dissipation.

6.7 Component placement

The i.MX 93 processor should always be placed away from edges in the center of the PCB so that heat can effectively spread in all directions. Placing the device on the edge or even on the corner of the PCB significantly reduces heat transfer from the device and dissipation capabilities of the PCB, as the heat cannot efficiently spread in the directions where the edges are present. This eventually results in local hot spots and rapid heating of the source component.

In addition, the processor should be mounted on the top side of the PCB, away from the chassis side walls, unless the side walls are being used as thermal solution path for the package. System designers should place heat generating components as far apart as possible to reduce thermal coupling effects. The thermal gradient is high near a power dissipating device, so even small amounts of separation help reduce thermal coupling.

An NXP-conducted PCB sensitivity simulation showed that a non-centered bare i.MX 93 FCBGA package on the PCB causes approximately 8-10% increase in junction temperature due to uneven heat propagation. This study highlights the need for centered component placement.

6.8 PCB surroundings

The surroundings of the PCB also influence the efficiency of heat transfer from the board into free space (air). There should be enough clearance from the top and bottom sides of the PCB. If narrow gaps are created, air flow is significantly limited, resulting in accumulation of hot air in the gap. The board cannot therefore effectively transfer heat in such areas. Also, the casing should be designed in a way that natural air convection could be utilized to improve heat transfer.

If a narrow gap at the bottom side cannot be avoided (quite common for System on Modules - SOMs), it should be considered to fill the gap under the i.MX 93 processor by thermally conductive gap filler. To further improve heat transfer, exposed copper pads should be added to the base board at the mounting spot of the filler.

6.8.1 Air flow considerations

Heat convection is more efficient for a vertically mounted board. Remember that components above heat producing devices run hotter than those below. If the board is to be horizontally mounted, place heat generating components on the PCB’s topside, if possible. A thermal plume (the chimney effect) forms more readily on a board’s topside and it helps disperse heat.

- Consider the system level air flow and air mover placement in the enclosure.
- Avoid sub-optimal component placement that might hinder airflow or natural convection.
- Avoid placing tall or bulky devices in the air flow path.
- Avoid routing circuitry in an area where mounting holes would need to go.
- Plan to make space for the thermal management solution early in the system design phase. Consider the complete board and packaging form factor (enclosure).

6.9 Heat sink considerations

The most frequently employed passive cooling device is the heat sink. It is a mass of thermally conductive metal which is physically mounted to a heat generating component. Adding a heat sink to the processor is an excellent method to dissipate heat. Commonly used heat sink materials are copper and aluminum.

- Copper has better thermal conductivity but is more expensive and difficult to process. It is heavier, has small heat capacity, and easily oxidizes. Lots of copper radiators might exceed the CPU weight limit.
- For most applications, an aluminum alloy heat sink is sufficient.

There are various parameters that affect not only the heat sink performance itself, but also the overall performance of the system. Choosing the correct type of heat sink depends largely on the thermal budget allowed for the heat sink and external conditions surrounding the heat sink.

A few design considerations when planning to add a heat sink in your design are listed below:

- Ensure adequate spacing around the device to accommodate the heat sink.
- Avoid routing circuitry in the area where mounting holes will be placed
  - Space is needed for anchoring the heat sink such as spring loaded screws, a clip, or push pins.
- Consider also the bottom side of the PCB where space for reinforcing support or securing mechanisms may be required.
  - A backing plate may be necessary on the back side of the printed circuit board opposite the flip-chip device to prevent board warpage.
- Consider temperature limits beneath the heat sink and ensure that temperature-sensitive components are not placed there to prevent overheating and damage.
- Ensure the orientation and spacing of the fins cause the heat to move as quickly as possible from the heat source (refer to Air Flow Considerations).
  - Improper orientation can inhibit the thermal performance of the heat sink. For more details on heat sink handling, refer to AN4871.

6.10 Thermal simulations

Thermal management is a very complex discipline with numerous variables that need to be considered. Thermal simulations should be performed in order to determine whether a system is capable of stable operation (to ensure no thermal runaways) for a given use case and to identify potentially overlooked issues.

NXP provides FloTHERM or Icepak simulation models for i.MX 93 processor series processor family. NXP strongly encourages customers to perform thermal simulations using these models in their form factor designs. It also recommends to perform specific use cases to get a holistic system thermal design and identify possible thermal bottlenecks. Thermal simulations become increasingly important in small form factor designs and operation in high ambient temperatures.

6.11 Software optimizations

Software based power and thermal management techniques can be very effective in reducing the need for more elaborate active or passive thermal management solutions and add little or no additional cost to the system design. Attention should be paid to the required system performance and power requirements, as lower the i.MX 93 processor power consumption lower the heat generated by the processor.

The i.MX 93 incorporates several low-power design techniques, to meet requirements of low-power design, while sustaining high performance operation. The activity profile of the customer application can have a significant impact on the thermal management techniques used and on the TDP. Carefully defining the system's worst case operating conditions can be an effective way to reduce power and thermal dissipation.

- System designers should utilize and enable all software power management techniques available for the i.MX 93.
- The SoC voltages and core frequencies of modules should be kept at the minimum specified levels and scaled dynamically with respect to the current performance demands of the application where possible.
- The processor should enter low-power modes under certain use cases whenever possible.
- All unused power rails should be turned off from the PMIC and power gate unused domains if possible.
- All unused module clocks should be turned off (Dynamically handled by NXP Linux BSP).
- Customers are encouraged to use the latest Linux BSP GA release available on nxp.com, which leverages the i.MX 93 processor power management features and incorporates various Linux software power management techniques.

For more details on the power consumption, refer to AN13054.

6.12 Thermal checklist

NXP recommends using the checklist below as a high-level guide for designing an optimal thermal management solution for your end product.

Table 31. Thermal checklist

Item	Activity	Check
1	Determine the Thermal Design Power (TDP)	
2	Determine the Activity Profile (use case dependent)	
3	Determine the product form factor constraints (orientation, x, y, and z limits, and so on)	
4	Determine the environmental operating conditions (ambient temperature, airflow regime - Forced or Natural Convection)	
5	Determine the junction temperature (Tj) for the i.MX 93 device to use (Industrial, consumer, and so on)	
6	Factor in board design considerations early (PCB layers, metallization, layout, component placement)	
7	Run thermal simulations to determine the best thermal management approach using form factor design and use cases	
8	Investigate adding heat spreading techniques, heat sinks to alleviate thermal bottlenecks	
9	Enable all software power management techniques which can minimize power consumption (less power, less heat)	
10	Consider lower power memory and other system components, or re-target use case. NXP highly recommends the use of LPDDR4X memories to lower power consumption.	

7 Revision history

The table below lists the revisions made to this document.

Table 32. Revision history

Revision number	Date	Substantive changes
1	13 April 2023	• Updated information for i.MX93 QSB board and 9x9 and 14x14 packages • Other updates
0	17 June 2022	Initial release

8 Legal information

8.1 Definitions

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