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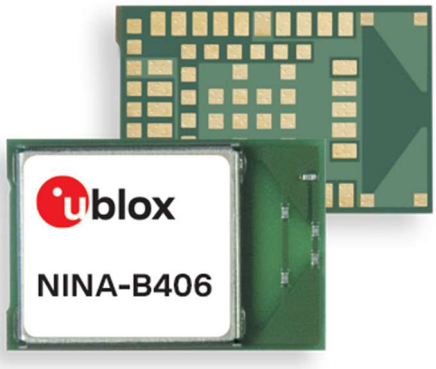
NINA-B40 series

Stand-alone Bluetooth 5.1 low energy modules

Data sheet



Abstract

This technical data sheet describes the stand-alone NINA-B40 series Bluetooth® 5.1 Low Energy modules. The NINA-B4 family includes two sub-series – the NINA-B40 and NINA-B41 series. The NINA-B40 series provides an open CPU architecture with a powerful MCU for customer applications, while the NINA-B41 series are delivered with pre-flashed u-connectXpress software.

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Product status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Initial Production	Early Production Information	Data from product verification. Revised and supplementary data may be published later.
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This document applies to the following products:

Product name	Type number	Software	Hardware version	PCN reference	Product status
NINA-B400	NINA-B400-00B-00	Open CPU	03	N/A	Initial Production
NINA-B406	NINA-B406-00B-00	Open CPU	04	N/A	Initial Production

Contents

1 Functional description

1.1 Overview

The NINA-B40 series comprises small, stand-alone Bluetooth 5.1 Low Energy wireless modules that are particularly suited for harsh professional environments.

Based on the Nordic Semiconductor nRF52833 chip that includes an integrated RF core and powerful Arm® Cortex®-M4 with FPU processor, NINA-B40 modules operate in all Bluetooth 5.1 modes – as well as 802.15.4 (Thread and Zigbee) and Nordic proprietary modes.

Featuring Angle of Arrival (AoA) and Angel of Departure (AoD) transceivers, the NINA-B40 series supports the Bluetooth 5.1 Direction Finding service. The service can be used for indoor positioning, wayfinding, and the tracking of assets.

NINA-B40 modules need only a single supply voltage in the range of 1.7 – 3.6 V and, as the supply voltage level can also be used as the I/O reference level, can be easily integrated into simple, single voltage rail systems. The broad supply voltage range makes the modules particularly useful in battery powered systems.

With the same pinout, physical size and mechanical design of NINA-B3 modules, NINA-B40 offers a natural upgrade path for existing NINA-B3 applications. See also NINA-B3 Data sheet [6] and NINA-B40 Product summary [5].

Table 1 describes the different models in the NINA-B40 series.

Model	Description
NINA-B400	Bluetooth 5.1 module that includes a powerful Arm® Cortex®-M4 with FPU, and delivers state-of-the-art power performance. All NINA-B40 variants are open CPU modules that enable customer applications to run on the built-in Arm® Cortex®-M4 with FPU. With 512 kB flash and 128 kB RAM, these modules offer sufficient capacity for customer applications on top of the Bluetooth Low Energy stack. NINA-B400 has a U.FL connector for use with an external antenna.
NINA-B406	Bluetooth 5.1 module that includes a powerful Arm® Cortex®-M4 with FPU, and delivers state-of-the-art power performance. All NINA-B40 variants are open CPU modules that enable customer applications to run on the built-in Arm® Cortex®-M4 with FPU. With 512 kB flash and 128 kB RAM, these modules offer sufficient capacity for customer applications on top of the Bluetooth Low Energy stack. NINA-B406 has an internal PCB trace antenna integrated in the module PCB. The internal antennas have an extensive range and are specifically designed for embedded devices.

Table 1: NINA-B40 series

☞ Already globally certified for use with an internal antenna or range of external antennas, the time, cost, and effort spent on deploying NINA-B4 modules into customer applications is reduced significantly.

1.2 Applications

- Industrial automation
- Smart buildings and cities
- Low power sensors
- Wireless-connected and configurable equipment
- Point-of-sales
- Health devices
- Real-time Location, RTLS
- Indoor positioning
- Asset tracking

1.3 Product description

Item	NINA-B400	NINA-B406
Bluetooth version	5.1	5.1
Band support	2.4 GHz, 40 channels	2.4 GHz, 40 channels
Typical conducted output power	+8 dBm	-
Radiated output power (EIRP)	+11 dBm (with typical antenna)	+11 dBm
RX sensitivity (conducted)	-95 dBm	-95 dBm
RX sensitivity, long range mode (conducted)	-102 dBm	-102 dBm
Supported 2.4 GHz radio modes	Bluetooth Low Energy IEEE 802.15.4 Proprietary 2.4 GHz modes	Bluetooth Low Energy IEEE 802.15.4 Proprietary 2.4 GHz modes
Supported Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps 125 kbps	1 Mbps 2 Mbps 500 kbps 125 kbps
Module size	10.0 x 15.0mm	10.0 x 15.0 mm

Table 2: NINA-B40 series characteristics summary

1.4 Ordering information

Ordering Code	Product
NINA-B400-00B	NINA-B40 module with antenna connector U.FL, open CPU for custom applications
NINA-B406-00B	NINA-B40 module with internal PCB trace antenna, open CPU for custom applications

Table 3: Product ordering codes

1.5 Hardware options

Except for the different antenna solutions, NINA-B40 series modules use an identical hardware configuration. The integrated DC/DC converter is available for higher efficiency under heavy load situations. See also section 2.1.1.

1.6 Software options

NINA-B40 modules are integrated with an Arm® Cortex®-M4 application processor with FPU, 512 kB flash memory and 128 kB RAM.

The structure of any software running on the module includes the following components:

- Radio stack
- Bootloader (optional)
- Application

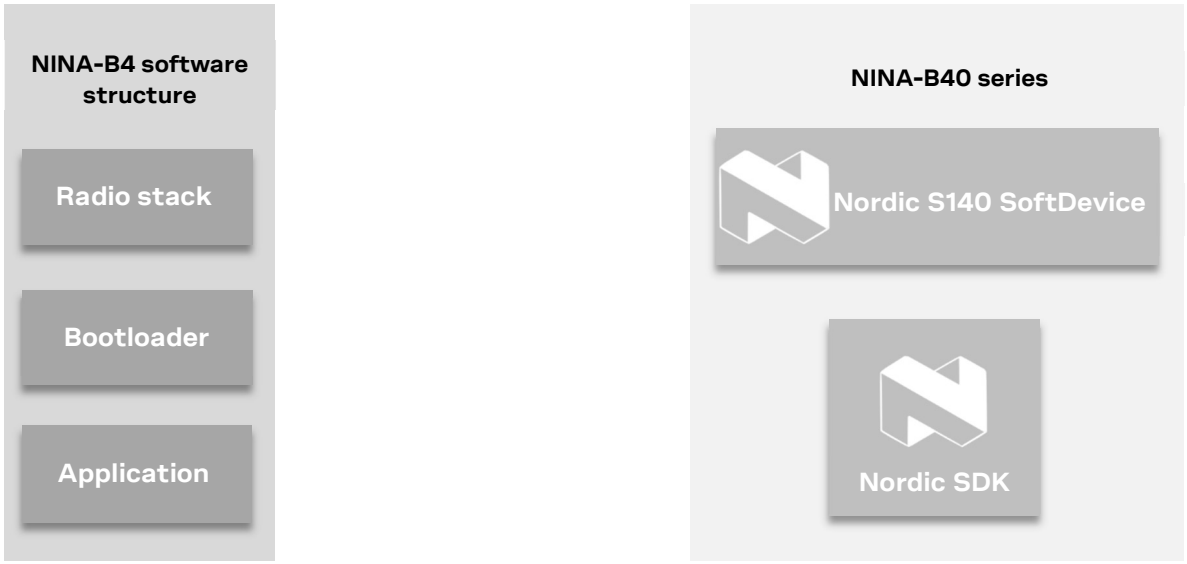


Figure 1: NINA-B40 software structure and available software options

1.6.1 Open CPU

The open CPU architecture of NINA-B40 series modules allows module integrators to build their own applications. u-blox recommends Nordic software to speed up the development process.

Nordic Semiconductor software provides a rich and well-tested software development environment for nRF52 based devices. It includes a broad selection of drivers, libraries, and example applications. It also includes other radio stacks.

1.7 Bluetooth device address

You can scan the data matrix barcode on the module label to retrieve the Bluetooth device address. See also section 0.

2 Interfaces

2.1 Power management

2.1.1 Module supply input (VCC)

NINA-B40 series modules use integrated step-down converters to transform the supply voltage presented at the **VCC** pin into a stable system voltage. Consequently, the modules are compatible for use in battery powered designs – without the need of an additional voltage converter.

The modules support two on-board converters:

- Low dropout (LDO)
- DC/DC buck

The module automatically switches between these converters to suit the prevailing current consumption. The DC/DC converter is more efficient under high loads when the radio is active, while the LDO converter is better suited for power saving modes.

2.1.2 Digital I/O interfaces reference voltage (VCC_IO)

All modules in the NINA series generally provide an additional voltage supply input for setting the I/O voltage level. In NINA-B40 series modules, the I/O voltage level is similar to the supply voltage and **VCC_IO** is internally connected to the supply input. Therefore, only a single supply voltage is needed for NINA-B40, which makes it ideal for battery powered designs.

☞ The supply arrangements can vary in other modules in the NINA series. A design that that is pin compatible with other NINA-series modules should keep the **VCC** and **VCC_IO** supply rails separate.

2.2 RF antenna interfaces

2.2.1 2.4 GHz radio (ANT)

NINA-B40 model versions have their own 2.4 GHz antenna solutions:

- NINA-B400 modules use an U.FL connector solution for external antenna. The **ANT** pin is internally disconnected on these models.
- NINA-B406 modules use an internal PCB trace antenna integrated into the module PCB. This low-profile antenna solution is useful in space constrained designs. The **ANT** pin is internally disconnected on these models. This solution uses antenna technology licensed from Proant AB.

☞ See the NINA-B4 System integration manual [3] for Antenna reference designs and integration instructions.

2.2.2 Near Field Communication (NFC)

NINA-B40 series modules include a Near Field Communication interface that can operate as a 13.56 MHz NFC tag that operates at a bit rate of 106 kbps.

As an NFC tag, data can be read from or written to the NINA-B40 modules using an NFC reader. NINA-B40 modules are not capable of reading other tags or initiating NFC communications.

The NFC interface can be used to wake the module from sleep mode, which means that the module can be kept in the deepest power save mode and still wake up properly to react to an NFC field.

Two pins are available for connecting to an external NFC antenna: **NFC1** and **NFC2**.

2.2.3 Direction Finding (AoA/AoD)

NINA-B40 modules support a location Bluetooth 5.1 service called Bluetooth Direction Finding. This service is used for indoor positioning, wayfinding, and tracking assets.

These phase-based functions require an antenna array, estimation algorithms and processing power to make it possible to triangulate and detect the direction of a Bluetooth signal down to a sub-meter accuracy. These functions are available for 1 Mbps and 2 Mbps Bluetooth LE modes.

The Angle of Arrival (AoA) receiver and Angel of Departure (AoD) transmitter use the antenna arrays that are switched on one by one. This switching sequence allows the direction of a peer device to be calculated. The derived IQ samples are used to determine the relative path lengths between the antenna pairs and subsequent location of the transmitter.

2.3 System functions

2.3.1 Power modes

NINA-B40 series modules use power-efficient LDO and DC/DC regulators and can operate in different power modes and configurations. Consequently, specific parts of the module can be powered off when they are not needed and complex wake-up events can be generated from different external and internal inputs.

2.3.1.1 System OFF mode

System OFF mode is the deepest power saving mode. It is in this mode that NINA-B40 modules sleep, so that all functionality is stopped to ensure minimum power consumption.

An external event is required to wake up the module from sleep in the system OFF mode. Although the module always reboots after waking up from the system OFF mode, some non-volatile registers in RAM can be configured so that they remain intact during and after going to the system OFF mode.

You can switch on or reboot NINA-B40 modules in any of the following ways:

- Rising edge of the VCC pin connected to a valid supply voltage
- Module reset, as described in section 2.3.2.
- Programmable digital or analog sensor event. In response to a rising voltage level flag from an analog comparator pin, or similar.
- NFC field detection
- 5 V supply to the **VBUS** pin (USB interface plug in)

2.3.1.2 System ON mode

When powered on or reset, NINA-B40 modules return to the default configuration set by the application software flashed in the module. In System ON mode all functional blocks and system peripherals are available in either RUN mode or in IDLE mode. The software configuration and the application under execution determines the mode of operation.

System ON mode has two optional sub-power modes, Constant Latency and Low-Power, as described in sections 0 and 2.3.1.2.2 respectively. Designers can choose which sub-power mode is most appropriate for the application, but only one can be enabled at any given time. These modes are active when the CPU or other peripherals are idling.

2.3.1.2.1 Constant latency

You can configure the CPU and other programmable peripherals to use minimal resources. The module can be turned on from sleep (System OFF mode) with constant and predictable CPU wakeup latency, but not without introducing some degradation in the power efficiency.

2.3.1.2.2 Low-Power

The module draws least power in the (default) Low-power mode of NINA-B40 modules. The automatic power management system in the Nordic chip limits the minimum power consumption. The module is turned on from sleep with varying CPU wakeup latency and peripherals tasks.

2.3.2 Module reset

NINA-B40 modules are reset by a low level on the **RESET_N** input pin, which is normally kept high using an internal pull-up. The low-level state causes an “external” or “hardware” reset of the module.

2.3.3 CPU and memory

The Nordic Semiconductor nRF52833 chip in the NINA-B40 series modules includes a powerful Arm® Cortex®-M4 with FPU processor. The processor works with a superset of 16 and 32-bit instructions (Thumb-2) at 64 MHz clock speed. It can use up to 37 interrupt vectors and 3 priority bits.

The nRF52833 chip has 512 kB of flash and 128 KB of RAM for code and data storage.

2.3.4 Direct Memory Access

All interfaces described in this data sheet support Direct Memory Access (DMA) to move any data generated from the interface directly into the RAM, without involving the CPU. This ensures fluent operation of the CPU with minimal need for interruption. To reduce the overall power consumption, DMA should be used as often as possible.

2.3.5 Programmable Peripheral Interconnect

The Nordic Semiconductor nRF52833 chip in the NINA-B40 series modules includes a programmable peripheral interconnect (PPI) switch matrix that connects various control signals between different interfaces and system functions. The switch allows most interfaces to bypass the CPU when triggering a system function. In this way, an incoming data packet can trigger a counter on the falling voltage level on an ADC or toggle a GPIO – without having to send an interrupt to the CPU. This functionality facilitates the development of smart, power-efficient applications that wake up the CPU only when it is necessary.

2.3.6 Real Time Counter (RTC)

A key system feature of the module is the Real Time Counter (RTC). This counter can generate and send multiple interrupts and events to the internal and external hardware blocks, CPU and radio. The events can be precisely timed and range from microseconds up to hours and leveraged for periodic Bluetooth LE advertising and other applications – without involving the CPU. The RTC can be operated in the active and standby modes.

2.4 Low Frequency Clock (LFXO)

NINA-B40 modules require two clocks, a high frequency clock and a low frequency clock.

- The high frequency clock is provided on-module by a high-accuracy 32 MHz crystal as required by the radio operation.
- The low frequency clock can be provided internally by an RC oscillator or synthesized from the fast clock, or externally by a 32.768 kHz crystal. An external crystal provides the lowest power consumption and greatest accuracy. Using the internal RC oscillator with calibration provides acceptable performance for Bluetooth low energy applications at a reduced cost and slight increase in power consumption.

For information about the LFXO operating parameters and performance of the clock, see Electrical specifications, Table 13.

☞ When using an external crystal with NINA modules at operating temperatures above 85 °C, certain limitations apply. For further information, see the Nordic nRF52833 specification for extended operating temperature. For Normal operating temperature range LXFO debounce time is 0.25s. For extended temperature range LXFO debounce time is 0.50s.

2.5 Serial interfaces

NINA-B40 modules provide the following serial communication interfaces:

- 2x UART interfaces: 4-wire universal asynchronous receiver/transmitter
- 4x SPI interfaces: Up to four serial peripheral interfaces can be used simultaneously
- 2x I2C interfaces: Inter-Integrated Circuit (I2C) interface for communication with digital sensors
- 1x I2S interface: Used to communicate with external audio devices
- 1x USB 2.0 device interface: The USB device interface to connect to the upstream host.

☞ Most digital interface pins on the module are shared between the digital, analog interfaces and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

☞ Two of the SPI interfaces share common hardware with the I2C interfaces. These interfaces cannot be used simultaneously. If both the I2C interfaces are in use only one SPI interface is available.

2.5.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control and baud rates up to 1 Mbps. Other characteristics of the UART interface are listed below:

- Pin configuration:
  - TXD, data output pin
  - RXD, data input pin
  - RTS, Request To Send, flow control output pin (optional)
  - CTS, Clear To Send, flow control input pin (optional)
- Hardware flow control or no flow control is supported.
- Power saving indication available on the hardware flow control output (**RTS** pin): The line is driven to the OFF state when the module is not ready to accept data signals.
- Programmable baud rate generator allows most industry standard rates, as well as non-standard rates up to 1 Mbps.
- Frame format configuration:
  - 8 data bits
  - Even or no-parity bit

- 1 stop bit
- Default frame configuration is 8N1, meaning eight (8) data bits, no (N) parity bit, and one (1) stop bit.
- Frames are transmitted in such a way that the least significant bit (LSB) is transmitted first.

2.5.2 Serial peripheral interface (SPI)

NINA-B40 supports up to four Serial Peripheral Interfaces with serial clock frequencies of up to 32 MHz. Characteristics of the SPI interfaces are listed below:

- Pin configuration in master mode:
  - **SCLK**, Serial clock output, up to 32 MHz
  - **MOSI**, Master Output Slave Input data line
  - **MISO**, Master Input Slave Output data line
  - **CS**, Chip/Slave select output, active low, selects which slave on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin.
  - **DCX**, Data/Command signal, this signal is optional but is sometimes used by the SPI slaves to distinguish between SPI commands and data
- Pin configuration in slave mode:
  - **SCLK**, Serial clock input
  - **MOSI**, Master Output Slave Input data line
  - MISO, Master Input Slave Output data line
  - **CS**, Chip/Slave select input, active low, connects/disconnects the slave interface from the bus.
- Both master and slave modes are supported on all the interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

2.5.3 Inter-Integrated Circuit interface (I2C)

The Inter-Integrated Circuit (I2C) interfaces can be used to transfer and/or receive data on a 2-wire bus network. The NINA-B40 modules can operate as both master and slave on the I2C bus using standard (100 kbps), fast (400 kbps), and 250 kbps transmission speeds. The interface supports clock stretching, which allows NINA-B40 to temporarily pause any I2C communications. Up to 127 individually addressable I2C devices can be connected to the same two signals.

- Pin configuration:
  - **SCL**, clock output in master mode, input in slave mode
  - **SDA**, data input/output pin

This interface requires external pull-up resistors to work properly in the master mode; see section 4.2.9 for suggested resistor values. The pull-up resistors are also required in slave mode and these should be placed at the master end of the interface.

2.5.4 Inter-IC Sound interface (I2S)

The Inter-IC Sound (I2S) interface can be used to transfer audio sample streams between NINA-B40 and external audio devices such as codecs, DACs, and ADCs. It supports original I2S and left or right-aligned interface formats in both master and slave modes.

- Pin configuration:
  - **MCK**, master clock
  - **LRCK**, left right/word/sample clock
  - **SCK**, serial clock
  - **SDIN**, serial data in
  - **SDOUT**, serial data out

The master side of an I2S interface always provides the **LRCK** and **SCK** clock signals, but some master devices cannot generate a **MCK** clock signal. NINA-B40 can supply a **MCK** clock signal in both master and slave modes to provide to those external systems that cannot generate their own clock signal. The two data signals - **SDIN** and **SDOUT** allow for simultaneous bi-directional audio streaming. The interface supports 8, 16, and 24-bit sample widths with up to 48 kHz sample rate.

2.5.5 USB 2.0 interface

The NINA-B40 series modules include a full speed Universal Serial Bus (USB) device interface which is compliant to version 2.0 of the USB specification. Characteristics of the USB interface include:

- Full speed device, up to 12 Mbit/s transfer speed
- MAC and PHY implemented in the hardware
- Pin configuration:
  - **VBUS**, 5 V supply input, required to use the interface
  - **USB_DP**, **USB_DM**, differential data pair
- Automatic or software-controlled pull up of the **USB_DP** pin

The USB interface has a dedicated power supply that requires a 5 V supply voltage to be applied to the **VBUS** pin. This allows the USB interface to be used even though the rest of the module might be battery powered or supplied by a 1.8 V supply etc.

2.6 Digital interfaces

2.6.1 Pulse Width Modulation (PWM)

NINA-B40 modules provide up to 16 independent PWM channels that can be used to generate complex waveforms. The waveforms can be used to control motors, dim LEDs, or as audio signals if connected to the speakers. Duty-cycle sequences may be stored in the RAM to be chained and looped into complex sequences without CPU intervention. Each channel uses a single GPIO pin as output.

2.6.2 Pulse Density Modulation (PDM)

The pulse density modulation interface is used to read signals from external audio frontends like digital microphones. It supports single or dual-channel (left and right) data input over a single GPIO pin. It supports up to 16 kHz sample rate and 16 bit samples. The interface uses the DMA to automatically move the sample data into RAM without CPU intervention. The interface uses two signals - **CLK** to output the sample clock and **DIN** to read the sample data.

2.6.3 Quadrature Decoder (QDEC)

The quadrature decoder is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs - **PHASE_A** and **PHASE_B**, and an optional **LED** output signal. The interface has a selectable sample period ranging from 128 µs to 131 ms.

2.7 Analog interfaces

10 out of the 40 digital GPIOs can be multiplexed to analog functions. The following analog functions are available:

- 1x 8-channel ADC
- 1x Analog comparator*
- 1x Low-power analog comparator*

*Only one comparator can be used at any given point in time.

2.7.1 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is used to sample analog voltage on the analog function enabled pins of the NINA-B40. Any of the 8 analog inputs can be used. Characteristics of the ADC include:

- Full swing input range of 0 V to **VCC**.
- 8/10/12-bit resolution
- 14-bit resolution while using oversampling
- Up to 200 kHz sample rate
- Single shot or continuous sampling
- Two operation modes: Single-ended or Differential
- Single-ended mode:
  - A single input pin is used
- Differential mode:
  - Two inputs are used and the voltage level difference between them is sampled

If the sampled signal level is much lower than the **VCC**, it is possible to lower the input range of the ADC to better encompass the wanted signal and achieve higher resolution. Continuous sampling can be configured to sample at a configurable time interval, or at different internal or external events, without CPU involvement.

2.7.2 Comparator

The analog comparator compares the analog voltage on one of the analog enabled pins in NINA-B40 with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross. Further characteristics of the comparator include:

- Full swing input range of 0 V to VCC
- Two operation modes: Single-ended or Differential
- Single-ended mode: A single reference level or an upper and lower hysteresis selectable from a 64-level reference ladder with a range from 0 V to VREF (described in Table 4)
- Differential mode: Two analog pin voltage levels are compared, optionally with a 50 mV hysteresis
- Three selectable performance modes - High speed, balanced, or power save

See section 4.2.10 for a comparison of the various analog comparator options.

2.7.3 Low power comparator

In addition to the power save mode available for the comparator, there is a separate low power comparator available on the NINA-B40 module. This allows for even lower power operation, at a slightly lower performance and with less configuration options. Characteristics of the low power comparator include:

- Full swing input range of 0 to **VCC**
- Two operation modes - Single-ended or Differential
- Single-ended mode:
  - The reference voltage **LP_VIN** is selected from a 15-level reference ladder
- Differential mode:
  - **GPIO_16** or **GPIO_18** is used as reference voltage
  - **LP_VIN** can be used to wake the system from sleep (system OFF mode)

Table 4 shows summary of the analog pin options. For information about the electrical specifications of the different analog comparator options, see section 4.2.10 .

Since the run current of the low power comparator is very low, it can be used as an analog trigger to wake up the CPU when the module sleeps in the System OFF mode. See section 2.3.1 for additional information.

2.7.4 Analog pin options

Table 4 shows the supported connections of the analog functions.

☞ An analog pin may not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	Any analog pin or VCC
ADCN	ADC differential negative input	Any analog pin or VCC
VIN+	Comparator input	Any analog pin
VREF	Comparator single-ended mode reference ladder input	Any analog pin, VCC, 1.2 V, 1.8V or 2.4V
VIN-	Comparator differential mode negative input	Any analog pin
LP_VIN+	Low-power comparator IN+	Any analog pin
LP_VIN-	Low-power comparator IN-	GPIO_16 or GPIO_18, 1/16 to 15/16 VCC in steps of 1/16 VCC

Table 4: Possible uses of the analog pins

2.8 GPIO

NINA-B40 series modules have a versatile pin-out. With no dedicated analog or digital interfaces, all module interfaces and functions must be allocated to a specific GPIO pin.

NINA-B40 modules have 40 GPIO pins. 10 of these are analog-enabled pins can be assigned to an analog function.

In addition to the serial interfaces, describes the digital and analog functions that can be assigned to a GPIO pin. Two of the GPIOs are optional NFC and two GPIOs optional for external an LFCLK crystal, namely XL1 and XL2.

Function	Description	Default NINA pin	Configurable GPIOs
General purpose input	**Digital input with configurable pull-up, pull-down, edge detection and interrupt generation**		**Any**
General purpose output	**Digital output with configurable drive strength, push-pull, open-collector, or open-emitter output**		**Any**
Pin disabled	**Pin is disconnected from the input and output buffers**	**All***	**Any**
Timer/ counter	**High precision time measurement between two pulses/ Pulse counting with interrupt/event generation**		**Any**
Interrupt/ Event trigger	**Interrupt/event trigger to the software application/ Wake up event**		**Any**
HIGH/LOW/Toggle on event	**Programmable digital level triggered by internal or external events without CPU involvement**		**Any**
ADC input	**8/10/12/14-bit analog to digital converter**		**Any analog**
Analog comparator input	**Compare two voltages, capable of generating wake-up events and interrupts**		**Any analog**
PWM output	**Output simple or complex pulse width modulation waveforms**		**Any**

Table 5: GPIO custom functions configuration

2.8.1 Drive strength

All GPIO pins are normally configured for lfow current consumption. Using this standard low-drive strength, any pin configured as an output can only source or sink a certain amount of current. If the timing requirements of any digital interface cannot be met, or if an LED requires more current than is available in this mode, a high drive strength mode is available so the digital output can draw more current. See section 4.2.8.

☞ Some GPIOs can introduce noise in the system when they are configured for high drive strength or connected to a signal with a switching speed higher than 10 kHz. See the pinout in section 3.1 for more information.

2.9 Debug interfaces

2.9.1 SWD

NINA-B40 series modules provide a Serial Wire Debug (SWD) interface for flashing and debugging. The SWD interface consists of two pins, **SWDCLK** and **SWDIO**.

2.9.2 Trace – Serial Wire Output

A serial trace option is available on the NINA-B40 series modules as an additional pin, **SWO**. The Serial Wire Output (SWO) is used to:

- Support printf style debugging
- Trace OS and application events
- Emit diagnostic system information

A debugger that supports Serial Wire Viewer (SWV) is required.

2.9.3 Parallel Trace

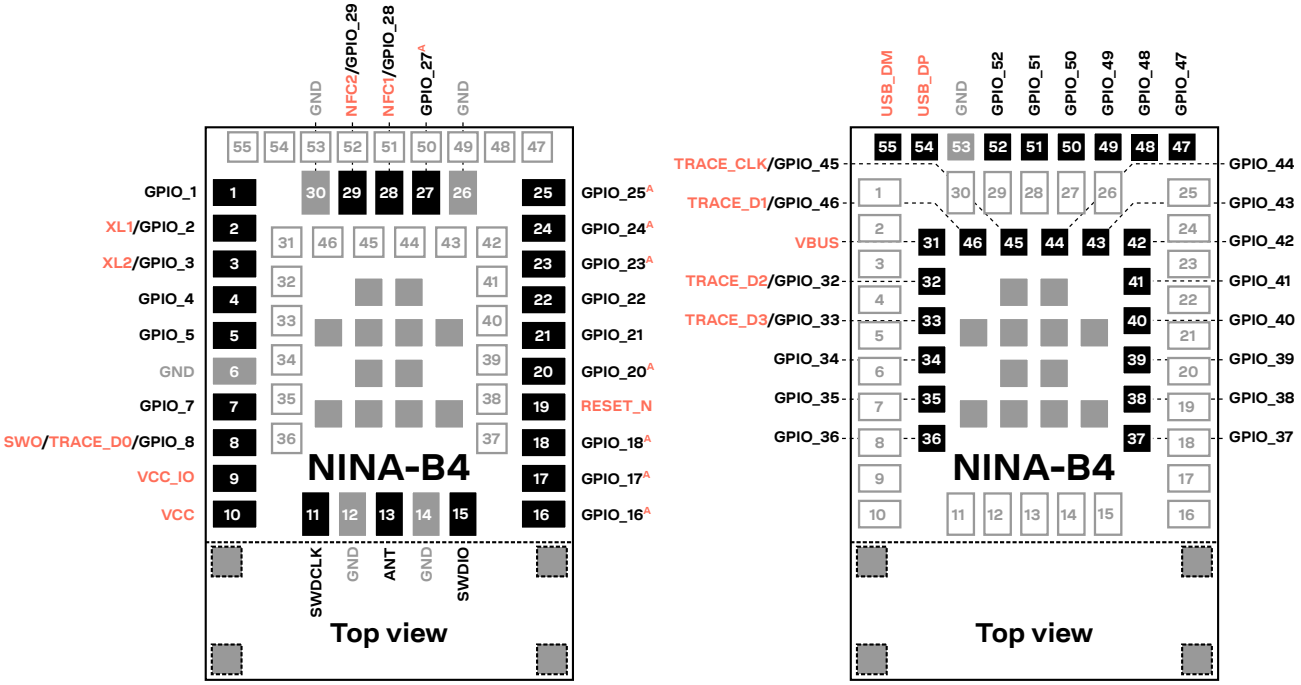
The NINA-B40 series modules support parallel trace output as well. This allows output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) resources in the Arm® Cortex®-M4 core of the nRF52833 chip in the NINA-B40. The ETM trace data allows a user to record exactly how the application goes through the CPU instructions in real time. The parallel trace interface uses 1 clock signal and 4 data signals respectively - **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2** and **TRACE_D3**.

3 Pin definition

3.1 NINA-B40 series pin assignment

Figure 2 shows an example of the module pin-out in an unconfigured state, where:

- The grey pins shown in the center of module are GND pins.
- The antenna area of the NINA- B400 and NINA-B406 is highlighted as a dotted line. The four grey pins in the antenna area are the GND pins that are supported on NINA-B406 only.
- Most of the digital or analog functions shown here and described in this data sheet can be freely assigned to any GPIO pin. Analog functions are limited to analog capable pins.
- Signals that are highlighted in red are not freely assignable but are locked to a specific pin.
- Some GPIO pins are connected to the pins located close to the radio part of the RF chip. Digital noise on these pins can reduce the radio sensitivity.



A = Analog function capable pin

Figure 2: NINA-B40 series pin assignment (top view)

⚠ Do not apply an NFC field to the NFC pins when they are configured as GPIOs. Applying the field in these circumstances can cause permanent damage to the module. When driving different logic levels on these pins in GPIO mode a small current leakage is expected. Ensure that NFC pins are set to the same logic level before entering any of the power saving modes. See section 4.2.8 for more information.

The pin-out for NINA-B40 series modules is shown in Table 6.

No.	Name	I/O	Description	nRF52 pin	Remarks
1	GPIO_1	I/O	General purpose I/O	P0.13	
2	XL1/GPIO_2	I/O	General purpose I/O Analog function enabled GPIO Connection for 32.768 kHz crystal	P0.00	May be used as a GPIO. If not used ground XL1 and XL2. If an external clock source is used instead of a crystal: Apply external low swing signal to XL1, ground XL2. Apply external full swing signal to XL1, leave XL2 grounded or unconnected. See the RC-OscillatorConfiguration AppNote [8]
3	XL2/GPIO_3	I/O	General purpose I/O Analog function enabled GPIO Connection for 32.76 kHz crystal	P0.01	
4	GPIO_4	I/O	General purpose I/O	P0.16	
5	GPIO_5	I/O	General purpose I/O	P0.17	
6	GND	-	Ground		
7	GPIO_7	I/O	General purpose I/O	P1.01	[1] Standard drive, low frequency GPIO only
8	SWO/TRACE_D0/ GPIO_8	I/O	General purpose I/O	P1.00	May be used for parallel/serial trace debug
9	VCC_IO	I	Module I/O level voltage input		Must be connected to VCC on NINA-B1
10	VCC	I	Module supply voltage input		1.7-3.6 V range
11	SWDCLK	I	Serial Wire Debug port clock signal	SWDCLK	
12	GND	-	Ground		
13	ANT	I/O	Tx/Rx antenna interface		50 Ω nominal characteristic impedance
14	GND	-	Ground		
15	SWDIO	I/O	Serial Wire Debug port data signal	SWDIO	
16	GPIO_16	I/O	Analog function enabled GPIO	P0.03	[1] Standard drive, low frequency GPIO only Pin is analog capable
17	GPIO_17	I/O	Analog function enabled GPIO	P0.28	[1] Standard drive, low frequency GPIO only Pin is analog capable
18	GPIO_18	I/O	Analog function enabled GPIO	P0.02	[1] Standard drive, low frequency GPIO only Pin is analog capable
19	RESET_N	I/O	System reset input	P0.18	Active low
20	GPIO_20	I/O	Analog function enabled GPIO	P0.31	[1] Standard drive, low frequency GPIO only Pin is analog capable, radio sensitive pin
21	GPIO_21	I/O	General purpose I/O	P0.23	[1] Standard drive, low frequency GPIO only
22	GPIO_22	I/O	General purpose I/O	P1.05	[1] Standard drive, low frequency GPIO only
23	GPIO_23	I/O	Analog function enabled GPIO	P0.29	[1] Standard drive, low frequency GPIO only Pin is analog capable
24	GPIO_24	I/O	Analog function enabled GPIO	P0.30	[1] Standard drive, low frequency GPIO only Pin is analog capable
25	GPIO_25	I/O	Analog function enabled GPIO	P0.04	Pin is analog capable
26	GND	-	Ground		
27	GPIO_27	I/O	Analog function enabled GPIO	P0.05	Pin is analog capable
28	NFC1/GPIO_28	I/O	NFC pin 1 (default)	P0.09	May be used as a GPIO [1] Standard drive, low frequency GPIO only
29	NFC2/GPIO_29	I/O	NFC pin 2 (default)	P0.10	May be used as a GPIO [1] Standard drive, low frequency GPIO only
30	GND	-	Ground		

No.	Name	I/O	Description	nRF52 pin	Remarks
31	VBUS	I	USB interface 5 V input	VBUS	Is required for USB interface to work
32	TRACE_D2/GPIO_32	I/O	General purpose I/O	P0.11	May be used for parallel trace debug
33	TRACE_D3/GPIO_33	I/O	General purpose I/O	P1.09	May be used for parallel trace debug
34	GPIO_34	I/O	General purpose I/O	P0.14	
35	GPIO_35	I/O	General purpose I/O	P1.04	[1] Standard drive, low frequency GPIO only
36	GPIO_36	I/O	General purpose I/O	P1.02	[1] Standard drive, low frequency GPIO only
37	GPIO_37	I/O	General purpose I/O	P1.06	[1] Standard drive, low frequency GPIO only
38	GPIO_38	I/O	General purpose I/O	P0.25	[1] Standard drive, low frequency GPIO only
39	GPIO_39	I/O	General purpose I/O	P1.07	[1] Standard drive, low frequency GPIO only
40	GPIO_40	I/O	General purpose I/O	P0.19	[1] Standard drive, low frequency GPIO only
41	GPIO_41	I/O	General purpose I/O	P1.03	[1] Standard drive, low frequency GPIO only
42	GPIO_42	I/O	General purpose I/O	P0.26	
43	GPIO_43	I/O	General purpose I/O	P0.15	
44	GPIO_44	I/O	General purpose I/O	P0.27	
45	TRACE_CLK/GPIO_45	I/O	General purpose I/O	P0.07	May be used for parallel or serial trace debug
46	TRACE_D1/GPIO_46	I/O	General purpose I/O	P0.12	May be used for parallel trace debug
47	GPIO_47	I/O	General purpose I/O	P0.06	
48	GPIO_48	I/O	General purpose I/O	P0.21	
49	GPIO_49	I/O	General purpose I/O	P0.22	
50	GPIO_50	I/O	General purpose I/O	P0.20	
51	GPIO_51	I/O	General purpose I/O	P1.08	
52	GPIO_52	I/O	General purpose I/O	P0.08	
53	GND	-	Ground		
54	USB_DP	I/O	USB differential data signal	USB_DP	
55	USB_DM	I/O	USB differential data signal	USB_DM	
	EGP	-	Exposed Ground Pins		The exposed pins in the center of the module should be connected to GND
	EAGP	-	Exposed Antenna Ground Pins		The exposed pins underneath the antenna area should be connected to GND

Table 6: NINA-B40 series pin-out

[1] It is advisable to keep frequencies below 10 kHz, and only use standard drive strength on these digital pins.

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings listed in the Absolute maximum rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions section of this document should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ Operating condition ranges define those limits within which the functionality of the device is guaranteed. Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	–0.3	3.9	V
V_DIO	Digital pin voltage	Input DC voltage at any digital I/O pin, VCC ≤ 3.6 V	–0.3	VCC + 0.3	V
		Input DC voltage at any digital I/O pin, VCC > 3.6 V	–0.3	3.9	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		+10	dBm

Table 7: Absolute maximum ratings

⚠ NINA-B40 modules are not protected against overvoltage or reversed voltages. Voltage spikes exceeding the power supply voltage parameters shown in Table 7 must be kept within the specified limits using appropriate protection devices.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except **ANT** pin			2**	kV	Human body model class 2 according to JEDEC JS001
			500**	V	Charged device model according to JESD22-C101
ESD indirect contact discharge			±8*	kV	According to EN 301 489-1

*Tested on NINA-B40 evaluation board.

**Target values, module qualification is ongoing.

Table 8: Maximum ESD ratings

⚠ NINA-B40 series modules are Electrostatic Sensitive Devices and require special precautions while handling. See section 8.4 for ESD handling instructions.

4.2 Operating conditions

☞ Unless otherwise specified, all given operating condition specifications are taken for an ambient temperature of 25 °C with a supply voltage of 3.3 V.

⚠ Operation beyond the specified operating conditions is not recommended. Any extended exposure outside of these specific limits can affect the device reliability.

⚠ The RAM Data retention endurance is 10,000 write/erase cycles (10 years) throughout the temperature range up to 85 °C. RAM Data retention is limited to 1000 write/erase cycles (3 years) at extended temperature range of 105 °C.

4.2.1 Operating temperature range

Parameter	Min	Max	Unit
Storage temperature	–40	+125	°C
Operating temperature	–40	+105	°C

Table 9: Temperature range

4.2.2 Supply/Power pins

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input supply voltage	1.7	3.3	3.6	V
t_RVCC	Supply voltage rise time			60	ms
VCC_ripple	VCC input noise peak to peak, 10 - 100 KHz			TBD	mV
	VCC input noise peak to peak, 100 KHz - 1 MHz			TBD	mV
	VCC input noise peak to peak, 1 - 3 MHz			TBD	mV
VCC_IO	I/O reference voltage		VCC		V

Table 10: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 11 shows the typical current consumption of NINA-B40 modules at 3V supply – regardless of the software that is used.

Condition	Typical	Peak
System OFF, no RAM retention.	600 nA	
System OFF, full 128 kB RAM retention.	1.3 µA	
System ON, full 128 kB RAM retention. System running on 32.768 kHz clock from internal oscillator.	2.6 µA	
CPU running CoreMark benchmarking tests @ 64 MHz from flash, DC/DC	3.3 mA	
Radio RX only @ 1 Mbps Bluetooth LE mode	6.0 mA	
Radio TX only, 0 dBm output power	6.0 mA	
Radio TX only, +8 dBm output power	15.5 mA	

Table 11: Module VCC current consumption

⚠ Make sure that the configured output power of your application product does not exceed the maximum allowed limits for your intended target market(s). For further information about your local limits, see Regulatory information application note [7].

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
Receiver input sensitivity	Conducted at 25 °C, 1 Mbit/s Bluetooth LE mode		–95		dBm
	Conducted at 25 °C, 2 Mbit/s Bluetooth LE mode		–92		dBm
	Conducted at 25 °C, 500 kbit/s Bluetooth LE mode		–98		dBm
	Conducted at 25 °C, 125 kbit/s Bluetooth LE mode		–102		dBm
Maximum output power	Conducted at 25 °C		+8		dBm
NINA-B406 antenna gain	Mounted on an EVB-NINA-B4		+2		dBi

Table 12: RF performance

4.2.5 32.768 kHz crystal (LFXO)

Symbol	Parameter	Typ.	Max.	Unit
F_{NOM_LFXO}	Crystal frequency	32.768	-	kHz
$F_{TOL\_LFXO\_BLE}$	Frequency tolerance, Bluetooth low energy applications[3]	-	±500	ppm
$f_{TOL\_LFXO\_ANT}$	Frequency Tolerance, ANT applications[4]	-	±50	ppm
C_{L_LFXO}	Load Capacitance	-	12.5	pF
C_{0_LFXO}	Shunt Capacitance	-	2	pF
R_{S_LFXO}	Equivalent series resistance	-	100	kΩ
C_{pin}	Input Capacitance on XL1 & XL2 pads	5	-	pF

Table 13: 32.768 kHz crystal (LFXO)

4.2.6 Antenna radiation patterns

Figure 3 provides an overview of the measurement procedure and describes how the NINA-B406 module is aligned to the XYZ-coordinate system.

A measurement is taken at every dotted position above the module image (shown left). Each measurement is represented as a grid point in the radiation pattern (shown right).

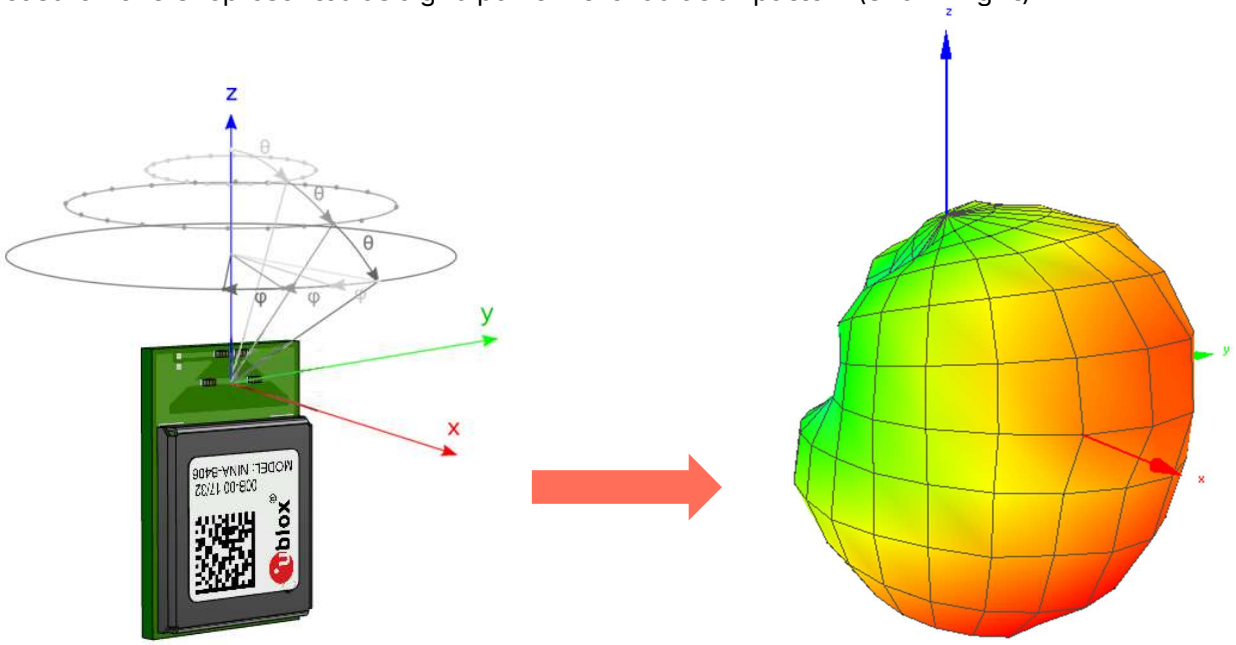
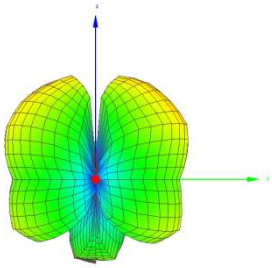
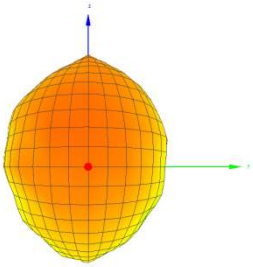
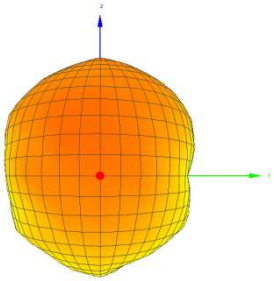
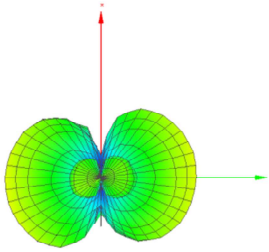
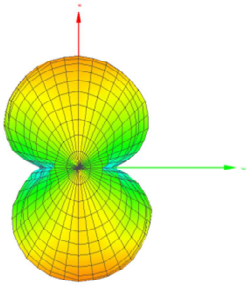
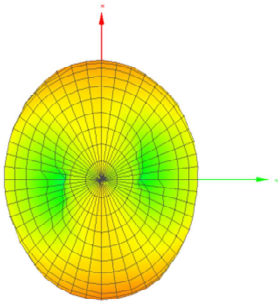
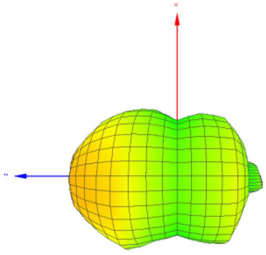
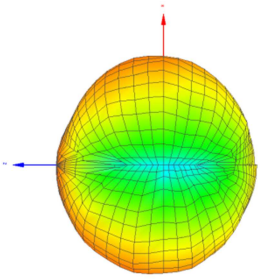
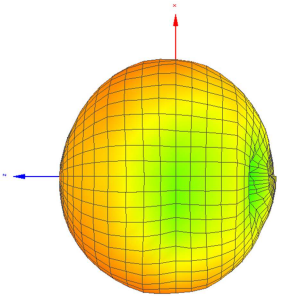
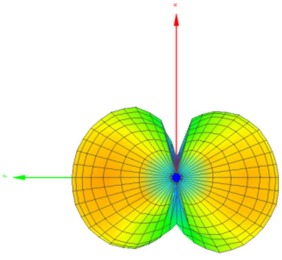
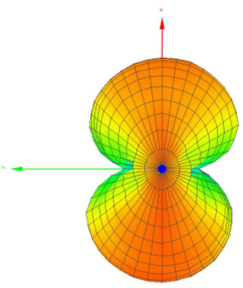
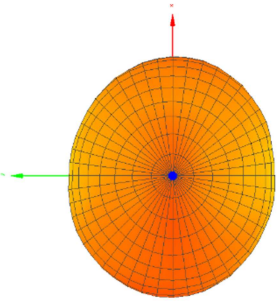


Figure 3: Measurement procedure for determining radiation patterns

[3] $f_{TOL\_LFXO\_BLE}$ and $f_{TOL\_LFXO\_ANT}$ are the maximum allowed for Bluetooth low energy and ANT applications. Actual tolerance depends on the crystal used.
[4] The ANT protocol requires the use of an external crystal.

The radiation patterns displayed in Table 14 shows the antenna gain of the NINA-B406 variant with internal antenna.

View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
	Antenna Gain (dBi) -25 -20 -15 -10 -5 0 5		
Top view, YZ plane positive X direction 			
Side view, XY plane negative Z direction 			
Side view, XZ plane negative Y direction 			
Side view, XY plane positive Z direction 			

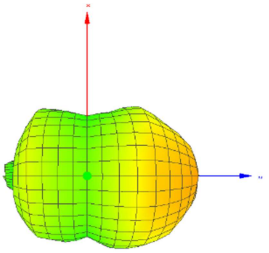
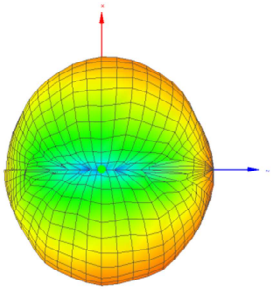
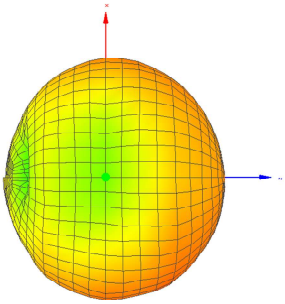
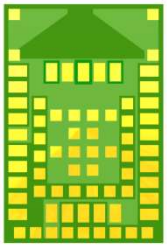
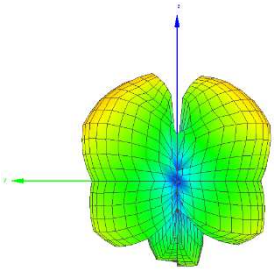
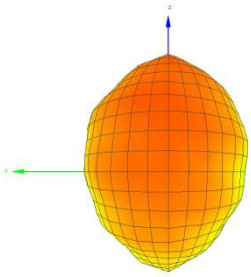
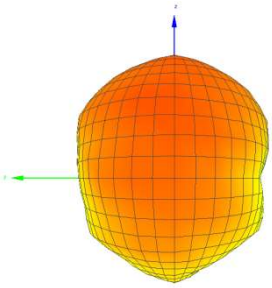
View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
	Antenna Gain (dBi) -25 -20 -15 -10 -5 0 5		
Side view, XZ plane positive Y direction 			
Bottom view, YZ plane negative X direction 			

Table 14: NINA-B4x6 antenna radiation patterns

4.2.7 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
RESET_N	Low-level input	0		0.3*VCC	V	
	Internal pull-up resistance		13		kΩ	
	RESET duration			55	ms	Time taken to release a pin reset.

Table 15: RESET_N pin characteristics

4.2.8 Digital pins

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
Any digital pin	Input characteristic: Low-level input	0		0.3*VCC	V	
	Input characteristic: high-level input	0.7*VCC		VCC	V	
	Output characteristic: Low-level output	0		0.4	V	Standard drive strength
		0		0.4	V	High drive strength
	Output characteristic: High-level output	VCC-0.4		VCC	V	Standard drive strength
		VCC-0.4		VCC	V	High drive strength
	Sink/Source current	1	2	4	mA	Standard drive strength
		3			mA	High drive strength, VCC < 2.7 V
		6	10	15	mA	High drive strength, sink, VCC ≥ 2.7 V
		6	9	14	mA	High drive strength, source, VCC ≥ 2.7 V

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
	Rise/Fall time		9 – 25		ns	Standard drive strength, depending on load capacitance
			4 – 8		ns	High drive strength, depending on load capacitance
	Input pull-up resistance	11	13	16	kΩ	Can be added to any GPIO pin configured as input
	Input pull-down resistance	11	13	16	kΩ	Can be added to any GPIO pin configured as input
GPIO_28, GPIO_29	Leakage current		1	10	µA	When not configured for NFC and driven to different logic levels

Table 16: Digital pin characteristics

4.2.9 I2C pull-up resistor values

Symbol	Parameter	Bus capacitance	Min	Typ	Max	Unit
R_PUstandard	External pull-up resistance required on I2C interface in standard mode (100 kbps)	10 pF	1	-	115	kΩ
		50 pF	1	-	23	kΩ
		200 pF	1	-	6	kΩ
		400 pF	1	-	3	kΩ
R_PUfast	External pull-up resistance required on I2C interface in fast mode (400 kbps)	10 pF	1	-	35	kΩ
		50 pF	1	-	7	kΩ
		200 pF	1	-	1.5	kΩ
		400 pF	1	-	1	kΩ

Table 17: Suggested pull-up resistor values

4.2.10 Analog comparator

Symbol	Parameter	Min	Typ	Max	Unit
t_powersave	Time to generate interrupt/event when the comparator is in power save mode		0.6		µs
t_balanced	Time to generate interrupt/event when the comparator is in balanced mode		0.2		µs
t_speed	Time to generate interrupt/event when the comparator is in high speed mode		0.1		µs

Table 18: Electrical specification of the two analog comparators

5 Mechanical specifications

5.1 NINA-B400 mechanical specification

Figure 4 shows the mechanical outline of NINA-B400 modules. NINA-B400 modules have the same footprint as the NINA-B406 outline, shown in Figure 5 and Figure 6.

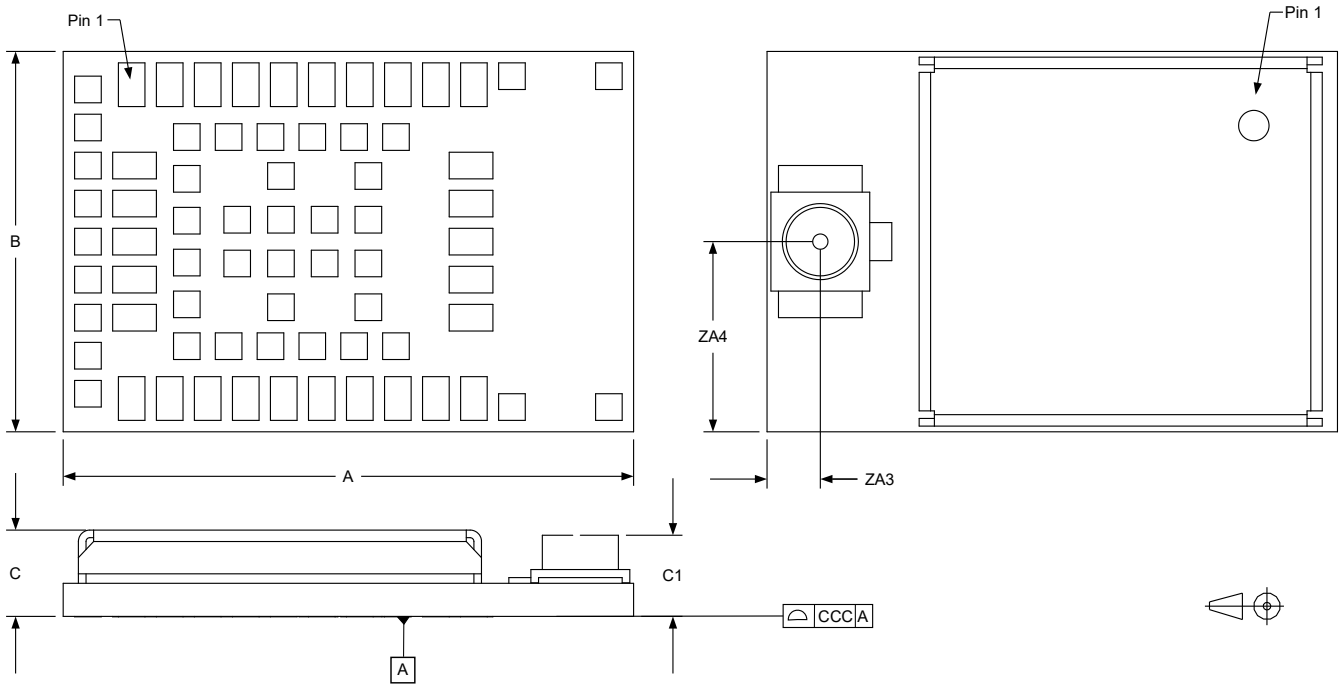


Figure 4: NINA-B400 mechanical outline

Table 19 describes the mechanical outline of NINA-B400 modules.

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	15.0	456.7	+0.20/–0.10	+7.9/–3.9
B	Module PCB width	10.0	393.7	+0.20/–0.10	+7.9/–3.9
C	Module thickness	2.23	87.8	+0.40/–0.20	+15.8/–7.9
C1	Module thickness at U.FL antenna connector	2.13	83.9	+0.40/–0.20	+15.8/–7.9
ccc	Seating plane coplanarity	0.10	3.9	+0.02/–0.10	+0.8/–3.9
ZA3	Horizontal pin of U.FL antenna connector center to left lower corner	1.40	55.1	±0.20	±7.9
ZA4	Vertical pin of U.FL antenna connector center to left lower corner	5.00	196.8	±0.20	±7.9
	Module weight [g]	<1.0			

Table 19: NINA-B400 mechanical outline data

5.2 NINA-B406 mechanical specification

Figure 5 shows the mechanical outline of NINA-B4x6 modules.

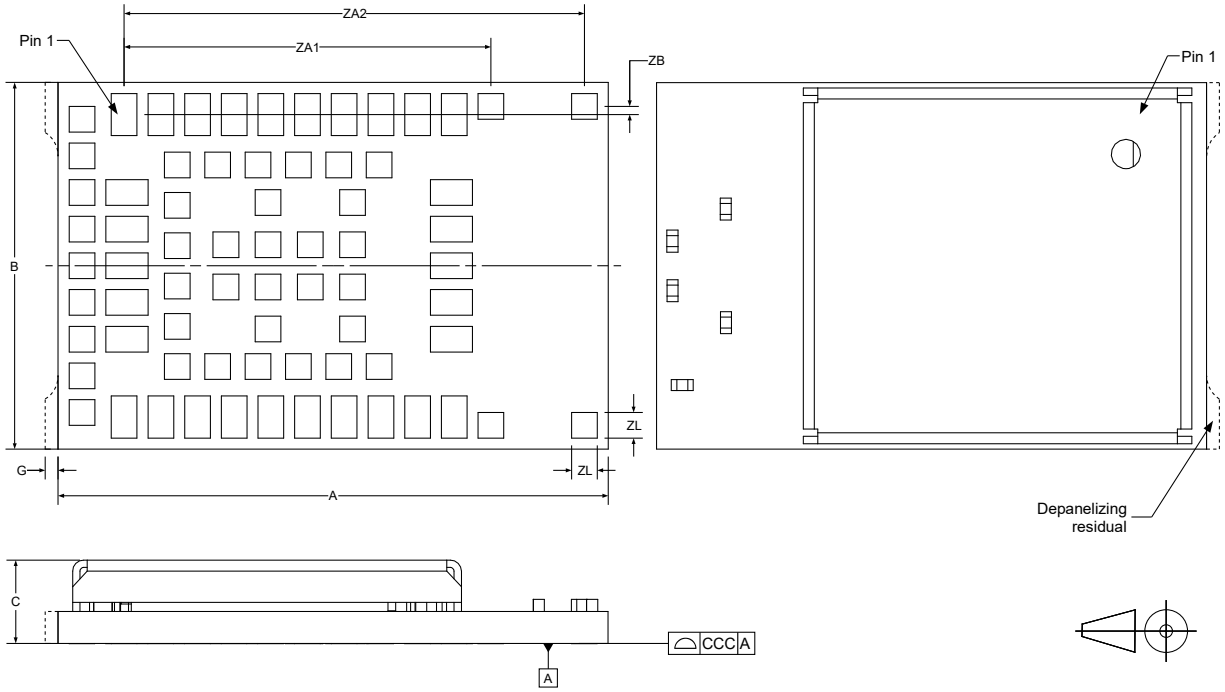


Figure 5: NINA-B40x6 mechanical outline

Figure 6 shows the pad dimensions of NINA-B4x modules. The dimensions are compatible with those of NINA-B301/B311 module variants.

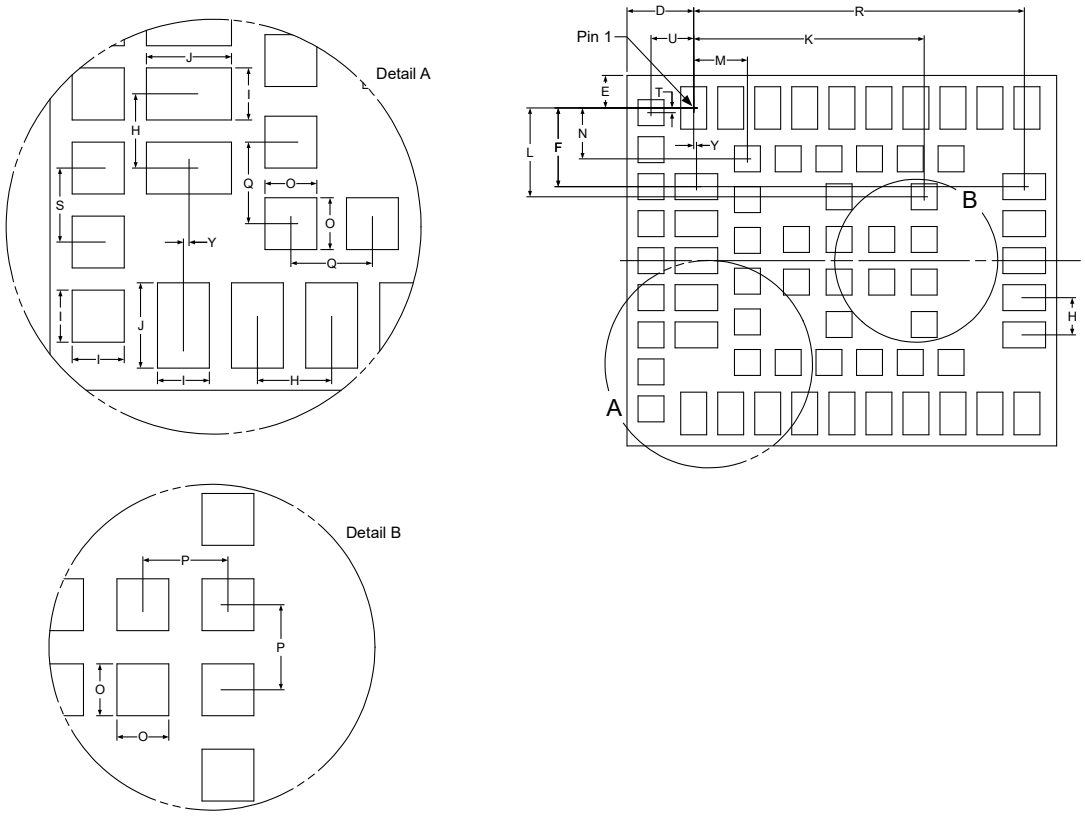


Figure 6: NINA-B40 pad dimensions

Table 20 describes the mechanical outline of NINA-B4x6 modules.

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	15.0	456.7	+0.20/–0.10	+7.9/–3.9
B	Module PCB width	10.0	393.7	+0.20/–0.10	+7.9/–3.9
C	Module thickness	2.23	87.8	+0.40/–0.20	+15.8/–7.9
ccc	Seating plane coplanarity	0.10	3.9	+0.02/–0.10	+0.8/–3.9
D	Horizontal edge to pin 1 center	1.80	70.9	±0.10	±3.9
E	Vertical edge to pin 1 center	0.875	34.5	±0.10	±3.9
F	Vertical pin 1 center to lateral pin center	2.125	87.9	±0.05	±2.0
G	Depanelizing residual	0.10	3.9	+0.25/-0.1	+9.8/-3.9
H	Lateral and antenna row pin to pin pitch	1.00	39.4	±0.05	±2.0
I	Lateral, antenna row and outer pin width	0.70	27.6	±0.05	±2.0
J	Lateral and antenna row pin length	1.15	45.3	±0.05	±2.0
K	Horizontal pin 1 center to central pin center	6.225	245.1	±0.05	±2.0
L	Vertical pin 1 center to central pin center	2.40	94.5	±0.05	±2.0
M	Horizontal pin 1 center to inner row pin center	1.45	57.1	±0.05	±2.0
N	Vertical pin 1 center to inner row pin center	1.375	54.1	±0.05	±2.0
O	Central, inner and outer row pin width and length	0.70	27.6	±0.05	±2.0
P	Central pin to central pin pitch	1.15	45.3	±0.05	±2.0
Q	Inner row pin to pin pitch	1.10	43.3	±0.05	±2.0
R	Horizontal pin 1 center to antenna row pin center	8.925	351.4	±0.05	±2.0
S	Outer row pin to pin pitch	1.00	39.4	±0.05	±2.0
T	Vertical pin 1 center to outer row pin center	0.125	4.9	±0.05	±2.0
U	Horizontal pin 1 center to outer row pin center	1.15	45.3	±0.05	±2.0
Y	Horizontal pin 1 center to lateral pin center	0.075	3.0	±0.05	±2.0
ZA1	Horizontal pin 1 center to first set of antenna GND pins pin center	10.0	393.7	±0.05	±2.0
ZA2	Horizontal pin 1 center to second set of antenna GND pins pin center	12.55	494.1	±0.05	±2.0
ZB	Vertical pin 1 center to antenna GND pin center	0.225	8.9	±0.05	±2.0
ZL	Antenna GND pin width and length	0.70	27.6	±0.05	±2.0
	Module weight [g]	<1.0			

Table 20: NINA-B406 mechanical outline data

6 Qualification and approvals

6.1 Country approvals

The NINA-B400 and NINA-B406 modules are certified for use in the following countries/regions:

Country/region	NINA-B400	NINA-B406
Europe	Approved	Approved
USA	Approved	Approved
Canada	Pending	Pending
Japan	Pending	Pending
Taiwan	Pending	Pending
South Korea	Pending	Pending
Brazil	Pending	Pending
Australia	Pending	Pending
New Zealand	Pending	Pending
South Africa	Pending	Pending

☞ For detailed information about the regulatory requirements that must be met when using NINA-B40 modules in an end product, see the NINA-B4 series certification application note [7].

6.2 Bluetooth qualification

NINA-B40 module series are qualified as an end product in accordance with the Bluetooth 5.1 specification.

Product type	QD ID	Listing date
End product	157158	2020-10-13

Table 21: NINA-B40 series Bluetooth qualified design ID

7 Antennas

See the Regulatory information application note [7] for information about approved antennas.

8 Product handling

8.1 Packaging

To enable efficient production, production lot set-up and tear-down, NINA-B40 series modules are delivered as hermetically sealed, reeled tapes. For more information about packaging, see the u-blox package information guide [1].

8.1.1 Reels

NINA-B40 modules are deliverable in quantities of 500 pieces on a reel. The reel types for NINA-B40 modules are described in Table 22. For more detailed information about the reel types, see the u-blox package information guide [1].

Model	Reel type
NINA-B400	A3
NINA-B406	A3

Table 22: Reel types for different NINA-B40 series models

8.1.2 Tapes

Figure 7 shows the position and orientation of NINA-B40 modules as they are delivered on tape.

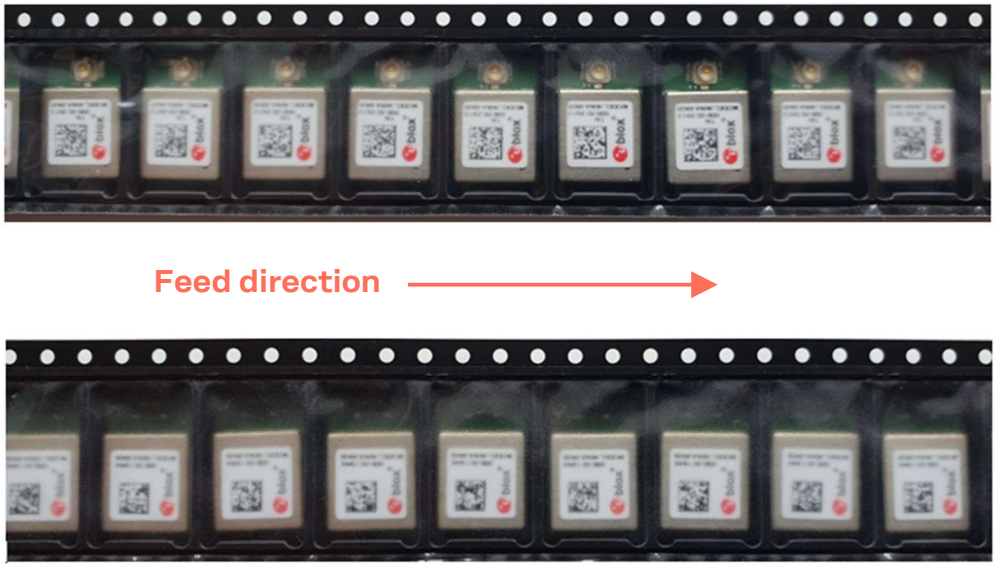
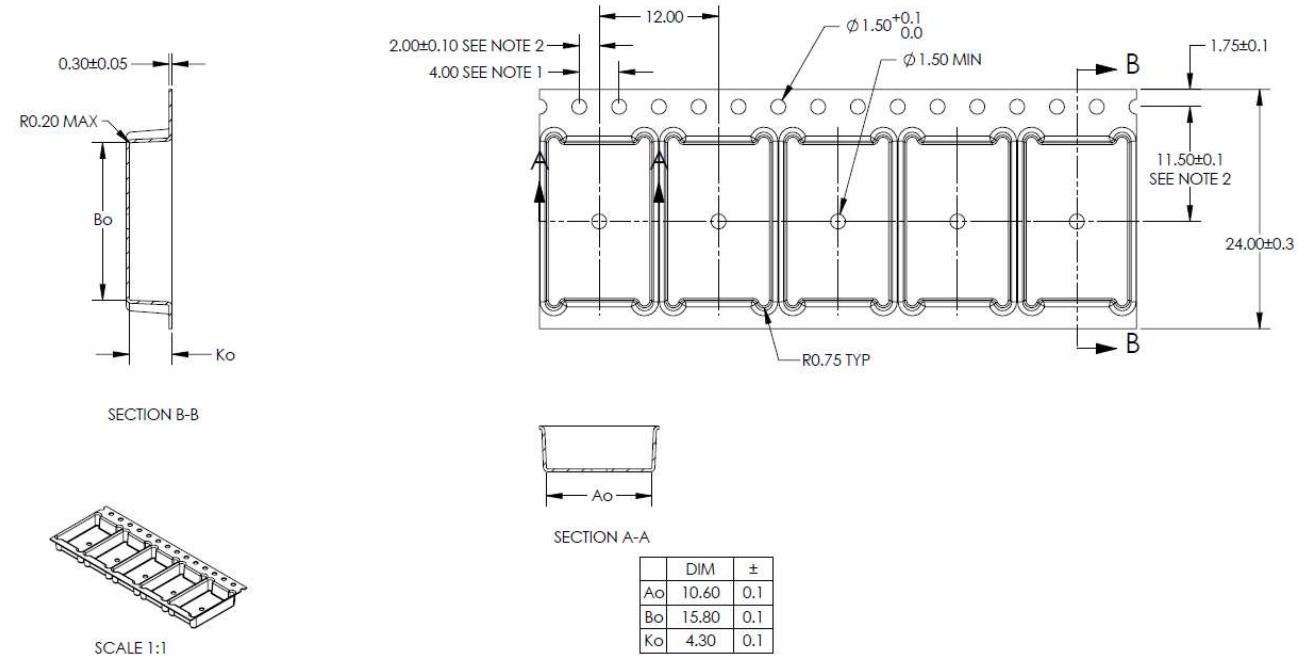


Figure 7: Orientation of NINA-B40 modules on tape

Figure 8 shows the tape dimensions of NINA-B40 modules on tape.



	DIM	±
Ao	10.60	0.1
Bo	15.80	0.1
Ko	4.30	0.1

Figure 8: NINA-B4x2 and NINA-B4x6 tape dimensions

8.2 Moisture sensitivity levels

⚠ In accordance with the IPC/JEDEC J-STD-020 standard, NINA-B40 series modules are tested, classified and rated as Moisture Sensitive Devices (MSD). The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions.

NINA-B40 series modules are rated at MSL level 4.

☞ For more information about the moisture sensitivity levels, labeling, and storage of u-blox chips, modules and antennas, see the u-blox package information guide [1].

☞ For general information about MSL, download the joint IPC/JEDEC J-STD-020 standard from www.jedec.org.

8.3 Reflow soldering

Reflow profiles are selected according to u-blox recommendations. For more information, see the NINA-B40 series system integration manual [3].

⚠ Failure to follow these recommendations can result in severe damage to the device.

8.4 ESD precautions

⚠ NINA-B40 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling NINA-B40 series modules without proper ESD protection may destroy or damage them permanently.

NINA-B40 series modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions appropriate for ESD sensitive components. Section 4.1.1 provides the maximum ESD ratings of NINA-B40 series modules.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates NINA-B40 series modules. Failure to observe these recommendations can result in severe damage to the device.

9 Product labeling

The labels of the NINA-B40 series modules include important product information.

Figure 13 shows the label applied to NINA-B40 series modules. It includes the u-blox logo, production lot, product type number, and certification numbers (if applicable).

Figure 13: Location of product type number on the NINA-B40 series module label

Reference	Description
1	Date of unit production (year/week)
2	Product version
3	Product name
4	Data Matrix with unique serial number of 19 alphanumeric symbols. The first 3 symbols represent module type number unique to each module variant, the next 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and the last 4 symbols represent the hardware and firmware version encoded HHFF.

Table 23: NINA-B40 series label description

Three different product code formats are shown on the label:

- **Product name** that identifies all u-blox modules – independent of the packaging and quality grade.
- **Ordering code** includes options and quality
- **Type number** includes the hardware and software versions.

Table 24 below details these three different formats:

Format	Structure
Product Name	PPPP-TGVV
Ordering Code	PPPP -TGVV-TTQ
Type Number	PPPP -TGVV-TTQ-XX

Table 24: Product code formats

Table 25 explains the various parts of the product code.

Code	Meaning	Example
PPPP	Form factor	NINA
TG	Platform (Technology and Generation) T – Dominant technology, for example, W: Wi-Fi, B: Bluetooth G - Generation	B4: Bluetooth Generation 4
VV	Variant based on the same platform; range [00…99]	11: default configuration, with antenna pin
TT	Major product version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 25: Part identification code

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
AOA	Angle of Arrival
AOD	Angle of Departure
Bluetooth LE	Bluetooth Low Energy
BPF	Band Pass Filter
CTS	Clear To Send
EDM	Extended Data mode
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GPIO	General Purpose Input/Output
IC	Industry Canada
I2C	Inter-Integrated Circuit
MCU	Micro Controller Unit
MSD	Moisture Sensitive Device
RTS	Request To Send
SPI	Serial Peripheral Interface
TBD	To be Defined
UART	Universal Asynchronous Receiver/Transmitter

Table 26: Explanation of the abbreviations and terms used

Related documents

[1] u-blox package information guide, UBX-14001652
[2] u-blox short range AT commands manual, UBX-14044127
[3] NINA-B4 system integration manual, UBX-19052230
[4] u-connectXpress software user guide, UBX-16024251
[5] NINA-B40 product summary, UBX-19047297
[6] NINA-B3 data sheet, UBX-17052099
[7] NINA-B4 series certification application note, UBX-20037320
[8] RC oscillator configuration, application note, UBX-20009242

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	17-Dec-2019	hekf	Initial release.
R02	25-Mar-2020	asoh, hisa, hekf	Updated NINA-B400 status from “In Development” to “Prototype”. GPIO pins updated to 38. EIRP value updated to 10 dBm.
R03	13-Aug-2020	asoh	Revised document scope and content to describe NINA-B400 and NINA-B406 modules (with NINA-B41 module variants to be later included in a separate data sheet). Updated the product status from “Prototype” to “Engineering Sample”. Revised module height dimensions given in sections 1.1 and 1.1, and updated Human body model class in section 4.1.1.
R04	16-Oct-2020	asoh	Updated the PCB trace antenna radiation pattern information in section 4.2.6. Revised the tape dimensions shown in section 8.1.2. Revised product status in Document information.

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