TeleVideo® Terminal Maintenance Training Manual

March 1983

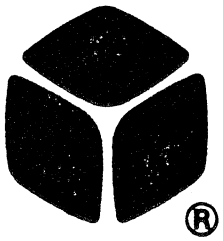
Disclaimer

TeleVideo Systems, Inc. makes no representations or warranties with respect to the contents hereof and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Further, TeleVideo Systems, Inc. reserves the right to revise this publication and to make changes from time to time in the content hereof without obligation of TeleVideo Systems, Inc. to notify any person of such revision or changes.

TeleVideo Systems, Inc., 1170 Morse Avenue, Sunnyvale, California 94086 408/745-7760

3029900 © TeleVideo 5/83 Printed in U.S.A.

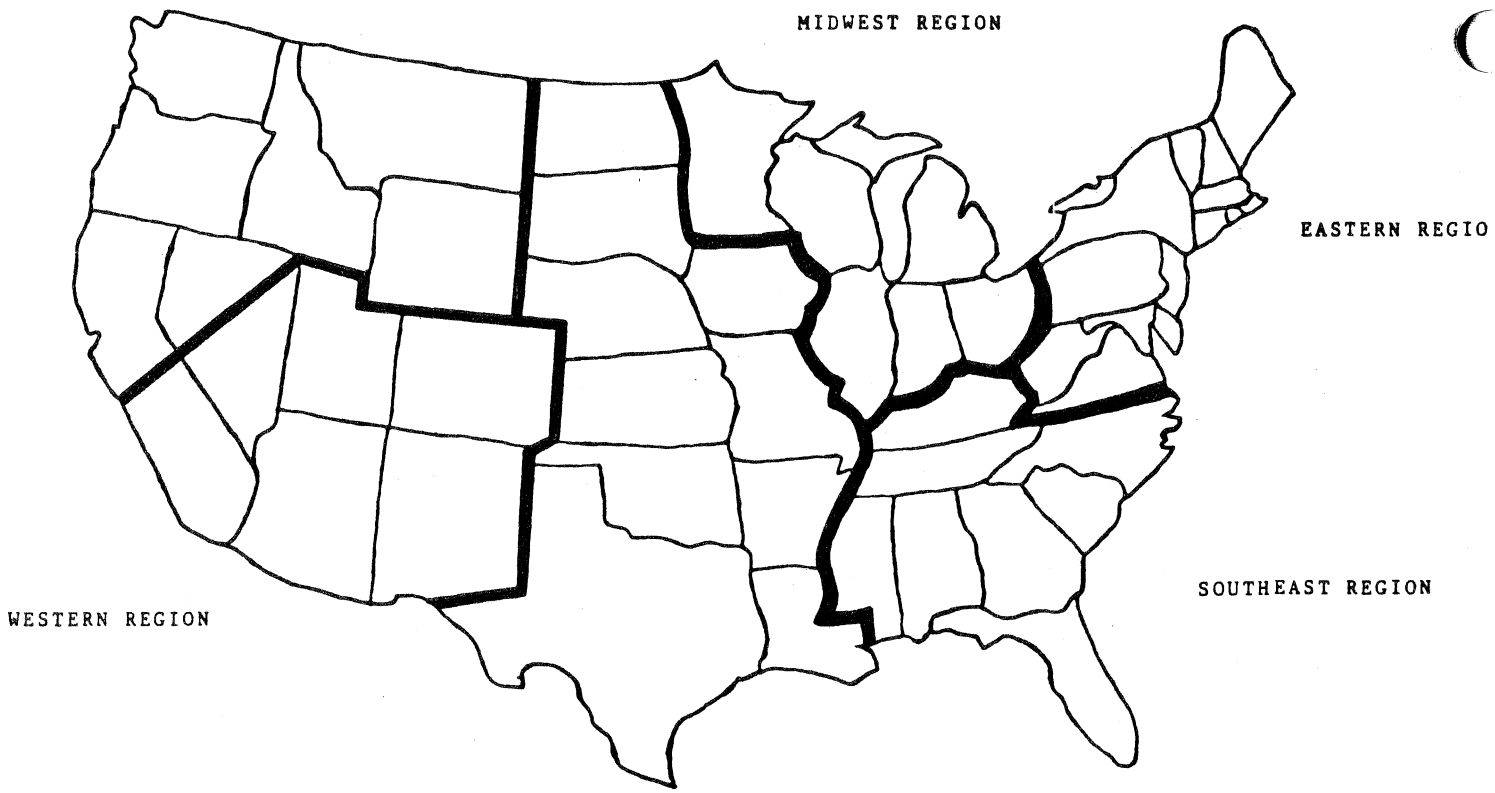
TABLE OF CONTENTS



ORDERING SPARE PARTS

Parts are ordered directly from Terminal Spare Parts order entry at our coporate head quarters in Sunnyvale, California. Call (408) 745-7760 or (800) 538-8725 (outside California). For international customers Telex 910-399-9621, attention Terminal Spares Order Entry. Contract customers and institutions can order parts on a Purchase Order and be invoiced; please have Purchase Order number and TeleVideo part number ready at time of call. All other customers must order parts on a C.O.D. or cash-in-advance basis. There is a $50.00 minimum on all orders (except manuals).

For orders placed in California, add 6.5% sales tax. There is a shipping and handling charge of $10.00 per order. There will be no drop shipments, so please include the shipping and billing addresses with your order. Shipments are made Best Way, which is UPS or U.S. Mail. Any special shipping requests will be accommodated, but any extra costs incurred will be added to the invoice.



REGIONAL SALES OFFICE

WESTERN REGION

505 N. TUSTIN AVE.
SUITE 253
SANTA ANA, CA. 92705
(714) 557-6095

EASTERN REGION

202 JOHNSON RD.
SUITE A-107
ATRUIM 1
MORRIS PLAINS, NJ 07950
(201) 267-8805

NORTHWEST REGION

1170 MORSE AVE
SUNNYVALE, CA. 94086
(408) 745-7760

SOUTHERN REGION

4560 BELTLINE RD.
SUITE 424
DALLAS, TX 75293
(214) 980-9978

SOUTHEAST REGION

5901-C PEACHTREE-DUNWOODY RD.
SUITE 260
ATLANTA, GA. 30328
(404) 399-6464

MIDWEST REGION

125 E. LAKE ST.
SUITE 203
BLOOMINGDALE, ILL. 60108
(312) 351-9350

October 29, 1982
TERMINAL SPARE PART PRICE LIST WITH REFERENCE TO NEW PART NUMBERS

DESCRIPTION	OLD P/N	NEW P/N	UNIT PRICE
MANUALS			
INSTAL & USER GUIDE 910	B300005-001	2004800	5.00
INSTAL & USER GUIDE 910PLUS	B300021-001	2004600	5.00
INSTAL & USER GUIDE 912/920	B300001-001	2001800	5.00
INSTAL & USER GUIDE 925	B300013-001	2003500	5.00
INSTAL & USER GUIDE 950	B300002-002	2002000	5.00
MAINTENANCE MANUAL 910/910PLUS	B300005-002	2002600	50.00
MAINTENANCE MANUAL 912/920	B300001-002	2001900	50.00
MAINTENANCE MANUAL 925	B300013-002	2003600	50.00
MAINTENANCE MANUAL 950	B300002-002	2002100	50.00
MODULES			
POWER SUPPLY MODULE	BC-01642	2195700	91.00
VIDEO MODULE	BC-01643	2195800	93.00
LOGIC BOARD 910	B900011-001	2014000	395.00
LOGIC BOARD 910 G/A	B900011-001	2014001	395.00
LOGIC BOARD 910PLUS	B900011-003	2014002	395.00
LOGIC BOARD 910PLUS G/A	B900011-003	2014500	395.00
LOGIC BOARD 912/920B	B900001-001	2009000	458.00
LOGIC BOARD 912/920C	B900001-001	2009002	458.00
LOGIC BOARD 925	B900014-001	2015500	514.00
LOGIC BOARD 925 G/A	B900014-001	2015501	514.00
LOGIC BOARD 950	B900002-001	2009500	539.00
LOGIC BOARD 950 G/A	B900002-001	2009501	539.00
KEYBOARD ASSEMBLY 910/910PLUS	K030330-003	2090001	105.00
KEYBOARD ASSEMBLY 912B	K030330-001	2206500	105.00
KEYBOARD ASSEMBLY 912C	K030330-003	2090000	105.00
KEYBOARD ASSEMBLY 920B	K030330-002	2089900	126.00
KEYBOARD ASSEMBLY 920C	K030330-004	2090100	126.00
KYBD ASSEMBLY W/HOUSING 925/950	K030331-001	2090200	175.00
TUBE, B/W P4 12"	T300002-001	2049100	179.00
TUBE, GREEN P31 12"	T300002-002	2049300	179.00
CASES			
TOP CASE 910/912	CRT-010267	2151600	97.80
TOP CASE 920	CRT-010334	2153800	97.80
TOP CASE 925/950	CRT-05001	2141800	97.80
TOP CASE KEYBOARD 925/950	CRT-04001	2204200	25.00
BOTTOM CASE 910/912/920	CRT-010268	2151700	70.20
BOTTOM CASE 925/950	CRT-05002	2141700	70.20
BOTTOM CASE KEYBOARD 925/950	CRT-04002	2199100	35.00
BEZEL TOP CASE 925/950	CRT-05003	2141900	20.00
BEZEL KEYBOARD 925/950	CRT-04003	2198000	10.00

KITS/OPTIONS

PATTERN GENERATOR (912/950 INSTALLED)		2122300	200.00
DEMO PROGRAM EPROM 910		8000094	16.00
DEMO PROGRAM EPROM 910PLUS		8000073	16.00
DEMO PROGRAM EPROM 925		8000072	16.00
DEMO PROGRAM EPROM 950		8000119	16.00
CONVERSION KIT 910		2169700	25.00
CONVERSION KIT 910PLUS		2169100	25.00
CONVERSION KIT CP/M WORDSTAR 950		2187400	100.00
CURRENT LOOP KIT 910/910PLUS	A300006-001	2131000	50.00
CURRENT LOOP KIT 925	A300006-002	2131100	60.00
MEMORY KIT 2ND PAGE 912/920	A300004-001	2001400	35.00
MEMORY KIT 2ND PAGE 925/950	A300004-002	2001500	40.00
MEMORY KIT 3RD,4TH PAGE 950	A300004-003	2001600	80.00
MEMORY KIT 2ND,3RD,4TH PAGE 950		2231700	120.00
SP PTS LOGIC BOARD 910	A300001-007	2000600	112.22
SP PTS LOGIC BOARD 910 G/A		2225400	158.12
SP PTS LOGIC BOARD 910PLUS	A300001-009	2000800	124.19
SP PTS LOGIC BOARD 910PLUS G/A		2225500	162.70
SP PTS LOGIC BOARD 912/920	A300001-001	2000000	150.80
SP PTS LOGIC BOARD 925	A300001-011	2001000	135.71
SP PTS LOGIC BOARD 925 G/A		2225300	181.61
SP PTS LOGIC BOARD 950	A300001-005	2000400	183.08
SP PTS LOGIC BOARD 950 G/A		2233000	218.90
SP PTS MECH 910/910PLUS	A300001-010	2000900	60.23
SP PTS MECH 912/920	A300001-003	2000200	66.03
SP PTS MECH 925/950	A300001-006	2000500	54.05
SP PTS POWER SUPPLY/VIDEO MOD	A300001-002	2000100	134.28
SP PTS ADDITIONAL PARTS	A300001-004	2000300	202.25

ELECTRICAL COMPONENTS — CAPACITORS

CAP CERAMIC 1.0PF 1KV SPARK GAP	C900100-012	2030900	2.04
CAP CERAMIC 220PF 50V	CC-50221SL	2195900	.72
CAP CERAMIC .01UF 16V 20%	C900100-001	2028700	.72
CAP CERAMIC 330PF 50V 20%	C900100-003	2029100	.72
CAP CERAMIC .1UF 50V 10%	C900100-008	2030100	.72
CAP DIP MICA 10PF	C600100-001	2024100	.72
CAP ELECTROLYTIC 22UF 15V	C700100-001	2025700	.72
CAP ELECTROLYTIC 22UF 50V	C700100-003	2026100	.72
CAP ELECTROLYTIC 4.4UF 35V 10%	C700100-008	2026900	2.08
CAP ELECTROLYTIC 10UF 16V 20%	C700100-010	2027300	.72
CAP ELECTROLYTIC 1UF 16V 10%	C700100-013	2027900	1.08
CAP ELECTROLYTIC .22UF 35V	C700100-016	2028500	.72
CAP ELECTROLYTIC 100UF 10V	CE-10107S	2196000	.72
CAP ELECTROLYTIC 22UF 100V	CE-10226SH	2196100	.72
CAP ELECTROLYTIC 2.2KUF 10V	CE-10228S	2196200	2.28
CAP ELECTROLYTIC 100UF 160V	CE-16107SH	2196300	6.60
CAP ELECTROLYTIC 22UF 160V	CE-16226SH	2196400	1.27
CAP ELECTROLYTIC 220UF 16V	CE-16227S	2199300	.72
CAP ELECTROLYTIC 3.3KUF 35V	CE-35338S	2196500	6.91
CAP ELECTROLYTIC 4.7KUF 16V	CE-35478S	2196600	6.56
CAP ELECTROLYTIC 4.7UF 16V	CM-16475	2196700	.72
CAP ELECTROLYTIC 470 35V	CT-35338S	2198200	1.68

CAP MICA 20PF	C600100-002	2024300	.72
CAP MICA 100PF 50V 5%	C600100-004	2024700	.72
CAP MICA 47PF 50V 5%	C600100-005	2024900	.72
CAP MICA 150PF 500V 1%	C600100-006	2025100	.72
CAP MICA 330PF 500V 5%	C600100-007	2025300	.95
CAP MICA 390PF 500V 5%	C600100-008	2025500	1.07
CAP MONOLYTHIC.01UF 50V 10%	C900100-002	2028900	.72
CAP MONOLYTHIC 330PF 100V 20%	C900100-004	2029300	.72
CAP MONOLYTHIC 47PF 100V 5%	C900100-005	2029500	1.08
CAP MONOLYTHIC 68PF 1KV 20%	C900100-007	2029900	.72
CAP MONOLYTHIC .039UF 50V 10%	C900100-009	2030300	.72
CAP MONOLYTHIC .039UF 50V 5%	C900100-010	2030500	1.08
CAP MYLAR .0068UF 200V	CM-20682H	2196800	.72
CAP MYLAR .001UF 50V	CM-50102	2196900	.72
CAP MYLAR .01UF 50V	CM-50103	2197000	.72
CAP MYLAR .047UF 50V	CM-50473	2197100	.72
CAP MYLAR .47UF 50V	CM-50474	2197200	1.44
CAP MYLAR .1UF 600V	CM-60104H	2197300	1.35
CAP MYLAR .047UF 400V	CO-40473H	2197500	1.86
CAP RADIAL LEAD 1UF 15V	C800100-001	2027901	.72
CAP TANTALUM .68UF 50V	C700100-002	2025900	1.74
CAP TANTALUM 3.3UF 50V 10%	C700100-005	2026300	2.40
CAP TANTALUM 10UF 25V 10%	C700100-009	2027100	1.98
CAP TANTALUM 4.7UF 16V 10%	C700100-011	2027500	.96
CAP TANTALUM .33UF 35V	CT-35334	2198100	1.20
CAP NON POLARIZED .20UF 50V	CN-152065	2197400	4.63

****

DIODES - REGULATORS - TRANSISTORS

****

DIODE ZENER IN759A/RD12EB	SD-10254	2201600	1.82
DIODE IN914	S360100-000	2047500	.72
DIODE IN920/KDS8513A	SD-10258	2201800	.90
DIODE IN4001	S360100-001	2047700	.91
DIODE IN4004/DS-130TB	SD-10257	2202200	1.00
DIODE IN5391/DS135D	SD-01251	2200600	.72
DIODE DSA17C/MR500	SD-01253	2201500	1.94
DIODE DS18/IDS135D	SD-01252	2201400	.72
DIODE DS113A/MRI-1000	SD-01255	2201700	6.29
DIODE LEC MV55A RED	S360100-003	2048100	3.00
DIODE P6KE	S360100-002	2047900	4.20
REGULATOR LAS1512	SI-0551	2202500	35.00
REGULATOR LAS16CB	R600005-001	2126900	18.60
REGULATOR LAS1605	R600004-003	2126800	23.70
REGULATOR LAS1812	SI-01553	2202400	35.00
REGULATOR 78MO5	R600000-001	2126100	3.96
TRANSISTOR 2N2219A	S350100-000	2045300	3.60
TRANSISTOR 2N2907A	S350100-003	2045900	.97
TRANSISTOR 2N3019	S350100-002	2045700	2.64
TRANSISTOR 2N3906/2SA495	ST-10351	2042200	.91
TRANSISTOR 2N4401/2SC1166	S350100-001	2045500	2.02
TRANSISTOR 2N5551/2SC983	S350100-009	2047100	2.59
TRANSISTOR 2N6121/2SC1173	ST-01353	2199700	4.00
TRANSISTOR 2N6124/2SA473	ST-01354	2202100	4.28
TRANSISTOR 2SC2233/MJE13006	S350100-010	2047300	22.80
TRANSISTOR KTC 1627A/MPSA06	S350100-007	2046700	2.07
TRANSISTOR 2N3904/KTC1815	S350100-006	2046500	4.50

FIRMWARE

SYSTEM EPROM 910	I800000-020	8000020	37.50
SYSTEM ROM 910	I800000-015	8000015	18.90
SYSTEM EPROM 910PLUS	I800000-040	8000040	25.00
SYSTEM ROM 912/920B (A49B1)	I740010-049	2033800	25.80
SYSTEM ROM 912/920C (A49C1)	I740010-050	2034000	25.80
SYSTEM EPROM 925	I800000-033	8000033	37.50
SYSTEM EPROM 925	I800000-031	8000031	37.50
SYSTEM ROM 950 (A41)	I800000-001	8000001	18.90
SYSTEM ROM 950 (A42)	I800000-007	8000007	18.90
CHAR GEN EPROM 910/910PLUS	I800000-021	8000021	37.50
CHAR GEN ROM 910/910PLUS	I800000-016	8000016	18.90
CHAR GEN ROM 912/920 (A3-2)	I740010-053	2034600	14.94
CHAR GEN EPROM 925	I800000-021	8000021	37.50
CHAR GEN ROM 925	I800000-016	8000016	18.90
CHAR GEN ROM 950 (A32)	I800000-003	8000003	18.90
CHAR GEN ROM 950 (A33)	I800000-002	8000002	18.90
KYBD EPROM 910/910PLUS	I800000-019	8000019	21.00
KYBD ENCDR 910/910PLUS	I800000-020	2053200	22.50
KYBD ENCDR 910/910PLUS	I740011-013	2051800	22.50
KYBD ROM 925/950 (U6)	I800000-009	8000009	37.50

INTERGRATED CIRCUITS

IC 74S00	I740010-000	2024000	2.20
IC 74LS00	I740010-001	2024200	1.72
IC 74LS03	I740010-002	2024400	1.72
IC 74S04	I740010-003	2024600	2.41
IC 74LS04	I740010-004	2024800	1.80
IC 74LS05	I740010-005	2025000	1.80
IC 74LS08	I740010-006	2025200	1.80
IC 74LS10	I740010-007	2025400	1.80
IC 74SL20	I740010-008	2025600	1.72
IC 74LS32	I740010-009	2025800	1.86
IC 74LS42	I740010-010	2026000	2.55
IC 74LS51	I740010-011	2026200	1.80
IC 74S74	I740010-012	2026400	3.58
IC 74LS74	I740010-013	2026600	1.80
IC 74LS86	I740010-014	2026800	2.07
IC 74LS109	I740010-015	2027000	2.00
IC 74LS139	I740010-016	2027200	3.18
IC 74LS157	I740010-017	2027400	2.76
IC 74LS163	I740010-018	2027600	4.56
IC 74LS166	I740010-019	2027800	5.04
IC 74LS173	I740010-020	2028000	4.14
IC 74LS174	I740010-021	2028200	3.18
IC 74LS253	I740010-022	2028400	3.24
IC 74LS367	I740010-023	2028600	2.76
IC 74LS373	I740010-024	2028800	3.48
IC 74LS374	I740010-025	2029000	3.48
IC 75188N/1488	I740010-026	2029200	4.14
IC 75189AN/1489	I740010-027	2029400	4.14
IC TIL117	I740010-029	2029800	4.48
IC NE555	I740010-031	2030200	2.58

IC DP8304	I740010-032	2030400	17.59
IC AMD2111-4A	I740010-033	2030600	13.32
IC 2502HP	I740010-034	2030800	15.52
IC TMS9927/5027	I740010-035	2031000	81.76
IC P8035	I740010-036	2031200	41.05
IC H11G3	I740010-051	2034200	3.45
IC 7406	I740010-054	2034800	2.05
IC 4N38	I740010-055	2035000	4.32
IC 7414	I740010-057	2035400	1.92
IC 2114	I740010-059	2035800	9.75
IC 74LS245/N8T245N	I740010-061	2036200	5.76
IC 74LS191	I740010-063	2036600	2.70
IC 74LS273	I740010-068	2037600	3.48
IC 74S240	I740010-069	2037800	8.82
IC 74LS175	I740010-070	2038000	1.74
IC 74S32/629	I740010-074	2038800	1.80
IC 74LS11	I740010-076	2040000	1.14
IC 93S16PC	I740010-080	2040800	6.60
IC 74LS138	I740010-081	2041000	1.68
IC 74LS02	I740010-084	2041600	1.14
IC 74LS241	I740010-086	2042000	3.54
IC AM26LS31	I740010-088	2042400	7.92
IC AM26LS32	I740010-089	2042600	7.92
IC 74LS240	I740010-096	2044000	3.54
IC 74LS244	I740010-097	2044200	5.52
IC 74S174	I740010-099	2044600	3.96
IC 74LS14	I740010-105	2045800	1.44
IC 6116	I740011-000	2049200	40.00
IC 6502A	I740011-002	2049600	28.94
IC 6545	I740011-003	2049800	66.24
IC 6551 1MHz	I740011-004	2155700	28.80
IC 6552A	I740011-005	2050200	27.21
IC Z80A SIO/2	I740011-007	2050600	58.00
IC Z80A CTC	I740011-008	2050800	16.80
IC Z80A CPU	I740011-009	2051000	21.18
IC Z80A DMA	I740011-010	2051200	56.76
IC 64K RAM DYN	I740011-012	2051600	83.76
IC 68B045 2 MHz	I740011-017	2052600	31.50
IC SY6551A-1 2MHz	I740011-019	2053000	24.00
IC SY6545A-1 2MHz	I740011-018	2052800	50.10
IC 910/910 PLUS GATE ARRAY		2057400	42.60
IC 925 GATE ARRAY		2057400	42.60
IC 950 GATE ARRAY A		2057600	23.88
IC 950 GATE ARRAY B		2057800	23.88

****

RESISTORS & POTENTIOMETERS

****

RES CF 68 OHM 1/4W 5%	R514000-001	2051100	.72
RES CF 270 OHM 1/4W 5%	R514000-002	2051300	.72
RES CF 330 OHM 1/4W 5%	R514000-003	2051500	.72
RES CF 470 OHM 1/4W 5%	R514000-004	2051700	.72
RES CF 510 OHM 1/4W 5%	R514000-005	2051900	.72
RES CF 1K OHM 1/4W 5%	R514000-006	2052100	.72
RES CF 1.8K OHM 1/4W 5%	R514000-007	2052300	.72
RES CF 3.3K OHM 1/4W 5%	R514000-009	2052700	.72
RES CF 4.7K OHM 1/4W 5%	R514000-011	2053100	.72
RES CF 180 OHM 1/4W 5%	R514000-012	2053300	.72

RES CF 1M OHM 1/4W 5%	R514000-014	2031500	.72
RES CF 750 OHM 1/4W 5%	R514000-015	2031700	.72
RES CF 1.2K OHM 1/4W 5%	R514000-016	2031900	.72
RES CF 100K OHM 1/4W 5%	R514000-017	2032100	.72
RES CF 51K OHM 1/4W 5%	R514000-018	2032300	.72
RES CF 22 OHM 1/4W 5%	R514000-024	2033500	.72
RES CF 47K OHM 1/4W 5%	R514000-025	2033700	.72
RES CF 150 OHM 1/4W 5%	R514000-026	2033900	.72
RES CF 10K OHM 1/4W 5%	R514000-027	2034100	.72
RES CF 200 OHM 1/4W 5%	R514000-028	2034300	.72
RES CF 33 OHM 1/4W 5%	R514000-029	2034500	.72
RES CF 100 OHM 1/4W 1%	R514000-031	2034900	.72
RES CF 51 OHM 1/4W 5%	R514000-037	2036100	.72
RES CF 22K OHM 1/4W 5%	R514000-038	2036300	.72
RES CF 27K OHM 1/4W 5%	R514000-043	2037300	.72
RES CF 47 OHM 1/4W 5%	R514000-045	2037700	.72
RES CF 2.7K OHM 1/4W 5%	R514000-048	2038300	.72
RES CF 91 OHM 1/4W 5%	R514000-049	2038500	.72
RES CF 2.2K OHM 1/4W 5%	R514000-050	2038700	.72
RES CF 3.9K OHM 1/4W 5%	R514000-051	2177400	.72
RES CF 6.8K OHM 1.4W 5%	R514000-052	2039100	.72
RES CF 30K OHM 1/4W 5%	R514000-053	2039300	.72
RES CF 56K OHM 1/4W 5%	R514000-054	2039500	.72
RES PACK 1K OHM SIP 10%	R514000-100	2040500	1.58
RES PACK 6.2K OHM SIP 10%	R514000-101	2040700	1.73
RES PACK 10K OHM SIP 5%	R514000-103	2041100	2.04
RES PACK 4.7K OHM SIP 10%	R514000-104	2041300	1.20
RES PACK 1K OHM SIP 5%	R514000-111	2042700	3.00
RES CF 510 OHM 1/2W 5%	R514003-000	2045100	.72
RES CF 220 OHM 1/2W 5%	R514003-001	2186000	.72
RES CF 390 OHM 1/2W 5%	R514003-002	2176600	.72
RES CF 820 OHM 1/2W 5%	R514003-003	2186200	.72
RES CF 1.5K OHM 1/2W 5%	R514003-004	2186300	.72
RES CF 10K OHM 1/2W 5%	R514003-005	2186400	.72
RES CF 2.2M OHM 1/2W 5%	R514003-006	2186500	.72
RES WW 0.6 OHM 2W	RC02608J	2177100	.72
POT BRIGHTNESS & VERTICAL HEIGHT	RF-07104B	2177700	1.06
POT VERTICAL LINEARITY	RF-07202B	2177800	1.06
POT VIDEO B +	RF-07473B	2177900	1.06
POT FOCUS	RV-24205B	2180100	3.86
POT CONTRAST	RV-24501B	2180200	2.77

****

TRANSFORMERS/COILS

****

TRANSFORMER; FLYBACK KFS-00093	IC-01467	2201300	55.48
TRANSFORMER; HORIZ DR HDT19	IC-01466	2201200	4.08
TRANSFORMER; POWER W/CON CRT858	IC-01465	2201100	129.24
COIL INDUCTOR 27UH .3PIE	IC-01464	2201000	1.20
COIL LINEARITY ADJUSTABLE	IC-01463	2213600	7.20
COIL LINEARITY NON ADJUSTABLE	IC-01462	2200900	5.24
COIL DEFLECTION YOKE W/CONN KYS-00060	IC-01461	2200800	31.63

MISCELLANEOUS

CRYSTAL 16MHZ OSC	I740010-090	2042800	27.00
CRYSTAL 23.814 MHZ (912/920)	M200401-001	2098600	11.11
CRYSTAL 5.7143MHZ	M200401-002	2098601	7.85
CRYSTAL 1.8432 MHZ	M200401-003	2098602	8.16
CRYSTAL 8.0000 MHZ	M200401-004	2098603	4.80
CRYSTAL 13.6080 MHZ	M200401-006	2098605	8.70
CRYSTAL 23.814 K1114A (950)	I740010-056	2035200	37.08
FUSE, 3A 125V 25EA.	FC12503A	2223700	11.85
FUSE, 1A 250V 25EA.	M200104-001	2223300	11.85
POWER ADAPTER PATTERN GEN		2176300	41.40
THERMISTER, SDT-100	3312453	2180300	1.44

MECHANICAL COMPONENTS — KEYCAPS

KEYCAP DG 1X1	20XXXXX	.72
KEYCAP DG 1X1 SCULP	20XXXXX	.72
KEYCAP DG 1X1 BLANK (25ea)*	2222100	13.50
KEYCAP DG 1X1 SCULP BLANK 0 (25ea)*	2231600	22.50
KEYCAP DG 1X1 SCULP BLANK -7 (25ea)*	2231300	22.50
KEYCAP DG 1X1 SCULP BLANK +7 (25ea)*	2231400	22.50
KEYCAP DG 1X1 SCULP BLANK +14 (25ea)*	2231500	22.50
KEYCAP DG 1X1-1/2	2072XXX	1.52
KEYCAP DG 1X1-1/2 SCULP	2084XXX	2.56
KEYCAP DG 1X1-1/2 BLANK (25ea)	2222200	33.00
KEYCAP DG 1X1-1/2 SCULP BLANK +7 (25ea)*	2231200	33.00
KEYCAP DG 1X8	2077400	1.98
KEYCAP DG 1X8 SCULP	2089700	3.00
KEYCAP LG 1X1	207XXXX	.72
KEYCAP LG 1X1 SCULP	208XXXX	.72
KEYCAP LG 1X1 BLANK (25ea)*	2222400	15.00
KEYCAP LG 1X1 SCULP BLANK 0 (25ea)*	2231100	22.50
KEYCAP LG 1X1 SCULP BLANK -7 (25ea)*	2231000	22.50
KEYCAP LG 1X1 LOW PRO	207XXXX	.72
KEYCAP LG 1X1 LOW PRO SCULP	2089XXX	.72
KEYCAP LG 1X1 LOW PRO BLANK (25ea)*	2222500	13.50
KEYCAP LG 1X1 LOW PRO SCULP BLANK (25ea)*	2223100	22.50
KEYCAP LG 1X1-1/4	2077300	1.52
KEYCAP LG 1X1-1/4 SCULP	2089600	2.44
KEYCAP LG 1X1-1/4 BLANK (25ea)*	2222600	31.50
KEYCAP LG 1X1-1/4 SCULP BLANK +7 (25ea)*	2230900	28.50
KEYCAP LG 1X1-1/2	2072XXX	1.52
KEYCAP LG 1X1-1/2 SCULP	2084XXX	2.56
KEYCAP LG 1X1-1/2 BLANK (25ea)*	2222300	33.00
KEYCAP LG 1X1-1/2 SCULP BLANK -7 (25ea)*	2230800	33.00
KEYCAP LG "L" RETURN	2077100	1.86
KEYCAP LG "L" BLANK (RETURN)	2077101	3.90
KEYCAP LG "L" SCULP RETURN	2089400	2.76
KEYCAP LG "L" SCULP BLANK (RETURN)	2161602	3.90
KEYCAP BLACK 1X1	20XXXXX	.72
KEYCAP BLACK 1X1 BLANK (25ea)*	2053700	22.50

KEYCAP BLACK 1X1-1/2		2063XXX	1.80
KEYCAP BLACK 1X1-1/2 BLANK (25ea)*		2221800	30.00
KEYCAP BLACK 1X8		2077500	2.70
KEYCAP TAN 1X1		206XXXX	.72
KEYCAP TAN 1X1 BLANK (25ea)*		2221900	18.00
KEYCAP TAN 1X1-1/2		2063700	1.80
KEYCAP TAN 1X1-1/2 BLANK (25ea)*		2222000	37.50
KEYCAP SET 910/910PLUS		2202700	52.44
KEYCAP SET 912B		2090300	52.44
KEYCAP SET 912C		2090500	52.44
KEYCAP SET 920B		2090400	63.24
KEYCAP SET 920C		2090600	56.58
KEYCAP SET 925/950		2090900	79.29
KEYCAP SET 925/950 SCULP		2091000	59.10

*BLANK KEYCAPS SOLD IN QTY 25

****

SWITCHES

****

KEYSWITCH	KS-123456	2199400	3.60
KEYSWITCH - ALPHA LOCK	KS-123457	2199500	6.22
SWITCH TOP ADJ 7 POS DIP	M200101-001	2174200	3.84
SWITCH TOP ADJ 10 POS DIP	M200101-002	2181000	3.90
SWITCH SIDE ADJ 10 POS DIP	M200101-003	2096800	5.70
PUSHBUTTON SWITCH	M200101-004	2096900	17.88
SWITCH POWER ON/OFF SPST	M200107-001	2097300	7.89
SWITCH POWER SELECT, DPDT	M200108-001	2097400	6.92

****

MISCELLANEOUS

****

CABLE ASY KEYBOARD 912/920	B510003-003	2005900	25.08
CABLE ASY KEYBOARD 910	B510003-009	2005901	25.08
CABLE ASY KEYBOARD 925/950	B510000-001	2005700	10.92
CABLE ASY MODEM RJ11	B510002-001	2135900	17.34
CONNECTOR 2 PIN RT ANGLE	M200601-006	2098703	.72
CONNECTOR 2 PIN STR WAF	M200603-002	2098800	.72
CONNECTOR 5 PIN STR WAF	M200603-005	2098802	.72
CONNECTOR 40 PIN HDR STRAIGHT	M200209-004	2098107	7.50
CONNECTOR KEYBOARD PCB 26PIN	M200601-004	2098701	4.21
CONNECTOR KEYBOARD RJ11	M200202-001	2097900	2.22
CONNECTOR RIGHT ANGLE RS232	M200201-001	2097800	10.62
CONNECTOR STRAIGHT RS232	M200201-005	2174300	20.00
CORD, POWER 6'3" 3 PRONG CONN		2109000	19.87
E-RING MINIMUM 25	CRT-010174	2223600	5.70
EQL ASY SPACE BAR DAMPER	K030500-003	2096300	.72
EQL ASY SPACE BAR, GUIDE STEM	K030500-002	2096200	.90
EQL ASY SPACE BAR, KEY GUIDE	K030500-001	2091200	1.80
EQL ASY SPACE BAR KEYGUIDE ARM	K030500-004	2096400	3.60
FUSE HOLDER, CLIP	4301512	2180400	.72
FUSE HOLDER, PANEL MOUNT	M200106-001	2097200	21.00
INSULATION PAD TRANSISTOR	M200100-002	2180800	.72
INSULATOR PAD CRYSTAL	M220000-001	2099700	1.02
KNOB, CONTRAST	CRT-010124	2153000	.72
KEYSTOPPERS 100ea	KS123458	2223800	12.00

PIVOTSHAFT MINIMUM 25	CRT-010138	2197800	4.68
SHROUD CONN 910/912/920	M400011-001	2100200	10.00
SHROUD CONN MODEM 910/912/920	M400011-002	2100201	20.00
SHROUD CONN 925/950	M400008-001	2100100	10.00
SHROUD CONN MODEM 925/950	M400008-002	2100103	20.00
SOCKET IC 14 PIN	M200301-004	2098403	.78
SOCKET IC 16 PIN	M200301-007	2098405	.72
SOCKET IC 18 PIN	M200301-001	2098400	.83
SOCKET IC 24 PIN	M200301-002	2098401	1.10
SOCKET IC 28 PIN	M200301-005	2098404	1.32
SOCKET IC 40 PIN	M200301-003	2098402	1.80
SOCKET IC 16 PIN LOW PROFILE	M200303-003	2174601	6.00

PART LIST: KEYCAPS | PART NUMBER DATE 12/09/82
MODEL: 970 DETACHABLE KEYBOARD PAGE 1 OF 4

DESCRIPTION	SCULPTURED/MATTED PRINTED	SCULPTURED/MATTED BLANK	PRINTED	BLANK	COMMENTS	NOTES
1X1 LIGHT GREY BLANK	------	2161600			0 DEGREES (1)	
1X1 LG SETUP/NOSCROLL	2088700	2161600			0 "	
1X1 LIGHT GREY F1	2085000	2161600			0 "	
1X1 LIGHT GREY F2	2085100	2161600			0 "	
1X1 LIGHT GREY F3	2085200	2161600			0 "	
1X1 LIGHT GREY F4	2085300	2161600			0 "	
1X1 LIGHT GREY F5	2085400	2161600			0 "	
1X1 LIGHT GREY F6	2085500	2161600			0 "	
1X1 LIGHT GREY F7	2085600	2161600			0 "	
1X1 LIGHT GREY F8	2085700	2161600			0 "	
1X1 LIGHT GREY F9	2085800	2161600			0 "	
1X1 LIGHT GREY F10	2085900	2161600			0 "	
1X1 LIGHT GREY F11	2086000	2161600			0 "	
1X1 LIGHT GREY F12	2087600	2161600			0 "	
1X1 LIGHT GREY F13	2087700	2161600			0 "	
1X1 LIGHT GREY F14	2087900	2161600			0 "	
1X1 LIGHT GREY F15	2087800	2161600			0 "	
1X1 LIGHT GREY F16	2088000	2161600			0 "	
1X1 LG CHAR INSERT	2086100	2161600			0 "	
1X1 LG CHAR DELETE	2086200	2161600			0 "	
1X1 LG LINE INSERT	2086300	2161600			0 "	
1X1 LG LINE DELETE	2086400	2161600			0 "	
1X1 DARK GREY BLANK	-------	2161700			+14 DEGREES	
1X1 DG LOC ESC/ESC	2084200	2161700			+14 "	
1X1 DARK GREY 1/!	2077800	2161700			+14 "	(2)
1X1 DARK GREY 2/@	2077900	2161700			+14 "	
1X1 DARK GREY 3/#	2078000	2161700			+14 "	
1X1 DARK GREY 4/$	2078100	2161700			+14 "	
1X1 DARK GREY 5/%	2078200	2161700			+14 "	
1X1 DARK GREY 6/	2078300	2161700			+14 "	
1X1 DARK GREY 7/&	2078400	2161700			+14 "	
1X1 DARK GREY 8/*	2078500	2161700			+14 "	
1X1 DARK GREY 9/(	2078600	2161700			+14 "	
1X1 DARK GREY 0/)	2078700	2161700			+14 "	
1X1 DARK GREY -/_	2078800	2161700			+14 "	
1X1 DARK GREY =/+	2078900	2161700			+14 "	

PARTLIST: KEYCAPS — PART NUMBER — DATE 12/09/82
MODEL: 970 DETACHABLE KEYBOARD — PAGE 2 OF 4

DESCRIPTION	SCULPTURED/MATTED KEYCAP PRINTED	SCULPTURED/MATTED KEYCAP BLANK	PRINTED	BLANK	COMMENTS	NOTES
1X1 DARK GREY `/~	2230100	2161700			+14	"
1X1 DARK GREY \/|	2079100	2161700			+14	"
1X1 DG BACK SPACE	2079200	2161700			+14	"
1X1-1/2 DARK GREY TAB	2084500	2161801			+7	"
1X1 DARK GREY Q	2080600	2161800			+7	"
1X1 DARK GREY W	2080700	2161800			+7	"
1X1 DARK GREY E	2080800	2161800			+7	"
1X1 DARK GREY R	2080900	2161800			+7	"
1X1 DARK GREY T	2081000	2161800			+7	DEGREES
1X1 DARK GREY Y	2081100	2161800			+7	"
1X1 DARK GREY U	2081200	2161800			+7	"
1X1 DARK GREY I	2081300	2161800			+7	"
1X1 DARK GREY O	2081400	2161800			+7	"
1X1 DARK GREY P	2081500	2161800			+7	"
1X1 DARK GREY[/]	2081600	2161800			+7	"
1X1-1/2 DG LINE FEED	2084400	2161801			+7	"
1X1-1/4 LG CLEAR SPACE	2088400	2161802			+7	"
1X1 LIGHT GREY CONTROL	2086900	2161600			0	DEGREES
1X1 DARK GREY ALPHA LOCK	2081800	2161601			0	"
1X1 DARK GREY A	2081900	2161601			0	"
1X1 DARK GREY S	2082000	2161601			0	"
1X1 DARK GREY D	2082100	2161601			0	"
1X1 DARK GREY F	2082200	2161601			0	"
1X1 DARK GREY G	2082300	2161601			0	"
1X1 DARK GREY H	2082400	2161601			0	"
1X1 DARK GREY J	2082500	2161601			0	"
1X1 DARK GREY K	2082600	2161601			0	"
1X1 DARK GREY L	2082700	2161601			0	"
1X1 DARK GREY ;/:	2082800	2161601			0	"
1X1 DARK GREY '/"	2082900	2161601			0	"
LIGHT GREY "L" RETURN	2089400	2161602			0	"
1X1 LIGHT GREY BREAK	2087000	2162101			0	"
1X1 DARK GREY BACK TAB	2081700	2161900			-7	"
1X1-1/2 LG SHIFT	2084700	2161902			-7	"
1X1 DARK GREY Z	2083000	2161900			-7	"

PARTLIST: KEYCAPS — PART NUMBER — DATE 12/09/82

MODEL: 970 DETACHABLE KEYBOARD — PAGE 3 OF 4

DESCRIPTION	SCULPTURED/MATTED KEYCAP PRINTED	SCULPTURED/MATTED KEYCAP BLANK	PRINTED	BLANK	COMMENTS	NOTES
1X1 DARK GREY X	2083100	2161900			-7 "	
1X1 DARK GREY C	2083200	2161900			-7 "	
1X1 DARK GREY V	2083300	2161900			-7 "	
1X1 DARK GREY B	2083400	2161900			-7 "	
1X1 DARK GREY N	2083500	2161900			-7 "	
1X1 DARK GREY M	2083600	2161900			-7 "	
1X1 DARK GREY ,/<	2083700	2161900			-7 "	
1X1 DARK GREY ./>	2083800	2161900			-7 "	
1X1 DARK GREY //?	2083900	2161900			-7 "	
1X1 DARK GREY {/}	2084000	2161900			-7 DEGREES	
1X1 LIGHT GREY DEL	2087100	2161901			-7 "	
1X1 LG PRINT (LP)	2089300	2162101			0 "	(3)
1X1 LG FUNCTION (LP)	2089000	2162101			0 "	(3)
1X8 DARK GREY SPACE BAR	2089700	-------			0 "	
1X1 LG HOME (LP)	2089100	2162101			0 "	(3)
1X1 LG CURSER (LP)	2140500	2162101			0 "	(3) (4)
1X1 LG LINE ERASE	2086500	2161600			0 "	
1X1 LG PAGE ERASE	2086600	2161600			0 "	
1X1 LIGHT GREY SEND	2088500	2161600			0 "	
1X1 DARK GREY 7	2079900	2161601			0 "	
1X1 DARK GREY 8	2080000	2161601			0 "	
1X1 DARK GREY 9	2080100	2161601			0 "	
1X1 DARK GREY 4	2079600	2161601			0 "	
1X1 DARK GREY 5	2079700	2161601			0 "	
1X1 DARK GREY 6	2079800	2161601			0 "	
1X1 DARK GREY 1	2079300	2161601			0 "	
1X1 DARK GREY 2	2079400	2161601			0 "	
1X1 DARK GREY 3	2079500	2161601			0 "	
1X1 DARK GREY ,	2080400	2161601			0 "	
1X2 DARK GREY 0	2088100	2251300			0 "	
1X1 DARK GREY .	2080500	2161601			0 "	
1X1 DARK GREY -	2080300	2161601			0 "	
1X1 DARK GREY PAGE	2087200	2161601			0 "	
1X1 DARK GREY CE	2087300	2161601			0 "	

PART LIST: KEYCAPS — PART NUMBER — DATE 12/09/82
MODEL: 970 DETACHABLE KEYBOARD — PAGE 4 OF 4

DESCRIPTION	SCULPTURED/MATTED KEYCAP PRINTED	SCULPTURED/MATTED KEYCAP BLANK	PRINTED	BLANK	COMMENTS	NOTES
1X1 DARK GREY RESET	2087400	2161601			0 DEGREES	
2x1 LIGHT GREY TAB	2088200	2251400			0 "	
2x1 LIGHT GREY ENTER	2088300	2251400			0 "	
1X1 DARK GREY 00	2180700	2161601			0 "	

NOTES

1) DEGREES REFER TO SCULPTURED/MATTED KEYCAPS ONLY
2) SLASH BETWEEN TWO CHARACTERS (ie: 1/!) FOR CLARITY AND IS NOT PRINTED ON KEYCAP
3) LOW PROFILE KEYS
4) SAME KEY CAN BE USED FOR ALL FOUR CURSER POSITIONS

PART LIST: KEYCAPS — PART NUMBER — DATE 11/15/82

MODEL: 925 DETACHABLE KEYBOARD
950 DETACHABLE KEYBOARD

DESCRIPTION	STEPPED KEYCAPS PRINTED	STEPPED KEYCAPS BLANK	SCULPTURED/MATTED KEYCAPS PRINTED	SCULPTURED/MATTED KEYCAPS BLANK	COMMENTS/NOTES
1X1 LIGHT GREY BLANK	-------	2073000	-------	2161600	0 DEGREES (1)
1X1 LG NO SCROLL/SETUP	2075500	2073000	2088700	2161600	0 "
1X1 LIGHT GREY F1	2073100	2073000	2085000	2161600	0 "
1X1 LIGHT GREY F2	2073200	2073000	2085100	2161600	0 "
1X1 LIGHT GREY F3	2073300	2073000	2085200	2161600	0 "
1X1 LIGHT GREY F4	2073400	2073000	2085300	2161600	0 "
1X1 LIGHT GREY F5	2073500	2073000	2085400	2161600	0 "
1X1 LIGHT GREY F6	2073600	2073000	2085500	2161600	0 "
1X1 LIGHT GREY F7	2073700	2073000	2085600	2161600	0 "
1X1 LIGHT GREY F8	2073800	2073000	2085700	2161600	0 "
1X1 LIGHT GREY F9	2073900	2073000	2085800	2161600	0 "
1X1 LIGHT GREY F10	2074000	2073000	2085900	2161600	0 "
1X1 LIGHT GREY F11	2074100	2073000	2086000	2161600	0 "
1X1 LG CHAR INSERT	2074200	2073000	2086100	2161600	0 "
1X1 LG CHAR DELETE	2074300	2073000	2086200	2161600	0 "
1X1 LG LINE INSERT	2074400	2073000	2086300	2161600	0 "
1X1 LG LINE DELETE	2074500	2073000	2086400	2161600	0 "
1X1 DARK GREY BLANK	-------	2065800	-------	2161700	+14 DEGREES
1X1 DG ESC/LOC ESC	2072300	2065800	2084200	2161700	+14 "
1X1 DARK GREY 1/!	2065900	2065800	2077800	2161700	+14 " (2)
1X1 DARK GREY 2/@	2066000	2065800	2077900	2161700	+14 "
1X1 DARK GREY 3/#	2066100	2065800	2078000	2161700	+14 "
1X1 DARK GREY 4/$	2066200	2065800	2078100	2161700	+14 "
1X1 DARK GREY 5/%	2066300	2065800	2078200	2161700	+14 "
1X1 DARK GREY 6/^	2066400	2065800	2078300	2161700	+14 "
1X1 DARK GREY 7/&	2066500	2065800	2078400	2161700	+14 "
1X1 DARK GREY 8/*	2066600	2065800	2078500	2161700	+14 "
1X1 DARK GREY 9/(	2066700	2065800	2078600	2161700	+14 "
1X1 DARK GREY 0/)	2066800	2065800	2078700	2161700	+14 "
1X1 DARK GREY -/_	2066900	2065800	2078800	2161700	+14 "
1X1 DARK GREY =/+	2067000	2065800	2078900	2161700	+14 "
1X1 DARK GREY `/~	2067100	2065800	2079000	2161700	+14 "
1X1 DARK GREY \/|	2067200	2065800	2079100	2161700	+14 "
1X1 DG BACK SPACE	2067300	2065800	2079200	2161700	+14 "
1X1-1/2 DARK GREY TAB	2072600	2072400	2084500	2161801	+7 "
1X1 DARK GREY Q	2068700	2065800	2080600	2161800	+7 "
1X1 DARK GREY W	2068800	2065800	2080700	2161800	+7 "
1X1 DARK GREY E	2068900	2065800	2080800	2161800	+7 "
1X1 DARK GREY R	2069000	2065800	2080900	2161800	+7 "

PAR. IST: KEYCAPS PART NUMB DATE 11/15/82
MODEL: 925 DETACHABLE KEYBOARD PAGE 2 OF 3
950 DETACHABLE KEYBOARD

DESCRIPTION	STEPPED KEYCAPS PRINTED	STEPPED KEYCAPS BLANK	SCULPTURED/MATTED KEYCAPS PRINTED	SCULPTURED/MATTED KEYCAPS BLANK	COMMENTS/NOTES
1X1 DARK GREY T	2069100	2065800	2081000	2161800	+7 DEGREES
1X1 DARK GREY Y	2069200	2065800	2081100	2161800	+7 "
1X1 DARK GREY U	2069300	2065800	2081200	2161800	+7 "
1X1 DARK GREY I	2069400	2065800	2081300	2161800	+7 "
1X1 DARK GREY O	2069500	2065800	2081400	2161800	+7 "
1X1 DARK GREY P	2069600	2065800	2081500	2161800	+7 "
1X1 DARK GREY [/]	2069700	2065800	2081600	2161800	+7 "
1X1-1/2 DG LINE FEED	2072500	2072400	2084400	2161801	+7 "
1X1-1/4 LG CLEAR SPACE	2077300	2077200	2089600	2161802	+7 "
1X1 LIGHT GREY CTRL	2075000	2073000	2086900	2161600	0 DEGREES
1X1 DARK GREY ALPHA LOCK	2069900	2065800	2081800	2161601	0 "
1X1 DARK GREY A	2070000	2065800	2081900	2161601	0 "
1X1 DARK GREY S	2070100	2065800	2082000	2161601	0 "
1X1 DARK GREY D	2070200	2065800	2082100	2161601	0 "
1X1 DARK GREY F	2070300	2065800	2082200	2161601	0 "
1X1 DARK GREY G	2070400	2065800	2082300	2161601	0 "
1X1 DARK GREY H	2070500	2065800	2082400	2161601	0 "
1X1 DARK GREY J	2070600	2065800	2082500	2161601	0 "
1X1 DARK GREY K	2070700	2065800	2082600	2161601	0 "
1X1 DARK GREY L	2070800	2065800	2082700	2161601	0 "
1X1 DARK GREY ;/:	2070900	2065800	2082800	2161601	0 "
1X1 DARK GREY '/"	2071000	2065800	2082900	2161601	0 "
LIGHT GREY "L" RETURN	2077100	2077101	2089400	2161602	0 "
1X1 LIGHT GREY BREAK	2075100	2073000	2087000	2161600	0 "
1X1 DARK GREY BACK TAB	2069800	2065800	2081700	2161900	-7 "
1X1-1/2 LG SHIFT	2072800	2072700	2084700	2161902	-7 "
1X1 DARK GREY Z	2071100	2065800	2083000	2161900	-7 "
1X1 DARK GREY X	2071200	2065800	2083100	2161900	-7 "
1X1 DARK GREY C	2071300	2065800	2083200	2161900	-7 "
1X1 DARK GREY V	2071400	2065800	2083300	2161900	-7 "
1X1 DARK GREY B	2071500	2065800	2083400	2161900	-7 "
1X1 DARK GREY N	2071600	2065800	2083500	2161900	-7 "
1X1 DARK GREY M	2071700	2065800	2083600	2161900	-7 "
1X1 DARK GREY ,/<	2071800	2065800	2083700	2161900	-7 "
1X1 DARK GREY ./>	2071900	2065800	2083800	2161900	-7 "
1X1 DARK GREY //?	2072000	2065800	2083900	2161900	-7 "

PA LIST: KEYCAPS PART NUMBER DATE 11/15/82

MODEL: 925 DETACHABLE KEYBOARD
        950 DETACHABLE KEYBOARD

DESCRIPTION	STEPPED KEYCAPS PRINTED	STEPPED KEYCAPS BLANK	SCULPTURED/MATTED KEYCAPS PRINTED	SCULPTURED/MATTED KEYCAPS BLANK	COMMENTS/NOTES
1X1 DARK GREY {/}	2072100	2065800	2084000	2161900	-7 DEGREES
1X1 LIGHT GREY DEL	2075200	2073000	2087100	2161901	-7 "
1X1 LG PRINT (LP)	2077000	2076500	2089300	2162101	0 " (3)
1X1 LG FUNCT (LP)	2076700	2076500	2089000	2162101	0 " (3)
1X8 DARK GREY SPACE BAR	2077400	-------	2089700	-------	0 "
1X1 LG HOME (LP)	2076800	2076500	2089100	2162101	0 " (3)
1X1 LG CURSER (LP)	2076900	2076500	2140500	2162101	0 " (3)(4)
1X1 LG LINE ERASE	2074600	2073000	2086500	2161600	0 "
1X1 LG PAGE ERASE	2074700	2073000	2086600	2161600	0 "
1X1 LIGHT GREY SEND	2075300	2073000	2088500	2161600	0 "
1X1 DARK GREY 7	2068000	2065800	2079900	2161601	0 "
1X1 DARK GREY 8	2068100	2065800	2080000	2161601	0 "
1X1 DARK GREY 9	2068200	2065800	2080100	2161601	0 "
1X1 DARK GREY 4	2067700	2065800	2079600	2161601	0 "
1X1 DARK GREY 5	2067800	2065800	2079700	2161601	0 "
1X1 DARK GREY 6	2067900	2065800	2079800	2161601	0 "
1X1 DARK GREY 1	2067400	2065800	2079300	2161601	0 "
1X1 DARK GREY 2	2067500	2065800	2079400	2161601	0 "
1X1 DARK GREY 3	2067600	2065800	2079500	2161601	0 "
1X1 DARK GREY ,	2068500	2065800	2080400	2161601	0 "
1X1 DARK GREY 0	2068300	2065800	2080200	2161601	0 "
1X1 DARK GREY .	2068600	2065800	2080500	2161601	0 "
1X1-1/2 LG ENTER	2072900	2072700	2084800	2162103	0 "
1X1 DARK GREY -	2068400	2065800	2080300	2161601	0 "

NOTES:

1) DEGREES REFER TO SCULPTURED/MATTED KEYCAPS ONLY
2) SLASH BETWEEN TWO CHARACTERS (ie: 1/!) IS FOR CLARITY AND IS NOT PRINTED ON KEYCAP
3) LOW PROFILE KEYCAPS
4) SAME KEYCAP CAN BE USED FOR ALL FOUR CURSER POSITIONS

PART LIST: KEYCAPS | PART NUMBER DATE 11/10/82

MODEL: 910/910PLUS KEYBOARD PAGE 1 OF 3

912C/920C KEYBOARD

DESCRIPTION	910/910PLUS PRINTED	912C/920C PRINTED	BLANK	COMMENTS
1X1 LIGHT GREY BLANK	-------	-------	2073000	
1X1 LIGHT GREY F1	-------	2073100	2073000	(1)
1X1 LIGHT GREY F2	-------	2073200	2073000	(1)
1X1 LIGHT GREY F3	-------	2073300	2073000	(1)
1X1 LIGHT GREY F4	-------	2073400	2073000	(1)
1X1 LIGHT GREY F5	-------	2073500	2073000	(1)
1X1 LIGHT GREY F6	-------	2073600	2073000	(1)
1X1 LIGHT GREY F7	-------	2073700	2073000	(1)
1X1 LIGHT GREY F8	-------	2073800	2073000	(1)
1X1 LIGHT GREY F9	-------	2073900	2073000	(1)
1X1 LIGHT GREY F10	-------	2074000	2073000	(1)
1X1 LIGHT GREY F11	-------	2074100	2073000	(1)
1X1 LG CHAR INSERT	-------	2074200	2073000	(1)
1X1 LG CHAR DELETE	-------	2074300	2073000	(1)
1X1 LG LINE DELETE	-------	2074400	2073000	(1)
1X1 LG LINE DELETE	-------	2074500	2073000	(1)
1X1 DARK GREY BLANK	-------	-------	2065800	
1X1 DARK GREY ESC	2072200	2072200	2065800	
1X1 DARK GREY 1/!	2065900	2065900	2065800	(2)
1X1 DARK GREY 2/@	2066000	2066000	2065800	
1X1 DARK GREY 3/#	2066100	2066100	2065800	
1X1 DARK GREY 4/$	2066200	2066200	2065800	
1X1 DARK GREY 5/%	2066300	2066300	2065800	
1X1 DARK GREY 6/^	2066400	2066400	2065800	
1X1 DARK GREY 7/&	2066500	2066500	2065800	
1X1 DARK GREY 8/*	2066600	2066600	2065800	
1X1 DARK GREY 9/(	2066700	2066700	2065800	
1X1 DARK GREY 0/)	2066800	2066800	2065800	
1X1 DARK GREY -/_	2066900	2066900	2065800	
1X1 DARK GREY =/+	2067000	2067000	2065800	
1X1 DARK GREY `/~	2067100	2067100	2065800	
1X1 DARK GREY \/|	2067200	2067200	2065800	
1X1 DG BACK SPACE	2067300	2067300	2065800	
1X1-1/2 DARK GREY TAB	2072600	2072600	2072400	
1X1 DARK GREY Q	2068700	2068700	2065800	
1X1 DARK GREY W	2068800	2068800	2065800	
1X1 DARK GREY E	2068900	2068900	2065800	
1X1 DARK GREY R	2069000	2069000	2065800	
1X1 DARK GREY T	2069100	2069100	2065800	
1X1 DARK GREY Y	2069200	2069200	2065800	
1X1 DARK GREY U	2069300	2069300	2065800	
1X1 DARK GREY I	2069400	2069400	2065800	

PARTLIST: KEYCAPS — PART NUMBER — DATE 11/10/82

MODEL: 910/910PLUS KEYBOARD
912C/920C KEYBOARD

DESCRIPTION	910/910PLUS PRINTED	912C/920C PRINTED	BLANK	COMMENTS
1X1 DARK GREY O	2069500	2069500	2065800	
1X1 DARK GREY P	2069600	2069600	2065800	
1X1 DARK GREY[/]	2069700	2069700	2065800	
1X1-1/2 DG LINE FEED	2072500	2072500	2072400	
1X1-1/4 LG CLEAR SPACE	2077300	2077300	2077200	
1X1 LIGHT GREY CTRL	2075000	2075000	2073000	
1X1 DG ALPHA LOCK	2069900	2069900	2073000	
1X1 DARK GREY A	2070000	2070000	2065800	
1X1 DARK GREY S	2070100	2070100	2065800	
1X1 DARK GREY D	2070200	2070200	2065800	
1X1 DARK GREY F	2070300	2070300	2065800	
1X1 DARK GREY G	2070400	2070400	2065800	
1X1 DARK GREY H	2070500	2070500	2065800	
1X1 DARK GREY J	2070600	2070600	2065800	
1X1 DARK GREY K	2070700	2070700	2065800	
1X1 DARK GREY L	2070800	2070800	2065800	
1X1 DARK GREY ;/:	2070900	2070900	2065800	
1X1 DARK GREY '/"	2071000	2071000	2065800	
LIGHT GREY "L" RETURN	2077100	2077100	2077101	
1X1 LIGHT GREY BREAK	2075100	2075100	2073000	
1X1 DARK GREY BACK TAB	2069800	2069800	2065800	
1X1-1/2 LG SHIFT	2072800	2072800	2072700	
1X1 DARK GREY Z	2071100	2071100	2065800	
1X1 DARK GREY X	2071200	2071200	2065800	
1X1 DARK GREY C	2071300	2071300	2065800	
1X1 DARK GREY V	2071400	2071400	2065800	
1X1 DARK GREY B	2071500	2071500	2065800	
1X1 DARK GREY N	2071600	2071600	2065800	
1X1 DARK GREY M	2071700	2071700	2065800	
1X1 DARK GREY ,/<	2071800	2071800	2065800	
1X1 DARK GREY ./>	2071900	2071900	2065800	
1X1 DARK GREY //?	2072000	2072000	2065800	
1X1 DARK GREY {/}	2072100	2072100	2065800	
1X1 LIGHT GREY DEL	2075200	2075200	2073000	
1X1 LIGHT GREY PRINT(LP)	2077000	-------	2076500	(3)
1X1 LG CONV/BLOCK (LP)	-------	2076600	2076500	(3)
1X1 LG FUNCT (LP)	2076700	2076700	2076500	(3)
1X8 DARK GREY SPACE BAR	2077400	2077400	-------	
1X1 LG HOME (LP)	2076800	2076800	2076500	(3)
1X1 LG CURSER (LP)	2076900	2076900	2076500	(3)(4)
1X1 LG LINE ERASE	-------	2074600	2073000	(1)
1X1 LG PAGE ERASE	-------	2074700	2073000	(1)
1X1 LG SEND LING	-------	2075300	2073000	(1)
1X1 LG SEND PAGE	-------	2074900	2073000	(1)
1X1 DARK GREY 7	2068000	2068000	2065800	
1X1 DARK GREY 8	2068100	2068100	2065800	
1X1 DARK GREY 9	2068200	2068200	2065800	
1X1 DARK GREY 4	2067700	2067700	2065800	

PARTLIST: KEYCAPS PART NUMBER DATE 11/10/82
MODEL: 910/910PLUS KEYBOARD PAGE 3 OF 3
912C/920C KEYBOARD

DESCRIPTION	910/910PLUS PRINTED	912C/920C PRINTED	BLANK	COMMENTS
1X1 DARK GREY 5	2067800	2067800	2065800	
1X1 DARK GREY 6	2067900	2067900	2065800	
1X1 DARK GREY 1	2067400	2067400	2065800	
1X1 DARK GREY 2	2067500	2067500	2065800	
1X1 DARK GREY 3	2067600	2067600	2065800	
1X1 DARK GREY ,	2068500	2068500	2065800	
1X1 DARK GREY 0	2068300	2068300	2065800	
1X1 DARK GREY .	2068600	2068600	2065800	
1X1-1/2 LG ENTER	2072900	2072900	2072700	
1X1 DARK GREY -	2068400	2068400	2065800	

1)KEYCAPS ARE FOR 920C KEYBOARD ONLY.
2)SLASH BETWEEN TWO CHARACTERS (ie: 1/!)IS FOR CLARITY AND IS NOT PRINTED ON KEYCAP
3)LOW PROFILE KEYCAPS
4)SAME KEYCAPS CAN BE USED FOR ALL FOUR CURSER POSITIONS

SPARE PART KITS

The following are the terminal spare part kits available through TeleVideo Systems, Inc. Each model terminal has been designated the following spare part kits:

A) Main Logic
B) Power supply/Video module
C) Mechanical components
D) Additional parts

The suggested stocking levels have been identified as follows:

For the first 50 terminals lea of kits A, B, C, & D are suggested.
For the next 50 terminals add lea of kits A, & B
For the next 50 terminals add lea of kits A, B, C, & D
For the next 50 terminals add lea of kits A, & B

The list price of the spare part kits (as shown on the Terminal Spare Parts Price List) reflect a 25% discount, if the items were purchased seperately.

*Attached are the kits currently available through TeleVideo.

SPARE PARTS KIT DATE___02/10/83___
MODEL: 910 TTL
LOGIC BOARD
PART NUMBER: 2000600

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035800	IC 2114 RAM
2036200	IC 74LS245/N8T245N
2049600	IC 6502A 2MHz CPU
2051800	IC KYBD ENCODER 910/910PLUS
2052800	IC SY6545A-1 2MHz CRTC
2053000	IC SY6551A-1 2MHz UART
8000020	IC EPROM SYS PROG 910
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 910 GATE ARRAY
LOGIC BOARD
PART NUMBER: 2225400

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035800	IC 2114 RAM
2036200	IC 74LS245/N8T245N
2049600	IC 6502A 2MHz CPU
2051800	IC KYBD ENCDR 910/910PLUS
2052800	IC SY6545A-1 2MHz CRTC
2053000	IC SY6551A-1 2MHz UART
8000020	IC EPROM SYS PROG 910
2057400	IC GATE ARRAY 910/925
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 910PLUS TTL
LOGIC BOARD
PART NUMBER: 2000800

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035800	IC 2114 RAM
2036200	IC 74LS245/N8T245N
2049600	IC 6502A 2MHz CPU
2051800	IC KYBD ENCDR 910/910PLUS
2052800	IC SY6545A-1 2MHz CRTC
2053000	IC SY6551A-1 2MHz UART
8000040	IC EPROM SYS PROG 910PLUS
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 910PLUS GATE ARRAY
LOGIC BOARD
PART NUMBER: 2225500

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035800	IC 2114 RAM
2036200	IC 74LS245/N8T245N
2049600	IC 6502A 2MHz CPU
2051800	IC KYBD ENCDR 910/910PLUS
2052800	IC SY6545A-1 2MHz CRTC
2053000	IC SY6551A-1 2MHz UART
8000040	IC EPROM SYS PROG 910PLUS
2057400	IC GATE ARRAY 910/925
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 912C/920C TTL
LOGIC BOARD
PART NUMBER: 2000000

PART #	DESCRIPTION
2026600	IC 74LS74
2027400	IC 74LS157
2028400	IC 74LS253
2029200	IC 1488/75188N
2029400	IC 75189AN/1489
2030800	IC 2502HP UART
2031000	IC TMS 9927/5027 CRTC
2031200	IC P8035 CPU
2034000	IC SYSTEM ROM 912/920C A49C1
2035800	IC 2114 RAM
2098600	XTAL 23.814 MHz CRYSTAL (912/920)
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 925 GATE ARRAY
LOGIC BOARD
PART NUMBER: 2225300

PART #	DESCRIPTION
2029000	IC 74LS374
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035800	IC 2114 RAM
2049600	IC 6502A 2MHz CPU
2052800	IC SY6545A-1 2MHz CRTC
2053000	IC SY6551A-1 2MHz UART
8000031	IC EPROM SYS PROG (A50)
8000033	IC EPROM SYS PROG (A49)
2057400	IC GATE ARRAY 910/925
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 925 TTL
LOGIC BOARD
PART NUMBER: 2001000

PART #	DESCRIPTION
2029000	IC 74LS374
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035800	IC 2114 RAM
2049600	IC 6502A CPU
2052800	IC SY6545A-1 2MHz CRTC
2053000	IC SY6551A-1 2MHz UART
8000031	IC EPROM SYS PROG 925 (A50)
8000033	IC EPROM SYS PROG 925 (A49)
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 950 TTL
LOGIC BOARD
PART NUMBER: 2000400

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035200	CRY K1114A 23.814 MHz (950)
2035800	IC 2114 RAM
2049600	IC 6502A CPU
2049800	IC 6545 CRTC
2155700	IC 6551 UART
2050200	IC 6522A VIA
8000043	IC EPROM SYS PROG 950 (A41)
8000044	IC EPROM SYS PROG 950 (A42)
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 950 GATE ARRAY
LOGIC BOARD
PART NUMBER: 2233000

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035200	CRY K1114A 23.814MHz (950)
2049600	IC 6502A CPU
2049800	IC 6545 CRTC
2155700	IC 6551 UART
2050200	IC 6552A VIA
8000043	IC EPROM SYS PROG 950 (A25)
8000044	IC EPROM SYS PROG 950 A20)
2057600	IC GATE ARRAY 950 A (A34)
2057800	IC GATE ARRAY 950 B (A37)
2049200	IC 6116 RAM 150ns
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 910/910PLUS
MECHANICAL
PART NUMBER: 2000900

PART #	DESCRIPTION
2005901	CABLE ASY KEYBOARD 910/910PLUS
2223700	FUSE 3A 125V (25EA)
2223300	FUSE 1A 250V (25EA)
2199400	KEYSWITCH (3ea)
2096800	SWITCH, SIDE ADJ 10 POS DIP
2097300	SWITCH, POWER ON/OFF SPST
2097800	CONNECTOR RIGHT ANGLE RS232
2100200	SHROUD, CONN 910/912/920
2180200	POT, CONTRAST

SPARE PARTS KIT
MODEL: 912/920
MECHANICAL
PART NUMBER: 2000200

DATE___02/10/83___

PART #	DESCRIPTION
2005900	CABLE ASY, KEYBOARD 912/920
2223700	FUSE, 3A/125V (25ea)
2223300	FUSE, 1A/250V (25ea)
2199400	KEYSWITCH (3ea)
2174200	SWITCH, TOP ADJ. 7 POS. DIP
2181000	SWITCH, TOP ADJ. 10 POS DIP
2096800	SWITCH, SIDE ADJ. 10 POS DIP.
2097300	SWITCH, POWER ON/OFF SPST
2097800	CONNECTOR RIGHT ANGLE RS232
2100200	SHROUD CONN 910/912/920
2180200	POT, CONTRAST

SPARE PARTS KIT
MODEL: 925/950
MECHANICAL
PART NUMBER: 2000500

DATE___02/10/83___

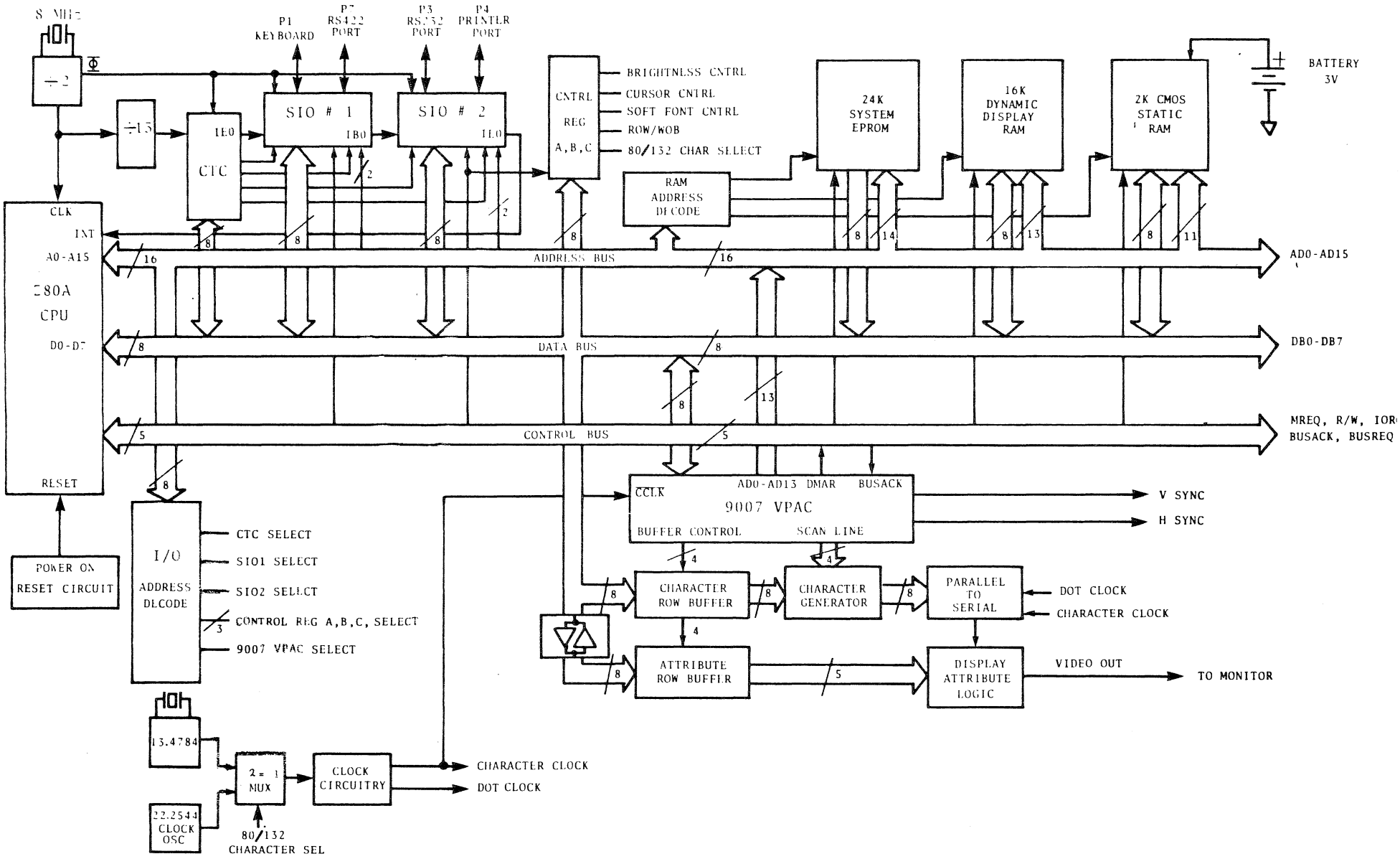
PART #	DESCRIPTION
2005700	CABLE ASY KEYBOARD 925/950
2223700	FUSE 3A 125V (25EA)
2223300	FUSE 1A 250V (25EA)
2199400	KEYSWITCH (3EA)
2096800	SWITCH SIDE ADJ 10 POS DIP
2097300	SWITCH POWER ON/OFF SPST
2097800	CONNECTOR RIGHT ANGLE RS232
2097900	CONNECTOR KEYBOARD RJ11
2100100	SHROUD, CONNECTOR 925/950
2180200	POT, CONTRAST

SPARE PARTS KIT: DATE___02/10/83___
MODEL: 910/910PLUS
912/920 925/950
POWER SUPPLY & VIDEO MODULE
PART NUMBER: 2000100

PART #	DESCRIPTION
2197300	CAP MYLAR, .1UF/600V (C504)
2199300	CAP ELECTROLYTIC 220UF (C305)
2200800	DEFLECTION YOKE W/CONN KYS-00060 (L202)
2201000	COIL INDUCTOR 27UH .3PIE (L302)
2213600	COIL LINEARITY ADJUSTABLE (L201)
2200900	COIL LINEARITY 5.4UH NON ADJUSTABLE (L201)
2200600	DIODE IN5391/DS135D (2ea)
2201500	DIODE DSA17C/MR500 (4ea)
2201600	DIODE, ZENER IN759A/RD12EB (D112)
2126800	REGULATOR, LAS1605 2A/5V (IC2)
2126900	REGULATOR, LAS16CB 2A/13.8V (IC1)
2176600	RESISTOR, CF 390 ohm 1/2w 5% (R102)
2201200	TRANSFORMER HORIZ DR HDT19 (T301)
2201300	TNFR FLYBACK KFS-00093 (T302)
2045500	TRANSISTOR 2N4401/2SC1166 (Q301)
2047100	TRANSISTOR 2N5551/2SC983 (Q103/Q105)
2047300	TRANSISTOR 2SC2233/MJE13006 (Q302)
2046700	TRANSISTOR KTC1627A/MPSA06 (Q102)
2280000	CAP NON POLARIZED 16uf/25V (C306)
2177700	POT 100K BRIGHT/VERT HEIGHT (SFR1/SFR4)
2177800	POT 2K VERT LINEARITY (SFR2)
2177900	POT 5K B+ 75VOLT ADJUST (SFR3)

SPARE PART KITS DATE___02/10/83___
MODEL: ALL
ADDITIONAL PARTS
PART NUMBER: 2000300

PART #	DESCRIPTION
2024000	IC 74S00
2024200	74LS00
2024400	74LS03
2024600	74S04
2024800	74LS04
2025000	74LS05
2025200	74LS08
2025400	74LS10
2025600	74LS20
2025800	74LS32
2026000	74LS42
2026200	74LS51
2026600	74LS74
2138500	74LS112
2027400	74LS157
2027600	74LS163
2048200	74LS164
2027800	74LS166
2028000	74LS173
2028200	74LS174
2044200	74LS244
2138600	74LS251
2028400	74LS253
2028600	74LS367
2028800	74LS373
2029000	74LS374
2030200	NE555
2030400	DP 8304
2030600	AMD2111-4A
2044200	74LS244
2030900	CAP CERAMIC 1.0pf 1KV SPARK GAP
2047500	DIODE, IN914
2201700	DIODE DS 113A/MRI-1000
2201800	DIODE, IN920/KDS8513A
2202200	DIODE, IN4004/DS13OTB
2180100	POT FOCUS 2M ohm
2177100	RESISTOR 0.6ohm WW 2W
2041300	RESISTOR PAC 4.7K ohm
2040700	RESISTOR PAC 6.2K ohm
2152800	SPEAKER 8ohm W/CONN
2097400	SWITCH, POWER SELECT, DPDT
2180300	THERMISTER, SDT-100
2201100	TRNF, POWER W/CONN (910/920/925/950)
2225600	TRNF, POWER W/CONN (970 ONLY)
2199700	TRANS 2N6121/25C1173
2202100	TRANS 2N6124/25A473



970 FUNCTIONAL BLOCK DIAGRAM

4-1

Overview

The terminal is controlled by a Z80 microprocessor operating at a clock speed of 4.0Mhz. The Z80 can address all 64K memory and refreshes the dynamic RAM via the built in dynamic memory refresh counter during one M1 cycle.

4-2

Display Fundamentals

The SMC 9007 video processor/controller is the heart of the display unit. It has 14 address lines and can address up to 16k of video memory. The chip has a row-table addressing mode and each data row on the screen has its own starting address. A row table exists in memory which contains the starting address of each data row. For a screen with 26 data rows the row table will consist of 26 14 bit address each pointing to the first character position of its respective data row.

The controller is programmed to handle 26 rows by 80 or 132 columns. A Double Row Buffer (DRB) allows the buffer be loaded at a slower speed while the other buffer is displaying at screen painting speed. This is especially important in attribute assembly mode (hidden attribute). After the DRB is loaded the controller address lines are three stated for the remaining scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentages of total memory cycles available to the processor is approximately (10-2)/10 which equals to 80%.

During attribute assembly, the attribute data is latched into the controller during one clock cycle, both the character and its attribute is driven out and written into the row buffer (two 8 bit row buffers). This allows one to reserve 8 bits for font and 8 bits for attributes and each attribute only affects the character associated with it.

Smooth scrolling all or part of the screen (split screen) is accomplished by a scroll offset register and two programmable registers which define the start data row and the end data row of the smooth scroll operation. The offset register will force the scan line counter outputs of the controller to start at the programmed offset value rather than zero for the data row that starts the smooth scroll internal.

Row attributes such as double height double width or single height single width are programmed by the most significant 2 bits of the row address pointer in the row-table.

4-3

Communications

The keyboard is scanned and decoded by using a single chip microcomputer on the seperate keyboard PCB. Keyboard entry is transmitted to the processor serially at 9600 baud and received thru an SIO. Key codes are assigned using a PROM located on the keyboard PCB. The keyboard would interrupt the CPU for every character that is entered.

The modem interface is similar to the keyboard interface and also uses half a Z80-SIO tie to the interrupt line. The SIO is connected via a pair of line driver and receiver to a standard EIA RS-232 connector.

The printer also uses half a Z80-SIO serial interface with optional interrupt control on the interrupt line. The SIO is connected to an RS232 connector.

4-4

Character Generation

The character generator is 16k bytes of static RAM. The fonts are loaded from system RAM into the font RAM by the CPU. The characters are in a 6X8 matrix placed in a 8X10 cell with half-dot shift to achieve a 11X8 resolution. Bit 0 and 7 on the character font are used to control the half-dot shift.

4-5

Terminal Memory

2K bytes of CMOS RAM with memory power back up, are used to store the terminal`s set up parameters and the special function key codes.

The terminal has 16K RAM space for display memory which provides up to 2 pages in hidden attribute mode. The CRT controller constantly refreshes the display memory to the display screen.

The terminal can have up to 24K bytes of EPROM (2764) space for firmware program code space. The rest of the RAM space not used by the display RAM can be used for program data space.

4-6

Operating Clocks

The Z80 CTC timing controller is used as a baud rate generator to generate the correct frequency clock for the 2 SIO channels. The baud rate on each channel is software programmable from 50 to 19.2K baud.

Interrupt Signals

The 970 CPU interrupt structure allows the peripheral device to identify the starting location of the interrupt service routine. This mode (mode 2) allows an indirect call to any memory location by a single 8 bit vector supplied by the peripheral. In this mode, the peripheral generating the interrupt places the vector onto the data bus in response to an interrupt acknowledge. The vector then becomes the least significant eight bits of the 16-bit indirect pointer.

The IEO and IEI lines of the peripheral devices are connected together in a daisy-chain fashion with the devices closest to the CPU having the lowest priority.

Frame interrupt interrupts the CPU every 1/60 second or 1/50 second depending on line frequency setting. This can be used as the real time clock source. The CRT controller frame interrupt must be enabled in order to generate the frame interrupt. In response to this interrupt, the CPU jumps to location 66H.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	PROTO REL		
	2	" "		
	3	" "		
	A	PROD REL PER ECO 0414		
	A1	PROD REL PER ECO 0443	9/1/82	
	B	PROD REL PER ECO 0459		
	C	" " ECO 0500	9/29/82	
	D	" " " 0518	11/9/82	

A1 DS8867 (OPTION)

A2 (OPTION)

A3 7414

A4 74LS145

A5 74LS145

A6 8049 8749

VR1 REGULATOR 78 M 05

CR1 IN914

CR2 IN914

Y1 5.7143MHZ

X1 AUDIO TRANSDUCER

Q1 2N4401

RESET CLK A7 MC14040 Q8 GND

SHIFT, CNTRL, ALPHA LOCK, FUNCT., RESET

NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACTOR ARE VALUED IN uF 50 VDC AND ARE 10%.

= KEY SWITCH

= NOT USED

APPLICATION		UNLESS OTHERWISE NOTED		DWN HHUR 33-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN		CHK Michael Hall	
2020900	-	ANG 2 PLC 3 PLC		ENGR	TITLE PCB SCHEMATIC 970 KYBD SI
				APPD	
		SCALE		APPD	
		MATERIAL	FINISH	APPD	

SIZE D | SHT 1 OF | DRAWING NO 2020800 | REV .0

S020024-201

D 2020800

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	PROTO REL		
	2	PROTO REL		
	3	"		
	4	PROD REL PER ECO 0584		
	A1	INCORP PER ECO 0640	5/31/83	
	A2	" " " 2011		
	B	" " " 2015		
	C	" " " 2053		

NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4W WATT ± 5%.
2. ALL CAPACTORS ARE VALUED IN µF AND ARE 50 VDC ±20%.

PARTS LIST				
QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

APPLICATION	
NEXT ASSY	USED ON
2021100	

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN: ANG ± PLC ± PLC

SCALE

MATERIAL

FINISH

DWN HUR 4-16-82
CHK
ENGR
APPD
APPD
APPD

TeleVideo, Inc.

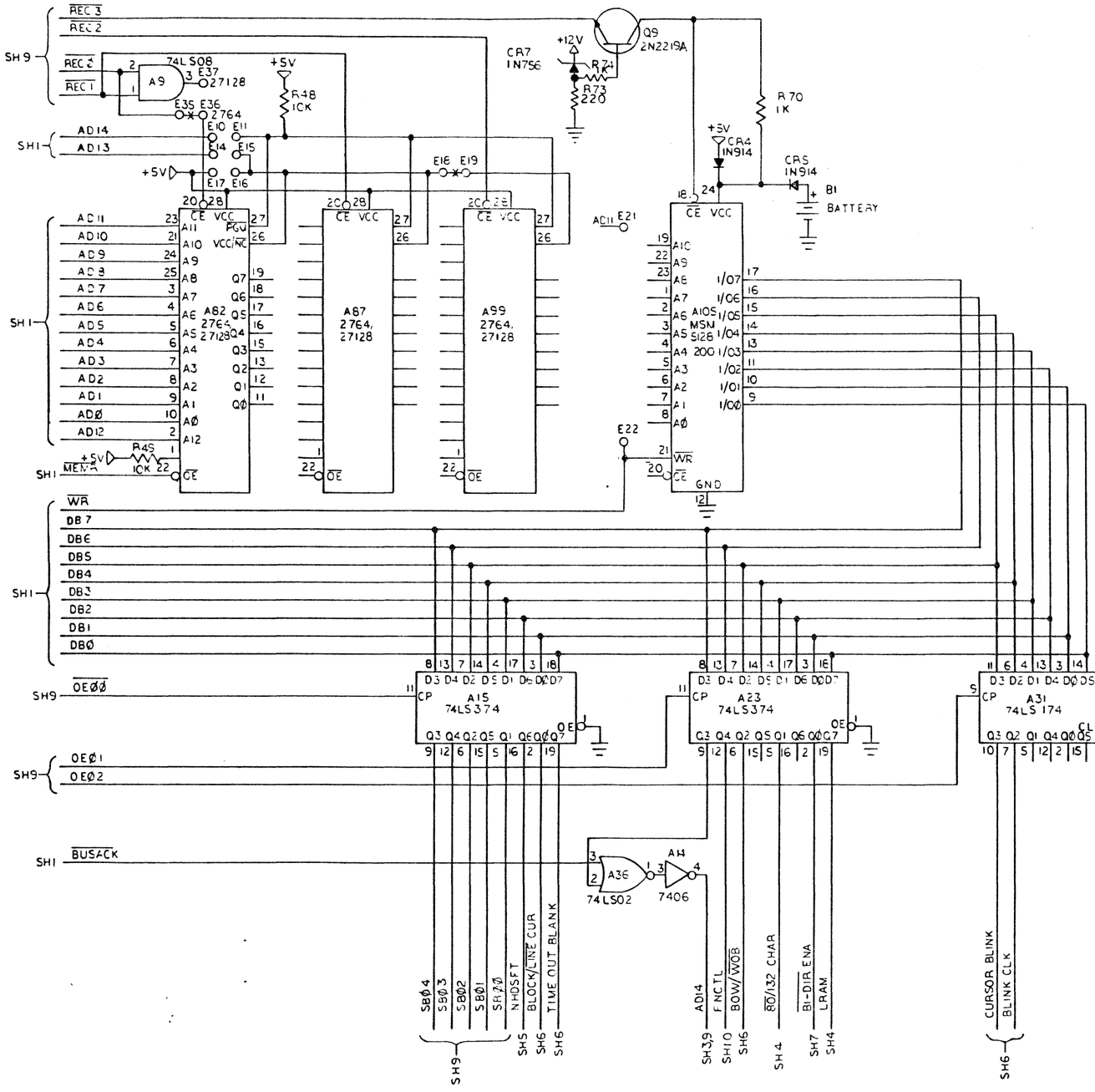
TITLE: PCB SCHEMATIC 52
970 CONT BD

SIZE D | SHT 1 OF 10 | DRAWING NO. 2021300 | REV C

DWG NO 2021300 | SH 1 | REV C

B600025-001

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT		



BE000025-001

PARTS LIST					
QTY REQD	FACM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION
APPLICATION					
NEXT ASSY	USED ON				

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG ± PLC ± PLC

SCALE: ~

MATERIAL

FINISH

DWN HJUR 4-20-82
CHK
ENG
APPD
APPD
APPD

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS INC AND CONTAINS INFORMATION WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO NO PART OF THIS DOCUMENT MAY BE COPIED REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS INC

TeleVideo, Inc.

TITLE
PCB SCHEMATIC
970 CONT BD 53

SIZE D | SHT 2 OF 10 | DRAWING NO. 2021300 | REV C

DRWG NO 2021300 SH 2 REV C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		

WR
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
SH1

SH1,2
ADI4
AD7
ADI3
AD6
ADI2
AD5
ADII
AD4
SH1

ADI0
AD3
AD9
AD2
AD8
ADI
ADI5
ADØ
SH1

E7 64K
E5 16K
E6

SH1 RFSH
SH1 MI
SH1 MREQ
SH4 9KRD
SH1 BUSACK
SH4 CCLK
SH4 DMAR
SH1 MEMR
SH1 BUSACK
SH4 DCLK
SH4 QBCLK

A110 74LS04
A20 74LS00
A19 74LS10
A114 74LS51
A113 74LS74
R61 4.7K
+5V

+5V RP6 4.7K A63
33Ω
R71 33
E25 64K
E30 16K
E32 64K
E26 NC
E28 16K
E27 64K
E29 16K
E31
-5V
+12V
+5V

A94 4116
A101 4116
A106 4116
A111 4116
A95 4116
A102 4116
A107 4116
A112 4116
D1 DØ R/W A7/VCC A6 A5 A4 A3 A2 A1 AØ CAS RAS VDD VSS

A103 74LS541
G1 G2
SH1
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ

74LS08 A105 A109 A108
74LS74 A113 A109 A108
R60 4.7K +5V

ADI5
MREQ
SH1

74LS32 A91 A91
A105 74LS08

B600075-001

QTY REQD	FROM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN	FITUR 4-22-82
NEXT ASSY	USED ON	ANG ± PLC ± PLC	CHK	
			ENG	
		SCALE	APPD	
		MATERIAL	FINISH	

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS, INC. AND CONTAINS INFORMATION WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO. NO PART OF THIS DOCUMENT MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS, INC.

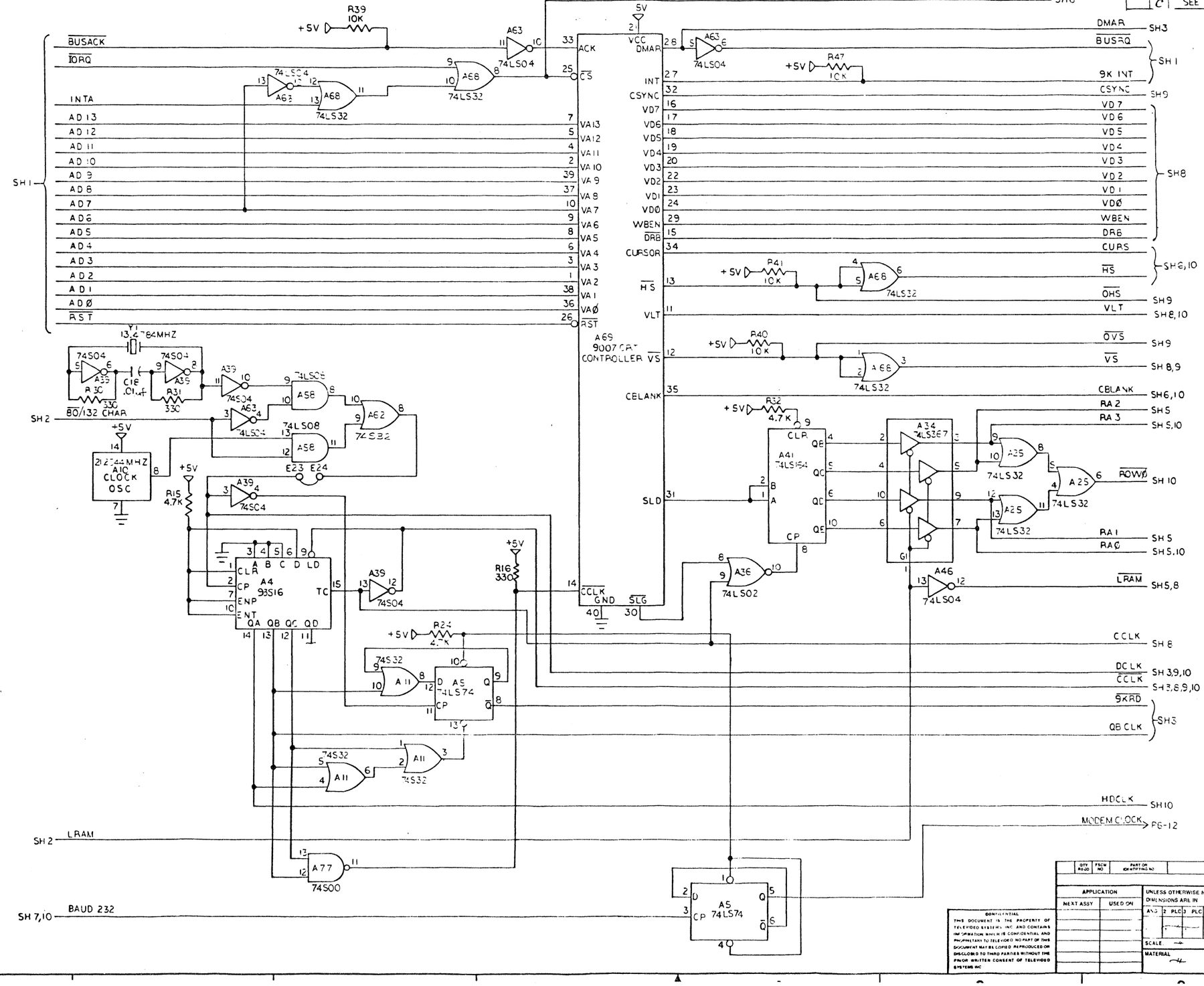
TeleVideo, Inc.

TITLE: PCB SCHEMATIC 970 CONT BD

SIZE	SHT	OF	DRAWING NO.	REV
D	3	10	2021300	C

2021300 ORIGINAL
2.1 PRINT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		



B60002500

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± PLCS ± PLC
SCALE —
MATERIAL —
FINISH —

DWN THUR 4-22-82
CHK
ENGR
APPD
APPD
APPD

TeleVideo, Inc.

TITLE
PCB SCHEMATIC
970 CONT BD 55

SIZE	SHT OF	DRAWING NO.	REV
D	4 OF 10	2021300	C

2021300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		

SH10 DCLKA
SH1 IOW
SH10 CAD3, CHAD7, CHAD6, CHAD5, CHAD4, CHAD3, CHAD2, CHAD1, CHADØ
SH8
SH10 UPSEL
SH1 DB7, DB6, DB5, DB4, DB3, DB2, DB1, DBØ
SH9 FNØ1
SH9 RAØ, RA1, RA2, RA3
SH4
SH9 FNØØ
SH10 CCLKA, DCLKA
SH9 FN Ø2
SH4 LRAM
SH10 HDINH
SH2 NHDSFT
SH6 DHDEN

LREN

A71 74LS32 — A76 74LS04 — E41 E42 — R44 4.7K +5V — P/W

A40 74LS157 — A64 74LS374 — A33 74LS173 — A65 74LS245 — A25 74LS32 — A71 74LS32 — A71 74LS32 — A47 74LS32

A56 6116/2716/2732 — OE — CS

ASC 74LS166 — CLR — SIN — INH — CLK LOAD — R36 4.7K +5V

A49 74S74 — R35 1K +5V

A48 74S253 — ST

A46 74LS04 — A46 74LS04 — A47 74LS32 — DOT SERIAL SH6

R37 4.7K +5V

A55 74LS163 — ENP — ENT — LP

74LS08 — A32 — A32 — 74LS08

R23 4,7K +5V

A24 74LS74 — A24 74LS74

A76 74LS04

74LS08 — A66 — A66 — 74LS08

HDEN SH6

B600025-001

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		
NEXT ASSY	USED ON	ANG ± PLC ± PLC	DWN HHUR 4-29-82	TeleVideo, Inc.
			CHK	
			ENG	
		SCALE	APPD	TITLE PCB SCHEMATIC 970 CONT BD 56
		MATERIAL	FINISH	SIZE D SHT 5 OF 10 DRAWING NO. 2021330 REV C

REVISIONS				
ZONE	TR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		

SHT 10 CCLKA

SHT 5 HDEN

SHT 10 ROW BLANK
SHT 2 CURSOR BLINK
SHT 4 CURS

SHT 2 BLOCK/LINE CUR
SHT 10 ROW 9
SHT 4 CBLANK

SHT 4 HS

A6 74LS377 (CP, D3, DØ, D6, D7, D5, D4, D2, D1, OE; Q3, QØ, Q6, Q7, Q5, Q4, Q2, Q1)

A12 74LS08 ×2 · A47 74LS32

DHDEN SHT 5

DC BLANK SHT 10

A2 74LS04

HS → P2-1

SHT 8 BLINK
SHT 2 BLINK CLK

SHT 8 BLANK

A38 74LS08 · A46 74LS04 · A39 74LS04 · A36 74LS32

SHT 5 DOT SERIAL

SHT 8 UNDER LINE

DCURS

A30 74LS00 · A22 74LS86

SHT 8 REVERSE VIDEO
SHT 2 BOW/WOB
SHT 8 HALF INTENSITY
SHT 2 TIME OUT BLANK

A7 74LS32 · A22 74LS86 · A14 7406

R17 270 · R5 22 · +5V · C6 4.7uf 16V · VIDEO SHIELD GND → P2-3 · R6 1K · R7 1K · R18 270 · CR1 IN914 · Q3 2N2219A · R75 68 · VIDEO → P2-4 · R19 330 · VMIX SHT9

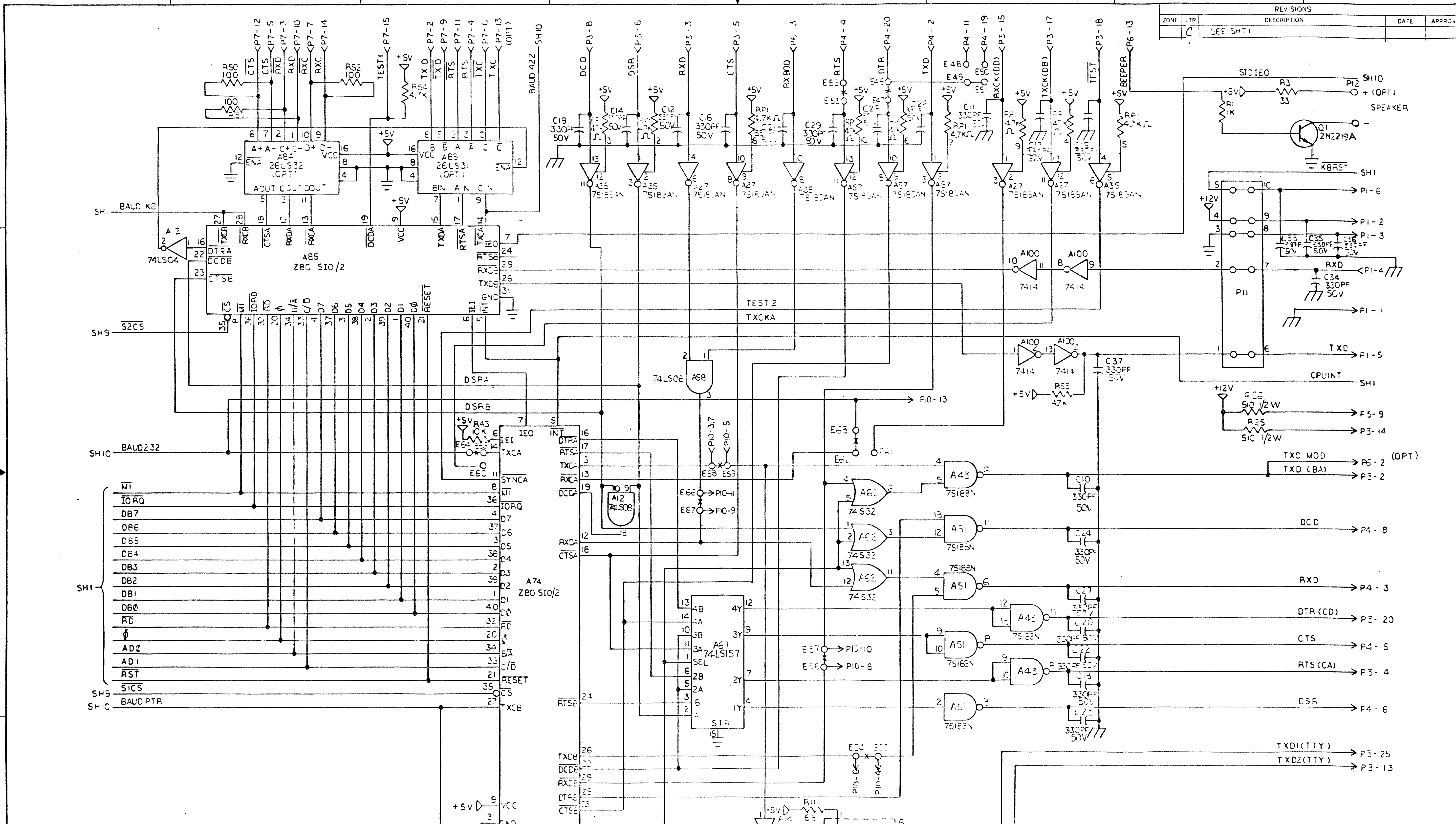
P5-5 → +12V
P5-4 → +5V
P5-1 → -5V
P5-3 → GND

C9 330PF 50V · C8 330PF 50V · C7 330PF 50V · C1 22uf 15V · C5 22uf 15V · C2,42-45 .1 · VR1 LM 79L05 ACZ (-12V IN, OUT) · C41,43,5 .1 · C39-41, 46-52,54, 56,58-63, 65-68,160 .1 · C3 22uf 15V · C4,53,55,57 .1 · C25 .1

B600025-001

PARTS LIST					
QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION
APPLICATION: NEXT ASSY / USED ON		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN: ANG ± PLC .3 PLC	DWN M. BELL · CHK · ENG · APPD · APPD · APPD	TeleVideo, Inc.	
		SCALE:	MATERIAL · FINISH	TITLE: PCB SCHEMATIC 970 CONT BD	
				SIZE D · SHT 6 OF 10 · DRAWING NO 2021300 · REV C	

2021300 9 C



B820025-001

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS INC AND CONTAINS INFORMATION WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO. NO PART OF THIS DOCUMENT MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS INC.

APPLICATION — NEXT ASSY — USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG PLC PLC
SCALE
MATERIAL
FINISH

DWN H HUR 5-6 82
CHK
ENGR
APPD
APPD
APPD

TeleVideo, Inc.

TITLE
PCB SCHEMATIC
970 CONT BD

SIZE D | SHT 7 OF 10 | DRAWING NO. 2021300 | REV C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		

SH1C CCLKA

SH1 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ

S-4 LRAM VS CCLK — 74LS00 A30

A54 9006-135 ODD CHAR. — CKEN OE DI7-DI0 DO7-DO0 WBEN CLK CLRCNT

A60 9006-135 Even — CKEN OE DI7-DI0 DO7-DO0 WBEN CLK CLRCNT

A53 9006-135 ODD ATTRB. — CKEN CLRCNT OE DI7-DI0 DO7-DO0 WBEN CLK

A59 9006-135 Even — OE DI7-DI0 DO7-DO0 WBEN CKEN CLK CLRCNT

A61 74LS374 — CP OE D7-D0 Q7-Q0

A45 74LS374 — CP OE D7-D0 Q7-Q0

A37 74LS374 — CP OE D7-D0 Q7-Q0

CKEN1

CHAD7 CHAD6 CHAD5 — SH5,10

CHAD4 CHAD3 CHAD2 CHAD1 CHADØ — SH5

SH 5,10

CLR1

A28 74LS157 — 1A 1B 2A 2B S 1Y 2Y G

OE1

SH1 BUSACK SH4 WBEN — A81 74LS32

A7 74LS32

SH4 9KSEL — A58 74LS08

SH1 IOR — A63 74LS04

A22 74LS245 NBT245N — B7 B6 B5 B4 B3 B2 B1 B0 / A7 A6 A5 A4 A3 A2 A1 AØ — G DIR

CLR2

SH4 VD7 VD6 VD5 VD4 VD3 VD2 VD1 VDØ

HALF INTENSITY
UNDER LINE
REVERSE VIDEO
BLINK
BLANK
— SH6

SH6,9

OE2 WBEN1

WBEN

OE1

A63 74LS04

VLT

+5V R34 4.7K

A44 74LSIØØ — S J CK K R C Q

A52 74LS157 — S 1A 1B 2A 2B 3A 3B 4A 4B 1Y 2Y 3Y 4Y 1S

SH4 CCLK VLT DRB — A35 74LS02

SH10 HCCLK

CLRLB

WBEN2

A46 74LS04

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS INC. AND CONTAINS INFORMATION WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO. NO PART OF THIS DOCUMENT MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS INC.

PARTS LIST

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — ANG 2 PLC 3 PLC

SCALE A

MATERIAL — FINISH

DWN H.C. 3-28-86 — CHK — ENG — APPD — APPD — APPD

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 970 CONT BD 59

SIZE D — SHT 8 OF 10 — DRAWING NO. 2021300 — REV C

8400325-001

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		

P3-12
P3-24
CR3 1N914
R33 100K
R27 3.3K
A20 74LS00
A43 75188
P3-10
A7 74LS32
VERT SYNC
P2-5
+5V
680
R9
Q8 2N2219A
COMPOSIT VIDEO
P2-6
R72 82
A8 7406
R20 470
R22 1K
R21 2K
R8 470
A2 74LS04
A6 7406
R4 100
A1 7406
SH4 VS
SH2 SB03 SB02 SB01 SB00
SH6 VMIX
SH4 CSYNC
SH2 SB04

GRAPHIC CONNECTOR OPT
+5V
P8-1
P8-2
SH1 AD0 / GRAFCS P8-3 P8-4
SH1 AD1 P8-5
+12V P8-6
SH1 AD2 P8-7
AD3 P8-8
P8-9
P8-10
P8-11
P8-12
P8-13
-12V P8-14
P8-15
P8-16
SH1 IOW P8-17
P8-18
P8-19
SH6 VMIX P8-20
DCLK P8-21
SH4 OHS P8-22
OVS P8-23
P8-24
SH4 CCLK P8-25
SH3 HALF INTENSITY P8-26

OPT
+12V P5-1 P5-14
-12V P5-5 P5-10
5V P5-6 P5-9

SH1 ICR
SH1 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
A75 74LS245 OPT
GDB7 GDB6 GDB5 GDB4 GDB3 GDB2 GDB1 GDB0

SH1 AD0 AD1 IOW INTA IORQ AD7 AD4 AD5 AD6 MREQ AD15 AD12 AD13 AD14
A76 74LS04
SH1,2
E20 E13 E12 E9 E8 E33 E34
A88 74LS138
A93 74LS138
A91 74LS32
FNCS
A83 74LS139
RECT3 RECT2 RECT1 RECT0
SH2
SHCS SHCS CTCCS
SH7 SH10
OE02 OE01 OE00
FN02 FN01 FN00
SH2 SH5

B82000E-001

QTY PER	ITEM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION	
NEXT ASSY	USED ON

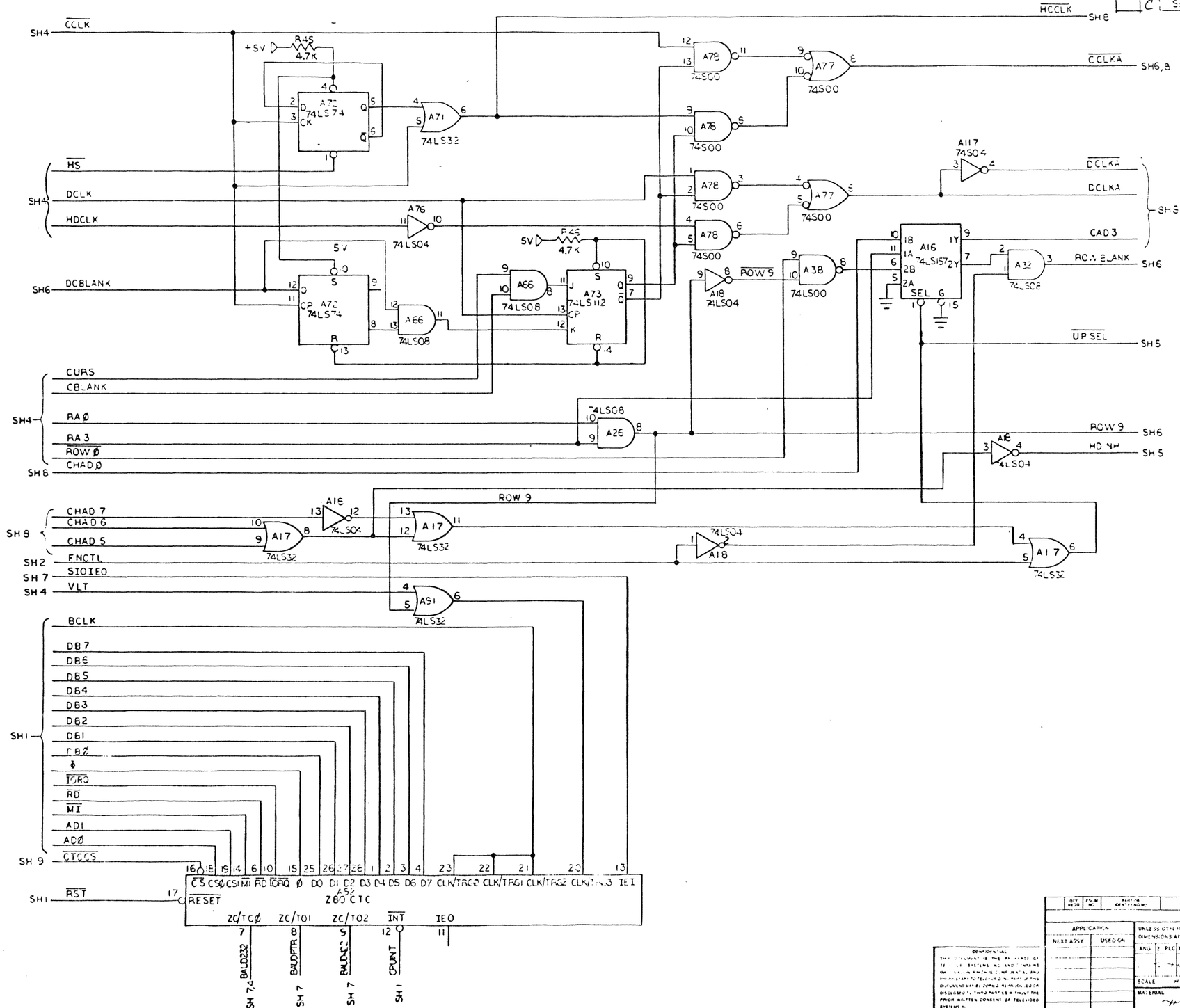
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± PLC ± PLC
SCALE
MATERIAL
FINISH

DWN KURS-10-82
CHK
ENG
APPD
APPD
APPD

TeleVideo, Inc.
TITLE PCB SCHEMATIC
S70 CONT BD 5/10
SIZE D SHT 9 OF 10 DRAWING NO. 2021300 REV C

ON SHEET 2021300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHT 1		



B4000025-001

PARTS LIST			
QTY PER	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION / MATERIAL SPECIFICATION

APPLICATION: NEXT ASSY | USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN INCHES AND ± PLC ± P.C.

SCALE M

MATERIAL

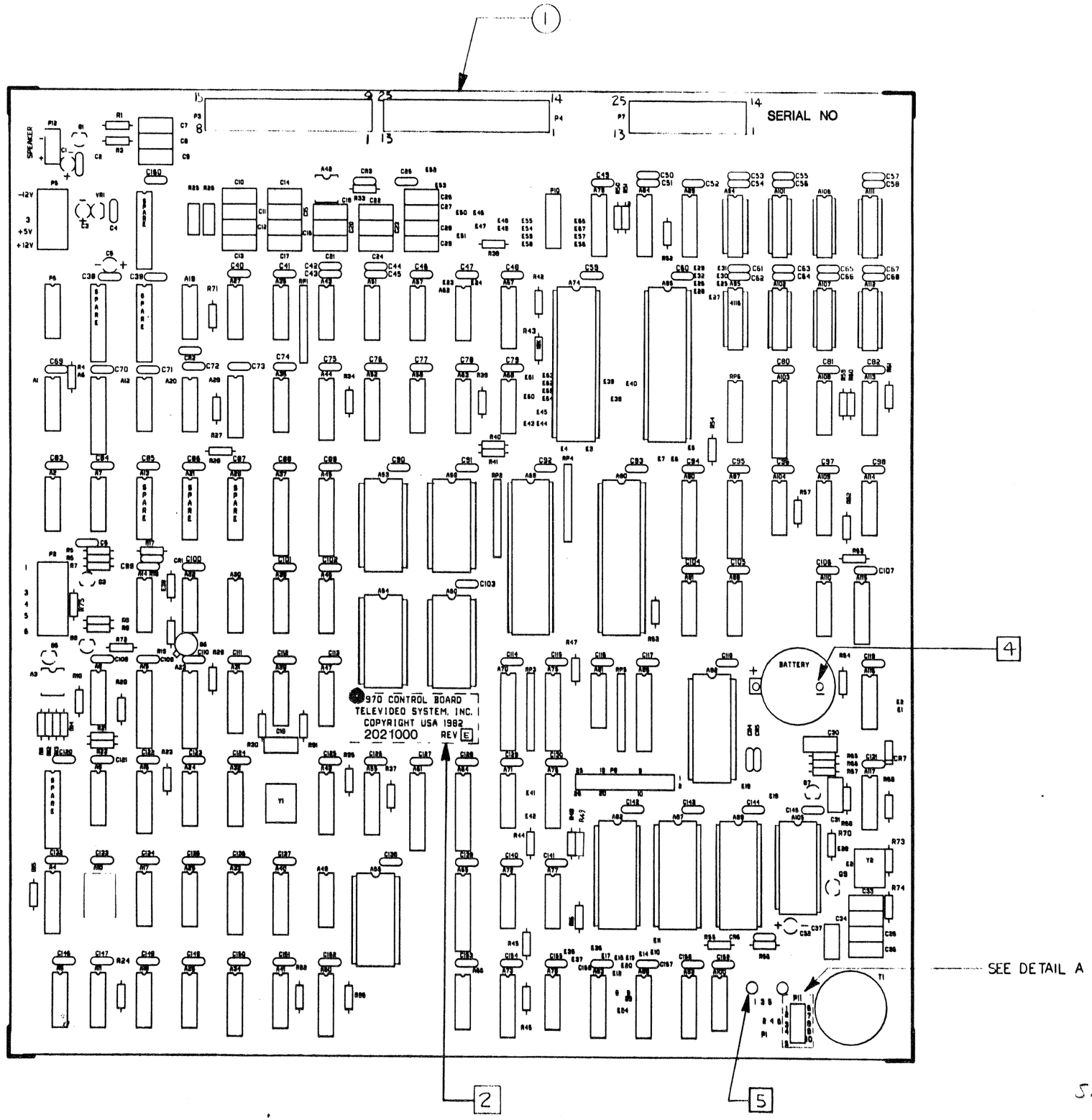
FINISH

DRAWN GR 5-10-82
CHK
ENGR
APPD
APPD
APPD

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 970 CONT BD 5/1

SIZE D | SHT 10 OF 10 | DRAWING NO. 2021300 | REV C

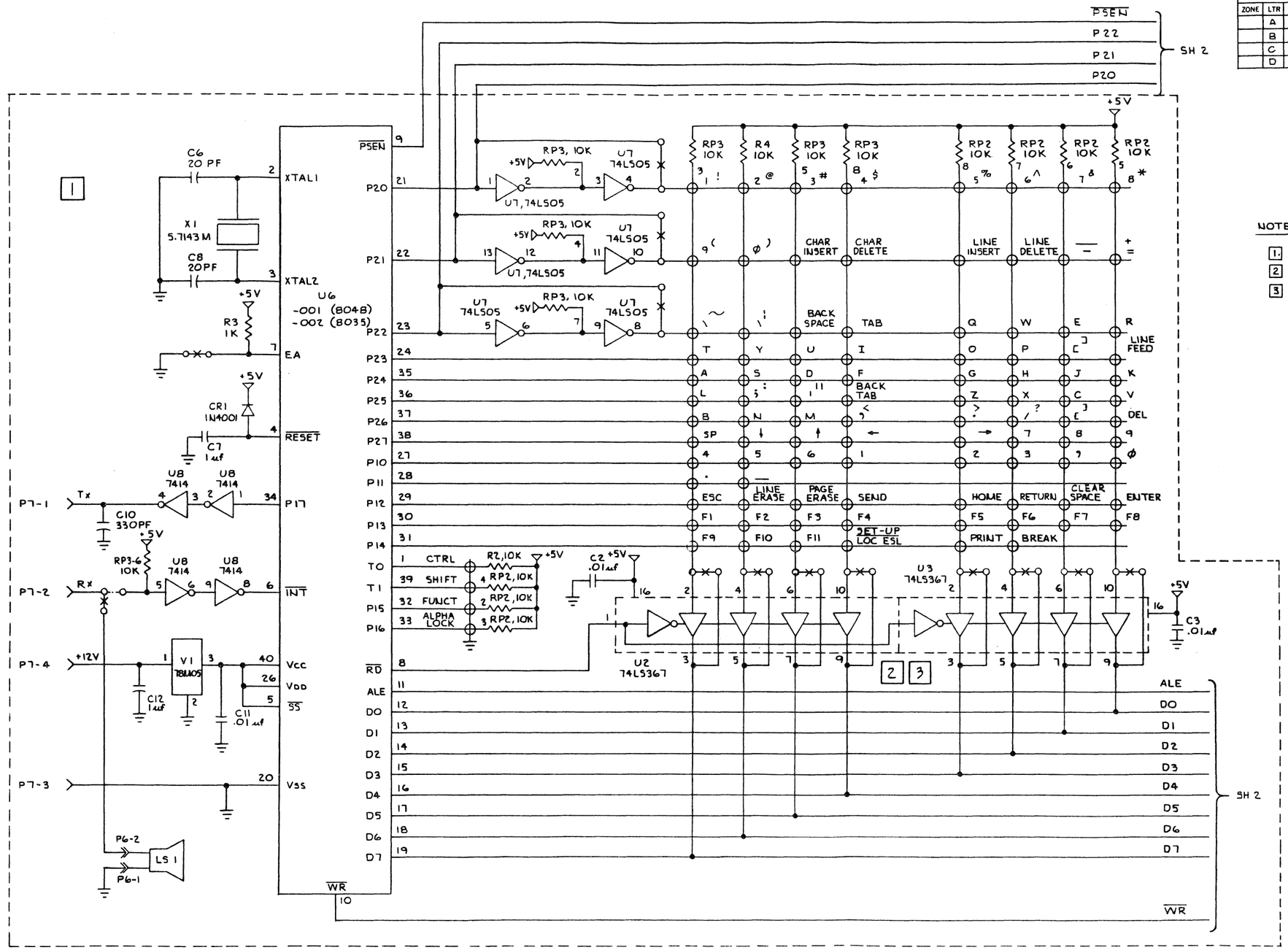

1
SERIAL NO
970 CONTROL BOARD
TELEVIDEO SYSTEM, INC.
COPYRIGHT USA 1982
2021000 REV E
BATTERY
SEE DETAIL A
2
4
5

S11A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 42		
	B	" " ECO 43		
	C	" " ECO 44		
	D	" " ECO 46		

NOTES:-UNLESS OTHERWISE SPECIFIED

1. VERSION -001 AND -002
2. VERSION -002 ONLY
3. CIRCUITRY OPTIONAL



B600003-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN	CHK	ENGR	APPD	APPD	APPD
NEXT ASSY	USED ON	DIMENSIONS ARE IN						
		ANG 2 PLC 3 PLC						
		SCALE NONE						
		MATERIAL						
		FINISH						

TeleVideo, Inc.

TITLE PCB SCHEMATICS 950 KEYBOARD

SIZE	SHT OF	DRAWING NO.	REV
D	1 OF 2	2010300	D

D 20103-00

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
2	4	4								C1,3,5,32	Cap Elec 22uf 15V 5%	2025700
3	1	1								C6	Cap Tant 4.7uf 16V 10%	2027500
4	26	26								C7-17,19-24,26-	Cap Cer 330 pf 50V 20%	2029100
										29,33-37		
5	125	125								C2,4,25,38-160	Cap Cer .1uf 50V 20%	2030100
6	1	1								C30	Cap Mono 47pf 100V 5%	2029500
7	2	2								C18,31	Cap Mono .01uf 50V 10%	2028900
8												
9												
10	1	1								A80	IC Z80A CPU A	2051000
11	1	1								A92	IC Z80A CTC A	2050800
12	2	2								A74,85	IC Z80A SIO/2A	2050600
13	2	2								A44,79	IC 74LS109	2027000
14	1	1								A73	IC 74LS112	2138500
15	7	7								A5,24,72,104,108,	IC 74LS74	2026600
										113,116		
16	2	2								A39,117	IC 74S04	2024600
17	6	6								A2,18,46,63,76,	IC 74LS04	2024800
										110		
18	1	1								A100	IC 7414	2035400

NOTES:

TITLE	DATE	
PCB ASSY CONTROL BOARD 970	5-4-83	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
19	7	7								A9,12,26,32,58,	IC 74LS08	2025200
										66,109		
20	3	3								A20,30,38	IC 74LS00	2024200
21	9	9								A7,17,25,47,62,	IC 74LS32	2025800
										68,71,81,91		
22	2	2								A86,103	IC 74LS244	2044200
23	2	2								A36,98	IC 74LS02	2041600
24	2	2								A88,93	IC 74LS138	2041000
25	1	1								A83	IC 74LS139	2027200
26	7	7								A6,15,23,37,45,	IC 74LS374	2029000
										61,64		
27	1	1								A31	IC 74LS174	2028200
28	1	1								A114	IC 74LS51	2026200
29	2	2								A90,97	IC 74LS241	2042000
30	2	2								A55,115	IC 74LS163	2027600
31	1	1								A41	IC 74LS164	2048200
32	1	1								A34	IC 74LS367	2028600
33	2	2								A65,70	IC 74LS245, N8T245N	2036200
34	1	1								A33	IC 74LS173	2028000
35	1	1								A48	IC 74S251	2138600
36	1	1								A49	IC 74S74	2026400

NOTES:

TITLE: 3 ASSY CONTROL BOARD 970

DATE: 5-4-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
37	1	1								A50	IC 74LS166	2027800
38	1	1								A19	IC 74LS10	2025400
39	3	3								A1,8,14	IC 7406	2034800
40	1	1								A22	IC 74LS86	2026800
41	5	5								A16,28,40,52,67	IC 74LS157	2027400
42												
43												
44	2	2								A43,51	IC 75188N	2029200
45	3	3								A27,35,57	IC 75189AN	2029400
46	1	1								A56	IC EPROM US/UK CHAR GEN	8000139
47	1	1								A82	IC 970 EPROM Firmware	8000100
48	1	1								A69	IC 9007 CRT Controller	2139900
49	4	4								A53,54,59,60	IC 9006-135 Buffer CRT Sgl	2140000
											Row	
50	8	8								A94,95,101,102,	IC 4116 16K Dynamic RAM	2139200
										106,107,111,112	120 ns	
51	1	1								A105	IC 2Kx8 6116 CMOS Static RAM	2138700
52	2	2								A3,42	IC 4N38	2035000
53	1	1								A10	21.2544 MHZ Clock OSC	2138900
54	1	1								A4	IC 93S16PC	2040800
55	1	1								A11	IC 74S32	2038800

NOTES:

TITLE PCB ASSY CONTROL BOARD 970

DATE 5-4-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
56	2	2								A77,78	IC 74S00	2024000
57	1	1								A87	IC 970 EPROM Firmware	8000101
58	1	1								A99	IC 970 EPROM Firmware	8000102
59												
60	1	1								Y2	Cry 8.0000 MHZ	2098603
61	1	1								Y1	Cry 13.4784 MHZ	2141400
62	6	6								XA53,54,56,59,	Socket 24P IC DIP	2098401
										60,105		
63	4	4								XA69,74,80,85	Socket 40P IC DIP	2098402
64	8	8								XA94,95,101,102,	Socket 16P IC DIP	2098405
										106,107,111,112		
65	4	4								XA82,87,92,99	Socket 28P IC DIP	2098404
66	2	2								P2,5	Plug 5P Str Waf	2098802
67	2	2								P3,4	Conn 25P PCB Metal D-Sub Fem	2165300
68	1	1								P1	Conn 6P RJ12 970 Logic Bd	2141200
69												
70												
71												
72												
73												
74	1	1								VR1	Volt Reg 79L05AC	2126200

NOTES:

TITLE 'B ASSY CONTROL BOARD 970

DATE 5-4-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
75	9	9								R39-43,47-49,56	Res C/F 10K Ohm 1.4W 5%	2034100
76	2	2								R27,28	Res C/F 3.3K Ohm 1.4W 5%	2052700
77	1	1								R9	Res C/F 680 Ohm 1.4W 5%	2037100
78	2	2								R5,67	Res C/F 22 Ohm 1/4W 5%	2033500
79	3	3								R3,59,71	Res C/F 33 Ohm 1/4W 5%	2034500
80	1	1								R72	Res C/F 82 Ohm 1/4W 5%	2144000
81	2	2								R11,75	Res C/F 68 Ohm 1/4W 5%	2051100
82	4	4								R4,50-52	Res M/F 100 Ohm 1/4W 1%	2034900
83	2	2								R66,73	Res C/F 220 Ohm 1/4W 5%	2040300
84	4	4								R16,19,30,31	Res C/F 330 Ohm 1/4W 5%	2051500
85	2	2								R17,18	Res C/F 270 Ohm 1/4W 5%	2051300
86	5	5								R8,12,20,68,69	Res C/F 470 Ohm 1/4W 5%	2051700
87	8	8								R1,6,7,22,35,65,	Res C/F 1K Ohm 1/4W 5%	2052100
										70,74		
88	1	1								R13	Res C/F 51K Ohm 1/4W 5%	2032300
89	1	1								R33	Res C/F 100K Ohm 1/4W 5%	2032100
90	22	22								R14,15,23,24,29,	Res C/F 4.7K Ohm 1/4W 5%	2053100
										32,34,36-38,44-		
										46,53-55,57,60-		
										64		
91	2	2								R25,26	Res C/F 510 Ohm 1/2W 5%	2045100

NOTES:

TITLE: ASSY CONTROL BOARD 970

DATE: 5-4-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A	D										
92	1	1								RP6	Res PK 33 Ohm 16 Pin DIP	2041700
93	3	3								RP1,3,5	Res PK 4.7K Ohm 10P SIP	2041300
94	1	1								R10	Res C/F 180 Ohm 1/4W 5%	2053300
95	1	1								R21	Res C/F 2K 1/4W 5%	2036900
96	2	2								RP2,4	Res PK 2.2K Ohm 10P SIP	2230000
97	2	2								Q5,7	Trans 2N2907A	2045900
98	6	6								CR1-6	Diode 1N914	2047500
99	4	4								Q1,3,8,9	Trans 2N2219A	2045300
100	1	1								Q6	Trans 2N3019	2045700
111												
112												
113												
114												
115												
116												
117	1	1								CR7	Diode Zener 1N756 8.2V	2244500
118	1	1									Battery Holder	2050101
119	1	1								B1	Battery	2050001

NOTES:

TITLE PCB ASSY CONTROL BOARD 970

DATE 5-4-83

TeleVideo Systems, Inc.

950 THEORY OF OPERATION

Table of Contents Page

950 THEORY OF OPERATION

MAIN LOGIC BOARD

Overview

Please refer to pages 1, 2, 3, and 4 of the block diagrams as you read the text that follows.

Page 1 shows the power-on reset, which is controlled by A17. During power-up, this chip sends the signals necessary to reset the CPU and to perform the initial diagnostic routine. This routine reads the switches in the back of the terminal and configures it for the proper handshaking protocol.

The 950's CPU is a 6502, located at A53.

The Shift clock (OSC1) generates the timing for the 950's logic system. The Stretch clock functions as the main clock for the CPU. Other clock circuits include the Crystal clock to the UARTs, the Shift clock, the DC Carry clock, the C clock, and the QC clock.

The CPU's address bus (6502 bus) addresses the ROM chips (A41 and A42).

The ROMs contain the operating instructions, the power-up diagnostics, and the other intructions necessary to operate the terminal. Most systems only use two ROMs, but the 950 contains an additional, optional ROM (A52).

The decoding gates (A58 and A63) select one of the three ROMs. The other decoder (A62) selects either the DISP.MEM (display memory) or the IOP.SEL (input/output select) signal.

The auxiliary chip on this page (6522) reads switches (S1 and S2), and generates the control signals for the video attributes and the bell, as well as several auxiliary control signals used to address the display RAM.

On page 2 of the block diagram, note the continuation of the 6502 and the 6522.

The CRT controller chip (CRTC 6545) generates the signals necessary to control the monitor portion of the terminal. It outputs three primary signals: horizontal synch, vertical synch, and cursor. These signals go to the video module.

The display RAMs are addressed by the 14 address bits coming from the CPU bus, as well as the memory address bits from the CRTC.

The multiplexers in the center of the page (A43 through A46) alternately select whether the CPU or the CRTC is permitted to address the system and the display RAMs (A25 through A28, A34 through A37).

The Phase clock controls this process. During one phase of the clock the CPU can address RAM. During the other phase, this multiplexer allows the CRTC to address RAM.

When the CPU addresses the system display RAMs, the bidirectional latch at A14 is enabled to either input or output data from the system RAMs. When the CRT controller addresses the RAMs, the latch at A24 holds the display data.

Normally, the outputs of the CRTC would be used for scrolling. However, since the 950 has a smooth scroll option, the output of the counter latches at the bottom of page 2 (A60 and A61) are used to scroll. The CPU controls these latches through the decoder at A62.

On page 3 of the block diagrams, the row address signals coming from these counter latches (A60 and A61) and the display data from the latch above it (A24) are used to address the character-generator ROMs (A32 and A33). The character-generator ROMs then output 14 bits to a parallel-to-serial shift register.

The DC.Carry signal loads these 14 bits at the shift register (A22 and A23), and the shift clock shifts the data into the video logic and the drivers as a serial data stream.

The eight bits of display data from latch A24, as well as one bit from the character generator ROMs, address the attribute registers.

The attribute registers' output also addresses the video logic and drivers, as do the video attribute signals sent by 6522. These signals (dark on light, cursor, force blank, blink rate, and maximum intensity) control the video attributes through the video logic and drivers. Note that, in the 950, the maximum intensity signal (MI) is standard. To highlight, the 950 uses half intensity. The output is routed to the video module.

The XTAL1 clock (clock source) controls the three UARTs on page 4 of the block diagrams.

A49 receives data from the keyboard.
A50 receives and transmits data for the main port (P3).
A51 receives and transmits data for the printer port (P4).

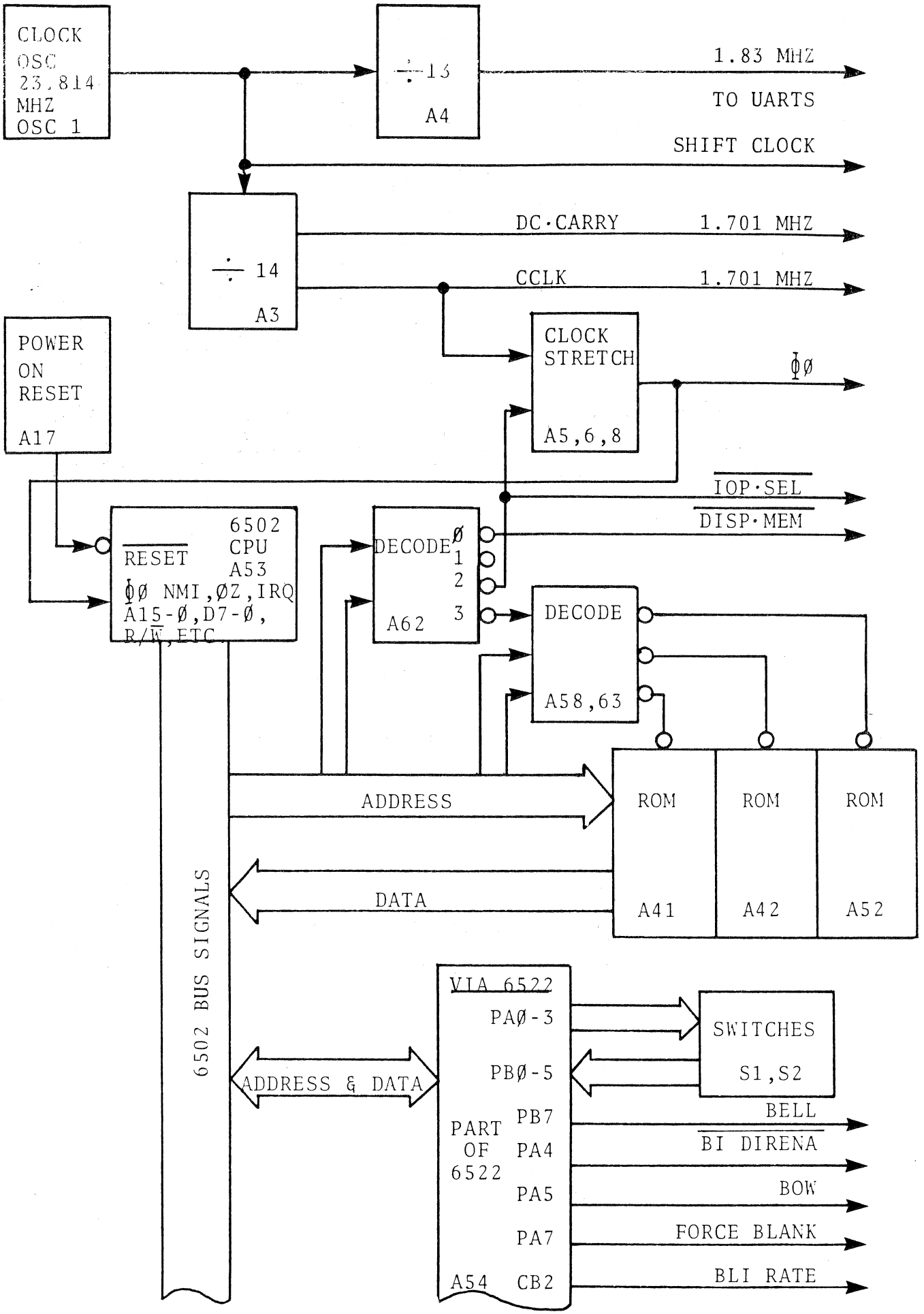
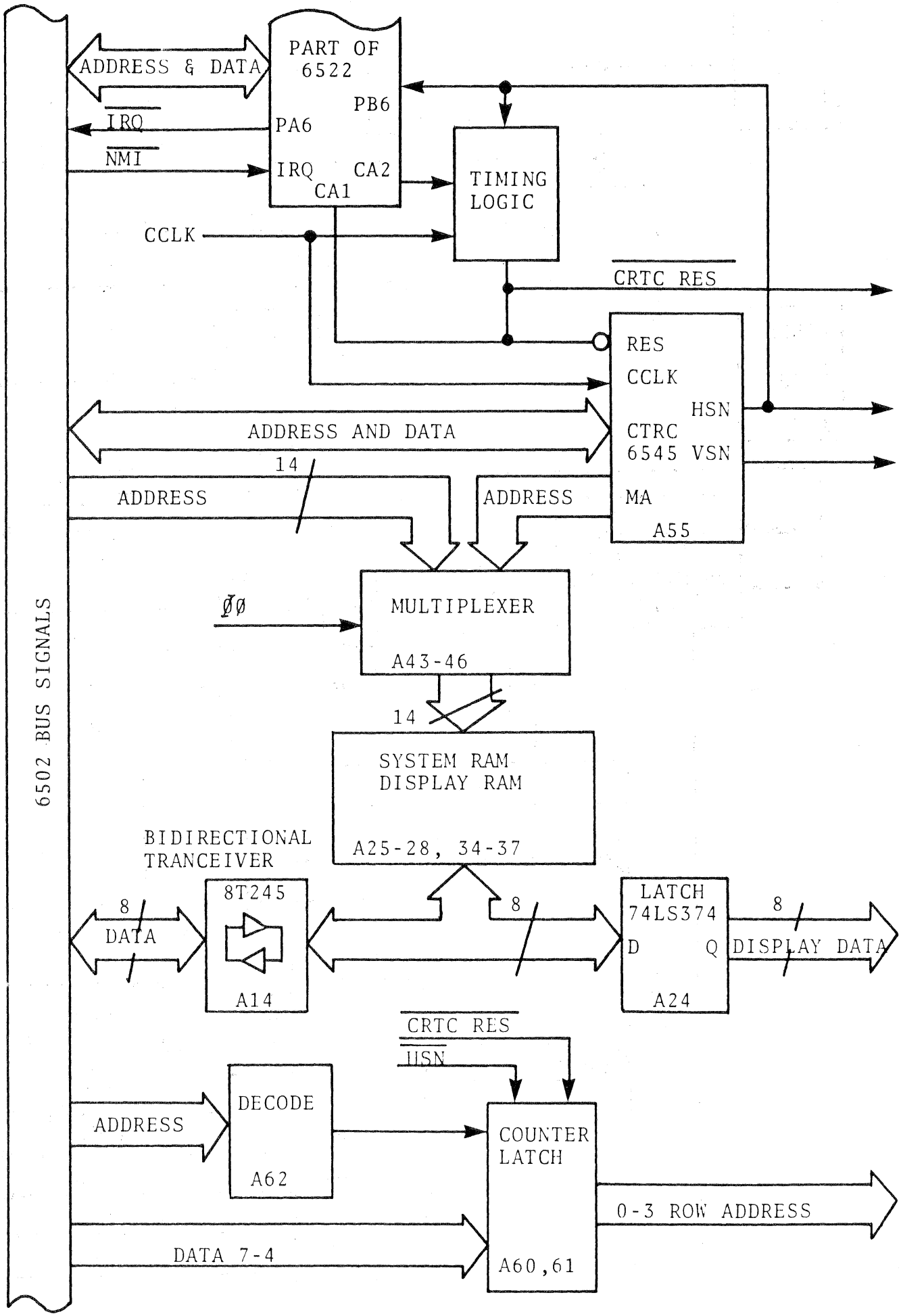


FIG. 1 CPU, TIMING AND CONTROL


6502 BUS SIGNALS
ADDRESS & DATA
PART OF 6522
PB6
IRQ
PA6
NMI
IRQ
CA2
CA1
TIMING LOGIC
CCLK
CRTC RES
RES
CCLK
HSN
ADDRESS AND DATA
CTRC 6545
VSN
14
ADDRESS
ADDRESS
MA
A55
ØØ
MULTIPLEXER
A43-46
14
SYSTEM RAM DISPLAY RAM
A25-28, 34-37
BIDIRECTIONAL TRANCEIVER
8
DATA
8T245
A14
8
LATCH 74LS374
D
Q
8
DISPLAY DATA
A24
CRTC RES
USN
ADDRESS
DECODE
A62
COUNTER LATCH
0-3 ROW ADDRESS
DATA 7-4
A60,61

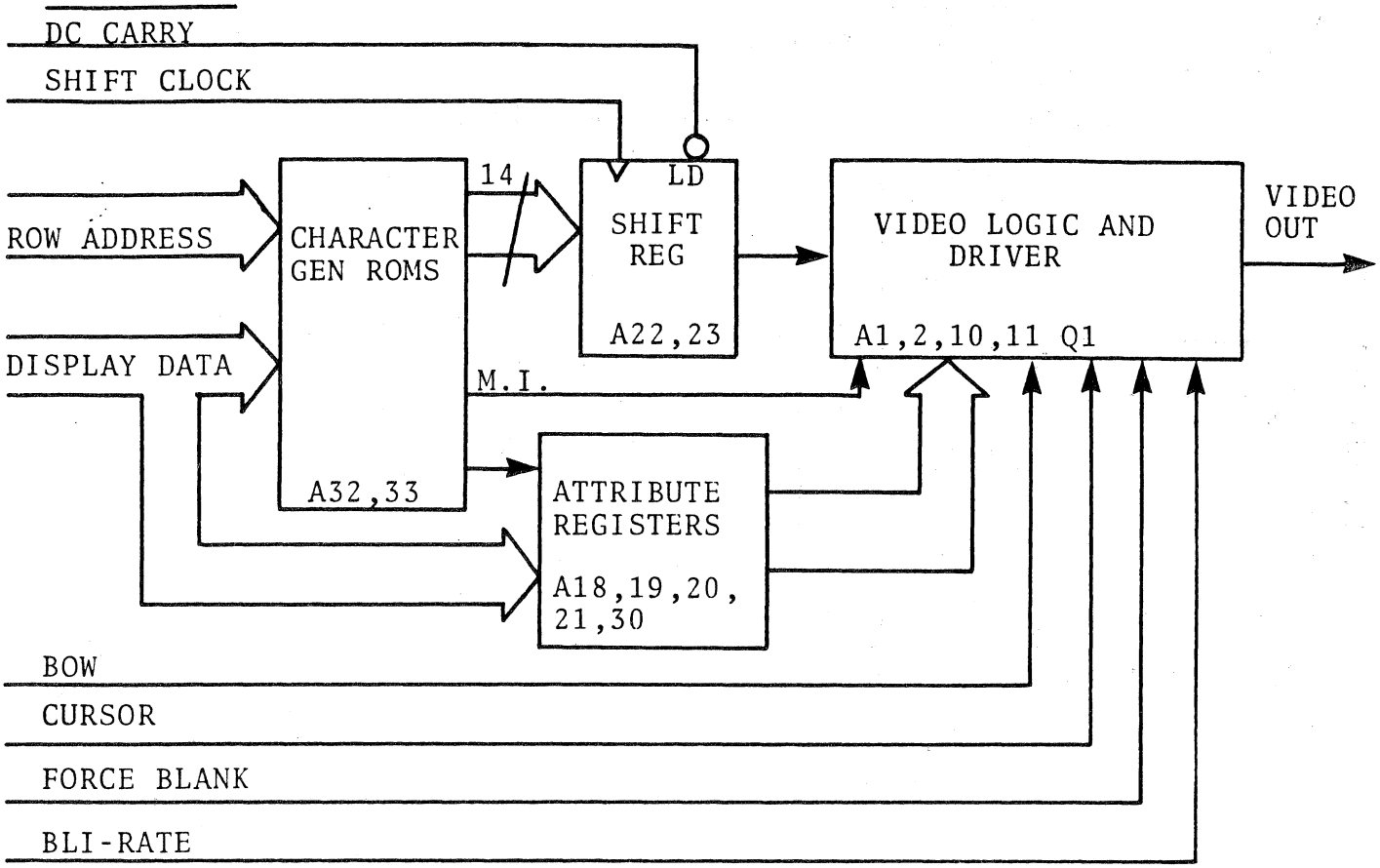


FIG. 3 VIDEO GENERATION

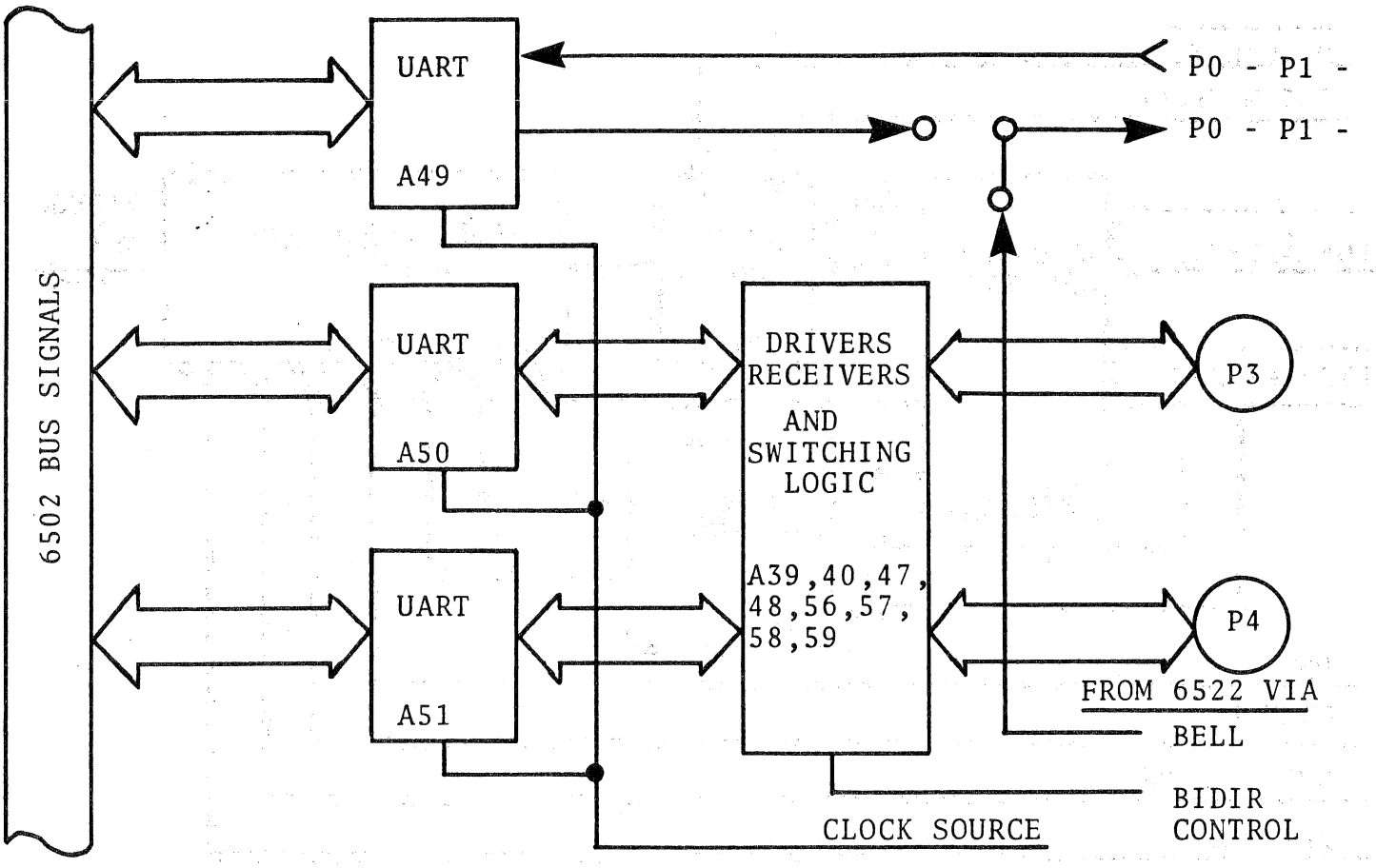


FIG. 4 I/O CIRCUITS

CPU Timing and Control

A 23.814 MHz. oscillator (OSC 1, sheet 6) generates the timing for the 950's entire internal logic system. Known as the Shift (or dot) clock, it drives the two shift registers (A22 and A23). These registers bring in parallel data and shift it out as serial dot data.

The active low* shift clock is gated with the terminal count output of the C.clock (Character clock) counter. Together they drive a latch (A24, sheet 4) that holds data from character addresses 0 through 7, as well as the flip-flop (A31, sheet 4) that controls the DEL CURSOR signal.

A 4-bit binary counter (A3, sheet 6) divides the shift clock's rate by 14, creating eight 1.701 mHz clocks.

The C.clock, which is the time base for character generation, drives the CRT chip (6545, sheet 2). The active low C.clock has two purposes. It drives the Hex D flip-flops (A64 and A71) that time the CRTC RESET. It also controls the Stretch clock, which generates clock periods twice the normal length (1175ns vs. 588ns) upon command from the CPU.

This circuit (sheet 6) accesses slower memory or peripheral devices. The final output (called "00" or "Phase Zero clock") goes to the 6502 and all the peripheral chips. The Phase Zero clock controls the CPU bus timing, and it triggers all data transfers between the CPU and the other internal processors.

The DC.carry signals function as two clocks. The active high DC.Carry clock drives a flip-flop (A19, sheet 4) that is part of the video attribute circuitry. The active low DC.Carry clock is connected to the LD or Shift/Load enable lines (A22 and A23, pin 15, sheet 4) of two parallel-to-serial shift registers (A22 and A23). These registers are part of the characacter generation circuitry.

The XTAL1 clock drives UARTs A49, A50, and A51, which interface data to and from the terminal.

The QC clock combines with three RAM address lines (A15, sheet 3) to form a 1-of-10 decoder. The decoder's output goes to the chip select lines of each system RAM and each page of memory. The QC clock also deselects the RAM chips while the address lines are settling.

Line lock and smooth scroll are two 950 features not normally attainable with the 6545 CRT controller. To use them, additional circuity is required.

*The active low state is indicated by a bar above the signal name.

To achieve line lock, the top of the 6545's display register must be reloaded at the beginning of each character row. A general description of this circuitry follows.

To achieve smooth scroll, a CPU-loadable count-up counter (A60, sheet 4) must replace the 6545's internal scan line counter.

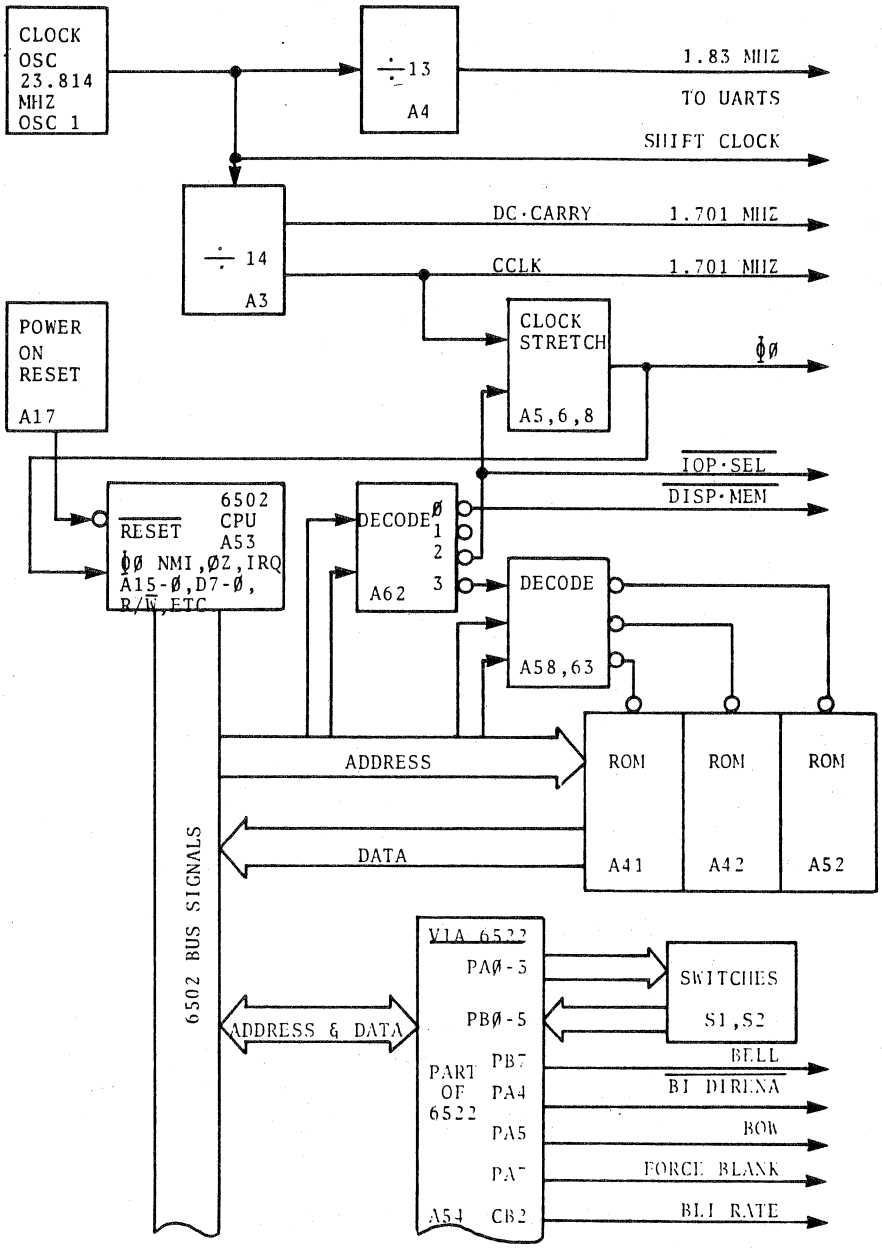


Figure 1 CPU, Timing, and Control

Display Controller

The 6545 (A55) generates each character's memory address in the display RAMS (A25 through A28) as it is to be displayed. It also generates the horizontal and vertical synchronization (synch) pulses necessary to control the deflection circuits of the monitor (CRT).

Note! In the text that follows, the term "scan line" refers to one of ten scan lines created by the electron beam, which makes up one data row.

The 6522's timer (T2) counts horizontal scan lines. When a specified number of scans have been executed, it interrupts the CPU (6502) with the NMI-interrupt. The CPU then loads the memory address of the next data row into the CRT controller (6545).

At the same time the NMI-interrupt is issued to the CPU, the CRTC reset timer (A64 and A71, sheet 7) is cleared, causing it to reset. The reset is released after seven C.CLK periods, and the CRTC starts timing the next character row. This operation allows the CPU to determine the order of the display lines so that some lines can be locked while others scroll.

To achieve a smooth scrolling effect, the number of scan lines in the character row and the starting scan line of each row must be specified.

The 6522's timer, which counts horizontal synch pulses, specifies the number of scan lines in the present character row. Normally, ten lines are used when smooth scroll is disabled. During a smooth scroll, this number ranges between 1 and 10 on the top and bottom rows.

To do this, the processor loads a 4-bit value into a latch (A61, sheet 4). When the CRTC is reset, this value is transferred to the counter (A60, sheet 4) and becomes the first scan line of the next data line. Each horizontal synch pulse then increases this value until the start of the next data line. At that point, it is preset again to a value determined by the CPU.

The CPU and the display controller share access to the system and display RAM during the alternate phase of the 6502's Phase 2 clock.

During the positive portion of the Phase 2 clock, the CPU address can be gated onto the RAM address bus through multiplexers (A43 through A46, sheet 2). A bidirectional transceiver (A14, sheet 3) passes data between the CPU data bus and the RAM data bus.

During the negative portion of the Phase 2 clock, the 6545 address bus (A55) is gated onto the RAM address bus, allowing the video data to be loaded into a latch (A24, sheet 4). This address becomes the input for the character generators and the attribute generation circuitry.

This alternating ("interleaved") access allows the processor to operate at normal speed without interruption or degradation of the display quality (which could be caused by accidental appropriation of the display bus by the processor as it accesses data).

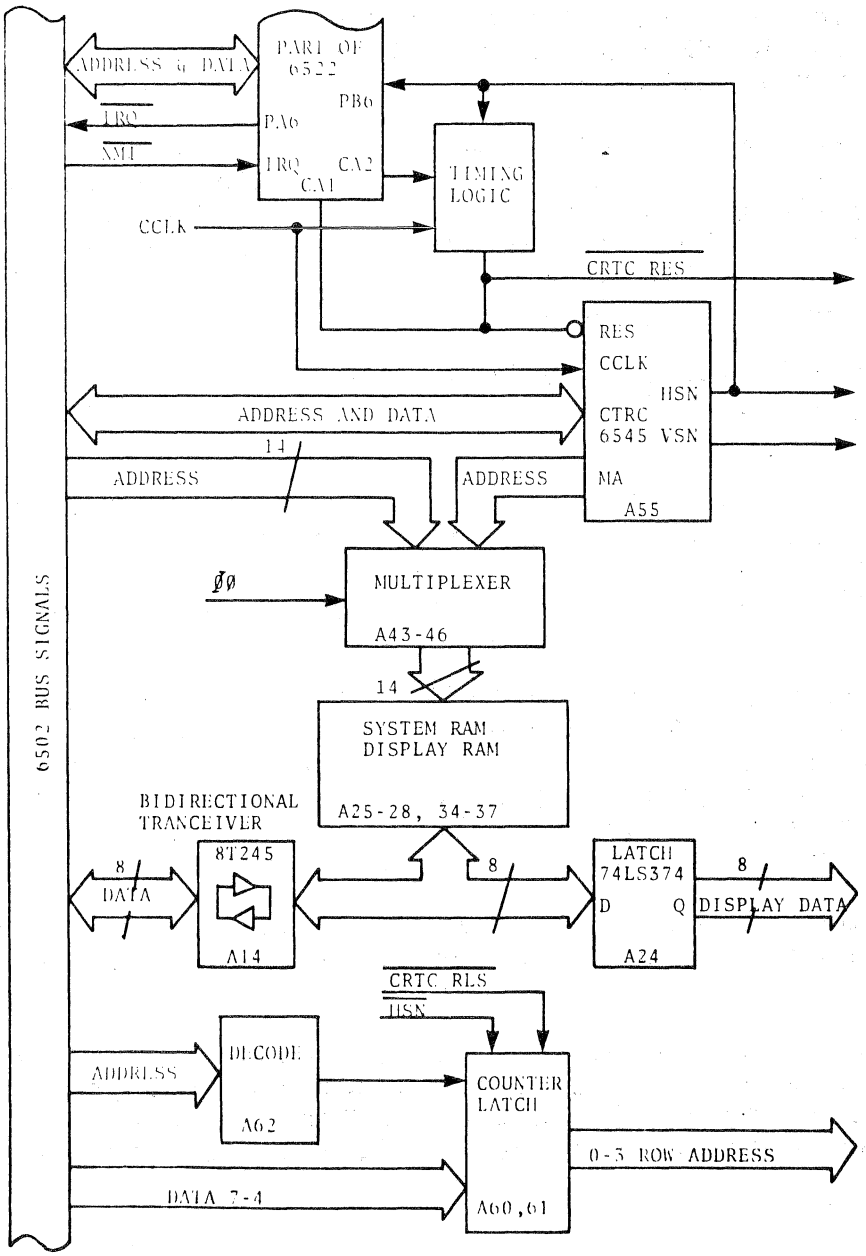


Figure 2 Display Controller

Video and Character Generation

To create the 950's display, the CRT scans horizontally from left to right, and vertically from top to bottom. Depending on the terminal's Hertz setting, the scan consists of 250 horizontal scan lines, each repeated 50 or 60 times per second. Each scan line displays 80 sections of 14-dot pixels. Each character line contains ten horizontal scan lines. This makes each character cell 14 pixels wide by 10 pixels high.

Characters are formed when the electron beam turns on individual pixels. The CRTC "MA" lines access the display memory once each character time (14 dot clocks). Once each cycle, the data from the display memory is then latched by the character address latch (A24, sheet 4). The output from this latch drives the eight most significant address lines of the character generator ROMs (A32 and A33, sheet 4).

The scan-line counter controls the four least significant address lines of the character generators. The scan-line counter's output changes only at the end of the scan line, when horizontal synch goes high.

The character generator's output is a 14-bit word that represents the pixel pattern to be displayed. The Shift clock loads this word into a 14-bit parallel-in/serial-out shift register (A22 and A23, sheet 4), and shifts it out, one bit at a time.

Thus, as the present pixel pattern of one character is loaded, the character address of the next character is latched. The bits shifted out of the shift register are mixed with display enable and the cursor and attribute data, creating the video output to the monitor. This signal turns the CRT's electron beam on and off as the beam sweeps the raster.

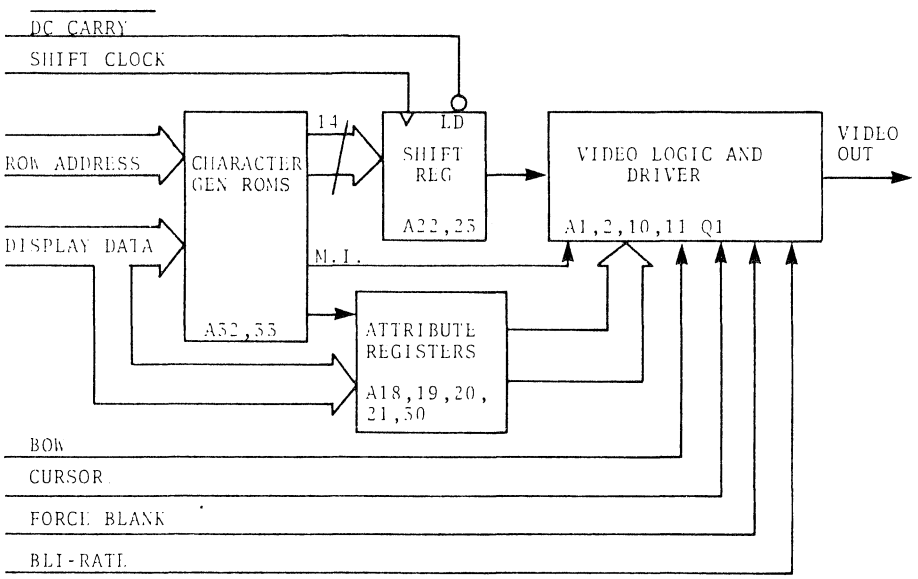


Figure 3 Video and Character Generation

Visual Attributes

The 950 has five visual attributes: half intensity, blink, blank, underline, and reverse video.

The only attribute created on a character-by-character basis is half intensity. All other attributes are "field" attributes; i.e. they have a specified starting and ending point. All characters between these points are affected by the attribute selected.

In the 950, attributes are stored in the display RAM just like displayed characters. An attribute character occupies a character space on the screen and is displayed as a half intensity space. The attribute becomes active immediately to the right of that space and remains in effect until the end of the screen.

Since an attribute is stored as a character in the display RAM, the character generation logic processes it as though it were a displayed character. However, the byte stored in RAM for an attribute character differs from that for a display character in that bits 4 and 7 are always set, while bits 5 and 6 are always reset.

Bits 0 through 3 define the active attribute. When the low-order character generator ROM (A33, sheet 4) is accessed by these codes (90 through 9F), the resulting data bit (A33, pin 17) is output as a high.

A21's data input comes from the output of a four-channel, two-to-one multiplexer (A20). While nonattribute characters are displayed, the multiplexer is driven by the output of A19. During an attribute character time, the output of Nand gate A11 is low, and it selects the A input to the multiplexer. This input connects with the output of the And gates that compare the previous attributes (output of A21) to the new attributes (output of A24).

If the previous attribute bit and the corresponding bit of the new attribute are both high, the output of the And gate is high. If one or both are low, the ouptut of the And gate is low and the attribute is turned off.

Thus, if an attribute is true for both the previous attribute and the new attribute, it is true while the new attribute is displayed on the screen. Otherwise, it turns off when the new attribute character starts.

The 950's attributes continue from character line to character line. Since any attribute on the previous line must be displayed on the current line until a new attribute is found, the logic must remember the last attribute of the previous line.

To summarize, A21's output is used by the video logic to turn visual attributes on or off. Its input can come from two sources: the output of the AND gates and the output of A19.

The output of the And gates defines the attribute(s) to be displayed during the attribute character, while A19's output determines the attribute(s) to be displayed during a nonattribute character.

A19's output is set to equal the previous character line's attribute until a new attribute is encountered. At that time, the output changes to the new attribute. A18 is used to remember the last attribute of a character in any character line.

Since each character line contains ten scan lines, the attribute data changes ten times. At the end of the displayed portion of each scan line, the Display Enable signal changes from high to low. This signal is then inverted and fed into a two-input Nand gate with the Delayed Display Enable signal, which changes one character time after Display Enable. Both signals are high only during the 81st character time of each scan line, creating a low pulse on the output of the Nand gate (A13 and A11). This pulse enables the output of a tri-state latch (A18).

A18's input comes from A20 and is latched only during the last scan line of the character row (pin 9, clock enable). This "remembers" the last attribute data of any character line. A18's output is latched into A19 at the end of the displayed portion of each scan line. A19's output then defines the attribute to be displayed during the current nonattribute character time.

The signals for Delayed Display Enable, Delayed Cursor, Dot Serial, Bow, Force Blank, and Visual Attribute Data are combined on sheet 6. They are gated together through A1, A9, A10, and A11, and are amplified to proper voltage and current levels by an NPN transistor Q1 (sheet 6). This transistor drives the video signal to the video module and/or external monitor (i.e. composite video).

Input/Output Circuits

Each of the three peripheral ports is controlled by a seperate 6551 UART.

UART A50 receives and transmits data for the main port (P3)
UART A51 receives and transmits data for the printer port (P4)
UART A49 receives data from the keyboard

The UARTs receive serial data, convert it to parallel data, and tie it directly to the CPU's data bus with input drivers, receivers, and switching circuits (A39, 40, 47, 48, 56, 57, 58, 50, sheet 5).

The use of seperate UARTs for the P3 and P4 ports allows the setting of different baud rates for each port.

The 1489 quadruple input line receivers (A57 and A40) convert RS232C voltage levels to TTL voltage levels. The 1488 quadruple output line drivers (A48 and A39) convert TTL voltage levels to RS232C voltage levels.

The output of A59, a quadruple 2-to-1 multiplexer, selects the output line drivers. A59 can select between two inputs (A or B), and route it to its respective outputs.

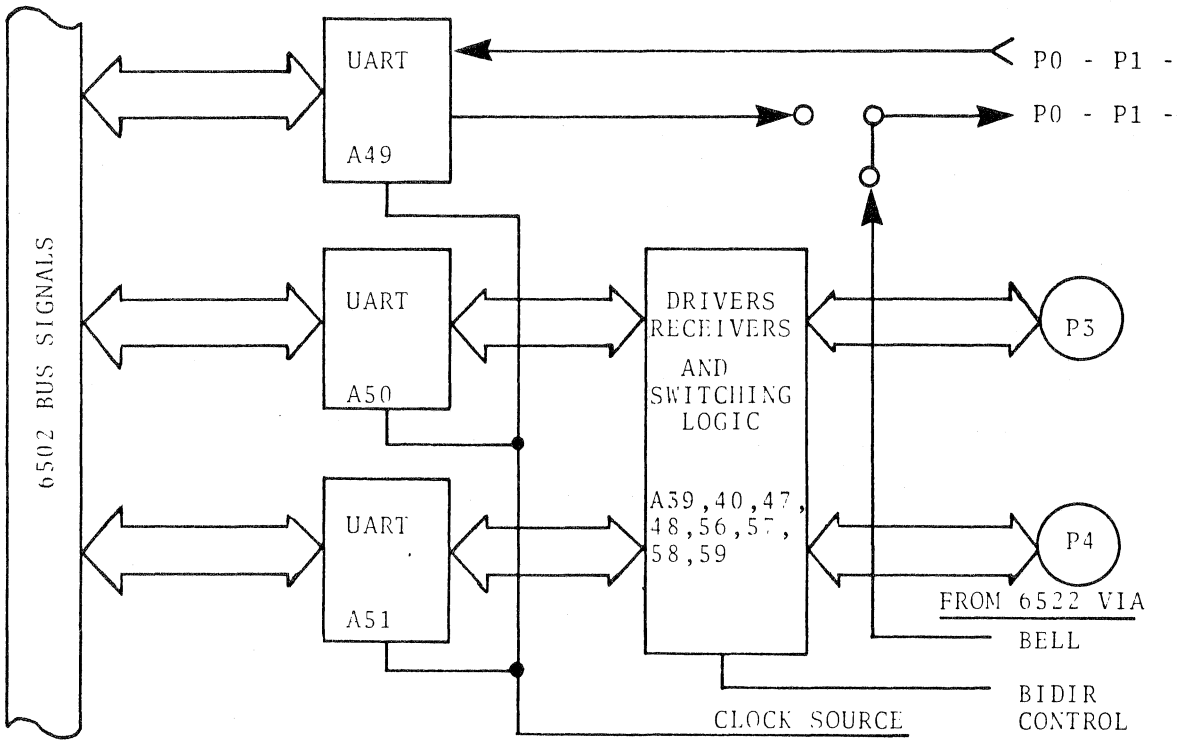


Figure 4 I/O Circuits

Overview

The 950 contains a microprocessor-based keyboard. The firmware monitors keyboard scanning, return-line testing, and communication with the control board.

In addition to the standard keyboard, additional parts let you create a keyboard that allows new key codes to be programmed into the keyboard PROM (2716).

Standard Keyboard (Version 1)

- Requires 5 volts (typical input current = 80 milliamps)
- 8048 microprocessor
- 1k byte ROM capacity (internal to the 8048)
- Asynchronous serial transmit and receive
- Baud rate = 1200 bits/sec.
- Word structure = 1 start bit, 8 data bits, 1 stop bit

Version 2 Keyboard with EPROM

- Requires 5 volts (typical input current = 150 milliamps)
- 8035 microprocessor
- 2K x 8 byte EPROM 2716 (external to 8035)
- Status display - 8 LED display
- Asynchronous serial transmit and receive
- Baud rate = 1200 bits/sec.
- Word structure = 1 start bit, 8 data bits, 1 stop bit

The Version 2 keyboard with the 2716 EPROM requires a larger memory map and storage capability in the microprocessor. Therefore, you must also change the standard 1K x 8B 8048 microprocessor to a 2K x 8B 8035.

To install it, cut jumpers A through M on the circuit side of the logic board and install the following components in the appropriate locations.

Components

U2,U3	74LS367
U4	75L5373
U5	EPROM (2716)
U7	74LS05
C2,C3	{.01uf cap}
C4,C5	{10% 50V}
R2	1K 5% 1/4 watt

Keyboard Layout

The keyboard contains 101 keys on a PC board, as shown in Figures 5-A and 5-B.

The key switches are arranged in an X-Y matrix (Figure 6). Only four special keys (CTRL, SHIFT, FUNCT, and ALPHA LOCK) are not included in the X-Y matrix.

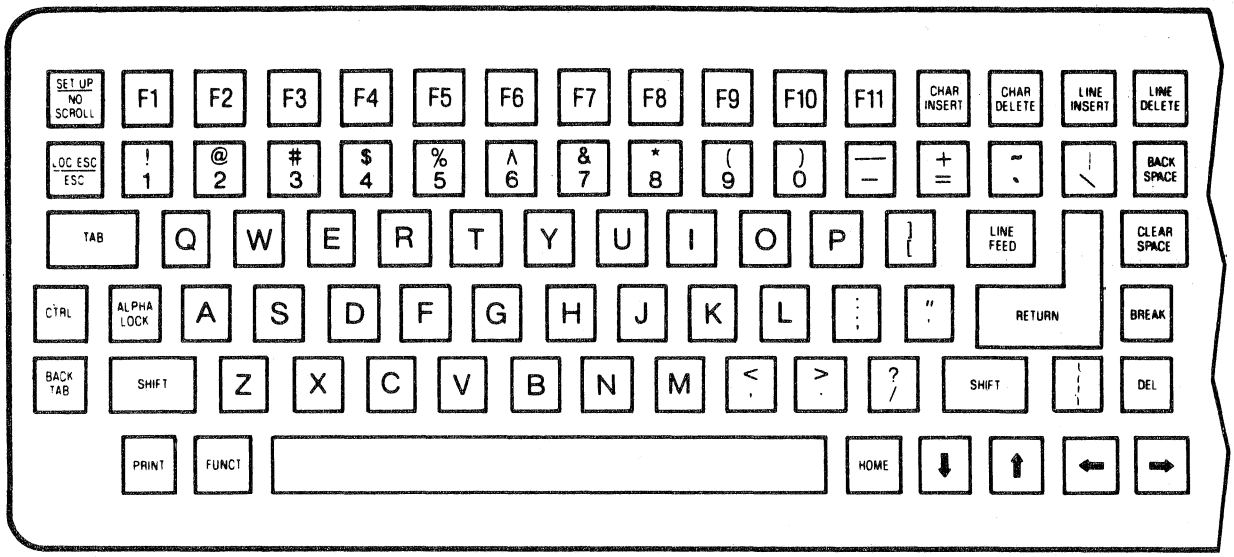


Figure 5-A Keyboard Layout

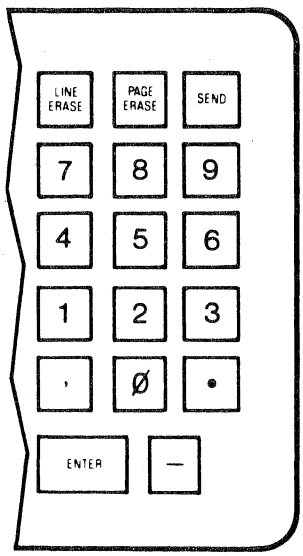


Figure 5-B
Keypad Layout

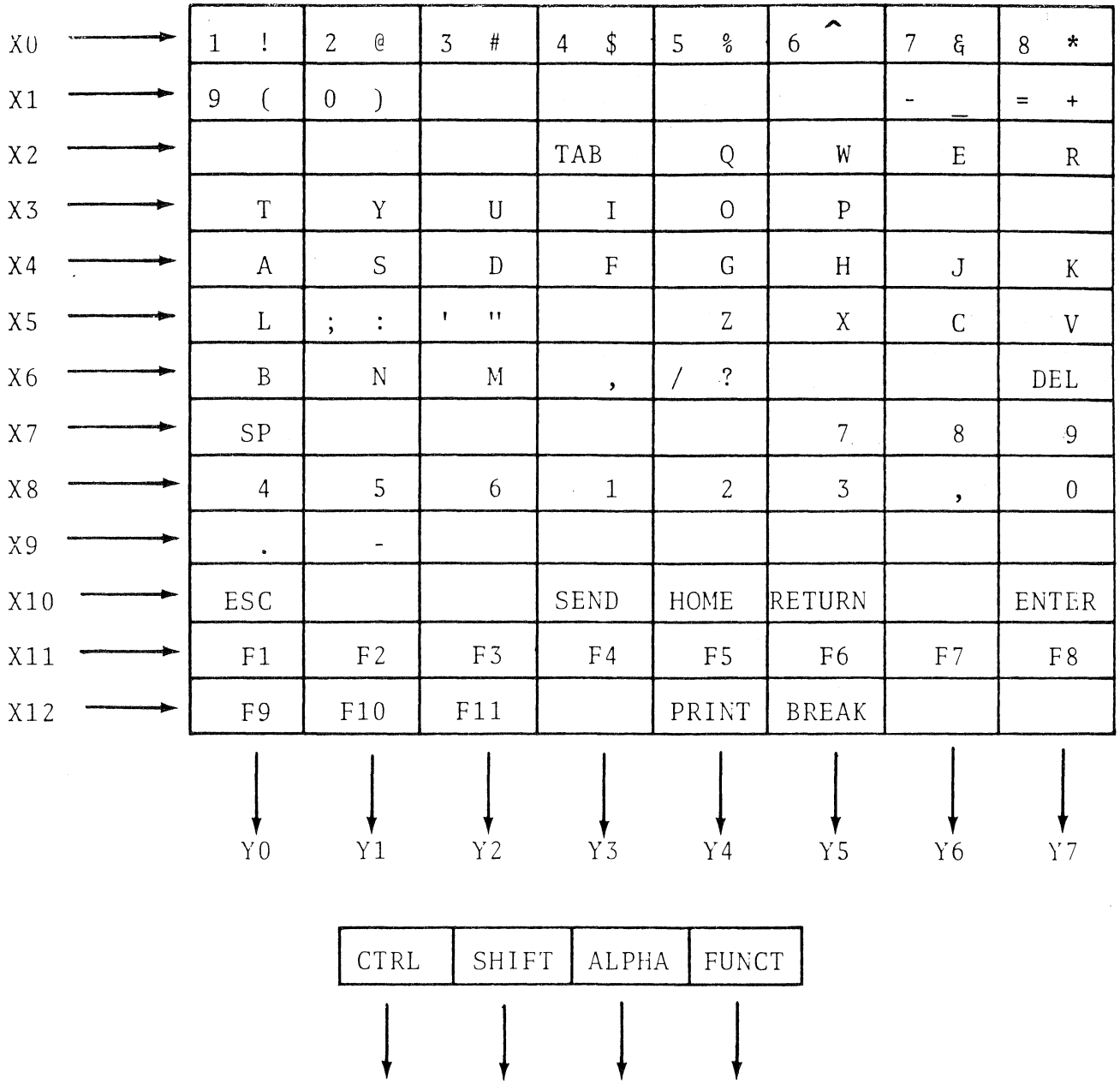


FIGURE 6 KEYBOARD X-Y MATRIX ARRANGEMENT

Keyboard Interface

Communication between the main control board and the keyboard controller is asynchronous. The standard asynchronous format used by the 950 (Figure 9) consists of one start bit, eight data bits, and one stop bit. The baud rate is set to 1200 bits/sec.

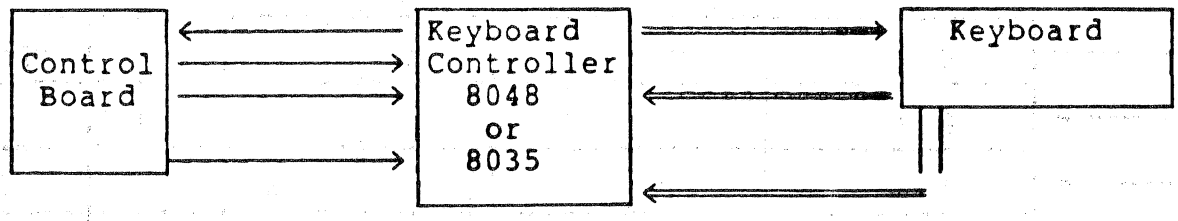


Figure 7 Keyboard Interface

Keyboard Scanning Method

The keyboard microprocessor (8048 or 8035) drives the scan lines (X lines), one at a time, to a low voltage. The return lines (Y lines) are tested by the microprocessor.

The keyboard matrix output ports (10 through 14, 20 through 27) latch the X0 through X12 lines to the keyboard. The connections are shown in Figure 7.

Whenever a low voltage is detected on a Y input line, it means that a key has been depressed. That key is at the intersection of the driven line (X) and the detected line (Y).

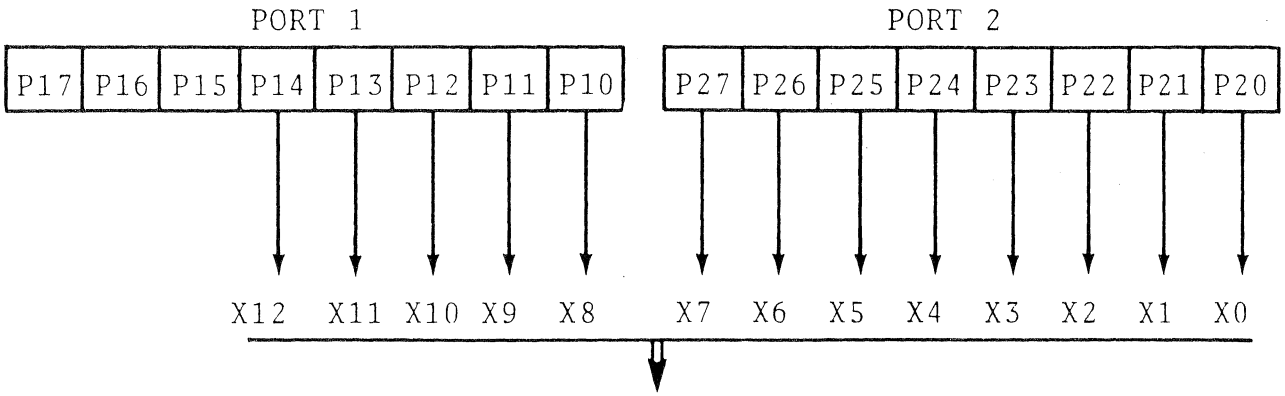


FIGURE 8 8048 PORTS

The return matrix lines (Y lines) from the keyboard are read by the microprocessor's data bus (D0 through D7). The connections are shown in Figure 8.

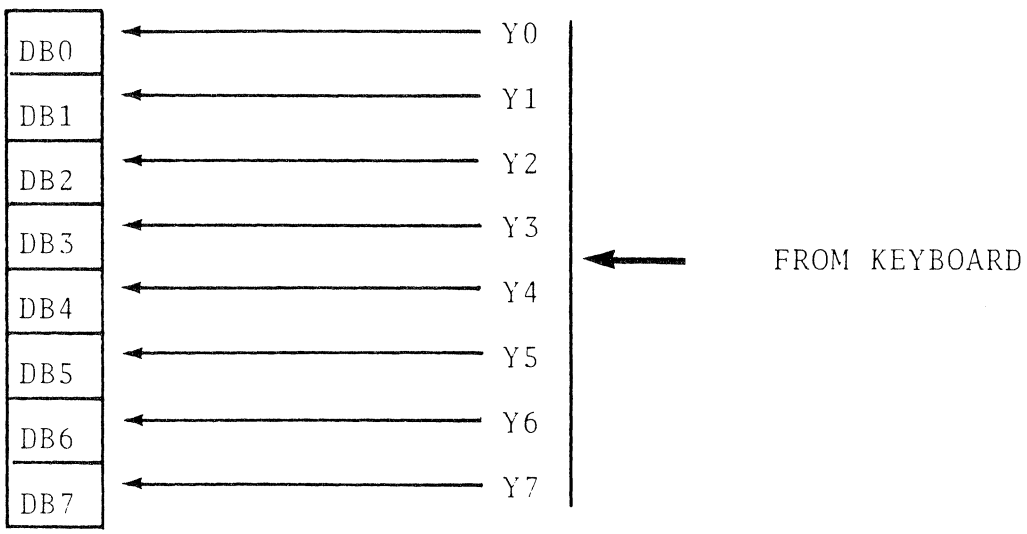


FIGURE 9 8048 DATA BUS

Basic Scan Routine

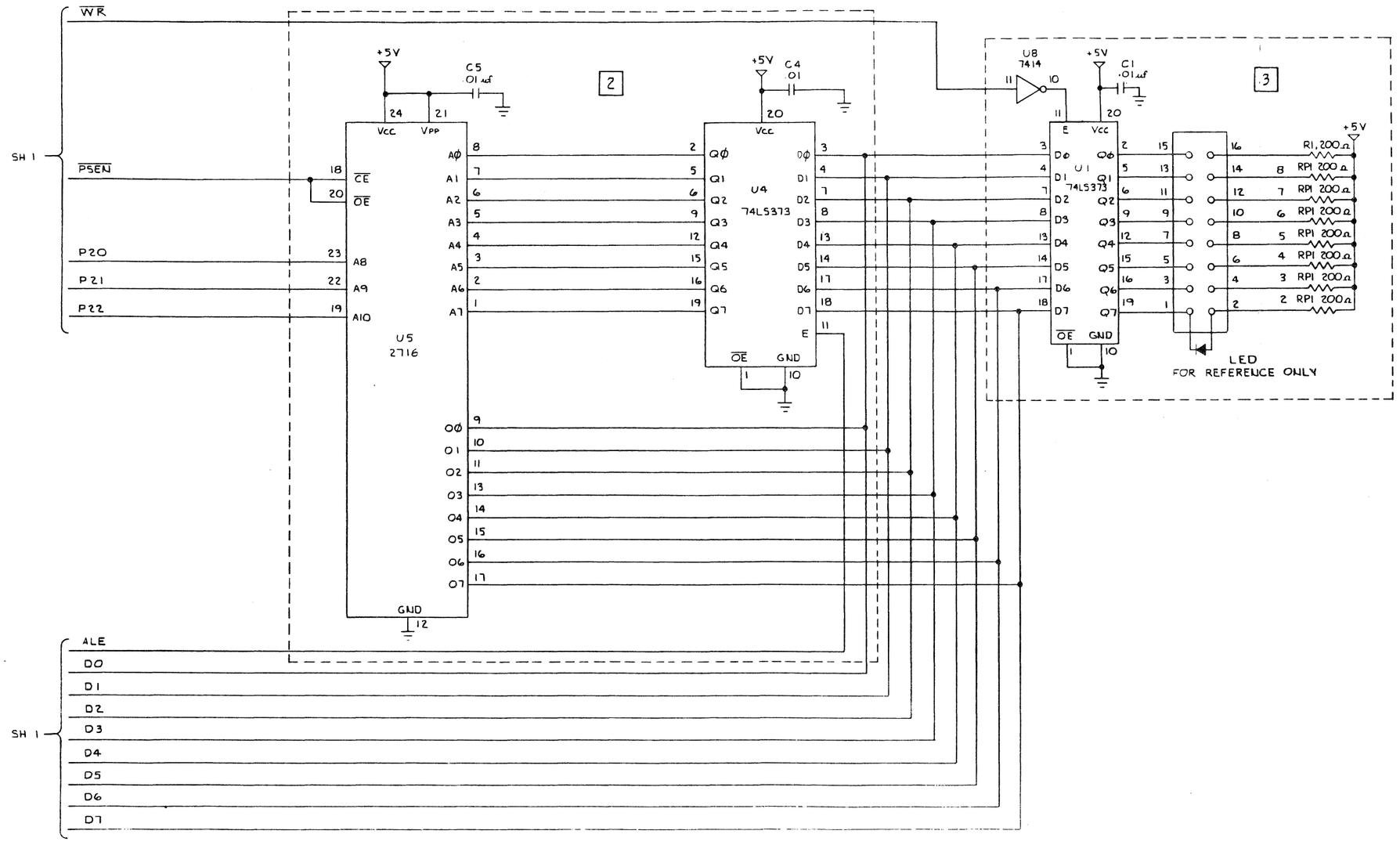
Starting the scan routine resets the transmit flag and enables the external interrupt for receiving status from the control board.

The keyboard matrix is scanned from the top row to the bottom row. As soon as a key is pressed, the row is tested bit by bit, from left to right. The matrix key codes are immediately encoded and stored in two registers (NEWKY 1 and NEWKY 2).

If the results of a matrix scan indicate that more than two keys are depressed, the program enters a delay loop for 11 ms. Meanwhile, the whole matrix is read once again to verify that the key is still depressed. After the key is proven to be valid, the microprocessor sends the proper code to the terminal.

If the depressed key is a repeat key, the last portion of the scan routine controls the length of the repeat delay (0.5 sec.) and the autorepeat rate (16 char/sec.). The program then branches back to the beginning of the scan routine.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		



APPLICATION			TeleVideo
NEXT A	USED ON		PCB SCHEMATIC
			950 KEYBOARD
			513
			SIZE D · SHT 2 OF 2 · DRAWING 2003-300 · REV D

D
2003-00

2K x 8 INIT.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 40		
	A1	" " ECO 45		
	B	" " ECO 41, 47		
	B1	" " ECO 54		
	B2	" " ECO 70, 82	9/21/81	
	B3	" " ECO 0438, 0442	4/16/82	

A69 74LS04 — A70 74LS00 — A63 74LS32 — A58 74LS32 — A62 74LS139 — A52 2332 — A42 2716/2332 — A41 2332/2564 8K×8 SYS ROM — A53 6502A

R24 1K, R23 1K, R39 3.3K, R45 3.3K, R46 3.3K — +5V

E20 E18 E17 E15 E14 E19 E16 E22 E23 E26 E21 E27 E28

SH 5,7 IRQ — SH 7 NMI — SH 6 ΦO — SH 6 RESET

DISP. MEM. — TOP. SEL. — SH 2,6 — SH 2,5,6,7

SCREG SEL — SH 4

P8-1 P8-2 P8-3 P8-8 P8-7

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15 R/W Φ2 DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

SH 2,5,7 — SH 2,5,7 — SH 2,7 — SH 2,7 — SH 2 — SH 2,5 — SH 2,5 — SH 2,5 — SH 2 — SH 2,6,7 — SH 2,3,5,7 — SH 2,5,7 — SH 2,3,5,7

B5	PROD REL PER ECO 0483	1/26/82	
B4	PROD REL PER ECO 0473		

APPLICATION		UNLESS OTHERWISE NOTED	DWN O. Caballero 9-25-80
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O. Caballero 9-25-80
		ANG ± PLC .2 PLC .4 PLC	ENGR T. Lilly 9/21/81
			APPD
		SCALE: NONE	APPD
		MATERIAL	APPD
			FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD. 5/4

SIZE D — SHT 1 OF 7 — DRAWING NO. 2009800 — REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 7 CRTC.RESET
SH 6 CCLK
SH 1 ABØ
SH 1 R/W
SH 1 DBØ DB1 DB2 DB3 DB4 DB5 DB6 DB7
SH 1 IO.P.SEL
SH 1 Ø0
SH 1 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 DISP.MEM
SH 6 SEL.CPU.ADDR.

+5V

A55 6545
Vcc 20
RES 2
CCLK 21
RS 24
R/W 22
DBØ 33 DB1 32 DB2 31 DB3 30 DB4 29 DB5 28 DB6 27 DB7 26
CS 25 Ø2 23 Vss 1

HSYNC 39 → HSN → SH 7
VSYNC 40 → VSN → SH 4,6
ENABLE 18 → DISPL.ENA → SH 4
CURSOR 19 → CURSOR → SH 4
RAØ 38 RA1 37 RA2 36 RA3 35 RA4/STB 34
MAØ 4 MA1 5 MA2 6 MA3 7 MA4 8 MA5 9 MA6 10 MA7 11 MA8 12 MA9 13 MA10 14 MA11 15 MA12 16 MA13 17

A63 74LS32 (13, 12 → 11)
A63 74LS32 (10, 9 → 8)
R25 1K

A46 74LS157 (DMEM.EN, AD.RAM.13, AD.RAM.12)
A45 74LS157 (DM.R/W, AD.RAM.11, AD.RAM.10, AD.RAM.9, AD.RAM.8)
A44 74LS157 (AD.RAM.7, AD.RAM.6, AD.RAM.5, AD.RAM.4)
A43 74LS157 (AD.RAM.3, AD.RAM.2, AD.RAM.1, AD.RAM.Ø)
SEL.CPU.ADDR. → SEL

SH 3 SH 3 SH 3 SH 3

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Q Corvallano 9-24-86	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK Q Corvallano	TITLE: PCB SCHEMATIC 950 CONT. BD. 515
			ENGR	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE B SHT 2 OF 7 DRAWING NO. 2009800 REV 85

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	BS	SEE SHT 1		

SH 2 AD.RAM 13
SH 2 AD.RAM 11
SH 2 AD.RAM 12
SH 2 QC.CLK
SH 6

A15 74LS42

A8 74LS04

A16 74LS32

A16 74LS32

SH 2 AD.RAM 10
AD.RAM 9
AD.RAM 8
AD.RAM 7
AD.RAM 6
AD.RAM 5
AD.RAM 4
AD.RAM 3
AD.RAM 2
AD.RAM 1
AD.RAM Ø

A25 2114
A26 2114
A27 2114
A28 2114
A34 6116
A35 6116
A36 6116
A37 6116

SH 2 DM.R/$\overline{W}$

SH 1 DB.7
DB.6
DB.5
DB.4
DB.3
DB.2
DB.1
DB.Ø

A14 8T245

SH 2 $\overline{DMEN.EN}$
SH 1 R/$\overline{W}$

CH.AD.7
CH.AD.6
CH.AD.5
CH.AD.4
CH.AD.3
CH.AD.2
CH.AD.1
CH.AD.Ø
SH 4

B600002-001

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± PLC .x ± PLC .xx ±
SCALE: NONE
MATERIAL
FINISH

DWN O. Cruickshank 9-25-80
CHK O. Cruickshank 9-25-80
ENGR
APPD
APPD
APPD

TeleVideo, Inc.

TITLE PCB SCHEMATIC 950 CONT. BD. SH 2

SIZE B | DRAWING NO. 2009800 | REV 85
SHT 2 OF 4

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
	B5	SEE SHT 1	

4K x 8

SH 3 { CH·AD·7, CH·AD·6, CH·AD·5, CH·AD·4, CH·AD·3, CH·AD·2, CH·AD·1, CH·AD·Ø

SH 7 { CRTC·RES, HSN

SH 1 { SCREG SEL., DB4, DB5, DB6, DB7

A24 74LS374 (8-bit D FF)

A60 74LS191 (4-bit U/D counter)

A61 74LS174 (6-bit D FF, MR)

R38 1K +5V

SH 6 SHIFT.CLK, SH 6 DC CARRY → A13 74LS00

SH 2 VSN

A18 74LS173 (4-bit D FF)

R14 1K +5V

E5, E6

DEL.DISPL.ENA, DISPL.EN → A13 74LS00

A2 74LS04

SH 6 SHIFT.CLK

SH 6 ROW 9 → A12 74LS04

SH 6 DISPL.ENA → A12 74LS04

A9 74LS00, A9 74LS00, A29 74LS08

SH 6 VSYNC (VSN)

A19 74LS174 (CLR)

A30 74LS08, A30 74LS08, A30 74LS08

A32 2332, A33 2332

R19 1K +5V

R20 1K +5V

VPP

74LS00 → A11

A20 74LS157 (SEL, STRB)

DC CARRY SH 6

CURSOR SH 2

A22 74LS166 (CLR, S.IN, CK, CK INH, LD, QH)

A23 74LS166 (LD, CLR, S.IN, CK, CK.INH, QH)

R16 1K +5V

R17 1K +5V

RAØ SH 6

RA3 SH 6

DOT SERIAL SH 6

A13 74LS00 → C75 100 pf

A12 74LS04

R18 1K +5V

A31 74LS74 (PR, CLR)

DEL CURSOR SH 6

A21 74S174 (CLR)

R15 1K +5V

UNDERLINE
REVERSE·VIDEO
BLINK
BLANK
DEL.DISPL.EN–
HALF·INTENSITY
→ SH 6

P10-1

ROW·9 SH6
DISPL·EN– SH4

B600002-001

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG 2 PLC 3 PLC

SCALE: NONE

MATERIAL

FINISH

DWN O. Castellano 9-25-86

CHK O. Castellano 9-

ENGR

APPD

APPD

APPD

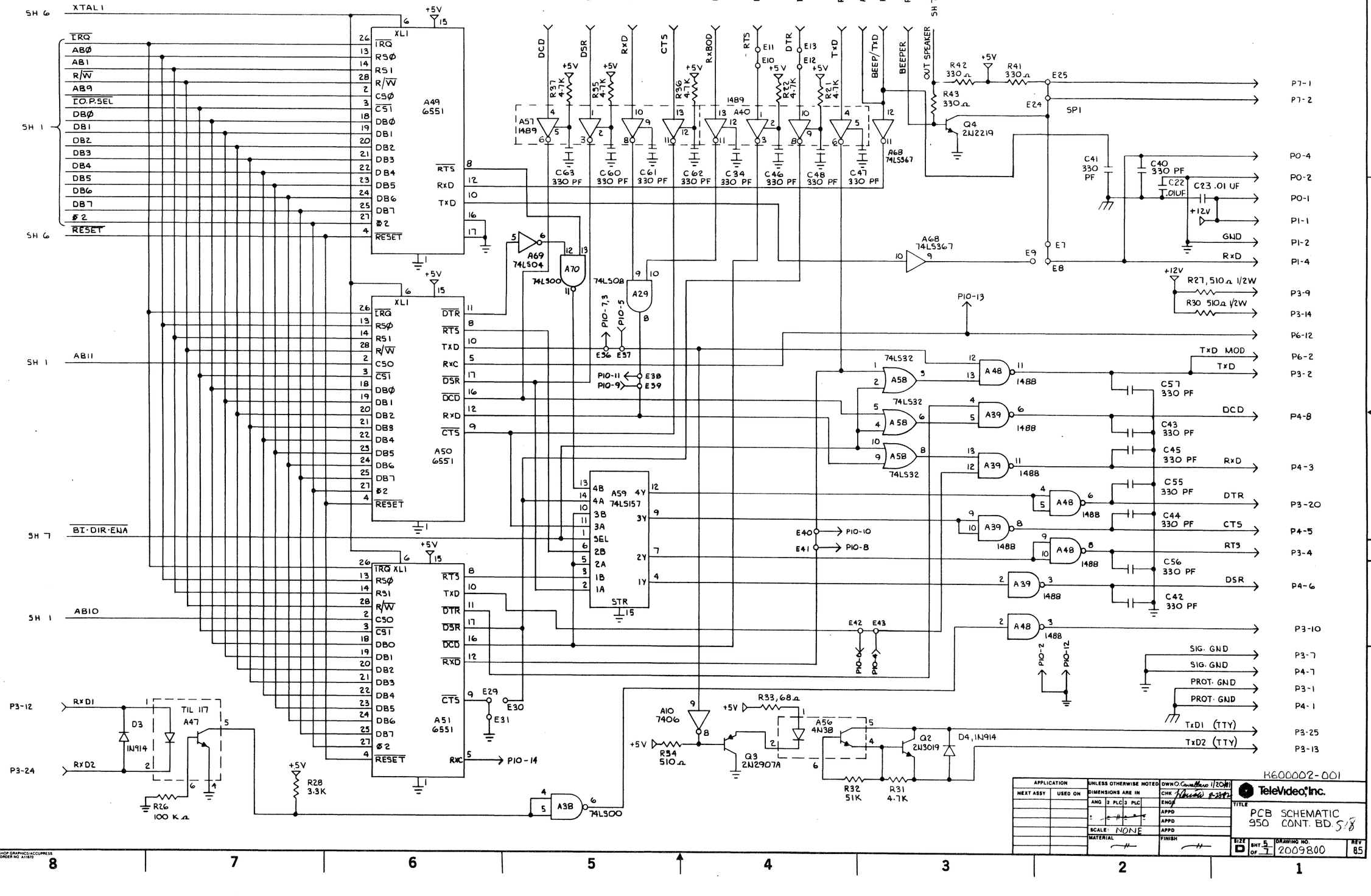
TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD. S/7

SIZE B SHT 4 OF 7 DRAWING NO. 2009800 REV B5

ATTRIBUTE Registers A19, A20, A21, A30

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Carvalho 1/20/81
NEXT ASSY	USED ON		CHK
		ANG 2 PLC 3 PLC	ENGR
			APPD
		SCALE: NONE	APPD
		MATERIAL	APPD
			FINISH

K600002-001

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD. 5/8

SIZE	SHT 5 OF 7	DRAWING NO.	REV
D		2009800	85

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 2 RA Ø
SH 2 RA 3
SH 7 BLACK·ON·WHITE (B·O·W)
SH 4 BLINK
SH 7 BLI·RATE
SH 4 BLANK
DOTS·SERIAL
ROW·9
UNDERLINE
DEL CURSOR
REVERSE VIDEO
DEL DISPL·EN –
HALF·INTENSITY
SH 7 FORCE·BLANK
SH 2 VSN
SH 7 HSN
SH 1 DISP·MEN
SH 1 IO·P·SEL
SH 1 AB13

74LS00 A11, A11, A9, A1
74LS04 A2
74LS86 A1
74LS00 A9
74LS86 A1
74LS04 A10
74LS04 A10
74LS04 A10
74LS04 A10
74LS04 A10
74LS04 A2
74LS86 A1
74LS04 A2
74LS32 A16
74LS04 A12, A12
74LS00 A13
ROW 9 SH 4
C9 0.01 µf

R5 1K
R6 750Ω
R3 1K
R4 270Ω
R1 1K
R2 68Ω
R7 22Ω
+5V
E1 E2
E3
E4
D1 1N914
Q1 2N2219
C6 4.7µf

+12V P8-5, P8-6, P6-1, P6-14
+5V P6-6, P6-9
-12V P6-5, P6-10
GND P6-7, P6-8, P8-9, P8-10
P2-4
P2-3
SH 4 COMP.V+TTL VIDEO P2-6
+VSYNC (VSN) P2-5
+HSYNC. P2-1
SEL·CPU·ADDR SH 2
DC.CARRY SH 4
C.CLK SH 2
DC.CARRY SH 4
C.CLK SH 7

R8 1K +5V
74LS163 A3 EN EN CLR ÷14 TC QD QC LD CLK
OSC.1 K1114A 23.814 MHZ
E33 E32
A12 74LS04
74LS32 A16
A2 74LS04
A8 74LS04
A5 74LS00
R10, 1K +5V
74LS109 A6 PR J Q CLK K CLR
Clock Stretch
A5 74LS00
R11 3.3K
R12 1M
R13 47K
A17 555 TIMER
C13 .01µf
C12 .01µf
C15 10µf
1N914 D2
R29 4.7K
A8 74LS04
C49 .01µf
RESET SH 1,5,7
Ø 0
SH 1 SHIFT.CLK.
SH 4 SHIFT·CLK
SH 4 XTAL1
SH 5 QC CLOCK
SH 3

R9, 1K +5V
74LS163 A4 EN EN CLR ÷13 QD QC QB QA LD CLK
74LS00 A7, A5
74LS08 A7

H600002-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN O. Castellanos 9-25-86	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O. Castellanos 9-25-86	TITLE
		ANG ± 2 PLC ± 3 PLC	ENGR	PCB SCHEMATIC
			APPD	950 CONT. BD. 5/9
		SCALE: NONE	APPD	
		MATERIAL —	FINISH —	SIZE B SHT 6 OF 7 DRAWING NO 2009800 REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 1 { DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ
SH 1 { ABØ AB1 AB2 AB3
SH 1 R/W
SH 1 ØO
SH 6 RESET
SH 1 IO.P.SEL
SH 1 AB 13
SH 1 NMI
SH 5 IRQ

+5V → 20 Vcc

A54 6522A

DB7 26 · DB6 27 · DB5 28 · DB4 29 · DB3 30 · DB2 31 · DB1 32 · DBØ 33
RSØ 38 · RS1 37 · RS2 36 · RS3 35
R/W 22 · Ø2 25 · RES 34 · CS1 23 · CS2 24 · IRQ 21 · PA6 8 · PB6 16
GND 1

CB2 19 · PA7 9 · PB7 17 · PBØ 10 · PB1 11 · PA3 5 · PA5 7 · PA2 4
PB2 12 · PB3 13 · PB4 14 · PB5 15 · PA4 6 · PA1 3 · PAØ 2 · CA1 40 · CA2 39

SH 5 BL1·RATE
SH 6 FORCE BLANK

+5V → RP4 RES. 1K (4 2 3 5 6) · RP1 RES. 1K (6 7 8)

A68 74LS367 (GND G2 1A 2A 3Y)
A67 74LS367 (GND 1A 2A 3A 4A 5A 6A)
A66 74LS367 (GND 1A 2A 3A 4A 5A 6A)
A65 74LS367 (GND 1A 2A 3A 4A 5A 6A)

OUT SPEAKER — SH 5
BLACK·ON·WHITE (BOW) — SH 6
BI.DIR.ENA — SH 5

+5V → RP3 RES. 1K (4 5 7 6 2 4 6 8) · RP2 RES. 1K (7 5 3 2)

+5V → R40 1K

A69 74LS04 (3 4 5) → 74LS00 A70 (4 5 6) → A64 74LS174 (CLR, 1D 2D 3D 4D → 4Q 5Q 6Q, CLK 9, GQ 15)

A69 74LS04 (9 8) → 74LS00 A70 (9 10 8) → CRTC RESET — SH 2,4

A71 74LS174 (CLR 13, D 12, CLK 11, Q 9, PR 10)
+5V → R44, 1K

A69 74LS04 (11 10)

SH 2 HSN
SH 6 C·CLK
SH 6 HSN

P5-5 +12V → +12V
P5-1 -12V → -12V
P5-4 +5V → +5V
P5-3 GND → GND

D5 IN4001 · C72 22 mf · C71 22 mf · C2-5,9-14,16,25 .01 mf · C1,7,8,31-33,37-39, 30,36 0.1 mf · 19-54,58,59 68-6B33,78 · C69 22 mf
C59 .01 mf · C58 .01 mf · C66 .01 mf · C67 .01 mf

B600002-001

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN: ANG ± 2 PLC, .x ± .1, .xx ± .05
SCALE: NONE
MATERIAL

DWN Q. Castellano 9-27-84 · CHK B. Castellano 9-28-84 · ENGR · APPD · APPD · APPD · FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD. 5.2V

SIZE B · SHT 1 OF 1 · DRAWING NO. 2009800 · REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 0333		
	A2	PROD REL PER ECO 0395		
	B	REVISED PER ECO 0456		
	B1	" " ECO 0554		
	~~B2~~	" " " ~~0544~~		

ZONE B3 LTR RECORD CHANGES PER ECO # 2010 DESCRIPTION 2/10/83 DATE APPD

B3 2009801

SH 6 — E19, E16, EX

E20 E18 E17 E15 E14 E19 E16

E44 E45

+5V R16 1K → A20 2532 (OE/CS, CS/A11) — R17 1K → A25 2532 (PD/PGM, A11, A12) — E27 E28

A15 2332 (CS, A11, A0–A10, I/O1–I/O8, VCC, GND)

A11 G502A

SH 7 — IRQ → IRO; NMI → NMI

SH 4 — Φ → Φ0

SH 7 — RESET → RESET

R39 3.3K, R38 3.3K, R23 3.3K → +5V

ABØ–AB15, R/W, Φ2, DBØ–DB7

E21 E22 E23 E26

E23 → SH 6

PII-8, PII-7, PII-5, PII-3

ABØ, AB1 → SH 2,5,7

AB2, AB3 → SH2,7

AB4–AB8 → SH2

AB8 → SH2,6

AB9–AB11 → SH2,5

AB12 → SH 2,6

AB13 → SH2,6,7

AB14, AB15 → SH 6

R/W → SH2,3,5,6,7 → PII-20

DBØ–DB3 → SH 2,3,5,7

DB4–DB7 → SH2,3,5,6,7

P8-1, P8-2, P8-3, P8-8, P8-7

NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACITORS ARE VALUED IN µF, 16VDC, ±20%
3. DRAWINGS COMFORMS WITH TELEVIDEO SPEC. 212730

B600002-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H HUR 3-8-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG 2 PLC 3 PLC	ENGR	TITLE
		± ± ±	APPD	PCB SCHEMATIC
		SCALE	APPD	CONT. BD 950 G/A 521
		MATERIAL	APPD	
		FINISH		SIZE D SHT 1 OF 7 DRAWING NO. 2009801 REV B3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	.	SEE SHT 1		

+5V
20 VCC

SH6 CRTC. RESET
SH4 CCLK
2 RES
21 CCLK

HSYNC 39 → HSN → SH6
VSYNC 40 → VSN → SH4,6
ENABLE 18 → DISPLENA
CURSOR 19 → CURSOR
→ SH4
RAØ 38 → P11-22
RA1 37 → P11-23
RA2 36
RA3 35
RA4/STB 34

SH1 ABØ, R/W
24 RS
22 R/W

A6 G545
1 VSS
3 LPEN

SH1 DBØ DB1 DB2 DB3 DB4 DB5 DB6 DB7
33 DBØ
32 DB1
31 DB2
30 DB3
29 DB4
28 DB5
27 DB6
26 DB7

MAØ 4
MA1 5
MA2 6
MA3 7
MA4 8
MA5 9
MA6 10
MA7 11
MA8 12
MA9 13
MA10 14
MA11 15
MA12 16
MA13 17

CS 25 Ø2 23

SH6 SEL CRTC
SH4 ØO

SH1 AB1 AB2 AB3 AB4 AB5 AB6 AB7

SH1 AB8 AB9 AB10 AB11

SH1 AB12 AB13
SH6 DISP. MEM

+5V
R11 4.7K

A7 74LS157
AI2 74LS157
A16 74LS157
A21 74LS157

SH6 SEL.CPU.ADDR

DMEM.EN, AD.RAM.13, AD.RAM.12 → SH3
AD.RAM.11, AD.RAM.10, AD.RAM.9, AD.RAM.8 → SH3
AD.RAM.7, AD.RAM.6, AD.RAM.5, AD.RAM.4 → SH3
AD.RAM.3, AD.RAM.2, AD.RAM.1, AD.RAM.Ø → SH3

B600002-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H HUR 3-8-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG 2 PLC 3 PLC	ENGR	TITLE: PCB SCHEMATIC CONT. BD 950 G/A S22
		SCALE	APPD	
		MATERIAL	APPD	
		FINISH	APPD	SIZE D, SHT 2 OF 7, DRAWING NO 2009801, REV B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT1		

SH2 AD.RAM.13
AD.RAM.11
AD.RAM.12
SH4 QC CLK
A2 74LS42
SH2 AD.RAM.10
AD.RAM.9
AD.RAM.8
AD.RAM.7
AD.RAM.6
AD.RAM.5
AD.RAM.4
AD.RAM.3
AD.RAM.2
AD.RAM.1
AD.RAM.Ø
A3 6116
A8 6116
A13 6116
A17 6116
A22 6116
SH6 DM.R/$\overline{W}$
SH1 DB.7
DB.6
DB.5
DB.4
DB.3
DB.2
DB.1
DB.Ø
A26 8T245
OE DIR
SH2 $\overline{DMEN.EN}$
SH1 R/$\overline{W}$
CH.AD.7
CH.AD.6
CH.AD.5
CH.AD.4
CH.AD.3
CH.AD.2
CH.AD.1
CH.AD.Ø
SH4
DB.7 → P11-24
DB.6 → P11-18
DB.5 → P11-15
DB.4 → P11-16
DB.3 → P11-13
DB.2 → P11-12
DB.1 → P11-11
DB.Ø → P11-10
P5-5 +12V → +12V
P5-1 -12V → -12V
P5-4 +5V → +5V
P5-3 GND → GND
CR1 IN4001
C2 22 50v
C3 22 50v
C27-55 C57-68 .01
0.1
C1 22 50v
C69 .01
C70 .01
C71 .01
C72 .01

APPLICATION		UNLESS OTHERWISE NOTED	DWN HHUR 3-9-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG ± 2 PLC ± 3 PLC ±	ENGR	TITLE PCB SCHEMATIC CONT. BD 950 G/A
		SCALE	APPD	
		MATERIAL	APPD	
			APPD	
			FINISH	

B&K0002-002

SIZE D | SHT 3 OF 7 | DRAWING NO 2009801 | REV B3

B | B3 | 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH3: CH.AD.7, CH.AD.6, CH.AD.5, CH.AD.4, CH.AD.3, CH.AD.2, CH.AD.1, CH.AD.Ø

A27 74LS374 (6D 3D 4D 5D 1D 8D 2D 7D, CLK, OE; 6Q 3Q 4Q 5Q 1Q 8Q 2Q 7Q)

SH6: RAØ, RA1, RA2, RA3

+5V — R18 4.7K

A30 2332 (VPP, VDD; A11 A10 A9 A8 A7 A6 A5 A4 CS; AØ A1 A2 A3; Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8)

R19 4.7K

A31 2332 (AØ A1 A2 A3 VPP; A11 A10 A9 A8 A7 A6 A5 A4 CS; VDD; Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8)

OSC1 K1114A 23.814 MHZ A45 — E32, E33

C24 47PF 50V; C23 20PF 50V; R41 33

LCHADØ LCHAD1 LCHAD2 LCHAD3

CG 15 CG 14 CG 13 CG 12 CG 11 CG 10 CG 9 CG 8 CG 7 CG 6 CG 5 CG 4 CG 3 CG 2 CG 1 CG Ø

SH7: B.O.W.
SH6: CLOCK EXTEND
SH6: ROW 9
SH2: VERT SYNC
SH6: HORIZ SYNC
SH2: DISPLAY ENABLE, CURSOR
SH7: BLINK RATE

CHAR LATCH OUT EN, LATCH CHAR, B.O.W., CLOCK EXTEND, SHIFT CLOCK, ROW 9, VERT SYNC, HORIZ SYNC, DISP.EN, CURSOR, BLINK RATE

A34 GATE ARRAY I740012-008

Ø0 → SH 1,2,5,6,7
XTAL 1 → SH5
CHAR CLOCK → SH2,6
QC CLOCK → SH3
COMPOSITE VIDEO, HALF INTENSITY, VIDEO → SH6
VSS

SHIFT CLOCK → P11-21

P3-12 RXDI — CR3 IN914 — TIL 117 A10 — R40 100K

P3-24 RX D2

R15 3.3K — A14 (74LS00) — A18 (1488) → P3-10

SIG.GND → P3-7, P4-7

PROT.GND → P3-1, P4-1

R4 68 — R5 510 — 4N38 A5 — Q2 2N2907A — Q3 2N3019 — CR2 IN914 — R10 51K — R9 4.7K

SH5 TXD — A14 (74LS00)

TXDI (TTY) → P3-25
TXD2 (TTY) → P3-13

+12V — R1 510 → P3-9; R2 510 → P3-14

+5V → P6-6, P6-9, P11-1, P11-2

+12V → P6-1, P6-14, P8-5, P8-6, P11-6

-12V → P6-5, P6-10, P8-9, P8-10, P11-14

E36 → P11-25

P6-7, P6-8, P10-2, P10-12, P11-9, P11-19

APPLICATION		UNLESS OTHERWISE NOTED	DWN	HUR 3-10-82
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG ± 2 PLC ± 3 PLC ±	ENGR	
		SCALE	APPD	
		MATERIAL	APPD	
			FINISH	

B600002-002

TeleVideo, Inc.

TITLE: PCB SCHEMATIC CONT. BD 950 G/A Sht 4

SIZE D | SHT 4 OF 7 | DRAWING NO. 2009801 | REV B3

2009801 B3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH4 XTAL 1
SH7 IRQ, AB Ø, AB 1, R/W, AB 9
SH1
SH6 IO.P.SEL, DB Ø, DB 1, DB 2, DB 3, DB 4, DB 5, DB 6, DB 7, ΦØ
SH1
SH4 Φ2
SH7 RESET
SH6 RXD
SH1 AB 11
SH6 DTR
SH7 BI.DIR.ENA
SH1 AB 10

A36 6551 — XTL, IRQ, RSØ, RS1, R/W, CSØ, CS1, DBØ–DB7, Φ2, RESET; RTS, RXD, TXD
A29 6551 — XTL, IRQ, RSØ, RS1, R/W, CSØ, CS1, DBØ–DB7, Φ2, RESET; DTR, RTS, TXD, RXC, DSR, DCO, RXD, CTS
A33 6551 — XTL, IRQ, RSØ, RS1, R/W, CSØ, CS1, DBØ–DB7, Φ2, RESET; DTR, DSR, DCD, RXD, CTS, TXD, RXC
A28 74LS157 — 4A, 3A, 3B, 2B, 2A, 1B, 1A, SEL, STR; 4Y, 3Y, 2Y, 1Y
A9 1489 — A32 1489

+5V; R12–R14, R20 4.7K; R21 4.7K; R7 330; R6 330; R8 330

DCD P3-8; DSR P3-6; RXD P3-3; CTS P3-5; RXD MOD P6-3; RTS P4-4; DTR P4-20; TXD P4-2; BEEP/TXD P0-3, P1-3; BEEPER P6-13; OUT SPEAKER SH 7

E10, E11, E12, E13, E25, E24, E7, E8, E9, E29, E30, E31

Q1 2N2219A

C8, C4, C9, C7, C13, C14, C18, C17 330 PF 100V
C25 330 PF 100V; C19 330PF 100V; C74 .01; C73 .01

A19 74LS32; A19 74LS37; A18 1488; A24 74LS32; A24; A23 1488; A23 1488; A18 1488; A23 1488; A18 1488; A23 1488

C10, C15, C16, C6, C11, C5, C12 330 PF 100V

P7-1
P7-2
P0-4
P0-2
P0-1
P1-1
+12V
GND
P1-2
P9-1
P9-2
RXD P1-4
RXD (MODEM)
RXD (HOST) } SH6

P10-11
P10-9
P10-3,7
P10-5
P10-13
P6-12
TXD SH4
TXD P3-2
TXD MOD P6-2
DCD P4-8
RXD P4-3
DTR P3-20
CTS P4-5
RTS P3-4
DSR P4-6
P10-10
P10-8
P10-6
P10-4
P10-14

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN HHUR 3-12-82
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK
2009501	—		ENGR
		SCALE:	APPD
		MATERIAL	APPD
			FINISH

B600002-002

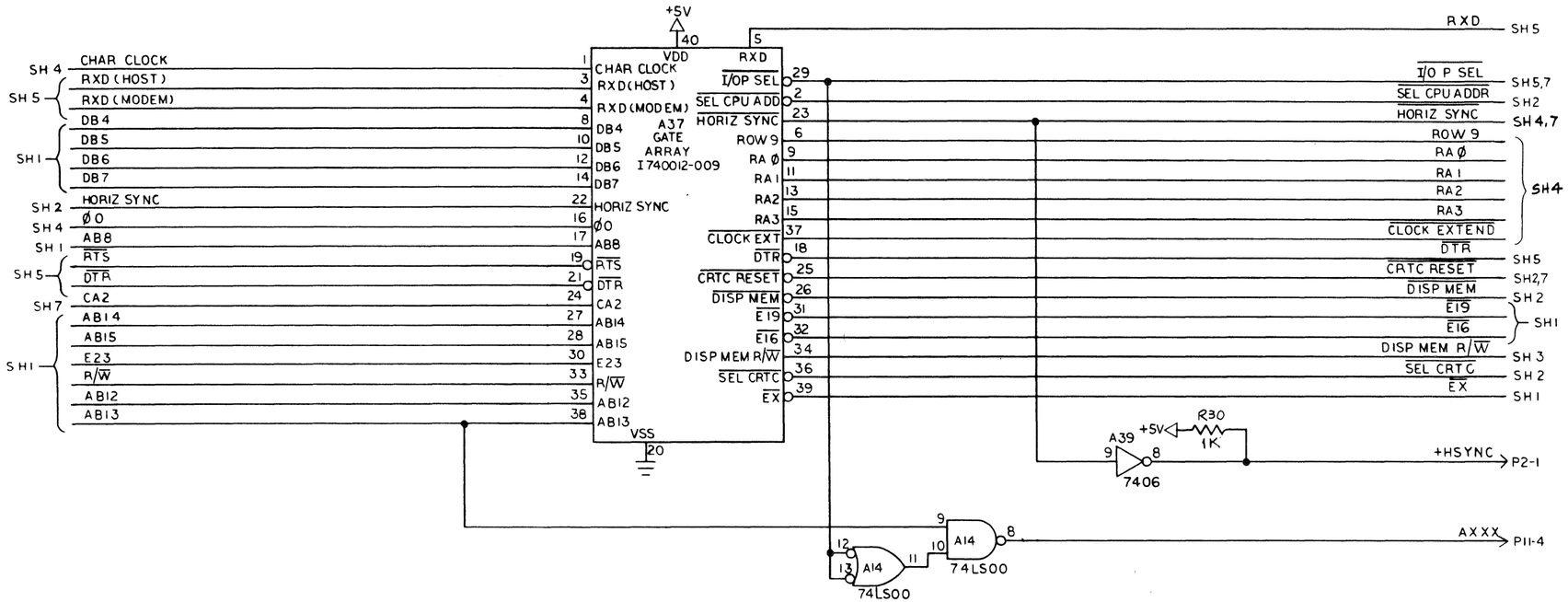
TeleVideo, Inc.

TITLE: PCB SCHEMATIC CONT. BD 950 G/A 5 of 5

SIZE D | SHT 5 OF 7 | DRAWING NO. 2009801 | REV B3

B3 | 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



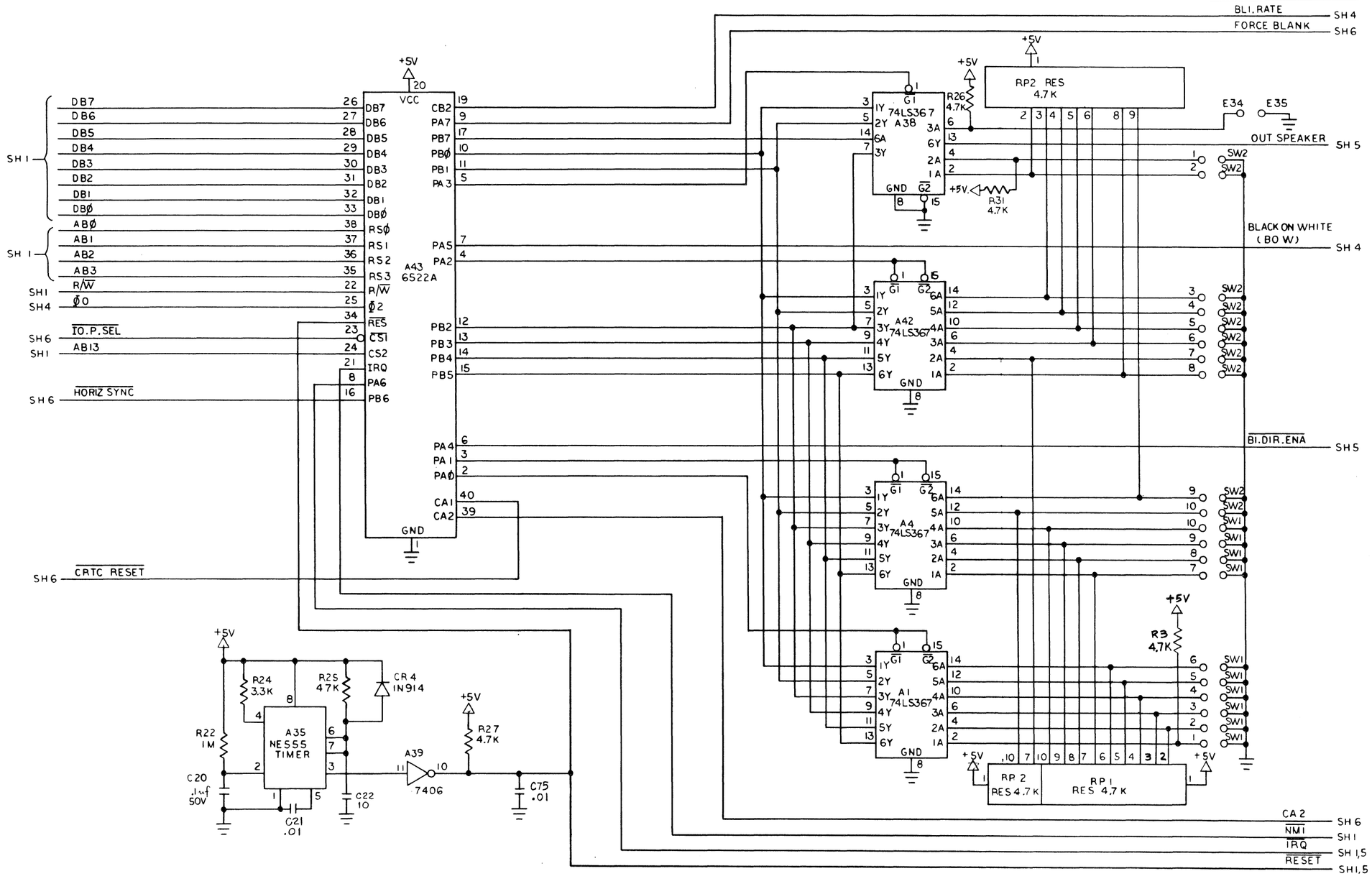
APPLICATION		UNLESS OTHERWISE NOTED	DWN HHUR 3-17-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG 2 PLC 3 PLC	ENGR	TITLE
		± ± ±	APPD	PCB SCHEMATIC
		SCALE:	APPD	CONT. BD 950 G/A
		MATERIAL	APPD	
			FINISH	

B600002-002

SIZE	SHT	OF	DRAWING NO.	REV
D	6	7	2009801	B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

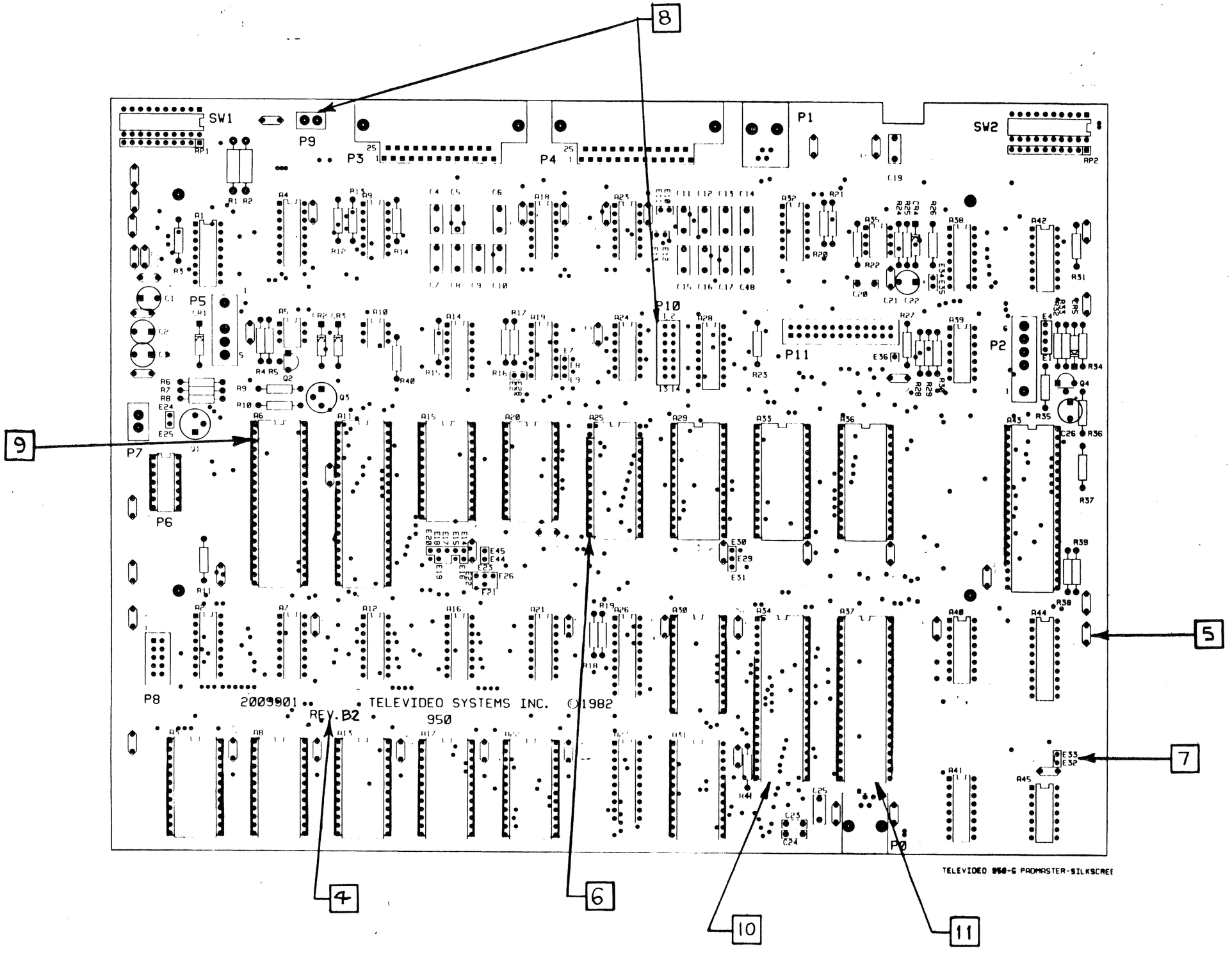


APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H HUR 3-15-82	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK	
2009501	—	SCALE: —	ENGR	TITLE
		MATERIAL —	APPD	PCB SCHEMATIC 5 of 7
		FINISH —	APPD	CONT. BD 950 G/A
			APPD	SIZE D · SHT 7 OF 7 · DRAWING NO. 2009801 · REV B3

B600002-002

B3 2009801

78
9 REQD
81
3 REQ'D
78
4
5 PL.
C36
C35
C15
R75
85
18
3
83
2 REQ'D
80
3 REQ'D
86
73
2 REQ'D


8
9
4
6
10
11
5
7
SW1
SW2
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P0
RP1
RP2
2009901 REV.B2
TELEVIDEO SYSTEMS INC. ©1982
950
TELEVIDEO 950-G PADMASTER-SILKSCREE

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
1	44									C2-5,9-14,16-29,	Cap CER .01uf 16V 20%	2028700
										31-33,37-39,49-		
										54,58,59,64-68,		
										73,74		
2	3									C69,71,72	Cap Elec 22uf 15V	2025700
3	17									C34,40-48,55-57,	Cap CER 330pf 50V 20%	2029100
										60-63		
4	1									C6	Cap Tant 4.7uf 16V 10%	2027500
5	1									C15	Cap Elec 10uf 16V 20%	2027300
6	5									C1,7,8,30,36	Cap Mono .1uf 20%	2186800
7	1									C75	Cap Mica 100pf 50V 5%	2024700
8	1									A60	IC 74LS191	2036600
9	1									A21	IC 74LS174	2044600
10	1									A6	IC 74LS109	2027000
11	6									A5,9,11,13,38,70	IC 74LS00	2024200
12	4									A2,8,12,69	IC 74LS04	2024800
13	1									A10	IC 7406	2034800
14	3									A7,29,30	IC 74LS08	2025200
15	3									A16,58,63	IC 74LS32	2025800
16	2									A31,71	IC 74LS74	2026600
17	1									A1	IC 74LS86	2026800

NOTES:

TITLE	DATE	
PCB ASSY 950 CONTROL BOARD	11-11-82	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
18	1									A62	IC 74LS139	2027200
19	6									A20,43-46,59	IC 74LS157	2027400
20	2									A3,4	IC 74LS163	2027600
21	2									A22,23	IC 74LS166	2027800
22	1									A18	IC 74LS173	2028000
23	3									A19 ,61,64	IC 74LS174	2028200
24	4									A65-68	IC 74LS367	2028600
25	1									A24	IC 74LS374	2029000
26	2									A39,48	IC 75188N	2029200
27	2									A40,57	IC 75189AN	2029400
28	1									A47	IC TIL117	2029800
29	1									A56	IC 4N38	2035000
30	4									A25-28	IC 2114ICB RAM	2035800
31	1									A34-37	IC 6116 RAM 150ns	2049200
32	1									A53	IC 6502A Micro	2049600
33	1									A55	IC 6545 Contr CRT	2049800
34	3									A49-51	IC 6551 1MHz UART	2155700
35	1									A54	IC 6522A	2050200
36	1									A14	IC 74LS245	2036200
37	1									OSC-1	CRY K1114A 23.814MHz OSC	2035200
38	1									A41	IC 2532 EPROM F00D Sys Prg950	8000043

NOTES:

TITLE	DATE	
PCB ASSY 950 CONTROL BOARD	11-11-82	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL										REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B												
39	1										A33	IC ROM Up Char Gen	8000002
40	1										A32	IC ROM Low Char Gen	8000003
41	1										A42	IC 2532E0000 EPROM Sys	8000044
												Prog 950	
42	1										A15	IC 74LS42	2026000
43	1										A17	IC NE555	2030200
44	2										R6,41	Res CF 750 Ohm 1/4W 5%	2031700
45	1										R32	Res CF 51K Ohm 1/4W 5%	2032300
46	2										R2,33	Res CF 68 Ohm 1/4W 5%	2051100
47	7										R21,22,29,31,	Res CF 4700 Ohm 1/4W 5%	2053100
											35-37		
48	1										R4	Res CF 270 Ohm 1/4W 5%	2051300
49	2										R42,43	Res CF 330 Ohm 1/4W 5%	2051500
50	1										R34	Res CF 510 Ohm 1/4W 5%	2051900
51	20										R1,3,5,8,9,10,14	Res CF 1000 Ohm 1/4W 5%	2052100
											15-20,23-25,38,		
											40,44		
52	5										R11,28,39,45,46	Res CF 3300 Ohm 1/4W 5%	2052700
53	1										R26	Res CF 100K 1/4W 5%	2032100
54	1										R12	Res CF 1M Ohm 1/4W 5%	2031500
55	4										RP1-4	Res PK 1K Ohm 8 Pin SIP	2042700

NOTES:

TITLE	DATE	
PCB ASSY 950 CONTROL BOARD	11-11-82	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
56	2									R27,30	Res CF 510 Ohm 1/2W 5%	2045100
57	1									R7	Res CF 22 Ohm 1/4W 5%	2033500
58												
59												
60												
61												
62												
63												
64												
65	2									Q1,4	Tran 2N2219A	2045300
66	1									Q2	Tran 2N3019	2045700
67	1									Q3	Tran 2N2907A	2045900
68												
69												
70	4									D1-4	Diode 1N914	2047500
71	1									D5	Diode 1N4001	2047700
72												
73	2									S1,2	Switch 10 Pos Dip/20P Side	2096800
											Adj	
74												
75												

NOTES:

TITLE	DATE	
PCB ASSY 950 CONTROL BOARD	11-11-82	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
76												
77	1									R13	Res CF 47K Ohm 1/4W 5%	2033700
78	9									XA32-37,41,42,52	Socket 24P IC Dip	2098401
80	3									XA49-51	Socket 28P IC Dip	2098404
81	3									XA53-55	Socket 40P IC Dip	2098402
82												
83	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
84	2									P2,5	Plug 5P Str Waf	2098802
85	1									P1	Conn PCB RJ11 Fem (AMP)	2097900
86	1									P9	Plug 2 P Str Waf	2098800
87	3									Q1,2,4	Insul Pad Tran 3005-A Large	2180800

NOTES:

TITLE		DATE	
	PCB ASSY 950 CONTROL BOARD		11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B2											
1												
2												
3												
4												
5												
6	1									C23	Cap Mica 20pf 50V 10%	2024300
7	1									C26	Cap Tant 4.7uf 16V 10%	2027500
8	1									C20	Cap Cer .1uf 50V 10%	2030100
9	48									C27-55,57-75	Cap Cer .01uf 16V 20%	2028700
10	1									C22	Cap Elect 10uf 16V 20%	2027300
11	17									C4-19,25	Cap Mono 330pf 100V 20%	2029300
12	3									C1,2,3	Cap Elect 22uf 50V 10%	2026100
13	1									C21	Cap Mono .01uf 50V 10%	2028900
14	1									C24	Cap Mica 47pf 50V 5%	2024900
15												
16	4									A1,4,38,42	IC 74LS367	2028600
17	1									A2	IC 74LS42	2026000
18	2									C3,22	IC 6116 RAM 150ns	2049200
19	1									A5	IC 4N38	2035000
20	1									A6	IC 6545 Contr CRT	2049800
21	5									A7,12,16,21,28	IC 74LS157	2027400

NOTES:

TITLE PCB ASSY CONTROL BOARD 950 GATE ARRAY

DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/IND O.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B2											
22	2									A9,32	IC 74189AN	2029400
23	1									A10	IC TIL117	2029800
24	1									A11	IC 6502A Micro	2049600
25	1									A14	IC 74LS00	2024200
26	1									A25	IC 2532 EPROM F000 Sys	8000043
27	2									A18,23	IC 75188N	2029200
28	2									A19,24	IC 74LS32	2025800
29												
30												
31	1									A26	IC 74LS245	2036200
32	1									A27	IC 74LS374	2029000
33	3									A29,33,36	IC 6551 UART 1MHz	2155700
34	1									A34	IC G/A 950(A)	2057600
35	1									A37	IC G/A 950(B)	2057800
36	1									A35	IC NE555	2030200
37	1									A39	IC 7406	2034800
38	1									A43	IC 6522A	2050200
39	1									A45	CRY K1114A 23.814MHz OSC	2035200
40	1									A20	IC 2532 E000 EPROM Sys	8000044
41	1									A31	IC ROM UP Char Gen	8000002
42	1									A30	IC ROM Char Gen Low 950	8000003

NOTES:

ITEM/ FIND NO.	QTY PER ASSM REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B2											
43	5									XA6,11,34,37,43	Socket IC 40P IC DIP	2098402
44	3									XA29,33,36	Socket IC 28P IC DIP	2098404
45	10									XA3,8,13,15,17,	Socket IC 24P IC DIP	2098401
										20,22,25,30,31		
46												
47	1									P6	Socket 14 Pin IC DIP	2098403
48	2									SW1,2	SW 10 Pos DIP/20P Side Adj	2096800
49	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
50												
51												
52												
53	1									P1	Conn PCB RJ11 Fem (AMP)	2097900
54												
55												
56	2									P2,5	Plug 5P Str Waf	2098802
57	1									Q3	Insul Pad Tran 3005-A	2180800
58												
59												
60	1									R41	Res CF 33 1/4W 5%	2034500
61	7									R16,17,28-30,34,	Res CF 1K 1/4W 5%	2052100
										37		

NOTES:

TITLE	DATE	
PCB ASSY CONTROL BOARD 950 GATE ARRAY	11-11-82	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B2											
62	1									R32	Res CF 270 1/4W 5%	2051300
63	1									R33	Res CF 750 1/4W 5%	2031700
64	1									R36	Res CF 22 1/4W 5%	2033500
65	2									R4,35	Res CF 68 1/4W 5%	2051100
66	5									R15,23,24,38,39	Res CF 3.3K 1/4W 5%	2052700
67	13									R3,9,11-14,18-21,	Res CF 4.7K 1/4W 5%	2053100
										26,27,31		
68	1									R22	Res CF 1M OHM 1/4W 5%	2031500
69	1									R40	Res CF 100K 1/4W 5%	2032100
	2									R1,2	Res CF 510 1/2W 5%	2045100
71	1									R10	Res CF 51K 1/4W 5%	2032300
72	3									R6-8	Res CF 330 1/4W 5%	2051500
73	2									RP1,2	Res DIP 4.7K 10P SIP	2041300
74	1									R25	Res CF 47K 1/4W 5%	2033700
75	1									R5	Res CF 510 1/4W 5%	2051900
76	1									CR1	Diode 1N4001	2047700
77	5									CR2-5	Diode 1N914	2047500
78	2									Q1,4	Trans 2N2219A	2045300
79	1									Q3	Trans 2N3019	2045700
80	1									Q2	Trans 2N2907A	2045900

NOTES:

TITLE	DATE	
PCB ASSY CONTROL BOARD 950 GATE ARRAY	11-11-82	TeleVideo Systems, Inc.

MODEL 925

THEORY OF OPERATION

4.1

OVERVIEW

The TeleVideo Model 925 terminal is the third member of a family of terminals based on the 6502A microprocessor. Circuitwise, it is very similar to the Model 910; the main differences being increased program ROM space, serial keyboard interface, and more complex attribute and communications sections. Functionally, the 925 is designed to be halfway between the more sophisticated Model 950 and the conversational 910.

As in the 950 and 910, the microprocessor is totally interrupt driven. This operation provides the most efficient and error free means for asynchronous reception and transmission of data.

4.2

OPERATING CLOCKS

There are three clocks of the 925 control board. Two of these are synchronized; shift clock and character clock, while the third, the receive and transmit clock, is totally independent of the other two. The basic clock on the board is the Video or Dot clock. It's frequency range is 13.608 megaHertz and is produced by a crystal controlled oscillator which is made up of the crystal, Y2, part of chip A16, and several passive feedback components (see Sheet 7 of schematic). This clock is used to shift video data out of a shift register for display on the CRT. It is also used to clock a counter, A24, to create the system clock. The system clock is designated 'Character Clock' on the 925 schematic. It is used for two purposes; character clock input to the CRT control chip (A59, Sheet 2) and as the system clock (00) input to the 6502A microprocessor (A60 Sheet 1).

A 74LS163 presettable 4 bit binary counter A24, Sheet 7) is used to divide the shift clock by eight; providing a frequency of 1.701 megaHertz. The 74LS163, which is normally a divide by 16 counter, is forced to divide by eight by loading a count of eight into the counter when it reaches it's highest count (15).

In this mode, the QC output of the counter is low for 4 clocks and high for 4, making it suitable for use as a symmetrical clock.

The two Asynchronous Communications Interface Adapters (ACIA #1 and ACIA #2, Sheet 5) have internal clock oscillators and require only that the external crystal be added. The circuitry of the 925 allows the two ACIA's to share one crystal, Y1.

Internal to each ACIA, the basic frequency of 1.8432 megaHertz is divieded down by a factor determined by a firmware controlled register. ACIA # 2, which is used for receiving keyboard data, is always set for 1200 baud (bits per second). ACIA # 1 is

shared by the Host Communications port (P3), and the printer port (P4). The baud rate for ACIA # 1 depends on the baud rate switch settings for the two ports.

4.3

ADDRESS DECODING

The 65,536 byte address field of the 6502A microprocessor (MPU) is divided as follows. The two highest address lines (A14 & A15) are decoded by a 1 of 4 decoder (half of A37, Sheet 1) to divide it into four 16,384 (16K) byte sections. The highest 16K bytes ($C000_{16}$ - $FFFF_{16}$)are used for program Read Only Memory (ROM).

The program ROM contains a program which controls the microprocessor, causing it to process data fed to it by the Keyboard or the host computer. The 16K block is divided further into two 8,192 (8K) byte sections. When the MPU is addressing the higher 8K bytes, the chip located at A50 is selected. When the MPU is addressing the lower 8K bytes, the chip located at A49 is selected.

The next lower 16K bytes, 8000-BFFF is used to access I/O devices. This output of A37 is connected to a 1 of 8 decoder (A29, Sheet 1) and the other section of A37 where, using lower order address lines, 12 individual locations are decoded. Each I/O device is treated as if it were an individual byte within the memory map.

The output labeled $\overline{4000\text{-}7FFF}$ from A37 defines the second lowest 16K clock within the address range. This signal is 'OR'ed with 02 low (A54, Sheet 1) to select two 6116, 2K by 8 bit RAM chips. (A47 and A48, Sheet 2).

These chips are used to store data to be displayed on the CRT (Display RAM). A48 contains data for one screen (page 1) and A47 the other (page 2).

The output labeled $\overline{0000\text{-}3FFF}$ is true (low) when the MPU is addressing any location within that range. It is used to select two 2114, 1K X 4 bit RAM chips. These RAMS are used to store variable data that is processed by the MPU during program execution. (System RAM).

4.4

TERMINAL MEMORY

Memory in the 925 terminal consists of ROM and RAM. As stated in Section 4.3, Program (or System) ROM is located within the range C000-FFFF. It is further broken down into two 8K byte

sections, C000-DFFF and E000-FFFF. Each of these sections is represented by a socket capable of accepting a 2K (2048) byte ROM, a 4K (4096) byte ROM or an 8K (8192) byte ROM. This allows expansion of program ROM from 2K bytes to 16K bytes in 2K byte increments. Each socket is selected using the C000-FFFF output of A37 'AND'ed with the high (E000-FFFF) or low (C000-DFFF) condition of address line A13.

The standard configuration of the 925 is 4K bytes located from D000-DFFF and another 4K bytes located from F000-FFFF.

System RAM consists of 1K (1024) bytes of static random access (read/write) memory. (A41 & 42, Sheet 1). The 0000-3FFF output of A37 is used to select these two chips. Since there are no other devices located in this section, further decoding is not required. System RAM is used as a buffer for characters received from and transmitted to the host computer and printer; 'Flags' used by the program for decision making, and for storing the states of various software 'timers'.

4.5

DISPLAY FUNDAMENTALS

The circuitry required to display data on the CRT other than the video circuitry, which is covered in Section 4.7 is made up of three parts; display memory, character generation memory and the CRT controller chip (A59, Sheet 2).

The display memory consists of 4K bytes of high speed static RAM (A47 & A48, Sheet 2). The screen contains 25 rows of 80 characters each for a total of 2000 characters. Therefore, each 6116 RAM (2048 bytes each) is capable of storing an entire screen of characters.

The address lines of the two 6116's are controlled by the outputs of three 2 to 1 multiplexers (A56, A57 & A58, Sheet 2). The sources for the inputs of the multiplexers are the address lines of the MPU (A0-A11) and the memory address outputs of the CRT controller (MA0-MA10). The multiplexers' inputs are switched by the 01 output to the MPU. This operation allows the CRT controller memory address lines to drive the display RAM address lines when 01 is high, while the MPU address lines are enabled during 01 low. The MPU accesses the display RAM to update a location due to keyboard input or transmission from the host (Write), or to READ a location for transmission to the host during a block mode transmit.

Display memory accesses from the MPU occur while 01 is low. Data from the display RAM is gated to and from the main Data Bus (D0-D7 lines of the MPU) by a byte wide bi-direction of 01. This buffer is selected if the MPU is addressing a location in Display RAM. The direction of the data is controlled by the R/W signal from the MPU during 02 high.

During the high portion of 01 (02 low), the CRT controller accesses the location specified by its memory address lines. The display RAM is always selected during 02 low and the R/W line of the display RAM is always high at this time. Because of this, any access of display RAM during 02 low will cause a read of the location being addressed. This data is latched by DC Carry (A39, Sheet 3) and used as address lines A3-A9 of the character generator ROM (A31, Sheet 3). A0, A1, and A2 address lines of the character generator ROM are controlled by the RA0, RA1, and RA2 lines from the CRT controller. These define which line of the 10 line character cell is in effect. The data to be displayed for the character and line being addressed is loaded into a parallel in/serial out shift register (A30, Sheet 2). During the next eight cycles of the shift clock this data is shifted out one bit at a time and combined with other signals to create the video output to the video amplifier in the monitor.

The MPU is capable, using address line A11, of writing to or reading from any of the 4096 bytes of display RAM. The CRT controller can only access a maximum of 2048 bytes (using MA0-MA10). To allow the second page to be displayed (providing that a chip is installed in A47), the program, in response to an ESC K, sets a bit in one of the control latches labeled 'Display Page Two'. This connects to the highest order line on the CRT controller side of the multiplexers. Thus, when 01 is high, this bit will be high and A47 will be accessed by the CRT controller.

4.6

INTERRUPT SIGNALS

As mentioned in Section 4.1, the MPU is interrupt driven in the 925. An interrupt is an input to the MPU which causes it to complete its present instruction, save the contents of its internal registers and go to a predetermined location in the program. The MPU will respond to an interrupt within a maximum of 8 system clock cycles of 4.7 microseconds.

The 6502A MPU has two interrupt inputs, IRQ and NMI. IRQ is a maskable interrupt which can, under program control, be ignored. NMI is non-maskable interrupt that cannot be ignored by the MPU.

The Model 925 uses the NMI for interrupts generted by the Keyboard ACIA (A33, Sheet 5). IRQ has two possible sources; the communications ACIA (A32, Sheet 4) and the vertical sync interrupt. The interrupts generated by the ACIA's indicate that data has been received or that the transmitter section is ready to accept a new character. The vertical sync interrupt is used by the program to increment timing registers used to keep track of the time of day, blink the cursor, time the bell, etc. When an interrupt occurs, the firmware (program ROM) must determine which source caused the interrupt and act accordingly.

4.7

VIDEO GENERATION

Control signals for the CRT monitor are generated by the CRT controller, the attribute logic and the shift register mentioned in Sectin 4.5.

The CRT controller produces vertical sync, horizontal sync, display enable and cursor signals. Horizontal and vertical sync are buffered and sent directly to the monitor. Display enable and cursor are used along with the attributes and serial data from the shift register to produce the video signal for the monitor.

Because of the character address latch (A39, Sheet 2), the character generator ROM, and the shift register, it takes two character clock times for a character addressed by the CRT controller to be displayed on the screen. The display enable and cursor signals simultaneously with the memory address coinciding with the position on the screen. Because of this the cursor and display enable signals must be delayed by two character clock times. This is accomplished by a hex D flip-flop (A22, Sheet 4).

The remaining two stages are used to provide a 1 character time delay for the attribute signal and half intensity signal (an additional delay is provided by the character address latch).

The 925 visual attributes are achieved in the following manner:

The high order bit coming out of the character address latch (Chad 7) is used to indicate a protected (half intensity) character. This is the only attribute which is done on a character by character basis. The remaining four attributes, blinking, blank (hidden characters), reverse video and underline, are produced by special characters written into the display RAM by the firmware in response to a special 3 character sequence. (See operators manual). These special characters are decoded to provide a signal labeled 'Attribute' (see pin 4 of A22, Sheet 3). This signal is used to gate DC Carry to the data input of a 'D' flip-flop (pin 2 of A1, Sheet 3) which is clocked on the rising edge of shift clock while DC Carry is low. As long as the character in the character address latch is an attribute character, the data input will be low when the flip-flop is clocked. This keeps the 'Q' output low, enabling the outputs of one of three quad tri-state latches (A19, Sheet 3). This latch is used to carry the existing attributes through a new attribute character, and its outputs are used only during the time that an attribute character is being displayed. (An attribute character is displayed as a half intensity blank). As soon As a non-attribute character is decoded, the 'Q' output of the D flip-flop (pin 5 of A1) is clocked high, disabling the outputs of A19. At the same time, Q output (pin 6) goes low. This is connected to one of the

output enable inputs of another quad tri-state latch (A20). The other output enable input of A20 is controlled by the Q output of another D flip-flop (pin 8 of A1) that goes low approximately 35 nanoseconds after pin 6 of A1. This operation ensures that the outputs of only one of the latches are active at any given time.

The purpose of the second latch is to contain the most recent attributes on the present scan line. The third quad tri-state latch (A21) is used to remember the last attribute character encountered. Unlike the first two latches, which are reset by horizontal sync (once each scan line) the third latch is reset only once each frame by vertical sync. In this manner, the attributes are allowed to continue from one character row to another. The outputs of this third latch are enabled when both D flip-flops mentioned earlier are reset (Q outputs low). The time during which these outputs are enabled is defined as; from the beginning of a new character row that was preceded by a character row containing an attribute character; until a new attribute character is found, i.e., if the only attribute character is character number 62 on character row 10, the outputs of A21 will be enabled at the start of character row 11 and remain enabled until the end of the frame (vertical sync).

The attribute signals, underline, reverse video, blink and blank, are combined with other signals pertinent to the video output (see upper left side of sheet 4), to create a stream of pulses used by the video amplifier to control the electron beam within the CRT.

4.8

COMMUNICATIONS

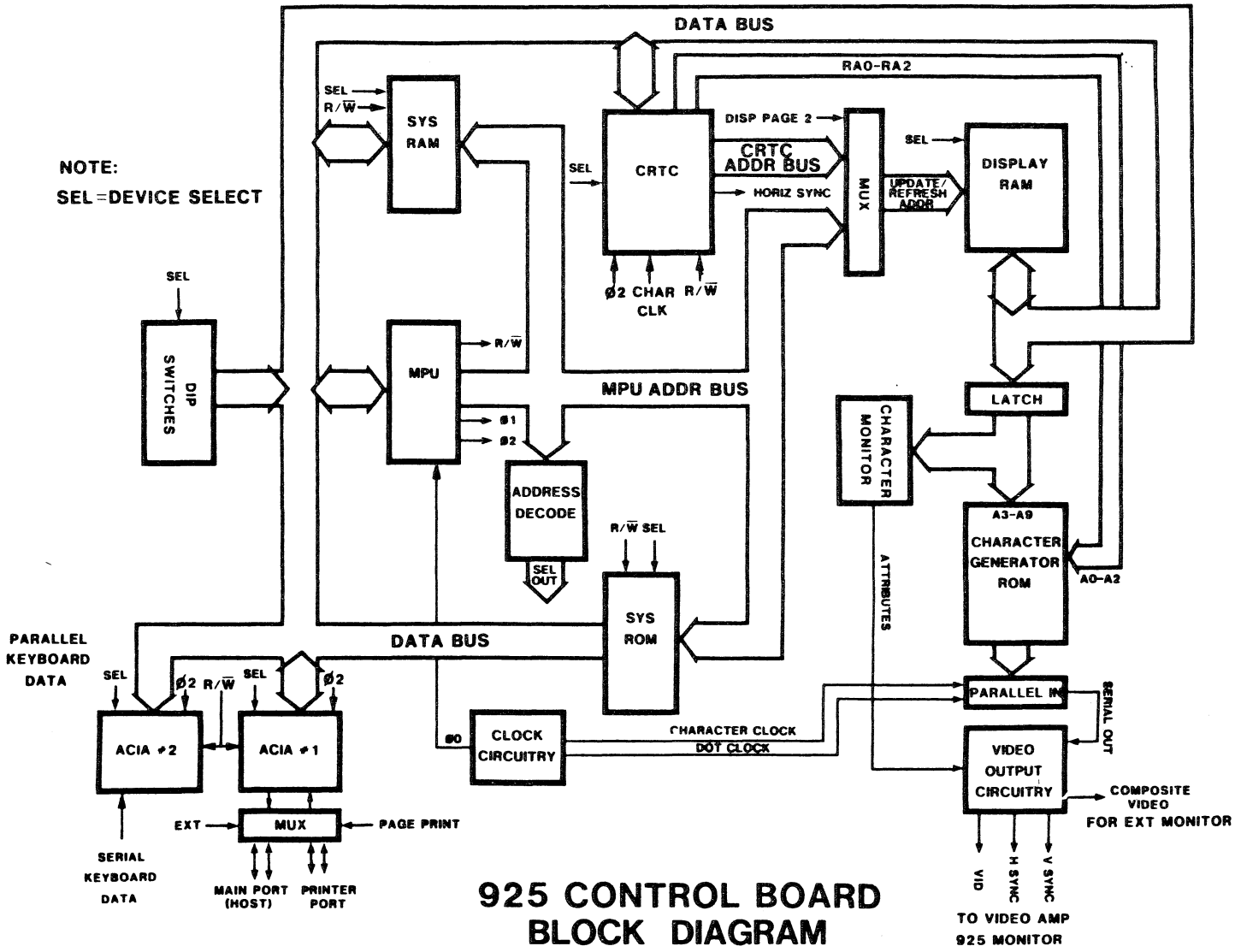
Data from the Keyboard is received via a standard RJ11 connector located on the rear of the board. ACIA # 2 (A33, Sheet 5) is used to convert the serial data into parallel form. When the ACIA receives a character, it interrupts the MPU via the NMI input. The MPU, during the NMI routine, reads the contents of the receive buffer of the ACIA. The keyclick is produced automatically by the hardware, requiring no firmware overhead. The IRQ output of the ACIA also connects to the trigger input of a simple one-shot circuit used to produce a pulse which drives the speaker located in the Keyborad (see lower left section of sheet 5).

The terminal connects to the host computer through P3 (sheet 5) which is a standard 25 pin D type connector located on the rear of the board. In half or full duplex, (conversational) mode, data is sent to the host one character at a time as it is typed on the keyboard. In block mode, data is not sent to the host unless a send command of some sort is entered on the keyboard. These modes of data transmission are completely under control of the firmware.

The 925 also has a separate connector which can be connected to a printer with a serial communications port. The connector for the printer port is P4. Data sent to the printer can come from two selectable sources; the host computer or the terminal screen (display RAM). To enable data from the Host to the printer, the control latch output labeled 'EXTENSION' is used. This gates data received on P3 pin 3 to P4 pin 3 via or gate A26 (pins 4,5,6). It also allows two possible control lines, DTR (P4-20) and Handshake (P4-11) to go to the host.

Another control latch output labeled '$\overline{\text{BI-DIR}}$' allows data from the printer (P4-2) to be sent to the host (P3-2). Data from the printer is not received by the 925 terminal.

During transmission from the host to the printer, the screen may (normal) or may not (transparent) be updated. Another mode of printer operation is page print. In this mode, text is entered on the screen (either page or display RAM) and, when the desired text is entered and properly edited, the data can be sent to the printer by depressing the 'PRINT' key. The data on the screen will be sent to the printer from the 'HOME' position to the cursor position. During page print, the data is not sent to the host. This is done by disabling the data to the host through another gate (A26 pin 8,9,10).



925 CONTROL BOARD BLOCK DIAGRAM

Figure 4-1

			D7	D6	D5	D4	D3	D2	D1	DØ	
Read Only	ROM # 1	FFFF F000	PROGRAM DATA								SYS ROM
	Unused ROM # 1	EFFF E000									
	ROM # 2	DFFF D000	PROGRAM DATA								
	Unused ROM # 2	CFFF C000									
	Unused I/O	BFFF 9004									I/O
Write	Control Latch # 2	9003	Display Mode	BOW/ WOB	Bell	Timeout Blank	Keyclick On/Off	DTR	Monitor Mode	Spare	
Read	Dipswitch Port # 2	9002	SP/MK	O/E	Par.	BOW/ WOB	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	Printer
Read	Dipswitch Port # 1	9001	Stop Bits	Edit	Word Length	925/ 920	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	Main
Write	Control Latch # 1	9000	CPU Reset	Exten.	Bi-Direc.	925/ 920ATT	60/ 50Hz	Cursor Under	Blink Clock	Page Print	
——	Spare	8070									
Read/Wr	Control Register	8063	Stop Bits	Word Lnth 1	Word Lnth 0	Rcvr Clk Source	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	ACIA #2 (Keybd)
Read/Wr	Command Register	8062	Par.2	Par.1	Par.0	Norm/ Echo	Xmit 1	Xmit 0	RCV IRQ	DTR	
Read/Wr	Status Register	8061	Read: Status Register				Write: Program Reset(No Data)				
Read/Wr	Transmit or Receive Data	8060	Read: Receive Register				Write: Transmitter Register				
Read	Dipswitch Port # 5	8050	Not Used		Cursor 1	Cursor 0	DTR	SRTS	Not Used		
Write	Reset IRQ	8040	NO DATA								
Read/Wr	Control Register	8033	Stop Bits	Word Lnth 1	Word Lnth 0	Rcvr Clk Source	Baud Rate 3	Baud Rate 2	Baud Rate 1	Baud Rate 0	ACIA #1 (Host)
Read/Wr	Command Register	8032	Par.2	Par.1	Par.0	Norm/ Echo	Xmit 1	Xmit 0	Rcv IRQ	DTR	
Read/Wr	Status Register	8031	Read: Status Register				Write: Program Reset(No Data)				
Read/Wr	Transmit or Receive Reg.	8030	Read: Receive Register				Write: Transmit Register				
Read/Wr	Read or Write Regs 0-31	8021			DISPLAY PARAMETERS						CTRC
Write	Address Register (Contains Reg. Number)	8020			REGISTER NUMBER						
Read	Dipswitch Port # 4	8010	Char Set 1	Char Set 0	Not Used		Keyclick On/Off	Test	Not Used		
Read	Dipswitch Port # 3	8000	Not Used		Line/Pg Att.	Timeout Blank	60/ 50Hz	CR/ CR-LF	Comm Mode 1	Comm Mode 0	
	Unused Display RAM	7FFF 4C00									Disp RAM
	Page 2	4BFF 4800									
	Page 1	47FF 4000									
	Unused Sys. RAM	3FFF 0400									Sys. RAM
		03FF 0000			VARIABLE PROGRAM DATA						

925 MEMORY MAP

Table 4-1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPRO'D
	A	PROD REL PER ECO 42		
	B	" " ECO 43		
	C	" " ECO 44		
	D	" " ECO 46		

NOTES: UNLESS OTHERWISE SPECIFIED

1. VERSION -001 AND -002
2. VERSION -002 ONLY
3. CIRCUITRY OPTIONAL

P-BUS
P22
P21
P20
SH 2

+5V

C6 20 PF
X1 5.7143 M
C8 20PF
XTAL1
XTAL2
U6
-001 (8048)
-002 (8035)
R3 1K
EA
CR1 IN4001
C7 1 uf
RESET
U8 7414
P7-1 Tx
C10 330PF
RP3-6 10K
P7-2 Rx
INT
P7-4 +12V
V1 78L05
C12 1 uf
C11 .01 uf
Vcc
Vdd
Vss
P7-3
P6-2
LS 1
P6-1
WR
10

PSEN
P20
P21
P22
P23
P24
P25
P26
P27
P10
P11
P12
P13
P14
P15
P16
RD
ALE
D0
D1
D2
D3
D4
D5
D6
D7

RP3, 10K
U7 74LS05

RP3 10K
R4 10K
RP2 10K

CHAR INSERT
CHAR DELETE
LINE INSERT
LINE DELETE
BACK SPACE
TAB
BACK TAB
LINE FEED
PAGE ERASE
SEND
HOME
RETURN
CLEAR SPACE
ENTER
SET-UP LOC ESL
PRINT
BREAK

1 CTRL
39 SHIFT
32 FUNCT
33 ALPHA LOCK
R2, 10K
RP2, 10K
C2 .01 uf
U2 74LS367
U3 74LS367
C3 .01 uf

SH 2

B600003-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN G. Gallo 10-1-85
NEXT ASSY	USED ON		CHK J.Cox 10-2-85
		ANG ± PLC ± PLC	ENGR [illegible]
			APPD
		SCALE	APPD
		MATERIAL	FINISH

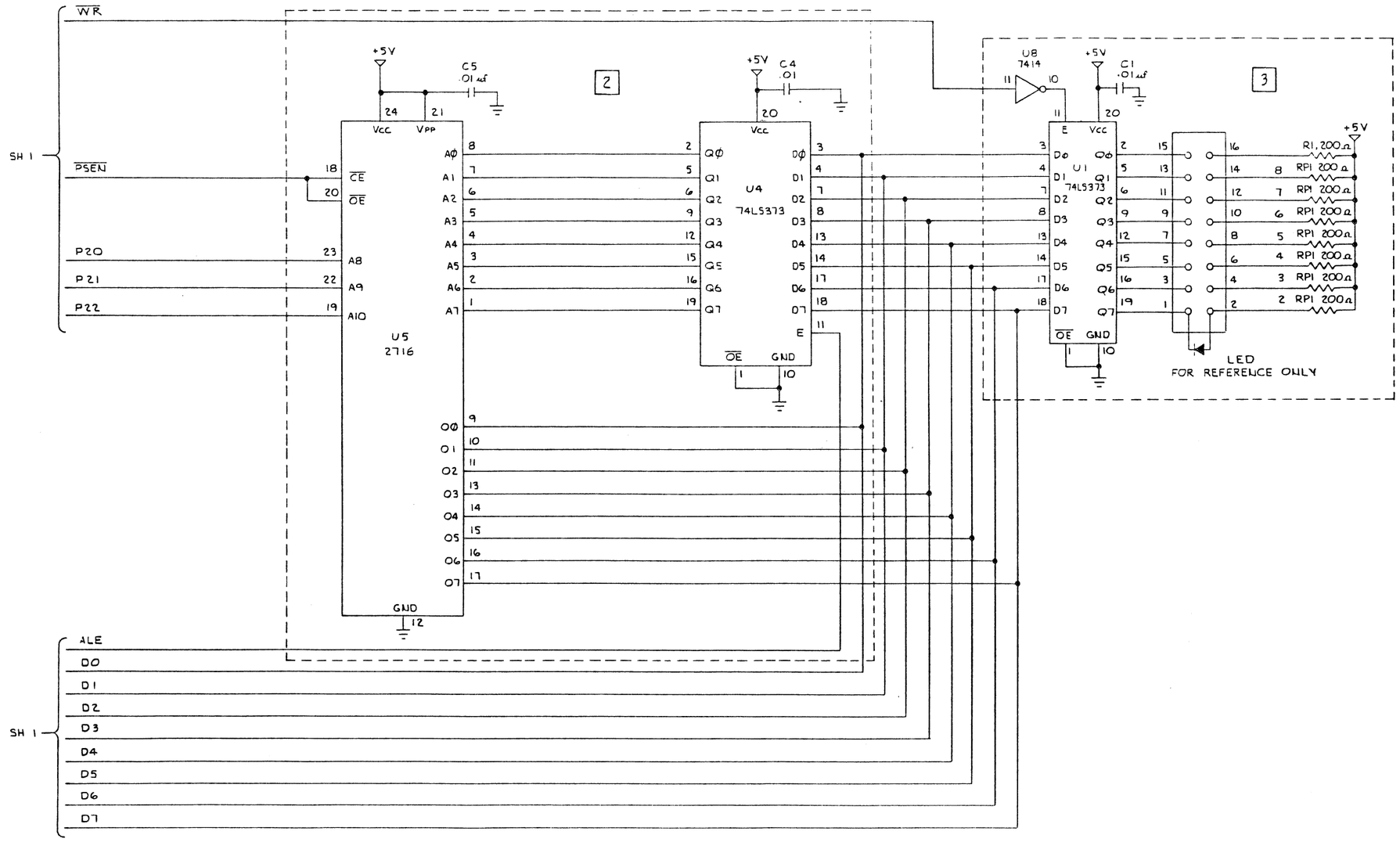
TeleVideo, Inc. 536A

TITLE PCB SCHEMATICS 950 KEYBOARD

SIZE D | SHT 1 OF 2 | DRAWING NO 2010300 | REV E

2010300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED	DWN Carol Ann 10-2-80	TeleVideo, Inc. 950
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK Carol Ann 10-2-80	TITLE PCB SCHEMATIC 950 KEYBOARD
		ANG 2 PLC 3 PLC	ENGR [illegible] 10-2-80	
		± ± ±	APPD [illegible]	
		SCALE N.O.T.S.	APPD	
		MATERIAL	FINISH	SIZE D SHT 2 OF 2 DRAW NO 2010300 REV E

2003-00

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD RELEASE		
	B	PROD REL PER ECO 150		
	B1	PROD REL PER ECO 151		
	B2	PROD REL PER ECO 212		
	B3	PROD REL PER ECO 277		
	B4	PROD REL PER ECO 305		
	B5	" " ECO 0426	5/2/82	

A60 6502A

A54 74LS08

A46 555

A16 74S04

A50 2333

A42 2114

A41 2114

A49 2333

A29 74LS138

8X0X	DIPSW PORT #3	SH6
8X1X	DIPSW PORT #4	SH6
8X2X	SEL CRTC	SH2
8X3X	SEL ACIA #1	SH5
8X4X	RESET IRQ	SH4
8X5X	DIPSW PORT #5	SH6
8X6X	KYBD ACIA	SH5
8X7X	SPARE	

P5-5	+12V	+12V
P5-1	-12V	-5V
P5-4	+5V	+5V
P5-3	GND	GND

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Sunny 1.7.81
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK
		ANG ± 2 PLC ± 3 PLC	ENGR
			APPD
		SCALE: NONE	APPD
		MATERIAL	APPD
			FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATICS 30 925 CONTROL BD.

SIZE D | SHT 1 OF 7 | DRAWING NO. 2015800 | REV B5

B5 2015800

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1810

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 1,6: D0 D1 D2 D3 D4 D5 D6 D7

SH 1: A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A12

SH 7 SHIFT CLOCK
SH 7 DC CARRY
SH 4 DISP RAM WR
SH 4 DISP RAM
SH 4 Ø2·W
SH 4 DISP RAM SEL
SH 1 Ø1
SH 7 DISP PGZ

SH 7 60HZ/50HZ (N/U) 2
SH 7 CHAR CLK 21
SH 1 R/W 22
SH 1 Ø2 23
SH 1 SELCRTC 8X2X 25

A59 6545A-1

RS 24
D0 33 D1 32 D2 31 D3 30 D4 29 D5 28 D6 27 D7 26
PROG SEL
CCLK
R/W
Ø2(E)
CS

DISP EN 18
CURSOR 19
HORIZ SYNC 39
VERT SYNC 40

MA0 4 MA1 5 MA2 6 MA3 7 MA4 8 MA5 9 MA6 10 MA7 11 MA8 12 MA9 13 MA10 14

RA0 38 RA1 37 RA2 36 RA3 35
RA0 RA1 RA2 RA3

RES

RP3 4.7K +5V

GND

SH 6 BIT 0
SH 6 BIT 1

A57 74LS157 A58 74LS157 A56 74LS157

74LS32 A38 A55 74LS00 A39 74LS04

A40 74LS245

A47 6116 A48 6116

74LS374 A39

A12 74LS32 A27 74LS04

A31 2332

RP3-0 4.7K

A30 74LS166

HORIZ SYNC B → P2-1
HORIZ SYNC → SH 3,4
DISP EN → SH 3
CURSOR → SH 3
HORIZ SYNC → SH 3
VERT SYNC → SH 3,4
CHAD 0
CHAD 1
CHAD 2
CHAD 3
CHAD 4
CHAD 5
CHAD 6
CHAD 7
} SH 3

DOT SERIAL → SH 4

A11 74LS32 A11 74LS32 A11 74LS32

RA0 → SH 4

A13 74LS08

ROW 10 → SH 3,4,7

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Swaney 9-11-81	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK 10/29/81	
		ANG 2 PLC 3 PLC	ENGR 10/29/81	TITLE PCB SCHEMATICS 3/ 925 CONTROL BD.
			APPD	
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 2 OF 9 DRAWING NO 2015800 REV 85

B5 2015830

BISHOP GRAPHICS, INC./PRESS
PEGBOARD NO. A1-1435

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 7 SHIFT CLOCK
SH 7 DC CARRY
SH 6 LINE/PAGE ATTS
SH 2 HORIZ SYNC
SH 2 HORIZ SYNC
SH 2 VERT SYNC
SH 2 CHAD 3
SH 2 CHAD 2
SH 2 CHAD 4
SH 2 CHAD 5
SH 2 CHAD 6
SH 7 MONITOR MODE
SH 7 DC CARRY
SH 2 DISP EN
SH 2 CURSOR
SH 7 CURSOR=BLOCK
SH 2 CHAD 7
SH 2 ROW 10
SH 2 CHAD 1
SH 2 CHAD0
SH 7 925/920 ATTS

A23 74LS32
A12 74LS32
A35 74LS04
A12 74LS32
A4 74LS02
A2 74LS10
A35 74LS04
ROW 10
A38 74LS32
A54 74LS08
A10 74LS08
A10 74LS08
A3 74LS00
A13 74LS08
A13 74LS08
A10 74LS08
A10 74LS08
A11 74LS32
A12 74LS32
A19 74LS32
A18 74LS08
A18 74LS08
A4 74LS02
A28 74LS32
A18 74LS08
A18 74LS08

RP2 4.7K
RP2 4.7K
+5V

A1 74LS74
A1 74LS74
A21 74LS173
A20 74LS173
A19 74LS173
A22 74LS174

Contains last ATT. encountered

Contains most recent ATT. on existing line

Contains Current ATTb. When being displayed

BLINK SH4
DEL DISP EN SH4
DEL CURSOR SH4
HALF INTENSITY SH4
REV VIDEO SH4
UNDERLINE SH4
BLANK SH4

BLANK
BLINK
925/920 ATTS

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Sunny 10-22-81	TeleVideo, Inc. 532
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK 10-29-81	TITLE PCB SCHEMATIC 925 CONTROL BD.
		SCALE: NONE	ENGR 10-29-81	APPD
		MATERIAL	FINISH	APPD
				APPD

SIZE D | SHT 3 OF 7 | DRAWING NO. 2015800 | REV B5

BISHOP GRAPHICS/ACCURPRESS RETAINER NO. A 1387G

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 3 BLINK
SH 7 BLINK CLK
SH 2 RAØ
SH 3 BLANK
SH 2 DOT SERIAL
SH 2 ROW 1Ø
SH 3 UNDERLINE
SH 7 TIMEOUT BLANK
SH 3 DEL CURSOR
SH 3 REV VIDEO
SH 7 BOW / WOB
SH 3 DEL DISP EN
SH 3 HALF INTENSITY
SH 2 HORIZ SYNC
SH 2 VERT SYNC
SH 1 RESET IRQ (8x4x)
SH 1 A13
SH 1 A14
SH 1 A15
SH 1 AØ
SH 1 A1
SH 1 A12
SH 1 Ø2
SH 1 R/W
SH 1 Ø1
SH 7 SET DISP RAM
SH 1 SYS RESET
SH 7 CHAR CLK

74LS00 A3, A2 74LS10, A16 74S04, A55 74LS00, A3 74LS00, A15 74LS86, A15 74LS86, A5 7406, A5 7406, A5 7406, A27 74LS04, A5 7406, A5 7406, A15 74LS86, A5 7406, A16 74S04, A15 74LS86, A5 7406, A35 74LS04, A55 74LS00, A37 74LS139, A54 74LS08, A55 74LS00, A35 74LS04, A4 74LS02, A36 74LS32, A6 74LS74, A36 74LS32, A36 74LS32, A23 74LS32

RP3 4.7K, +5V, A6 74LS74, RP3 4.7K, +5V, A6 74LS74

E3 E4, E1, E2, R7 750, R8 270, R9 1K, R5 1K, R4 1K, R2 22, +5V, C3 4.7µf, CR1 IN914, Q1 2N2219, R3 68

VIDEO SHIELDGND → P2-3
VIDEO → P2-4
COMP V+TTL VIDEO → P2-6
VERT SYNC → P2-5

VERT SYNC/IRQ SH 1
E000-FFFF SH 1
C000-DFFF SH 1
9xxØ
9xx1 DIPSWITCH PORT #1 SH 6
9xx2 DIPSWITCH PORT #2 SH 6
9xx3
8000-BFFF SH 1
0000-3FFF SH 1
DISP RAM SEL SH 2
CONTROL LATCH #1 SH 7
CONTROL LATCH #2 SH 7
Ø2·W SH 1,2
DISP RAM WR SH 2
DISP RAM SH 2

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG 2 PLC 3 PLC	DWN Sweeney 10-22-81 CHK ENGR APPD APPD APPD
NEXT ASSY	USED ON	SCALE: NONE MATERIAL	FINISH

TeleVideo, Inc. 533

TITLE: PCB SCHEMATIC 925 CONTROL BD.

SIZE D | SHT 4 OF 7 | DRAWING NO. 2015800 | REV B5

B5 2015800

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

P4-4 RTS E5
P4-11 HSHAKE E6 E7
P3-18 TEST E8 E9
P3-6 DSR 12 S3 9
P4-20 DTR E10 E11

+5V
RP2 4.7K
A17 75189
C20 C22 C23 C21 330pf (4)

SH7 EXTENSION

+5V
RP2 4.7K
A9 75189
P3-8 DCD 13 S3 8
P3-5 CTS
P3-3 RxD
P6-3 RxD
P4-2 SERIAL DATA FROM PRINTER
C11 C13 C12 C10 330pf

SH7 DTR
SH7 BI-DIRECTIONAL
SH7 PAGE PRINT

SH1 SEL ACIA (8x3x)
SH1 R/W
SH1 Ø2
SH1 AØ
SH1 A1
SH1 DØ D1 D2 D3 D4 D5 D6 D7
1,2,6

+5V
A32 ACIA #1 6551A-1
DSR CSØ VCC
DCD CTS RXD CS1 R/W Ø2 RSØ RS1 DØ D1 D2 D3 D4 D5 D6 D7 RST GND
TxD RTS IRQ RxC XTAL1 XTAL2
R28 10K
RP3 4.7K
Y1 OPTIONAL
C31 10pf
R18 3.3K
C32 10pf
Y1 1.8432 MHZ

+5V
A33 ACIA #2 6551A-1
CSØ VCC R/W Ø2 RSØ RS1 DØ D1 D2 D3 D4 D5 D6 D7 CS1 R×D
XTAL1 XTAL2 IRQ RxC TxD CTS DCD DSR RST GND
Y3 OPTIONAL
RP3 4.7K

SH1 KYBD ACIA (8X6X)
P0-3
P1-3
C8 330 pf
A13 74LS08
SH1 SYS RESET

A28 A26 A27 A14 74LS32 74LS04

A25 75188
A34 75188

HSHAKE SH6
TEST SH6
DTR SH6

HSHAKE P3-11
DSR P4-6
DCD P4-8
CTS P4-5
C62 C66 C63 C65 330 pf

DTR EN S3 P3-20
E15 E16 E14
TxD P3-2
TXD MODEM P6-2
SERIAL DATA TO PRINTER P4-3
RTS P3-4
C67 C69 C64 C68 330 pf

IRQ (ACIA) SH1
RxC P6-12

NMI SH1,7

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Sunny 10-18-81	TeleVideo, Inc. 534
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± 2 PLC 3 PLC	ENGR	TITLE
			APPD	PCB SCHEMATIC
		SCALE NONE	APPD	925 CONTROL BD
		MATERIAL	APPD	
			FINISH	SIZE D SHT 5 OF 7 DRAWING NO. 2015800 REV B5

E5 2015800

BISHOP GRAPHICS ACCURIPAD RELEASE NO. A1-1810

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH1 DIPSWITCH PORT #5
SH1 DIPSWITCH PORT#4
SH1 DIPSWITCH PORT#3
SH4 DIPSWITCH PORT #2
SH4 DIPSWITCH PORT#1

RP5 4.7K
+5V
R23 4.7K

S1
BD RT 3
BD RT 2
BD RT 1
BD RTØ
WD LENGTH
STOP BITS

EDIT
920/925
BD RT3
BD RT2
BD RT1
BD RTØ
PAR 2
PAR 1
PAR Ø
BOW/WOB
COMM MODE Ø
COMM MODE 1
50/60 HZ
CR/CR-LF

S2

R1 4.7K +5V

RP1 4.7K

RP4 4.7K

S3
TIMEOUT BLANK ENABLE
LINE/PAGE ATTRIBUTES
KEY CLICK
CHAR SET 1
CHAR SET Ø
CURSOR 1
CURSOR Ø

SH5 DTR
SH5 TEST
SH5 HSHAKE

A53 74LS244
A52 74LS244
A51 74LS244
A43 74LS244

DØ D1 D2 D3 D4 D5 D6 D7 SH 2,5,7

LINE/PAGE ATTRIBUTES SH3
BIT 1 SH2
BITØ SH2

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Sunny 10.20.81
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK 10/20/81
		ANG ± PLC ± 3 PLC ±	ENGR 10/20/81
		SCALE: NONE	APPD
		MATERIAL	FINISH

TeleVideo, Inc.

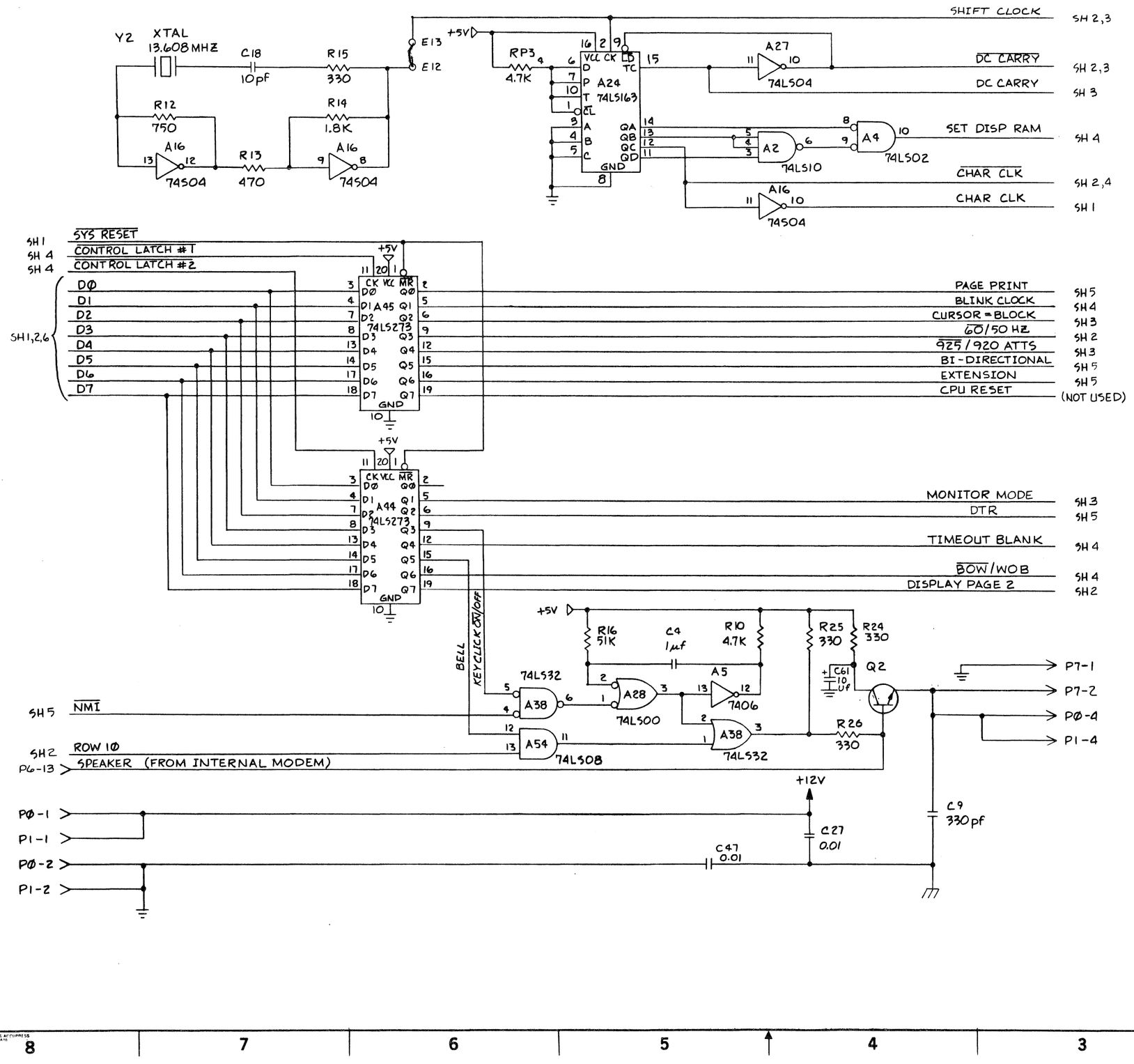
TITLE: PCB SCHEMATIC 925 CONTROL BD.

SIZE D | SHT 6 OF 7 | DRAWING NO. 2015800 | REV B5

B5 2015800

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1187D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		



NOTE:

P6 IS A 14- OR 16-PIN DIP SOCKET FOR OPTIONAL BOARD CONNECTION.

* PINS 0 & 15 ARE PINS 1 & 16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

B600014-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN Swany 10-21-81	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	TITLE
		ANG 2 PLC 3 PLC	ENGR	PCB SCHEMATIC 925 CONTROL BD
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 7 OF 7 DRAWING NO. 2015800 REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 235	3/3/82	
	A1	" " ECO 0370,0410,0426		
	A2	" " ECO 437		
	A3	" " ECO 0530		

A11 6502A

A8 74LS08

A6 555

A31 7406

A14 2333

A13 74LS138

A9 2114

A10 2114

A15 2333

RP3 4.7K

P5-5 +12V
P5-1 -12V
P5-4 +5V
P5-3 GND

NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS ±5 % AND ARE 1/4 WATT.
2. ALL CAPACTOR ARE VALUED IN MICOFARADS ±10% AND ARE 50 VDC.
3. DRAWINGS COMFORMS WITH TELEVIDEO SPEC. NO S000000-001.
4. P6 IS A 14-OR 16-PIN DIP SOCKET FOR OPTIONAL BOARD CONNECTION
5. PINS Ø&15 ARE PINS 1&16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H. Hue 1-12-82	TeleVideo, Inc. 531
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC ± ± . .	CHK 2/3/82	TITLE PCB SCHEMATIC CONT BD 925 R/A
		SCALE None	ENGR 3/3/82	
		MATERIAL	APPD 3/4/82	
		FINISH	APPD	
			APPD	SIZE D SHT 1 OF 6 DRAWING NO 201580! REV A

A3 201580!

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

SH6 MONITOR MODE
SH1 D0 D1 D2 D3 D4 D5 D6 D7
SH1 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
SH6 SHIFT CLOCK
SH6 DC CARRY
SH3 DISP RAM WR
SH3 DISP RAM
SH3 Ø2 W
SH1 Ø1
SH1 A12
SH6 DISP FG2

SH6 CHAR CLK
SH6 R/W
SH1 Ø2
SH1 SEL CRTC 8X2X

+5V
A28 6545A-1
R21 4.7K
RES
RS D0 D1 D2 D3 D4 D5 D6 D7 N/C CCLK R/W Ø2(E) CS
DISP EN
CURSOR
HORIZ SYNC
VERT SYNC
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10
RA0 RA1 RA2 RA3
GND

A22 74LS157
A21 74LS157
A20 74LS157
S VCC 1A 1B 2A 2B 3A 3B 4A 4B 1Y 2Y 3Y 4Y G GND

A19 74LS245
DIR G VCC A1 A2 A3 A4 A5 A6 A7 A8 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 GND

A32 6116
A33 6116
CS VCC R/W A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 D0 D1 D2 D3 D4 D5 D6 D7 OE GND

A18 74LS374
VCC CLK D0 D1 D2 D3 D4 D5 D6 D7 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 OE GND

A17 2332
A8 A9 A10 A11 A0 A1 A2 GND CS2

A12 74LS166
PE MR VCC CP DS CE GND QH D0 D1 D2 D3 D4 D5 D6 D7

RP3 4.7K

74LS32 A42 → A36 74LS04 → ATTRIBUTE SH3
A37 74LS08 → HORIZ SYNC B → P2-1
74LS04 A36 → A30 74LS32 → A30 74LS32
DISP EN SH3
CURSOR SH3
HORIZ SYNC SH3
VERT SYNC SH3
CHAD0 CHAD1 CHAD2 CHAD3 CHAD7 SH3
13 DOT SERIAL SH3
PAGE 2 SEL SH3
RA0 RA1 RA2 RA3 SH3

SH3 PAGE1
SH3 PAGE2
SH5 BIT0
SH5 BIT1

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED		DWN H. Hsu 1-13-82	TeleVideo, Inc. 538
NEXT ASSY	USED ON	DIMENSIONS ARE IN		CHK	TITLE PCB SCHEMATIC CONT BD 925 G/A
		ANG ± 2 PLC ± 3 PLC ±		ENGR	
		SCALE: NONE		APPD	SIZE D SHT 2 OF 6 DRAWING NO. 2015801 REV A3
		MATERIAL X	FINISH X	APPD	

2015801 A3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

SH2 HORIZ SYNC
SH1 SYS REST
SH2 CURSOR
DISP EN
VERT SYNC
SH1 R/W
Ø1
Ø2
SH6 BLINK CLOCK
BOW/WOB
CURSOR=BLOCK
SH2 CHAD 7
RA 3
RA Ø
RA 1
RA 2
CHAD 3
CHAD 2
CHAD 1
CHAD Ø
SH2 DOTS SERIAL
SH6 925/920 ATTS
SH2 PAGE 2 SEL
DC CARRY
SH6 SHIFT CLOCK
SET DISP RAM
SH2 ATTRIBUTE
SH5 LINE/PAGE ATTRIBUTES

+5V
15
1
37 H SYNC
SYS. RST 19
CURSOR IN 6
DISP. EN. 4
VERT. SYNC 29
R/W 34
Ø1 31
Ø2 32
4000-7FFF
BLINK CLK 10
BOW/WOB 9
CURSOR=BLOCK 16
CHAD7 14
RA3 22
RAØ 21
RA1 24
RA2 25
CHAD3 2
CHAD2 3
CHAD1 39
CHADØ 38
VDD
VSS 35
PG.ONE 26
PG.TWO 30
DISP.RAM 36
Ø2·W 23
ROW10 20
VIDEO 7
HALF INT. 8
COMP.VID 5
970/925 17
T/P ATT. 18
DOT SER 11
925 SER 40
PG 2 28
DCCLK 13
SH SET 27
DR ATT. 33
A39 GATE ARRAY 70200-11A
+5V
R4 4.7K

HORIZ SYNC → P11-22
PAGE ONE
PAGE TWO
DISP RAM
Ø2·W
SH 2
SH1,2
ROW 10 SH6 → P11-17
VIDEO
VIDEO
HALF INTENSITY
COMPOSITE VIDEO
SH6
HALF INTENSITY → P11-26

SHIFT CLOCK → P11-21
VERT SYNC → P11-23

74LS04
A36 3 4
A35 5 6 74LS00
E000-FFFF SH1
A42 5 6 74LS32
C000-FFFF 4
C000-DFFF SH1
9XX0
9XX1 DIPSWITCH PORT #1 SH5
9XX2 DIPSWITCH PORT #2 SH5
9XX3
8000-BFFF SH1
0000-3FFF SH1
A43 4 5 6 74LS32 CONTROL LATCH #1 SH6
A43 9 10 8 74LS32 CONTROL LATCH #2 SH6
A43 2 1 3 74LS32
A43 12 13 11 74LS32 DISP RAM WR SH 2

A13
SH1 A14
A15
AØ
A1
A12

+5V
16 Vcc
A38 74LS139
2 1A
3 1B
14 2A
13 2B
15 2G
1 1G
2YØ 12
2Y1 11
2Y2 10
2Y3 9
1Y3 7
1Y2 6
1Y1 5
1YØ 4
GND 8

A35 12 13 11 74LS00
A36 1 2 74LS04

SH6 CHAR CLK
A40 5 6 74S04 VERT SYNC → P2-5
+5V RP3 4.7K 10
A7 74LS74 10 S 12 D 11 CK R 13 Q 9 Q̄ 8
VERT SYNC/IRQ SH 1
SH1 RESET IRQ (8X4X)

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN				DWN H.Hur 1-14-81	TeleVideo, Inc. S39
NEXT ASSY	USED ON	ANG	2 PLC	3 PLC		CHK	TITLE PCB SCHEMATIC CONT BD 925 G/A
		±	±	±	° ±	ENGR	
		SCALE: NONE				APPD	
		MATERIAL				FINISH	SIZE D SHT 3 OF 5 DRAWING NO 2015801 REV A3

A3 2015801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

P4-4 RTS E5
P4-11 HSHAKE E6 E7
P3-18 TEST E8 E9
P3-6 DSR S3
P4-20 DTR E10 E11
+5V
RP3 4.7K
A1 75189
C9 330PF 100V
C7 330PF 100V
C6 330PF 100V
C8 330PF 100V
SH6 EXTENSION
P3-8 DCD S3
P3-5 CTS
P3-3 RXD
P6-3 RXD
P4-2 SERIAL DATA FROM PRINTER
A2 75189
C2 330PF 100V
C3 330PF 100V
C5 330PF 100V
C4 330PF 100V
SH6 DTR
SH6 BI-DIRECTIONAL
SH6 PAGE PRINT
PIO-11
PIO-9
SEL ACIA (8X3X)
R/W
Ø2
AØ
A1
DØ
D1
D2
D3
D4
D5
D6
D7
SH1
A4 ACIA#1 6551A-1
A5 ACIA#2 6551A-1
KYBD ACIA (8X6X)
PØ-3
P1-3
C1 330pf 100V
A8 74LS08
SYS RESET
RP4 4.7K
A31 7406
A35 74LS32
A40 74S04
A24 74LS32
A30 74LS32
A36 74LS04
E29
E30
E31
E32
HSHAKE SH5
TEST SH5
DTR SH5
A16 75188
C14 330PF 100V
C13 330PF 100V
C11 330PF 100V
C12 330PF 100V
HSHAKE → P3-11
DSR → P4-6
DCD → P4-8
CTS → P4-5
E15 E16 E14
DTREN
S3
P3-20
C10 330PF 100V
C17 330PF 100V
C15 330PF 100V
C16 330PF 100V
A23
TXD → P3-2
TXD MODEM → P6-2
SERIAL DATA TO PRINTER → P4-3
RTS → P3-4
P10-5
P10-7/10
IRQ (ACIA) SH1
RXC → P6-12
RXC → P10-13
R13 4.7K +5V
Y1 OPTIONAL
Y3 OPTIONAL
R17 10K
C23 10pf
R16 1K
C22 10pf
Y1 1.8432 MHZ
R15 4.7K
NMI SH1,6

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H. Hu 1-21-82	TeleVideo, Inc. 540
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	TITLE
		ANG ± 2 PLC ± 3 PLC ±	ENGR	PCB SCHEMATIC CONT BD 925 G/A
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 4 OF 6 DRAWING NO 2015801 REV A3

A3 2015801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

SH1 DIPSWITCH PORT #5
SH1 DIPSWITCH PORT #4
SH1 DIPSWITCH PORT #3
SH3 DIPSWITCH PORT #2
SH3 DIPSWITCH PORT #1

+5V — R3 4.7K — RP1 4.7K

S1
BD RT 3
BD RT 2
BD RT 1
BD RT Ø
WD LENGTH
STOP BITS

EDIT 920/925
BD RT3
BD RT2
BD RT1
BD RTØ

S2
PAR 2
PAR 1
PARØ
BOW / WOB
COMM MODE Ø
COMM MODE 1
50/60 HZ
CR/CR-LF

RP2 4.7K — RP4 4.7K — +5V

RP3 4.7K

S3
TIMEOUT BLANK ENABLE
LINE/PAGE ATTRIBUTES
KEY CLICK
CHAR SET1
CHAR SETØ
CURSOR 1
CURSOR Ø

SH4 { DTR, TEST, HSHAKE }

A3 74LS244 — A41 74LS244 — A34 74LS244 — A29 74LS244

DØ D1 D2 D3 D4 D5 D6 D7 — SH1

LINE/PAGE ATTRIBUTES — SH3
BIT 1 — SH2
BIT Ø — SH2

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H. Hur 1-22-82
NEXT ASSY	USED ON		CHK
		ANG ± 2 PLC ± 3 PLC ±	ENGR
			APPD
		SCALE: NONE	APPD
		MATERIAL X	APPD FINISH X

TeleVideo, Inc. 541

TITLE: PCB SCHEMATIC CONT BD 925 G/A

SIZE D | SHT 5 OF 6 | DRAWING NO 2015801 | REV A3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHEET 1		

Y2 XTAL 13.608 MHZ
C31 10 pf 50V
R27 330
R25 750
R26 1.8K
R28 470
A40 74S04
E13
E12
+5V
R11 1K
A25 74LS163
SHIFT CLOCK SH2,3
A36 74LS04
A40 74S04
A37 74LS08
DC CARRY SH 2,3
SET DISP RAM SH 3
CHAR CLK SH2,3
CHAR CLK SH 1
SH1 SYS RESET
SH3 CONTROL LATCH #1
SH3 CONTROL LATCH #2
SH1 D0 D1 D2 D3 D4 D5 D6 D7
A27 74LS273
PAGE PRINT SH4
BLINK CLOCK SH 3
CURSOR=BLOCK SH 3
SPARE
525/920 ATTS SH 3
BI-DIRECTIONAL SH4
EXTENSION SH4
CPU RESET
(NOT USED)
A26 74LS273
MONITOR MODE SH 2
DTR SH4
BOW/WOB SH 3
DISPLY PAGE 2 SH 2
C33 1uf 16V
TIMEOUT BLANK
R2 51K
C18A 1uf 16V
R10 4.7K
R24 330
R22 330
Q2 2N4401
C30 10uf 16V
R23 330
74LS32 A42
A35 74LS00
A31 7406
A37 74LS08
P7-1
P7-2
P0-4
P1-4
SH4 NMI
SH3 ROW 10
P6-13 SPEAKER (FROM INTERNAL MODEM)
P0-1
P1-1
P0-2
P1-2
+12V
.01uf 16V
C19 330 pf 100V
SH 3 VIDEO
E3 E4
R6 750
R1 22
C18 4.7uf 16V
R7 1K
CR1 IN914
R5 270
R8 10K
R9 33
Q1 2N4401
VIDEO SHIELD GND P2-3
VIDEO P2-4
E1
E2
SH3 HALF INTENSITY
SH3 COMPOSITE VIDEO
R16 1K
COMP V+TTL VIDEO P2-6

+12V → P6-1, P6-14
-12V → P6-5, P6-10
+5V → P6-6, P6-9, P6-7, P6-8

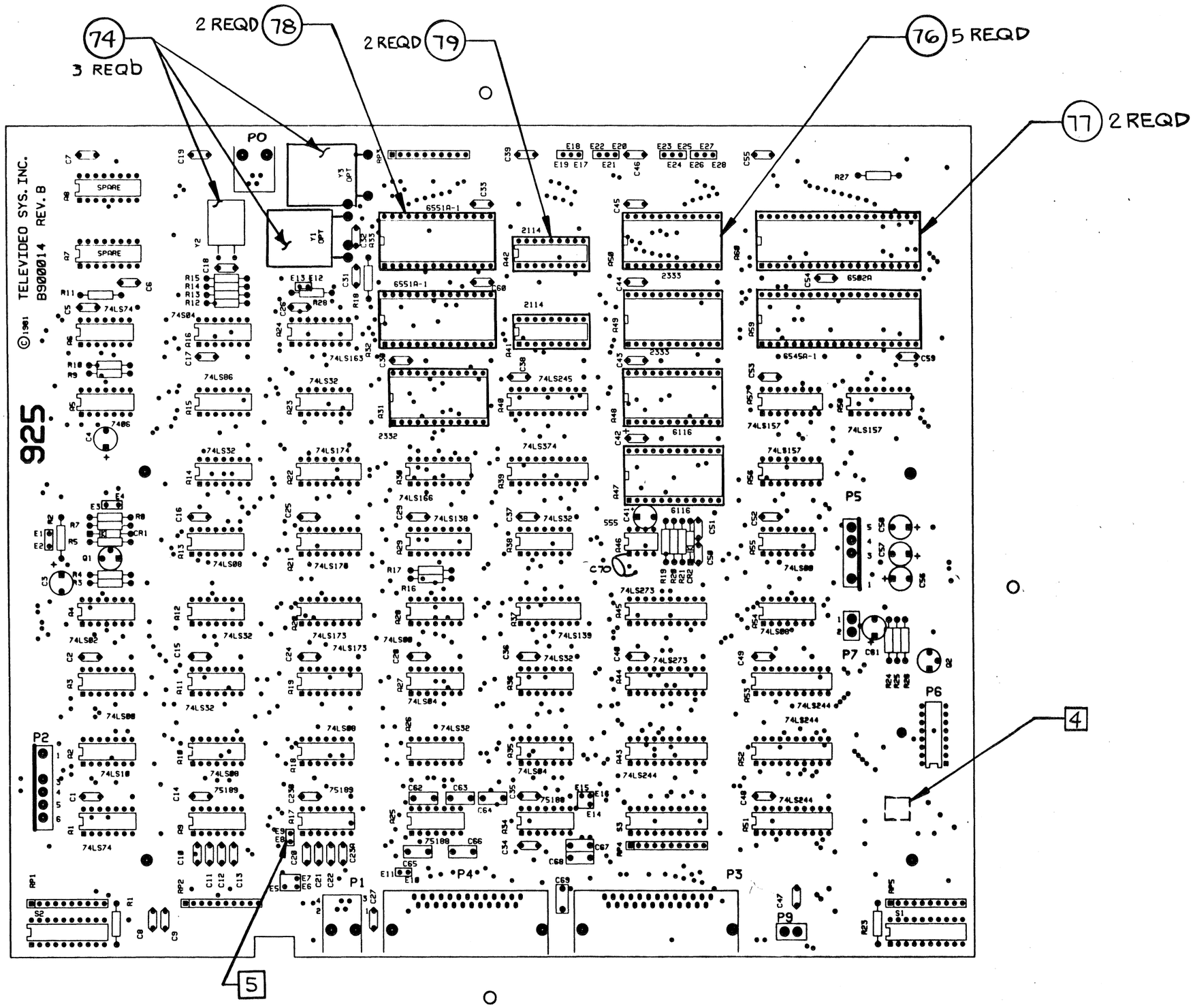
P3-12 RXD+ → P6-15 (SEE NOTE 5)
P3-24 RXD- → P6-0 (SEE NOTE 5)
P6-11 TXD+ → P3-25
P6-4 TXD- → P3-13
CURRENT LOOP COMM (OPTIONAL)

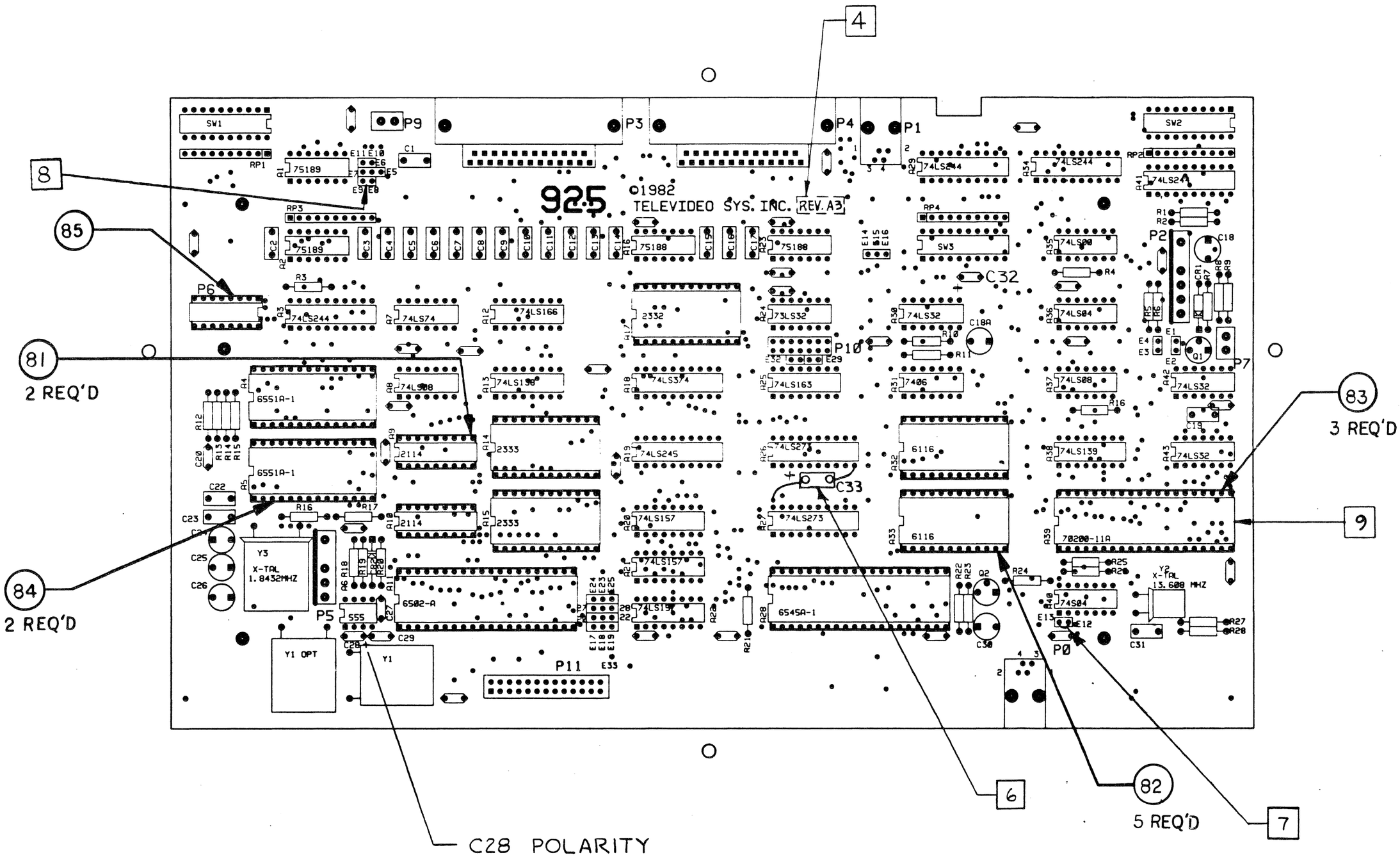
P9-1, P9-2, P3-1, P4-1 → CHASSIS GND

P3-7, P4-7 → LOGIC GND

B600014-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H.Hur 1-25-82	TeleVideo, Inc. 542
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± 2 PLC ± 3 PLC ±	ENGR	TITLE PCB SCHEMATIC CONT BD 925 G/A
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 6 OF 6 DRAWING NO 2015801 REV A3


74
3 REQb
2 REQD 78
2 REQD 79
76 5 REQD
77 2 REQD
925
©1981 TELEVIDEO SYS. INC.
B900014 REV. B
P0
P1
P2
P3
P4
P5
P6
P7
P9
SPARE
SPARE
74LS74
74S04
74LS86
74LS32
74LS163
74LS245
74LS374
74LS174
74LS166
74LS138
74LS32
74LS00
74LS02
74LS32
74LS173
74LS175
74LS00
74LS32
74LS00
74LS32
74LS10
74LS08
75189
74LS74
74LS00
74LS32
74LS04
74LS139
74LS32
74LS273
74LS273
74LS00
74LS244
74LS244
74LS244
74LS157
74LS157
74LS157
74LS00
6551A-1
6551A-1
6551A-1
2114
2114
2114
2333
2333
6502A
6545A-1
6116
6116
6116
2332
7406
555
Y1 OPT
Y3 OPT
Y2
Q1
Q2
CR1
RP1
RP2
RP3
RP4
RP5
S1
S2
S3
5
4


925
©1982
TELEVIDEO SYS. INC. REV. A3
SW1
SW2
SW3
RP1
RP2
RP3
RP4
P1
P2
P3
P4
P5
P6
P7
P9
P10
P11
P0
C1
C32
C33
75189
75188
74LS244
74LS74
74LS166
2332
74LS32
74LS00
74LS04
74LS08
74LS139
74LS32
74LS374
74LS163
74LS245
74LS157
74LS273
74LS279
74LS51
7406
6116
6551A-1
2114
2333
6502-A
6545A-1
70200-11A
555
Y3
X-TAL
1.8432MHZ
Y2
X-TAL
13.600 MHZ
Y1 OPT
Y1
Q1
Q2
C28 POLARITY
8
85
81
2 REQ'D
84
2 REQ'D
4
83
3 REQ'D
9
6
82
5 REQ'D
7

544

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
1												
2	1									A46	IC NE555	2030200
3	2									A41,42	IC 2114ICB RAM	2035800
4	1									A31	IC ROM Char Gen 910	8000016
5												
6												
7	1									A47	IC 6116 RAM 150ns	2049200
8	1									A60	IC 6502A Micro	2049600
9	1									A59	IC CR Contr SY6545A/A	2052800
10	2									A32,33	IC SY6551A/-1 UART 2MHz	2053000
11	3									A3,28,55	IC 74LS00	2024200
12	1									A4	IC 74LS02	2041600
13	1									A16	IC 74S04	2024600
14	2									A27,35	IC 74LS04	2024800
15	1									A5	IC 7406	2034800
16	4									A10,13,18,54	IC 74LS08	2025200
17	1									A2	IC 74LS10	2025400
18	7									A11,12,14,23,26,	IC 74LS32	2025800
										36,38		
19	2									A1,6	IC 74LS74	2026600
20	1									A15	IC 74LS86	2026800

NOTES:

TITLE: PCB ASSY 925 CONTROL BOARD

DATE: 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
21	1									A29	IC 74LS138	2041000
22	1									A37	IC 74LS139	2027200
23	3									A56-58	IC 74LS157	2027400
24	1									A24	IC 74LS163	2027600
25	1									A30	IC 74LS166	2027800
26	3									A19-21	IC 74LS173	2028000
27	1									A22	IC 74LS174	2028200
28	4									A43,51-53	IC 74LS244	2044200
29	1									A40	IC 74LS245	2036200
30	2									A44,45	IC 74LS273	2037600
31	1									A39	IC 74LS374	2029000
32	2									A25,34	IC 75188N	2029200
33	2									A9,17	IC 75189AN	2029400
34												
35												
36	1									R19	Res CF 1M Ohm 1/4W 5%	2031500
37	1									R2	Res CF 22 Ohm 1/4W 5%	2033500
38	1									R3	Res CF 68 Ohm 1/4W 5%	2051100
39	1									R8	Res CF 270 Ohm 1/4W 5%	2051300
40	4									R15,24-26	Res CF 330 Ohm 1/4W 5%	2051500
41	1									R13	Res CF 470 Ohm 1/4W 5%	2051700

NOTES:

TITLE PCB ASSY 925 CONTROL BOARD

DATE 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
42	2									R7,12	Res CF 750 Ohm 1/4W 5%	2031700
43	3									R4,5,9	Res CF 1000 Ohm 1/4W 5%	2052100
44	1									R14	Res CF 1800 Ohm 1/4W 5%	2052300
45												
46	6									R1,10,11,17,23,	Res CF 4700 Ohm 1/4W 5%	2053100
										27		
47	1									R21	Res CF 47K Ohm 1/4W 5%	2033700
48	1									R16	Res CF 51K Ohm 1/4W 5%	2032300
49												
50												
51	5									RP1-5	Res Pk 4.7K Ohm 10P SIP	2041300
52												
53												
54	35									C2,5,7,14-17,19,	Cap Cer .01uf 16V 20%	2028700
										23B,24-26,28-30,		
										33-40,43-46,48,		
										49,52-55,60		
55	5									C6,27,47,50,51	Cap Mono .01uf 50V 10%	2028900
56	1									C4	Cap Elec 1uf 16V 10%	2027900
57	2									C1,3	Cap Tant 4.7uf 16V 10%	2027500
58	2									C41,61	Cap Elec 10uf 16V 20%	2027300

NOTES:

TITLE	DATE	
PCB ASSY 925 CONTROL BOARD	1-14-83	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
59	3									C56-58	Cap Elec 22uf 15V	2025700
60	1									C18	Cap Mica 10pf	2024100
61	19									C8-13,20-23,62-	Cap Cer 330pf 50V 20%	2029100
										70		
62	1									C42	Cap Tant 10uf 25V 10%	2027100
63												
64	2									CR1,2	Diode IN914	2047500
65	1									R20	Res CF 3300 Ohm 1/4W 5%	2052700
66												
67												
68	2									Q1,2	Tran 2N4401 NPN/Silicon	2045500
69												
70												
71	2									Y1,5	Cry 1.8432 MHz	2098602
72	1									Y2	Cry 13.6080 MHz	2098605
73												
74												
75	3									S1-3	Switch 10P DIP/20P Side Adj	2096800
76	5									A31-47-50	Socket 24P IC DIP	2098401
77	2									A59,60	Socket 40P IC DIP	2098402
78	2									A32,33	Socket 28P IC DIP	2098404

NOTES:

TITLE PCB ASSY 925 CONTROL BOARD

DATE 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
79	2									A41,42	Socket 18P IC DIP	2098400
80												
81	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
82	1									P1	Conn PCB RJ11 Fem (AMP)	2097900
83	2									P2,5	Plug 5P STR Waf	2098802
84	1									A50	IC 2732 EPROM Sys Pro 925	8000031
85	1									A49	IC 2732 EPROM Sys Prog 925	8000033

NOTES:

TITLE

PCB ASSY 925 CONTROL BOARD

DATE

1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
1												
2												
3												
4												
5												
6												
7	1									A11	IC 6502A Micro	2049600
8	1									A28	IC CR Contr SY6545A/A	2052800
9	2									A4,5	IC SY6551A/-1 UART 2MHz	2053000
10	1									A39	IC Gate Array 910/925	2057400
11	1									A14	IC 2732 EPROM Sys Pro 925	8000031
12	1									A15	IC 2732 EPROM Sys Pro 925	8000033
13	1									A32	IC 6116 RAM 150ns	2049200
14	1									A17	IC ROM Char Gen 910	8000016
15	2									A9,10	IC 2114ICB RAM	2035800
16	1									A35	IC 74LS00	2024200
17	1									A40	IC 74S04	2024600
18	1									A36	IC 74LS04	2024800
19	2									A8,37	IC 74LS08	2025200
20	4									A24,30,42,43	IC 74LS32	2025800
21	1									A7	IC 74LS74	2026600

NOTES:

TITLE		DATE	
	PCB ASSY 925 GATE ARRAY CONTROL BOARD		1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
22	1									A38	IC 74LS139	2027200
23	3									A20-22	IC 74LS157	2027400
24	1									A12	IC 74LS166	2027800
25	1									A18	IC 74LS374	2029000
26	2									A16,23	IC 75188N	2029200
27	2									A1,2	IC 75189AN	2029400
28	1									A6	IC NE555	2030200
29	1									A31	IC 7406	2034800
30	1									A19	IC 74LS245	2036200
31	2									A26,27	IC 74LS273	2037600
32	1									A13	IC 74LS138	2041000
33	4									A3,29,34,41	IC 74LS244	2044200
34	1									A25	IC 74LS163	2027600
35												
36												
37												
38	1									R9	Res CF 33 Ohm 1/4W 5%	2034500
39	1									R5	Res CF 270 Ohm 1/4W 5%	2051300
40	4									R22-24,27	Res CF 330 Ohm 1/4W 5%	2051500
41	1									R28	Res CF 470 Ohm 1/4W 5%	2051700
42	3									R7,11,16	Res CF 1000 Ohm 1/4W 5%	2052100

NOTES:

TITLE

PCB ASSY 925 GATE ARRAY CONTROL BOARD

DATE

1-14-83

TeleVideo Systems, Inc.

ITEM/IND O.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
43	1									R26	Res CF 1800 Ohm 1/4W 5%	2052300
44	1									R18	Res CF 3300 Ohm 1/4W 5%	2052700
45	8									R3,4,10,12-15,21	Res CF 4700 Ohm 1/4W 5%	2053100
46	1									R20	Res CF 1M Ohm 1/4W 5%	2031500
47	2									R6,25	Res CF 750 Ohm 1/4W 5%	2031700
48	1									R2	Res CF 51K Ohm 1/4W 5%	2032300
49	1									R1	Res CF 22 Ohm 1/4W 5%	2033500
50	1									R19	Res CF 47K Ohm 1/4W 5%	2033700
51												
52												
53	1									R8	Res CF 10K Ohm 1/4W 5%	2034100
54	4									RP1-4	Res Pk 4.7K Ohm 10P SIP	2041300
55												
56												
57	1									C32	Cap Tant 10uf 25V 10%	2027100
58	1									C31	Cap Mica 10pf	2024100
59	3									C24-26	Cap Elec 22uf 15V	2025700
60	2									C28,30	Cap Elec 10uf 16V 20%	2027300
61	1									C18	Cap Tant 4.7uf 16V 10%	2027500
62	2									C18A,33	Cap Elec 1uf 16V 10%	2027900
63	27									Unmarked	Cap Cer .01uf 16V 20%	2028700

NOTES:

TITLE	DATE	
PCB ASSY 925 GATE ARRAY CONTROL BOARD	1-14-83	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
64	1									C27	Cap Mono .01uf 50V 10%	2028900
65	19									C1-17,19	Cap Mono 330pf 100V 20%	2029300
66	1									C29	Cap Cer .1uf 50V 10%	2030100
67												
68												
69	2									CR1,2	Diode IN914	2047500
70	2									Q1,2	Tran 2N4401 NPN/Silicon	2045500
71	2									Y1,3	Cry 1.8432 MHz	2098602
72	1									Y2	Cry 13.6080 MHz	2098605
73												
74												
75												
76												
77												
78	3									SW1-3	Switch 10P DIP/20P Side Adj	2096800
79												
80												
81	2									XA9,10	Socket 18P IC DIP	2098400
82	5									XA14,15,17,32,33	Socket 24P IC DIP	2098401
83	3									XA11,28,39	Socket 40P IC DIP	2098402
84	2									XA4,5	Socket 28P IC DIP	2098404

NOTES:

TITLE	DATE	
PCB ASSY 925 GATE ARRAY CONTROL BOARD	1-14-83	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
85	1									XP6	Socket 16P IC DIP	2098405
86												
87												
88	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
89	1									P1	Conn PCB RJ11 Fem (AMP)	2097900
90	2									P2,5	Plug 5P STR Waf	2098802
91	1									P9	Plug 2P STR Waf	2098800

NOTES:

TITLE: PCB ASSY 925 GATE ARRAY CONTROL BOARD

DATE: 1-14-83

TeleVideo Systems, Inc.

CONTROL BOARD
THEORY OF OPERATION

TeleVideo Systems, Inc.
1170 Morse Ave., Sunnyvale, CA 94086
(408) 745-7760 TWX 910-338-7633 "TVI VIDEO"

THEORY OF OPERATION

TABLE OF CONTENTS

LIST OF FIGURES

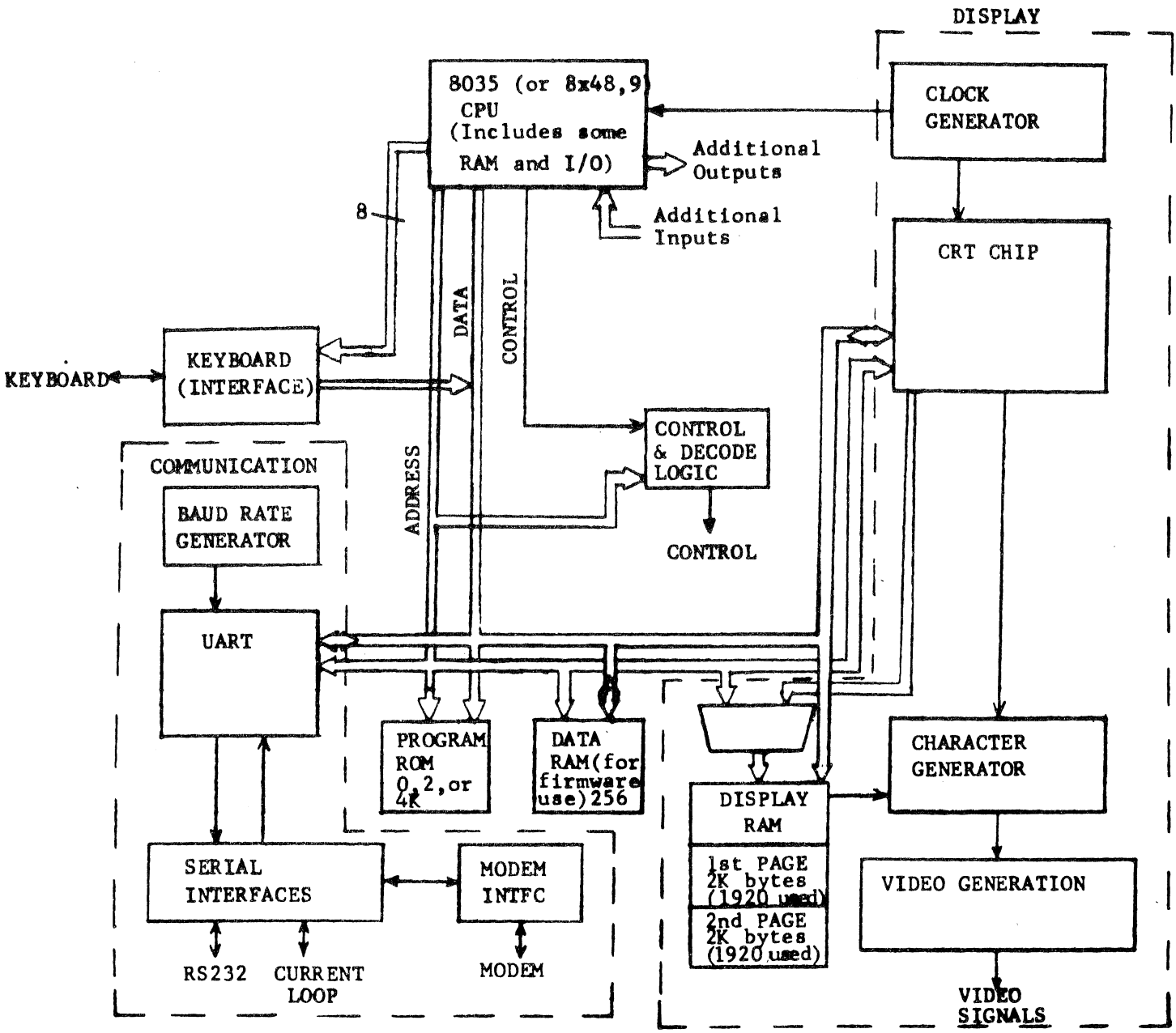
LIST OF TABLES

APPENDIXES

1. ARCHITECTURE OVERVIEW

The terminal's circuitry is composed of the major functional blocks as shown in Figure 1.1.

FIGURE 1.1: SYSTEM BLOCK DIAGRAM



The CPU has control over all functional sections of the terminal via a data/address bus and additional control lines. The Display and Communication sections have some circuitry that runs independently of the CPU. The Display section refreshes the video continuously, automatically. The Communication section can send and receive words at the serial level without CPU intervention.

The CPU is the Intel 8035. (See Appendix A, 8035 Specification) The bussed expansion capability of the CPU is used in order to provide external program memory, data read/write memory, display memory, and memory-mapped I/O.

Depending on firmware requirements 2K or 4K bytes of external program ROM can be accommodated. (Instead of the 8035, it is possible to use an 8048 or 8049 CPU, thus 1K bytes or 2K bytes, respectively, of external program ROM memory can be omitted.)

In addition to the internal data memory of the CPU, there is a 256 x 8 Data RAM (two 2111's) external to the CPU that is usable as read/write storage by the firmware.

The characters being displayed on the screen are accessed by the CPU via two 2K-byte blocks of read/write memory (RAM). This memory is on the same external data/address bus as the 256 x 8 Data RAM and is accessed in a similar manner. In addition to the normal read/write control lines, the Display RAM requires that the address multiplexing logic be properly controlled by the CPU for transfers to/from the display RAM.

The I/O signal lines on the CPU chip that are not used for the expansion

data/address bus, are used for various control and status functions. Additional I/O data, control, and status ports are gained by use of the expansion bus. Part of the data expansion addresses are used to implement these Input and Output capabilities. (This is known as memory-mapped I/O.) Thus, these I/O ports are treated by firmware in a manner similar to the RAM accesses, but are used for I/O transfers.

Via the I/O (direct and memory-mapped) the CPU interfaces to:

(1) the CRT chip and other display circuitry

(2) the UART and other communication circuitry

and (3) the keyboard.

The display I/O gives the CPU control over the CRT chip (including initializing the CRT chip, reading/writing the cursor position, and scrolling) and some video display circuitry (including a FORCE BLANK control).

Once initialized the CRT chip and other display circuitry can automatically perform the continuous refreshing required of the CRT by generating the video, horizontal sync, and vertical sync signals required by the CRT.

The communication I/O gives the CPU control over the UART chip (including initializing the UART's mode and sending/receiving characters on the word level) and some other communication circuitry (including printer port control, BREAK control, and control over the RS232 'ready' and 'clear' types of signals.

Once initialized the UART chip and other communication circuitry automatically perform the parallel-to-serial, serial-to-parallel, and signal level conversions required for the serial interfaces.

The Keyboard I/O allows the CPU and its firmware to scan the switch matrix that is connected to the keyboard connector.

A clock generator provides the CRT chip with the exact clock frequency required. Additionally, frequencies are tapped off for use by the CPU and the communication baud rate generator.

Accessable switches and jumpers allow the user to select many options and configurations.

Operation of the above system capabilities is described in more detail in the following sections. Page references are to the schematics of this terminal controller module.

2. OPERATION OF THE CPU INTERFACES

The CPU is the center of control in this terminal (system). This section describes the CPU, the expansion bus, and the interfaces used to control the other parts of the system. Sections 2.1 through 2.4 provides most of the information required by the firmware programmer in order to control the system.

2.1 CPU

The CPU (Central Processing Unit) is the 8035 (A54, schematic page 1). It is the Intel "Single Chip Computer", containing control circuitry for program execution, as well as program registers, read/write memory, and I/O ports. The 8035, a member of the 8048 family of single chip computers, is the version which does not contain the program ROM memory internally. The system could, if desired, use an 8048 or 8748 (each of which has 1K bytes of internal program memory) or an 8049 (which has 2K bytes of internal program memory). Using these devices can eliminate the need for all or part of the external program memory (A49 and A50, page 2). The exact configuration is an implementation and cost trade-off decision. When using internal program memory the EA (External Access) pin must be grounded by installing jumper W1 (page 1).

Appendix A contains the current 8035/8048/8748/8049 specification.

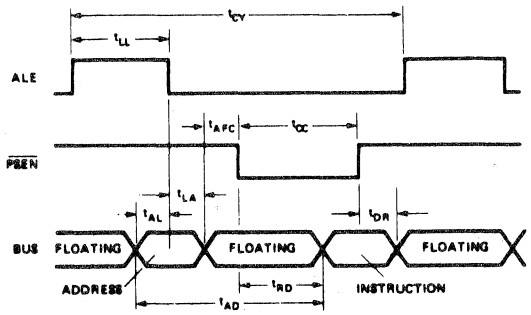
CLOCK: The CPU clock is the +6MHz (5.9535 MHz, more precisely) signal as produced by the clock generator (page 4). (See Section 5.1.) It is connected to the CPU X1 pin (A54-2, page 1). X2 requires no connection.

RESET: CPU power-up reset is effected in the normal manner by connecting the 1μF capacitor (C1) to CPU pin 4 (RESET, A54-4, page 1) and to ground. A resistor, internal to the CPU, provides the RC time constant.

ALE: The Address Latch Enable (ALE, A54-11, page 1) signal occurs once during each CPU cycle (every 2.5 μsec.). This occurs during every internal CPU cycle as well as every external CPU cycle. There are two types of external cycles: instruction fetch and data read/write. ALE is used for both in order to latch the 8 lower address bits.

$\overline{\text{PSEN}}$: Following ALE, for each external instruction fetch, the Program Store Enable ($\overline{\text{PSEN}}$, A54-9, page 1) signal occurs, see Figure 2.1. This causes a byte to be read from the program ROM (see Section 2.3.1 and 4.1).

FIGURE 2.1: INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY

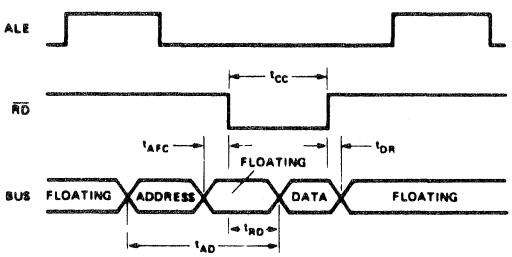


(See Appendix A for AC/DC characteristics.)

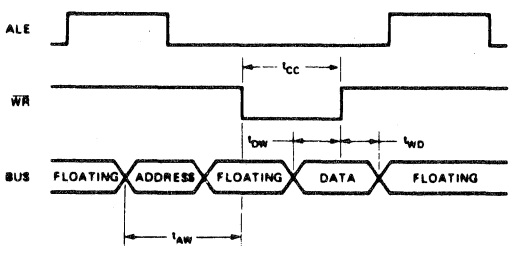
$\overline{\text{RD}}$ and $\overline{\text{WR}}$: Following ALE, for each external data read/write, either the BUS read ($\overline{\text{RD}}$, A54-8, page 1) or the BUS write ($\overline{\text{WR}}$, A54-10, page 1) signal occurs. This causes a byte to be either read from external data memory or written to external data memory, see Figure 2.2.

FIGURE 2.2:

READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY



(See Appendix A for AC/DC Characteristics.)

This system uses these read/write cycles to perform external accesses to Data RAM (Section 2.3.2), Display RAM (Section 2.3.3), and memory mapped I/O (Section 2.4).

All other CPU signals are used as bus or I/O signals. They are described in other sections of this document:

PIN NAME	A54 PIN NUMBER	SIGNAL	Section
DBØ→DB7	12→19	Data Bus	2.2
P2Ø→P23	21→24	Address Signals (4MSBS)	2.2.2
P24	35	+4Hz FLASHER	2.4.1
P25	36	-DCR	2.4.2
P26	37	-PTR RDY	2.4.2
P27	38	-HALF DUPLEX	2.4.2
INT	6	-VSYNC	2.4.1
T1	39	-ADV BLANK	2.4.1
TØ	1	-CTS	2.4.2
P1Ø→P17	27→34	KEYBOARD CONNECTOR P1- 8→15	2.4.3
$\overline{\text{PROG}}$	25	-RESETUART	2.4.2

Figure 2.2.1 CPU Signals

2.2 BUS

During the external CPU cycles described in Section 2.1, the Data/Address bus signal lines carry the address information to the external components and the data information to or from those components.

2.2.1 DATA

The eight data lines +DBØ through +DB7 carry the data between the CPU pins (A54-12→19, page 1) and all of the external memory and I/O devices (pages 1 through 4). Additionally, during ALE, data lines provide the eight

least significant address signals to the D inputs of the address latch (74LS373, A51, page 1). (See timing in Figures 2.1 and 2.2). The data lines are pulled up to provide adequate high drive characteristics.

2.2.2 ADDRESS

There are twelve address lines, +AØ through +A11, used to address the memories and memory mapped I/O. The eight least significant address bits are latched (in 74LS373, A51, page 1) during ALE. The outputs of this latch provide +AØ through A7, all of which are used by the memories on pages 2 and 3. The four most significant address bits are provided by the CPU via the output pins P2Ø→P23 (A54 - 21→24) for +A8, +A9, +A10, and +A11. Four 74LS04 inverters (of A67) buffer +A11 and +AlØ, which are used for memory and memory-mapped I/O selection.

All twelve Address lines go to the program ROMs (A49 and A50) on page 2. (See Section 2.3.1.)

The data's address space is used by the RAMs and the memory mapped I/O. When +A11 is high +AØ through +A10 address the display RAM, page 3, see Section 2.3.3. When +A11 is low, and +AlØ is low, then +AØ through +A7 address the data RAM (page 2, A52 and A53, see Section 2.3.2). When +A11 is low, and +AlØ is high, then the memory mapped I/O decoder (74LS42, A58, page 1) is enabled, see Section 2.4.

2.3 MEMORY INTERFACES

2.3.1 PROGRAM ROM INTERFACE

When external program instruction memory is required, then IC locations A49 and A50 (page 2) are used. The types and configurations of ROMs used determine the operation:

	CONFIGURATION	ROM In A49	ROM In A50	JUMPERS W26	W27	W28	W29
#1:	NO EXTERNAL ROM	NONE	NONE	D.C.	D.C.	D.C.	D.C.
#2:	2K EXTERNAL ROM LOCATED 0→2K	NONE	2316E	OUT	IN	OUT	IN
#3:	2K EXTERNAL ROM LOCATED 2K→4K	2316E	NONE	OUT	IN	OUT	IN
#4:	4K EXTERNAL ROM	2316E	2316E	OUT	IN	OUT	IN
#5:	4K EXTERNAL ROM	2332	NONE	IN	OUT	IN	OUT

Figure 2.3.1 ROM Configuration D.C. = DON'T CARE

The configuration determines which instruction fetches will result in external ROM accesses. Note that an 8048, which has 1K of internal program memory, will only execute external fetches for the 1K to 4K address range (unless the EA pin is pulled high). Section 4.1 describes the operation of the ROMs.

2.3.2 DATA RAM INTERFACE

The 256 x 8 Data RAM is selected when the external address is:

A11	A10	A9	A8	A7 A0	
0	0	D.C.	D.C.	byte select	D.C. = DON'T CARE

which, in hex, is 0XX = 1XX = 2XX = 3XX, where XX is the byte select.

2.3.3 DISPLAY RAM INTERFACES

There are two 2048 byte display RAM PAGES. (Only 1920 bytes are actually displayed in standard operation.) (four 2114's; A6, A8, A10, and A12; on schematics page 3) can be addressed when +PG SEL is set true (output bit 0

to memory mapped I/O location 4ØC; see Section 2.4.1.). PAGE 2 (four 2114's; A5, A7, A9, and A11; on schematics page 3) can be addressed when +PGSEL is set false (i.e., to zero).

For whichever of the two PAGEs is enabled (by +PGSEL), the Display RAM is selected when the external address is:

A11	A10→AØ
1	byte select

which, in hex, is 8XX—FXX.

Performing a read or write to external data memory in this address range will automatically override the refresh circuitry's addressing of the Display RAM, giving the CPU priority at all times. Section 2.4.1 describes how the CPU can be synchronized with the refreshing to accomplish accesses only during blanking periods.

Due to hardware implementation efficiencies the addressing of the 1920 characters being displayed on the CRT is not a direct linear mapping within the 2048 byte Display RAMs. Table 2.1 shows 80 character by 24 line display with the corresponding Display RAM locations for each character.

2.4 I/O CONTROL AND STATUS INTERFACES

All memory mapped I/O ports use the 74LS42 decoder (A58, page 1) to detect the +A2, +A3, +A10, and +A11 address lines. +A2 and +A3 select which port is being addressed, while the combination of +A11 = 0 and +A10 = 1 is required for all memory mapped operations. Additionally the keyboard circuitry uses +AØ and +A1, and the CRT chip uses +AØ, +A1, +A4, and +A5 for additional addressing.

TABLE 2.1

Corresponding Display RAM Addresses
for the 80 Character x 24 Line Display

CHAR ROW DEC	CHAR ROW HEX	CHAR POSITION: DEC	0----------15	16----------31	32----------47	48----------63	64----------79	ROW DEC.
		CHAR POSITION: HEX	0----------F	10----------1F	20----------2F	30----------3F	40----------4F	
0	0		800----------83F				E00----------E0F	0
1	1		840----------87F				E40----------E4F	1
2	2		880----------8BF				E80----------E8F	2
3	3		8C0----------8FF				EC0----------ECF	3
4	4		900----------93F				F00----------F0F	4
5	5		940----------97F				F40----------F4F	5
6	6		980----------9BF				F80----------F8F	6
7	7		9C0----------9FF				FC0----------FCF	7
8	8		A00----------A3F				E10----------E1F	8
9	9		A40----------A7F				E50----------E5F	9
10	A		A80----------ABF				E90----------E9F	10
11	B		AC0----------AFF				ED0----------EDF	11
12	C		B00----------B3F				F10----------F1F	12
13	D		B40----------B7F				F50----------F5F	13
14	E		B80----------BBF				F90----------F9F	14
15	F		BC0----------BFF				FD0----------FDF	15
16	10		C00----------C3F				E20----------E2F	16
17	11		C40----------C7F				E60----------E6F	17
18	12		C80----------CBF				EA0----------EAF	18
19	13		CC0----------CFF				EE0----------EEF	19
20	14		D00----------D3F				F20----------F2F	20
21	15		D40----------D7F				F60----------F6F	21
22	16		D80----------DBF				FA0----------FAF	22
23	17		DC0----------DFF				FE0----------FE0	23

The 74LS42 (A58) decoder must also be enabled by the delayed signal which is the OR of the RD and WR signals. (This delay provides adequate data setup time for the UART.)

The $\overline{WR}$ signal provides the "C" input (A58-1) to the decoder, which causes decoder outputs Ø→3 to be "I/O writes" and 4→7 to be "I/O reads."

I/O beyond the memory mapped I/O comes directly from CPU I/O pins. All of the I/O is described in Sections 2.4.1 through 2.4.4, below.

2.4.1 CRT CHIP AND DISPLAY CONTROL

CRT CHIP: The CRT chip responds to the following memory-mapped I/O addresses:

Figure 2.4.1a CRT Chip Addressing

ADDRESS BIT												ADDR IN	RD	CRT CHIP
11	10	9	8	7	6	5	4	3	2	1	Ø	HEX*	or WRT	OPERATION
0	1	D.C.	D.C.	D.C.	D.C.	X	X	0	0	X	X			SELECT CRT CHIP
0	1	D.C.	D.C.	D.C.	D.C.	0	0	0	0	0	0	400	WRT	CONTROL REG Ø
↑	↑	↑	↑	↑	↑	0	0	↑	↑	0	1	401	WRT	" " 1
						0	0			1	0	402	WRT	" " 2
						0	0			1	1	403	WRT	" " 3
						0	1			0	0	410	WRT	" " 4
						0	1			0	1	411	WRT	" " 5
						0	1			1	0	412	WRT	" " 6
						0	1			1	1	413	RD	Processor Self Load NOT USED
						1	0			0	0	420	RD	Read Cursor Char Addr.
						1	0			0	1	421	RD	Read Cursor Line Addr.
						1	0			1	0	422	RD	Reset
						1	0			1	1	423	RD	Up Scroll
						1	1			0	0	430	WRT	Load Cursor Char Addr.
						1	1			0	1	431	WRT	Load Cursor Line Addr.
↓	↓	↓	↓	↓	↓	1	1	↓	↓	1	0	432	RD	Start Timing Chain
0	1	D.C.	D.C.	D.C.	D.C.	1	1	0	0	1	1	433	RD	Non-Processor Self Load NOT USED

D.C. = DON'T CARE *Assumes DON'T CARES = Ø

The above CRT Chip operations are as defined in the 5027 CRT CHIP specifications, Appendix B. In order to attain the 24 lines of 80 characters each at either 50 Hz or 60 Hz, the Control Registers should be loaded by the

CPU as follows:

Figure 2.4.1b Control Register

CONTROL REGISTER	VALUE (IN HEX)	
	50 Hz	60 Hz
Ø	68	68
1	43	43
2	4D	4D
3	97	97
4	22	Ø7
5	32	17
6	17	17

Section 5.2 describes the operations directed by the above control registers.

-VSYNC: The CPU receives the vertical synchronizing signal at the INT input of the CPU (A54-6, page 1). This allows the CPU firmware to perform timed operations based on the very precise 50 Hz or 60 Hz -VSYNC signal.

-ADVBLANK: The CPU can synchronize to the display's blanking time by sensing this signal. This allows the CPU to perform Display RAM accesses only during blank times, if desired, to avoid visable effects on the display. When the CRT CHIP is programmed with the standard values (as listed above) the -ADVBLANK signal is 25 character times long (active low) during horizontal blanking. However, Display RAM access by the refresh circuitry starts one character time before the end of -ADVBLANK. This means that from the detected leading edge of -ADVBLANK the CPU has 24 character times (less the sampling period) during which it can be guaranteed blanking. Each character time is 588 nsec. which mean the CPU has 14.1 μsec (less the T1 sampling period) to perform the Display Ram read or write without effecting the refresh logic.

+4Hz FLASHER: The CPU firmware is to generate this output at P24 (A54-35) by using the -VSYNC interrupt input (see above) and dividing down appropriately. +4Hz FLASHER is used to flash the Cursor (if jumpered to do so by inserting W25) and is divided by 2 to generate the 2 Hz signal used to gate the blinking video field(s) on and off.

+FORCE BLANK: The CPU firmware can force the video to be blanked by outputting a 1 on this bit. +FORCE BLANK is part of the 74LS174 Output Port (A47-15, page 1) which is loaded by performing the memory-mapped I/O write to location 40C (HEX) or, more precisely,

Address Bit:	11	10	9	8	7	6	5	4	3	2	1	0
Value:	0	1	DC	DC	DC	DC	DC	DC	1	1	0	0

DC = DON'T CARE

Data bit 5 is the +FORCE BLANK bit. Firmware would normally keep an image of this port in RAM, such that only the bits of interest can be changed without affecting the others. A summary of output port 40CH is:

Output to 40CH

Bit	Signal	
7	DON'T CARE	
6	DON'T CARE	
5	+FORCE BLANK	(see above)
4	+SEL LPT	(see Section 2.4.2)
3	-BREAK	(" " ")
2	-RQS	(" " ")
1	+BEEP	(" " 2.4.4)
0	+PG SEL	(see below)

Figure 2.4.1c Output Port 40CH Summary

+PG SEL: The CPU firmware selects which 2048-byte PAGE of display RAM is to be displayed. (Only 1920 characters are actually displayed.) This also selects which RAM is accessed by the CPU via the Display RAM addresses (Section 2.3.3). +PG SEL is set to a 0 to select PAGE 1 and is set to a 1 to select PAGE 2. This control bit is data bit 0 on output port 40CH as described under +FORCE BLANK, above.

2.4.2 UART AND COMMUNICATION CONTROL

UART CHIP: The UART Chip responds to the following memory-mapped I/O addresses:

ADDRESS BIT												ADDR IN HEX*	READ or WRT	UART OPERATION
11	10	9	8	7	6	5	4	3	2	1	0			
0	1	DC	DC	DC	DC	DC	DC	0	1	DC	DC	404	READ	Read Data Enable
0	1	DC	DC	DC	DC	DC	DC	1	0	DC	DC	408	WRT	Write Data Strobe
0	1	DC	DC	DC	DC	DC	DC	1	0	DC	DC	408	READ	Status Word Enable

Data Bit	Status
3	FE, FRAME ERROR
2	PE, PARITY ERROR
1	TBMT, TRANSMIT BUFFER EMPTY
0	DTA, DATA AVAILABLE

DC = DON'T CARE
* Assumes DON'T CARES = Ø

Figure 2.4.2 UART Chip Address

The above UART Chip operations are as defined in the UART specification in Appendix C. The hardware operation of the UART interface is described in Section 6.

+RESET UART: The CPU firmware can pulse this line by using I/O expander instructions (which strobe the $\overline{\text{PROG}}$ output pin of the CPU, A54-25, page 1). This signal is connected to the UART's RESET input.

+SEL LPT: The CPU controls this signal by performing a memory-mapped output operation to address 40CH with bit 4 being +SEL LPT:

Output 40CH

Bit	Signal	
7	DON'T CARE	
6	" "	
5	+FORCE BLANK	(Section 2.4.1)
4	+SEL LPT	
3	-BREAK	(see below)
2	-RQS	(see below)
1	+BEEP	(see Section 2.4.4)
0	+PG SEL	(" " 2.4.1)

When set to 1, the +SEL LPT control line enables the line printer serial communication transmitter (connector P4-3, PRT DATA (RS 232), page 2) and disables the normal transmitter data driver (connector P3-2, TXD (RS 232), page 2). When set to Ø, +SEL LPT disables the printer transmitter and enables the normal serial transmitter. Additionally, +SEL LPT selects the line printer serial baud rate (as determined by switches S3) when set to a 1, or the normal serial baud rate (as determined by switches S1). This allows the printer and normal serial interfaces to have independent baud rates. (Note that the UART does not receive serial data at the normal baud rate when the printer is enabled.)

-BREAK: This signal is controlled by the CPU using address 4ØCH, bit 3 (see above). -BREAK, when set to Ø forces the selected serial transmit line to the "break" state. This allows the CPU firmware to create the desired Break condition for the desired duration.

-RQS: This output bit (address 4ØCH, bit 2, see above) directly drives the normal terminal serial interface's RTS (Request to Send, P3-4, page 2)

which also goes to the modem connector (P6-4, page 2). Additionally this can drive DTR (P3-20, page 2), if enabled using switch S5-3, 12. This bit can also drive the printer's serial port TERM RDY lines P4-8 and/or P4-6 (page 2) which can be connected by jumpers W12 and W13, respectively.

-DCR: The CPU can input -DCR on I/O pin P25 (A54-36, page 1). This signal can come from any of 3 different places: (1) "DCR (RS232)" at P3-6 (page 2) which can be enabled by switch S5-1, 14; (2) "DCR (RS232)" at P3-8 (page 2) which can be enabled by switch S5-2, 13; and (3) Modem connector P6-7 (page 2).

-PTR RDY: The firmware inputs this signal via the CPU I/O pin P26 (A54-37, page 1). It is the Printer Ready signal derived from connector P4-20 (+PTRRDY (RS232), page 2).

-HALF DUPLEX: The CPU firmware reads CPU I/O pin P27 (A54-38, page 1) to determine the Full/Half Duplex mode. When -HALF DUPLEX is Ø the firmware should enter half duplex mode and when 1 the terminal should be in full duplex mode. -HALF DUPLEX is derived from switch S2-3,18 (page 1), one side of which is grounded.

2.4.3 KEYBOARD I/O INTERFACES

The outputs to the Keyboard matrix consist of the 8 lines from the CPU I/O pins P1Ø→P17 (A54-27→34, page 1) which are connected to Keyboard connector pins P1-8 through P1-15, respectively. There are 12 inputs from the matrix and 4 inputs from individual keys. All inputs are pulled up by 1K ohm resistors to +5V.

Figure 2.4.3 Keyboard I/O Interfaces

The CPU reads Keyboard inputs via the following memory-mapped I/O reads:

ADDRESS BIT 11	10	9	8	7	6	5	4	3	2	1	0	ADDR IN HEX*	KEYBOARD INPUTS (P1 Connector Pins) On Data Bits 7	6	5	4	3	2	1	0
0	1	DC	DC	DC	DC	DC	DC	1	1	0	0	40C	+50Hz	(ALPHA) 3	26	(SHFT) 4	(CTL) 6	(FUNC) 5	16	20
								1	1	0	1	40D	"	"	25	"	"	"	17	21
								1	1	1	0	40E	"	"	24	"	"	"	18	22
0	1	DC	DC	DC	DC	DC	DC	1	1	1	1	40F	"	"	7	"	"	"	19	23

Non Keyboard

DC = DON'T CARE
* Assumes DON'T CARES = 0

Note that the 4 individual keys are input on all four addresses. "-50 Hz" is also input with these input operations and is to determine the terminal's refresh rate upon power up, as described in Section 2.4.4.

Appendix D provides the descriptions of keyboard matrix with which this system has been interfaced.

2.4.4 OTHER I/O INTERFACES

-50 Hz: As described under Section 2.4.3, above, this signal can be read by the CPU firmware on memory-mapped I/O address 40C (as well as many others) on data bit 7. The firmware should sense this bit during power-up and initialize the CRT chip accordingly (see Section 2.4.1). When -50 Hz = 0 then the 50 Hz mode should be established, else the 60 Hz mode. This signal is derived from switch S2 pins 17 and 4 (pin 4 is grounded).

+BEEP: The CPU firmware can control the beeper (audio signal, 1200 Hz) with bit 1 of the memory-mapped I/O write to address 40CH (see, also, Sections 2.4.1 and 2.4.2 for the other control bits affected). The +BEEP signal is

gated with the +1200 Hz signal (on page 1 with 74LS00, A61-1,2,3) which is then inverted to drive transistor Q2 which, in turn, drives the 8 ohm speaker connected to P7-1,2. When +BEEP is Ø the gating is such that the +1200 Hz is removed and the transistor Q2 is put in the off (non-conducting) state.

3. OPERATION OF JUMPERS AND SWITCHES

Presented below is a summary of the switches and jumpers used in the system. Included are short descriptions of their functions and references to other pertinent sections of this document. Though redundant, this section should provide quick reference for software, hardware, and systems technical personnel.

JUMPER #	DESCRIPTION		Schem. Page	Reference Sections	Comments
	INSERTED	REMOVED			
W1	USE INTERNAL PROGRAM MEMORY (ROM)	USE EXTERNAL PROGRAM MEMORY (ROM)	1	2.1	
W2					NOT USED
W3					"
W4					"
W6	P3 CONN: CURRENT LOOP SEND SHORT 510 SERIES	KEEP 510 IN SERIES	2	6.3	▷2
W7					NOT USED
W8					"
W9					"
W10					"
W11					"
W12	P4 CONN: TERM RDY (RS232C) SENT ON P4-6	P4-6 NOT CONN	2	6.3	
W13	P4 CONN: TERM RDY (RS232C) SENT ON P4-8	P4-8 NOT CONN	2	6.3	

Table 3.0 Summary of Switches and Jumpers

JUMPER #	DESCRIPTION		Schem. Page	Reference Sections	Comments
	INSERTED	REMOVED			
	P3 CURRENT LOOP SEND				
W14	CONN "COLLECTOR END" TO P3-25	"COLLECTOR END" not CONNECTED TO P3 -25	2	6.3	2
W15	CONN "EMITTER END" TO P3-25	"EMITTER END" NOT CONN TO P3-25	2	6.3	2
W16	CONN "EMITTER END" TO P3-13	"EMITTER END" NOT CONN TO P3-13	2	6.3	2
W17	CONN P3-13 TO GND	P3-13 NOT CONN TO GND	2	6.3	2
W22					Not used
W23					Not used
W24					Not used
W25	CURSOR FLASHES OFF ON (INVERSE VIDEO)	CURSOR DOES NOT FLASH AND IS INVERSE VIDEO	5	5.4	
W26	for 2332 ROM at A49	for all others	2	2.3.1, 4.1	
W27	for 2316E, 8316E, 2716 ROMs at A49 or A50	for all others	2	2.3.1, 4.1	
W28	for 2332 ROM at A49	for all others	2	2.3.1, 4.1	
W29	for 2316E, 8316E, 2716 ROMs at A49 or A50	for all others	2	2.3.1, 4.1	
W30	For all character generator PROMs	For no standard character generator PROMs	5	5.3	

JUMPER #	DESCRIPTION		Schem. Page	Reference Sections	Comments
	INSERTED	REMOVED			
	OPTIONAL RESISTORS				
R28	P3 CONN: CURRENT LOOP SEND, PULLS HIGH END TO +12V.	NOT PULLED UP	2	6.3	▷2

SWITCH #	PINS	DESCRIPTION CLOSED	OPEN	Schem. Page	Reference Sections	Comments
COMMUNICATION PORT BAUD RATE SELECT (P3-2 and 3)						
S1	1-2	19,200	NOT 19,200	6	6.1	
	2-1	9,600	NOT 9,600	6	6.1	
	3-1	4,800	NOT 4,800	6	6.1	
	4-17	2,400	NOT 2,400	6	6.1	
	5-16	1,200	NOT 1,200	6	6.1	
	6-15	600	NOT 600	6	6.1	
	7-14	300	NOT 300	6	6.1	
	8-13	150	NOT 150	6	6.1	
	9-12	75	NOT 75	6	6.1	
S1	10-11	110	NOT 110	6	6.1	
S2	10-11	SHORT OUT 270 IN SERIES WITH CHARACTER VIDEO	KEEP 270 IN SERIES (FOR COMPOS VIDEO)	5	5.4	OPEN FOR COMPOS VID (SEE S2-1,20)
	2-19	SELECT LOWER HALF OF CHARACTER GENERATOR	SELECT UPPER HALF OF CHARACTER GENERATOR	5	5.3	
	3-18	HALF DUPLEX	FULL DUPLEX	1	2.4.2	
	4-17	50Hz	60Hz	1	2.4.4	
	5-16	PARITY IN TRANS AND RCV	NO PARITY	2	6.2; C	(see also S2-9,12)
	6-15	1 STOP BIT (TRANS)	2 STOP BITS (TRANS)	2	6.2; C	
	7-14 NB1 8-13 NB2	BITS PER CHAR	S2-7,14: CLOSED OPEN CLOSED OPEN S2-8,13: CLOSED CLOSED OPEN OPEN #BITS = 5 6 7 8	2	6.2; C	
	9-12	SEND AND RECEIVE: ODD PARITY	EVEN PARITY	2	6.2; C	(see also S2-5,16)
S2	1-20	a)+VIDEO P2-4 GETS COMPOS SYNC TOO	a)+VIDEO P2-4 HAS NO SYNC's	5	5.4	S2-10,11 SHOULD BE OPEN FOR VIDEO WITH COMPOS SYNC
		b)+TTL VIDEO BECOMES VIDEO WITH COMPOS SYNC(P2-6)	b)+TTL VIDEO P2-6 IS ONLY COMPOS SYNC			

SWITCH #	PINS	DESCRIPTION CLOSED	OPEN	Schem. Page	Reference Sections	Comments
S3	1-20	19,200	NOT 19,200	6	6.1	1
	2-19	9,600	NOT 9,600	6	6.1	
	3-18	4,800	NOT 4,800	6	6.1	
	4-17	2,400	NOT 2,400	6	6.1	
	5-16	1,200	NOT 1,200	6	6.1	
	6-15	600	NOT 600	6	6.1	
	7-14	300	NOT 300	6	6.1	
	8-13	150	NOT 150	6	6.1	
	9-12	75	NOT 75	6	6.1	
S3	10-11	110	NOT 110	6	6.1	
S5	1-14	CONN P3: RECEIVE DCR(RS232C) FROM P3-10	DO NOT RECEIVE DCR FROM P3-10	2	6.3	1
	2-13	CONN P3: RECEIVE DCR(RS232C) FROM P3-8	DO NOT RECEIVE DCR FROM P3-8	2	6.3	
	3-12	CONN P3: P3-20 (DTR) DRIVEN BY SAME AS RTS (P3-4				1
	4-11	CONN P3: P3-20 (DTR) PULLED TO +12V VIA 3.3K	P3-20 (DTR) NOT PULLED HIGH			
	5-10 6-9	CONN P3: RECEIVE SERIAL DATA RS232C P3-3	DO NOT RECEIVE SERIAL DATA RS232C P3-3	2	6.3	1
S5	7-8	CONN P3: RECEIVE SERIAL DATA CURRENT LOOP P3-12, 24	DO NOT RECEIVE SERIAL DATA CURRENT LOOP P3-12,24	2	6.3	

1 CLOSED CONDITIONS OF SWITCHES WITHIN INDICATED SWITCH GROUP ARE MUTUALLY EXCLUSIVE

2 MUTUALLY EXCLUSIVE CURRENT LOOP SEND CONNECTIONS FOR P3

P3 CONN: ISOLATED (W6, W-14, W-16 INSERTED) VS. 1-SIDE GND (R28, W15, W17 INSERTED)

4. PROGRAM MEMORY OPERATION

The operation of the hardware for the program memory is described in sections 4.1 (program ROM) and 4.2 (data RAM). The functional interface for system and firmware reference is described in sections 2.3.1 and 2.3.2.

4.1 PROGRAM ROM

When external program memory is required by the CPU, the (P)ROMs at locations A49 and A50 (page 2) are used.

The two ROMs have the 11 address lines and the 8 output data lines in common. The lower 8 address lines (+A7→+AØ) come from the address latch (A51, page 1) and +A10, +A9, and +A8 come from CPU port 2: bit 2 (A54-23, buffered), bit 1 (A54-22) and bit Ø (A54-21), respectively. The output data lines are connected to the CPU data bus (+DB7→+DBØ).

If the ROMs are 2316E types (i.e., 16K bits) then memory address bit A11 (derived from CPU port 2 bit 3, A54-24) selects which ROM is enabled when -PSEN goes active. +A11 and its inverse are each gated with -PSEN (page 1, A66-1,2,3 and A66-11,12,13) yielding -ROM1CS or -ROMØCS, one of which goes active when -PSEN goes active. -ROMØCS goes active for +A11=Ø and -ROM1CS goes active for +A11=1. -ROMØCS selects the ROM at A50 (page 2, A50-20). -ROM1CS selects the ROM at A49 (A49-20). Note that for 2316E-type ROMs jumper W29 is inserted (and W28 is not) in order to pass the -ROM1CS signal. Jumper W27 must be inserted (and W26 not inserted) for 2316E ROMs. This provides pin 21 (on A49 and A50) with +5V, which is required for PROMs (2716 or 2758) that may be used, and provides the high logic level for the ROMs that have a positive chip select at this pin.

If a 2332-type (i.e., 32K bit) ROM is used then jumper W28 and W26 must be inserted while omitting W29 and W27. This provides A49-20 with -PSEN directly such that this ROM is selected on every -PSEN cycle, not just when +A11=1. Jumper W26 connects +A11 to A49-21 providing the ROM with the required 12th address bit.

The negative chip select at pin 18 (on A49 and A50) is permanently grounded.

4.2 DATA RAM

The 2111A (or 8111A) RAM chips (page 2, A52 and A53) comprise a 256 x 8 block of read/write memory, with A52 providing for data bits 7, 6, 5, and 4 and A53 for bits 3, 2, 1 and Ø. This data leaves and enters via IO1→IO4 (pins 11→14) on A52 and A53, and is connected to the CPU data bus +DB7 +DBØ (see page 2). The required 8 address bits are +A7→+AØ.

This 256 x 8 RAM is enabled when +A10 and +A11 are both logic Ø by generating -DSCS (page 1, A66-4,5,6) which connects to A52-15 and A53-15.

-DSCS in conjunction with -RD pulse (from the CPU, page 1, A54-8) causes the RAMs' outputs to be enabled (via A52 and A53 pin 9). During -RD the addressed data is then driven onto the data bus.

-DSCS in conjunction with -WR pulse (from the CPU, A54-10) causes the RAMs (via A52 and A53 pins 16) to write the 8 bits from the data bus at the addressed internal locations.

5. DISPLAY OPERATION

5.1 CLOCK GENERATION

The crystal oscillator (page 4) uses an astable 74S04 configuration to generate the 23.814 MHz signal (at A55-4). The crystal is series resonant at 23.814 MHz. The 74LS109 flipflop (A56-2→7) divides the basic clock by 2 to provide an 11.907 MHz "square" wave, +CLK (A56-6) and -CLK (A56-7). These two signals go on to the Video Generation circuitry on page 5 (see Section 5.4) to provide the gating and shifting clock for the basic dot of the video generation.

See Figure 5.1 for the timing diagram.

The 74LS163 dot counter (page 4, A57) provides the display character clock (+DC CARRY, A57-15) to the video generation logic (page 5) and its frequency equivalent, -DC2 (A55-12), to the 5027 CRT Chip (at A23-12, page 4). The counter's bits Q_A, Q_B, and Q_C generate the dot counter bits +DCØ, +DC1, and +DC2, respectively. +DCØ and +DC2 are used on page 5 by the video generation circuitry (Section 5.4). +DC1 generates an asymetrical 3.402 MHz (11.907 ÷ 3.5) signal which is used on page 6 by the baud rate generator (Section 6.1).

+CLK is divided by 2 by the 74LS109 (page 4, A56-10→15) to generate +6MHz (actually 5.9535 MHz) on A56-10. +6MHz goes to the CPU (page 1, A54-2) to provide the basic CPU clock.

5.2 CRT CHIP OPERATION

The CRT 5027 Video Timer and Controller ("VTAC" or "CRT CHIP") for SMC Microsystems Corporation is described in detail by the specification in Appendix B. This section describes the CRT Chip's specific operation

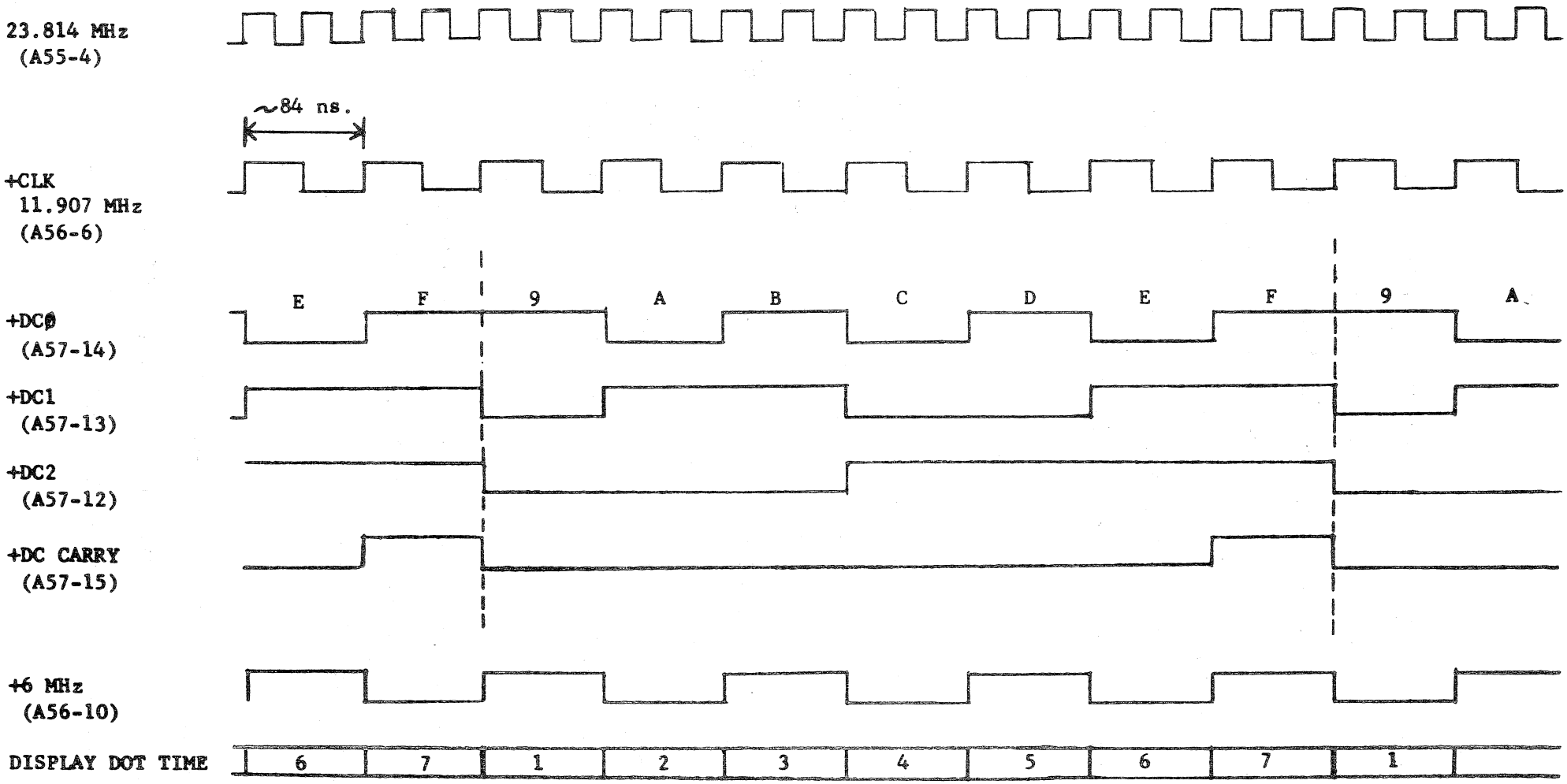


FIGURE 5.1
CLOCK GENERATION TIMING DIAGRAM

when the control registers are programmed for this system as described in Section 2.4.1.

Clock Input: The clock input (DCC, A23-12, page 4) to the CRT chip is at the display character rate. It is the same as the inverse of +DC2 in Figure 5.1. The CRT Chip Specification in Appendix B shows timing of the output signals relative to the input clock.

Hardware Addressing Operation: Accessing the CRT CHIP (page 4) is performed by presenting the proper address inputs (A3→AØ, A23-2,1,40, and 39) and then providing a negative strobe at the data select ($\overline{DS}$, A23-9). Depending on the address inputs the chip performs a read (DB7→DBØ, A23-18→25, drive the CPU data bus +DB7→+DBØ) or a write (the chips DB7 DBØ accept data from the CPU data bus +DB7→+DBØ). Of the 16 addressable I/O registers (ports in the CRT CHIP) 9 are output (write) and 7 are input (read) ports. The address table in Section 2.4.1 shows which ports are write and which are read. Note that the address lines connected to the chip's address pins are: +A5, +A4, +A1 and +AØ to the chip's A3, A2, A1, and AØ, respectively. Since the CRT Chip wants only one control strobe (i.e., not both a read and a write strobe) the read and write outputs of the I/O decoder (page 1, A58) for address decodes "400" are logically OR'd (by A43-11,12,13, page 1) yielding -SEL CRT CHIP. This signal provides the data select for the CRT Chip (A23-9, page 4). The "400" decoded signal, in conjunction with the 4 address lines, accounts for the I/O address locations (as presented in the table in Section 2.4.1).

Operation of CRT Chip programming: As stated in Section 2.4.1 the 7 control registers must be programmed for either 50 Hz or 60 Hz for standard operation:

CONTROL REGISTER	VALUE (IN HEX)	
	50 Hz	60 Hz
Ø	68	68
1	43	43
2	4Ø	4Ø
3	97	97
4	22	Ø7
5	32	17
6	17	17

Variations from this might be possible for special cases, but for 24 lines of 80 displayed characters (at 50 Hz or 60 Hz refresh rates) it is necessary to use these values with the clock generation and video generation circuitry provided in this system.

The above control register values provide the following parameters to the CRT Chip (see also the CRT Chip timing, Figure 5.2):

5.2.1 -- Control Register Ø

Bits 7→Ø = N; Horizontal Line count where Total Characters/Line = N + 1.

50 Hz Total Characters/Line = 68_{16} + 1

= 104_{10} + 1

= 105

60 Hz --Same--

5.2.2 -- Control Register 1

Bit 7; Interlaced/Non-Interlaced

where 1 = Interlaced; Ø = Non-Interlaced

50 Hz Bit 7 = Ø, Non-Interlaced

60 Hz --Same--

Bits 6→3 = N; Horizontal Sync Width

where Horiz Sync Width Character Times = N

(N = 1→15; N = Ø, disallowed)

50 Hz Horiz Sync Width Char Times = 8

60 Hz --Same--

Bits 2→Ø = N; Horizontal Sync Delay

where Horiz Sync Delay Char Times = N

(N = 1→7; N = 0, disallowed)

50 Hz Horiz Sync Delay Char Times = 3

60 Hz --Same--

5.2.3 -- Control Register 2

Bit 7, not used (= Ø)

Bits 6→3 = N; Scans/Data Row

Where Scans/Data Row = N + 1

50 Hz Scans/Data Row = 9 + 1
= 10_{10}

60 Hz --Same--

Bits 2→Ø = T; Characters/Data Row

where T is defined in a table in the CRT Chip Specification (Appendix B, last page).

For DB 2 = 1, DB1 = Ø, DB Ø = 1 the

Characters per Data Row = 80

50 Hz Characters/Data Row = f(T)
= f(5)
= 80_{10}

60 Hz --Same--

5.2.4 -- Control Register 3

Bits 7, 6 = T; Skew Bits (Refer to 5.4)

where T is defined in a table in the CRT Chip Specification (Appendix B, last page).

For DB 7 = 1, DB 6 = Ø the Skew Bits

are Sync/Blank Delay = 1 Character Time

Cursor Delay = Ø Character Time

50 Hz Skew Bits = f(T)

= $f(2_{10})$

= Sync/Blank Delay of 1 Char Times

Cursor Delay of no Char Times

60 Hz --Same--

Bits 5→Ø = N; Data Rows/Frame

where Number of Data Rows = N + 1

(N = Ø 63)

50 Hz Number of Data Rows = 17_{16} + 1

= 23_{10} + 1

= 24

60 Hz --Same--

5.2.5 -- Control Register 4

Bits 7→Ø = N; Scans/Frame

where, in non-interlaced mode,

Scans/Frame = 2N + 256

50 Hz Scans/Frame = $2 \cdot 22_{16} + 256_{10}$

= $2 \cdot 34_{10} + 256_{10}$

= $68_{10} + 256_{10}$

= 324_{10}

60 Hz Scans/Frame = 2·Ø7 + 256

= 14 + 256

= 270_{10}

5.2.6 -- Control Register 5

Bits 7→Ø = N; Vertical Data Start

where N = number of raster lines after leading edge of vertical sync of vertical start position.

50 Hz Vertical Data Start (raster lines) = 32_{16}

= 50_{10}

60 Hz Vertical Data Start (raster lines) = 17_{16}

= 23_{10}

5.2.7 -- Control Register 6

Bits 7, 6, not used (= Ø)

Bits 5→Ø = N; Last Displayed Data Row

where N = Address of last displayed data row, N = 0 to 63

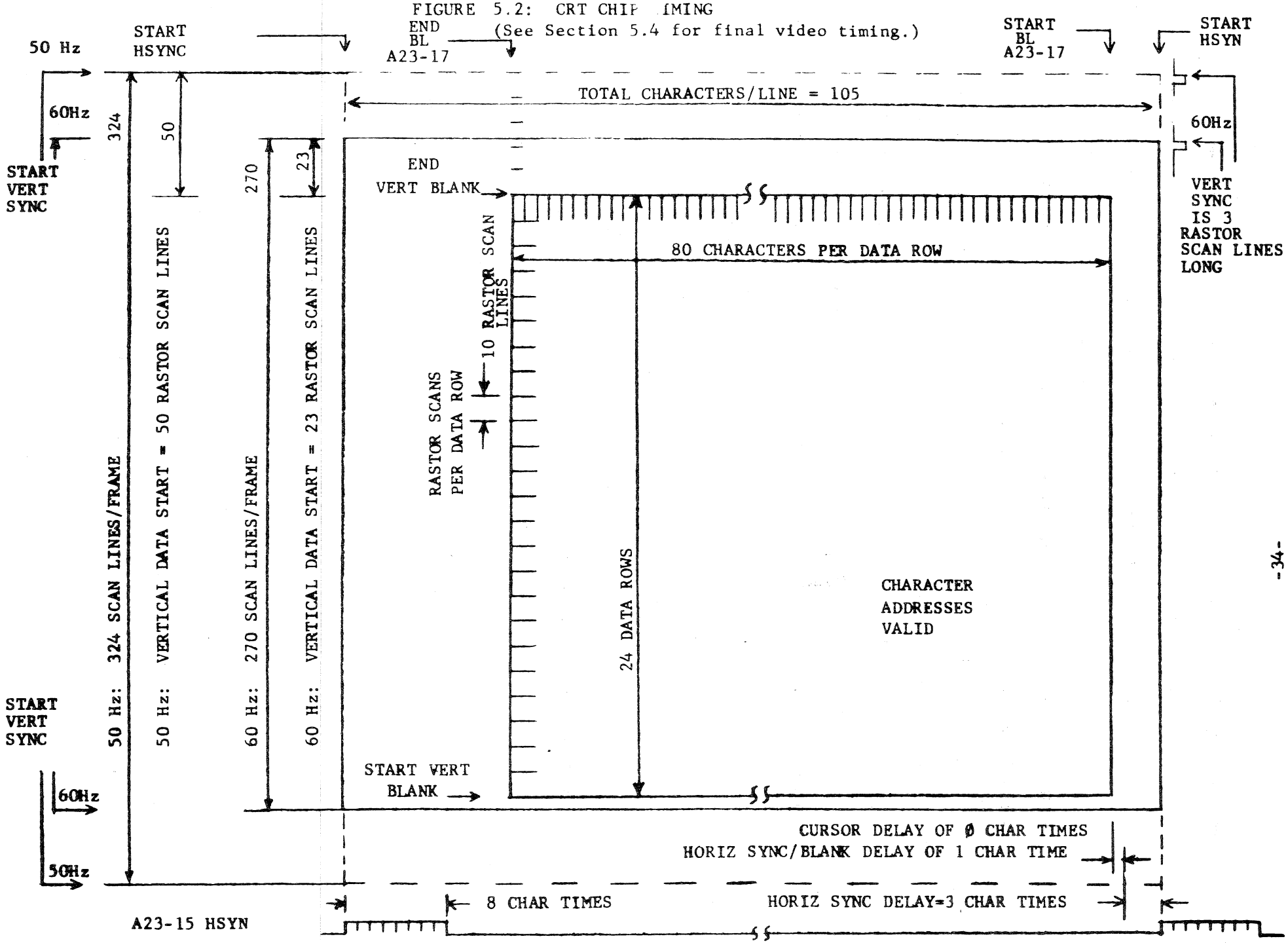
50 Hz Last Displayed Data Row = 17_{16}

= 23_{10}

60 Hz --Same--

Figure 4.2 presents the timing of a frame showing the relationship between the Valid Character Addresses (for the 24 80-character rows) and the Blanking and Sync signals. The left and right edges correspond to the start of Horizontal Sync, and the top and bottom edges (different for 50 Hz and 60 Hz) correspond to the start of Vertical Sync. The inner solid-lined rectangle (24 Data Rows x 80 characters) represents the time during which the CRT Chip outputs valid addresses on H6→HØ (A23-32→38, page 4), R3→RØ (A23-4,5,7,8), and DR4→DRØ (A23-30,29,28,27,26). The H6→HØ lines go from Ø to 79 on each scan across the 80 character positions. R3→RØ count out the 24 character rows, covering all rows Ø through 23 on each frame (the starting and ending counts are programmatically changed using the Last Data

FIGURE 5.2: CRT CHIP TIMING
(See Section 5.4 for final video timing.)



Row Control and/or the Up Scroll command).

The positive-true blanking signal (BL, A23-17, page 4) is emitted 1 character time after the end of the last (80th) character to the end of the 1st character address, as well as continuously from the end of the last character row until the beginning of the first character row. (Note that additional data pipelining and blanking flipflop delays cause the final video and blanking to have a different timing relationship--see Section 5.4.)

The Horizontal Sync (HSYN, A23-15) and Composite Sync (CSYN, A23-10) are each delayed by 1 character time (as for blanking, above) and additionally have a "front porch" of 3 more character times before the HSYNC begins. (See Section 5.4 for final video/sync/blanking relationships.) The HSYN signal and the horizontal part of CSYN are 8 character times long.

Vertical Sync (VSYN, A23-11, page 4) starts after the last scan line of the frame and lasts for 3 horizontal scan line times. CSYN is VSYN OR'd internally with HSYN. The programming of the Total Scan Lines per Frame determines whether there are 50 or 60 frames per second. Following the last scan line (at the same time VSYN starts) the Vertical Data Start is delayed by 50 scan lines for 50 Hz and by 23 scan lines for 60 Hz. This is varied to provide for approximately the same vertical centering for both 50 Hz and 60 Hz.

The cursor signal (CRV, A23-16, page 4) is not delayed (internal to the CRT Chip) and is emitted during the times when the internal Cursor Address matches the Character Address (row (DR5→DRØ) and horizontal position (H6→HØ)). (Note that the external pipeline and delays will cause the final video and cursor to have the same relationship but actual displayed video occurs two character times later; see Section 5.4).

Refer to the CRT Chip Specification (Appendix B) for the functional operation of the other (non-initializing) CRT commands. Section 2.4.1 provides the I/O addresses to be used for these commands. (Note that Processor Self Load and Non-Processor Self Load commands do not apply to this system--self load is not used.)

5.3 DISPLAY RAM AND CHARACTER GENERATION

The displayed characters are stored and retrieved from the 2114-3 RAMs (random access, read/write memories) shown on page 3. There are two display pages (banks) of 1920 characters (bytes) each. Display Page 1 is composed of A6,8,10 and 12 and is enabled when +PG SEL (A47-2, page 1) is low (logic Ø). (+PG SEL is data bit Ø on output port 4ØCH. See Section 2.4.1.) +PG SEL enters the decoder 74LS139 (A27-3, page 3) to cause the proper RAMs to be selected, as described in this table:

TABLE 5.1: DISPLAY RAM CHIP SELECT

	DISPLAY PAGE 1		DISPLAY PAGE 2	
+PG SEL	0	0	1	1
HIGH ORDER ADDRESS BIT (A10 or +RAM1Ø)	0	1	0	1
RAM Chip for +DISP DATA 7,2,1,Ø (IC Numbers are given.)	A12	A10	A9	A11
RAM Chip for +DISP DATA 6,5,4,3 (IC Numbers are given.)	A8	A6	A5	A7

The 11 address lines come from either of two sources: the CPU's +AØ→A1Ø or from the CRT Chip (and associated logic) addresses +RAMØ→+RAM1Ø. The CPU's address lines are the normal ones (as described in Section 2.2.2). The CRT Chip's address lines are derived from the data row (DRØ→4) and data column (HØ→6) address outputs (see A23, page 4). Combinatorial logic gates (page 4;

A34-1,2,3, A34-11,12,13, A37, A38-1,2, A38-3,4, A38-5,6, and A38-8,9) condition the CRT address outputs such that:

(1) the 1st 64 characters of each data row are ordered sequentially in the +RAMx addresses from Ø to DFFH.

(2) the last 16 characters of each data row are placed in the +RAMx addresses from EØØH to FFFH (with 8 16-byte holes being unused).

Table 2.1 in Section 2.3.3 shows exactly which +RAMx addresses correspond to the character position addresses. This mapping is performed in order to get the 1920 characters within the 2048-byte RAM, by transforming the 12 row/column addresses (5 row, 7 column) into 11 RAM address lines.

The most significant address bit (1Ø) enters the same decoder (page 3, A27-2), as did +PG SEL. Table 5.1, above, shows how this selects a pair of RAM chips.

The selection between the CPU addresses (+AØ→+A10) and the CRT chip's refresh addresses (+RAMØ→+RAM1Ø) is made using three quad multiplexers (A24, A25, and A26, page 3). The multiplexers normally select the CRT Chip addresses, but when the CPU performs an external data read or write with +A11 = 1 then the multiplexers automatically select the CPU's address lines. The advanced read-or-write signal +ADVRDOR WR (from A39-6, page 1) is gated with +A11 (at A40-1,2,3, page 3) to form the multiplexer control signal.

Data between the CPU (via +DB7→Ø) and the display RAMs (+DISP DATA 7→Ø) is transferred through the 8304 bi-directional transceiver (A13, page 3). The +RD PULSE from the CPU (A38-12 inverted from A54-8, page 1) controls the direction of the transceiver for CPU reads from or writes to the RAM. The

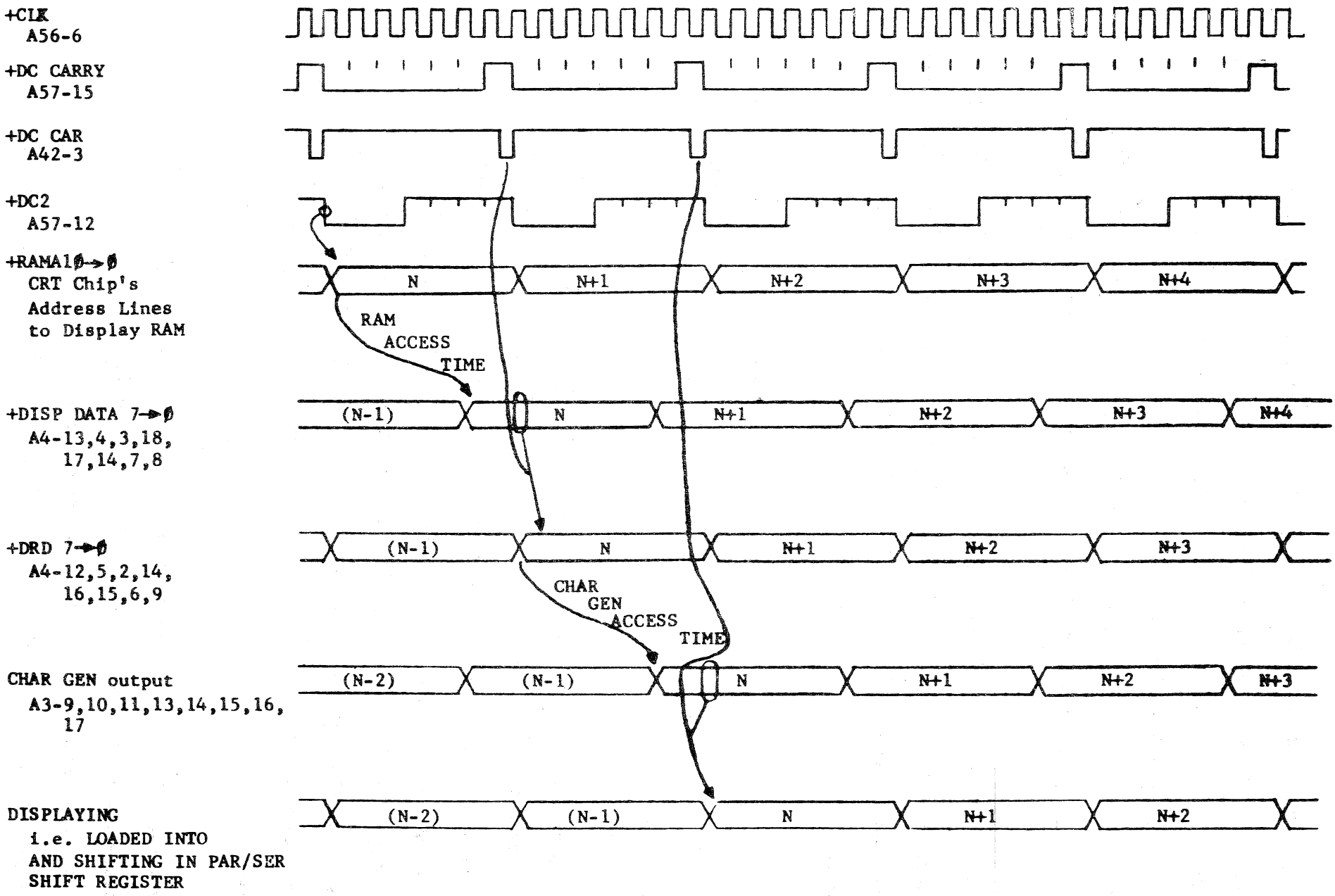


FIGURE 5.3: DISPLAY DATA TIMING

delayed read-or-write signal +RD OR WRT (A41-10, page 1) is gated with +A11 (A40-11,12,13, page 3) such that when +A11 = 1 for a +RD OR WRT the transceiver is enabled (A13-9, page 3). The delayed write pulse (-WRT PULSE, A40-8, page 1) is gated with the inverse of +A11 (A40-6, page 3) using a 74LS32 gate (A34-8,9,10) to generate the write-enable signal that goes to the RAM's. (pins 10). This signal is delayed by -WRT PULSE) at the beginning to provide proper address setup time, but goes away early (with the CPU's -WR signal) to provide guaranteed data (on writes) and address hold times.

The CPU can synchronize itself with the video so that it only accesses during blanking periods. The synchronization can be done such that one character can be transferred during horizontal blanking by using -ADV BLANK which is connected to T1 (A54-39, page 1); or the CPU can transfer a number of characters during vertical blanking by reacting to -VSYNC which is connected to INT (A54-6, page 1). Failure to synchronize may cause 1 or 2 displayed character's worth of a scan line to be garbaged on the CRT. This might appear as "drop-outs" on the display.

During normal display refresh cycles the addresses to the RAM's are multiplexed to come from the CRT chip's +RAMØ→1Ø. (+PG SEL is still in effect, see Table 5.1). The data being read from the RAMs on +DISP DATA 7→Ø goes to the pipeline latch (A4, page 5). Figure 5.3 shows the timing for accessing and transferring the display data. +DC CAR (A42-3, page 5) shows the times for accessing or transferring successive characters. +DC2 is the basic data character clock going to the CRT Chip (being inverted and input or DCC, A23-12, page 4).

The +RAM A1Ø→Ø addresses from the CRT chip change following the indicated edge of +DC2. Call this new address "N". The RAMs access location N,

putting valid data onto the +DISP DATA 7→Ø lines before the next +DC CAR pulse. When that pulse occurs the +DISP DATA for character N is loaded into the pipeline latch (A4-11, page 5) causing the outputs of the latch (+DRD 7→Ø) to be the code for character N. (Refer to Figure 5.3.)

+DRD 6→Ø comprise part of the address inputs to the character generator ROM. Three of the scan row address lines +DOTA 2→Ø (A23-5,7,8) provide the rest of the address inputs. (DOTA 2→Ø do not change on a character by character basis, only line by line; see Appendix B.) During the next character-time the character generator is accessing the dot information for the addressed character's addressed scan-row, see Figure 5.3. By the next +DC CAR pulse the character generator output is available to be loaded into the shift register (A2, page 5) and the dot-shift control logic (A45, page 5, see Section 5.4). Note that while character N is being displayed, character N+2 is being accessed by the display RAM and that character N+1 is being accessed by the character generator ROM.

+DRD7 (A4-12, page 5) from the pipeline latch, indicating a character to be displayed with "half" intensity, goes to a flip-flop (A16-12, page 5) where it is latch by the next +DC CAR. This causes the displayed character's video intensity to be reduced (see Section 5.4). The pipeline latch outputs +DRD5 and +DRD6, when both low, cause the video to be suppressed and +DRD4,3, 2,1, and Ø to be used as special control information. Section 5.4 describes the operation of these circuits.

The character generator is designed to produce patterns for 96 characters. (32 character positions are lost for the control codes referred to above.) Each character has 8 scan lines available and 8 bits of pattern information

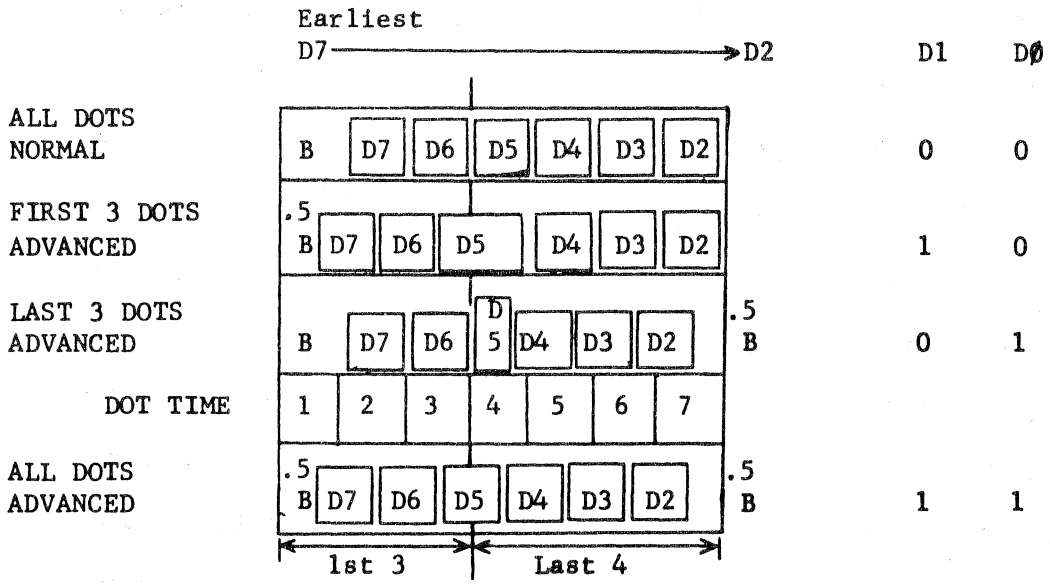
are produced. This calls for a ROM capacity of 128 (=96+32) characters X 8 scan lines X 8 bits = 8K bits. The ROM's socket location is made to accept a 2758, 2716, or 2316E. The 2758, being exactly 8K bits, satisfies the requirements. To use it jumper W30 (page 5) must be installed and switch S2,19 (page 5) must be closed. The 2716 and 2316E, being 16K bits, have twice the capacity and can provide two different character sets. S2 closed provides one and S2 open provides the other. (Jumper W30 must always be installed.)

There are 10 raster scan lines (Ø→9) per character row, but only 8 can have specified display data in the character generator. Rows Ø and 9 are always blanked as far as pattern information from the character generator is concerned (but row 9 may have the controlled underline information, see Section 5.4.). This is why only three scan line addresses, enter the character generator ROM (A3-6,7,8 page 5). Each consecutive 8 locations in the ROM are for each character. Note that the first 32 characters (groups of 8) are lost, as described above. Location Ø within a group of 8 for a character, has the video pattern information for the rastor scan line number 8 (out of the Ø→9). The locations 1 to 7 have information for scan line number 1 to 7, respectively. For example the character at locations 1ØØH to 1Ø8H (the first displayable character, i.e. the 33rd group of 8) has the following relationships:

1ØØH	Scan Line 8 data pattern
1Ø1H	" " 1 " "
1Ø2H	" " 2 " "
1Ø3H	" " 3 " "
1Ø4H	" " 4 " "
1Ø5H	" " 5 " "
1Ø6H	" " 6 " "
1Ø7H	" " 7 " "

The data pattern for each scan line of each character is determined from the 8 bits at the ROM location. 6 of the bits represent the actual dots to be displayed. The other 2 bits specify the half-dot shift characteristics of the 6 displayed bits. This half-dot shift characteristic provides for a much finer horizontal resolution without increasing CRT bandwidth requirements. ROM output bits D1 and DØ (A3-10,9, page 5) provide the dot shift specification. D7→D2 (A3-17,16,15,14,13,11) provide the actual dot information. D7 goes out first in time. A 1 for any bit indicates positive (brighter) video. The 4 possible half-dot shift patterns are as follows:

FIGURE 5.4: DOT SHIFT FORMATS



B = Blank Dot Position
.5B = ½ Blank Dot Position

NOTE: The dots and shift controls must be encoded such that there will be no ½ dot actually formed (i.e. ½-dot on or off between two other dots that are both the same but opposite the polarity of the ½-dot).

Section 5.4 describes the operation of the video generation circuitry that displays the above-described character patterns.

5.4 VIDEO GENERATION

Basic Video: The basic video "dots" (1) emanate from the shift register A2-13, page 5) (2) are then delayed by either one full or one-half dot time (A17-5 or 9, respectively) with the desired one being selected (using A18-1,2,3 and A18-4,5,6 along with the two inputs A19-2,4 and output on A19-6), (3) are next complemented if dictated by controls and/or +CURSOR (A21-4,5,6), (4) are then open-collector driven onto a multi-level video point where there is blank, half, and full intensity and, possibly, sync levels (video is driven by A15-4,5,6), and (5) are finally emitter-follower driven onto P2-4 (by Q1, page 5).

SHIFT REGISTER: The character generator's 6 output pattern bits are loaded into the shift register as shown in Figure 5.3. +DC CARRY (A57-15, page 4) causes the load (via A42-11,12,13 to A2-15, page 5) at +CLK rising. This load may be inhibited (at A42-13, page 5) by a number of conditions (at A19-8, 9,10,12,13, page 5). These inhibit conditions are:

(a) control character code (+DRD5 = Ø and +DRD6 = Ø), as detected by A22-1,2,3 which goes to A19-13.

(b) first scan line for a character row (+DOT. A3→Ø = ØØØØ) as detected by A22-8,9,10, A21-11,12,13, and A22-4,5,6 which go to A19-9.

(c) control registers say flash (A31-5 = 1 and A31-9 = 1, page 5) and +4Hz divided-by-2 (A34-5) equals Ø, as detected by A33-3,4,5,6 which goes to A19-10.

(d) tenth scan line for a character row (+DOTA3→Ø = 1ØØ1) as detected by A20-11,12,13 which goes to A19-12.

The above inhibiting conditions (at A19-8, page 5) are also loaded into the flip flop A16-2,6 (page 5) with the +DCCAR pulse. The flip flop's

output clears the shift registers contents during the first dot time. (See Figure 5.5.)

Normally (when allowed to load) the 6 data bits (from D7→Ø of the character generator) are shifted as shown in Figure 5.5. For the 7th dot time a Ø emanates from the shift register (QH, A2-13, page 5). All bits are shifted into the two dot select flip-flops (A17-9,12 and A17-2,5) where one (A17-9,12) is clocked by -CLK (at A17-11), allowing that flip-flop to have the data from the shift register in advance of the other normally clocked flip-flops (A17-2,5). This means that A17-9 has the "advanced" dot and A17-5 has the "normal" dot.

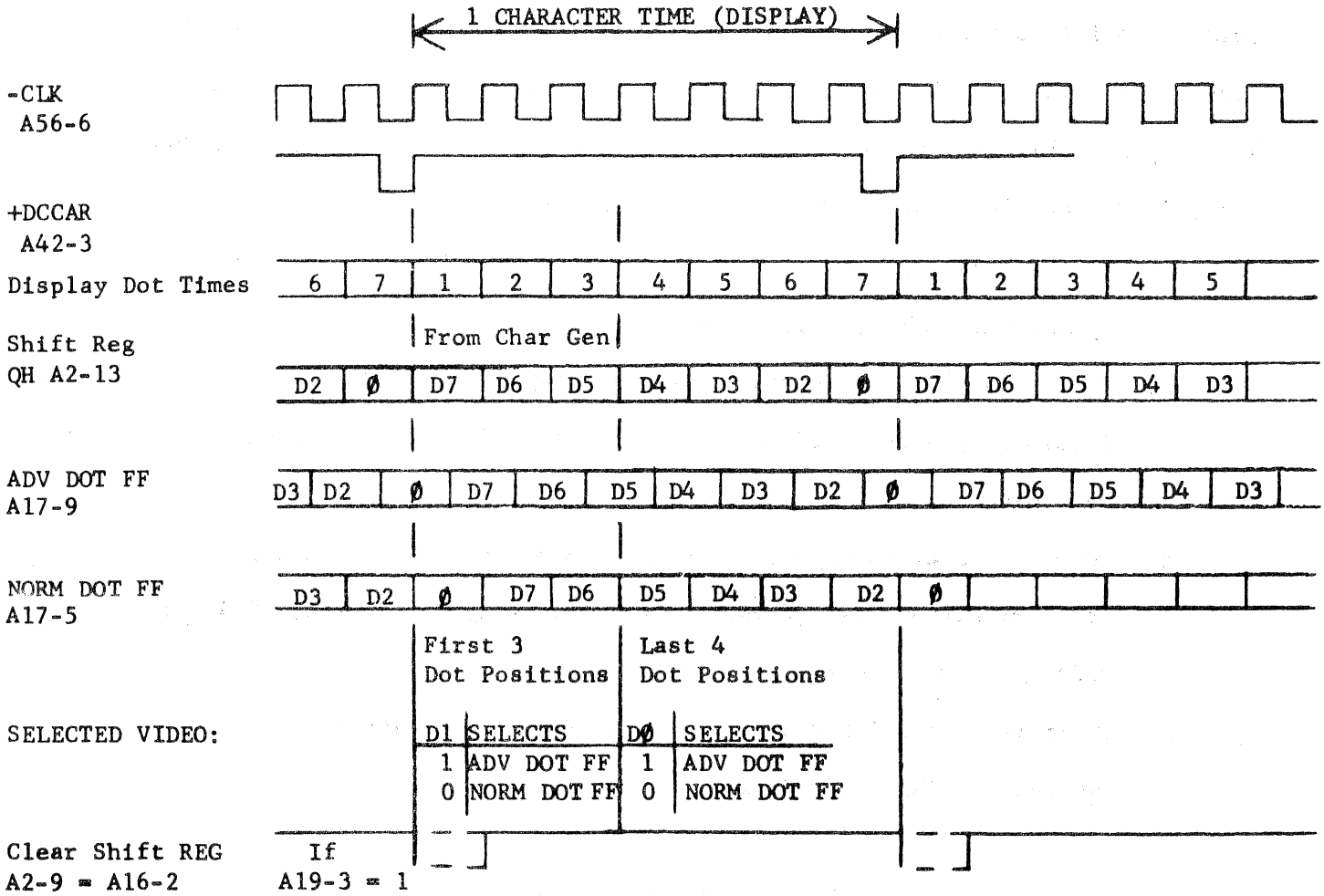


FIGURE 5.5: VIDEO DOT

DISPLAY SIGNAL RELATIONSHIPS (VIDEO, BLANK, CURSOR, HSYNC): The relationships between the various signals that directly effect the display are shown in Figure 5.6. The top portion of the diagram has the relative character positions for the "display RAM", "character generation", and "displaying video" activities. (See Figure 5.3 for more details.) Shown in Figure 5.6 are the first few and last few character positions for a horizontal scan line.

The following signals are controlled by CRT outputs:

(1) RAM Accessing (display RAM address for indicated character)

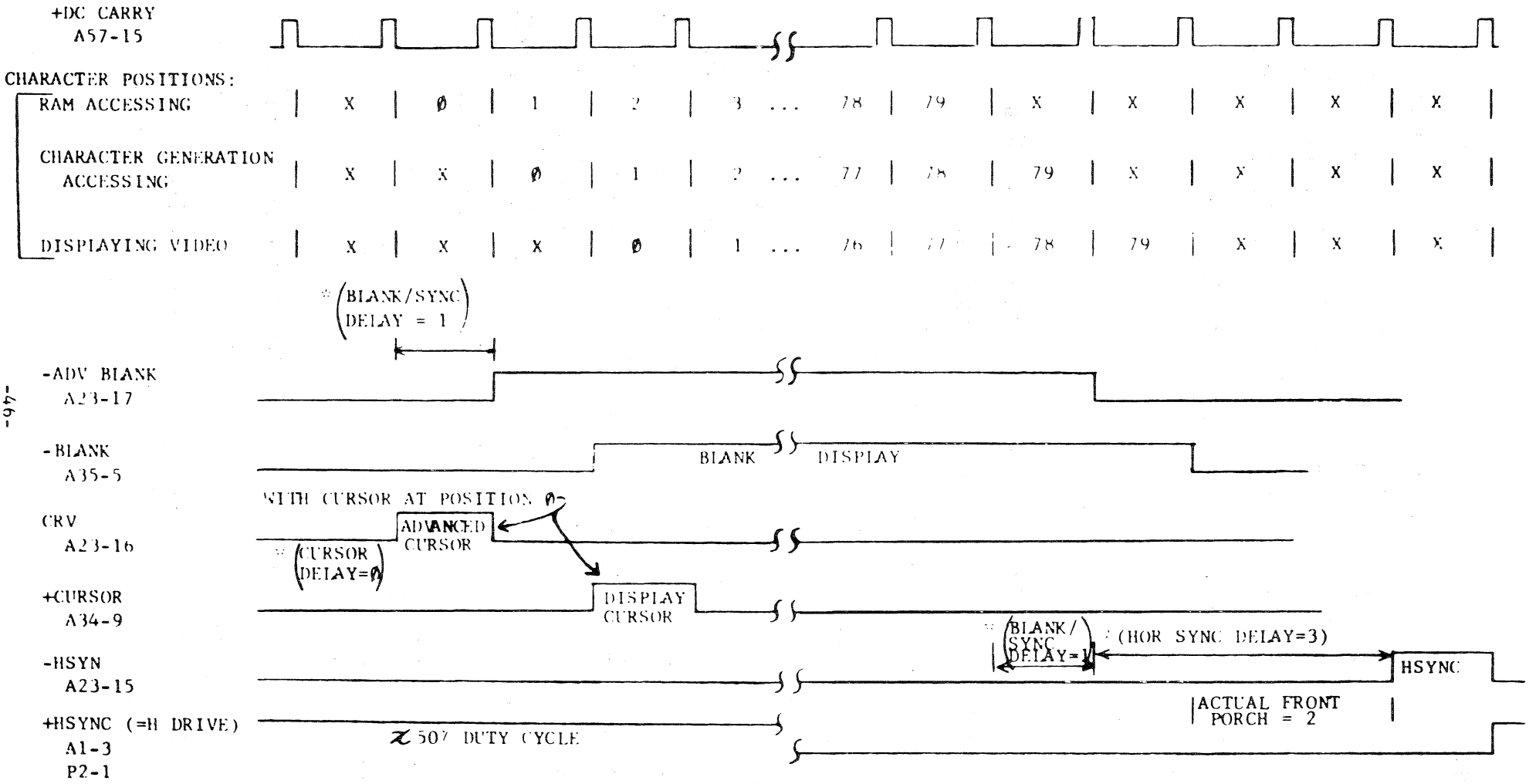
(2) -ADV BLANK (delay by 1 with respect to addresses)

(3) CRV (delayed by Ø with respect to addresses)

(4) HSYN (delayed by 1 with respect to addresses)

The delays are as programmed into the CRT chip, see Section 5.2. -ADV BLANK is delayed one more character time (by A35-2,5, page 4, as clocked by +DCCAR) in order to line it up with displaying video. This +BLANK signal (A35-5) goes through an open collector driver (A14-12,13, page 5) in order to blank the video. ADV BLANK and BLANK are used for addition gating functions as described in other parts of this section. Additionally, -ADVBLANK goes to the CPU's T1 input (A54-39, page 1) to permit synchronization with the video by the CPU for performing accesses to the display RAM without disturbing the display refresh. (See Section 5.3.)

The cursor signal from the CRT Chip (A23-16, page 4) is delayed 2 character times (by A35-9,12 and A34-1,12, clocked by +DCCAR, page 5) to line it up with the video being displayed. The +CURSOR signal complements the normal video signal (using A21-1,2,3 and A21-4,5,6, page 5) including the effect



*See Section 5.2 for CRT programming.
NOTE: See Figure 5.3 for character position details.

FIGURE 5.6: DISPLAYED VIDEO RELATIONSHIPS

of the INVERT VIDEO bit (A28-6 to A21-2) of the control register. Additional gating (at A18-11,12,13, page 5) permits optional (by installing jumper W25) 4 Hz flashing (on-off) of the video at the cursor position. For this option when the cursor is flashing "on" (A18-11=Ø), the Zero-Intensity driver (A15-1,2,3, page 5) is disabled and "on" video is injected into the video signal (at A19-1, page 5). During Zero-Intensity this causes video to be "on" (not because of the injected "on" video but because the Zero-Intensity signal, A32-6, disables the video driver, A15-4, 5,6, through an inverter, A33-1,2,12,13). During other (non-zero) intensities the cursor "on" causes the character position to have all dots "on" because of the injected "on" video. This causes the character's background to change (flash) to the same polarity as the character itself (which is already inverted once or twice by the +CURSOR signal and, possibly, by the INVERT VIDEO control bit).

Horizontal sync (A23-15, page) is programmatically delayed in the CRT Chip by 4 character times (1 for SYNC/BLANK DELAY and 3 for HSYN DELAY, see Section 5.2) from the end of the last RAM address character position. With video being delayed 2 more character times a 2-character "front porch" is provided (see Figure 5.6 and Appendix B). HSYN (A23-15) is inverted (A36-10,11, page 4) to drive a one-shot (A1-2,3) which generates a horizontal drive signal (called +HSYNC) that goes to the video connector (P2-1, page 5). (-HSYNC is also used for other timing (on page 5) as described in the paragraph below that presents the video control register.)

VSYNC (A23-11, page 4), which is inverted twice (A56-12,13 and A56-1,2, page 4) and driven (by A14-10,11, page 5) onto -VSYNC (P2-5), has the timing as described in Section 5.2 and Appendix B. (VSYNC signals are

also used for video control register timing, see below.) -COMPSYNC (A23-10, page 4) is inverted (A15-11,12,13, page 5) and driven (by inverting driver A14-8,9, page 5) onto P2-6. Its main use is to provide the composite sync to the multi-level video signal (by closing switch S2-10,11 and opening switch S2-1,20, page 5). When the switch settings are made then P2-6 provides +TTL VIDEO in addition to a TTL composite sync signal.

HALF-DOT-SHIFT LOGIC: As described in Section 5.3 each scan line of each character can specify a half dot shift characteristic for each the first 3 dot positions and the last 4 dot positions. D1 (from A3-10, page 5) selects the half dot shift for the first 3 dot positions (D1=1 selects the advance dots, D1=Ø selects normal dots. DØ (A3-9) selects the half dot shift for the last 4 dot positions. Section 5.3 shows a portrayal of the 4 possibilities. D1 and DØ are latched into A45-2,5 and A45-12,9 (respectively) by +DCCAR (A42-3 to A45-3 and A45-11) which is the same time as when the shift register is loaded. The outputs of A45-5,6 determine whether the normal or advanced dot is selected. The Q output (A45-5) enables (via A18-4,5,6) the advanced dot (from A17-9). The $\overline{Q}$ output (A17-6) enables (via A18-1,2,3) the normal dot (from A17-5). +DC2=1 and +DCØ=Ø (inverted by A44-12,13, page 5) cause (via A46-3,4,5,6 and A46-8,9, 10,11) the selecting flip-flop A45-2,5) to take on the value of the flip-flop that stored the DØ value A45-9,12). This occurs between the 3rd and 4th dot time (see Figure 5.1) causing the dot shift patterns shown in Figure 5.4. The dot-select gates (A18-4,5,6 and A18-1,2,3) have their outputs OR'd (with other signals at A19-2,4) to form the pre-complemented video signal at A19-6.

IN-STREAM VIDEO CONTROL REGISTER: Six flip-flops implement a 4-bit control register that captures video control information from the display character

stream. As described in Section 5.3 the control information comes from the outputs of the pipeline latch (A4, page 5) and uses up 32 (of the possible 128) character encodings. A control character is denoted by having bits 6 and 5 equal to Ø (+DRD6 and +DRD5, A4-5,2) which is detected by the gate A22-1,2,3, page 5. The output of this gate (A22-3) is inverted (A44-1,2) to yield +CONTROL. The control register flip-flops are clocked by signals that are essentially the same as +DCCAR (see Figures 5.3 and 5.5) but are enabled only under the following conditions:

(1) +CONTROL is true;

(2) valid characters are in the character stream at the pipeline register A4 (which is when the signal -ADVBLANK is high, see Figure 5.6);

(3) the intensity control bits (+DRD3,2) require that +DRD4=1 to be clocked.

These conditions are gated (using A43-12,3, A43-4,5,6, A43-8,9,10, A42-4,5,6, and A42-8,9,10, all on page 5) with +DCCARRY (at A43-5) and -CLK (at A42-4 and A42-10) to generate the clocking signals for the UNDERLINE (+DRDØ) and INVERT VIDEO (+DRD1) bits (as clocked from A42-6) and the INTENSITY bits (+DRD3,2, as clocked from A42-8 which is inverted by A44-10,11, page 5).

CONTROL CODES: BIT 6=Ø, BIT 5=Ø

THEN START UNDERLINE BIT Ø=1

END UNDERLINE BIT Ø=Ø

START INVERSE VIDEO BIT 1=1

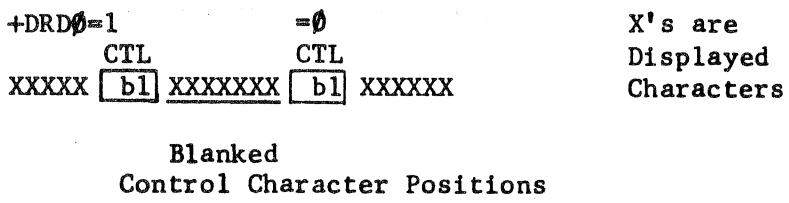
END INVERSE VIDEO BIT 1=Ø

IF ALSO BIT 4=1 THEN

	BIT 3	2
START ZERO INTENSITY	Ø	Ø
START FLASH (2Hz)	1	1

	BIT 3	2
NORMAL	1	Ø
NORMAL	Ø	1

UNDERLINING: Bit Ø of control characters (+DRDØ, A4-9) is clocked (A29-11) into the UNDERLINE flip-flop (A29-9,12, page 5). If +DRDØ = 1, then, to prevent the control character position itself (which is blanked, as described in the "SHIFT-REGISTER" paragraph above) from being underlined, a second flip-flop (A28-9,12) provides a one-character delay. The second flip-flop is clocked by +DCCAR at every character time. If +DRDØ=Ø, then the output of the first flip-flop (A29-9) clears the second immediately (via A28-13), causing the underline to disappear at the beginning of a control character:



The actual underlining (as controlled by A28-9) is gated (at A18-8,9,10, page 5) with +10th Dot Row which indicates the last rastor scan line for a character row (as denoted by A20-11,12,13 and inverted by A80-1,2,3, page 5). The output of the gate (A18-8) forces a video "on" condition (at A19-5). (See also Inter-Scan-Line Storage, below.)

INVERTED VIDEO: Bit 1 of control characters (+DR01, A4-6) are clocked (A29-3) into the INVERTED VIDEO flip-flop (A29-2,5, page 5). As with the UNDERLINE flip-flop pair (described above), the INVERTED VIDEO has two flip-flops (A29-2,5, and A28-2,5) which, when Bit 1=1, delay the effect on the video until the following character, but when Bit 1=Ø they turn off the inverse video immediately (using the second flip-flop's clear,

A28-1). The actual inverting (as controlled by A28-6) is exclusive OR'd with the +CURSOR signal (at A21-1,2,3, page 5) and the video signal (using A21-4,5,6). Thus the video may, in effect, be complemented twice, once by the INVERT VIDEO control and once by the +CURSOR signal. If the flashing cursor option (jumper W25) is not installed then the presence of the cursor at the end of an INVERT VIDEO field will cause ambiguity in visually determining the cursor position on the screen. (See also Inter-Scan-Line Storage, below.)

INTENSITY CONTROLS: When bit 4 (+DRD4, A4-14) of control characters equals 1, then bits 3 and 2 (+DRD3,2, A4-16,15) are clocked (A31-3,11) into the INTENSITY control flip-flops (A31-2,5 and A31-9,12, page 5). These flip-flops affect the intensity immediately when loaded. When bit 3 (A31-5) and bit 2 (A31-9) both equal zero, this is detected (by gating A31-6 and A31-10 at A32-4,5,6, page 5) and causes a driver (A15-1,2,3) to zero the video. (This driver may be disabled at the cursor position at a 4 Hz on-off rate, if the flash cursor option, jumper W25, is installed. See CURSOR, above.) When bit 3 and bit 2 both equal one, this is detected and gated with a 2 Hz square ware (at A33-3,4,5,6, page 5) in order to produce a video flashing (on-off) effect. The gate's output (A33-6) inhibits and clears the dot shift register (via A19-10,8). (See SHIFT REGISTER, above.) Any other combinations of bits 3 and 2 (specifically bit 3,2, = 1,0 or = Ø,1) allow the normal intensity to be used.

INTER-SCAN-LINE STORAGE OF CONTROL REGISTER: The register A30 (page 5) stores the CONTROL REGISTER values at the end of the 80th character at the 10th scan line of a character row. At the beginning of each of the 10 scan

lines of the next character row the values in the storage register are loaded into the control register flip-flops. This allows UNDERLINE, INVERTED VIDEO, and INTENSITY controls to carry over from one character row to the next character row. The storage register (A30) is loaded at the end of the tenth scan line by gating -BLANK, +ADVBLANK, and +10th DOT ROW (all at A33-8,9,10,11, page 5) which, when all equal to 1, define that the 80th character on scan line 10 is being displayed. The gate's output (A33-8) passes through A32-9,8 to provide one of the load enables for the storage register (A30-9). The other load enable (A30-10) is driven true by -10th DOT ROW (A20-11 through A32-11,12,13). In this way the storage register is loaded with the control register bits -BITØ (from A29-8), -BIT 1 (A29-6), -BIT 2 (A31-10, and +BIT 3 (A31-5) into storage register data input 4D, 3D, 2D, and 1D (A30-11,12,13,14), respectively.

Before loading the control register flip-flops at the beginning of each scan line, all flip-flops are set to their initialized condition by the -HSYNC (A36-10, page 4) signal:

UNDERLINE (A29-9) is set to Ø (via A29-13)

INVERT VIDEO (A29-5) is set to Ø (via A29-1)

INTENSITY (bits 3,2 at A31-5,9) is set to 1,Ø (via A31-4,13)

The outputs of the storage register are enabled (A30-2) by the combination of +ADV BLANK and +BLANK (at A20-4,5,6) (except during VSYNC, see below). These outputs go to the 4 control flip-flops causing them to preset or clear in a manner appropriate with the stored bit value. If a stored bit is high at the output then the corresponding flip-flop is not changed because the "initialized state" (see above) is already correct. If a stored bit is low

at the output then the flip-flop is forced to the opposite of the "initialized state". The flip-flops end up in the state indicated by the storage register:

NAME	BIT #	INITIALIZED VALUE	STORAGE REGISTER VALUE	FINAL FLIP-FLOP VALUE
UNDERLINE	Ø	Ø	(= -BITØ) Ø	1
			1	Ø
INVERT VIDEO	1	Ø	(= -BIT1) Ø	1
			1	Ø
INTENSITY	2	Ø	(= -BIT2) Ø	1
	3	1	(= +BIT3) Ø	Ø
			1	1

Figure 5.7 Storage Register Value

Additionally, during vertical blanking, the signal -VSYNC (A36-12, page 4) causes (through A32-8,9,10 and A32-11,12,13) both enables (A30-9,10) of the storage register be driven true. +VSYNC (A36-2) forces the storage register's outputs to be disabled (at A30-1). This causes the control flip-flops to stay in their initialized state as forced by -HSYNC (from A36-10, page 4, to A29-1, A29-13, A31-4, and A31-13, page 5). This also causes the storage register to have the same values. Following VSYNC these values are:

UNDERLINE = Ø

INVERT VIDEO = Ø

INTENSITY = 1,Ø (i.e., NORMAL)

HALF-INTENSITY (="PROTECTED" by firmware): Bit 7 of every character (A4-12, +DRD7, page 5) controls whether or not that character is displayed with half intensity. At the same time the shift register is loaded +DCCAR (A42-3, page 5) loads (A16-11, page 5) +DRD7 (A16-7) in a flip-flop whose output (A16-9) is driven (by A15-8,9,10) through 510 ohms (R9) to the combined video

node. With the driver's output (A15-8) low the combined video is loaded down more, causing the intensity level, if any, to be reduced.

COMBINED VIDEO: The following open-collector drivers make up the combined video signal (A15-6, page 5):

Half intensity	A15-8 through 510 ohm, R9
Zero intensity	A15-3
Video (Dots)	A15-6
BLANK	A14-12
FORCE BLANK	A14-2

+FORCE BLANK's driver (A14-1,2) allows the CPU to blank the screen at any time (to avoid unsightly display effects, for example, during massive display data accesses). The CPU writes a 1 in bit 5 to external data (memory mapped I/O) address 40CH to cause the screen to blank. (See Section 2.4.1.)

For video without sync signals switch S2-1,20 is opened and switch S2-10,11 is closed. Resistors R2 and R3 (510 ohms and 1K ohm) provide the level pullup capability. The emitter-follower implementation of Q1 provides a high input impedance and a low output impedance which drives (through R4, 68 ohms) +VIDEO (P2-4). A convenient ground signal is provided on P2-3.

For composite video (i.e., video with sync signals) switch S2-1,20 is closed and switch S2-10,11 is opened. This puts a 260 ohm resistor (R1) in series with the previous combined video which prevents zero intensity from reaching as low a level at S2-1. Closing S2-1,20 allows composite sync (A14-8) to cause the lowest level in the new video signal. This "TTL" driven video signal is output on P2-6 +TTL VIDEO. As above, the signal is driven by the emitter follower (Q1) to drive +VIDEO (P2-4).

6. COMMUNICATION OPERATION

6.1 Baud Rate Generation

The baud rate frequencies for the computer (P3) and printer (P4) serial communication interfaces are determined by the counters and switches shown on page 6 of the schematics. The input clock is TDC1 (A57-13, page 4), which is an asymmetrical 3.402 MHz signal (see Figure 5.0). The first counter (A73, page 6) divides this by 11 to yield a 309,273 Hz signal (A73-11) suitable for the 19,200 baud rate. Counter A70 and A71 each provide 4 levels of dividing by 2 to yield clocks for 9600 down to 75 baud. Counter A72 divides A70's output by 11 to yield (at A72-11) a clock suitable for 110 baud.

Switch S1 selects the baud rate for the computer (P3) port by enabling one (and only one, as enforced by the user) signal to A74-9 (page 6). (See Section 3's table for switch settings.) Switch S3 does the same for the printer (P4) port by enabling one signal to A74-2. The CPU selects one of these two signals with +SELLPT (A74-1,2,3) the printer port and -SELLPT=1 enables (at A74-8,9,10) the computer port. +SELLPT is controlled by the CPU as bit 4 in memory mapped I/O port 40CH. (See Section 2,4.1.) The selected baud rate results in +BAUD GEN (A47-11,12,13) which goes to the UART (A48-12,40, page 2).

6.2 UART Operation

Details of the UART chip's (A48, page 2) internal operation are given in its specification in Appendix C. Section 2.4.2 presents programmer-level I/O information.

UART I/O Interface: Three I/O ports (2 read and 1 write) are used to interface the CPU to the UART. The data write port (address 408-H) is enabled by address decoder output 2 (A58-3, page 1) which goes to the UART's - DS (A48-23, page 2). When pulsed (as per Section 2) on this input the UART receives a byte on CPU data lines (+DB7→Ø) which are connected to UART inputs DB8→Ø (page 2). The data read pulse, -RDE (address 408H), from the decoder (A58-6) enables (RDE, A48-4) the UART's read outputs (RD8→L) onto the CPU data bus (+DB7→Ø, respectively). -RDE also pulsed the UART's reset Data available input (A48-18). The status word enable read pulse, -SWE (address 404H), from the decoder (A58-7) enables (48-10) four status bits onto the CPU data bus:

FE, Frame Error,	from A48-14 to +DB3
PE, Parity Error,	from A48-13 to +DB2
TBMT, Transmit Buffer Empty,	from A48-22 to +DB1
DTA, Data Available,	from A48-19 to +DBØ.

UART SWITCH CONTROLS: Five switches provide operational control over the UART, see Appendix C and Section 3:

S2-5, 16	Parity	A48-35
S2-6, 15	Stop Bits	A48-36
S2-7, 14	Number of Bits	A48-38
S2-8, 13	" " "	A48-37
S2-9, 12	ODD/EVEN PARITY	A48-39

The -HALF DUPLEX signal goes directly into the CPU (A54-38, page 18, from switch S2-3,18). It is not implemented with the UART, but by the firmware.

UART RESET: The CPU resets the UART by pulsing the -PROG pin (A54-25, page 1) which is inverted (by A67-1,2, page 1) yielding +RESETUART to drive the UART's MR input (A48-21, page 2).

UART SERIAL OPERATION: As described in Appendix C the UART uses the receive and transmit clocks, (A48-17,40) at 16 times the baud rate, to transmit data (A48-25) and receive data (A48-20). The clock is as selected in the BAUD RATE GENERATION logic (+BAUDGEN, A74-11, page 6; see Section 6.1).

6.3 SERIAL INTERFACES

The computer and printer serial interfaces can be either RS232C-type levels or current loop. The serial data is transmitted as both RS232 and current loop (for the selected interface). Two switches must be set to select which type of data will be received on the computer port:

Receive RS232C on P3-3 -- Close S5-6,9

Receive Current Loop on P3-12,24 -- Close S5-7,8

(only one switch should be closed).

6.3.1 RS232 Operation:

COMPUTER PORT, P3:

Receive Data is input on P3-3 (by A60-12, page 2) and passed through switch S5-6,9 to the UART (A48-20). (See also Section 6.3.3 for P6).

Clear to send is input on P3-5 (by A60-8,10) yielding -CTS which the CPU can input on TØ (A54-1, page 1). (See also Section 6.3.3.)

A "Data Carrier Ready" signal can be selectively input on P3-6 (as switched by S5-1,14) or on P3-8 (as switched by S5-2,13). With both switches open 3.3KΩ resistor (R32) pulls the input to +12V, the true condition. The output of the RS232 receiver (A60-11, page 2) becomes -DCR which the CPU can read on port 2 bit 5 (45-36, page 1). (See also Section 6.3.3.)

Transmit Data for the computer RS232 port is driven to P3-2, TXD, (by A59-4,5,6, page 2). The input to the driver (A59-4,5) is enabled (at A61-4,5,6) by the control signal -SELLPT (A62-4 to A61-5) which, before inversion (by A62-3,4), is +SELLPT as output by the CPU on bit 4 of memory mapped I/O port 40CH (See Section 2.4.1). When -SELLPT disables the transmit port (-SELLPT low) the output (at A59-6, P3-2) is kept low (defined by the RS232C specification as the "OFF", marking condition, or binary 1 condition.) -BREAK (A47-10, page 1, CPU output to 40CH bit 3) when true (low) can force (via A61-11,12,13, page 2) the transmit data to the spacing condition (RS232 is positive, defined as "ON") if enabled (at A61-4,5,6) by -SELLPT being high. The data signal itself (at A61-12) comes from the UART's -TXD output (A48-25). (See also Section 6.3.3 for P6.)

The CPU controlled -RQS signal (A47-7, page 1, CPU output to 40CH bit 2) is the source for driving (using A59-2,3, page 2) the RTS signal at P3-4. By closing switch S5-3,12 this driver will also drive DTR at P3-20. Alternatively, DTR could be pulled permanently to the "ON" (positive) state by closing switch S5-4,11 (and leaving S5-3,12 open).

Pin P3-7 is ground on the RS232 computer port.

PRINTER PORT, P4:

The RS232 printer port has no serial data receive capability. However +PRTRDY (P4-20, page 2) is received (by A60-4,6) and sent to the CPU as -PRTRDY (A60-6, page 2) on CPU port 2 bit 6 (A54-37, page 1). If P4-20 is left disconnected, then a 3.3KΩ resistor (R18) pulls the signal to the ON state.

Transmit Data for the printer RS232 port is driven to P4-3, PRT DATA (by A59-8,9,10, page 2). The input to the driver (A59-9,10) is enabled (at A61-8,9,10) by the control signal +SELLPT (A47-12, page 1) which is output by the CPU on bit 4 of output location 40CH (See Section 2.4.1). The transmit data is otherwise controlled by +SELLPT and -BREAK in the same manner as described above (for -SELLPT and -BREAK) for the computer RS232 transmit data, above. The data, as above, originates from the UART's -TXD (A48-25).

The RS232 printer port also drives (with A59-11,12,13) P4-6 (by installing jumper W12) and/or P4-8 (by installing jumper W13) with the CPU controlled signal -RQS (A47-7, page 1, CPU output to 40CH bit 2).

Pin P4-7 is ground on the RS232 printer port.

6.3.2 Current Loop Operation

COMPUTER PORT, P3: The computer has both transmit and receive current loop interfaces. The receive circuit uses an opto isolator (4N37 at A6-3, page 2) to receive a current loop with current (conventional) entering at P3-12 (RXD1) and leaving at P3-24 (RXD2). Adiode (D2) provide a reverse current path. The opto-isolator's output (A63-5) feed an inverted (A62-10,11), the

output of which (when passed by a closed S5-7,8 switch) provide the UART with serial input data (A48-20). (Note that the RS232 switch S5-6,9 should be open during current loop operation). The current loop receiver circuit is very low impedance such that the equipment driving this input must limit the current, to not more than 40 mA (with a 20 mA minimum).

The current loop driver for the computer port is opto-isolated (A65,4N33) also. Its source (via A62-5,6) is the same as what is input to the RS232 driver, causing it to parallel that pin's actions (See Section 6.3.1). A completely isolated output is provided at P3-25 (TXD1) and P3-13 if jumpers W14 and W16 are installed (and jumpers W15, W17, and W6, and resistor R28 are not installed). Alternatively by installing R28, W6, W15, and W17, a current (limited by R28) can be driven into P3-25 (TXD1) and returned to ground at P3-13 (TXD2).

7. KEYBOARD OPERATION

The keyboard matrix is driven on connector P1 (pins 8 to 15) by the CPU with bits 7 to Ø of port 1 (A54-34 to 27), page 1). The twelve inputs are received by multiplexers (with all of A69 and A68-9 to 15, and 2, page 1) to be received by the CPU via the four memory-mapped input locations 4ØC, 4ØD, 4ØE, and 4ØF (Hex) as described in Section 2.4.3. This is done using the 4ØC decoder output KBRD (A58-9, page 1) and +A1 and +AØ (at A69-2,14 and A68-2,14), causing the multiplexers to output data on +DBØ (A69-9), +DB1 (A69-7), +DB5 (A68-9). Additionally for all addresses 4ØC to 4ØF separate switches from the keyboard are input on the following bits:

+DB2	P1-5	FUNC	(using A76-11,12)
+DB3	P1-6	CTL	(using A76-13,14)
+DB4	P1-4	SHFT	(using A76-2,3)
+DB5	P1-3	ALPHA	(using A76-4,5)

See also Section 2.4.3 for CPU interface usage and Appendix C for the standard keyboard matrix expected on the interface.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
1	1	1	1	1	1					C2	Cap DIP Mica 10pf 100D03	2024100
2	3	3	3	3	3					C3,6,7	Cap R/L 22uf 15V	2025700
3	1	1	1	1	1					C1	Cap R/L 1uf 15V	2027901
4	47	47	47	47	47					unmarked	Cap C/D .01uf 20% 16V	2028700
5	1	4	1	1	1					C10	Cap C/D .01uf 10% 50V Y5P	2028900
6	2	2	0	0	2					C11,12	Cap C/D 330pf 50V 20%	2029100
7	1	1	1	1	1					A42	IC 74S00	2024000
8	5	5	5	5	5					A18,20,40,61.74	IC 74LS00	2024200
9	1	1	1	1	1					A15	IC 74LS03	2024400
10	1	1	1	1	1					A55	IC 74S04	2024600
11	5	5	5	5	5					A36,38,44,62,67	IC 74LS04	2024800
12	1	1	1	1	1					A14	IC 74LS05	2025000
13	2	2	2	2	2					A32,43	IC 74LS08	2025200
14	2	2	2	2	2					A33,46	IC 74LS10	2025400
15	1	1	1	1	1					A19	IC 74LS20	2025600
16	3	3	3	3	3					A22,39,66	IC 74LS32	2025800
17	1	1	1	1	1					A58	IC 74LS42	2026000
18	1	1	1	1	1					A37	IC 74LS51	2026200
19	1	1	1	1	1					A17	IC 74S74	2026400
20	8	8	7	8	8					A16,28,29,31,34,	IC 74LS74	2026600
										35,45,77		

NOTES:

TITLE
CONTROL BOARD, TVI-912/920 TERMINAL

DATE
02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
21	1	1	1	1	1					A21	IC 74LS86	2026800
22	1	1	1	1	1					A56	IC 74LS109	2027000
23	1	1			1					A27	IC 74LS139	2027200
24	4	4	3	4	4					A24,25,26,78	IC 74LS157	2027400
25	5	5	5	5	5					A57,70-73	IC 74LS163	2027600
26	1	1	1	1	1					A2	IC 74LS166	2027800
27	1	1	1	1	1					A30	IC 74LS173	2028000
28	2	2	2	2	2					A41,47	IC 74LS174	2028200
29	2	2	2	2	2					A68,69	IC 75LS253	2028400
30	1	1	1	1	1					A76	IC 74LS367	2028600
31	1	1	1	1	1					A51	IC 74LS373	2028800
32	1	1	1	1	1					A4	IC 74LS374	2029000
33	1	1	1	1	1					A59	IC 75188N	2029200
34	1	1	1	1	1					A60	IC 75189AN	2029400
35	1	1	0	0	1					A65	IC H11G3	2034200
36	1	1	1	1	1					A63	IC TIL117, 4N37	2029300
37	1	1	1	1	1					A3	IC 2316 ROM A3-2	2034600
38	1	1	1	1	1					A1	IC NE555	2030200
39	1	1	1	1	1					A13	IC DP8304	2030400
40	2	2	2	2	2					A52,53	IC AMD2111-4A	2030600
41	1	1	1	1	1					A48	IC 2502, AY-5-1013A	2030800

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
42	1	1	1	1	1					A23	IC 5027,5037,TMS9927	2031000
43	1	1	1	1	1					A54	IC Microprocessor P8035	2031200
44	4	4	4	4	4					A6,8,10,12	IC TMS4045-25NL, 2114 300NS	2035800
45			(4)	(4)	(4)					A5,7,9,11	IC TMS 4045 Option-2nd page	
46			0	1	1					A49B	IC 8332A 32K ROM A49B	2032600
47			0	1	1					A49C	IC 8332A 32K ROM A49C	2032600
48			(1)	0	0					A49R	IC 2316 16K ROM A49R	2032200
49			(1)	0	0					A50R	IC 2316 16K ROM A50R	2032400
50	1	1									IC A49C1	2034000
51	1	1	1	1	1					S5	Dip Switch 7 Pos Top	2174200
52	1	1	(1)	1	1					S3	Dip Switch 10 Pos Top	2181000
53	2	2	2	2	2					S1,2	Dip Switch 10 Pos Side	2096800
54	2	2	(2)	2	2					P3,4	Connector RS232 R/A	2097800
55	4	4	4	4	4					XA5,7,9,11	Socket IC 18 Pin	2098400
56			1	1	1					XA49	Socket IC 24 Pin	2098401
57	3	3	1	1	1					XA50	Socket IC 24 Pin	2098401
58	3	3	2	2	2					XA23,54	Socket IC 40 Pin	2098402
59	1	1	0	0	1					XS4	Socket IC 14 Pin	2098403
60	1	1	1	1	1					X1	Cry 23.814 MHz Fundamental	2098600
61	1	1	1	1	1					P7	Plug 2 Pin	2098501
62	2	2	2	2	2					P2,5	Plug 5 Pin	2098706

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
63	1	1	1	1	1					P1	Plug 26 Pin	2098701
64	2	2	2	2	2					R4,31	Res C/F 68 Ohm 5% 1/4W	2051100
65	1	1	1	1	1					R22	Res C/F 180 Ohm 5% 1/4W	2053300
66	2	2	2	2	2					R1,19	Res C/F 270 Ohm 5% 1/4W	2051300
67	3	3	4	4	4					R11,20,29,30	Res C/F 330 Ohm 5% 1/4W	2051500
68	1	1	1	1	1					R13	Res C/F 470 Ohm 5% 1/4W	2051700
69	2	2	3	3	3					R2,14,25	Res C/F 510 Ohm 5% 1/4W	2051900
70	2	2	1	1	1					R9	Res C/F 750 Ohm 5% 1/4W	2031700
71	6	6	6	6	6					R3,5,8,10,15,16	Res C/F 1K Ohm 5% 1/4W	2052100
72			1	0	0					R34	Res C/F 1K Ohm 5% 1/4W	2052100
73	2	2	0	0	2					R41,42	Res C/F 1K Ohm 5% 1/4W	2052100
74	1	1	1	1	1					R7	Res C/F 1.2K Ohm 5% 1/4W	2031900
75	1	1	1	1	1					R12	Res C/F 1.8K Ohm 5% 1/4W	2052300
76			1	1	1					R17	Res C/F 3.3K Ohm 5% 1/4W	2052700
77	2	2	3	3	0					R18,32,33	Res C/F 3.3K Ohm 5% 1/4W	2052700
78	1	1	1	1	1					R6	Res C/F 4.7K Ohm 5% 1/4W	2053100
79	5	5	0	0	5					R36-40	Res C/F 4.7K Ohm 5% 1/4W	2053100
80		1	0	0	1					R23	Res C/F 51K Ohm 5% 1/4W	2032300
81	1									R23		2032500
82			1	1	0					R23	Res C/F 1M Ohm 5% 1/4W	2031500
83	5	5	4	4	4					RP1,2,4,6	Res Pack 1K Ohm	2040500

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

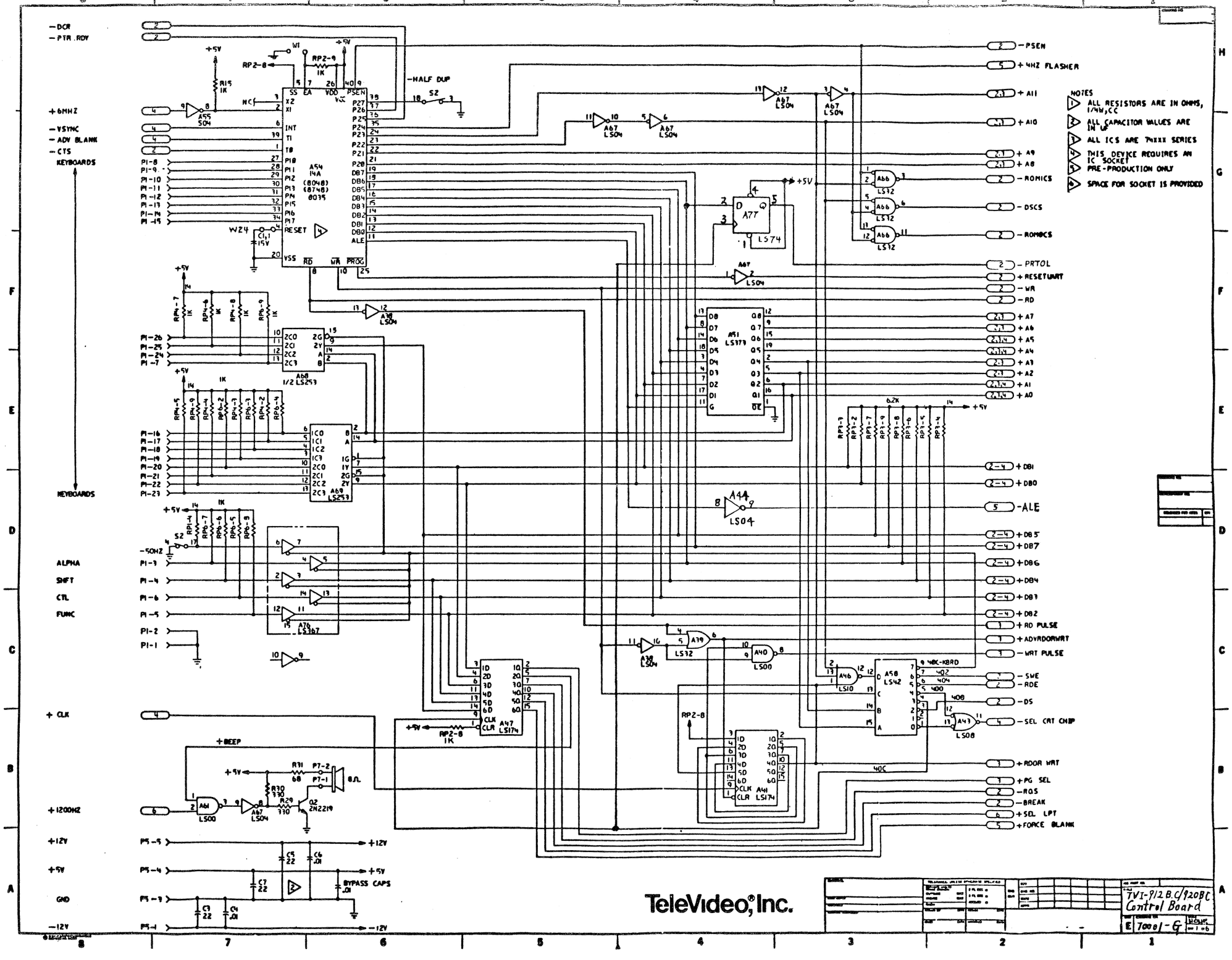
ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
84	1	1	0	1	1					RP3	Res Pack 6.2K Ohm	2040700
85		1								R43	Res C/F 10K Ohm 5% 1/4W	2033300
86	2	2	2	2	2					Q1,2	TR 2N4401	2045500
87	3	3	3	3	3					D1,2,3	Diode 1N914	2047500
88		1									P6KE15A Diode	2047900

NOTES:

TITLE CONTROL BOARD, TVI-912/920 TERMINAL

DATE 2-1-83

TeleVideo Systems, Inc.


-DCR
-PTR .RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
KEYBOARDS
ALPHA
SHIFT
CTL
FUNC
+CLK
+1200HZ
+12V
+5V
GND
-12V
-50HZ
+BEEP
-HALF DUP
A54 14A (8048) (8748) 8035
A51 LS379
A77 LS74
A67 LS04
A68 1/2 LS253
A69 LS253
A70 LS367
A47 LS174
A44 LS04
A66 LS00
A39 LS32
A40 LS00
A46 LS10
A58 LS42
A43 LS08
A66 LS32
2N2219
-PSEN
+4MZ FLASHER
+A11
+A10
+A9
+A8
-ROMCS
-DSCS
-ROMOCS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CRT CHIP
+RDOR WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
NOTES
ALL RESISTORS ARE IN OHMS, 1/4W,CC
ALL CAPACITOR VALUES ARE IN uF
ALL ICS ARE 74xxx SERIES
THIS DEVICE REQUIRES AN IC SOCKET
PRE-PRODUCTION ONLY
SPACE FOR SOCKET IS PROVIDED
BYPASS CAPS .01
TeleVideo, Inc.
TVI-912B,C/920B,C Control Board
E 7008I-G

+A11
-ROMICS
-PSEN
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
-ROMSCS
-PRTDL
-RD
-WR
-DSCS
TELEPHONE INTERFACE P8-1 P8-6 P8-7 P8-8 → P6-11 P6-12 P6-13 P6-14
-SWE
-DS
-RDE
+BAUD GEN
+RESETUART
RCVD(RS232) P3-3 P6-5 P6-6
RXDI(TTY) P3-12
RXD2(TTY) P3-24
+SEL LPT
-BREAK
-RQS
CTS(RS232) P3-5 P6-9 P6-10
DSR(RS232) P3-6
DCD(RS232) P3-8
+PRTRDY(RS232) P4-20
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
-SELLPT
-CTS
-DCR
-PRT DY
P3-25 TXDI(TTY)
P3-17 TXD2(TTY)
P3-2 TXD(RS232) P6-4
P4-3 PRT DATA(RS232)
P3-4 RTS(RS232) P6-8
P3-20 DTR(RS232)
P4-8 TERM RDY
P4-6 TERM RDY(RS232)
P3-7 TELEPHONE INTERFACE P4-7
(NOT USED)
A49 2716E 8316E (2716)
A50 2716E 8316E (2716)
A52 8111A OR (2111A)
A53 8111A OR (2111A)
A68 IC3 IC2 IC1 IC0 LS253
A78 LS157
A69 TIL117
A60 75189
A62 LS04
A61 LS00
A59 75188
A48 COM2502/M
R37 1K +5V
S2
S4
RP5-2
RP1-8 RP2-7 RP3-6 RP4-5 RP2-8
R20 3.3K
R19 260
R32 3.3K
R18 3.3K
R17 3.3K
R22 180
R28 100 (OPT)
R29 1M
R25 470
D2 1N914
D3 1N914
W8 W9 W22 W23 W34 W14 W15 W16 W17 W18 W12
S5
+5V +12V -12V
TeleVideo, Inc.
E 7001-G

DISPLAY RAM ADDRESS

+ RAMA9
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A9
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

A27 LS139
-CS3
-CS2
-CS1
-CS0

+ PG SEL

+5V
4.7K
A21 LS86

A13 DP8304
B⇔A
T⇔R
DIR T/R
EN

+ D87
+ D80
+ RD PULSE

+ RD OR WRT
+ A11

A40 LS00
A39 LS32

+ ADV RD OR WRT
- WRT PULSE

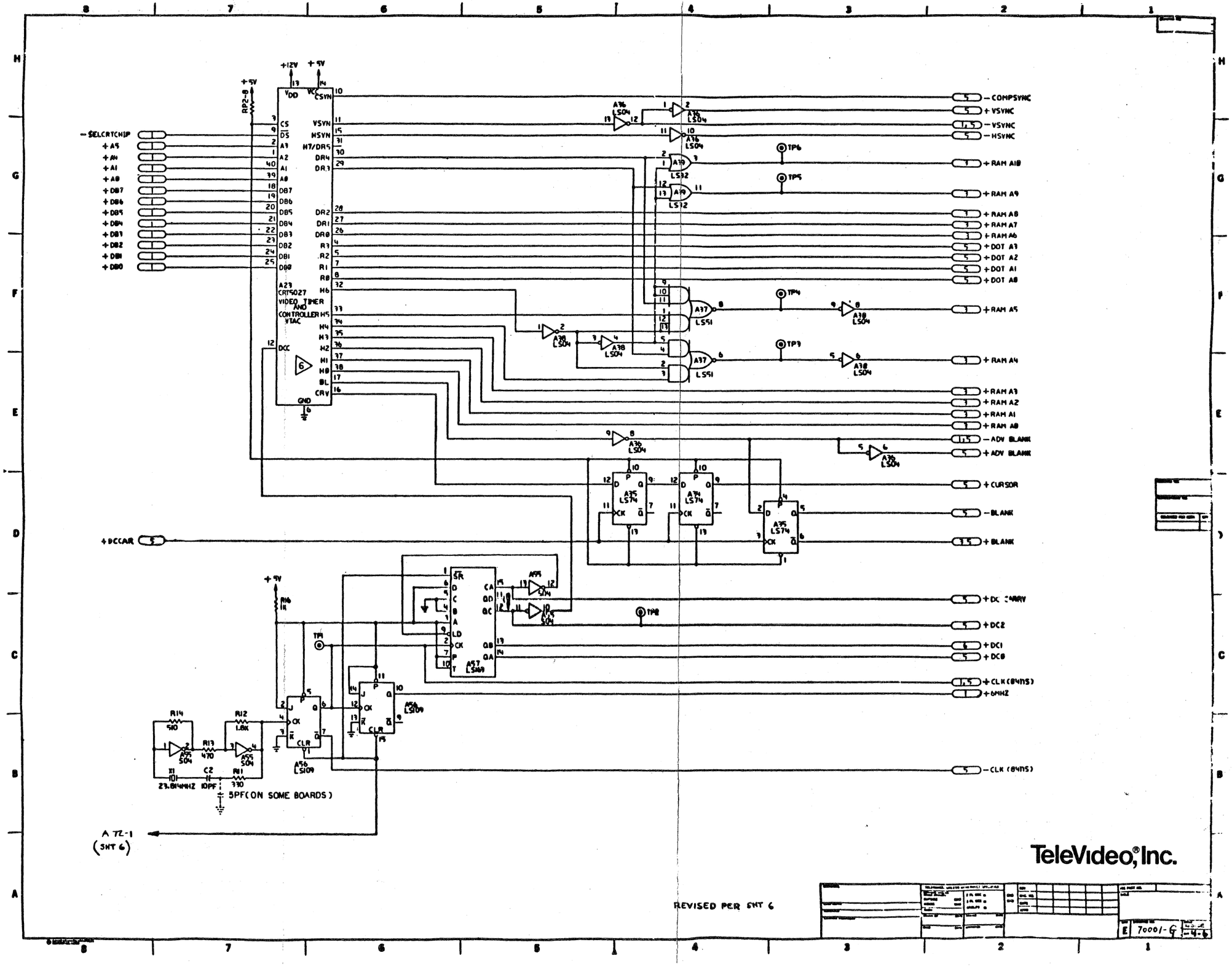
2114-3
OPT

+ DISPDATA 7
+ DISPDATA 0
- CPACC

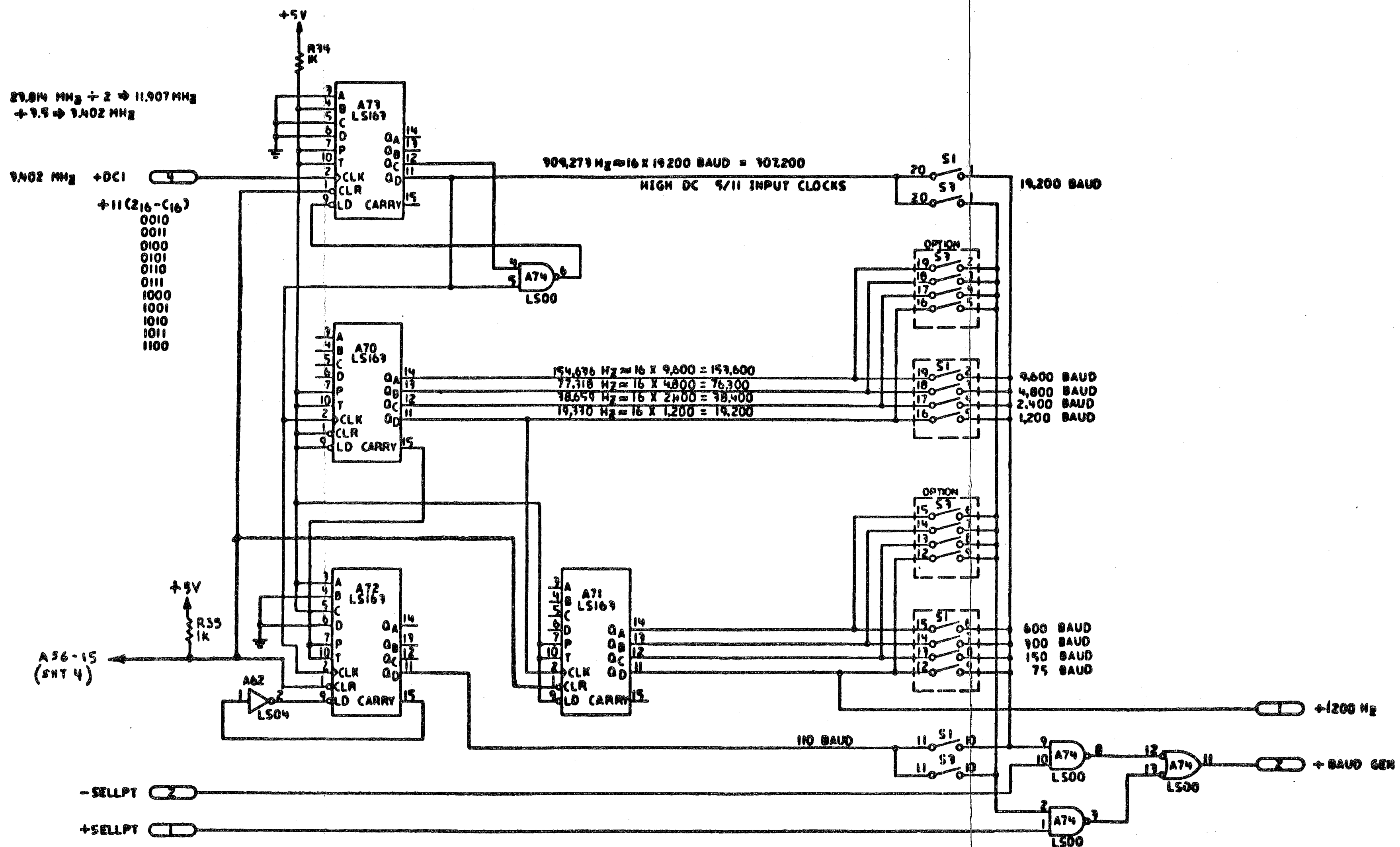
REVISED PER SHEET 6

TeleVideo, Inc.

E 7000/-G -3-6


+12V
+5V
RP2-8
VDD
VCC
CRT5027
VIDEO TIMING AND CONTROLLER
VTAC
GND
CSYN
VSYN
HSYN
H7/DR5
DR4
DR3
DR2
DR1
DR0
R3
R2
R1
R0
H6
H5
H4
H3
H2
H1
H0
BL
CRV
DCC
CS
DS
A1
A2
A1
A0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
-SELCRTCHIP
+A5
+A4
+A3
+A2
+A1
+A0
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
-COMPSYNC
+VSYNC
-VSYNC
-HSYNC
+RAM A10
+RAM A9
+RAM A8
+RAM A7
+RAM A6
+DOT A3
+DOT A2
+DOT A1
+DOT A0
+RAM A5
+RAM A4
+RAM A3
+RAM A2
+RAM A1
+RAM A0
-ADV BLANK
+ADV BLANK
+CURSOR
-BLANK
+BLANK
+DCCARR
+DC CARRY
+DC2
+DC1
+DC0
+CLK (84MHZ)
+6MHZ
-CLK (84MHZ)
TP6
TP5
TP4
TP3
TP2
TP1
A39 LS32
A37 LS51
A35 LS74
A34 LS74
A35 LS74
A57 LS169
A56 LS109
A55 LS04
A36 LS04
A38 LS04
R14 510
R12 1.8K
R13 470
R1 330
C2 10PF
X1 23.814MHZ
5PF(ON SOME BOARDS)
A 72-1 (SHT 6)
REVISED PER SHT 6
TeleVideo, Inc.
E
7000/-6

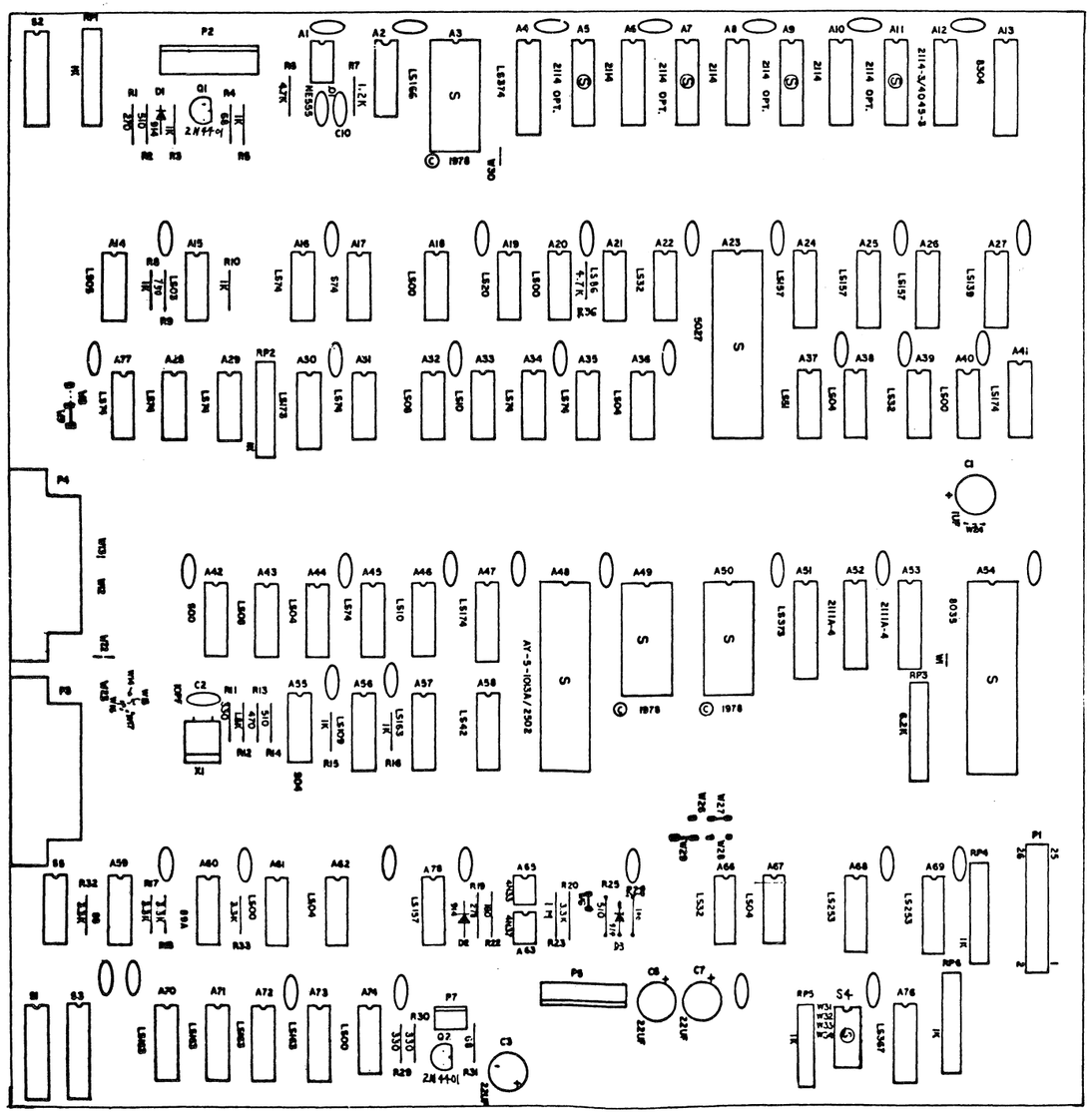
+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+5V
+DC0
-ALE
-CPACC
+DC2
+DISP DATA 7
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCAR
"2716" W30
LOW
+DRD0
+DRD1
+DRD2
+DRD3
+DRD4
+DRD5
+DRD6
+DRD7
2716E
UNDERLINE
INVERT VIDEO
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC
A62 LS04
A14 LS05 (O.C.)
A44 LS04
A55 S04
TeleVideo, Inc.



BAUD RATE GENERATION

TeleVideo®, Inc.

E 70001-G



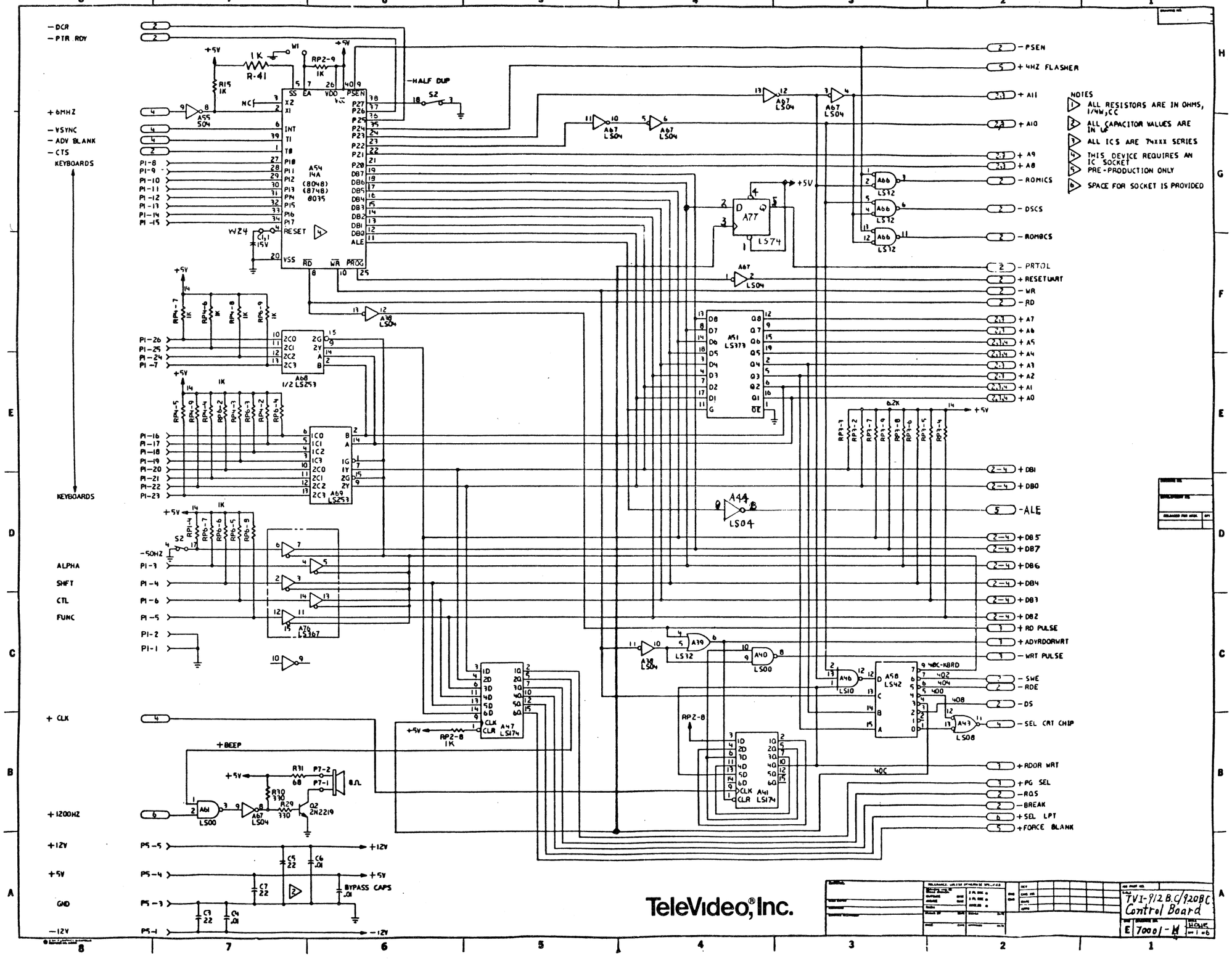
Note

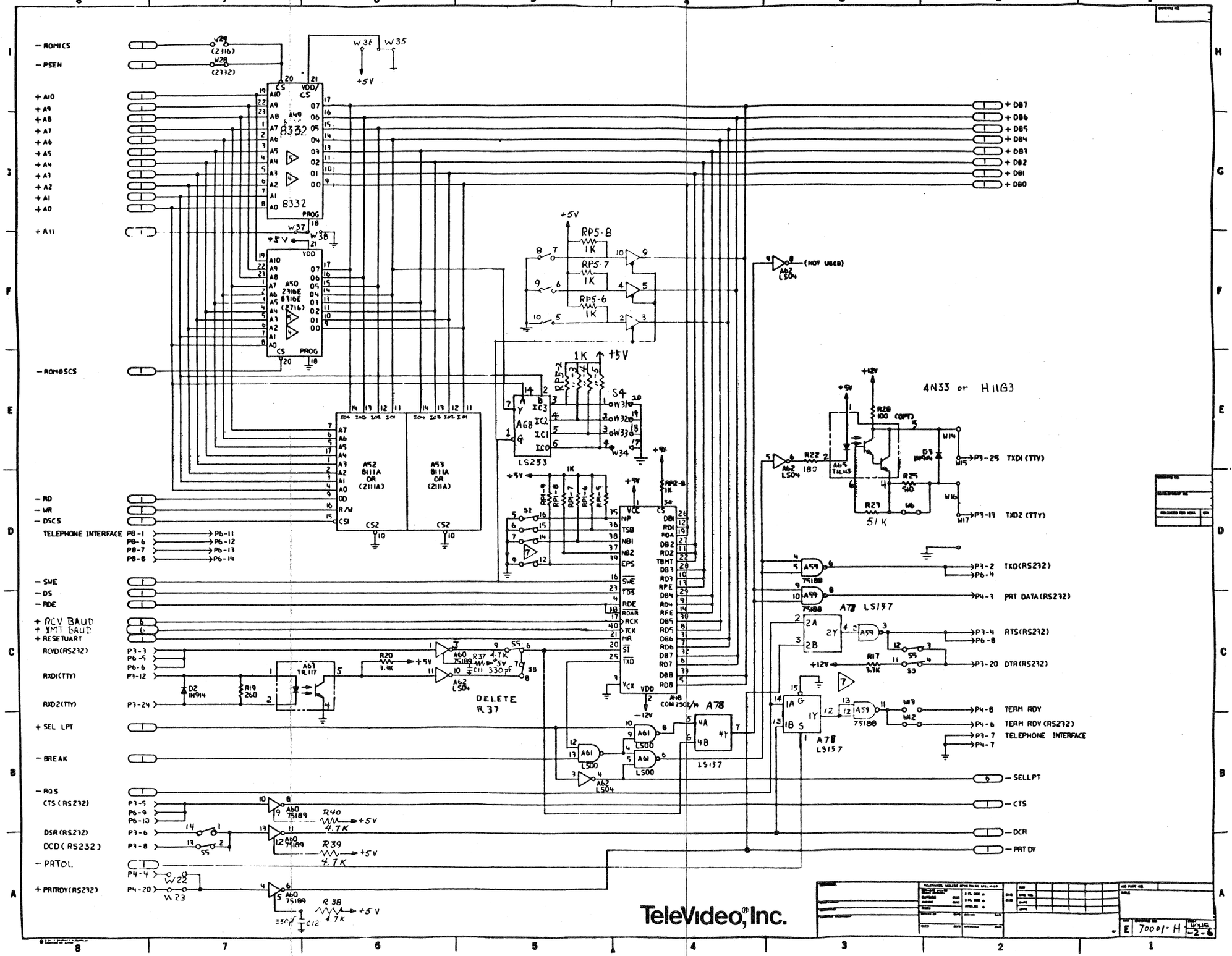
1. ⓢ shows sockets only are mounted at those locations. A5. A7. A9, A11 and S4.
2. S shows chips are mounted on socket at A3. A23. A49. A50 and A54.
3. For 2nd page memory option, add 2114 chips at A5. A7. A9 and A11.

12-72

TeleVideo, Inc.
3190 Coronado Dr. Santa Clara, CA 95051

TOLERANCES (UNLESS OTHERWISE NOTED)	REVISIONS			ASSEMBLY DRAWING		
DECIMAL ±	NO	DATE	BY	TVI-912 B.C/920 B.C CONTROL BOARD		
FRACTIONAL ±	1			DRAWN BY	SCALE	MATERIAL
ANGULAR ±	2			CHK'D	DATE	DRAWING NO
	3			TRACED	APP'D	70001-G
	4					
	5					


-DCR
-PTR RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
ALPHA
SHFT
CTL
FUNC
-50HZ
+CLK
+1200HZ
+12V
+5V
GND
-12V
+BEEP
-HALF DUP
1K
R-41
RP2-9
R15
S2
S4
W1
W24
C1,1
*15V
A54
14A
(8048)
(8748)
8035
SS EA VDD PSEN
X2 X1
INT TI T0
P10 P11 P12 P13 P14 P15 P16 P17
RESET
VSS RD WR PROG
P27 P26 P25 P24 P23 P22 P21 P20
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 ALE
A55 S04
A67 LS04
A68 1/2 LS253
A69 LS253
A76 LS367
A78 LS04
A77 LS74
A81 LS373
A44 LS04
A39 LS32
A40 LS00
A41 LS174
A46 LS10
A58 LS42
A43 LS08
A64 LS00
A66 LS32
A47 LS174
RP2-8 1K
R31 68
R30 330
R29 330
Q2 2N2219
8Ω
C5 22
C6 .01
C7 22
C9 22
C4 .01
BYPASS CAPS .01
6.2K
-PSEN
+4HZ FLASHER
+A11
+A10
+A9
+A8
-ROM1CS
-DSCS
-ROM0CS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CRT CHIP
+RDOR WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
40C
40B-KBRD
402
404
400
408
NOTES
1. ALL RESISTORS ARE IN OHMS, 1/4W, CC
2. ALL CAPACITOR VALUES ARE IN uF
3. ALL ICS ARE 74xxx SERIES
4. THIS DEVICE REQUIRES AN IC SOCKET
5. PRE-PRODUCTION ONLY
6. SPACE FOR SOCKET IS PROVIDED
TeleVideo, Inc.
TVI-912 B,C/920B,C
Control Board
E 7000-H
SCALE: NONE
SHT 1 of 6


-ROMICS
-PSEN
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+A11
-ROMOSCS
-RD
-WR
-DSCS
TELEPHONE INTERFACE P8-1 → P6-11
P8-6 → P6-12
P8-7 → P6-13
P8-8 → P6-14
-SWE
-DS
-RDE
+RCV BAUD
+XMT BAUD
+RESETUART
RCVD(RS232) P3-3 P6-5 P6-6
RXDI(TTY) P3-12
RXD2(TTY) P3-24
+SEL LPT
-BREAK
-RQS
CTS(RS232) P3-5 P6-9 P6-10
DSR(RS232) P3-6
DCD(RS232) P3-8
-PRTDL
P4-4
+PRTRDY(RS232) P4-20
W22
W23
W28 (2732)
W29 (2716)
W36
W35
+5V
W37
W38
A49 8332
A50 2716E 8316E (2716)
A52 8111A OR (2111A)
A53 8111A OR (2111A)
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
RP5-8 1K
RP5-7 1K
RP5-6 1K
RP5-2 1K
RP4-9 1K
RP4-8 1K
RP4-7 1K
RP4-6 1K
RP4-5 1K
RP2-8 1K
A68 LS253
A78 CDN2502/N
A78 LS157
A60 75189
A62 LS04
A63 TIL117
A61 LS00
A59 75188
A69 TIL113
D2 IN914
D3 IN4744
R19 260
R20 3.9K
R37 4.7K
C11 330pF
C12 330pF
R40 4.7K
R39 4.7K
R38 4.7K
R22 180
R23 51K
R25 510
R28 100 (OPT)
R17 3.3K
DELETE R37
4N33 or H11G3
(NOT USED)
P3-25 TXDI (TTY)
P3-13 TXD2 (TTY)
P3-2 TXD(RS232)
P6-4
P4-3 PRT DATA(RS232)
P3-4 RTS(RS232)
P6-8
P3-20 DTR(RS232)
P4-8 TERM RDY
P4-6 TERM RDY(RS232)
P3-7 TELEPHONE INTERFACE
P4-7
-SELLPT
-CTS
-DCR
-PRTDY
TeleVideo, Inc.
E 70001-H

DISPLAY RAM ADDRESS

+ RAMA13
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A13
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

+ PG SEL
A27 LS139
-CS3
-CS2
-CS1
-CS0

+5V
R36 4.7K
A21 LS86

+ DB7
6
5
4
3
2
1
+ DB0
+ RD PULSE
A13 DP8304 B⇔A T⇔R DIR T/R EN

+ RD OR WRT
+ A11
A40 LS00
A40 LS00
A40 LS00
A39 LS32
+ ADV RD OR WRT
- WRT PULSE

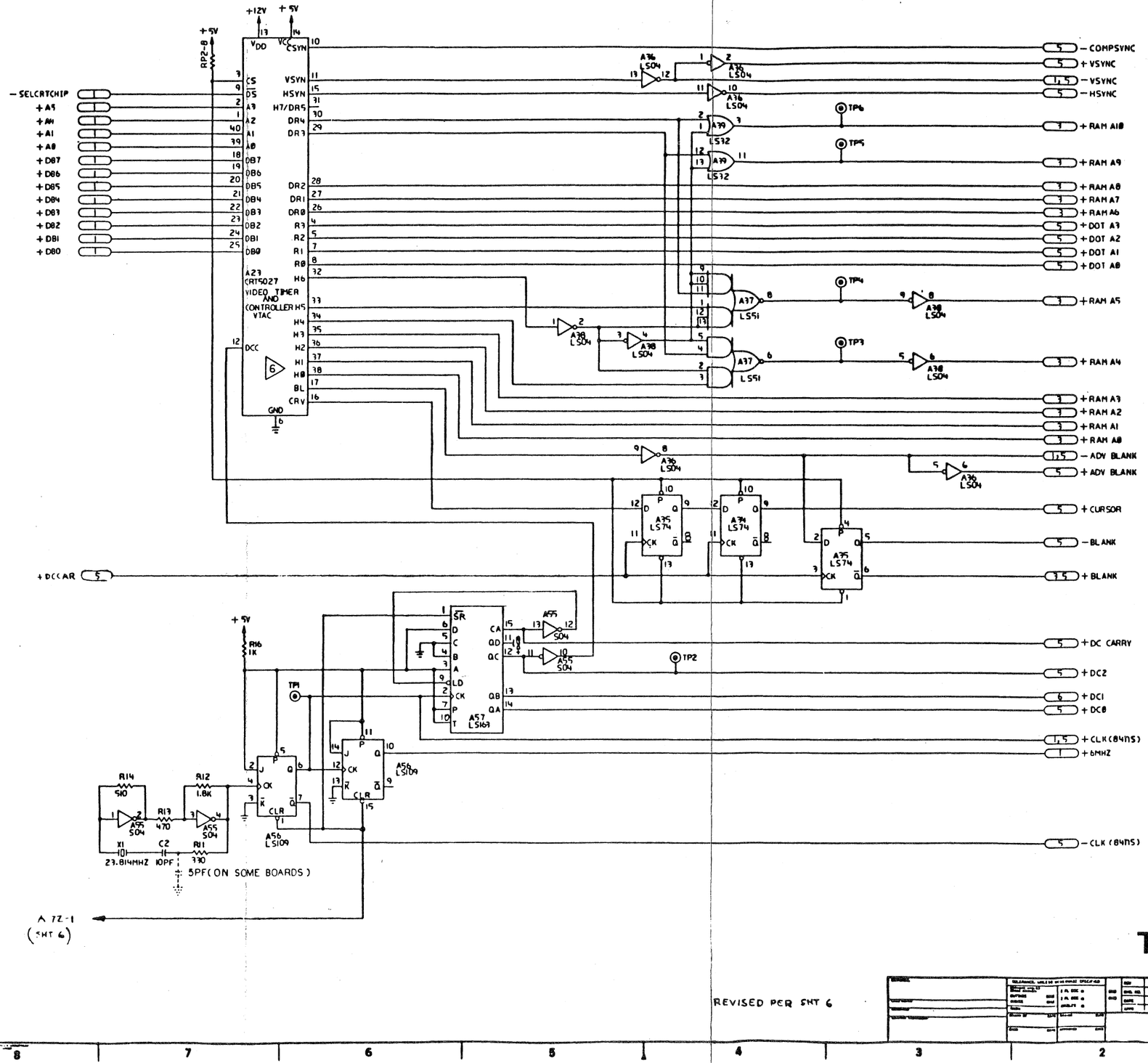
2114-3 OPT

+ DISPDATA 7
6
5
4
3
2
1
+ DISPDATA 0
- CPACC

REVISED PER SHEET 6

TeleVideo, Inc.

E 70001-H

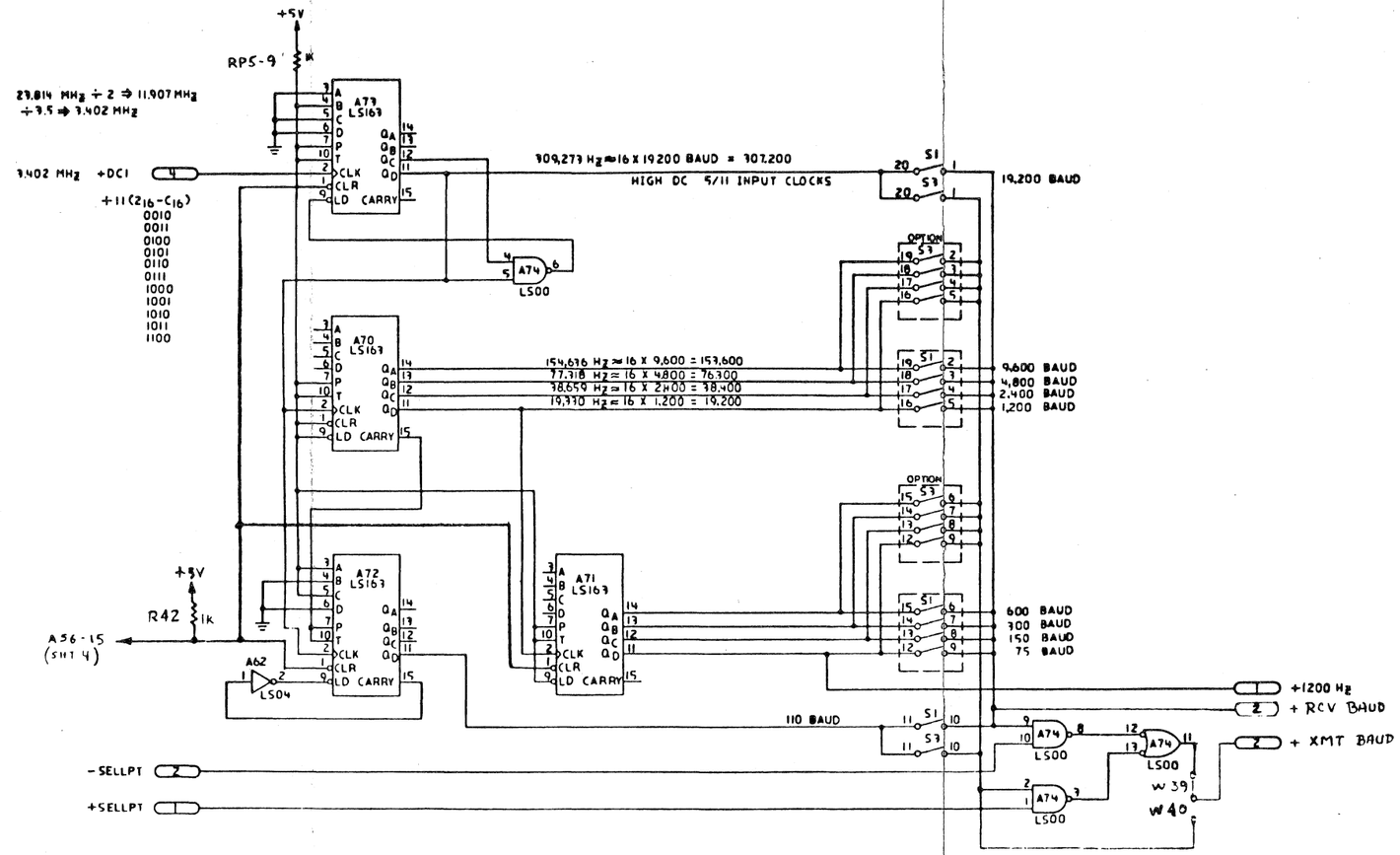

+12V
+5V
RP2-8
- SELCRTCHIP
+A5
+A4
+A3
+A2
+A1
+A0
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
CRT5027
VIDEO TIMER AND CONTROLLER VTAC
- COMPSYNC
+ VSYNC
- VSYNC
- HSYNC
+ RAM A10
+ RAM A9
+ RAM A8
+ RAM A7
+ RAM A6
+ DOT A3
+ DOT A2
+ DOT A1
+ DOT A0
+ RAM A5
+ RAM A4
+ RAM A3
+ RAM A2
+ RAM A1
+ RAM A0
- ADV BLANK
+ ADV BLANK
+ CURSOR
- BLANK
+ BLANK
+ DCCAR
+ DC CARRY
+ DC2
+ DC1
+ DC0
+ CLK (64NS)
+ 6MHZ
- CLK (64NS)
TP6
TP5
TP4
TP3
TP2
TP1
A39 LS32
A37 LS51
A38 LS04
A36 LS04
A35 LS74
A34 LS74
A57 LS163
A56 LS109
A55 S04
R16 1K
R14 510
R12 1.8K
R13 470
R11 330
X1 23.814MHZ
C2 10PF
5PF (ON SOME BOARDS)
A 72-1 (SHT 6)
REVISED PER SHT 6
TeleVideo, Inc.
E 70001-H

+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+DC0
-ALE
-CPACC
+DC2
+DISP DATA 7
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCAR
UNDERLINE
INVERT VIDEO
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC

A62 LS04
A36 LS04
A14 LS05 (O.C.)
A62 LS04
A55 S04
A20 LS00

TeleVideo, Inc.

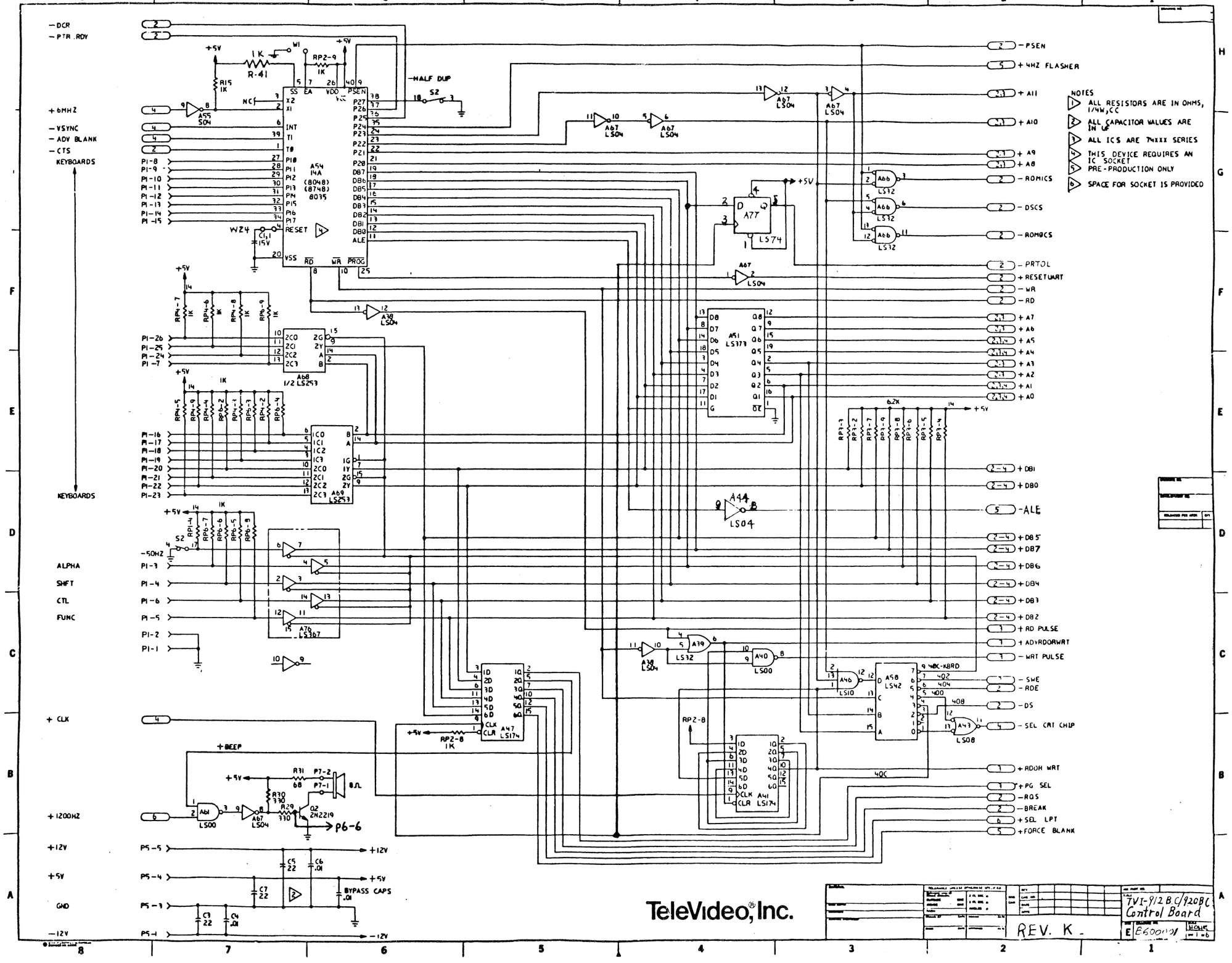
E 7000/-H -5-6

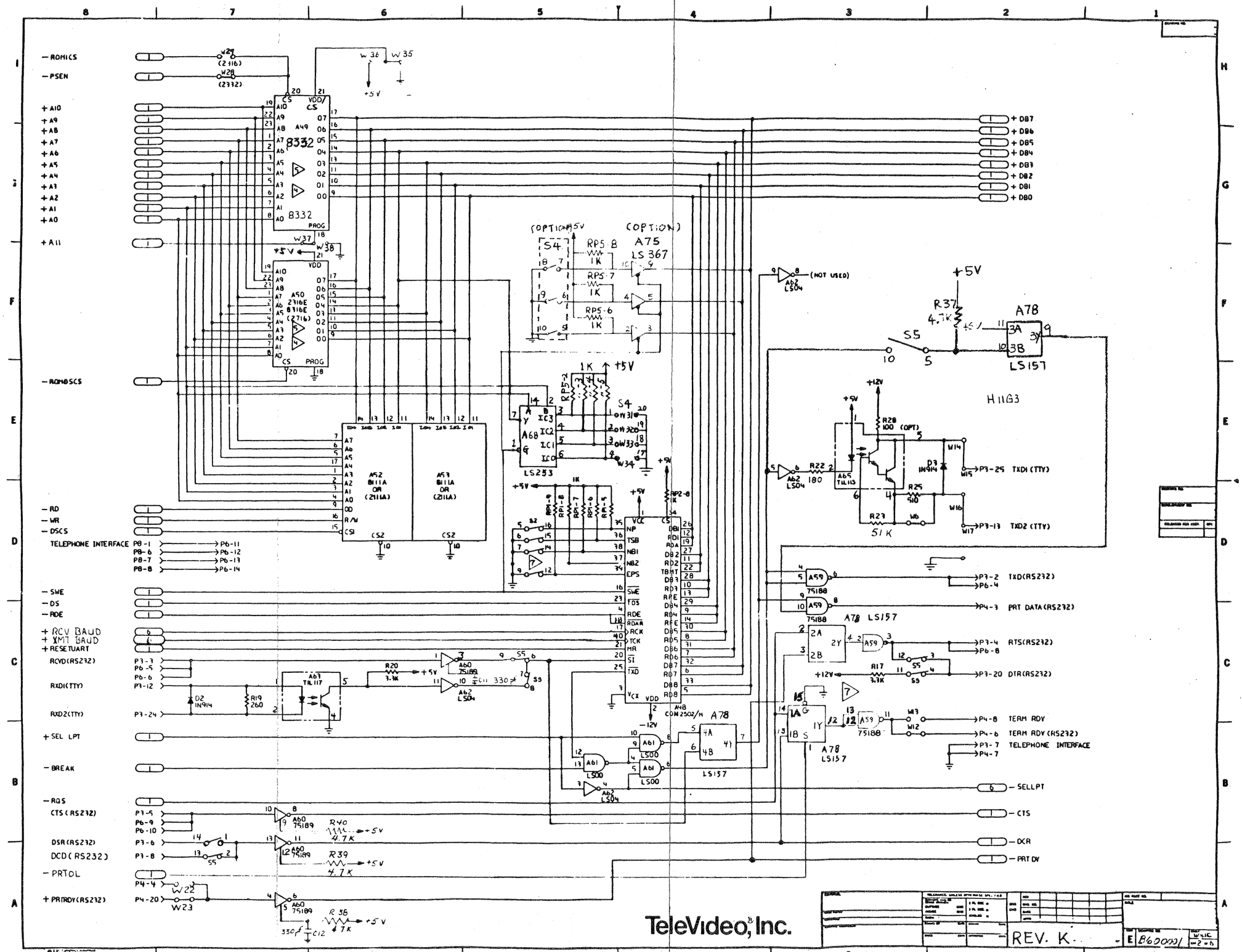


BAUD RATE GENERATION

TeleVideo, Inc.

E 70001-H


NOTES
ALL RESISTORS ARE IN OHMS, 1/4W, CC
ALL CAPACITOR VALUES ARE IN UF
ALL ICS ARE 74XXX SERIES
THIS DEVICE REQUIRES AN IC SOCKET
PRE-PRODUCTION ONLY
SPACE FOR SOCKET IS PROVIDED
-DCR
-PTR. RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
ALPHA
SHFT
CTL
FUNC
+ CLK
+1200HZ
+12V
+5V
GND
-12V
-50HZ
+BEEP
-HALF DUP
+PSEN
+4HZ FLASHER
+A11
+A10
+A9
+A8
-ROM1CS
-DSCS
-ROM0CS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CAT CHIP
+RDOH WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
TeleVideo, Inc.
TVI-912B C/920B C Control Board
REV. K
E 8600101


-ROMICS
-PSEN
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+A11
-ROM0SCS
-RD
-WR
-DSCS
TELEPHONE INTERFACE P8-1 → P6-11
P8-6 → P6-12
P8-7 → P6-13
P8-8 → P6-14
-SWE
-DS
-RDE
+RCV BAUD
+XMT BAUD
+RESET UART
RCVD(RS232) P3-3, P6-5
RXDI(TTY) P6-6, P3-12
RXD2(TTY) P3-24
+SEL LPT
-BREAK
-RQS
CTS(RS232) P3-5, P6-9, P6-10
DSR(RS232) P3-6
DCD(RS232) P3-8
-PRTDL P4-4
+PRTRDY(RS232) P4-20
8332
2716
A52 8111A OR (2111A)
A53 8111A OR (2111A)
A49
A50 2316E 8316E (2716)
A48 COM2502/H
A78
A75 LS367
A68 LS253
A63 TIL117
A60 75189
A61 LS00
A62 LS504
A59 75188
A65 TIL113
LS157
H11G3
(OPTION) +5V
(OPTION) A75 LS367
RPS-8 1K
RPS-7 1K
RPS-6 1K
S4
S5
W20 (2716)
W28 (2732)
W36
W35
W37
W38
+5V
+12V
-12V
1K
R37 4.7K
R28 100 (OPT)
R22 180
R25 510
R23 51K
D3 IN914
D2 IN914
R19 260
R20 3.3K
R40 4.7K
R39 4.7K
R36 4.7K
C11 330pf
C12 330pf
W22
W23
(NOT USED)
P3-25 TXDI (TTY)
P3-13 TXD2 (TTY)
P3-2 TXD(RS232)
P6-4
P4-3 PRT DATA(RS232)
P3-4 RTS(RS232)
P6-8
P3-20 DTR(RS232)
P4-8 TERM RDY
P4-6 TERM RDY(RS232)
P3-7 TELEPHONE INTERFACE
P4-7
-SELLPT
-CTS
-DCR
-PRT DV
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
TeleVideo, Inc.
REV. K
B600001

DISPLAY RAM ADDRESS

+ RAMA3
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A3
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

A27 LS139
+ PG SEL
-CS3
-CS2
-CS1
-CS0

+5V
R36 4.7K
A21 LS86

A13 DP8304
+ DB7
+ DB0
+ RD PULSE
B⇔A
T⇔R
DIR T/R
EN

+ RD OR WRT
+ A11
A40 LS00
A39 LS32
+ ADV RD OR WRT
- WRT PULSE

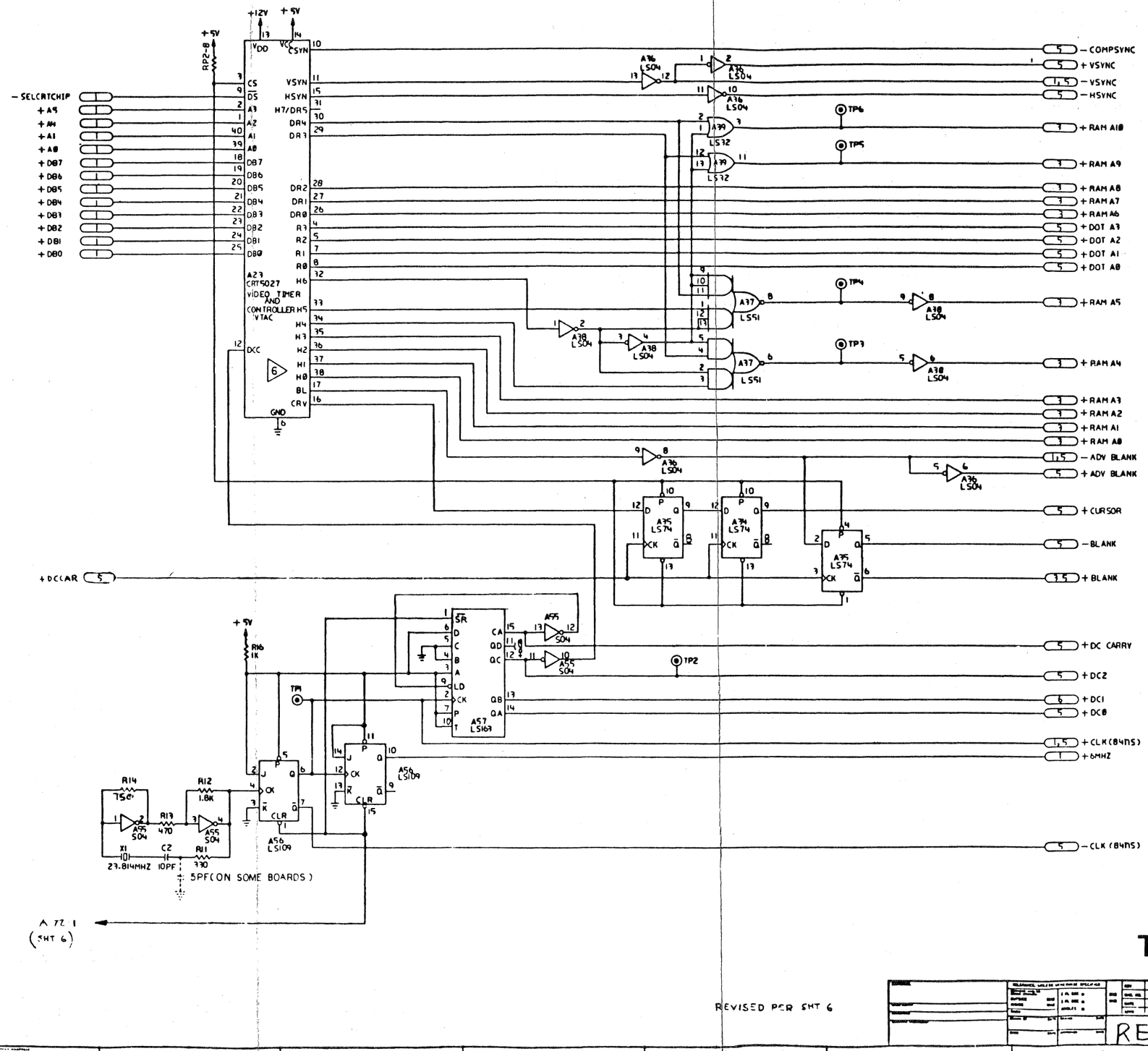
2114-3
WE
CS
OPT

+ DISPDATA 7
+ DISPDATA 0
- C PACC

TeleVideo, Inc.

REVISED PER SHEET 6

REV. K

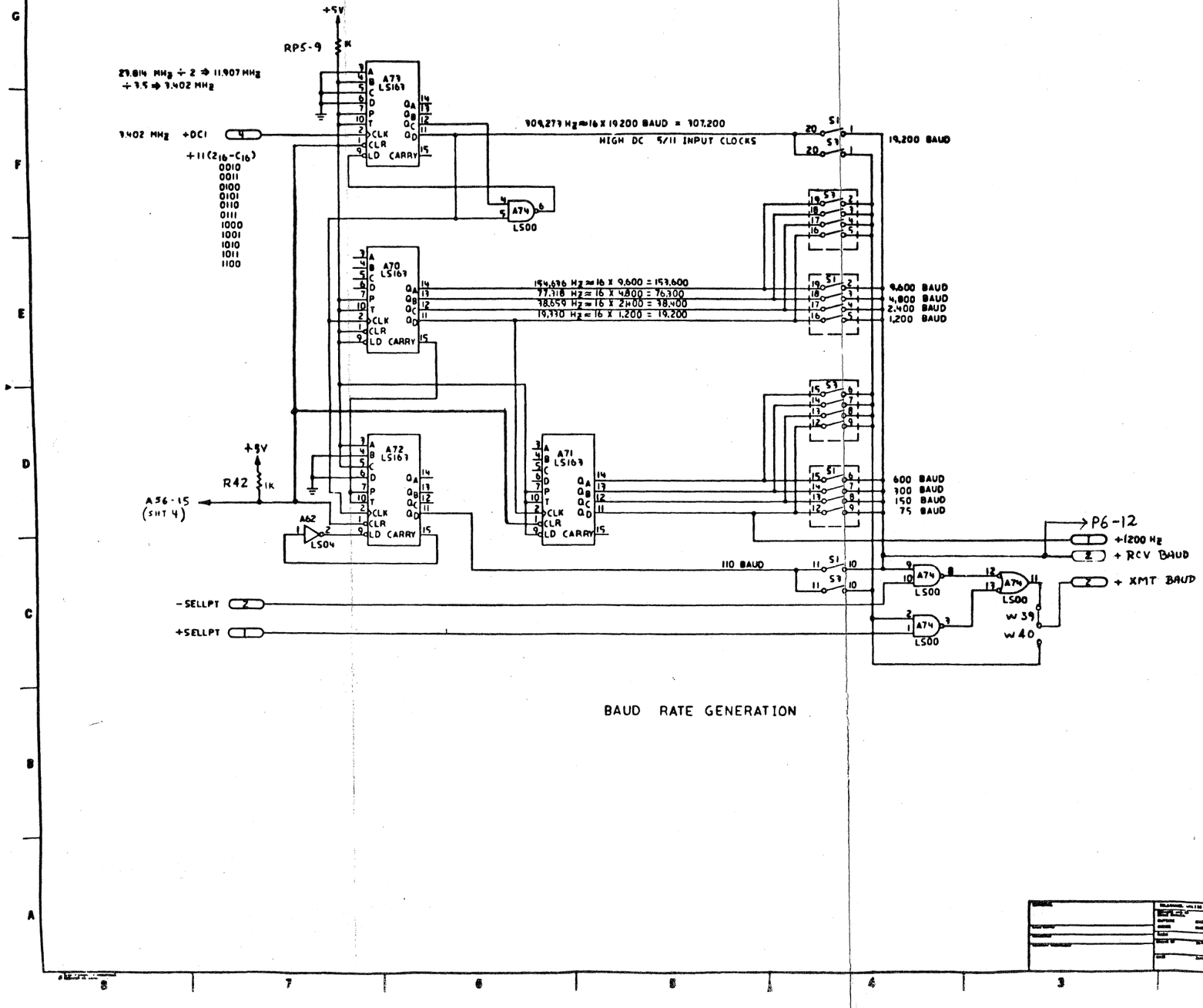

+12V
+5V
RP2-8
VDD
VCC
CSYN
VSYN
HSYN
H7/DR5
DR4
DR3
DR2
DR1
DR0
R3
R2
R1
R0
H6
H5
H4
H3
H2
H1
H0
BL
CRV
GND
DCC
CS
DS
A23
CRT5027
VIDEO TIMER AND CONTROLLER VTAC
- SELCRTCHIP
+ A9
+ A4
+ A1
+ A0
+ DB7
+ DB6
+ DB5
+ DB4
+ DB3
+ DB2
+ DB1
+ DB0
A36 LS04
A39 LS32
A37 LS51
A38 LS04
TP6
TP5
TP4
TP3
TP2
TP1
- COMPSYNC
+ VSYNC
- VSYNC
- HSYNC
+ RAM A10
+ RAM A9
+ RAM A8
+ RAM A7
+ RAM A6
+ DOT A3
+ DOT A2
+ DOT A1
+ DOT A0
+ RAM A5
+ RAM A4
+ RAM A3
+ RAM A2
+ RAM A1
+ RAM A0
- ADV BLANK
+ ADV BLANK
+ CURSOR
- BLANK
+ BLANK
+ DC CARRY
+ DC2
+ DC1
+ DC0
+ CLK (84NS)
+ 6MHZ
- CLK (84NS)
+ DCCAR
A35 LS74
A34 LS74
A55 S04
A57 LS163
A56 LS109
R16 1K
R14 75Ω
R12 1.8K
R13 470
R11 330
C2 10PF
X1 27.814MHZ
5PF (ON SOME BOARDS)
A 72-1 (SHT 6)
REVISED PER SHT 6
TeleVideo, Inc.
REV. K
B600001-4-6

+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+DC0
+5V
-ALE
-CPACC
+DC2
+DISP DATA 7 6 5 4 3 2 1
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCA7
UNDERLINE
INVERT VIDEO
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC
A62 LS04
A36 LS04
A14 LS05 (O.C.)
A62 LS04
A55 S04
LS00

TeleVideo, Inc.

REV. K

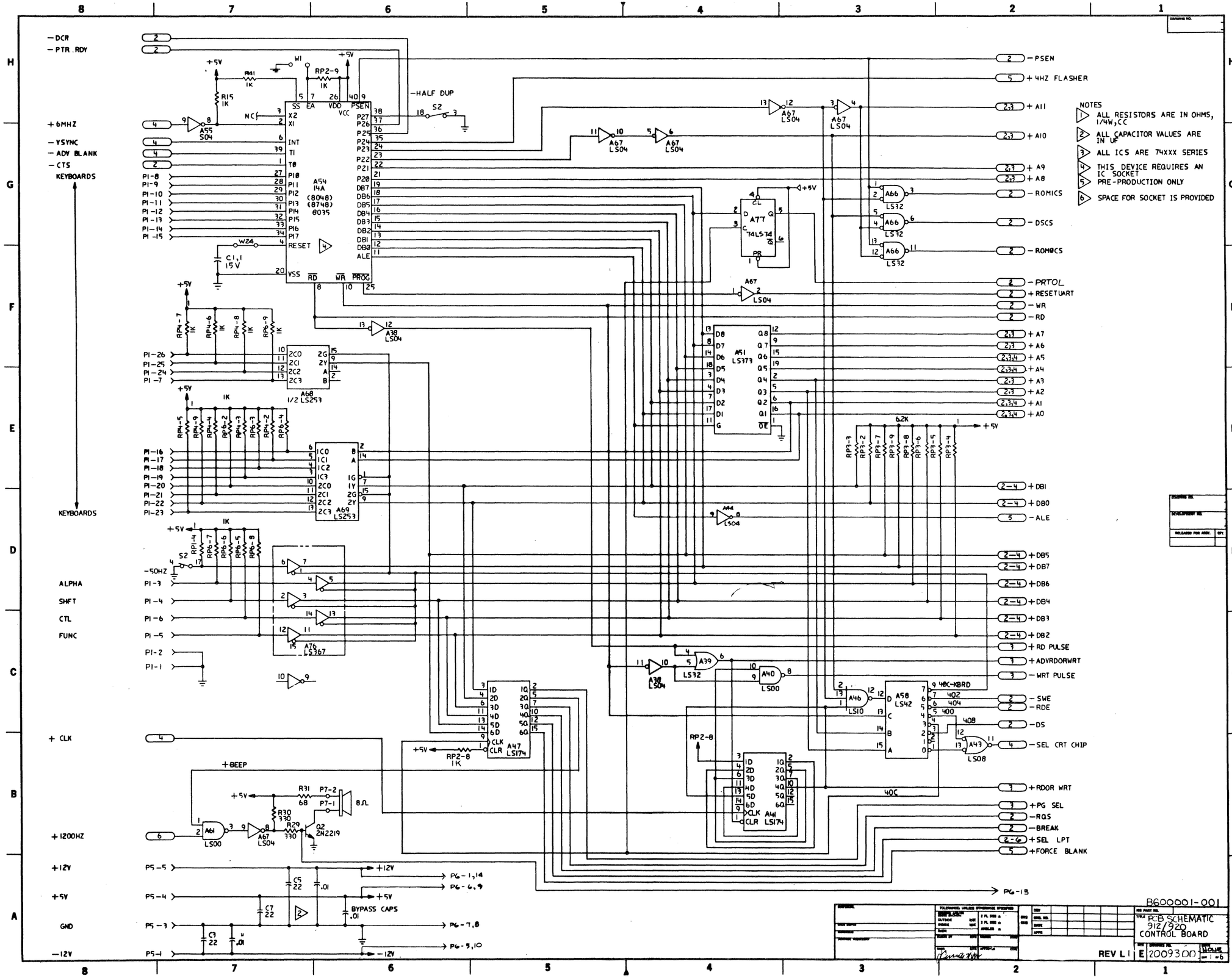
E 8600001 1-5-6



BAUD RATE GENERATION

TeleVideo, Inc.

REV. K


NOTES
1 ALL RESISTORS ARE IN OHMS, 1/4W, CC
2 ALL CAPACITOR VALUES ARE IN UF
3 ALL ICS ARE 74XXX SERIES
4 THIS DEVICE REQUIRES AN IC SOCKET
5 PRE-PRODUCTION ONLY
6 SPACE FOR SOCKET IS PROVIDED
-DCR
-PTR.RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
KEYBOARDS
-HALF DUP
A54 I4A (8048) (8748) 8035
A55 S04
A67 LS04
A77 74LS74
A51 LS373
A68 1/2 LS253
A69 LS253
A76 LS367
A47 LS174
A38 LS04
A39 LS32
A40 LS00
A44 LS04
A46 LS10
A58 LS42
A66 LS32
A43 LS08
A61 LS00
A67 LS04
A44 LS174
-PSEN
+4HZ FLASHER
+A11
+A10
+A9
+A8
-ROMICS
-DSCS
-ROM0CS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CRT CHIP
+RDOR WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
+CLK
+1200HZ
+12V
+5V
GND
-12V
+BEEP
ALPHA
SHFT
CTL
FUNC
-50HZ
P6-13
B600001-001
PCB SCHEMATIC 912/920 CONTROL BOARD
REV L1
E
2009300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

P7-2
P7-1
P3-5 CTS (RS232)
P7-4
P7-3
-PRTOL
+SEL LPT
-BREAK
-RQS (RS232)
P3-8 DCD (RS232)
P3-6 DSR
P4-Z PRT RCV
P6-3
P3-3 RCVD (RS232)
P3-12 RXD1 (TTY)
P3-24 RXD2 (TTY)
P4-4
P4-20 PRT RDY (RS232)
P7-8
P7-5 +RCV BAUD
P7-10
P7-9 +XMT BAUD
P7-11 RESET UART
-RDE
-DS
P7-6 EDC
-RD
-WR
-DSCS
-ROM0CS
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
-ROM1CS
-PSEN
A11
-SWE

A60 75189
R40 4.7K +5V
A62 74LS04
A66 74LS32
A61 74LS00
A61 74LS00
A61 74LS00
W50
W54
W56
W55
W58
W57
W46
W45
W47
W49
R39 4.7K +5V
R43 10K
R20 3.3K
A60 75189
C11 330pF
A32 74LS08
A62 74LS04
W48
A63 TIL 117
D2 IN914
R19 680
A60 75189
R38 4.7K +5V
W53
C12 330 pF
W22
W23
W43
W44
W29
W28
W36
W35
W38
W37
A60 75189
2332 A49
2316E A50 (2716)
8111A (2111A) A52
8111A (2111A) A53
RP5 1K
S4
A68 LS253
A75 74LS367
(OPTION)

A62 74LS04
R22 180
A69 TIL 113
R26 100 (OPT) +12V
D3 IN914
R25 510
R23 1K
W14
W15
W16
W17
W6
TXD1 (TTY) P3-25
TXD2 (TTY) P3-13
TXD (RS232) P3-2 P6-2
W51
W52
75188 A59
W55
R37 4.7K +5V
A78 74LS157
75188 A59
PRT DATA (RS232) P4-3
W13 TERM RDY (RS232)
W12 TERM RDY (RS232) P4-8 P4-6
RTS (RS232) P3-4
DTR (RS232) P3-20
+12V R17 3.3K
-PRT RDY
-DCR
RP1 1K
S2
RP2-8
A48 COM2502/H
-12V
SIGNAL GND P3-7 P4-7
+DB0
+DB1
+DB2
+DB3
+DB4
+DB5
+DB6
+DB7

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Sonny 5-14-81
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK Alexander 7/3/81
		SCALE:	ENGR
		MATERIAL	APPD
			APPD
			APPD
			FINISH

B600001-001

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 912/920 CONT. BD. 565

SIZE D | SHT 2 OF 6 | DRAWING NO. 2009300 | REV L1

DISPLAY RAM ADDRESS

+ RAMA9
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A3
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

A27 LS139

+ PG SEL
-CS3
-CS2
-CS1
-CS0

+5V
R36 4.7K
A21 74LS86

A12 2114-3
A10 2114-3
A6 2114-3
A11 2114-3
A9 2114-3
A7 2114-3
A5 2114-3
OPT

A13 DP8304

+ DB7
+ DB0
+ RD PULSE

+ RD OR WRT
+ A11
A40 LS00
A39 LS32
+ ADV RD OR WRT
- WRT PULSE

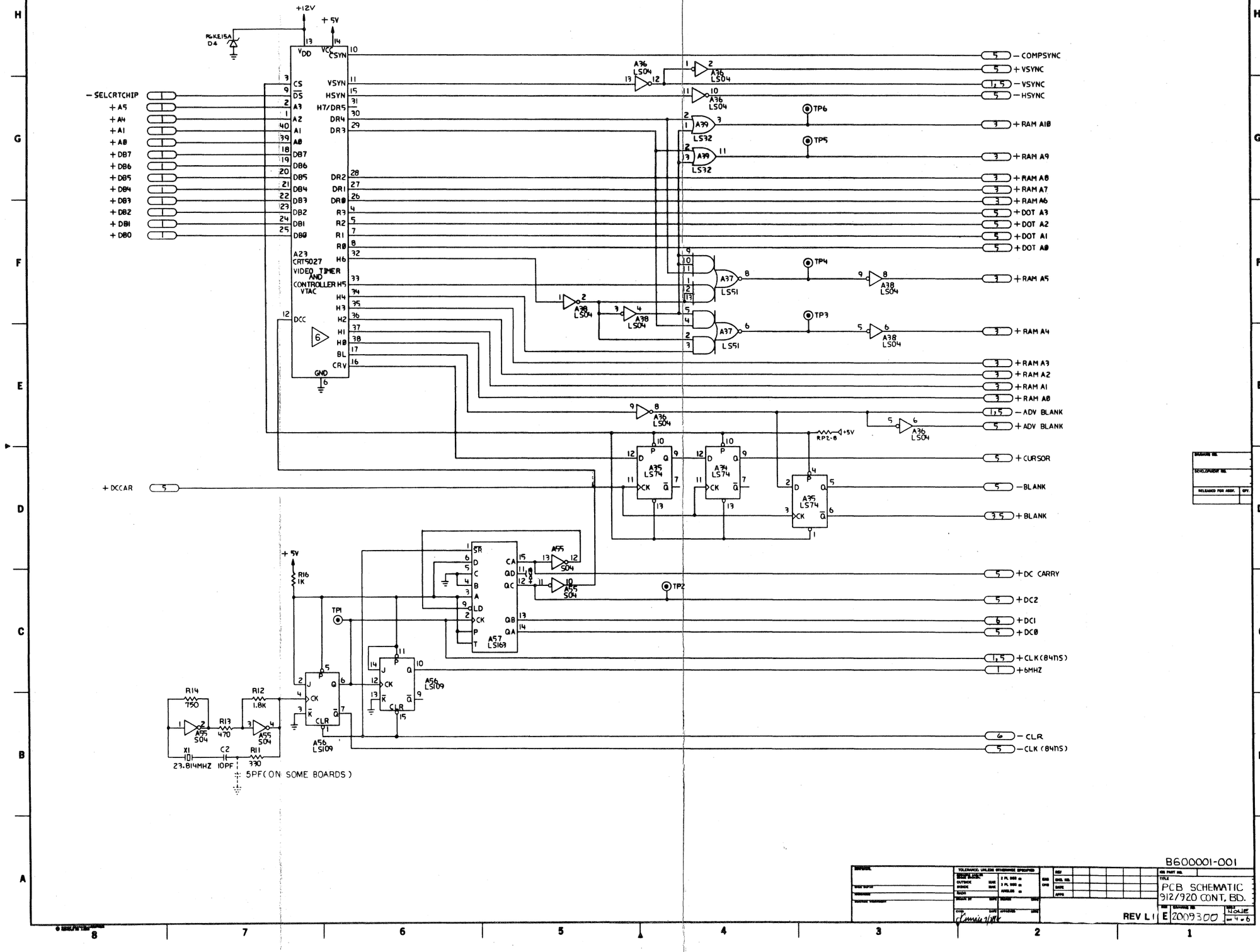
+ DISPDATA 7
+ DISPDATA 0
- CPACC

B600001-001

PCB SCHEMATIC
912/920 CONT. BD.

REV L1

E 2009300



B600001-001

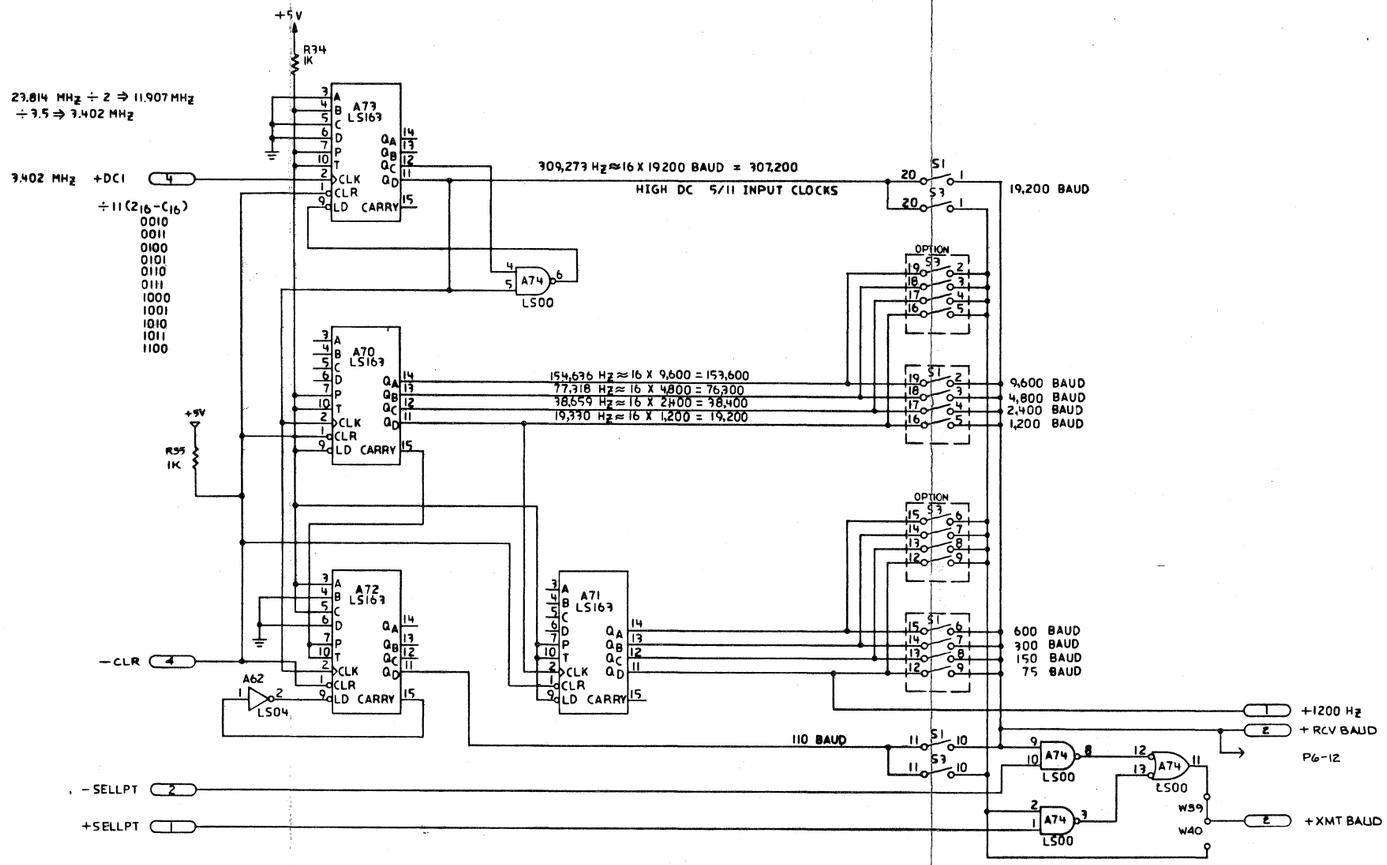
PCB SCHEMATIC 912/920 CONT. BD.

REV L1

E 2009300

SHT 4 of 6

+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+DC0
-ALE
-CPACC
+DC2
+DISP DATA 7
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCAR
LOW
"2716" W30
S2
+DRD0
+DRD1
+DRD2
+DRD3
+DRD4
+DRD5
+DRD6
+DRD7
UNDERLINE
INVERT VIDEO
W42
W41
CR
IN914
Q1 2N2219
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC
NE555
VCC RST
THR
DISCH OUT
CTLV
GND
PCB SCHEMATIC
912/920 CONT. BD.
REV L1
B600001-001
E 2009300
SHEET 5 of 6



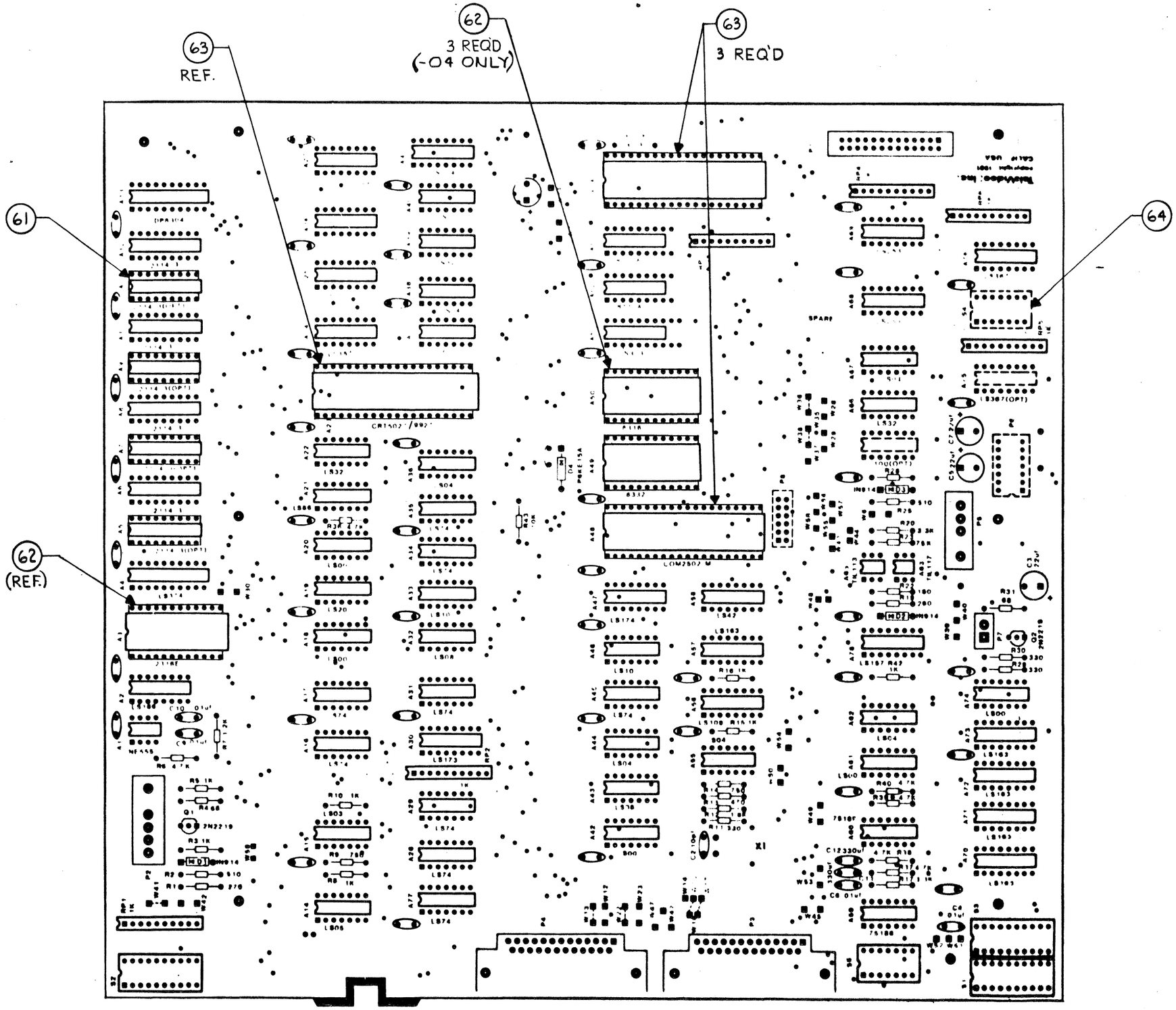
BAUD RATE GENERATION

B60000-001

PCB SCHEMATIC
912/920 CONT. BD.

REV L 1

E 2009300


63
REF.
62
3 REQ'D
(-04 ONLY)
63
3 REQ'D
61
64
62
(REF.)

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
1	1	1	1	1	1					C2	Cap DIP Mica 10pf 100D03	2024100
2	3	3	3	3	3					C3,6,7	Cap R/L 22uf 15V	2025700
3	1	1	1	1	1					C1	Cap R/L 1uf 15V	2027901
4	47	47	47	47	47					unmarked	Cap C/D .01uf 20% 16V	2028700
5	1	4	1	1	1					C10	Cap C/D .01uf 10% 50V Y5P	2028900
6	2	2	0	0	2					C11,12	Cap C/D 330pf 50V 20%	2029100
7	1	1	1	1	1					A42	IC 74S00	2024000
8	5	5	5	5	5					A18,20,40,61.74	IC 74LS00	2024200
9	1	1	1	1	1					A15	IC 74LS03	2024400
10	1	1	1	1	1					A55	IC 74S04	2024600
11	5	5	5	5	5					A36,38,44,62,67	IC 74LS04	2024800
12	1	1	1	1	1					A14	IC 74LS05	2025000
13	2	2	2	2	2					A32,43	IC 74LS08	2025200
14	2	2	2	2	2					A33,46	IC 74LS10	2025400
15	1	1	1	1	1					A19	IC 74LS20	2025600
16	3	3	3	3	3					A22,39,66	IC 74LS32	2025800
17	1	1	1	1	1					A58	IC 74LS42	2026000
18	1	1	1	1	1					A37	IC 74LS51	2026200
19	1	1	1	1	1					A17	IC 74S74	2026400
20	8	8	7	8	8					A16,28,29,31,34,	IC 74LS74	2026600
										35,45,77		

NOTES:

TITLE
CONTROL BOARD, TVI-912/920 TERMINAL

DATE
02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
21	1	1	1	1	1					A21	IC 74LS86	2026800
22	1	1	1	1	1					A56	IC 74LS109	2027000
23	1	1			1					A27	IC 74LS139	2027200
24	4	4	3	4	4					A24,25,26,78	IC 74LS157	2027400
25	5	5	5	5	5					A57,70-73	IC 74LS163	2027600
26	1	1	1	1	1					A2	IC 74LS166	2027800
27	1	1	1	1	1					A30	IC 74LS173	2028000
28	2	2	2	2	2					A41,47	IC 74LS174	2028200
29	2	2	2	2	2					A68,69	IC 75LS253	2028400
30	1	1	1	1	1					A76	IC 74LS367	2028600
31	1	1	1	1	1					A51	IC 74LS373	2028800
32	1	1	1	1	1					A4	IC 74LS374	2029000
33	1	1	1	1	1					A59	IC 75188N	2029200
34	1	1	1	1	1					A60	IC 75189AN	2029400
35	1	1	0	0	1					A65	IC H11G3	2034200
36	1	1	1	1	1					A63	IC TIL117, 4N37	2029300
37	1	1	1	1	1					A3	IC 2316 ROM A3-2	2034600
38	1	1	1	1	1					A1	IC NE555	2030200
39	1	1	1	1	1					A13	IC DP8304	2030400
40	2	2	2	2	2					A52,53	IC AMD2111-4A	2030600
41	1	1	1	1	1					A48	IC 2502, AY-5-1013A	2030800

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
42	1	1	1	1	1					A23	IC 5027,5037,TMS9927	2031000
43	1	1	1	1	1					A54	IC Microprocessor P8035	2031200
44	4	4	4	4	4					A6,8,10,12	IC TMS4045-25NL, 2114 300NS	2035800
45			(4)	(4)	(4)					A5,7,9,11	IC TMS 4045 Option-2nd page	
46			0	1	1					A49B	IC 8332A 32K ROM A49B	2032600
47			0	1	1					A49C	IC 8332A 32K ROM A49C	2032600
48			(1)	0	0					A49R	IC 2316 16K ROM A49R	2032200
49			(1)	0	0					A50R	IC 2316 16K ROM A50R	2032400
50	1	1									IC A49C1	2034000
51	1	1	1	1	1					S5	Dip Switch 7 Pos Top	2174200
52	1	1	(1)	1	1					S3	Dip Switch 10 Pos Top	2181000
53	2	2	2	2	2					S1,2	Dip Switch 10 Pos Side	2096800
54	2	2	(2)	2	2					P3,4	Connector RS232 R/A	2097800
55	4	4	4	4	4					XA5,7,9,11	Socket IC 18 Pin	2098400
56			1	1	1					XA49	Socket IC 24 Pin	2098401
57	3	3	1	1	1					XA50	Socket IC 24 Pin	2098401
58	3	3	2	2	2					XA23,54	Socket IC 40 Pin	2098402
59	1	1	0	0	1					XS4	Socket IC 14 Pin	2098403
60	1	1	1	1	1					X1	Cry 23.814 MHz Fundamental	2098600
61	1	1	1	1	1					P7	Plug 2 Pin	2098501
62	2	2	2	2	2					P2,5	Plug 5 Pin	2098706

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
63	1	1	1	1	1					P1	Plug 26 Pin	2098701
64	2	2	2	2	2					R4,31	Res C/F 68 Ohm 5% 1/4W	2051100
65	1	1	1	1	1					R22	Res C/F 180 Ohm 5% 1/4W	2053300
66	2	2	2	2	2					R1,19	Res C/F 270 Ohm 5% 1/4W	2051300
67	3	3	4	4	4					R11,20,29,30	Res C/F 330 Ohm 5% 1/4W	2051500
68	1	1	1	1	1					R13	Res C/F 470 Ohm 5% 1/4W	2051700
69	2	2	3	3	3					R2,14,25	Res C/F 510 Ohm 5% 1/4W	2051900
70	2	2	1	1	1					R9	Res C/F 750 Ohm 5% 1/4W	2031700
71	6	6	6	6	6					R3,5,8,10,15,16	Res C/F 1K Ohm 5% 1/4W	2052100
72			1	0	0					R34	Res C/F 1K Ohm 5% 1/4W	2052100
73	2	2	0	0	2					R41,42	Res C/F 1K Ohm 5% 1/4W	2052100
74	1	1	1	1	1					R7	Res C/F 1.2K Ohm 5% 1/4W	2031900
75	1	1	1	1	1					R12	Res C/F 1.8K Ohm 5% 1/4W	2052300
76			1	1	1					R17	Res C/F 3.3K Ohm 5% 1/4W	2052700
77	2	2	3	3	0					R18,32,33	Res C/F 3.3K Ohm 5% 1/4W	2052700
78	1	1	1	1	1					R6	Res C/F 4.7K Ohm 5% 1/4W	2053100
79	5	5	0	0	5					R36-40	Res C/F 4.7K Ohm 5% 1/4W	2053100
80		1	0	0	1					R23	Res C/F 51K Ohm 5% 1/4W	2032300
81	1									R23		2032500
82			1	1	0					R23	Res C/F 1M Ohm 5% 1/4W	2031500
83	5	5	4	4	4					RP1,2,4,6	Res Pack 1K Ohm	2040500

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
84	1	1	0	1	1					RP3	Res Pack 6.2K Ohm	2040700
85		1								R43	Res C/F 10K Ohm 5% 1/4W	2033300
86	2	2	2	2	2					Q1,2	TR 2N4401	2045500
87	3	3	3	3	3					D1,2,3	Diode 1N914	2047500
88		1									P6KE15A Diode	2047900

NOTES:

TITLE CONTROL BOARD, TVI-912/920 TERMINAL

DATE 2-1-83

TeleVideo Systems, Inc.

MODEL 910

THEORY OF OPERATION

Section

MODEL 910 THEORY OF OPERATION

4.1

OVERVIEW

The Model 910 terminal is a microprocessor-based product which employs a maximum of standard large-scale integration (LSI) circuits. This design approach helps simplify the printed circuit board and provides for a large degree of maintainability. Because the terminal is microprocessor based, with all communications and keyboard functions firmware controlled, the terminal's operation is quite easy to modify.

The microprocessor is, after initialization, totally interrupt driven, i.e., the microprocessor is normally idling unless it receives an interrupt, which is an input to the microprocessor indicating that data is available which must be processed. This operation is described in Section 4.6.

4.2

VIDEO CLOCK

The most basic block in the circuit is the video (or dot) clock. The frequency of the video clock is 13.608 megaHertz, produced by a crystal-controlled oscillator formed by part of Chip A22, the crystal Y2, and several other passive components (see Sheet 3 of the schematic).

This clock is used to shift video information out of a shift register (see Section 4.7) and is divided down to create the system clock.

System Clock - The system clock is created by dividing the video clock by eight to derive a system clock frequency of 1.701 mega Hertz. This function is performed by a presettable four-bit binary counter (A15, sheet 3) as follows: When the counter reaches its terminal count 15 or F_{16}, the next positive transition of the video clock loads a count of eight into the counter. This happens every eight counts of the video clock. The QC output of the counter is high for four counts and low for four counts, and is used to provide a symmetrical clock for the microprocessor system.

Keyboard Clock - The keyboard controller (A1, Sheet 5) has a self-contained oscillator which provides a clock for scanning the keyboard matrix. The frequency is controlled by C53 and R26, which are selected to produce a frequency of approximately 80 kiloHertz.

Baud Rate Clock - The communications baud rate clock is internal to the asynchronous communications interface adapter (ACIA) chip (A19, Sheet 4). Using a 1.8432 megaHertz crystal, the ACIA

(under firmware control) provides all of the 15 baud rates possible for the Model 910.

4.3

ADDRESS DECODING

The 6502A microprocessor is capable of addressing 65,536 bytes of memory. The Model 910 uses only a fraction of this capability, allowing a rather simple decode. The entire range of the 6502 is divided into four sections of 16,384 bytes each. The lowest section is reserved for system RAM, of which only 1024 bytes are used. The next highest section contains display RAM, of which only 2048 bytes are used. The second highest section is used for input/output parts, of which only 14 are used; the highest section contains system ROM, which is 4096 bytes (expandable to 8192 bytes).

Dividing the address range into four sections is accomplished using a 1 of 4 decoded (A17, Sheet 1) connected to address lines A14 and A15.

4.4

TERMINAL MEMORY

System ROM - System ROM consists of a single 4096-byte ROM (A45, Sheet 1). This chip is selected when the microprocessor is addressing within the range of $C000_{16}$ - $FFFF_{16}$. Since there is no other memory located in this range, it "looks like" F000-FFFF, which is the upper-most 4096 bytes of the address space.

It is possible, by moving a jumper and using a larger chip, to increase the system ROM to 8192 bytes.

System RAM - System RAM consists of 1024 bytes (A50 and A51, Sheet 1) of static RAM. These chips are selected when the microprocessor is addressing within the range of $0000 - 3FFF_{16}$. Again, since there is no other memory within this range, system RAM has an effective address range of $0000_{16} - 03FF_{16}$.

4.5

DISPLAY FUNDAMENTALS

The circuitry required to display data on the CRT other than the video circuitry (covered in 4.7) is divided into three sections:

- Display memory
- Character generation
- CRT Controller (CRTC)

The display memory consists of 2048 bytes of high-speed static RAM, which is 128 bytes more than required to store one screen (24 rows of 80 characters) or 1920 characters. These chips (A30, A31, A36, and A37, Sheet 2) are accessed by two sources: the microprocessor and the CRTC.

The CRTC causes a "read" of a location within the display RAM once during each cycle of the system clock, cycling completely through the memory ten times each frame (60 frames per second). This operation is called "screen refresh".

The data stored in the display RAM is changed or updated by the microprocessor as necessary due to keypresses or receipt of data from the computer. To allow for addressing the display RAM from two sources without effects on the screen, the address outputs from the microprocessor and the CRTC are connected to the display RAM through multiplexers (A25, A32, and A38, Sheet 2) which connect the CRTC's address lines during the first half of the system clock and the microprocessor address lines during the second half of the system clock.

When the CRTC addresses a location display RAM, the contents of the location being addressed are latched by a byte-wide latch (A43, Sheet 3). The output of this latch connects to the address line of a characger generator ROM (A48, Sheet 3) which contains data necessary to form characters on the screen. The data from the character-generator ROM is loaded into a shift register (A49, Sheet 3) and shifted out, one bit at a time, by the dot clock for use by the video circuitry.

4.6

INTERRUPT SIGNALS

As mentioned in the Overview section, the microprocessor is entirely interrupt driven in the Model 910. An interrupt is merely an input to the microprocessor which tells it to complete its present operation and then go to another location in the program. The microprocessor will respond to an interrupt within eight system clock period (or 4.7 microseconds).

There are two types of interrupts to the 6502:

- Maskable (IRQ)
- Nonmaskable (NMI)

The maskable interrupt can be disabled by the program, while the nonmaskable interrupt cannot. Therefore the nonmaskable interrupt has priority over the maskable interrupt.

In the Model 910, NMI is used for an interrupt from the keyboard encoder (A1, Sheet 5). When a key is pressed, the keyboard encoder senses it, times a delay for debounce, and pre-

sents data on its data outputs. When this data is ready, the data ready output (A1, pin 1G) is pulsed, setting a flip-flop (A7, Sheet 4) causing an NMI. During the NMI, routine data from the keyboard encodes is read and the flip-flop is reset.

IRQ is also used and is caused by two sources: the ACIA (A19, Sheet 4) and the vertical sync from the CRTC which occurs 60 times per second (if set for 60 Hertz operation). The interrupt from the ACIA indicates there are data to be sent to or received from the computer. The interrupt from the CRTC is used to time intervals used for repeat key, blinking, bell, etc. The IRQ from the ACIA is produced by its IRQ output. Vertical sync from the CRTC sets a flip-flop (A40, Sheet 4) which causes an IRQ. During the IRQ routine, the ACIA is checked to see if it has caused the interrupt. If so, the ACIA is serviced and data sent or received, after which the processor returns to where it was prior to the interrupt. If not, then the CRTC must have caused the interrupt.

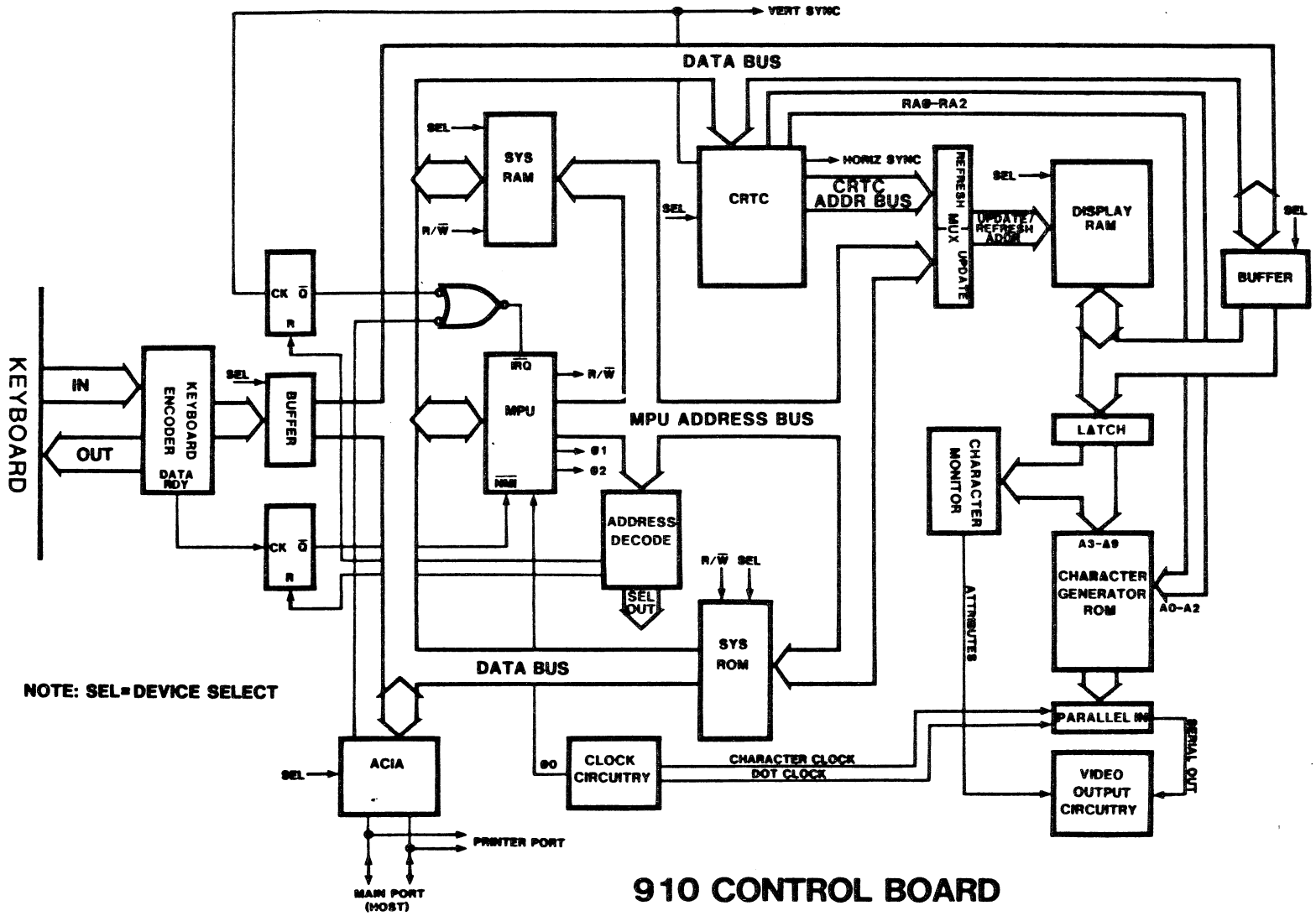
4.7

VIDEO GENERATOR

Control signals for the CRT monitor are generated by the CRTC, the attribute latch, and the output of the shift register mentioned in 4.5.

The CRTC generates the horizontal sync pulse and vertical sync pulse which define the horizontal and vertical dimensions of the display.

Through an amplifier in the monitor, the video output controls the electron beam in the CRT (turns it on and off). This is created by the stream of bits coming out of the shift register which combine with the attributes, cursor, and display enable, outputs from the CRTC, and the black on white/white on black control. This circuitry is shown in the top half of Sheet 4 of the schematic.



910 CONTROL BOARD

Figure 4-1

Model 910/910 PLUS MEMORY MAP

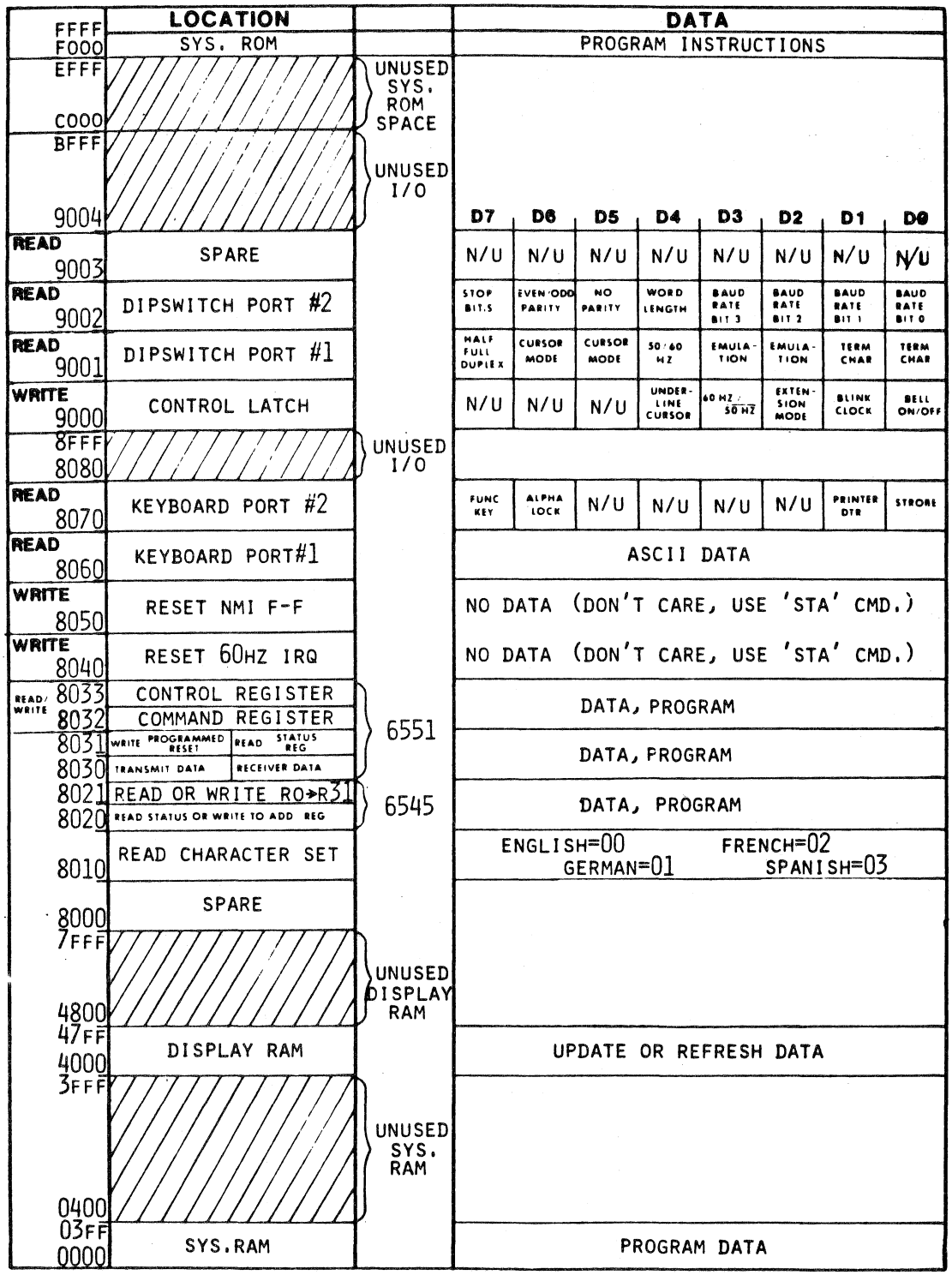


Table 4-1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ENGINEER RELEASE		
	B	ECO 80.116		

A39 6502A

A46 74LS08

A23 74LS04

A17 74LS139

A9 74LS00

A45 2332

A50 2114

A51 2114

A33 74LS32

A29 74LS32

A21 74LS08

A47 74LS02

A7 74LS74

A16 74LS138

A4 555

A22 74S04

R8 1K

R13 3.3K

R14 47K

R12 1M

RZ2 4.7K

RP1 4.7K

RP4 1K

RZ1 1K

CR1 IN914

C14 10µf

C22 0.01µf

C 23 0.01µf

C28 0.01µf

SH3 CHAR CLK

SH4 NMI

SH4 VERTSYNC/IRQ

SH4 IRQ (ACIA)

SH3 SET DISP RAM

SH3 CHAR CLK

R/W SH 2,4

Ø2 SH 2,4

Ø1 SH 2,3

D0–D7 SH 2,4,5

9XXØ

8000-BFFF

4000-7FFF

2000-FFFF

0000-3FFF

9XX1 DIPSWITCH PORT #1 SH5

9XX2 DIPSWITCH PORT #2 SH5

Ø2:W SH2

DISP RAM SEL SH2

DISP RAM WR SH2

DISP RAM SH2

CONTROL LATCH SH4

SYS RESET SH4

8X0X CHAR SET SEL RD SH5

8X1X SEL CRTC SH2

8X2X SEL ACIA SH4

8X3X RESET IRQ SH4

8X4X RESET NMI SH4

8X5X KYBD PORT #1 SH5

8X6X KYBD PORT #2 SH5

8X7X

A0–A12 SH4

A0–A9 SH2

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN				DWN	TeleVideo, Inc. 511
NEXT ASSY	USED ON					CHK	
		ANG	2 PLC	3 PLC		ENGR	TITLE 910 CONTROL BD
		±	±	±		APPD 3/15/84	
		SCALE				APPD	
		MATERIAL				FINISH	SIZE D SHT 1 OF 3 DRAWING NO 2014300 REV B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	SEE SHT 1		

CURSOR → SH3
RA0 → SH3
RA1 → SH3
RA2 → SH3
RA3 → SH3
DISP EN → SH3
HORIZ SYNC → SH3
VERT SYNC → SH4

SH1 DISP RAM WR
E43 OEM OPT
SH1 DISP RAM SEL
SH3 ROW 1Ø
SH4 CURSOR=UNDERLINE
SH4 60 HZ/50HZ → 3 PROG SEL
SH3 CHAR CLK → 21 CCLK
SH1 R/W → 22 R/W
SH1 ØZ → 23 ØZ(E)
SH1 SELCTRC 8XZX → 25 C3
RES
R15 1K
+5V
2Ø VCC
24 R3
GND 1

A26
68B045
6545

SH1,4,5 D0 D1 D2 D3 D4 D5 D6 D7 → 33 32 31 30 29 28 27 26 D0 D1 D2 D3 D4 D5 D6 D7

SH1 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10

SH1 Ø1
SH1 DISPRAM
SH1 Ø2·W

A44 74LS245 (DIR, CE, VCC; Y1-Y8; A1-A8; GND 10)

A20 74LS00 ×2
A27 74LS32
A23 74LS04
A29 74LS32 ×2
A28 74LS10
A34 74LS00
A33 74LS32
A34 74LS00

4000-43FF
4400-47FF

CURSOR 38
RA0 37
RA1 36
RA2 35
RA3 18
DISP EN 39
HORIZ SYNC 39
VERT SYNC 4Ø

A25 74LS157: MA0 MA1 MA2 MA3 → A0' A1' A2' A3'
A32 74LS157: MA4 MA5 MA6 MA7 → A4' A5' A6' A7'
A38 74LS157: 12 MA8, 13 MA9, 14 MA10 → A8' A9' A10'

A30 2114 A0'-A9' → D0' D1' D2' D3'
A36 2114 A0'-A9' → D4' D5' D6' D7'
A31 2114 A0'-A9' → D0' D1' D2' D3'
A37 2114 A0'-A9' → D4' D5' D6' D7'
A24 6116 * A0'-A10' → D0'-D7'
E39 E40 E41

D0' D1' D2' D3' D4' D5' D6' D7' → SH3

P5-5 +12V → +12V
P5-1 -12V → -12V
P5-4 +5V → +5V
P5-3 GND → GND
C3 22µf ELEC
C37 22µf ELEC
C20 22µf ELEC
C33 .01µf CER
0.1µf CER
ALL CAPS NOT SHOWN

* - OPTIONAL CHIP

B600011-00

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN	TeleVideo, Inc. SVL
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK	TITLE: PCB SCHEMATIC CONT BD 210
			ENGR	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D · SHT 2 OF 5 · DRAWING NO 2014300 · REV B1

B1 2014300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	SEE SHT1		

SH2 HORIZ SYNC — 74LS32 A29 — A23 74LS04 — HORIZ SYNC B SH4; HORIZ SYNC SH4

SH2 DISP EN — DEL DISP EN SH4

SH2 CURSOR — DEL CURSOR SH4

HALF INTENSITY SH4

ATT BLK SH4

CHAD7

ATTRIBUTE

RP1 4.7K +5V

A46 74LS08 — A47 74LS02 — A40 1/2 74 S74 — A41 A42 74LS174

SH1 Ø1 — UNDERLINE SH4; REV VIDEO SH4; BLINK SH4; BLANK SH4

BLANK — A35 74LS32 — A47 74LS02

DC CARRY

SHIFT CLOCK

SH2 D0' D1' D2' D3' D4' D5' D6' D7' — A43 74LS374

CHAD0 CHAD1 CHAD2 CHAD3 CHAD4 CHAD5 CHAD6 — A48 2332

A49 74LS166 — DOT SERIAL SH4

RP1 4.7K

RP4 1K

A15 74LS163 — A23 74LS04 — A28 74LS10 — A47 74LS02 — SET DISP RAM SH1

CHAR CLK SH1,2

CHAR CLK SH1

A22 74S04

Y2 XTAL 13.608 MHZ — C30 10pF — R23 330 — R24 750 — R17 1.8K — R18 470

SH2 RA0 RA1 RA2 — CHARACTER SET SELECT — E4 E5 E6 E7

SH2 RA3 — A46 74LS08 — A35 74LS32

BIT Ø SH5

BIT 1 SH5

ROW 1Ø SH2,4

RAØ SH4

B600011-00

APPLICATION		UNLESS OTHERWISE NOTED	OWN	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	TITLE PCB SCHEMATIC CONT BD SIO
		ANG ± PLC ± PLC ±	ENGR	
		SCALE NONE	APPD	SIZE D SHT OF 3 DRAWING NO 2014300 REV B1
		MATERIAL	FINISH	

B1 2014300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	SEE SHT 1		

SH3 HORIZ SYNC B
SH3 RAO
SH3 BLINK
SH4 BLINK CLK
SH3 BLANK
SH3 DOT SERIAL
SH3 ROW 10
SH3 UNDERLINE
SH3 DEL CURSOR
SH3 REV VIDEO
SH5 BOW/WOB
SH3 DEL DISP EN
SH3 ATT BLK
SH3 HALF INTENSITY
SH3 HORIZ SYNC
SH2 VERT SYNC

A34 74LS00 · A28 74LS10 · A22 74S04 · A13 74LS00 · A13 74LS00 · A14 74LS86 · A34 74LS00 · A14 74LS86 · A14 74LS86 · A12 7406 · A13 74LS00 · A12 7406 · A13 74LS00 · A21 74LS08 · A12 7406 · A22 74S04 · A14 74LS86 · A12 7406

HORIZ SYNC → P2-1

+5V
R2 22
C2 4.7µF
R4 750
R5 1K
R7 1K
R6 68
R3 270
R27 1K
CR3 1N914
Q2 2N2219
E10 E11 E12 E13

VIDEO SHIELDGND → P2-3
VIDEO → P2-4
COMP V + TTL VIDEO → P2-6
VERT SYNC → P2-5
VERT SYNC / IRQ → SH1

RP1 4.7K +5V
A40 74S74

SH1 RESET IRQ 8X4X
SH5 DATA RDY
SH1 8X5X RESET NMI

RP4 1K +5V
A7 74LS74

NMI → SH1
DTR → SH5

DTR · +5V · 4.7K
A5 75189 · SW2 · C5 C7 C6 C8 330pf

P4-20 DTR
P3-3 RxD
P6-3 RxD
P3-5 CTS
P3-8 DCD 12
P3-6 DSR 13
E14 E15 E16

74LS00 · A9 · +12V · A10 75188 · -12V

TxD MODEM → P6-2
TxD → P3-2
RTS → P3-4
DTR E17 E18 E19 SERIAL DATA, PRINTER → P4-3
DTR EN 10 S2 → P3-20

SH1 SEL ACIA (8X3X)
SH1 R/W
SH1 Ø2
SH1 AØ
SH1 A1
SH1,2,5 DØ D1 D2 D3 D4 D5 D6 D7

ACIA 6551A-1 A19
+5V RP1 4.7K
Y1 1.8432 MHZ

IRQ (ACIA) → SH1
RxC → P6-12

SH1 SYS RESET
SH1 CONTROL LATCH

74LS174 A18

BELL · EXT · SPARE

+5V R16 68 · R20 330 · R19 330 · Q1 2N2219 · A21 74LS08

P7-2 SPEAKER
P7-1
BLINK CLK → SH4
60HZ /50HZ → SH2
CURSOR = UNDERLINE → SH2

SH3 ROW 10 (1620 HZ)
P6-13

B600C11-00

APPLICATION		UNLESS OTHERWISE NOTED	DWN mwy 4.9.81	TeleVideo, Inc. SYS
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG 2 PLC 3 PLC	ENGR	TITLE PCB SCHEMATIC CONT BD 910
		SCALE	APPD	
		MATERIAL	FINISH	SIZE D · SHT 4 OF 5 · DRAWING NO 22 4300 · REV B1

B 2014300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	SEE SHT1		

SH1 CHAR SET SEL RD 8X1X
SH1 DIPSWITCH PORT # 2 9XX2
SH1 DIPSWITCH PORT # 1 9XX1
SH1 KYBD PORT # 1 8X6X
SH1 KYBD PORT # 2 8X7X

RP4 1K
A12 7406
P1-4 SHIFT
P1-6 CONTROL
+5V
A1 AY-5-3600 KR-3600
P1-20 P1-16 P1-21 P1-17 P1-22 P1-18 P1-23 P1-19 P1-26 P1-8 P1-9 P1-10 P1-11 P1-12 P1-13 P1-14 P1-15
RDY
-12V
B1 B2 B3 B4 B5 B6 B7 B8 B9
C35 20pf
FREQ CONT
RZ5 100K
LO/RO DELAY
R26 1K
C32 0.039 µF
RP4 1K
SH4 DTR
P1-5 FUNC KEY
P1-3 ALPHA LOCK KEY

A2 2716
E23 E25 E27 E29 E31 E33 E35 E37 E24 E26 E28 E30 E32 E34 E36 E38

A3 A8 A6 A11 74LS367

DATA RDY SH4
D7 D6 D5 D4 D3 D2 D1 D0 SH1,2,4

RP2 1K
S1
1 BD RT3
2 BD RT2
3 BD RT1
4 BD RTØ
5 WD LNGTH
6 PAR
7 O/E
8 STP BITS
9 TCHAR1
1Ø
TCHARØ
R1 1K

S2
1 EM1
2 EMØ
3 50/60
4 CURSOR
5 CURSOR
6 F/HDX
7 BOW/WOB
RP3 1K

SH3 BITØ
SH3 BIT1
BOW/WOB SH4

NOTE:
P6 IS A 14- OR 16-PIN DIP SOCKET FOR OPTION BOARD CONNECTION. * PINS Ø & 15 ARE PINS 1 & 16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

+12V → P6-1, P6-14
-12V → P6-5, P6-10
+5V → P6-6, P6-9, P6-7, P6-8

*P6-15 → RxD+ → P3-12
*P6-Ø → RxD- → P3-24
P3-25 → TxD+ → P6-11
P3-13 → TxD- → P6-4
CURRENT LOOP COMM (OPTIONAL)

P1-1 P1-2 P3-1 P3-7 P4-1 P4-7

3600011-00

APPLICATION		UNLESS OTHERWISE NOTED	DWN	TeleVideo, Inc. 575
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG 2 PLC 3 PLC	ENGR	TITLE: PCB SCHEMATIC CONT BD 910
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D, SHT 5 OF 5, DRAWING NO 2014300, REV B1

B1 2014300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD RELEASE		
	B	PROD RELEASE PER ECO 82,116		
	B1	PROD RELEASE PER ECO 123,162,165,204,212		
	B2	REISSUED ECO 281		
	B3	REISSUED ECO 302		
	B4	REISSUED ECO 383	7/27/82	

DWG NO 2014302 SH 1 REV B4

B600011-003

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG ± 2 PLC ± 3 PLC

SCALE: X

MATERIAL

DWN

CHK

ENGR

APPD

APPD

APPD

FINISH X

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS, INC. AND CONTAINS INFORMATION WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO. NO PART OF THIS DOCUMENT MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS INC.

TeleVideo, Inc. 57

TITLE PCB SCHEMATIC CONTROL BD 910 PLUS

SIZE D | SHT 1 OF 5 | DRAWING NO. 2014302 | REV B4

BISHOP GRAPHICS ACCUPRESS REORDER NO. A17366 P0000809-001 REV A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	E4	SHEET 1		

CURSOR SH3
RA0 SH3
RA1 SH3
RA2 SH3
RA3 SH3
DISP EN SH3
HORIZ SYNC SH3
VERT SYNC SH4

SH3: D0' D1' D2' D3' D4' D5' D6' D7'

DISP RAM WR
OEM OPT
DISP RAM SEL
R/W
CURSOR=UNDERLINE
4C00-43FF
4400-47FF
74LS00 74LS04 74LS32 74LS10 74LS157 74LS245 74LS374 74LS545 74LS138 2114 6116
A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31 A32 A33 A34 A35 A36 A37 A44
E21 E22 E39 E40 E41
+5V
GND
R15 1K
MAP CLK
CE
RE
A26
PROTECT
ADDR SEL
MA0 MA1 MA2 MA3 MA5 MA6 MA7 MA8 MA9 MA10
RS
DISPRAM
DIR
P5-5 +12V
P5-1 -12V
P5-4 +5V
P5-3 GND
C3 22µf ELEC
C37 22µf ELEC
C20 22µf ELEC
C33 0.01µf CER
0.1µf CER
ALL CAPS NOT SHOWN

* - OPTIONAL CHIP

B600011-003

APPLICATION		UNLESS OTHERWISE NOTED	DWN Lange 4-8-81	TeleVideo, Inc. 977
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK 505-4	
		ANG 2 PLC 3 PLC	ENGR	TITLE PCB SCHEMATIC CONTROL BD 910 PLUS
			APPD 5/5/81	
		SCALE: NONE	APPD	
		MATERIAL	APPD	SIZE D SHT 2 OF 5 DRAWING NO. 2014302 REV 84
			FINISH	

BISHOP GRAPHICS ACCUPRESS REORDER NO. A11670

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B4	SEE SHT1		

HORIZ SYNC B — SH4
HORIZ SYNC — SH4
DEL DISP EN — SH4
DEL CURSOR — SH4
HALF INTENSITY — SH4
ATT BLK — SH4
UNDERLINE — SH4
REV VIDEO — SH4
BLINK — SH4
BLANK — SH4
DOT SERIAL — SH4
SET DISP RAM — SH1
CHAR CLK — SH1,2
CHAR CLK — SH1
BIT 2 — SH5
BIT 1 — SH5
ROW 10 — SH2,4
RA0 — SH4

SH2 HORIZ SYNC
SH2 DISP EN
SH2 CURSOR
SH1 A1
SH2 DA0
SH2 DA1
SH2 DA2
SH2 DA3

CHAD7
ATTRIBUTE
CHAD0
CHAD1
CHAD2
CHAD3
CHAD4
CHAD5
CHAD6

A41 74LS174
A42 74LS174
A40 74S174
A43 74LS374
A48 2332
A49 74LS166
A15 74LS163
A46 74LS08
A47 74LS02
A48 74LS08
A35 74LS32
A33
A27 74LS32
A23 74LS04
A22 74S04
A28 74LS10

RP1 4.7K
RP4 1K
HALF TEK SOFT SELECT
E4
E5
E6
E7

Y2 XTAL 13.608 MHZ
C30 10pf
RZ3 330
RZ4 750
R17 1.8K
R18 470

DC CARRY
SHIFT CLOCK

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± PLC .X ± PLC .XX ± PLC .XXX ± PLC
SCALE NONE
MATERIAL
FINISH

DRWN
CHK
ENGR
APPD 5/24/90
APPD
APPD

TeleVideo, Inc. SYS

TITLE
PCB SCHEMATIC
CONTROL BD 910 PLUS

SIZE D | SHT 3 OF 3 | DRAWING NO 2014302 | REV B4

B4 2014302

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B4	SEE SHT 1		

HORIZ SYNC
RA0
BLINK
BLINK CLK
BLANK
DOT SERIAL
ROW 10
UNDERLINE
DEL CURSOR
REV VIDEO
BOW/WOB
DEL DISP EN
ATT BLK
HALF INTENSITY
HORIZ SYNC
VERT SYNC

A24 74LS00 · A28 74LS10 · A22 74S04 · A13 74LS00 · A13 74LS00 · A34 74LS00 · A14 74LS86 · A14 74LS86 · A14 74LS86 · A12 7406 · A13 74LS00 · A12 7406 · A13 74LS00 · A21 74LS08 · A12 7406 · A22 74S04 · A14 74LS86 · A12 7406

HORIZ SYNC → P2-1
+5V · R2 22 · C2 4.7µF
VIDEO SHIELDGND → P2-3
R4 750 · R5 1K · R7 1K · R6 68 · R3 270 · R27 1K · CR3 IN914 · Q2 2N2219
E10 E11 E12 E13
VIDEO → P2-4
COMP V + TTL VIDEO → P2-6
VERT SYNC → P2-5
VERT SYNC / IRQ
SH1

RP1 4.7K · +5V · A40 74S74 · RESET IRQ 8X4X · DATA RDY · 8X5X RESET NMI

RP4 1K · +5V · A7 74LS74
NMI → SH1
DTR → SH5

DTR · +5V · 4.7K · A5 75189 · C5 C7 C6 C8 330pf
P4-20 DTR
P3-3 RxD
P6-3 RxD
P3-5 CTS
P3-8 DCD 12
P3-6 DSR 13
SW2 · E14 E15 E16

74LS00 · A9 · +12V · A10 75188 · -12V · A9 74LS00
TxD MODEM → P6-2
TxD → P3-2
RTS → P3-4
DTR · E17 E18 E19
SERIAL DATA, PRINTER → P4-3
DTR EN 10 · S2
P3-20

SEL ACIA (8X3X) · R/W · Ø2 · AØ · A1 · DØ D1 D2 D3 D4 D5 D6 D7 (SH1,2,5)
ACIA 6551A-1 (A19) · RPI 4.7K · Y1 1.8432 MHZ
IRQ (ACIA) → SH1
RxC → P6-12

SYS RESET
CONTROL LATCH
A18 74LS174 · BELL · EXT · SPARE
+5V · R16 68 · R20 330 · R19 330 · A21 74LS08 · Q1 2N2219
P7-2 SPEAKER
P7-1
BLINK CLK → SH4
60HZ /50HZ → SH2
CURSOR=UNDERLINE → SH2

ROW 10 (1620 HZ) → SH3
P6-13

B600011-003

APPLICATION		UNLESS OTHERWISE NOTED	DWN 4-9-81	TeleVideo Inc. 579
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± PLC .3 PLC	ENGR	TITLE: PCB SCHEMATIC CONTROL BD 910 PLUS
			APPD	
		SCALE: 8/11/15	APPD	
		MATERIAL	FINISH	SIZE D · SHT 4 OF 5 · DRAWING NO. 2014302 · REV B4

BISHOP GRAPHICS ACCUPRESS REORDER NO A11670

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B4	RELEASE SHT 1		

SH1 CHAR SET SEL RD 8XXX
SH1 DIPSWITCH PORT # 2 9XX2
SH1 DIPSWITCH PORT # 1 9XX1
SH1 KYBD PORT #1 9X0X
SH1 KYBD PORT #2 9X7X

DATA RDY SH4

SH1,2,4: D7 D6 D5 D4 D3 D2 D1 D0

RP4 1K ×9 — +5V
P1-4 SHIFT
P1-6 CONTROL
A12 7406
A1 AY-5-3600 / KR-3600
P1-20 P1-16 P1-21 P1-17 P1-22 P1-18 P1-23 P1-19 P1-26 P1-8 P1-9 P1-10 P1-11 P1-12 P1-13 P1-14 P1-15
FREQ CONT: C35 20pf, R25 100K
LO/RO DELAY GND
R26 1K, C32 0.039 mf
RP4 1K ×2

SH4 DTR
P1-5 FUNC KEY
P1-3 ALPHALOCK KEY

A2 2716 — -12V
E23 E24 E25 E26 E27 E28 E29 E30 E31 E32 E33 E34 E35 E36 E37 E38

A8 74LS367 — D7 D6 D5 D4 D3 D2 D1 D0

S1: 1 BD RT3, 2 BD RT2, 3 BD RT1, 4 BD RT0, 5 WD LNGTH, 6 PAR, 7 O/E, 8 STP BITS, 9 TCHAR1, 10
RP2 1K ×8
TCHAR0
R1 1K

A11 74LS367 — D3 D2 D1 D0 D4 D5
A6 74LS367 — D0 D7 D1 D0 D2 D3
A52 74LS367 — D4 D5 D6 D7 D0 D1

S2: 1 EM1, 2 EM0, 3 50/60, 4 CURSOR, 5 CURSOR, 6 F/HDX, 7 BOW/WOB
RP3 1K ×8

BOW/WOB SH4

SH3 BIT 0
SH3 BIT 1

P1-1 P1-2 P3-1 P3-7 P4-1 P4-7

NOTE:
P6 IS A 14- OR 16-PIN DIP SOCKET FOR OPTION BOARD CONNECTION. * PINS 0 & 15 ARE PINS 1 & 16 IF A 16-PIN SOCKET IS INSTALLED FOR P6.

+12V → P6-1, P6-14
-12V → P6-5, P6-10
+5V → P6-6, P6-9, P6-7, P6-8

*P6-15 → RxD+ → P3-12
*P6-0 → RxD- → P3-24
P3-25 → TxD+ → P6-11
P3-13 → TxD- → P6-4
CURRENT LOOP COMM (OPTIONAL)

E80011-003

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN	TeleVideo, Inc. 579A
NEXT ASSY	USED ON	ANG ± PLC .X PLC	CHK	
			ENGR	TITLE: PCB SCHEMATIC
		SCALE	APPD	CONTROL BD 910 PLUS
		MATERIAL	APPD	
			APPD	SIZE D — SHT 5 OF 5 — DRAWING NO. 2014302 — REV B4

BISHOP GRAPHICS ACCUPRESS REORDER NO. A1167

2014302

NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACTOR ARE VALUED IN MICOFARADS ±10% AND ARE 50 VDC.
3. DRAWINGS COMFORM WITH TELEVIDEO SPEC. NO S000000-001.
4. THIS SCHEMATIC ALSO USED FOR CONTROL BD 910 + G/A.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 249		3/4/82
	A2	PROD REL PER ECO 0379		
	A3	PROD REL PER ECO 0400		
	A4	PROD REL PER ECO 0516, 0521, 0529		
	A5	REVISED PER ECO 3001		

A27 6502A
A28 74LS08
A29 74LS00
A21 74S04
A30 74LS139
A38 2532
A32 2114
A31 2114
A34 74LS32
A37 74LS138
A4 555
A7 7406
R28 1K
R25 4.7K
R24 4.7K
R7 47K
R6 3.3K
R8 1M
C4 0.1uf
C5 10uf 16V
C6 0.01uf
C9 0.01uf
CR1 IN914
RP2 4.7K

SH3 CHAR CLK
SH4 NMI
SH4 VERT SYNC/IRQ
SH4 IRQ (ACIA)
SH3 Ø2·W
SH3 DISP RAM

PII-20
SH2,3,4 R/W
SH2,3,4 Ø2
SH2,3 Ø1
SH2,4,5 D0-D7

CONTROL LATCH SH4
DIPSWITCH PORT #1 SH5
DIPSWITCH PORT #2 SH5
4000-7FFF SH3
DISP RAM WR SH2
SYS RESET SH4

PII-4 CHAR SET SEL RB SH5
SEL CRTC SH2
SEL ACIA SH4
RESET IRQ SH4
RESET NMI SH4
KYBD PORT #1 SH5
KYBD PORT #2 SH5

SH2,4 A0
PII-3 A1
SH2,4 A2
PII-5 A3
SH2 A4
PII-7 A5
SH2 A6
PII-8 A7
A8
A9
A10

SH2

B600011-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H. Hus 1-11-82
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK 3/4/82
2014405	—	ANG ± 2 PLC ± 3 PLC ±	ENGR 3/4/82
		SCALE NONE	APPD
		MATERIAL	APPD
			FINISH

TeleVideo, Inc. 950
TITLE: PCB SCHEMATIC CONT BD 910 G/A
SIZE D | SHT 1 OF 5 | DRAWING NO. 2014301 | REV A5

2014301 A5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A5	SEE SHT 1		

+5V
20 VCC
19 CURSOR
38 RAØ
37 RA1
36 RA2
35 RA3
18 DISPEN
39 HORZSYNC
40 VERTSYNC
3 PROG SEL
21 CCLK
22 R/W
23 Ø2(E)
25 CS
2 RES
A20 6545A-1 CRTC
24 RS
1 GND

SH5 60HZ/50HZ
SH3 CHAR CLK
SH1 R/W
SH1 Ø2
SH1 SEL CTRC 8X2X
+5V R13 4.7K

CURSOR
RAØ
RA1
RA2
RA3
DISP EN
HORIZ SYNC
VERT SYNC
SH3
SH3,4
P11-22
P11-23

SH1,4,5 DØ D1 D2 D3 D4 D5 D6 D7
33 DØ
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7

A19 74LS157 SEL.B VCC GND G
AØ MAØ
A1 MA1
A2 MA2
A3 MA3

A23 74LS157 SEL.B VCC GND G
A4 MA4
A5 MA5
A6 MA6
A7 MA7

A26 74LS157 SEL.B VCC GND G
MA8
MA9
MA10
A8
A9
A10

AØ' A1' A2' A3' A4' A5' A6' A7' A8' A9' A10'

A13 6116
OE CS VCC R/W GND
AØ A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
DØ D1 D2 D3 D4 D5 D6 D7
DØ' D1' D2' D3' D4' D5' D6' D7'
SH3

A14 74LS245 DIR G VCC GND
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
A1 A2 A3 A4 A5 A6 A7 A8

A35 74LS04

SH1 AØ A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 Ø1
SH1 PAGE ONE
SH3 Ø2.W
SH1 DISP RAM WR
SH3 DISP RAM

P5-5 +12V → +12V
P5-1 -12V → -12V
P5-4 +5V → +5V
P5-3 GND → GND
C3 22uF ELEC
C2 22uF ELEC
C7 22uF ELEC
C1~C13 0.1uF CER
C20 10uf 25V
ALL CAPS NOT SHOWN

+5V
+12V
-12V
P6-6 P6-9 P11-1 P11-2
P6-1 P6-14 P11-6
P6-5 P6-10 P11-14

NOTE: P6 IS A14 - OR 16 - PIN DIP SOCKET FOR OPTION BOARD CONNECTION. *PINS 0 & 15 ARE PINS 1 & 16 IF A16 - PIN SOCKET IS INSTALLED FOR P6.

E33 → P11-25
* P6-15 RXD+ → P3-12
* P6-Ø RXD- → P3-24
P3-25 TXD+ → P6-11
P3-13 TXD- → P6-4
CURRENT LOOP COMM (OPTIONAL)

B600011-002

APPLICATION		UNLESS OTHERWISE NOTED	DWN H. Hwr 12-31-81	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK J. Cassida 7/1/82	
2014405	—	ANG 2 PLC 3 PLC	ENG	TITLE
			APPD	PCB SCHEMATIC
		SCALE: NONE	APPD	CONT BD 910 G/A
		MATERIAL	FINISH	SIZE D SHT 2 OF 5 DRAWING NO. 2014301 REV A5

A5 2014301

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A11670

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A6	SEE SHT 1		

74LS32 A34

SH2 HORIZ SYNC

HORIZ SYNC B SH 4

SH1 SYS RESET
SH2 CURSOR
SH2 DISP EN.
SH2 VERT. SYNC.
SH1 R/W
SH1 Ø1
SH1 Ø2
SH1 4000-7FFF
SH4 BLINK CLOCK
SH5 BOW/WOB
SH4 CURSOR = BLOCK
SH2 RA3

+5V

A22 GATE ARRAY 70200-11B

H SYNC, VDD, SYS.RST, CURSOR IN, DISP EN., VERT.SYNC, R/W, Ø1, Ø2, 4000-7FFF, BLINK CLK, BOW/WOB, CURSOR=BLOCK, CHAD 7, RA3, RAØ, RA1, RA2, CHAD3, CHAD2, CHAD1, CHADØ, DOT 925 910 PG, SER 930 925 2 DCCLK DR ATT., SH. SET, VSS, PG.ONE, PG.TWO, DISP.RAM, Ø2·W, ROW 10, VIDEO, HALF INT., COMP.VID, L/P ATT.

PAGE ONE SH 2
DISP. RAM SH1,2
Ø2·W SH1,2
ROW 10 SH 4
VIDEO SH 4 → P11-17
HALF INTENSITY SH 4 → P11-26
COMPOSITE VIDEO SH 4

+5V RP4 4.7K E35 E34

SET DISP RAM
DC CARRY
SHIFT CLOCK → P11-21

→ P3-1
→ P4-1

+5V RP3 4.7K

A12 74LS374 (VCC CLK DØ D7 D2 D5 D3 D4 GND OE → QØ Q7 Q1 Q6 Q2 Q5 Q3 Q4)

SH2 DØ′ D1′ D2′ D3′ D4′ D5′ D6′ D7′

A17 2332 (A3 A4 A5 A6 A7 A8 A9 A10 A11 CS2 GND)

CHADØ CHAD1 CHAD2 CHAD3 CHAD4 CHAD5 CHAD6

A18 74LS166 (PE MR VCC CP DØ D1 D2 D3 D4 D5 D6 D7 → QH, CE, DS GND)

SH2 RAØ RA1 RA2

+5V RP3 4.7K E4 E5 E6 E7

Y2 XTAL 13.608 MHZ C18 10pf R17 330 R14 750 R16 470 R15 1.8K

74S04 A21 ×4

A25 TC 74LS163 (VCC CK LD D P T CL A B C QA QB QC QD GND)

E36 E37

A21 74S04 → A24 74LS02 → A29 74LS00 → CHAR CLK SH1

→ P1-1
→ P1-2
→ P3-7
→ P4-7
→ P6-7
→ P6-8
→ P11-9
→ P11-19

74LS02 A24 (12 11 → 13 4 → 5)
A28 74LS08 (6)
W1 W2
A29 74LS00 (4 5 → 6)
A35 74LS04 (13 → 12)

BIT Ø SH 5
BIT 1 SH 5

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H. Huc 1-4-82
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC	CHK
2014805	—		ENGR
			APPD
		SCALE: NONE	APPD
		MATERIAL	APPD
			FINISH

B600011-002

TeleVideo, Inc.

TITLE: PCB SCHEMATIC CONT BD 910 G/A

SIZE D | SHT 3 OF 5 | DRAWING NO. 2014301 | REV A5

2014301 A5

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A11670

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A5	SEE SHT 1		

SH3 HORIZ SYNC B
SH2 VERT SYNC
SH1 RESET IRQ 8X4X
SH3 VIDEO
SH3 HALF INTENSITY
SH3 COMPOSITE VIDEO
SH5 DATA RDY
SH1 8X5X RESET NMI
P10-8
P10-9
P10-5
P4-20 DTR
P3-3 RXD
P6-3 RXD
P3-5 CTS
P3-8 DCD
P3-6 DSR
SH1 SEL ACIA (8X3X)
R/W
Ø2
AØ
A1
DØ
D1
D2
D3
SH1,2,5 D4
D5
D6
D7
SH1 SYS RESET
SH1 CONTROL LATCH
SH3 ROW 10 (1620 HZ)
P6-13

A21 74S04
4.7K RP4 +5V
A36 74S74
R19 22 +5V
C19 4.7uF
R21 750
R20 1K
R23 1K
R22 270
E10 E11
CR2 IN914
E12 E13
Q2 2N2219
R27 10K
R26 33
A7 7406
E38 E39
E40 E41
E42 E43
A16 74LS74
RP3 4.7K +5V
A7 7406
RP4 4.7K +5V
A10 75189
SW2
E14 E15 E16
330pf
A15 ACIA 6551A-1
A29 74LS00
RP4 4.7K
Y1 1.842 MHZ
A9 75188
+12V -12V
C10 C17 330pf
C11 C12 330pf
E17 E18 E19
A11 74LS174
A28 74LS08
Q1 2N2219
R3 68
R4 330
R5 330
A7 7406
R18 4.7K +5V CURSOR = BLOCK

P2-1 HORZ SYNC
P2-5 VERT SYNC
SH1 VERT SYNC/IRQ
P2-3 VIDEO SHIELD GND
P2-4 VIDEO
P2-6 COMP V + TTL VIDEO
P10-10
P10-11
P10-7
SH1 NMI
SH5 DTR
P6-2 TXD MODEM
P3-2 TXD
P3-4 RTS
P4-3 SERIAL DATA, PRINTER
P3-20 DTR EN
SH1 IRQ (ACIA)
P6-12 RXC
P10-13
P10-4
P10-6
P10-2
P10-12
P7-2 SPEAKER
P7-1
SH3 BLINK CLK
SH3

BELL
EXT
SPARE

APPLICATION		UNLESS OTHERWISE NOTED	DWN H.H. 1-4-82
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK J. Lewis 2/8/82
2014405	—	ANG 2 PLC 3 PLC	ENGR
			APPD
		SCALE: NONE	APPD
		MATERIAL	APPD
			FINISH

B600011-002
TeleVideo, Inc. 583
TITLE: PCB SCHEMATIC CONT BD 910 G/A
SIZE D | SHT 4 OF 5 | DRAWING NO. 2014301 | REV A5

2014301 A5

BISHOP GRAPHICS ACCUPRESS RECORDER NO. A1870

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A5	SEE SHT 1		

SH1 — CHAR SET SEL RD 8X1X
SH1 — DIPSWITCH PORT #2 9XX2
SH1 — DIPSWITCH PORT #1 9XX1

DATA RDY → SH4

P1-4
P1-6
P1-20
P1-16
P1-21
P1-17
P1-22
P1-18
P1-23
P1-19
P1-26
P1-8
P1-9
P1-10
P1-11
P1-12
P1-13
P1-14
P1-15

A1 AV-5-3600 / KR-3600

SH4 DTR
P1-5 FUNC KEY
P1-3 ALPHALOCK KEY
SH1 KYBD PORT #1 8X6X
SH1 KYBD PORT #2 8X7X

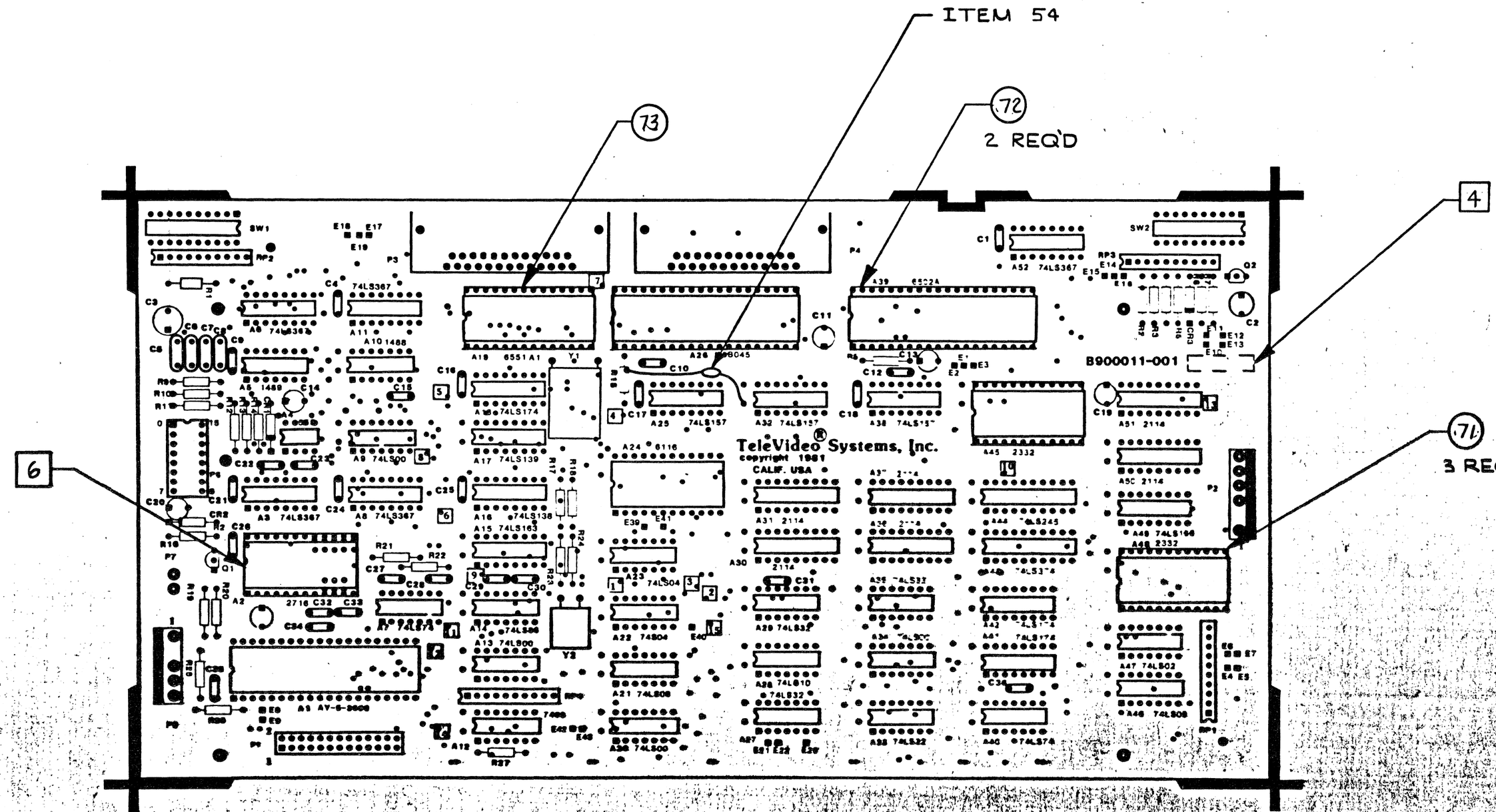
SH3 BIT Ø
SH3 BIT 1

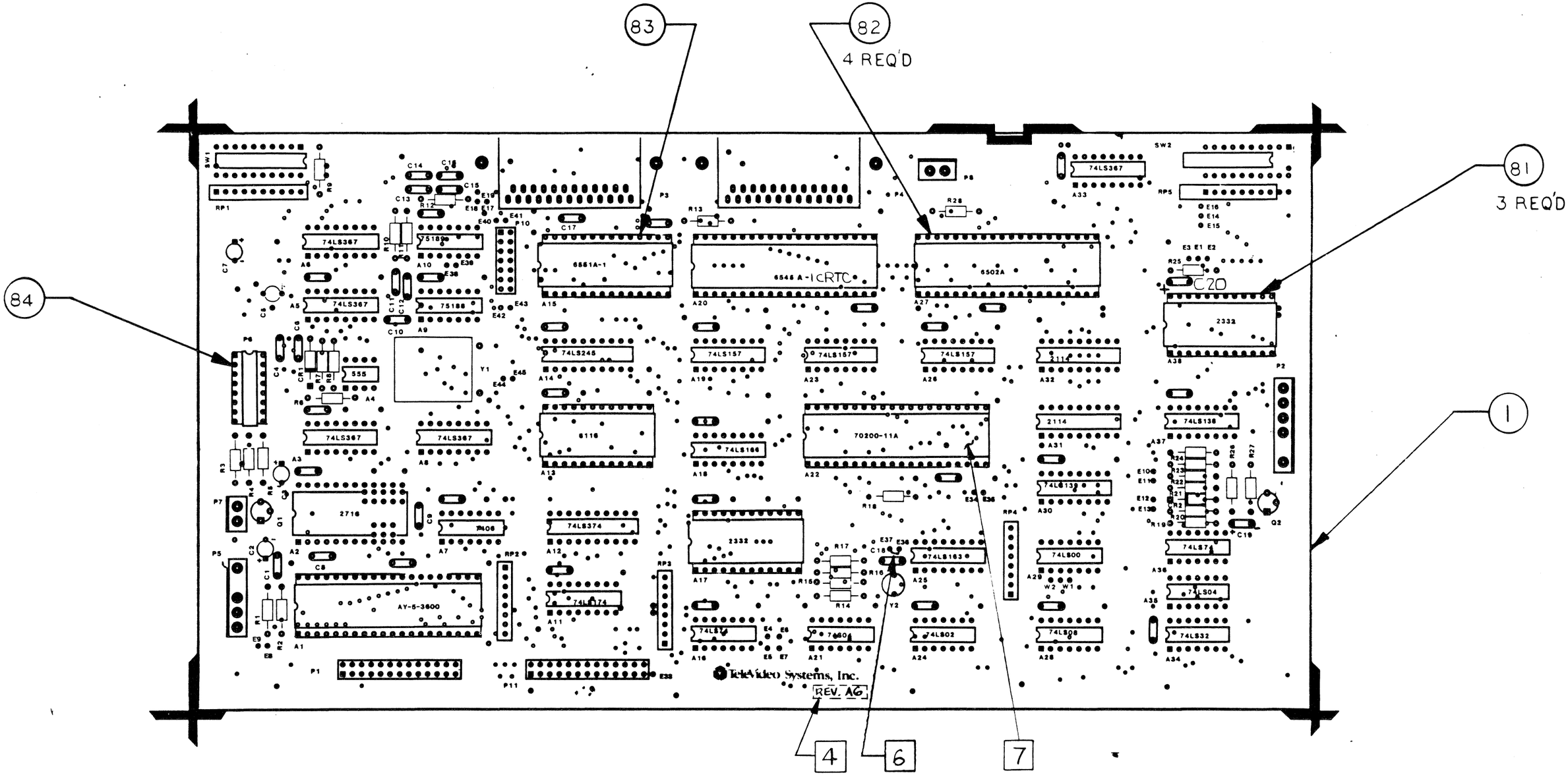
P11-13
P11-12
P11-11
P11-10
P11-16
P11-15
P11-18
P11-24

50/60 HZ → SH 2
BOW/WOB → SH4
D7
D6
D5
D4
D3
D2
D1
DØ
SH1,2,4

B600011-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG 2 PLC 3 PLC	DWN H. Hurl 6-82	TeleVideo, Inc. S84
NEXT ASSY	USED ON		CHK	
2014405	—		ENG	TITLE PCB SCHEMATIC CONT BD 910 G/A
			APPD	
		SCALE: NONE	APPD	
		MATERIAL —	FINISH —	SIZE D SHT 5 OF 5 DRAWING NO 2014301 REV A5


ITEM 54
73
72
2 REQ'D
4
6
71
3 REQ'D
B900011-001
TeleVideo® Systems, Inc.
copyright 1981
CALIF. USA


83
82
4 REQ'D
81
3 REQ'D
84
1
4
6
7
74LS367
74LS245
74LS157
74LS138
74LS00
74LS04
74LS32
74LS08
74LS02
74LS374
74LS163
74LS86
74LS367
555
2716
AY-5-3600
6116
2332
2114
6561A-1
6545A-1 CRTC
6502A
70200-11A
TeleVideo Systems, Inc.
REV. A6

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
1												
2	1									A40	IC 74S74	2026400
3	1									A4	IC NE 555	2030200
4	1									A39	IC 6502A Micro	2049600
5	1									A17	IC 74LS139	2027200
6	1									A16	IC 74LS138	2041000
7	1									A45	IC EP 32K 350ns Sys Prg 910	8000020
8	1									A48	IC ROM 32K 450ns Char Gen	8000016
											910	
9	1									A44	IC 74LS245	2036200
10	2									A50,51	IC 2114ICB RAM	2035800
11	1									A24	IC 6116 RAM 150ns	2049200
12	1									A43	IC 74LS374	2029000
13	1									A49	IC 74LS166	2027800
14	1									A1	IC Encoder Kybd 910	2051800
15	5									A3,5,8,11,52	IC 74LS367	2028600
16	1									A7	IC 74LS74 (TI,SIG)	2026600
17	1									A5	IC 75189AN	2029400
18	1									A10	IC 75188N	2029200
19	1									A19	IC SY6551A-1 2MHz(SYN,AMI)	2053000
20	2									A18,41	IC 74LS174	2028200

NOTES:

TITLE: PCB ASSY CONTROL BOARD 910

DATE: 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
21	3									A9,13,34	IC 74LS00	2024200
22	2									A21,46	IC 74LS08	2025200
23	3									A29,33,35	IC 74LS32	2025800
24	1									A28	IC 74LS10	2025400
25	1									A47	IC 74LS02	2041600
26	1									A14	IC 74LS86	2026800
27	1									A23	IC 74LS04	2024800
28	1									A22	IC 74S04	2024600
29	1									A12	IC 7406	2034800
30	1									A15	IC 74LS163	2027600
31	1									A26	IC 68B045 CRT Contr/ROM	2052600
											2MHz	
32	3									A25,32,38	IC 74LS157	2027400
33	1									A42	IC 74S174	2044600
34	1									R13	Res CF 3.3K .25W 5%	2052700
35	4									R9,10,11,22	Res CF 4.7K .25W 5%	2053100
36	1									R14	Res CF 47K .25W 5%	2033700
37	1									R12	Res CF 1M .25W 5%	2031500
38	1									R25	Res CF 100K .25W 5%	2032100
39	1									R3	Res CF 270 .25W 5%	2051300
40	2									R4,24	Res CF 750 .25W 5%	2031700

NOTES:

TITLE PCB ASSY CONTROL BOARD 910

DATE 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
41	8									R1,5,7,8,15,21,	Res CF 1K .25W 5%	2052100
										26,27		
42												
43	1									R2	Res CF 22 .25W 5%	2033500
44	2									R6,16	Res CF 66 .25W 5%	2051100
45	3									R19,20,23	Res CF 330 .25W 5%	2051500
46	1									R18	Res CF 470 .25W 5%	2051700
47	1									R17	Res CF 1.8K .25W 5%	2052300
48	3									RP2,3,4	Res Pk 1K 10P SIP	2040500
49	1									RP1	Res Pk 4.7K 10P SIP	2041300
50	1									C30	Cap Mica 10pf	2024100
51	3									C3,20,37	Cap Elect 22uf 15V	2025700
52	1									C14	Cap Elect 10uf 16V 20%	2027300
53	3									C22,23,28	Cap Cer .01uf	2028700
54	1										Cap Tant 10uf 25V 10%	2027100
55	1									C35	Cap Mica 20pf	2024300
56	1									C32	Cap Mono .039uf 50V 10%	2030300
57	4									C2,11,13,19	Cap Tant 4.7uf 16V 10%	2027500
58	4									C5-8	Cap Cer 330pf 50V 20%	2029100
59	19									Unmarked	Cap Cer .1uf 50V 10%	2030100
60	2									CR1,3	Diode IN914	2047500

NOTES:

TITLE PCB ASSY CONTROL BOARD 910

DATE 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
61												
62	2									Q1,2	Tran 2N4401 NPN/Silicon	2045500
63												
64												
65	1									Y2	Cry 13.608 MHz	2098605
66	1									Y1	Cry 1.8432 MHz	2098602
67												
68												
69	2									S1,2	SW 10 Pos DIP/20P Sid Adj	2096800
70												
71	3									X(A2),45,48,24	Socket IC DIP 24P	2098401
72	3									XA1,26,39	Socket IC DIP 40P	2098402
73	1									XA19	Socket IC DIP 28P	2098404
74												
75	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
76	1									P1	Plug 26P RT 3	2098701
77	2									P2,5	Plug 5P STR Waf	2098802
78	1									P7	Plug 2P STR Waf	2098800
79												
80												

NOTES:

TITLE PCB ASSY CONTROL BOARD 910

DATE 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
1												
2												
3												
4												
5	1									A4	IC NE 555	2030200
6	1									A27	IC 6502A Micro	2049600
7	1									A30	IC 74LS139	2027200
8	1									A37	IC 74LS138	2041000
9	1									A38	IC EP 32K 350ns Sys Prg 910	8000020
10	1									A17	IC ROM 450ns Char Gen 910	8000016
11	1									A14	IC 74LS245	2036200
12	2									A31,32	IC 2114 ICB RAM	2035800
13	1									A13	IC 6116 RAM 150ns	2049200
14	1									A12	IC 74LS374	2029000
15	1									A18	IC 74LS166	2027800
16	1									A1	IC Encoder Kybd 910	2051800
17	5									A3,5,6,8,33	IC 74LS367	2028600
18	2									A16,36	IC 74LS74	2026600
19	1									A10	IC 75189AN	2029400
20	1									A9	IC 75188N	2029200
21	1									A15	IC SY6551A-1 UART 2MHz	2053000

NOTES:

TITLE: PCB ASSY CONTROL BOARD 910 GATE ARRAY

DATE: 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
22	1									A11	IC 74LS174	2028200
23	1									A29	IC 74LS00	2024200
24	1									A28	IC 74LS08	2025200
25	1									A34	IC 74LS32	2025800
26	1									A22	IC G/A 910/925	2057400
27	1									A24	IC 74LS02	2041600
28	1									A35	IC 74LS04	2024800
29	1									A21	IC 74S04	2024600
30	1									A7	IC 7406	2034800
31	1									A25	IC 74LS163	2027600
32	1									A20	IC CRT Cont SY6545A-1	2052800
33	3									A19,23,26	IC 74LS157	2027400
34												
35												
36												
37												
38	1									R6	Res CF 3.3K 1/4W 5%	2052700
39	8									R9-13,18,24,25	Res CF 4.7K 1/4W 5%	2053100
40	1									R7	Res CF 47K 1/4W 5%	2033700
41	1									R8	Res CF 1M Ohm 1/4W 5%	2031500
42	1									R2	Res CF 100K 1/4W 5%	2032100

NOTES:

TITLE

PCB ASSY CONTROL BOARD 910 GATE ARRAY

DATE

1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
43	1									R22	Res CF 270 Ohm 1/4W 5%	2051300
44	2									R14,21	Res CF 750 Ohm 1/4W 5%	2031700
45	4									R1,20,23,28	Res CF 1K 1/4W 5%	2052100
46	1									R19	Res CF 22 Ohm 1/4W 5%	2033500
47	1									R3	Res CF 68 Ohm 1/4W 5%	2051100
48	3									R4,5,17	Res CF 330 Ohm 1/4W 5%	2051500
49	1									R1	Res CF 470 Ohm 1/4W 5%	2051700
50	1									R15	Res CF 1.8K 1/4W 5%	2052300
51	1									R26	Res CF 33 Ohm 1/4W 5%	2034500
52	1									R27	Res CF 10K 1/4W 5%	2034100
53												
54	2									RP1,5	Res Pk 4.7K Ohm 10P SIP	2041300
55	3									RP2-4	Res Pk 4.7K Ohm 8P SIP	2042900
56												
57												
58	1									C18	Cap Mica 10pf 50V 5%	2024100
59	3									C2,3,7	Cap Elec 22uf 15V -10% to	2025700
											+100%	
60	1									C5	Cap Elec 10uf 16V 20%	2027300
61	27									C6,9,21-43	Cap Cer .01uf 16V 20%	2028700
62	1									C4	Cap Cer .1uf 50V 10%	2030100

NOTES:

TITLE
PCB ASSY CONTROL BOARD 910 GATE ARRAY

DATE
1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
63	1									C1	Cap Mica 20pf 50V 10%	2024300
64	1									C8	Cap Mono .039uf 50V 10%	2030300
65	1									C19	Cap Tant 4.7uf 16V 10%	2027500
66	8									C10-17	Cap Cer 330pf 50V 20%	2029100
67	1									C20	Cap Tant 10uf 25V 10%	2027100
68												
69												
70												
71	2									CR1,2	Diode IN914	2047500
72												
73	2									Q1,2	Tran 2N4401 NPN/Silicon	2045500
74												
75	1									Y2	Crystal 13.608 MHz	2098605
76	1									Y1	Crystal 1.8432 MHz	2098602
77												
78												
79	2									SW1,2	Switch 10 Pos DIP	2096800
80												
81	3									A13,17,38	Socket IC, 24 Pin	2098401
82	4									A1,20,22,27	Socket IC, 40 Pin	2098402
83	1									A15	Socket IC, 28 Pin	2098404

NOTES:

TITLE: PCB ASSY CONTROL BOARD 910 GATE ARRAY

DATE: 1-14-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	A											
84	1									P6	Socket IC, 16 Pin	2098405
85	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
86	1									P1	Plug 26P RT 3	2098701
87	2									P2,5	Conn 5P STR Wafer	2098802
88	1									P7	Conn 2P STR Wafer	2098800
89												
90												
91												
92												
93												
94												

NOTES:

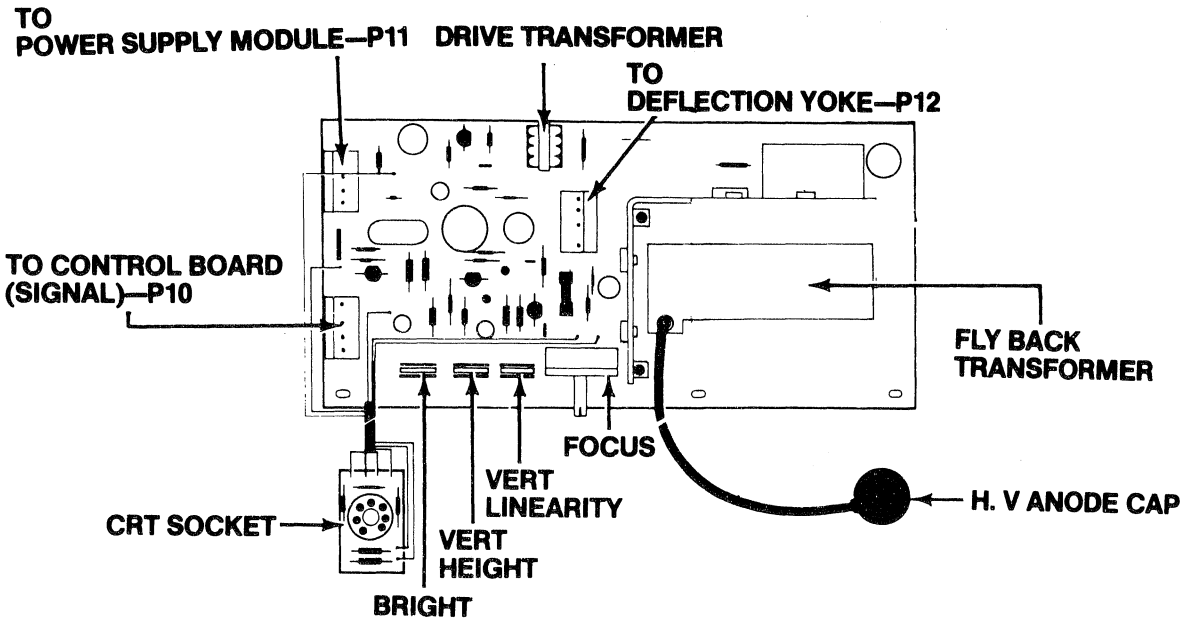
TITLE PCB ASSY CONTROL BOARD 910 GATE ARRAY

DATE 1-14-83

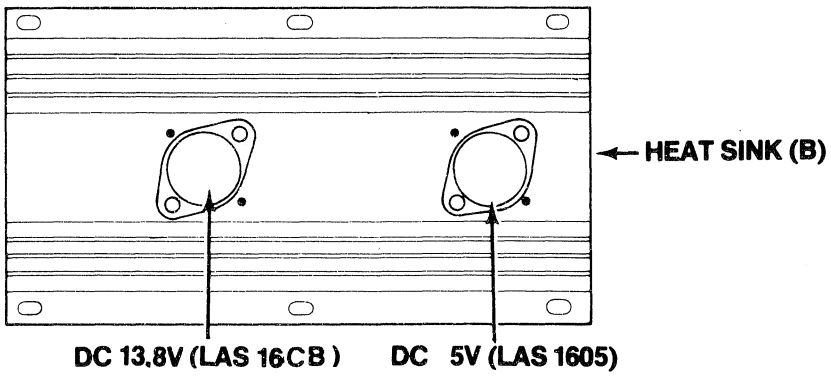
TeleVideo Systems, Inc.

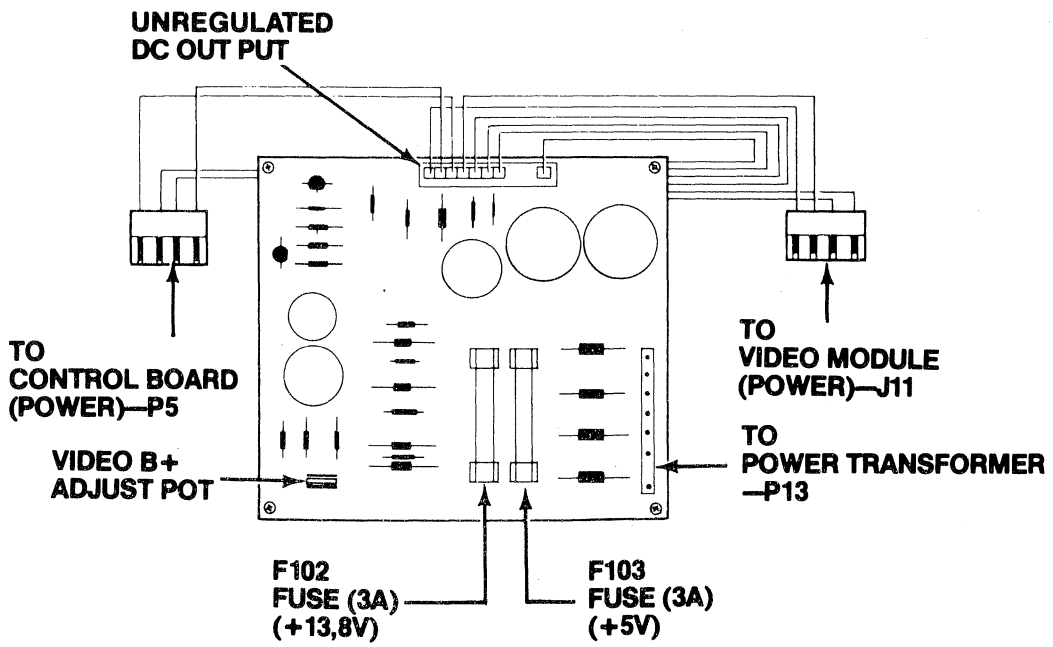
VIDEO MONITOR/POWER SUPPLY SCHEMATICS AND PARTS LIST

TeleVideo Systems, Inc.
1170 Morse Ave., Sunnyvale, CA 94086
(408) 745-7760 TWX 910-338-7633 "TVI VIDEO"

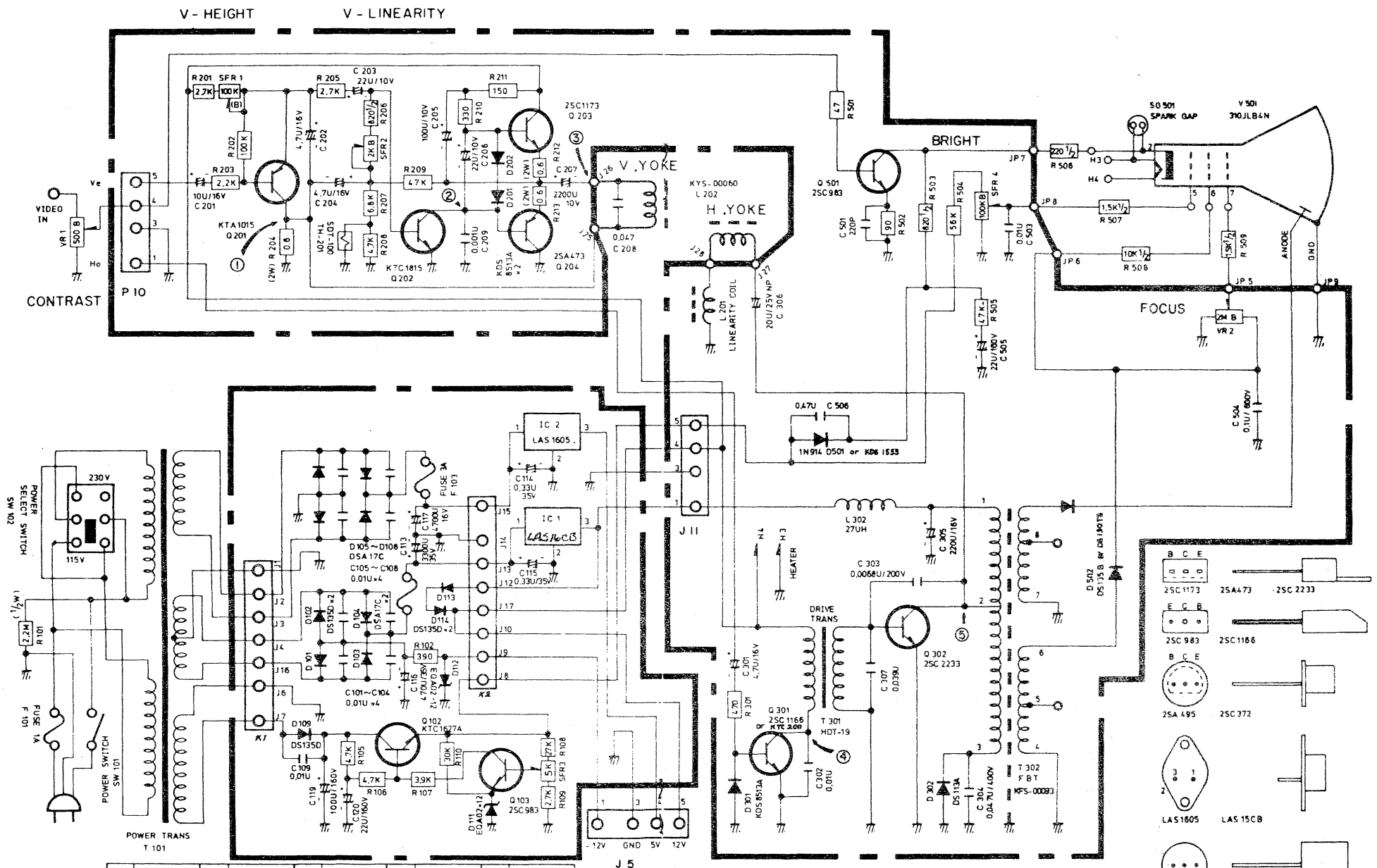


VIDEO MONITOR MODULE





POWER SUPPLY MODULE

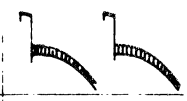
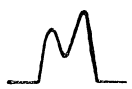
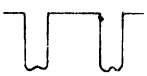
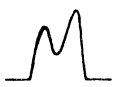


1	Vp-p 0.7	2	Vp-p 6.5	3	Vp-p 6.5	4	Vp-p 20	5	Vp-p 124

1. All resistance values in OHM K=1,000 M=1,000,000.
2. All capacitor values in FARAD U=10^{-6} P=10^{-12}.
3. Unless otherwise stated, working voltages of capacitors are 50 volts.
4. This schematic diagram covers basic or representative chassis only. There may be some component or partial schematic difference between actual chassis and the schematic diagram.

TR WAVEFORM and VOLTAGE

Attachement 1

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC 1)	LAS1512	Regulation	12	2.5		12	0.0	—	0.0	0.0	—
(IC 2)	LAS1605	〃		1.6		5	0.0	—	0.0	0.0	—
(IC 3)	LAS1812	〃		0.1		-12	0.0	—	0.0	0.0	—
(IC 4)	LAS15CB	〃		1.4		13.8	0.0	—	0.0	0.0	—
Q102	2SC509	〃	78.7	0.0	—	86.4	1.5		98.0	0.0	—
Q103	2SC983	〃	12.0	0.0	—	75.7	0.0	—	11.9	0.0	—
Q 201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q 202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	—
Q 203	2SC1173	Vert Out	9.36	6.5		12	0.0	—	8.76	6.5	
Q 204	2SA473	Vert Out	8.0	6.5		0.0	0.0	—	8.6	6.5	
Q 301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	—
Q 302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	—
Q 501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D 302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
1										R101	2.2M Ohm 1/2W CFR	2186500
2										R102	390 Ohm 1/2W CFR	2186100
3										R105,106,208	4.7K Ohm 1/4W CFR	2053100
4										R107	3.9K Ohm 1/4W CFR	2177400
5										R108	27K Ohm 1/4W CFR	2037300
6										R109,201,205	2.7K Ohm 1/4W CFR	2038300
7										R110	30K Ohm 1/4W CFR	2039300
8										R202	100K Ohm 1/4W CFR	2032100
9										R203	2.2K Ohm 1/4W CFR	2038700
10										R204,212,213	0.6 Ohm 2W Wire Wound Res	2177100
11										R206,503	820 Ohm 1/2W CFR	2186200
12										R207	6.8K Ohm 1/4W CFR	2039100
13										R209,505	47K Ohm 1/4W CFR	2033700
14										R210	330 Ohm 1/4W CFR	2051500
15										R211	150 Ohm 1/4W CFR	2033900
16										R214	270 Ohm 1/4W CFR	2051300
17										R301	470 Ohm 1/4W CFR	2051700
18										R501	47 Ohm 1/4W CFR	2037700
19										R502	90 Ohm 1/4W CFR	2177600
20										R504	56K Ohm 1/4W CFR	2039500
21										R506	220 Ohm 1/2W CFR	2186000

NOTES:

TITLE: VIDEO MONITOR AND POWER SUPPLY PARTS LIST

DATE: 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
22										R507,509	1.5K Ohm 1/2W CFR	2186300
23										R508	10K Ohm 1/2W CFR	2186400
24										SFR1, SFR4	100K Ohm Pot	2177700
25										SFR2	2K Ohm Pot	2177800
26										SFR3	5K Ohm Pot	2177900
27										VR1	500 Ohm Pot	2180200
28										VR2	2M Ohm Pot	2180100
29										TH201	1.1K Ohm Thurmister	2180300
30										C101-109	0.01uF 16V Ceramic 20%	2028700
31										C113	3,300uF 35V Electrolytic	2196500
32										C114,115	0.33uF 35V Tantal	2198100
33										C116	470uF 35V Electrolytic	2198200
34										C117	4700uF 16V Electrolytic	2196600
35										C119	110uF 160V Electrolytic	2196300
36										C120	22uF 160V Electrolytic	2196400
37										C201	10uF 16V Electrolytic	2027300
38										C202,204	4.7uF 16V Tantal	2027500
39										C203	22uF 15V Electrolytic	2025700
40										C205	100uF 10V Electrolytic	2196000
41										C206	22uF 10V Electrolytic	2196100
42										C207	2200uF 10V Electrolytic	2196200

NOTES:

TITLE VIDEO MONITOR AND POWER SUPPLY PARTS LIST DATE 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
43										C208	0.047uF/50V Mylar	2197100
44										C209	0.001uF/50V Mylar	2196900
45										C301	4.7uF/16V Electrolytic	2196700
46										C302	0.01uF/50V Mylar	2197000
47										C303	0.0068uF/200V Mylar	2196800
48										C304	0.047uF/400V Mylar	2197500
49										C305	220uF/16V Electrolytic	2199300
50										C306	16uF/25V NP	2280000
51										C307	0.039uF/50V Mylar	2030500
52										C501	220PF 50V Ceramic	2195900
53										C502	0.01uF/50V	2197000
54										C503	0.01uF 50V Ceramic	2028900
55										C504	0.1uF 600V Mylar	2197300
56										C505	22uF 100V Electrolytic	2196100
57										C506	0.47uF 50V Mylar	2197200
58										SG501	1KV Spark Gap	2030900
59										SW101	SPST 115V 10A/230V 5A Pwr SW	2097300
60										SW102	DPDT 115/230V Power Line	2097400
											Slide Switch	
61										F101	1A/250V	2097000
62										F102,103	3A/125V	2193100

NOTES:

TITLE
VIDEO MONITOR AND POWER SUPPLY PARTS LIST

DATE
1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
63										M003	Fuse Clip	2180400
64										Q102	KTC 1627A or MPS-A06	2046700
65										Q103,501	2SC983 or 2N5551	2193200
66										Q201	KTA 1015 or 2N3906	2042200
67										Q202	KTC11815 or 2N3904	2046500
68										Q203	2SC1173 or 2N6121	2199700
69										Q204	2SA473 or 2N6124	2202100
70										Q301	KTC 200(2SC1166) or 2N4401	2045500
71										Q302	2SC2233 or MJE13006	2047300
72										IC1	LAS 16CB 13.8V Regulator	2126900
73										IC2	LAS 1605 5V Regulator	2126800
74										V501	B & W Pr 12"	2049100
75										V501	CRT Green P31 12"	2049300
76										D101-108	DS 135D or 1N5391 Rectifier	2200600
77										D109	DS 135C Rectifier	2201400
78										D111,112	EQA01-12 or 1N759A Zener	2201600
											Diode	
79										D302	DS-113A or MRI-1000 Damper	2201700
											Diode	
80										D501	1N914 or KDS1553 Switching	2047500
											Diode	

NOTES:

TITLE VIDEO MONITOR AND POWER SUPPLY PARTS LIST

DATE 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
81										D502	DS-130TB or 1N4004 600V	2202200
											Rectifier	
82										D201,202,301	KDS-8513A or 1N920 Silicon	2201800
											Diode	
83										D113,114	DS 135D Rectifier	2200600
84										L202	KYS-00060 D.Y Coil	2200800
85										L201	5.4uH Linearity Coil	2200900
86										L201	Adjustable Linearity Coil	2213600
87										L302	27uH Inductor Coil	2201000
88										T101	Power Transformer	2201100
89										T301	Drive Transformer	2201200
90										T302	Flyback Transformer	2201300

NOTES:

TITLE	VIDEO MONITOR AND POWER SUPPLY PARTS LIST	DATE	1-13-83	TeleVideo Systems, Inc.

VIDEO MONITOR/POWER SUPPLY SCHEMATICS AND PARTS LIST

TeleVideo Systems, Inc.
1170 Morse Ave., Sunnyvale, CA 94086
(408) 745-7760 TWX 910-338-7633 "TVI VIDEO"

VIDEO MONITOR

The Video Monitor is made up of two sections; the vertical amplifier and the horizontal amplifier. These amplifiers provide the voltages necessary to drive the CRT yoke, which deflects the electron beam across the CRT.

The electron beam which is generated by the CRT electron gun is swept across and down the screen to create what are called scan lines, which we discussed in character generation. The movement of the beam is driven by vertical and horizontal sweep rates which are both determined by the display circuitry on the logic board. The horizontal sweep is approximatly 16KHz and the vertical sweep is usually 60Hz for domestic and 50Hz for European applications.

The Horizontal sync pulses coming into the Video Monitor are inverted by transistor Q305 and then trigger IC301. In the precision timing mode of operation, the pulse width of IC301 is precisely controlled by R304, R306 and C312. The output Of IC301 is then coupled by Q303 and Q301 to drive transformer T301. The output of T301 is then amplified by Drive transistor Q302. This transistor drives both horizontal yoke windings, as well as the step-up transformer that produces the anode high voltage and the grid voltage for the CRT grid in the neck of the CRT. A new width coil is used for better Raster width control.

The Vertical sync. pulse's coming into the Video Monitor are converted to a sawtooth wave-form. When this is first done the sawtooth pulse is going from a negative leading edge to a positive falling edge, the pulse goes through transistor Q202 and is inverted to it's usable form. Now the pulse is going from a positive 2 volt leading edge to a negative - 2.5 volt falling edge. The timing here is critical because with in one sawtooth pulse there are 250 horizontal pulse's that will occur. This is the total number of horizontal scan lines on the CRT. The sawtooth pulse has to be proportional to all the previous pulse's or the timing will be wrong for the vertical sweep as well as the horizontal sweep. When the vertical sweep is negitive Q201 is conducting and C202 will be discharging. During the positive portion Q201 will cut off and allow C202 to charge. During the time that C202 is charging the electron beam will be scanning. The vertical sweep scans from top to the bottom, once the scan reaches the bottom of the page a (blank) occurs the video beam is turned off and it is retraced back to the top of the screen, this is the time when C202 is discharging. After the retrace the beam is once again turned on and begins it's scan routine. Adjusting SFR1 (vert. height) and SFR2 (vert. linearity) will change the rate of charge of C202 thus changing the slope of the sawtooth pulse.

POWER SUPPLY

Voltages are created and regulated as follows. A 24VAC voltage is rectified by Diode D105, 106, 107 and 108 resulting in a 31VDC output. This 31V is then filtered through C106 (3300MF/50V) and applied to five Volt switching regulator IC103. The output voltage of IC103 is filtered by L101 (200uH 5%) and C110 (2200MF/10V).

The raw 24VDC voltages for the positive and negative 12VDC are rectified by Diodes D101, 102, 103 and 104. The +24V is regulated by IC101 and Q101 for output voltage +12V. This is then filtered through C116. Negative 12V is stabilized by IC102 and filtered by C105.

A 79 volt AC waveform is applied to the halfwave rectifier D109 which is filtered by C115. the resulting 92VDC level is then regulated by a series voltage regulator. The stabilization network comprised of sensing and control elements, Q103 and Q102.

The 75VDC level goes to the Cathode of the CRT tube and spot killed quickly by D501 and C506 to protect burn out on the screen surface of when user turned off.

The high voltage needed to drive the CRT tube V501 are derived from the flyback transformer T302 on the Video Monitor.

TUBE SPECIFICATION

14 INCH 90 DEGREE, HIGH RESOLUTION

DISPLAY TUBE

340CXB 4N

The 340CXB4N is a 14 inch 90 degree high resolution, rectangular display tube primarily intended for use as a alpha-numerical and graphic display tube for computer peripheral devices. The tube is provided with banded type integral implosion protection (with mounting lugs). The tube features a low reflectance, high contrast screen.

ELECTRICAL DATA

Heating	
Indirect by AC or DC:	
Heater voltage	12.0 volts
Heater current	75 nA
Focusing Method	Electrostatic
Deflection Method	Magnetic
Deflection Angles (Approx.)	
Diagonal	90 degrees
Horizontal	80 degrees
Vertical	65 degrees
Anode voltage	16,000 max. volts
	9,000 min. volts

Using high voltage with this tube internal flash-overs may occur, which may cause damage to the cathode of the tube and to various circuit components on the video monitor board. Therefore it is necessary to provide protective circuits using spark-gaps etc. These should be connected as illustrated in figure #1 below.

Figure 1.

No other connections between external conductive coating and chassis are permissible.

OPTICAL DATA

Faceplate	Filterglass
Anti-reflection treatment	Treated
Screen	Aluminized
Appearance	Low Reflective*

* The dark-colored screen, in combination with the filterglass, produces the low reflectivity (equivalent to a 20% light transmission filterglass) for easy-to-see display.

MECHANICAL DATA

Tube Dimensions:

Overall length	297.0 max. mm
Greatest dimensions of tube (excluding lugs)	
Diagonal	348.3 +/- 2.7 mm
Width	295.3 +/- 2.7 mm
Heigth	237.0 +/- 2.7 mm
Useful screen dimensions (projected)	
Diagonal	322.3 min. mm
Width	270.2 min. mm
Heigth	210.7 min. mm

Pin Position Alignment	Pin No 7 aligns approx. with anode contact.
Operating Position	Any
Weight (approx.)	3.5 kg
Implosion Protection	Tension band (with mounting lugs)

GENERAL CONSIDERATIONS:

1. Tube handling. Care should be taken not to scratch the tube.

2. Impact. The tubes should never be exposed to impacts of more than 30G during handling or transportation.

3. Grounding. The external conductive coating of the tube should be grounded with multiple contacts (e.g. a contact plate having many fingers.) Poor contact might cause local heating resulting in tube leakage.

WARNING

SHOCK HAZARD:

The high voltage at which the tube is operated may be very dangerous. Design of the equipment should include safeguards to prevent the user from coming in contact with the high voltage. Extreme care should be taken in the servicing or adjustment of any high voltage circuit.

Caution must be exercised during the replacement or servicing of the tube since a residual electrical charge is stored within the tube. Before handling the tube remove any undersible residual high voltage charge from the tube, by shorting the anode contact button to the frame of the terminal as illustrated in figure #2. Discharging the high voltage to isolated metal parts sucha as cabinets and control brackets may produce a shock hazard.

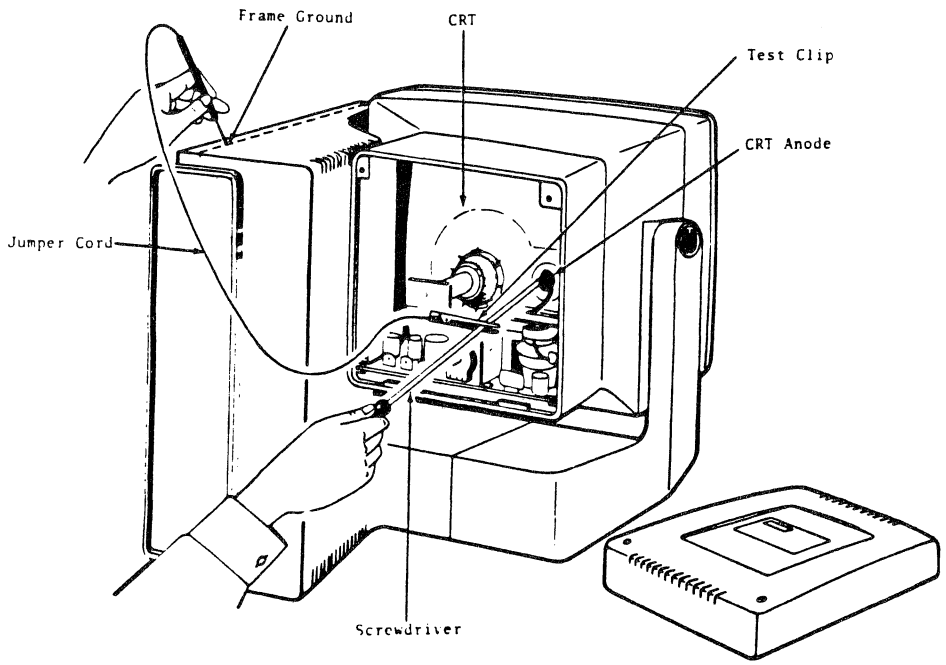
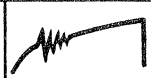


Figure 2.

TABLE 6-1
SIGNAL WAVEFORMS

LOCATION	FUNCTION	DC	AC	BASE(IN)	DC	AC	COL.(OUT)	DC	AC	EMIT(GND)
IC101	REGULA-TION	22	1.0		12	0.0	——	0.0	0.0	——
IC102	"	-22	0.0	——	-12	0.0	——	0.0	0.0	——
IC013	"	28	1.0		5	0.0	——	0.0	0.0	——
Q101	"	22	1.0		12	0.0	——	0.0	0.0	——
Q102	"	65	0.0	——	100	1.0		65	0.0	——
Q103	"	125	0.0	——	50	0.0	——	12	0.0	——
Q201	VERT AMP	-0.8	3.0		-0.3	0.6		0.0	1.5	
Q202	"	0.2	0.5		3.5	8.0		0.0	0.0	——
Q203	"	5.0	8.0		12	0.0	——	5.0	8.0	
Q204	"	4.0	8.0		0.0	0.0	——	4.0	8.0	
Q301	HORIZ AMP	-0.7	1.5		0.0	15		0.0	0.0	——
Q302	"	-3.0	4.0		0.0	160		0.0	0.0	——
Q303	"	2.2	1.5		3.0	1.5		0.8	3.5	
Q304	"	0.6	0.0	——	0.0	3.0		0.0	0.0	——
Q305	"	-1.2	2.2		0.0	8.0		0.0	0.0	——
Q501	VIDEO AMP	0.4	0.0	——	37	27		0.0	0.0	——

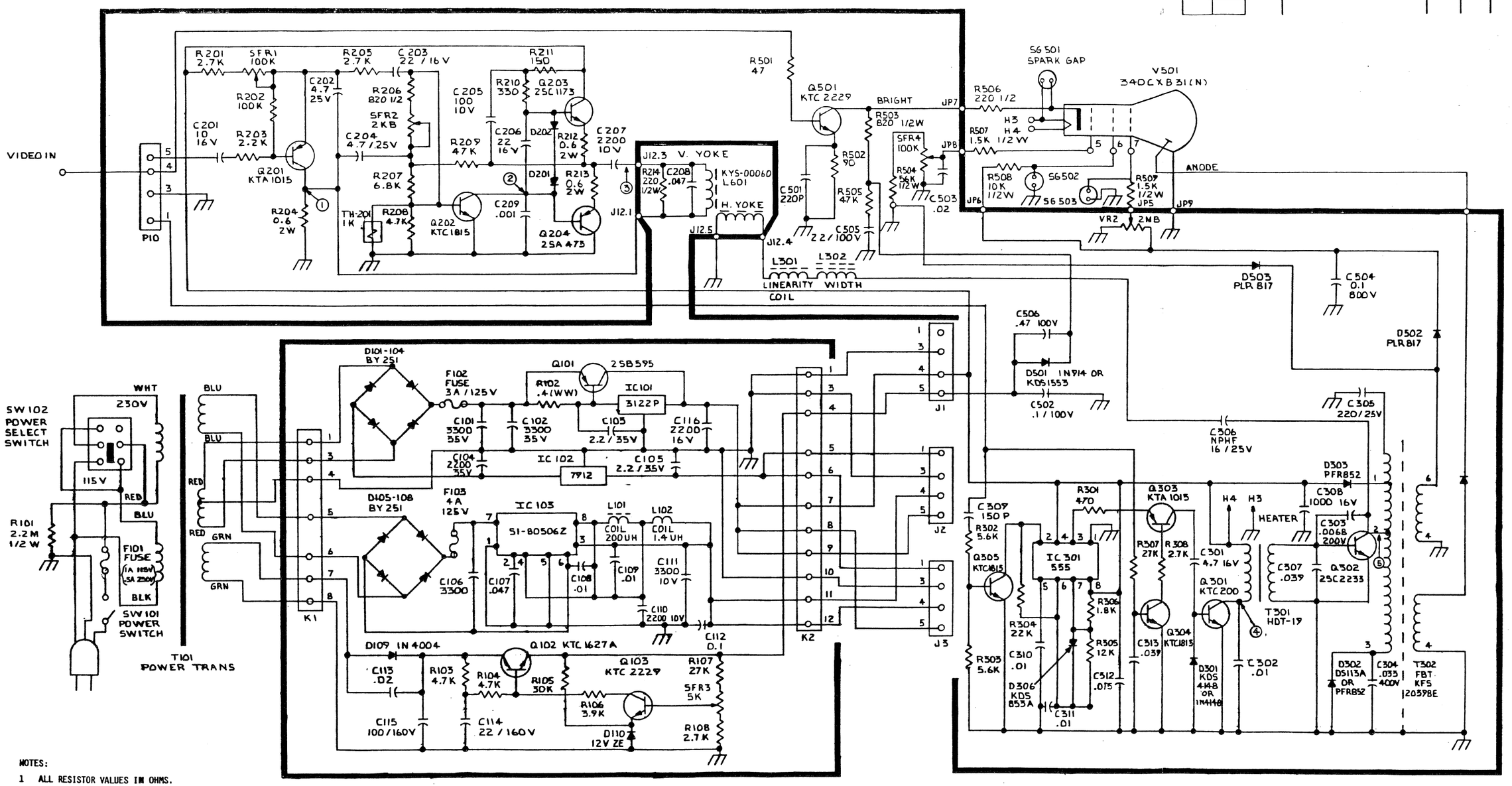
ALL VOLTAGE MEASURES MADE WITH OSCILLOSCOPE

DC READING TAKEN OF SIGNAL BASELINE

AC READING TAKEN OF PEAK TO PEAK AMPLITUDE

NOTE: ANY RIPPLE MEASUREMENT LESS THAN ONE VOLT IS NOT ILLUSTRATED.

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PROD RELEASE	2064	4/18/83	



NOTES:

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN FARADS.
3. UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
4. THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENTS OT PARTIAL SCHEMATIC BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

1	Vpp 0.6	2	Vpp 8.0	3	Vpp 8.0	4	Vpp 15	5	Vpp 160

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION (MM) INCH
X = ± ±
XX = ± ±
XXX = ± ±
ANGLES ±
CONTRACT NUMBER
DES DATE 5/6/83
DR DATE
CHK DATE
ENGR DATE 5/6/83
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc. 587

PCB SCHEMATIC DIAGRAM
POWER SPLY VIDEO MON 970

SIZE	CODE IDENT		REV
D		3201200	A
SCALE		SHEET / OF /	

TERMINAL TROUBLESHOOTING GUIDE

Document 2191400
Revision B

28 February 1983

Disclaimer

TeleVideo Systems, Inc.
1170 Morse Avenue
Sunnyvale, California 94086

1. INTRODUCTION

This is a general troubleshooting guide to be used with the Operator's Manual, Maintenance Manual, and Service Bulletins as required. By following the procedures described here, you should be able to quickly isolate and repair most field failures.

The following sections are included:

2. OVERVIEW OF TERMINAL MODULES

The design of TeleVideo® terminals permits fast fault isolation since the terminal hardware is divided into four main modules:

1. Video monitor
2. Power supply
3. Main logic board
4. Keyboard

The video monitor and power supply are common to all TeleVideo terminals and may be freely interchanged. Terminal keyboards are interchangeable, as outlined in the section on the keyboard. The main logic board is the only module that provides each terminal with its unique characteristics.

The quickest and easiest way to isolate the malfunctioning module is to exchange (swap) each module with a known good module. Once the faulty module is identified, refer to the appropriate troubleshooting table.

WARNING!

High voltages are retained by the CRT tube and capacitors even after power has been turned off. As soon as you open the case, clip one end of a wire to the chassis. Attach the other end of the wire to an insulated screwdriver. Being careful not to touch the metal part of the screwdriver, gently slip the metal end of the screwdriver under the cap of the anode, as shown in Figure 2-1.

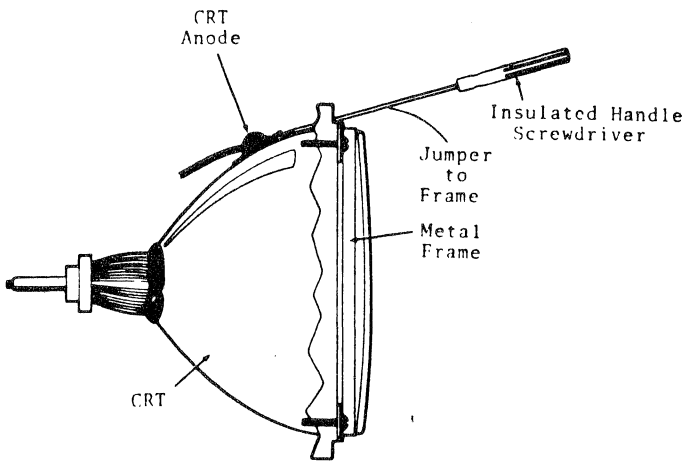


Figure 2-1 Discharging Voltages

3. FUNCTIONAL DESCRIPTION OF MODULES

Logic Board

The logic board processes and controls all data received and transmitted, and generates the video and sync signals required to display data.

The logic board consists of the following five functional areas:

1. Display processor
2. Display generator
3. Keyboard interface
4. Main port interface
5. Printer port interface

Power Supply

The power supply provides DC operating voltages to all circuits in the terminal. The power supply contains two user-replaceable 3 AG-type fuses.

Video Monitor

The video monitor contains horizontal, vertical, and intensity modulation circuits which produce a television-type conventional noninterlaced raster display on the screen. Character signals received from the display generator cause intensified dots to appear at precise intervals on a raster line. These dots, when combined with other dots on other raster lines above and/or below a given line, produce characters.

Keyboard

910/910 PLUS/912C/920C--This keyboard sends matrixed data via a ribbon cable to the logic board, where the ASCII code is generated.

This data is encoded in the 910/910 PLUS by the keyboard encoder (position A1) and in the 912C/920C by the CPU (position A54) and the multiplexers (positions A68 and A69).

The keyboards for these models are all functionally interchangeable. The 910/910 PLUS keyboard has a PRINT keycap where 912C/920C models have a BLOCK/CONV keycap. The 920C keyboard is also fitted with an additional top row of function and editing keys.

925/950--On this keyboard, data is encoded by a microprocessor on the keyboard (position U6) and sent in an ASCII serial data stream to the logic board via the coiled cable. On the logic board, the keyboard interface circuits convert the keyboard data from serial to parallel data for input to the display processor circuitry. All detachable keyboards are identical and interchangeable.

4. TROUBLESHOOTING THE LOGIC BOARD

Visual Inspection

With the Logic Board Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Internal and external switch settings: are they all correct?

* Socketed chips: are they all plugged tightly into their sockets?

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

* Wires: are any broken, loose, or frayed?

* Components: are any overheated or burned?

With the Logic Board Removed--Make these inspections with the logic board removed. The procedure for removing the logic board varies slightly according to the model. Follow the appropriate directions for your model.

910/910 PLUS/912C/920C

To remove the logic board:

1. Turn the power off.

2. On the logic board, disconnect:

   P1 (keyboard input)
   P2 (video signals)
   P3 (RS232C port) if connected
   P4 (printer port) if connected
   P5 (voltage connector)
   P6 (modem connector) if connected
   P7 (speaker connector)

3. Remove the four (910/910 PLUS) or six (912C/920C) securing screws on the logic board.

4. Carefully remove the logic board.

1. Turn the power off.

2. On the logic board, disconnect:

   P1 (keyboard input)
   P3 (RS232C port) if connected
   P4 (printer port) if connected
   P6 (modem connector) if connected

3. Carefully slide the logic board half way out of the terminal and disconnect:

   P2 (video signals)
   P5 (voltage connector)

4. Carefully slide the logic board entirely out of the terminal.

With the logic board removed, inspect the logic board for:

* Overheated or burned components
* Missing or broken components
* Cracked, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Bent pins

STOP!

If defects are found, correct them and recheck the terminal before continuing.

If no defects are found, reinstall the logic board before proceeding with the procedures in the next section, Large Scale Integration Failures.

Large Scale Integration Failures

Since most failures involve Large Scale Integration (LSI) chips, this step will quickly repair most failures encountered. Exchange all socketed chips, one at a time, with known good chips. If the logic board malfunctions after the chips are swapped, confirm the operation of the data lines described in the next section, Data Line Operation.

NOTE!

The remainder of this guide involves troubleshooting to the component level and requires schematics, an oscilloscope, a working knowledge of transistor-transistor logic (TTL), and basic debugging skills.

Data Line Operation

Confirm that the data lines are operating properly before proceeding further.

NOTE!

It is beyond the scope of this bulletin to list all possible data line problems.

The best place to check the data lines is directly from the CPU (see page 1 of the schematics). There should be activity on all data lines and the signals should range from 0 (ground) to +4.5 to +5.0 volts. If the malfunction persists after you have confirmed proper operation of the data lines, follow the procedures in the next section, Debugging Tables.

Debugging Tables

NOTE!

The items listed in the tables in this section are only suspect areas; they should **not** be automatically replaced when the symptoms listed are present.

Table 4-1 910/910 PLUS Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video	6502	A39	1 of 5
	6545	A26	2 of 5
	2114	A30, A31, A36, A37	2 of 5
	or		
	6116	A24	2 of 5
	Crystal	Y2	3 of 5
	74LS163	A15	3 of 5
	2332	A45	1 of 5
	2N2219	Q2	4 of 5
Distorted video	6502	A39	1 of 5
	6545	A26	2 of 5
	6116	A24	2 of 5
	or		
	2114	A30, A31, A36, A37	2 of 5
	2332	A48	3 of 5
	74LS166	A49	3 of 5
Horizontal bar across screen	6545	A26	2 of 5
	74S04	A22	4 of 5
Loss of underline, reverse video, blinking, or blanking	74LS174	A42	3 of 5
	6545	A26	2 of 5
Loss of half intensity	74LS175	A41	3 of 5
	6545	A26	2 of 5
Loss of all attributes	6545	A26	2 of 5
	74S74	A40*	3 of 5
Unable to transmit data	75188	A10	4 of 5
	6551A	A19	4 of 5
Unable to receive data	75189	A5	4 of 5
	6551A	A19	4 of 5
Poor/no printing	75189	A5	4 of 5
	75188	A10	4 of 5
	6551A	A19	4 of 5
Incorrect/no keyboard response	AY-5-3600	A1	5 of 5
	2716	A2**	5 of 5

Notes
*Must be a Texas Instruments part.
**If used.

Table 4-1 Continued

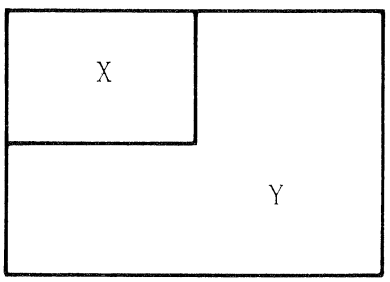
Symptom	Suspect Areas Part No.	Position	Schematic Page
SHIFT or CTRL keys do not function	A6-5-3600	A1	5 of 5
	7406	A12	5 of 5
	RP4		5 of 5
ALPHA LOCK or FUNCT keys do not function	AY-5-3600	A1	5 of 5
	74LS364	A8	5 of 5
	RP4		5 of 5
Keys repeat	AY-5-3600	A1	5 of 5

*Must be a Texas Instruments part.
**If used.

Table 4-2 912/920 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video, no beep	8035	A54	1 of 6
	5027	A23	4 of 6
	23.814-MHz Crystal	X1	4 of 6
	74LS109	A56	4 of 6
	74LS163	A57	4 of 6
	System ROMs	A49	2 of 6
	System ROMs	A50*	2 of 6
	2332	A3	5 of 6
No video, constant beep	5027	A23	4 of 6
	2114 RAM, page 1	A6, A8, A10, A12	3 of 6
	2114 RAM, page 2	A5, A7, A9, A11	3 of 6
Horizontal bar across screen	5027	A23	4 of 6
	74LS08	A32	5 of 6
	74LS05	A14	5 of 6
Bad video or incorrect character displayed in:			
Area X of screen**	2114 RAMs	A8	3 of 6
	2114 RAMs	A12	3 of 6
Area Y of screen**	2114 RAMs	A6	3 of 6
	2114 RAMs	A10	3 of 6
Bad video on entire screen	74LS157	A24, A25, A26	3 of 6
	74LS00	A40	3 of 6
	8035	A54	1 of 6
	5027	A23	4 of 6

Notes
* If installed
**



Areas X and Y of Screen

Table 4-2 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Distorted characters	2316	A3	5 of 6
	8035	A54	1 of 6
	2114 RAMs	A5 through A12	3 of 6
Unable to transmit	75188	A59	2 of 6
	74LS157	A78	2 of 6
	2502	A48	2 of 6
Unable to receive	75189	A60	2 of 6
	74LS157	A78	2 of 6
	2502	A48	2 of 6
Loss of blinking or blanking	74LS74	A35	4 of 6
	5027	A23	4 of 6
Loss of half intensity	74LS74	A16	5 of 6
	74LS03	A15	5 of 6
	5027	A23	4 of 6
Loss or underlining/reverse video	74LS74	A28	5 of 6
	74LS74	A29	5 of 6
	5027	A23	4 of 6
Incorrect or no keyboard input	8035	A54	1 of 6
	74LS253	A68	1 of 6
	74LS253	A69	1 of 6
ALPHA LOCK, SHIFT, CTRL, or Function keys do not function	74LS364	A76	1 of 6
	74LS42	A58	1 of 6
Unable to select one or more baud rates	74LS163 Counter	A70 through A73	6 of 6
	Baud rate switch	S1	6 of 6
	74LS00 Nand Gate	A74	6 of 6

Table 4-3 925 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No beep, no video	13.6080-MHz Crystal	Y2	7 of 7
	74LS00	A55	4 of 7
	74LS139	A37	4 of 7
	6502A	A60	1 of 7
	6545A-1	A59	2 of 7
Constant beep, no video	6502A	A60	1 of 7
	6545A-1	A59	2 of 7
	74LS223	A44	7 of 7
Horizontal bar	74504	A16	7 of 7
	6545A-1	A59	2 of 7
Bad video	10uf cap	C41	1 of 7
	74LS74	A6	4 of 7
	6545A-1	A59	2 of 7
Distorted characters	74LS166	A30	2 of 7
	2332	A31	2 of 7
Unable to transmit to computer	75188	A34	5 of 7
	6551	A32	5 of 7
	74LS32	A26	5 of 7
Unable to receive from computer	75189	A9, A17	5 of 7
	6551	A32	5 of 7
Unable to transmit to printer	75188	A34, A25	5 of 7
	74LS32	A26	5 of 7
	6551	A32	5 of 7
Unable to receive from printer	75189	A9, A19	5 of 7
	74LS32	A26	5 of 7
	75188	A25	5 of 7
Loss of any video attribute	74LS173	A19, A20, A21	3 of 7
	74LS245	A40	2 of 7
	74LS374	A39	2 of o7
	2332	A50, A49	1 of 7
No keyboard communication*	1.8432-MHz Crystal	Y1	5 of 7
	6551	A33	5 of 7
	6502A	A60	1 of 7

*Refer also to Service Bulletin 2, Eliminating Keyboard Lockup

Table 4-3 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to select switch bank S1	Switch	S1	6 of 7
	74LS244	A53, A52	6 of 7
	Resistor pack	RP5	6 of 7
Unable to select switch bank S2	Switch	S2	6 of 7
	74LS244	A51, A52, A53	6 of 7
	Resistor pack	RP1	6 of 7
Unable to select switch bank S3	Switch	S3	6 of 7
	74LS244	A43, A51,	6 of 7
	Resistor pack	RP4	6 of 7

Table 4-4 950 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video, no beep	6502	A53	1 of 7
	6551	A49, A50 A51	5 of 7
	6545	A56	2 of 7
	Program ROMs	A41, A42	1 of 7
	User ROMs	A52	1 of 7
	Character Generator ROMs	A32, A33	4 of 7
	23.824-MHz Crystal	OSC1	6 of 7
	74LS163	A3	6 of 7
	74LS109	A6	6 of 7
No video, constant beep	6545	A56	2 of 7
	2114 RAMs	A25, A26, A27, A28	3 of 7
Horizontal bar across screen	6545	A56	2 of 7
	2114 RAMs	A25, A26, A27, A28	3 of 7
Bad video, one section of screen	2114	A25	3 of 7
	2114	A26	3 of 7
	2114	A27	3 of 7
	2114	A28	3 of 7
Bad video on only one page			
Page 1	6116	A37	3 of 7
Page 2	6116	A34	3 of 7
Page 3	6116	A35	3 of 7
Page 4	6116	A36	3 of 7
Bad video on entire screen	74LS157	A43 through A46	2 of 7
	6545	A55	2 of 7
	6502	A53	1 of 7
Distorted characters	2332	A32, A33	4 of 7
	74LS166	A22, A23	4 of 7
	6502	A53	1 of 7
	All 2114's	A25 through A28	3 of 7

Table 4-4 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to transmit to system	1488	A48	5 of 7
	74LS32	A58	5 of 7
	6551	A50	5 of 7
	74LS157	A59	5 of 7
Unable to receive from system	1489	A57	5 of 7
	74LS08	A29	5 of 7
	6551	A51	5 of 7
Unable to transmit to printer	1488	A39	5 of 7
	74LS32	A58	5 of 7
	6551	A51	5 of 7
	74LS157	A59	5 of 7
Unable to receive from printer	1489	A40	5 of 7
	6551	A51	5 of 7
Loss of any video attribute	74LS174	A19	4 of 7
	74LS157	A20	4 of 7
	74LS174	A21	4 of 7
Incorrect or no keyboard input	6502	A53	1 of 7
	6551	A49	3 of 7
Unable to select one or more baud rates	6502	A53	1 of 7
	6552	A54	7 of 7
	74LS367	A65, A66	7 of 7
	RP 2		7 of 7
	RP 3		7 of 7
	Switch 1		7 of 7

"Gate Array" Logic board, Supplement Debugging Guide

Although the components are laid out differently, "Gate Array" boards are completely interchangable with TTL boards. When troubleshooting the "Gate Array" Logic boards care should be taken when handling the CMOS devices. The "Gate Array" chip positions are listed below. When exchanging these custom CMOS chips one must be grounded to earth ground to avoid damage to the chip from static discharge.

Model No.	Televideo Part Number	Location
910, 910Plus	2057400	A22
925	2057400	A39
950, Chip A	2057600	A34
Chip B	2057800	A37

Follow the procedure in the begining of this section for a visual inspection of the logic board.

Table 4-5 910/910 PLUS GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video	6545A-1	A20	2 of 5
	6502	A27	1 of 5
	6116	A13	2 of 5
	Crystal	Y2	3 of 5
	2532	A38	1 of 5
	74LS163	A25	3 of 5
	74LS166	A18	3 of 5
	2N2219	Q2	4 of 5
	70200-11B	A22	3 of 5
Distorted video	6545A-1	A20	2 of 5
	6116	A13	2 of 5
	70200-11B	A22	3 of 5
	74LS166	A18	3 of 5
	2532	A38	1 of 5
Horizontal Bar across screen	6545A-1	A20	2 of 5
	74LS08	A37	2 of 5
Loss of Attribute	70200-11B	A22	3 of 5
	6545A-1	A20	2 of 5
Unable to Transmit to Computer or printer	75188	A9	4 of 5
	6551A-1	A15	4 of 5
Unable to Receive from Computer or printer	75189	A10	4 of 5
	6551A-1	A15	4 of 5
Inncorect/ no keyboard response	AY-5-3600	A1	5 of 5
	2716	A2	5 of 5
	74LS367	A3,A8	5 of 5
Shift or CTRL keys inoperative	AY-5-3600	A1	5 of 5
	7406	A7	5 of 5
	resistor pack	RP2	5 of 5
Alpha Lock or Funct keys inoperative	AY-5-3600	A1	5 of 5
	74LS367	A8	5 of 5
	resistor pack	RP2	5 of 5
Repeating keys	AY-5-3600	A1	5 of 5

Table 4-6 925 GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic page
No video/ no beep	Crystal	Y2	6 of 6
	70200-11A	A39	3 of 6
	74LS139	A38	3 of 6
	6502	A11	1 of 6
	6545A-1	A28	2 of 6
Constant beep/ no video	6545A-1	A28	2 of 6
	74LS273	A26	6 of 6
	6502	A11	1 of 6
Horizontal bar across screen	6545A-1	A28	2 of 6
	74S04	A40	3 of 6
Bad video	10uF cap	C28	1 of 6
	6545A-1	A28	2 of 6
	70200-11a	A39	3 of 6
Distorted characters	2332	A17	2 of 6
	74LS166	A12	2 of 6
Loss of Attribute	70200-11A	A39	3 of 6
	2333	A14,A15	1 of 6
No transmit to computer or printer	75188	A23	4 of 6
	6551A-1	A4	4 of 6
	74LS32	A24	4 of 6
No receive from computer or printer	75189	A2	4 of 6
	6551A-1	A4	4 of 6
No keyboard response	Crystal	Y3	4 of 6
	6551A-1	A5	4 of 6
	6502	A11	1 of 6
Unable to select S1	Switch	S1	5 of 6
	74LS244	A3,A41	5 of 6
	resistor pack	RP1	5 of 6
Unable to select S2	Switch	S2	5 of 6
	74LS244	A3,A41, A34	5 of 6
	resistor pack	RP2	5 of 6
Unable to select S3	Switch	S3	5 of 6
	74LS244	A34,A29	5 of 6
	resistor pack	RP4	5 of 6

Table 4-7 950 GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video/ no beep	6502	A11	1 of 7
	6551	A29,A33	5 of 7
		A36	
	6545	A6	2 of 7
	740012	A34	4 of 7
	2532	A20,A25	1 of 7
	2332	A30,A31	4 of 7
	Crystal	OSC 1	4 of 7
No video/ constant beep	6545	A6	2 0f 7
	6116	A3	3 of 7
Horizontal bar across screen	6545	A6	2 of 7
	7406	A39	6 of 7
Bad video	6116	A8,A13	3 of 7
		A17,A22	3 of 7
	74LS157	A7,A12	2 of 7
		A16,A21	2 of 7
	6545	A6	2 of 7
	6502	A11	1 of 7
	740012	A34	4 of 7
Distorted characters	2332	A30,A31	4 of 7
	740012	A34	4 of 7
	740012	A37	6 of 7
Loss of Attributes	740012	A34	4 of 7
Unable to transmit to computer	75188	A18	5 of 7
	74LS32	A19	5 of 7
	6551	A29	5 of 7
	74LS157	A28	5 of 7
Unable to receive from computer	75189	A9	5 of 7
	740012	A37	6 of 7
	6551	A29	5 of 7
Unable to transmit to printer	75188	A23	5 of 7
	74LS32	A24	5 of 7
	6551	A33	5 of 7
	74LS157	A28	5 of 7
Unable to receive from printer	75189	A32	5 of 7
	6551	A33	5 of 7
Inncorect/ no keyboard response	6551	A36	5 of 7
	6502	A11	1 of 7
	74LS32	A19	5 of 7

Table 4-7 continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to select S1	Switch	S1	7 of 7
	resistor pack	RP1,RP2	7 of 7
	74LS367	A1,A4	7 of 7
	6552	A43	7 of 7
	6502	A11	1 of 7
Unable to select S2	Switch	S2	7 of 7
	resistor pack	RP2	7 of 7
	74LS367	A4,A38 A42	7 of 7
	6552	A43	7 of 7
	6502	A11	1 of 7

5. TROUBLESHOOTING THE KEYBOARD

Visual Inspection

With the Keyboard Installed--Turn off power to the terminal. Check keyboard alignment; are any keys binding on the cover?

Open the top case.

910/910 PLUS/912/920

Remove the two screws from the bottom front corners of the terminal. Carefully tip the top case back until it rests on a firm surface.

NOTE!

The terminal will now be top heavy and may tip over if there is not sufficient table space to support the top.

925/950

Remove the four screws from the bottom of the keyboard case. Carefully life off the top of the keyboard case and set it aside.

Check the following areas:

* Key switches:

  Foreign objects (e.g., paperclips, staples, matches)

  Liquid residue (e.g., coffee, soft drinks)

  Broken keyswitches

  Missing or incorrectly placed keycaps

* Cables:

  Broken wires

  Loose wires at connectors

  Creased, kinked, or cut cables

* Connectors:

  Loose or damaged connectors

  Bent pins

  Dirty contacts

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

With the Keyboard Removed--Make the following inspections with the keyboard removed from its case. The procedure for removing the keyboard varies slightly according to the model.

910/910 PLUS/912/920

To remove the keyboard:

1. Unplug the ribbon cable from the logic board.
2. Remove the two securing screws and washers from the inner bottom corners of the keyboard.
3. Carefully remove the keyboard from the surrounding case.

925/950

To remove the keyboard:

1. Disconnect on the keyboard:

   P6 (speaker connector)
   P7 (keyboard cable)

2. Remove the four screws from the bottom corners of the keyboard case.
3. Carefully remove the keyboard from the bottom case.

Inspect the keyboard for:

* Overheated, damaged, or burned components
* Cracked, shorted, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Broken, loose, or frayed wires

NOTE!

If any defects are found, correct them and recheck before continuing.

Table 5-1 Keyboard Debugging Guide

Symptom	Suspect Areas	Models
One key inoperative/ intermittent	Respective keyswitch	A
	Open trace/bad solder joint	A
	8048 keyboard CPU, position U6	B
Several keys inoperative/intermittent	Open/shorted trace	A
	Broken/loose jumper	A
	Defective ribbon cable	C, D
	Bent pin at ribbon cable connectors	C, D
	8048 keyboard CPU, position U6	B
	10K ohm resistor packs, positions RP2, RP3	B
	10K ohm resistor, position R3	B
All keys inoperative	Open/shorted trace	A
	Defective ribbon or keyboard cable	A
	8048 keyboard CPU, position U6	B
	7805 +5V regulator, position V1	B
	5.7143-MHz crystal, position X1	B
SHIFT, FUNCT, or ALPHA LOCK keys	10K ohm resistor pack, position RP2	
	8048 keyboard CPU, position U6	B
CTRL key inoperative	10K ohm resistor pack, position R2	
	8048 keyboard CPU, position U6	B
Incorrect characters	Shorted trace	A
	Shorted/improperly plugged ribbon cable	C, D
	8048 keyboard CPU, position U6	B

Legend
A = All
B = 925/950
C = 910/910 PLUS
D = 912/920

Table 5-1 Continued

Symptom	Suspect Areas	Models
Keys repeat	Respective keyswitch*	B, D
	Shorted trace	A
	Shorted ribbon cable	C, D
	8048 keyboard CPU, position U6	B

Legend
A = All
B = 925/950
C = 910/910 PLUS
D = 912/920

Note
*On the 910/910 PLUS terminals, a key which is shorted will not repeat on power up. Instead, any key pressed will repeat until another key is pressed.

6. TROUBLESHOOTING THE VIDEO MONITOR

Visual Inspection

With the Video Monitor Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

* Wires: are any broken, loose, or frayed?

* Components: are any overheated, leaking, or burned?

If any defects are found, correct them and recheck the terminal before continuing.

With the Video Monitor Removed--The following inspections should be made with the video monitor removed.

To remove the video monitor:

1. With the power off and the cover removed, disconnect the following connections on the video monitor:

   J10 (signal input)
   J11 (DC power)
   J12 (yoke)

2. Disconnect the following parts on the CRT tube:

   CRT socket (small printed circuit board at rear of tube)

   Anode lead (SEE WARNING ON PAGE 2-1)

   Ground wire

3. Remove the three securing screws on the video monitor.

4. Carefully remove the video monitor.

With the video monitor removed, inspect it for:

* Overheated, leaking, or burned components
* Missing or broken components
* Cracked, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Bent pins

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

If no defects are found, reinstall the video monitor.

Apply power.

WARNING!

High voltages are present on the video logic board. USE EXTREME CARE during troubleshooting.

The four adjustments which can be made to the video board are listed in Table 6-1. The controls are shown in Figure 6-1.

Table 6-1 Video Board Adjustments

Problem	Control
Characters are too bright or too dim	Brightness
Whole screen is too tall or too short	Height
Characters are not even in height from the top to the bottom of the screen	Linearity
Characters are not sharp	Focus

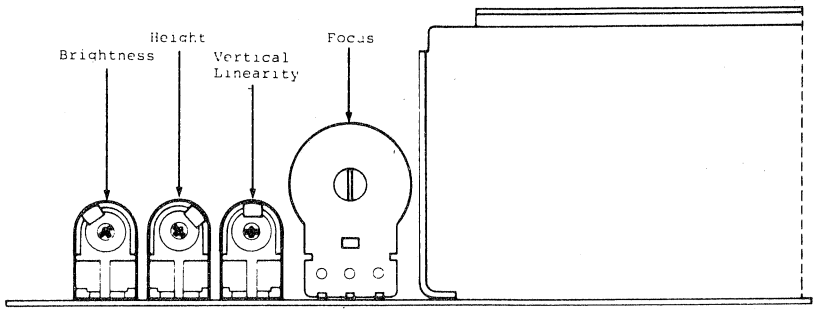


Figure 6-1 Location of Controls on Video Board

Debugging Guide

This section will help you troubleshoot specific malfunctions. Table 6-2 lists voltage levels and wave forms.

SYMPTOM: No Vertical Deflection

1. Check Q201 collector for vertical deflection.

   a. If it is present, proceed to Step 2.

   b. If it is not present, check the base of Q201.

   c. If vertical deflection is present at the base, isolate the Q201 collector to see if signal is being pulled down. If there is still no output at Q201, suspect Q201.

   d. If vertical deflection is not present at the base, troubleshoot between the base of Q201 and P10 pin 5 (vertical sync signal from the logic board).

2. Check Q202 collector for vertical deflection.

   a. If it is present, proceed to Step 3.

   b. If it is not present, check the base of Q202.

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC 1)	LAS1512	Regulation	12	2.5		12	0.0		0.0	0.0	
(IC 2)	LAS1605	〃		1.6		5	0.0		0.0	0.0	
(IC 3)	LAS1812	〃		0.1		-12	0.0		0.0	0.0	
(IC 4)	LAS15CB	〃		1.4		13.8	0.0		0.0	0.0	
Q102	2SC509	〃	78.7	0.0		86.4	1.5		98.0	0.0	
Q103	2SC983	〃	12.0	0.0		75.7	0.0		11.2	0.0	
Q201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q202	2SC372	Vert Drive	0.58	1.5		8.0	6.5		0.0	0.0	
Q203	2SC1173	Vert Out	9.36	6.5		12	0.0		8.76	6.5	
Q204	2SA473	Vert Out	8.0	6.5		0.0	0.0		8.6	6.5	
Q301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	
Q302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	
Q501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

Table 6-2 Voltage Levels and Waveforms

c. If vertical deflection is present at the base, isolate the Q202 collector to see if signal is being pulled down. If there is still no output at Q202, suspect Q202.

d. If vertical deflection is not present at the base, troubleshoot back from the base of Q202.

3. Check the negative side of C207 for vertical deflection.

a. If vertical deflection is present, the vertical drive section of the video monitor is good. If a vertical problem still exists, check the following areas:

Connections
CRT socket
Related components (small pcb at neck of CRT)

b. If vertical deflection is not present at C207, check the Q203 emitter.

c. If vertical deflection is not present at the Q203 emitter, check the base of Q203.

d. If vertical deflection is present at the base, suspect Q203.

e. If not present at the base of Q203, troubleshoot back.

f. If Q203 emitter is good, check Q204 emitter.

g. If vertical deflection is not present at Q204 emitter, check the base of A204.

h. If present at base, suspect A204.

i. If not present at base, troubleshoot back from Q204.

NOTE!

Since Q203 and Q204 are a matched set of push/pull amplifiers, replace both if one require replacement.

SYMPTOM: No Horizontal Deflections

1. Check the Q301 deflector for horizontal deflections.

a. If horizontal deflections are present, proceed to Step 2.

b. If not present, check the base of Q301.

c. If horizontal deflections are present at the base, isolate the Q301 collector to see if signal is being pulled down.

d. If there is no output at the Q301 collector, suspect Q301.

e. If horizontal deflections are not present at the base of Q301, troubleshoot between the base of Q301 and P10 pin 1 (horizontal sync signal from the logic board).

2. Check the Q302 deflector for horizontal deflections.

a. If horizontal deflections are present, proceed to Step 3.

b. If not present, check the base of Q302.

c. If horizontal deflections are present at the base, isolate the Q302 collector to see if signal is being pulled down.

d. If there is no output at the Q302 collector, suspect A302.

e. If horizontal deflections are not present at the base of Q301, suspect T301 (drive transformer) or Q302.

f. If the proper signal is present at Q302 collector, suspect the following areas:

C306
L201

SYMPTOM: No Video

1. Suspect the following areas:

L302
Q302
Q301
T302 (FBT)
C305
Q501

2. Check for cracked, broken, or lifted traces.

SYMPTOM: Jittery Screen

1. Make sure that yoke connector J12 is not dirty.

2. Suspect C504.

3. Check for

   * Bad crimps

   * Poor solder joints (loose solder balls, cold solder joints, or solder bridges)

SYMPTOM: Poor Linearity

1. If horizontal linearity is the problem, check L201.

2. If vertical linearity is the problem, check the following:

   a. Adjust SFT 2 (linearity potentiometer)

   b. Q203 and Q204

SYMPTOM: Fuses Blow and/or Voltage is Low

1. Check T302 (FBT)

2. Check for cracked, broken, or lifted traces.

7. TROUBLESHOOTING THE POWER SUPPLY

Visual Inspection

With the Power Supply Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

  Depressed pins in connectors

* Wires: are any broken, loose, or frayed?

* Components: are any overheated, leaking, or burned?

* Bad fuse

  NOTE!

  Check the fuse with an ohm meter. Do not rely on a visual check.

* Loose fuse holder

If defects are found, correct them and recheck the terminal before continuing.

With the Power Supply Removed--The following inspections should be made with the power supply removed.

To remove the power supply:

1. Turn the power off and remove the cover.
2. Unplug the power cord from the wall outlet.
3. Disconnect K1 (AC input) on the power supply.
4. Disconnect J11 on the video monitor.
5. Disconnect J5 on the logic board.
6. Remove the securing screws on the power supply (four on the 925/950; three on 910/910 PLUS/912/920).
7. Carefully remove the power supply.

With the Power Supply Removed--Inspect the power supply for:

* Overheated, leaking, or burned components
* Bad crimps
* Bad connectors/connections

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

Disassemble the power supply by removing the four securing screws and spacers which hold the small pcb on the heat sink.

Debugging Guide

This section will help you troubleshoot specific malfunctions. Table 6-2 lists voltage levels and waveforms.

SYMPTOM: No +5V DC

1. Remove F103 and check for approximately +13V on one side of the fuseholder.

   a. If correct voltage is not present, suspect the following areas:

      C105 through C108

      D105 through D108

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

   b. If correct voltage is present, suspect the following areas:

      F103 (fuse)

      LAS1605

      C114

      C113

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

SYMPTOM: +5V DC is Low

1. Check the following areas:

   LAS1605

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No +12V DC or 13.8V DC

1. Remove F102 and check for +24V on one side of the fuseholder.

   a. If correct voltage is not present, suspect the following areas:

      C101 through C104
      D103 through D104
      Bad crimps
      Bad connectors/connections
      Broken or loose clips

   b. If correct voltage is present, suspect the following areas:

      LAS15CB/LAS16CB

      C115

      C113

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

SYMPTOM: +12V DC or +13.8V DC is Low

1. Check the following areas:

   LAS15CB

   C113

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No -12V DC

1. Check the following areas:

   C101 and C102

   D101 and D102

   D112

   C116

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No +75V DC

1. Check the following areas:

   C109 (can be removed; do not need to be replaced)
   C120
   C119
   Q102
   Q103

SYMPTOM: +75V DC is Low

1. Adjust SFR3.

2. If +75V DC cannot be adjusted, check the following areas:

   Q103
   C109

If no defects are found, reinstall the video monitor. Make sure the securing screws are locked tight before proceeding.

Apply power.

TROUBLESHOOTING GUIDE FOR 970 TERMINAL

This is a general troubleshooting guide to be used with the Operator's Manual, Maintenance Manual, and Service Bulletins as required. By following the procedures described here, you should be able to quickly isolate and repair most field failures.

SECTION 1 OVERVIEW OF TERMINAL MODULES

The design of Televideo terminals permits fast fault isolation since the terminal is divided into four main modules.

1. Video monitor
2. Power supply
3. Main logic board
4. Keyboard

The 970 terminal begins a new generation of terminals. The design of the video monitor and DC power supply boards has been simplified to use fewer DC voltages. This change in design makes these two boards unique and noninterchangeable with the earlier Televideo terminals 910, 912, 920, 925 and 950. Interchange the video monitor and power supply boards only with boards of the same type. However a logic board of the older type terminal maybe connected to the video monitor and power supply of the 970.

To verify a malfunctioning module exchange (swap) each module with a known good one. Once the malfunctioning module is identified, refer to the appropriate section in this guide for futher troubleshooting.

DISCHARGE PROCEDURE

High voltages are retained by the CRT tube and capacitors even after power has been turned off. As soon as you open the case, clip one end of a wire to the chassis. Attach the other end of the wire to an insulated screwdriver. being careful not to touch the metal part of the screwdriver, gently slip the metal end of the screwdriver under the cap of the anode, as shown in Figure 1.1

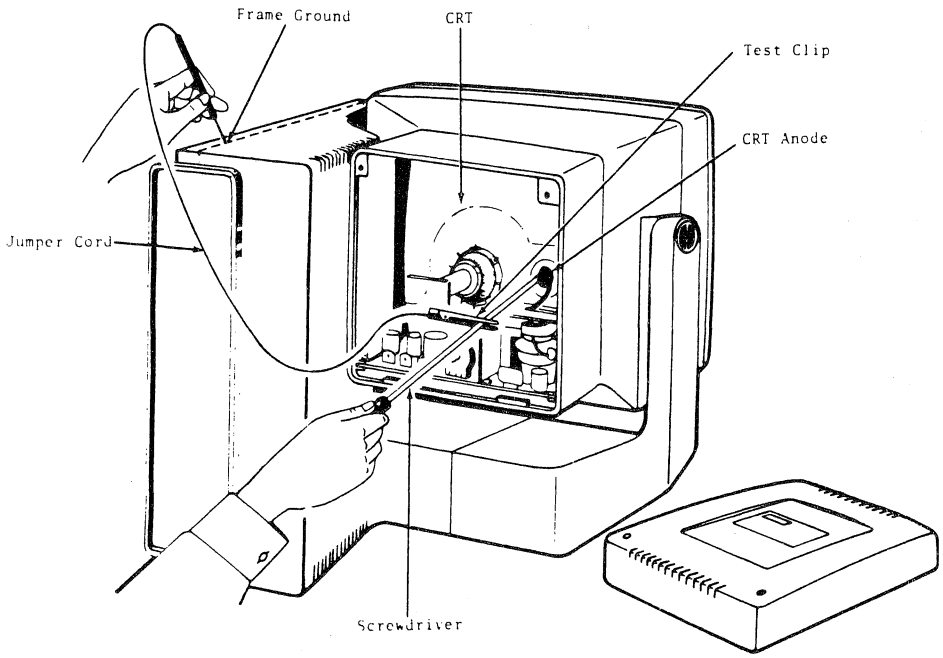


FIGURE 1-1 Discharging Voltages

SECTION 2 FUNCTIONAL DESCRIPTION OF MODULES

LOGIC BOARD

The logic board processes, stores and manipulates data received and transmitted, and generates the video and sync signals necessary to display data on the terminal's screen.

The main logic board is divided into the four following active sections.

1. Main processor
2. Display processor
3. 16K RAM memory
4. I/O Interface logic

POWER SUPPLY

The power supply supplies four DC voltages 12v, -12v, 75v, and 5v to circuits within the terminal. Two fuses located on the power supply are user replaceable.

VIDEO MONITOR

The video monitor contains horizontal, vertical, and video amplification circuits which produce a television-type noninterlaced raster display. Video signals received from the display circuitry generate pixels (dots) at various positions across scan lines. These pixels, when combined with other pixels of scan lines above and/or below a given line, produce characters.

KEYBOARD

Data is encoded by a 8049 microprocessor located in position A6 of the keyboard. The encoded data is sent to the main logic board serially via the coiled interface cable. On the main logic board the serial data is converted to parallel and applied to the main processor which by way of terminal firmware deciphers the two bytes of encoded data received from the keyboard processor.

SECTION 3 TROUBLESHOOTING THE LOGIC BOARD

3.1 VISUAL INSPECTION

With the logic board installed and power removed, remove the two screws at the bottom of the vented cooling tower and swing the bottom part of the panel away from the case, and check the items listed below.

1. Socketed chips: are they all securely seated into their sockets and are the chip pins all straight?

2. Connectors: look for

   Loose, damaged or corroded connectors

   Bad crimps

3. Wires: are any broken, loose or frayed?

4. Components: are any components deformed or discolored?

With the logic board removed, make the following inspections.

To remove the logic board:

1. Turn the power off.

2. On the logic board, carefully disconnect:

   P1, P2, P3, P4 and P5 connectors

3. Remove the four screws in the four corners of the logic board

4. Carefully remove the logic board.

With the logic board removed, closely inspect the board for:

1. Deformed, discolored or missing components.

2. Cracked, broken or lifted traces.

3. Poor solder joints (loose solder balls, cold solder joints, or solder bridges).

4. Bent pins on the IC chips.

NOTE!

If defects are found, correct them and retest the terminal before continuing.

3.2 LSI FAILURES

Since most malfunctions involve LSI chips, this step may quickly remedy most failures. Exchange all socketed chips with known good chips, testing the terminal after exchanging each LSI chip. If the logic board still malfunctions after completeing the previous steps, confirm the operation of the data lines as outlined in the section Data Line Operation.

The remainder of this section involves troubleshooting to the component level and requires schematics, an oscilloscope, a working knowledge of transistor-transistor logic (TTL) with experience in TTL troubleshooting.

3.3 DATA LINE OPERATION

Confirm that the data lines are operating properly before proceeding futher.

NOTE!

It is beyond the scope of this troubleshooting guide to list all possible data line problems.

With the logic board reconnected check the data and address lines that interface the Z80 CPU chip with the rest of the terminal logic. There should be activity on all data and address lines with voltages rangeing from 0v to 5v. If the malfunction persists after you have confirmed proper operation of the data lines, follow the procedure in the next section, Debugging Table.

3.4 SELFTESTS

The following tests are designed to aid the service personel in troubleshooting the 970 terminal.

Two 25 pin male RS232 connectors are needed to make a test cable. The cable is an one to one pin assignment for the following pin requirements:2, 3, 4, 5, 6, 7, 8 and 20. This cable is to be used when testing the comunications of the terminal.

Display tests: Depressing shift SET UP 1 will display all characters and attributes on the screen. Depressing shift SET UP 3, 4 or ESC # 8 will fill the entire screen with one particular character. This test is helpfull when adjusting the terminal focus, height or linearity.

Comunication tests: A test cable as outlined above is required to successfully exercise the test. Connect one end of the test cable to P3 and the other end to P4. Depress shift SET UP 2 or one of the sequences below. The result of the test, PASS or FAIL will be displayed in the lower right of the status line.

Confidence test: Confidence test wil preform certain tests to the terminal. Depress ESC [2 ; Ps y to initiate the test. Ps is the parameter indicating the test to be done. Ps is computed by taking the weight indicated for each desired test and adding them together. The values assigned each test are defined in table 3.1.

TABLE 3-1

WEIGHT	TEST PERFORMED
1	ROM AND RAM TEST (CHECK ROMS' LRC AND TEST DISPLAYABLE RAM)
2	RS-232C PORT TEST (P3-P4 LOOPBACK CONNECTOR REQUIRED)
4	EIA CONTROL TEST (P3-P4 LOOPBACK CONNECTOR REQUIRED)
8	REPEAT SELECTED TEST(S) INDEFINITELY (UNTIL FAILURE OR POWER OFF)

3.5 970 LOGIC BOARD DEBUGGING TABLE

NOTE!

The items listed in the table in this section are only suspect areas; they should not be automatically replaced when the symptoms listed are present.

SYMPTOM	SUSPECT AREAS		SCHEMATIC
	PART NO.	POSITION	PAGE
No video	Z80	A80	#1
	9007	A69	#4
	6116	A56	#5
	74LS166	A50	#5
	74S251	A48	#5
	2N2219	Q3	#6
Constant or no beep	8049(KYBD)	A6	#1
	Z80	A80	#1
	Firmware	A82,87,99	#2
No cursor	9007	A69	#4
	74LS374	A6	#6
Distorted characters	6116	A56	#5
	74LS245	A65	#5
	74LS374	A64	#5
	74LS173	A33	#5
	74LS157	A40	#5
	74LS166	A50	#5
	74S251	A48	#5
	Firmware	A82,87,99	#2
Bad video every other line	9006	A54,60	#8
Bad attribute " "" "	9006	A53,59	#8
Loss of specific attribute	9007	A69	#4
	74LS374	A37,45	#8
Horizontal bar	9007	A69	#4
	74LS32	A68	#4
	74LS32	A7	#9
No transmit P3	75188	A43	#7
	Z80 SIO	A74	#7
	Z80 CTC	A92	#10
No transmit P4	75188	A51	#7
	Z80 SIO	A74	#7
	Z80 CTC	A92	#10

970 DEBUGGING TABLE CONTINUED

SYMPTOM	SUSPECT AREAS		SCHEMATIC
	PART NO.	POSITION	PAGE
No transmit P7	26LS31	A89	#7
	Z80 SIO	A85	#7
	Z80 CTC	A92	#10
No receive P3	75189	A27	#7
	74LS08	A58	#7
	Z80 SIO	A74	#7
	Z80 CTC	A92	#10
No receive P4	75189	A57	#7
	Z80 SIO	A74	#7
	Z80 CTC	A92	#10
No receive P7	26LS32	A84	#7
	Z80 SIO	A85	#7
	Z80 CTC	A92	#10
Incorrect or no kybd response	7414	A100	#7
	Z80 SIO	A85	#7
	Z80 CTC	A92	#10
	74LS138	A93	#9
Incorrect Baud rate	Z80 CTC	A92	#10
	74LS138	A93	#9
	74LS163	A115	#1
Loss of Bidirectional comunication	74LS374	A23	#2
	74LS32	A62	#7

SECTION 4 TROUBLESHOOTING THE KEYBOARD

4.1 VISUAL INSPECTION

Disconnect the keyboard from the rest of the terminal and remove the six screws from the bottom of the keyboard case. Carefully lift of the top of the keyboard case and set it aside.

Check the Key switches for the following:

1. Foreign objects (e.g., paperclips, staples, matches)
2. Liquid residue (e.g., coffee, soft drink)
3. Broken keyswitches
4. Missing or incorrectly placed keycaps

NOTE!

If defects are found, correct them and retest the terminal before continuing.

Visual Inspection with the keyboard removed from the case

Remove the screws from the corners of the keyboard and remove the keyboard from its case.

Inspect the keyboard for:

1. Deformed or discolored components
2. Cracked, shorted, or lifted traces
3. Poor solder joints (loose solder balls, solder bridges, or cold solder joints)

4.2 970 KEYBOARD DEBUGGING TABLE

SYMPTOM	SUSPECT AREAS		SCHEMATIC
	PART NO.	POSITION	PAGE
One key inoperative/ intermittent	Keyswitch		#1
	Open trace,solder joint		#1
	8049 (kybd)	A6	#1
Several keys inoperative/intermittent	Open/shorted trace		#1
	8049	A6	#1
	74LS145	A4,5	#1
	Resistorpack	RP1	#1
All keys inoperative	Open/shorted trace		#1
	8049	A6	#1
	Regulator	VR1	#1
	Crystal	Y1	#1
Incorrect characters	Shorted trace		#1
	8049	A6	#1
No beep or key click	8049	A6	#1

SECTION 5 TROUBLESHOOTING THE VIDEO MONITOR

5.1 VISUAL INSPECTION

With the video monitor installed turn off the power to the terminal, remove the two screws from the rear of the CRT case and place the cover aside. Check the following possible problem areas:

1. Connectors: look for
   - A. Loose or damaged connectors
   - B. Dirty contacts
   - C. Bad crimps
2. Wires: are any broken, loose, or frayed?
3. Components: are any deformed, leaking, or discolored?

If any defects are found, correct them and retest the terminal before continuing.

With the video monitor removed--The following inspections should be made.

To remove the video monitor:

1. With the power off remove and set the cover aside and disconnect the following connections on the video monitor:
   - A. J1 (DC voltages)
   - B. P10 (signal)
   - C. J11 (yoke)
2. Disconnect the following parts on the CRT tube:
   - A. CRT socket (small circuit board at rear of tube) CAUTION pull socket off straight back to avoid breaking the small nipple of tube.
   - B. Anode lead (WARNING see discharge procedure in section one)
   - C. Ground wire
3. Remove the securing screws on the video monitor.
4. Carefully slide the video monitor out of the case.

With the video monitor removed inspect it for:

1. Deformed, leaking, or discolored components
2. Missing or damaged components
3. Cracked or lifted traces
4. Poor solder joints (loose solder balls, solder bridges, or cold solder joints)

NOTE!

If defects are found, correct them and retest the terminal before continuing.

If no defects are found, reinstall the video monitor and apply power.

WARNING!

High voltages are present on the video monitor . USE EXTREME CARE during troubleshooting.

The four adjustments which can be made to the video monitor are listed in Table 5-1. The controls are shown in Figure 5-1.

TABLE 5-1

PROBLEM	CONTROL
Intensity of characters too bright, too dim	Bright
Whole screen is to tall or to short	Height
Characters are not even in height from the top to the bottom of the screen	Linearity
Characters are not in focus	Focus

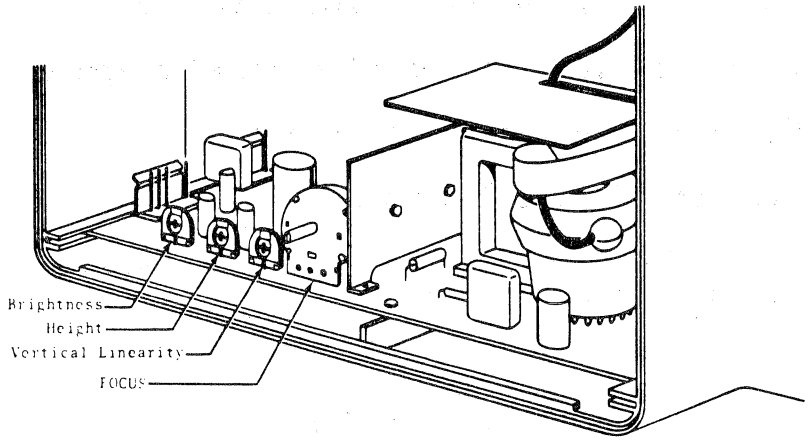


FIGURE 5-1

5.2 VIDEO MONITOR DEBUGGING GUIDE

The remainder of this section deals with specific malfunctions and possible causes.

SYMPTOM: No Vertical Defection

1. Check the emmiter of Q201 for the vert. signal.

   A. If it is present, proceed to step 2.

   B. If it is not present, check the base of Q201.

   C. If the vertical deflection is not present at the base, troubleshoot between the base of Q201 and P10 pin five.

2. Check the collector of Q202 for the vert. signal.

   A. If it is present, proceed to step 3.

   B. If it is not present, check the base of Q202.

   C. If the vertical deflection is not present at the base, troubleshoot back from the base of Q202.

3. Check the negative side of C207 for vertical deflection.

   A. If vetical deflection is present, the vertical drive of the video monitor is good. The following areas should be checked if the vertical deflection continues to fail.

      (1) Connectors P10 and J12
      (2) Yoke windings

   B. Check emmiter of Q203.

   C. Check base of Q203.

   D. If vertical deflection present at base of Q203 suspect Q203.

   E. If not present at base of Q203, troubleshoot back.

   F. If Q203 emmiter is good, check Q204 emmiter.

   G. Check base of Q204.

   H. If vertical deflection present at base of Q204 suspect Q204.

   I. If not present at base, troubleshoot back from Q204. Since Q203 and Q204 are a matched pair of push/pull amplifiers, replace both if one fails.

SYMPTOM: No Horizontal Deflection

1. Check the collector of Q305 for horizontal pulses.

   A. If the pulse is present, proceed to step 2.

   B. If absent check the base of Q305.

   C. If the Horizontal deflection is not present at the base troubeshoot between the base of Q305 and P10 pin one.

2. Check the output of IC301 at pin 3 if absent suspect IC301.

3. Check the collector of Q303 for horizontal pulse.

   A. If present proceed to step 4.

   B. If absent monitor the emmiter of Q303.

   C. If not present at the emmiter troubleshoot back.

4. Check the collector of Q301 for horizontal deflection pulses.

   A. If pulses are present proceed to step 5.

   B. If missing check for a signal at the base of Q301.

   C. If no signal present troubleshoot back.

5. Check the collector of Q302 for the horizontal signal.

   A. If present the horizontal deflection amplifiers are operating properly. Check the connection from J11 to the yoke windings.

   B. If not present check the base of Q302 for the signal.

   C. If the signal is absent at the base of Q302 troubleshoot back.

SECTION 6 TROUBLESHOOTING THE POWER SUUPLY

6.1 VISUAL INSPECTION

With the Power Supply Installed--Turn off power to the terminal, complete the procedure on removal of the logic board, and check the following possible problem areas:

1. Connectors: look for

   A. Loose or damaged connectors

   B. Dirty contacts

   C. Bad crimps

   D. Bad fuse

2. Wires: are any broken, loose, or frayed?

3. Components: are any deformed, leaking, or discolored?

   NOTE!

   Check the fuse with an ohm meter. Do not rely on a visual check.

4. Loose fuse holder

5. If defects are found, correct them and retest the terminal.

With the Power Supply removed--The following inspections should be made.

To remove the power supply:

1. Turn off the power and unplug the power cord from the wall outlet.

2. Remove the main logic board as outlined in section 3.

3. Disconnect K1, K2 on the power supply PCB.

4. Carefully slide the power supply PCB up away from the regulators and remove it.

With the Power Supply Removed--Inspect the power supply for:

1. Deformed, leaking, or discolored components

2. Burned or lifted traces

3. Bad crimps on K1 and K2 connectors

4. Poor connections

If defects are found, correct the defects and retest the terminal before proceeding.

6.2 POWER SUPPLY DEBUGGING GUIDE

The remainder of this section deals with specific malfunctions and possible causes.

SYMPTOM: No +5V DC

1. Remove F103 and check for approximately 34V DC. If the correct voltage is not present, suspect the following components:

   A. D105 through D108

   B. Bad crimps, or poor connections to K1.

2. If the correct voltage is present, suspect the following components:

   A. F103

   B. 80506Z

   C. C106 through C112

SYMPTOM: +5V DC is low

1. Check the following components:

   A. IC103 (80506Z)

   B. C106 through C112

   C. Damaged or loose connectors

SYMPTOM: No +12V DC

1. Remove F102 and check for approximately 26V DC. If the voltage is not present, suspect the following components:

   A. D101 through D104

   B. Bad crimps or poor connections to K1.

2. If the correct voltage is present, suspect the following components:

   A. IC101 (3122P)

   B. Q101

   C. C101, C102, C103, and C116

SYMPTOM: +12V DC is low

1. Check the following components:

   A. R102

   B. IC101 (3122P)

   C. C103

   D. Damaged or loose connectors

SYMPTOM: No -12V DC

1. Check the following components:

   A. D101 through D104

   B. C104 and C105

   C. IC102 (7912)

   D. Damaged or loose connections

SYMPTOM: No +75V DC

1. Check the following components:

   A. D109

   B. C113, C114, and C115

   C. Q102 and Q103

SYMPTOM: +75V DC is low

1. Adjust SFR3

2. If unable to adjust SFR3, check the following components

   A. Q102 and Q103

   B. D110

PRELIMINARY

8048H/8048H-1/8035HL/8035HL-1
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048H/8048H-1 Mask Programmable ROM**
- **8035HL/8035HL-1 CPU Only with Power Down Mode**

- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4 usec and 1.9 usec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM**
  64 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The Intel® 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

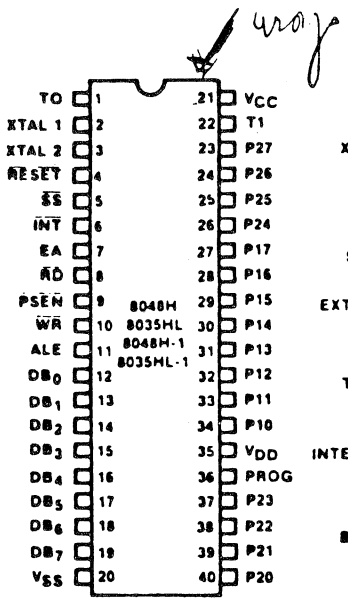
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

To reduce development problems to a minimum and provide maximum flexibility, a logically and functionally pin compatible version of the 8048H with UV-erasable user-programmable EPROM program memory is available. The 8748 will emulate the 8048H up to 6 MHz clock frequency with minor differences.

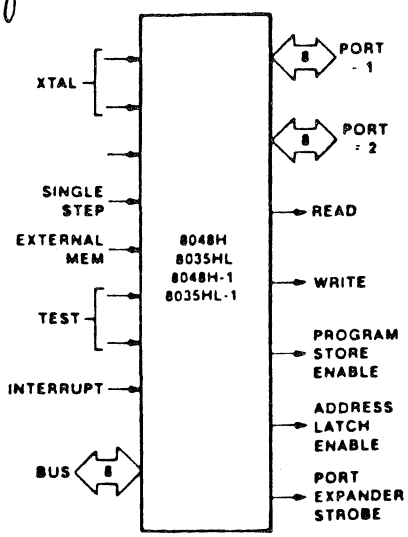
The 8048H is fully compatible with the 8048 when operated at 6 MHz.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

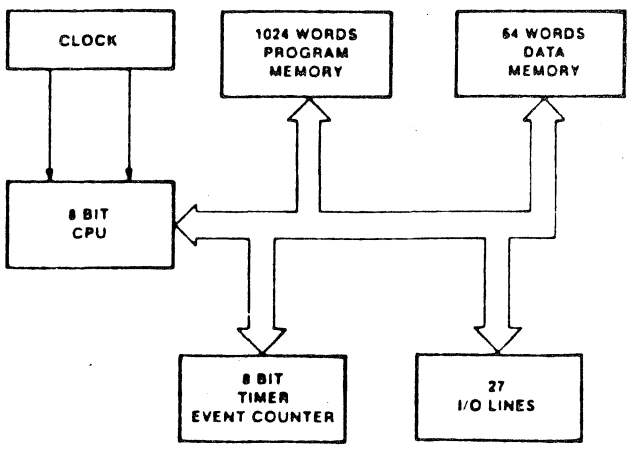
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin =	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24	8-bit quasi-bidirectional port.
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A,P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JTO addr	Jump on TO = 1	2	2
JNTO addr	Jump on TO = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RETR	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	CLear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNT1	Enable timer/counter interrupt	1	1
DIS TCNT1	Disable timer/counter interrupt	1	1

Control

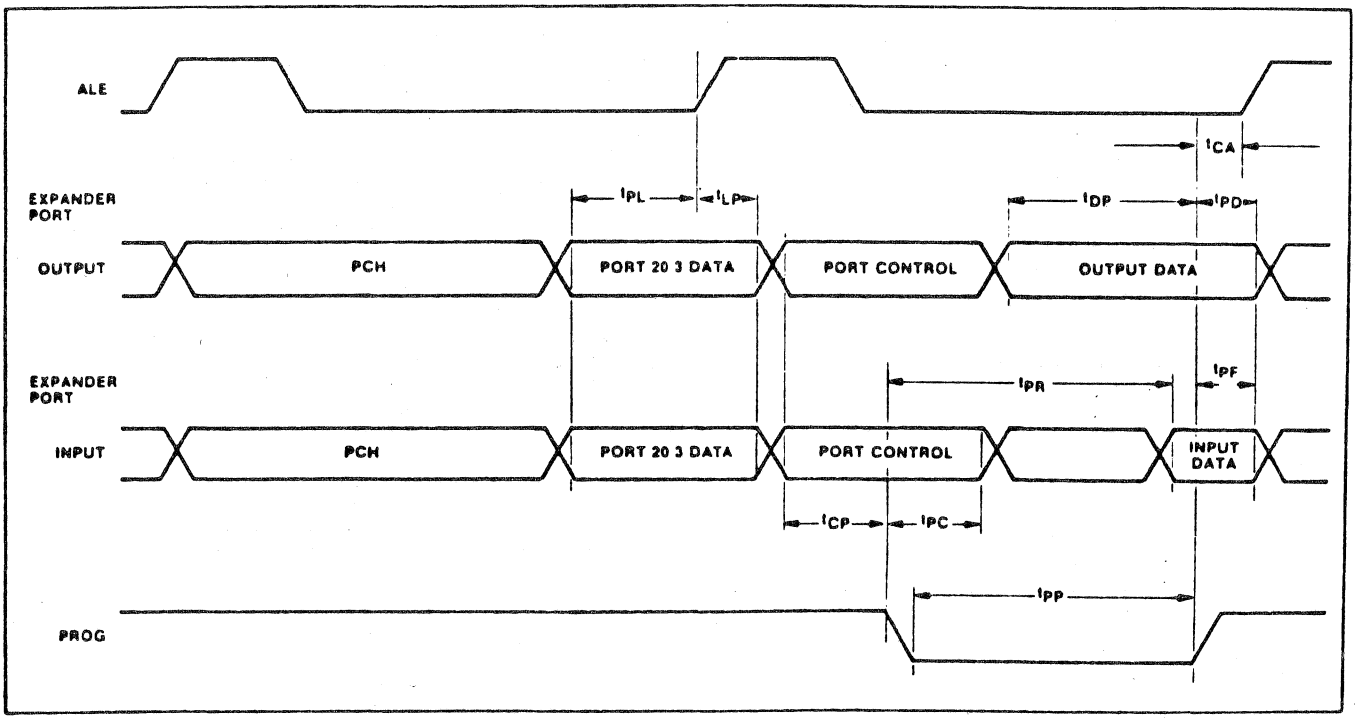
Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT 0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

A.C. CHARACTERISTICS (PORT 2 TIMING) TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit
		6 MHz		8 MHz		11 MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Port control Setup Before Falling Edge of PROG.	110		105				ns
t_{PC}	Port Control Hold After Falling Edge of PROG.	100		90				ns
t_{PR}	PROG to Time P2 Input Must Be Valid		810		700		650	ns
t_{PF}	Input Data Hold Time	0	150	0	150	0	150	ns
t_{DP}	Output Data Setup Time	250		210		200		ns
t_{PD}	Output Data Hold Time	65		35		20		ns
t_{PP}	PROG Pulse Width	1200		970		700		ns
t_{PL}	Port 2 I/O Data Setup	350		300		250		ns
t_{LP}	Port 2 I/O Data Hold	150		65		20		ns

PORT 2 TIMING



BUS TIMING AS A FUNCTION OF TCY *

SYMBOL	FUNCTION OF TCY		
T_{LL}	7/30	T_{CY}	MIN
T_{AL}	1/10	T_{CY}	MIN
T_{LA}	1/15	T_{CY}	MIN
T_{CC} (1)	1/2	T_{CY}	MIN
T_{CC} (2)	2/5	T_{CY}	MIN
T_{DW}	2/15	T_{CY}	MIN
T_{WD}	1/15	T_{CY}	MIN
T_{DR}	0		MIN

T_{CC} (1) : $\overline{RD}/\overline{WR}$
T_{CC} (2) : $\overline{PSEN}$

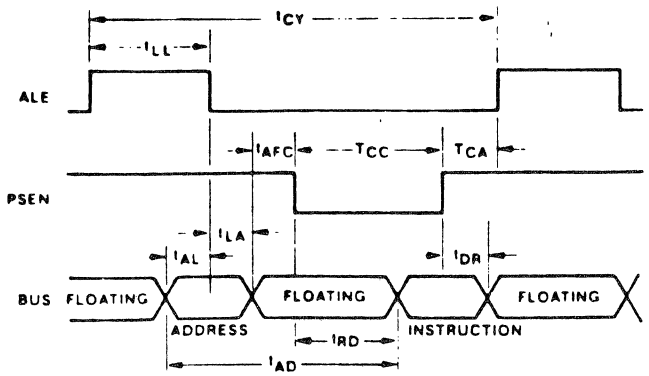
SYMBOL	FUNCTION OF TCY		
T_{RD} (1)	11/30	T_{CY}	MAX
T_{RD} (2)	3/10	T_{CY}	MAX
T_{AW}	3/10	T_{CY}	MIN
T_{AD} (1)	1/2	T_{CY}	MAX
T_{AD} (2)	1/3	T_{CY}	MAX
T_{AFC}	1/30	T_{CY}	MIN
T_{CA}	1/15	T_{CY}	MIN

T_{RD} (1) : $\overline{RD}$
T_{RD} (2) : $\overline{PSEN}$

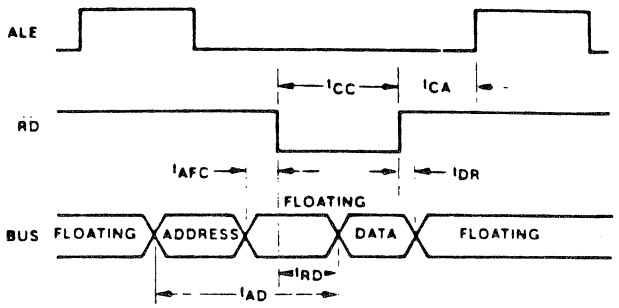
T_{AD} (1) : $\overline{RD}$
T_{AD} (2) : $\overline{PSEN}$

* APPROXIMATE VALUES NOT INCLUDING GATE DELAYS.

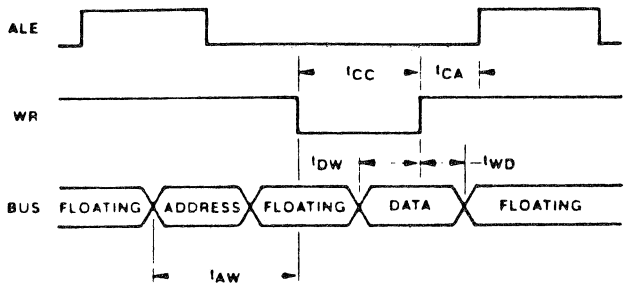
WAVEFORMS



Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory

Input and Output for A.C.Tests

A.C. CHARACTERISTICS TA = 0°C to 70°C VCC = VDD = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit	Conditions (Note 1)
		6 MHz		8 MHz		11 MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		270		150		ns	
t_{AL}	Address Setup to ALE	75		75		70		ns	
t_{LA}	Address Hold from ALE	65		65		50		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700		490		300		ns	
t_{DW}	Data Setup before $\overline{WR}$	370		370		280		ns	
t_{WD}	Data Hold after $\overline{WR}$	80		80		40		ns	CL = 20pF (NOTE 2)
t_{CY}	Cycle Time	2.5		1.875		1.36		μs	
t_{DR}	Data Hold	0	200	0	150	0	100	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		340		200	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		210		200		ns	
t_{AD}	Address Setup to Data In		950		650		400	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		-1		ns	
t_{CA}	Control Pulse to ALE	10		10		0		ns	

NOTE 1: Control outputs CL = 80 pF
BUS outputs CL = 150 pF

NOTE 2: BUS High Impedance Load: 20 pF

PART NUMBER
R6551

Rockwell

R6500 Microcomputer System
DATA SHEET

Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

With the R6551, a crystal is the only required external support component – eliminating the multiple-component support that is typically needed.

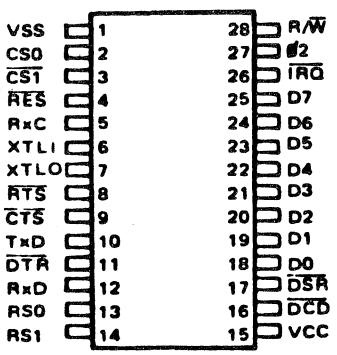
In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and check data, parameters and status.

FEATURES

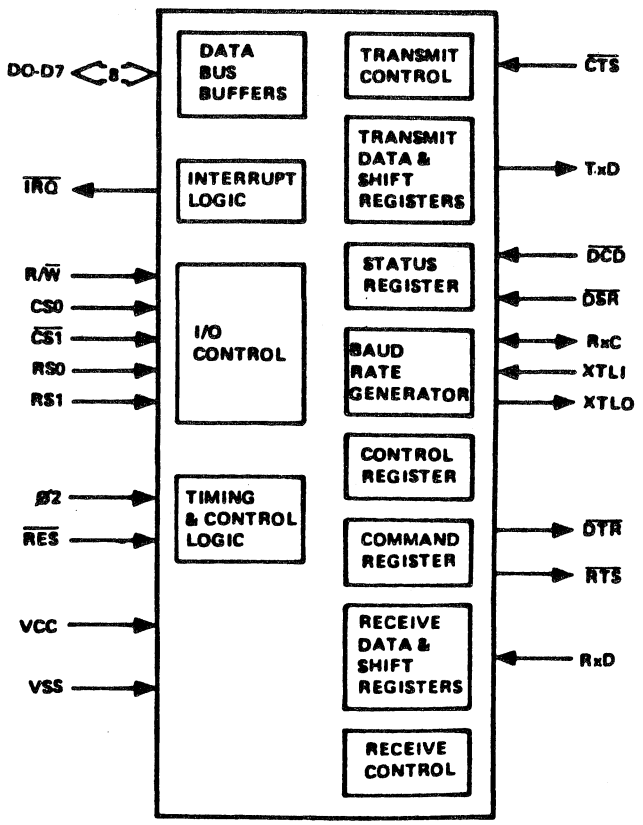
- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6551P	Plastic	1 MHz	0°C to +70°C
R6551AP	Plastic	2 MHz	0°C to +70°C
R6551C	Ceramic	1 MHz	0°C to +70°C
R6551AC	Ceramic	2 MHz	0°C to +70°C



R6551 Pin Configuration

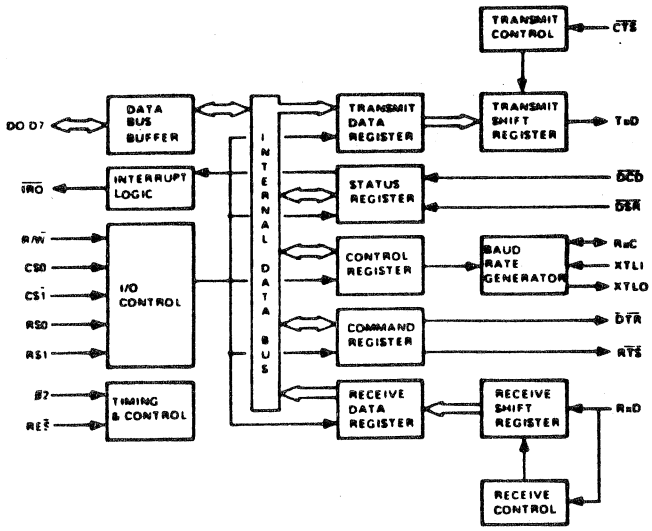


R6551 Interface Diagram

Asynchronous Communication Interface Adapter (ACIA)

Specifications subject to change without notice
Document No. 29000 D53
Rev. 1, January 1981

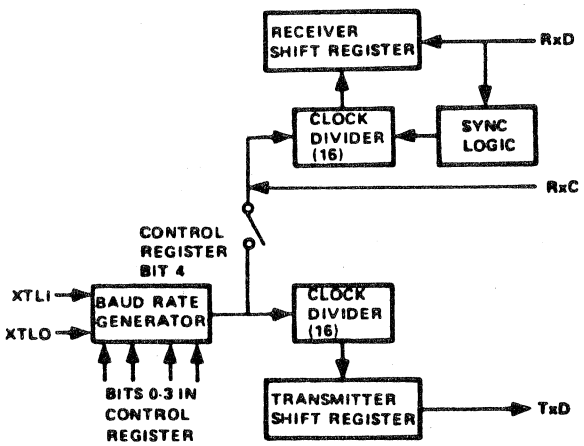
INTERNAL ORGANIZATION



R6551 Block Diagram

Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.



Transmitter/Receiver Clock Circuits

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

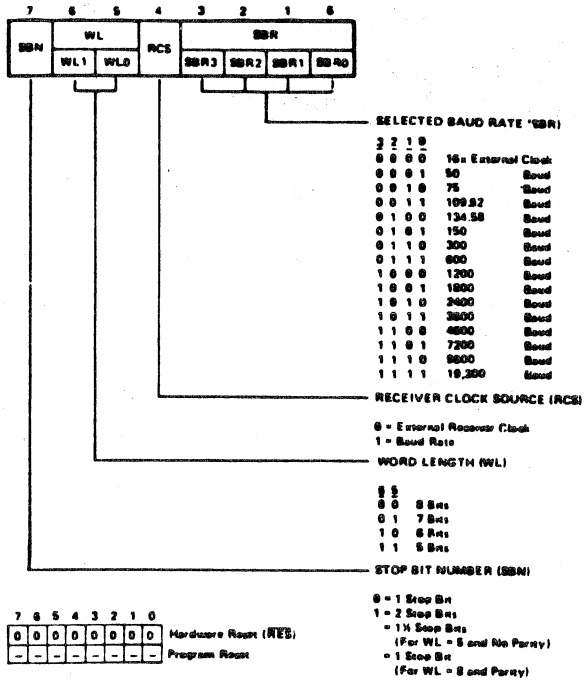
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Control Register

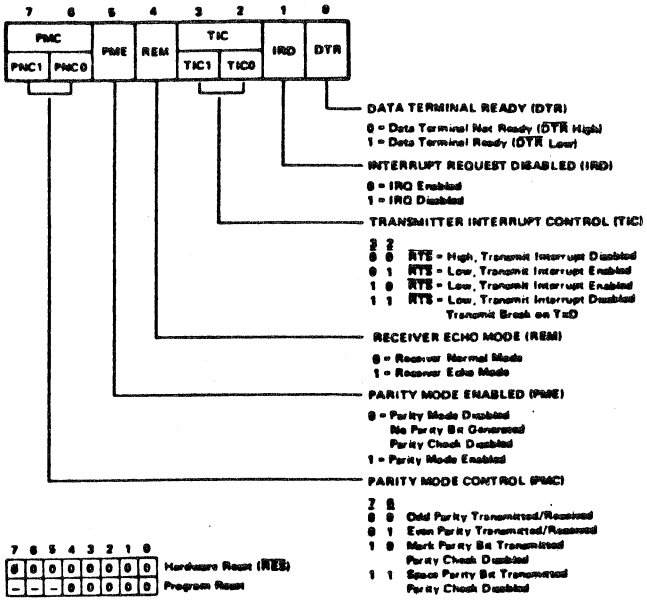
The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.



R6551 Control Register

Command Register

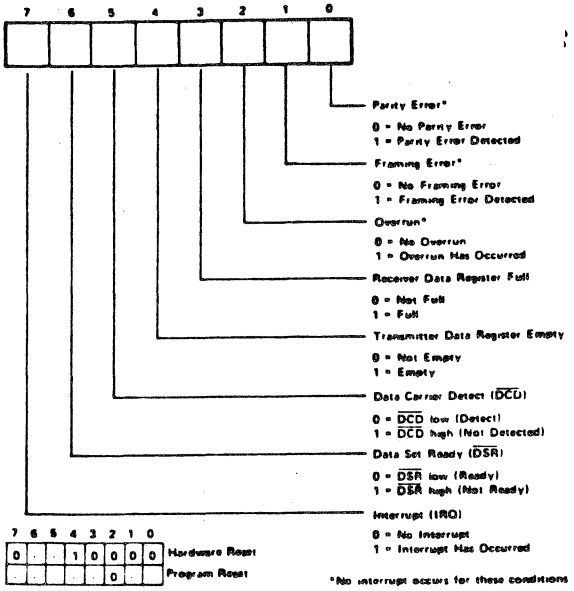
The Command Register controls specific modes and functions.



R6551 Command Register

Status Register

The Status Register reports the status of various R6551 functions



R6551 Status Register

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

Ø2 (Input Clock)

The input clock is the system Ø2 clock and is used to synchronize all data transfers between the system microprocessor and the R6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6551. A low on the R/$\overline{W}$ pin allows a write to the R6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

D0-D7 (Data Bus)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance, except during Read cycles when the R6551 is selected.

CS0, $\overline{CS1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and $\overline{CS1}$ is low.

RS0, RS1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear Bits 0 through 4 in the Command Register and Bit 2 in the Status Register. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTLI, XTLO (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the Control Register).

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the Control Register).

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input, and must be connected. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect)

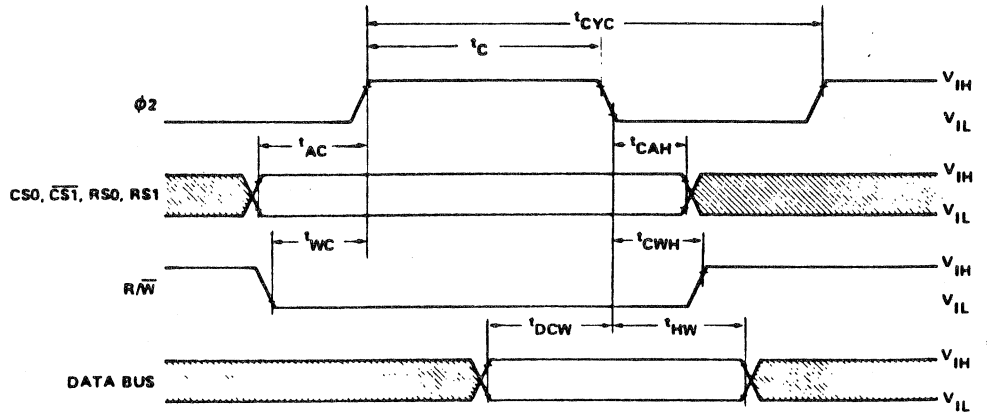
The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. Like $\overline{DSR}$, $\overline{DCD}$ is a high-impedance input, and must be connected.

READ/WRITE CYCLE CHARACTERISTICS

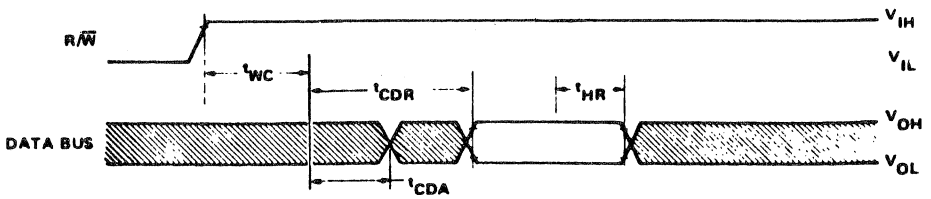
(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Ø2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{AC}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)



Write Timing Characteristics



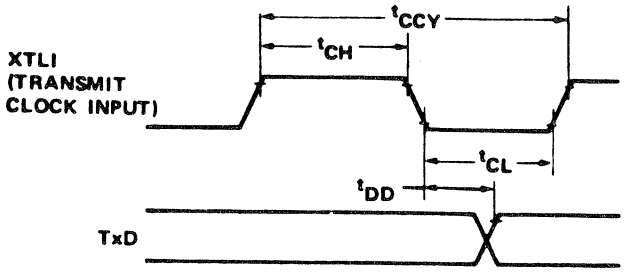
Read Timing Characteristics

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTLI to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
$\overline{RTS}$ Propagation Delay	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

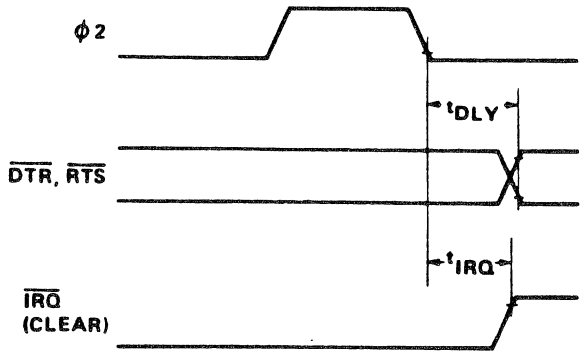
(t_r, t_f = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

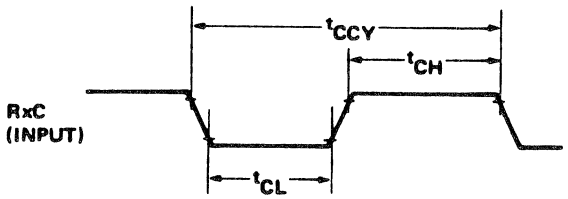


NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock



Interrupt and Output Timing

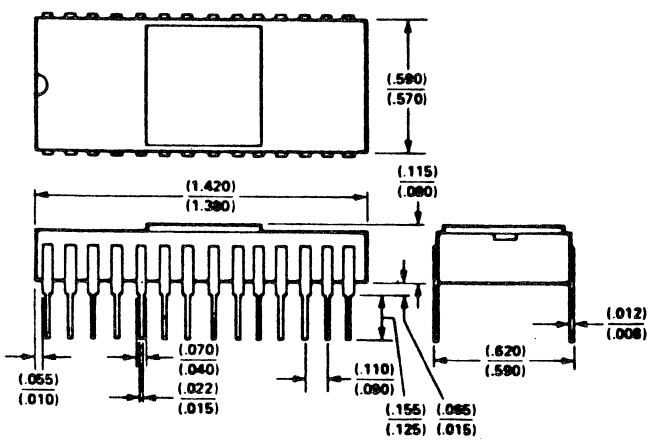


NOTE: RxD rate is 1/16 RxC rate

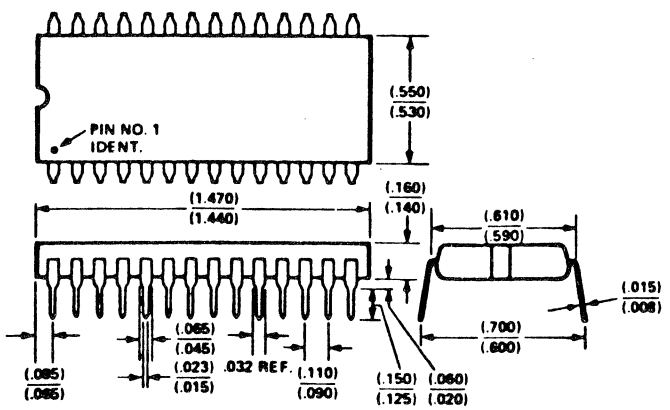
Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



DOCUMENT NO. 29000 D39
REV. 3, FEBRUARY 1979

PART NUMBER
R650X and R651X

Rockwell

R6500 Microcomputer System DATA SHEET

R6500 MICROPROCESSORS (CPU's)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Output

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

Ordering Information

Order Number: R65XX___

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = −40°C to +85°C (Industrial)
  - MT = −55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

NOTE: Contact your local Rockwell Representative concerning availability.

R6500 Signal Description

Clocks (ϕ_1, ϕ_2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A0-A15)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA).

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3K Ω register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 and must be externally synchronized.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

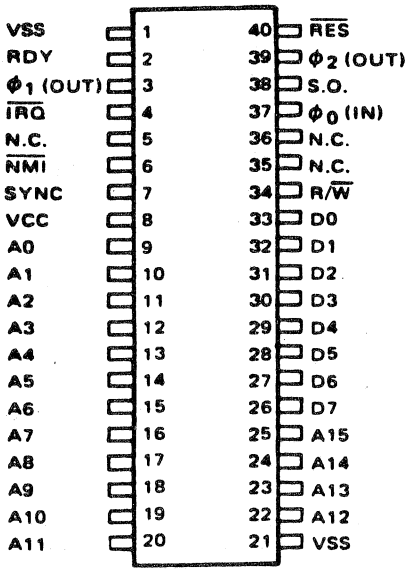
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

R6502 – 40 Pin Package



Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt

INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← 7 6 5 4 3 2 1 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							• • 0 • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																															M_7 M_6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • •	CLV
CMP	A - M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X - M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y - M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M - 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X - 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y - 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → 7 6 5 4 3 2 1 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S - 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S - 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	7 6 5 4 3 2 1 0 ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	C → 7 6 5 4 3 2 1 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A - M - $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																														96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED

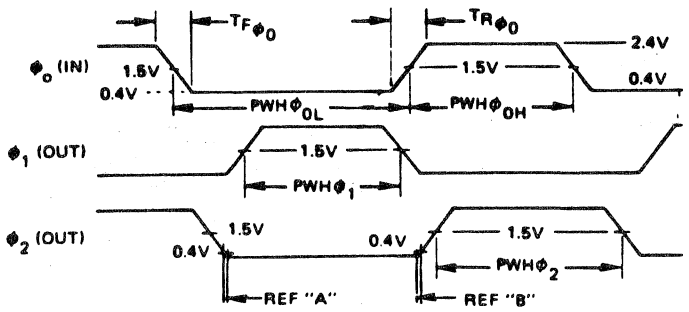
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

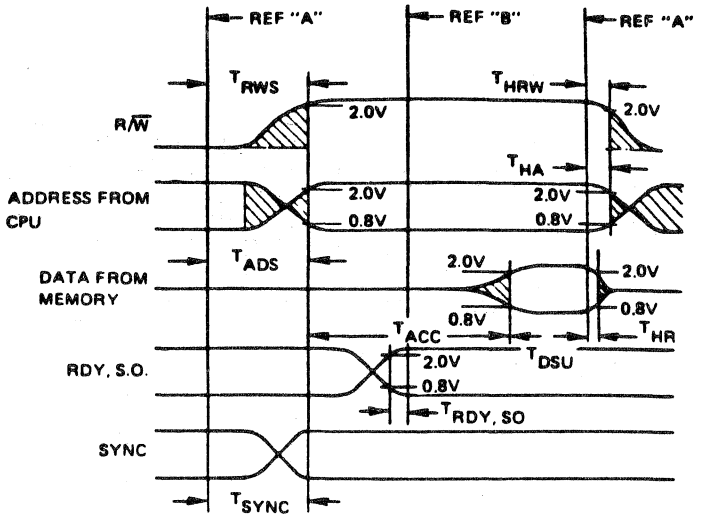
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M_7	MEMORY BIT 7
Y	INDEX Y	-	SUBTRACT	M_6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO BYTES
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR		

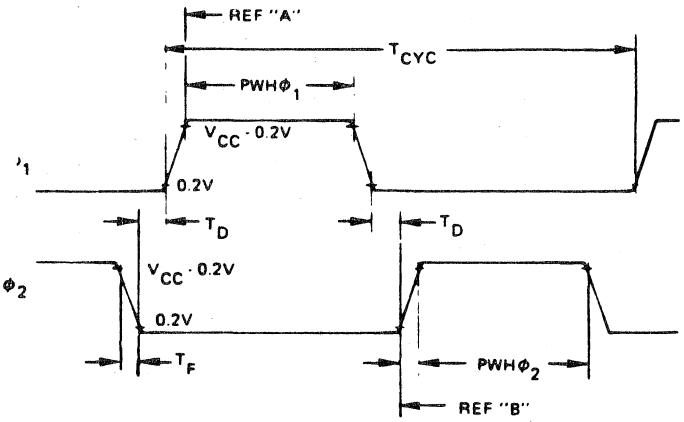
Clock Timing – R6502, 03, 04, 05, 06, 07



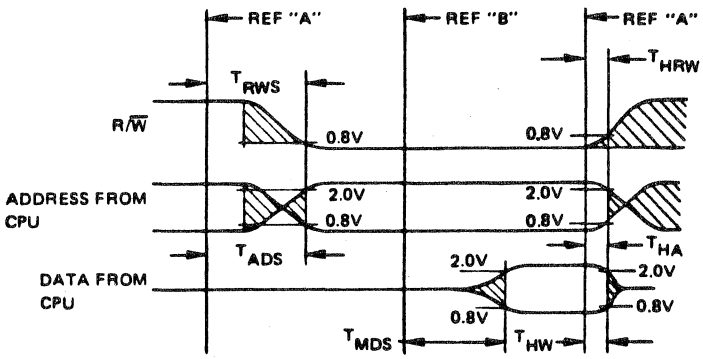
Timing for Reading Data from Memory or Peripherals



Clock Timing – R6512, 13, 14, 15

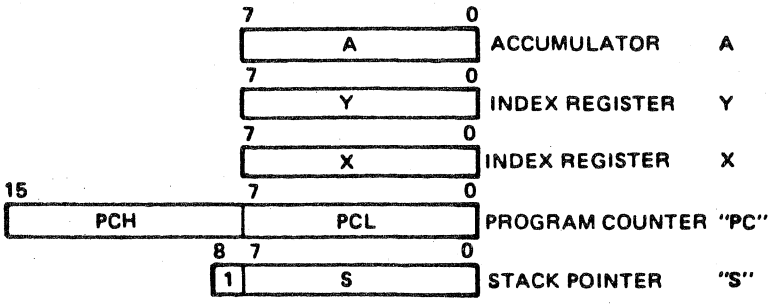


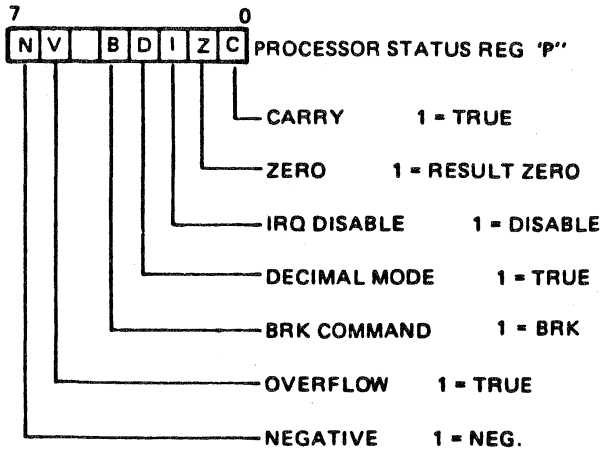
Timing for Writing Data to Memory or Peripherals

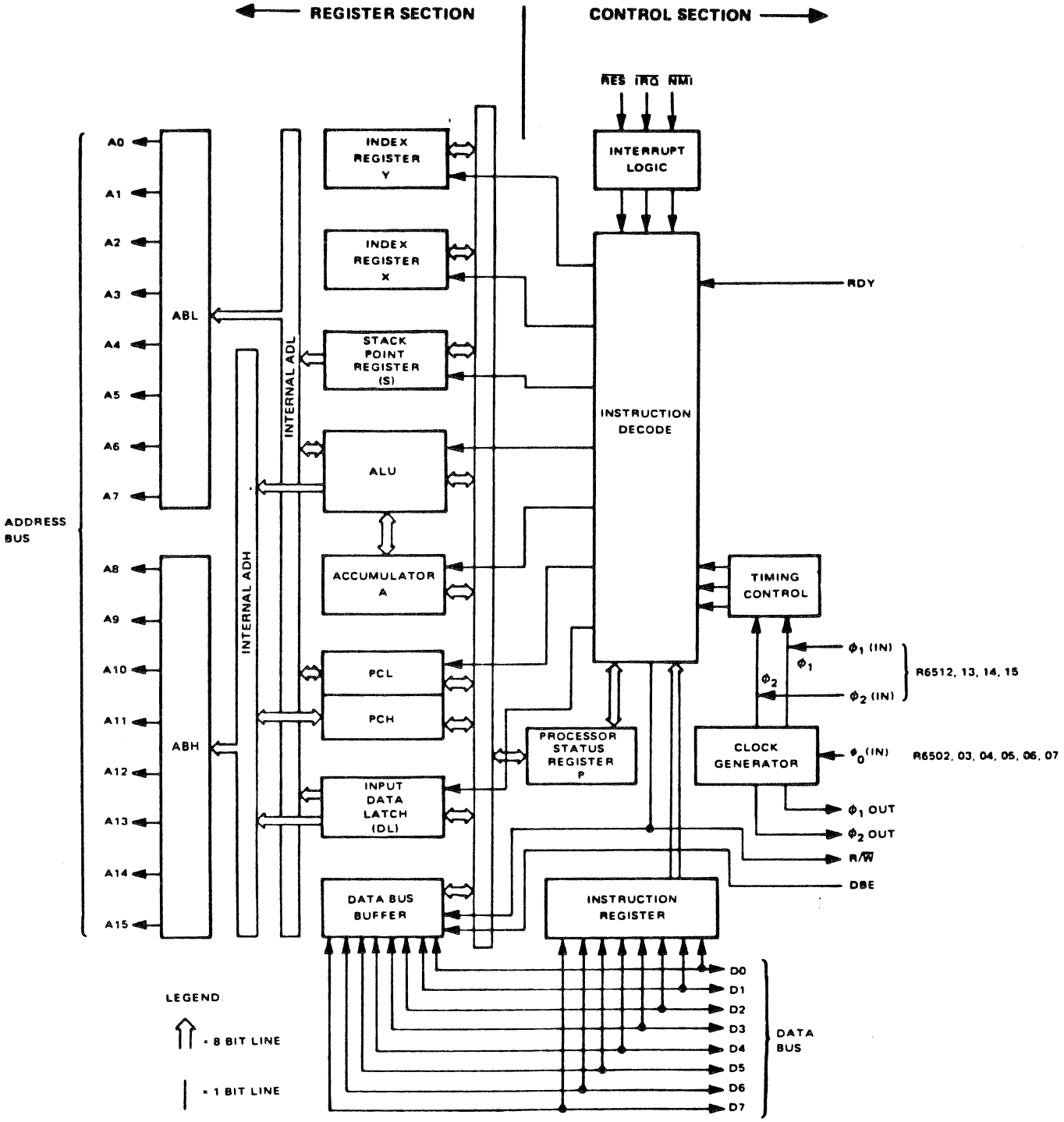


Note: "REF." means Reference Points on clocks.

PROGRAMMING MODEL







Note 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

R6500 Internal Architecture

DOCUMENT NO. 29000 D47
REVISION 1, OCT. 1978

PART NUMBER
R6522

Rockwell

R6500 Microcomputer System
DATA SHEET

VERSATILE INTERFACE ADAPTER (VIA)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . . as well as low-cost design aids and documentation.

DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

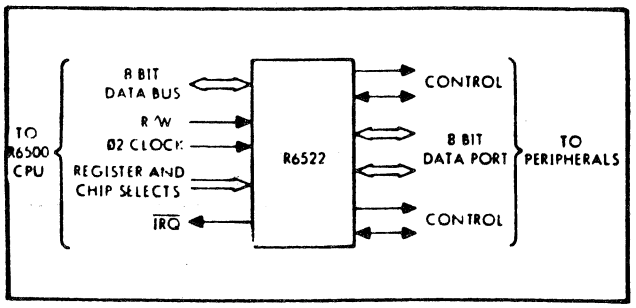
Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization: Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers.

FEATURES

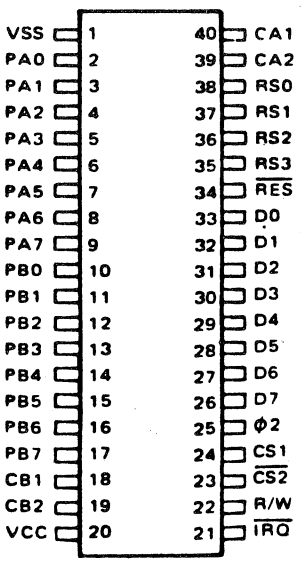
- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6522P	Plastic	1 MHz	0°C to +70°C
R6522AP	Plastic	2 MHz	0°C to +70°C
R6522C	Ceramic	1 MHz	0°C to +70°C
R6522AC	Ceramic	2 MHz	0°C to +70°C
R6522PE	Plastic	1 MHz	-40°C to +85°C
R6522APE	Plastic	2 MHz	-40°C to +85°C
R6522CE	Ceramic	1 MHz	-40°C to +85°C
R6522ACE	Ceramic	2 MHz	-40°C to +85°C
R6522CMT	Ceramic	1 MHz	-55°C to +125°C



Basic R6522 Interface Diagram



Pin Configuration

R6522 VERSATILE INTERFACE ADAPTER (VIA)

Specifications subject to change without notice

OPERATION SUMMARY

Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks	RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB		H	L	L	L	T2L-L T2C-L	Write Latch Read Counter
L	L	L	H	ORA	Controls Handshake						
L	L	H	L	DDRB		H	L	L	H	T2C-H	Triggers T2L-L/T2C-L Transfer
L	L	H	H	DDRA							
						H	L	H		SR	
L	H	L	L	T1L-L T1C-L	Write Latch Read Counter	H	L	H	H	ACR	
						H	H	L	L	PCR	
L	H	L	H	T1C-H	Trigger T1L-L/T1C-L Transfer	H	H	L	H	IFR	
						H	H	H	L	IER	
L	H	H	L	T1L-L		H	H	H	H	ORA	No Effect on Handshake
L	H	H	H	T1L-H							

Note: L = 0.4V DC, H = 2.4V DC.

Timer 2 Control

RS3	RS2	RS1	RS0	R/W = L	R/W = H
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

Writing the Timer 1 Register

The operations which take place when writing to each of the four T1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation (R/W = L)
L	H	L	L	Write into low order latch
L	H	L	H	Write into high order latch Write into high order counter Transfer low order latch into low order counter Reset T1 interrupt flag
L	H	H	L	Write low order latch
X	H	H	H	Write high order latch Reset T1 interrupt flag

Reading the Timer 1 Registers

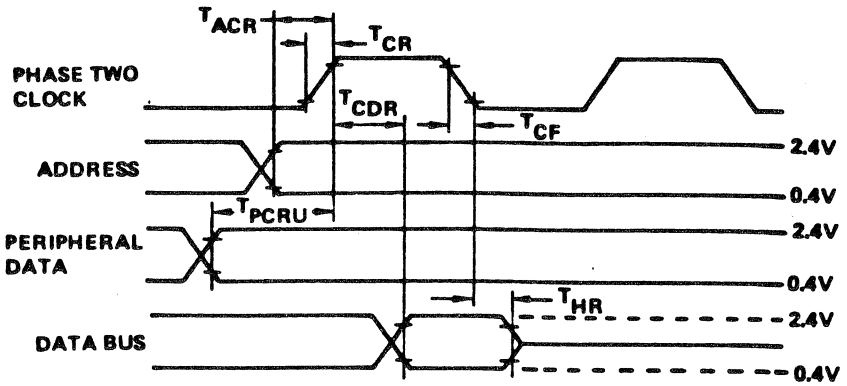
For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter Reset T1 interrupt flag
L	H	L	H	Read T1 high order counter
L	H	H	L	Read T1 low order latch
L	H	H	H	Read T1 high order latch

TIMING CHARACTERISTICS

Read Timing Characteristics (loading 130 pF and one TTL load)

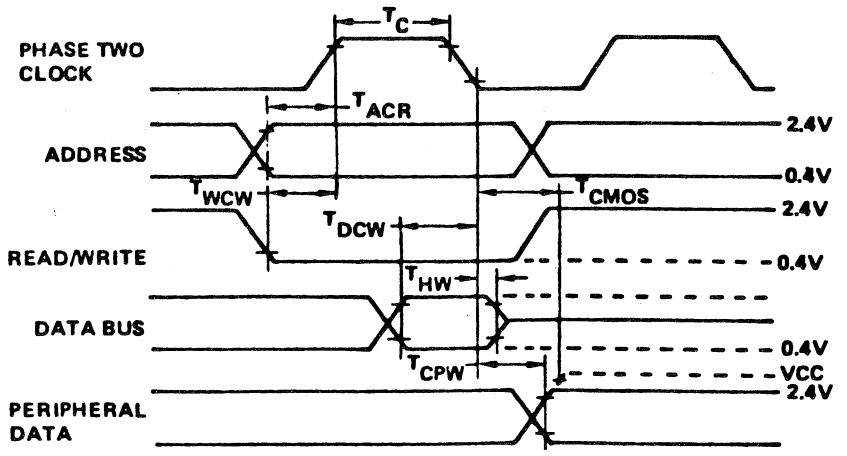
Parameter	Symbol	Min	Typ	Max	Unit
Delay time, address valid to clock positive transition	T_{ACR}	180	–	–	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	–	–	395	nS
Peripheral data setup time	T_{PCR}	300	–	–	nS
Data bus hold time	T_{HR}	10	–	–	nS
Rise and fall time for clock input	T_{RC} T_{RF}	–	–	25	nS



Read Timing Characteristics

Write Timing Characteristics

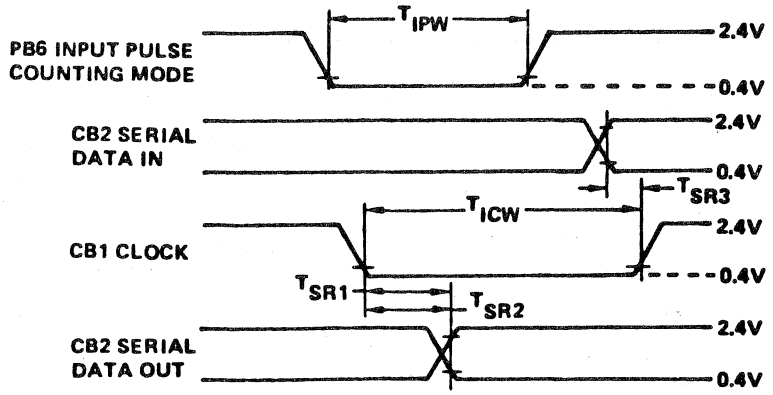
Parameter	Symbol	Min	Typ	Max	Unit
Enable pulse width	T_C	0.47	–	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	–	–	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	–	–	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	–	–	nS
Data bus hold time	T_{HW}	10	–	–	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	–	–	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (VCC - 30%)	T_{CMOS}	–	–	2.0	μS



Write Timing Characteristics

I/O Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2 and CB2 input signals	T_{RF}	–	–	1.0	μs
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode)	T_{CA2}	–	–	1.0	μs
Delay time, clock negative transition to CA2 positive transition (pulse mode)	T_{RS1}	–	–	1.0	μs
Delay time, CA1 active transition to CA2 positive transition (handshake mode)	T_{RS2}	–	–	2.0	μs
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake)	T_{WHS}	–	–	1.0	μs
Delay time, peripheral data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode)	T_{RS3}	–	–	1.0	μs
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode)	T_{RS4}	–	–	2.0	μs
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching)	T_{IL}	300	–	–	ns
Delay time CB1 negative transition to CB2 data valid (internal SR clock, shift out)	T_{SR1}	–	–	300	ns
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out)	T_{SR2}	–	–	300	ns
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	–	–	300	ns
Pulse Width – PB6 Input Pulse	T_{IPW}	2	–	–	μs
Pulse Width – CB1 Input Clock	T_{ICW}	2	–	–	μs
Pulse Spacing – PB6 Input Pulse	I_{IPS}	2	–	–	μs
Pulse Spacing – CB1 Input Pulse	I_{ICS}	2	–	–	μs



I/O Timing Characteristics

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded
0	1	Generate continuous interrupts
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation
1	1	Generate continuous interrupts and a square wave output on PB7

FUNCTION CONTROL

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the Interval Timers (T1, T2), and the Serial Port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Typical functions are shown below:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode – Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode – Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
0	1	0	Input mode – Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	Independent interrupt input mode – Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode – Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse output mode – CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode – The CA2 output is held low in this mode.
1	1	1	Manual output mode – The CA2 output is held high in this mode.

Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The Auxiliary Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

Rockwell

R6500 Microcomputer System
DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

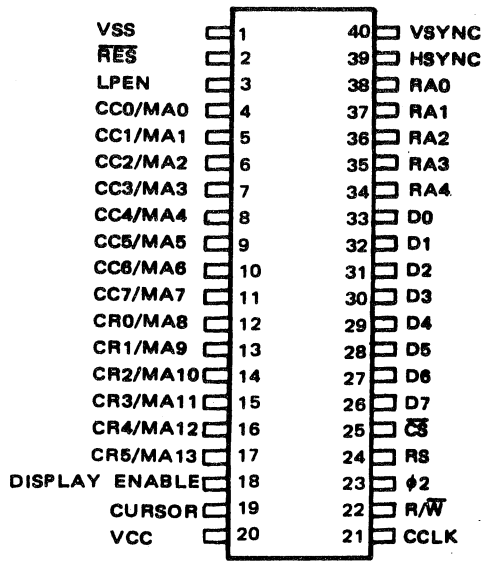
The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply



R6545-1 Pin Configuration

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C

Specifications subject to change without notice
Document No. 29000 D67
December 1980

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The input clock is the system Phase 2 (ϕ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/$\overline{W}$ = low) into the Address Register and reads (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency. $\overline{RES}$ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

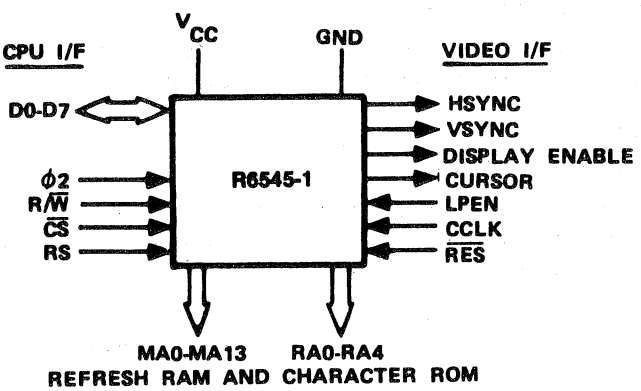
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Reg. No.	Register Name	Register Units	Read (R/$\overline{W}$ = High)	Write (R/$\overline{W}$ = Low)	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓				4	3	2	1	0
0	0	X	X	X	X	X	X	Status Register	—	✓			6	5					
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control	—		✓	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓		6	5	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓				4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Address (H)	—		✓			5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Address (L)	—		✓	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	—	✓	✓			5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	—	✓	✓	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Register (H)	—	✓				5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Register (L)	—	✓		7	6	5	4	3	2	1	0

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

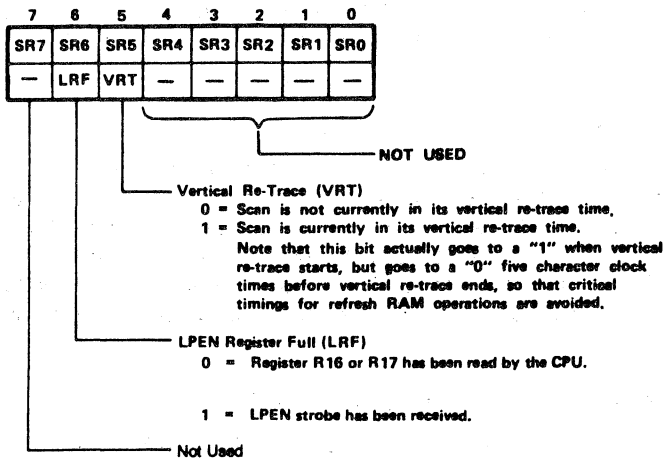
INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When $\overline{CS}$ and RS are low, then this register may be loaded; when $\overline{CS}$ is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:



NOTE: The Status Register takes the State, | – | 0 | 1 | – | – | – | – | – |

immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

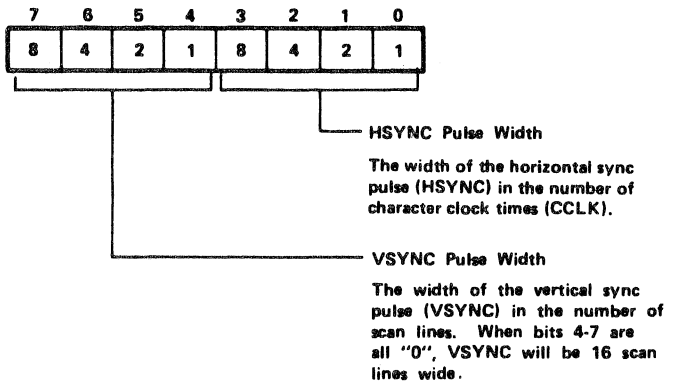
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

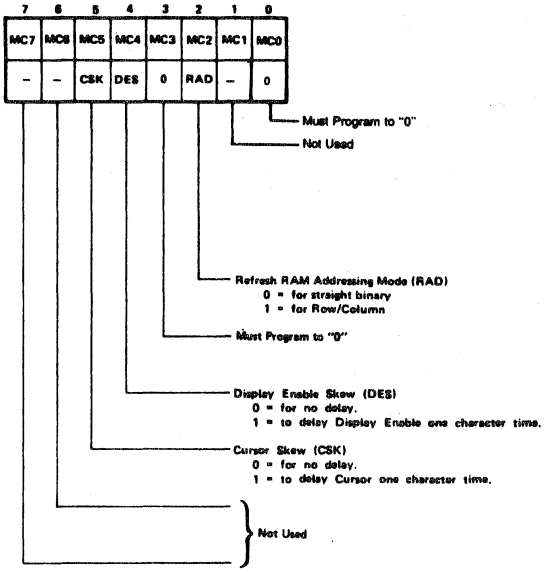
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE
R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH
R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

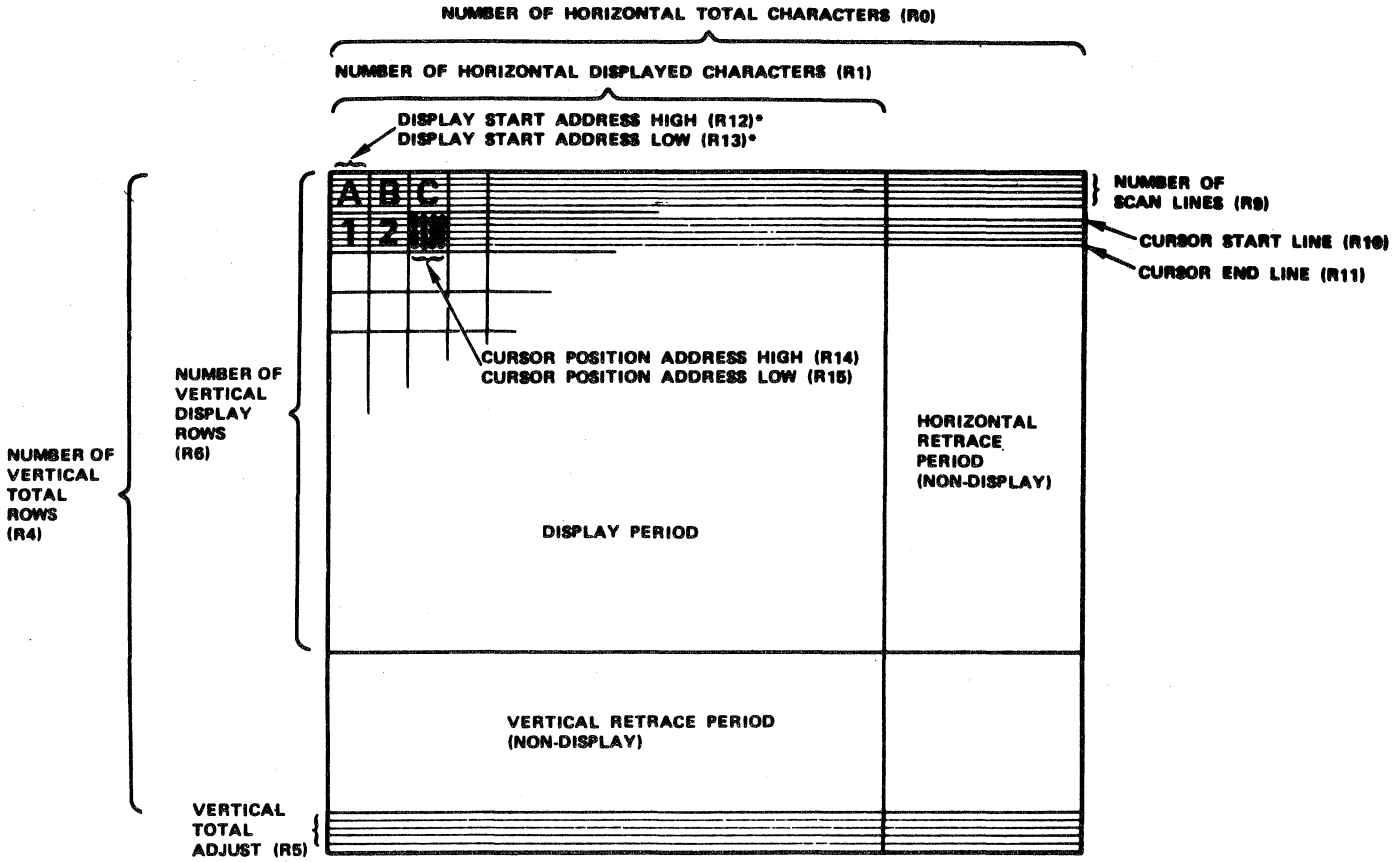


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH
R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH
R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = "0".

(2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	3		76	77	78	79	80	81		89
80	81	82	83		156	157	158	159	160	161		169
160	161	162				237	238	239	240			249
240	241	242				317	318	319	320			329
1680	1681	1682				1757	1758	1759	1760			1769
1760	1761	1762				1837	1838	1839	1840			1849
1840	1841	1842				1917	1918	1919	1920			1929
1920	1921	1922				1997	1998	1999	2000			2009
2000	2001	2002				2077	2078	2079	2080			2089
2640	2641	2642				2717	2718	2720				2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

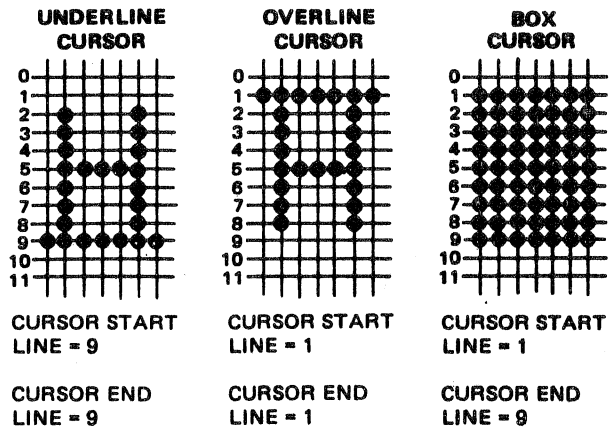


Figure 3. Cursor Display Scan Line Control Examples

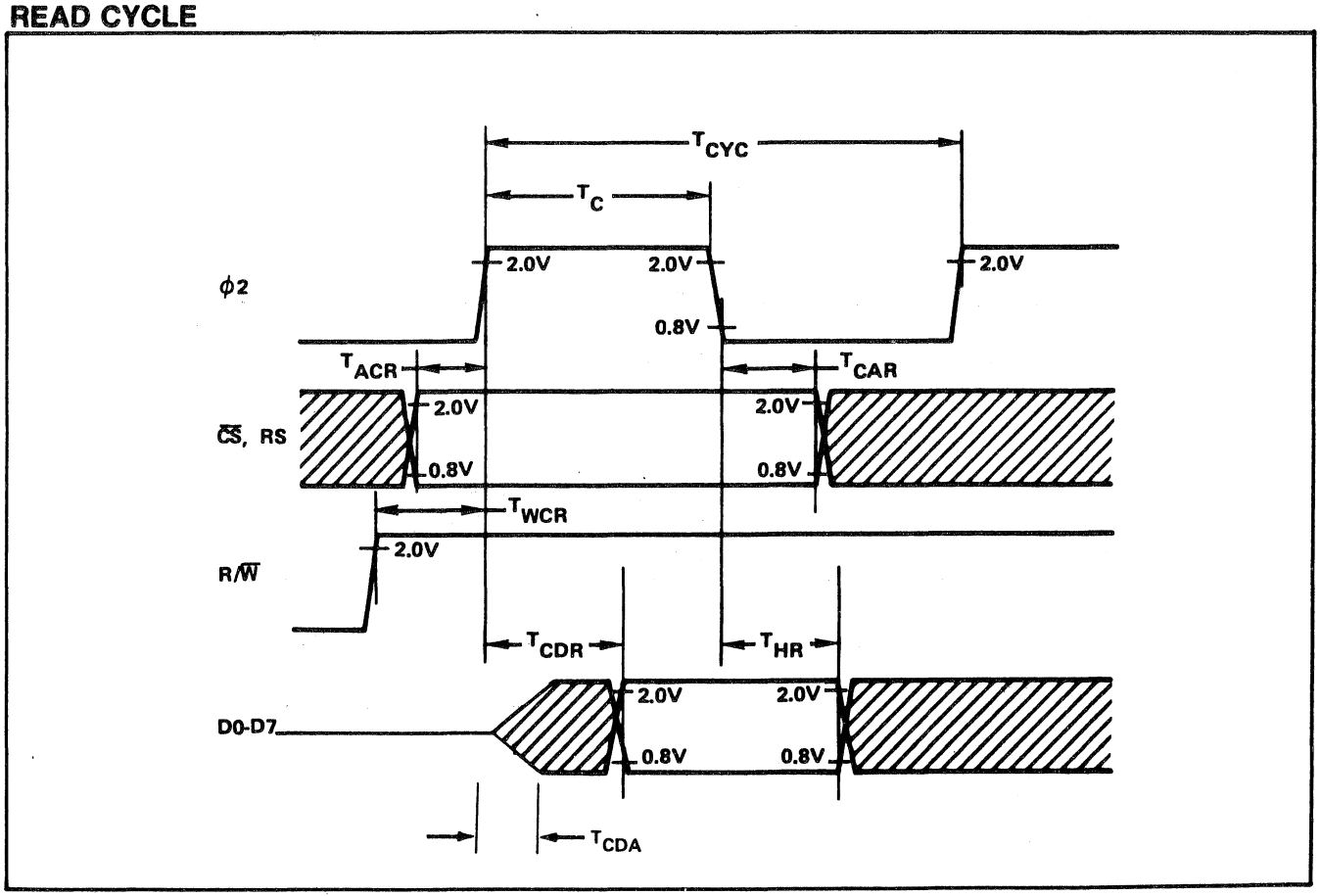
MPU READ TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACR}	180	–	90	–	ns
Address Hold Time	T_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCR}	180	–	90	–	ns
Read Access Time	T_{CDR}	–	340	–	150	ns
Read Hold Time	T_{HR}	10	–	10	–	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

READ CYCLE



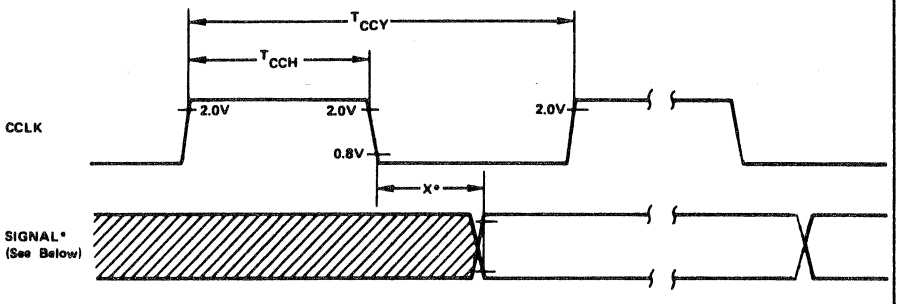
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCY}	0.4	40	0.4	40	µs
Char. Clock Pulse Width	T_{CCH}	200	–	200	–	ns
MA0-MA13 Propagation Delay	T_{MAD}	–	300	–	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	–	300	–	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	–	450	–	450	ns
HYSNC Propagation Delay	T_{HSD}	–	450	–	450	ns
VSYNC Propagation	T_{VSD}	–	450	–	450	ns
Cursor Propagation Delay	T_{CDD}	–	450	–	450	ns
LPEN Strobe Width	T_{LPH}	150	–	150	–	ns
LPEN to CCLK Delay	T_{LP1}	20	–	20	–	ns
CCLK to LPEN Delay	T_{LP2}	0	–	0	–	ns

t_r, t_f = 20 ns (max)

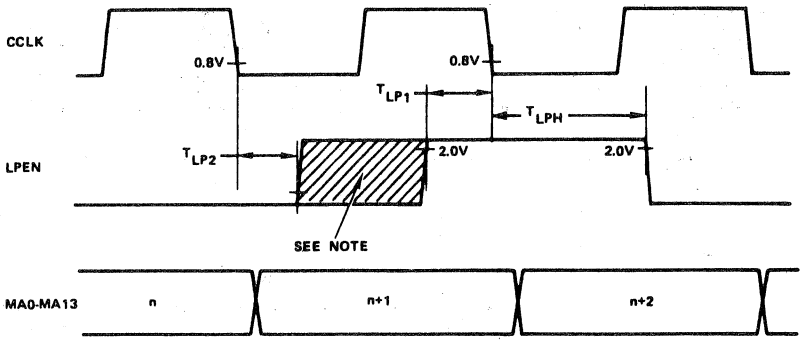
SYSTEM TIMING DEFINITIONS



*

SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

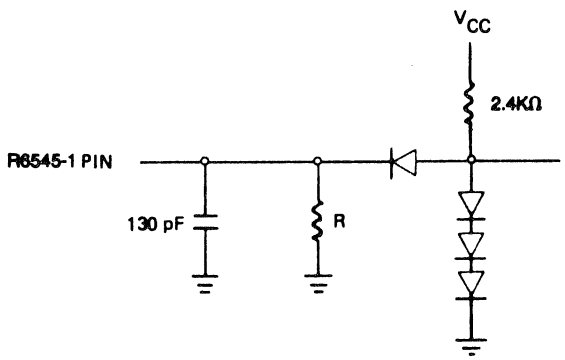
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	–	2.5	μAdc
Three-State Input Leakage (D0-D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	–	10.0	μAdc
Output High Voltage I_{LOAD} = 205 μAdc (D0-D7) I_{LOAD} = 100 μAdc (all others)	V_{OH}	2.4	–	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	–	0.4	Vdc
Power Dissipation	P_D	–	1000	mW
Input Capacitance				
Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	C_{IN}	–	10.0	pF
D0-D7		–	12.5	pF
Output Capacitance	C_{OUT}	–	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

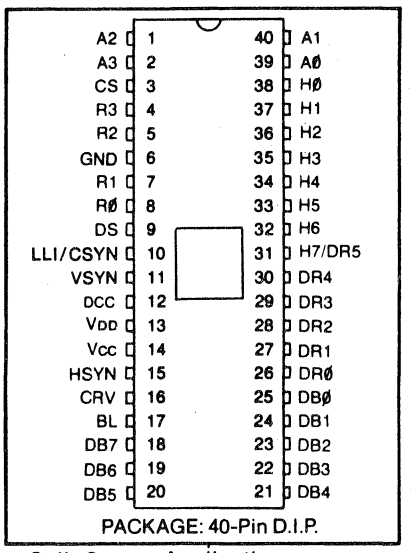
CRT 5027
CRT 5037
CRT 5057*
μPC FAMILY

CRT Video Timer and Controller VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Lock Line Input (CRT 5057)
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync (CRT 5027, CRT 5037)
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)
- ☐ Graphics Compatible

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

SECTION IV

GENERAL DESCRIPTION

The CRT Video Timer and Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

Three versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

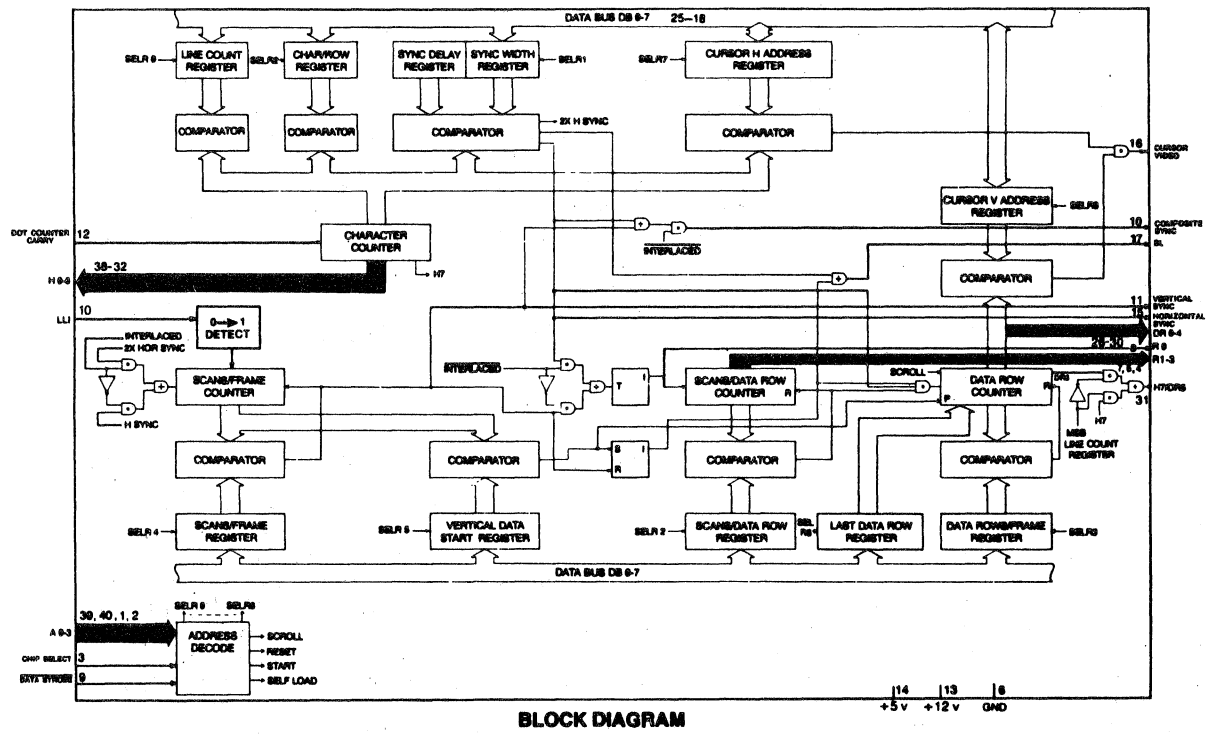
The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's® vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to the line lock input. The VTAC® will inhibit generation of vertical sync until a zero to one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.®

To provide the pin required for the line lock input, the composite sync output is not provided in the CRT 5057.

*FOR FUTURE RELEASE

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≥128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN/ LLI	Composite Sync Output/ Line Lock Input	O/I	Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057, this pin is the Line Lock Input. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to this pin.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply



BLOCK DIAGRAM

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 15 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Control Registers Programming Chart

Horizontal Line Count: Total Characters/Line = N + 1, N = 0 to 255 (DB0 = LSB)

Characters/Data Row:

DB2	DB1	DB0		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: = N, from 1 to 7 character times (DB0 = LSB) (N = 0 Disallowed)

Horizontal Sync Width: = N, from 1 to 15 character times (DB3 = LSB) (N = 0 Disallowed)

Skew Bits

DB7	DB8	Sync/Blank Delay (Character Times)	Cursor Delay (Character Times)
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations:
Let X = value of 8 assigned bits. (DB0 = LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.

Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).

Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (=3H).

Vertical Data Start: N = number of raster lines delay after leading edge of vertical sync of vertical start position. (DB0 = LSB)

Data Rows/Frame: Number of data rows = N + 1, N = 0 to 63 (DBO = LSB)

Last Data Row: N = Address of last dsplayed data row, N = 0 to 63, ie; for 24 data rows, program N = 23. (DB0 = LSB)

Mode: Register, 1, DB7 = 1 establishes Interlace.

Scans/Data Row:

Interlace Mode

CRT 5027: Scans per Data Row = N + 1 where N = programmed number of data rows. N = 0 to 15. Scans per data row must be even counts only.

CRT 5037, CRT 5057: Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

CRT 5027, CRT 5037, CRT 5057: Scans per Data Row = N + 1, odd or even count. N = 0 to 15.

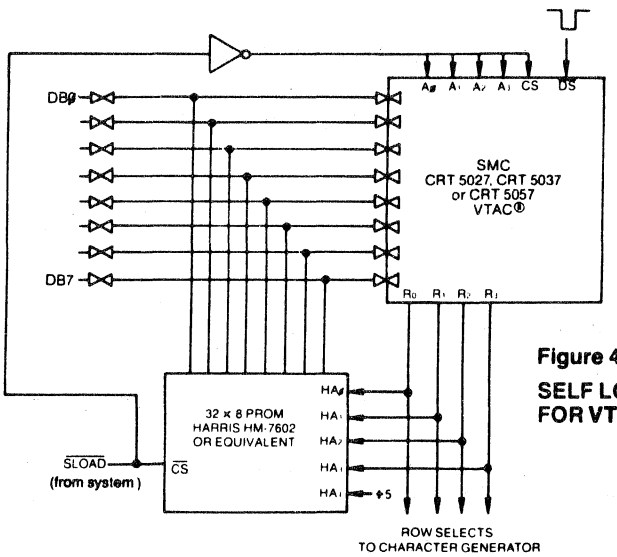


Figure 4.

SELF LOADING SCHEME FOR VTAC® SET-UP

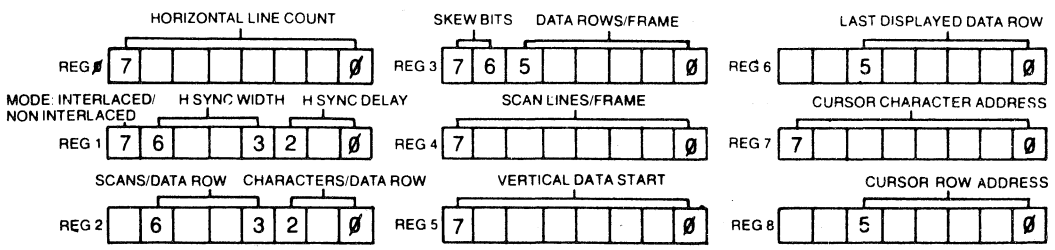
Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing VTAC® to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address*	
1	1	0	1	Load Cursor Line Address*	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VTAC®, the Dot Counter Carry should be held low when the command is removed.

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

TABLE 1

BIT ASSIGNMENT CHART



AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

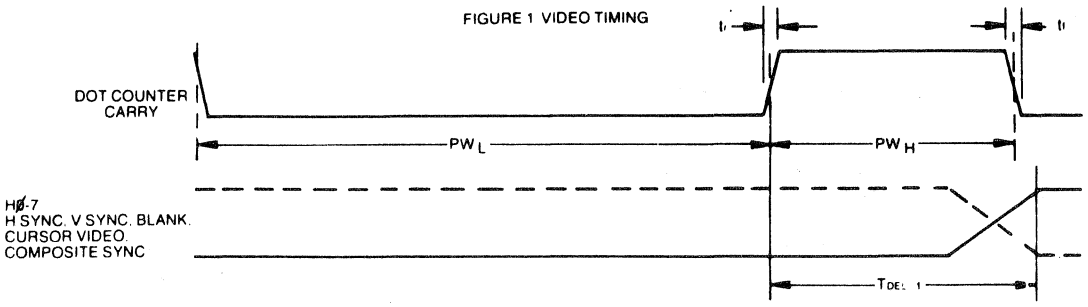


FIGURE 2 LOAD/READ TIMING

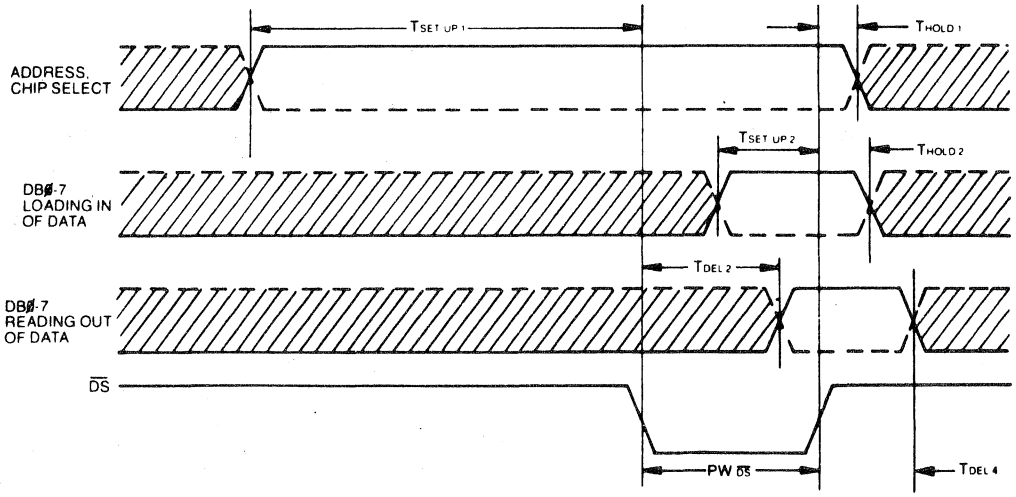
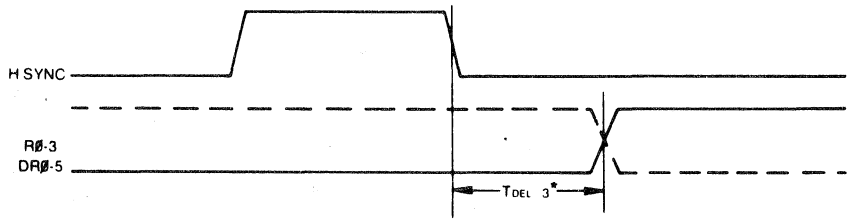
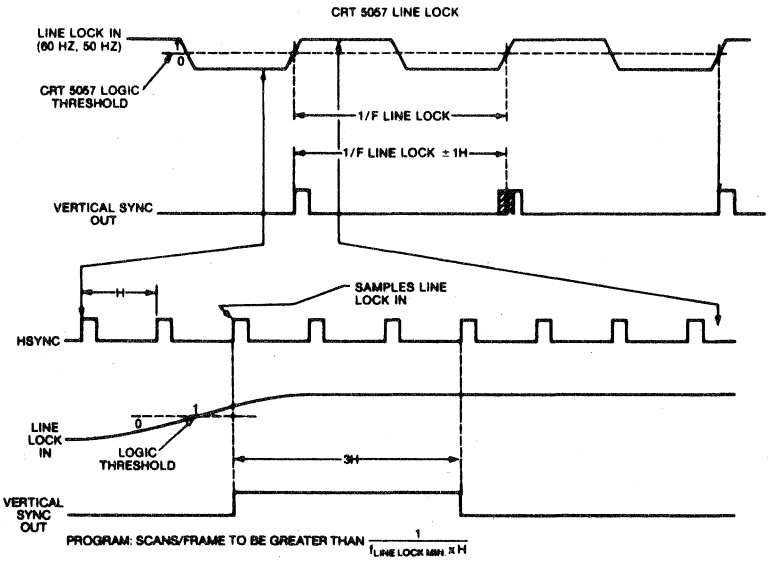


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING



*RØ-3 and DRØ-5 may change prior to the falling edge of H sync



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, unless otherwise noted)

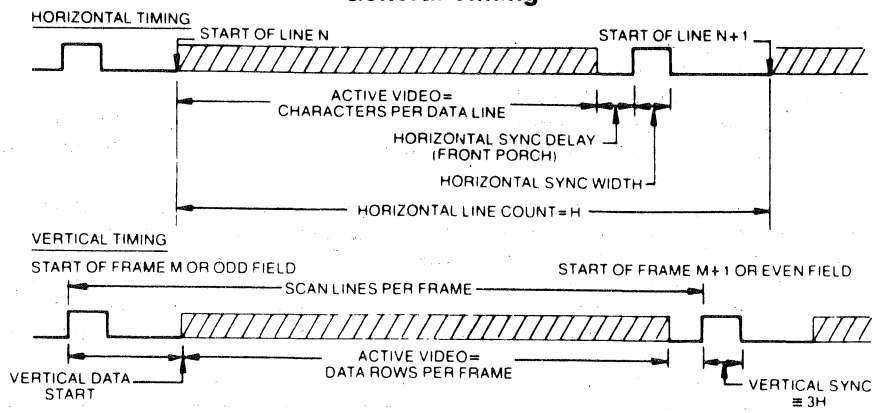
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC} − 1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL} = 3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL} = 1.6ma
High Level—V_{OH} for RØ-3, DBØ-7	2.4				I_{OH} = 80μa
High Level—V_{OH} all others	2.4				I_{OH} = 40μa
INPUT CURRENT					
Low Level, I_{IL} (Address, CS only)			250	μA	V_{IN} = 0.4V
Leakage, I_{IL} (All Inputs except Address, CS)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	$0.4V \leq V_{IN} \leq 5.25V$
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	70	mA	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2		4.0	MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	215			ns	Figure 1
t_r, t_f		10	50	ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$	150ns		10μs		Figure 2
ADDRESS, CHIP SELECT					
Set-up time	125			ns	Figure 2
Hold time	50			ns	Figure 2
DATA BUS—LOADING					
Set-up time	125			ns	Figure 2
Hold time	75			ns	Figure 2
DATA BUS—READING					
T_{DEL2}			125	ns	Figure 2, CL = 50pF
T_{DEL4}	5		60	ns	Figure 2, CL = 50pF
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL1}			125	ns	Figure 1, CL = 20pF
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}	*		500	ns	Figure 3, CL = 20pF

*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

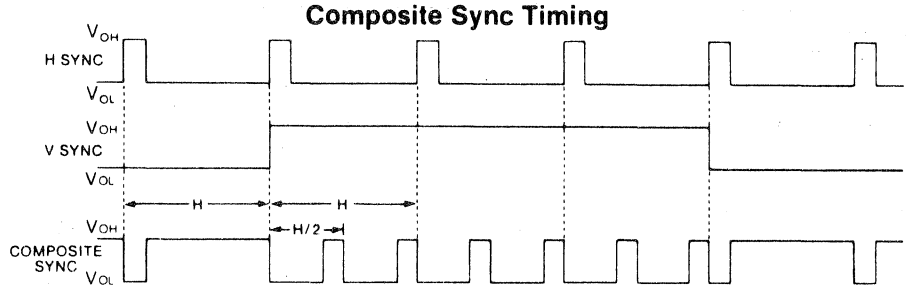
Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

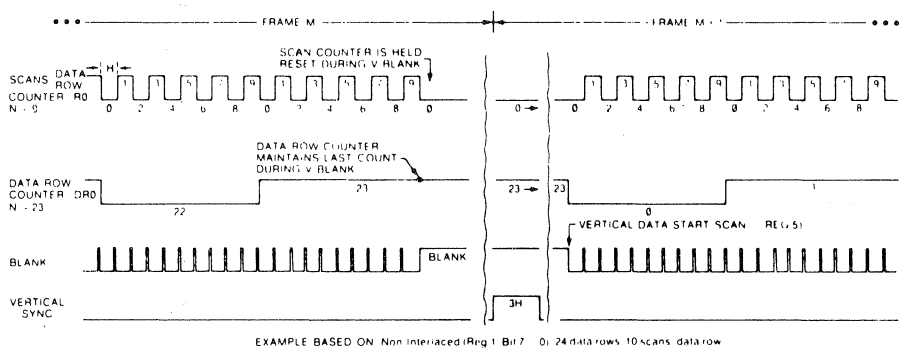
General Timing



Composite Sync Timing



Vertical Sync Timing



EXAMPLE BASED ON Non Interlaced (Reg 1 Bit 7 = 0), 24 data rows, 10 scans data row

Start-up, CRT 5027

When employing microprocessor controlled loading of the CRT 5027's registers, the following sequence of instructions is necessary:

ADDRESS				COMMAND
1	1	1	0	Start Timing Chain
1	0	1	0	Reset
0	0	0	0	Load Register 0
		.		.
		.		.
		.		.
0	1	1	0	Load Register 6
1	1	1	0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to insure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes. This sequence is optional with the CRT 5037 or CRT 5057.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

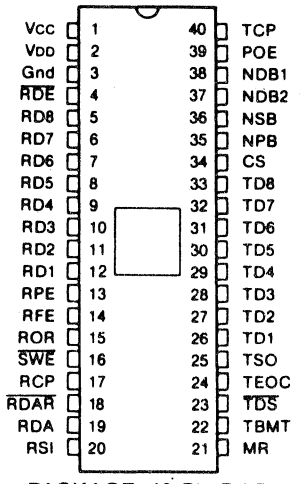
COM2502
COM2017
COM2502/H
COM2017/H

Universal Asynchronous Receiver/Transmitter UART

FEATURES

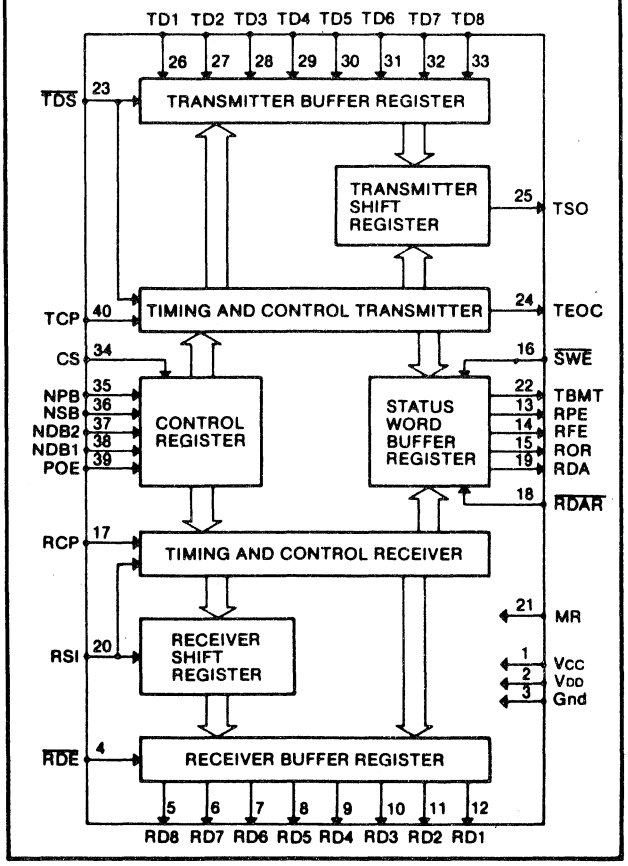
- ☐ Direct TTL Compatibility — no interfacing circuits required
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Start Bit Verification — decreases error rate
- ☐ Fully Programmable — data word length, parity mode, number of stop bits; one, one and one-half, or two
- ☐ High Speed Operation — 40K baud, 200ns strobes
- ☐ Master Reset — Resets all status outputs
- ☐ Tri-State Outputs — bus structure oriented
- ☐ Low Power — minimum power requirements
- ☐ Input Protected — eliminates handling problems
- ☐ Ceramic or Plastic Dip Package — easy board insertion

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolothic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code from the COM2017 or COM2017/H. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

DESCRIPTION OF OPERATION—TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

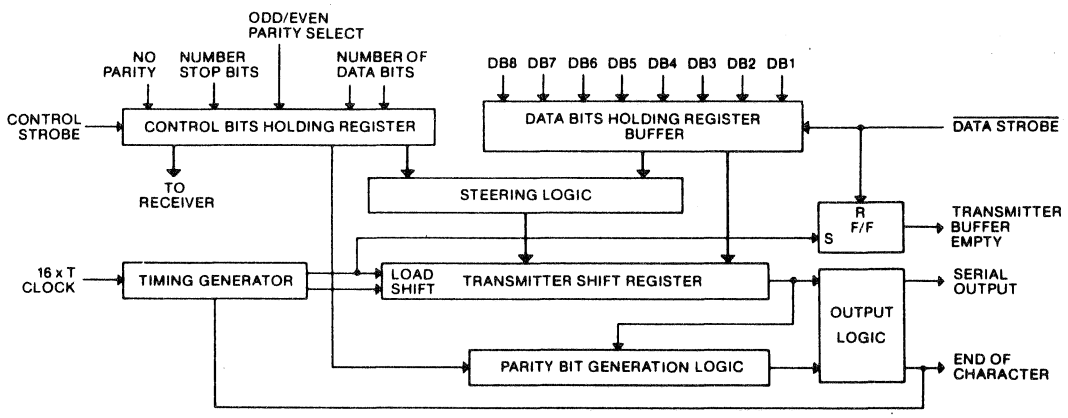
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

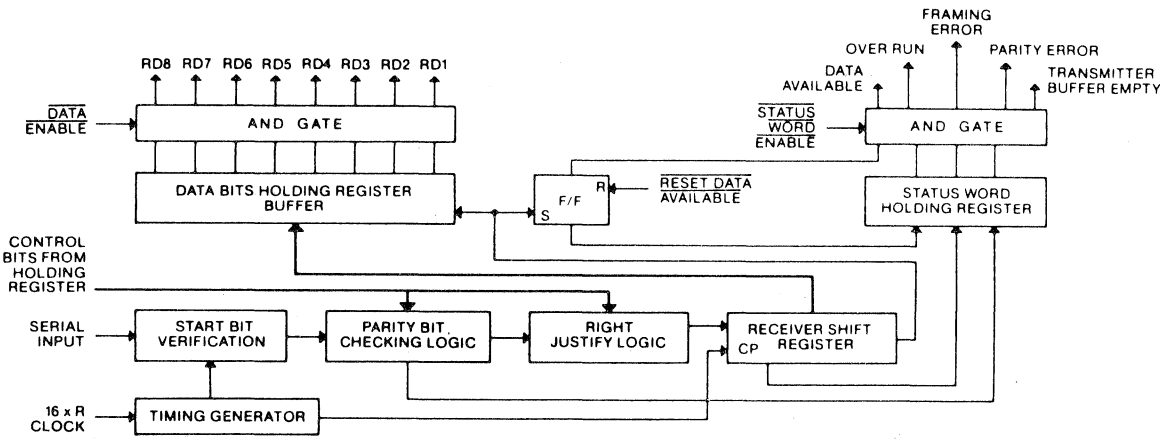
If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	V_{DD}	Power Supply	−12 volt Supply
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

DESCRIPTION OF PIN FUNCTIONS

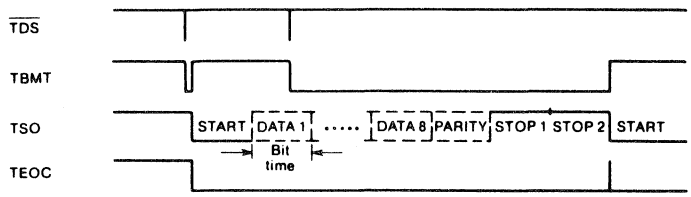
PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

DESCRIPTION OF PIN FUNCTION

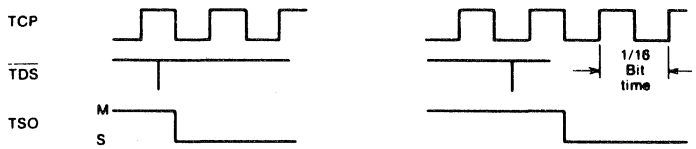
PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 2017 or COM 2017/H.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

SECTION III

TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

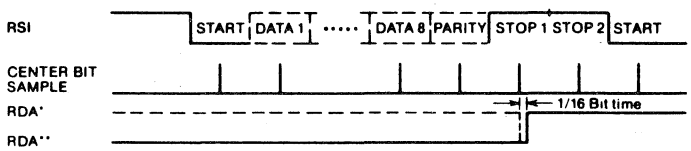


TRANSMITTER START-UP



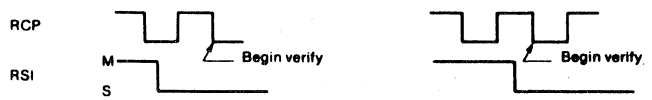
Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of $\overline{TDS}$.

RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS



*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

START BIT DETECT/VERIFY



If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

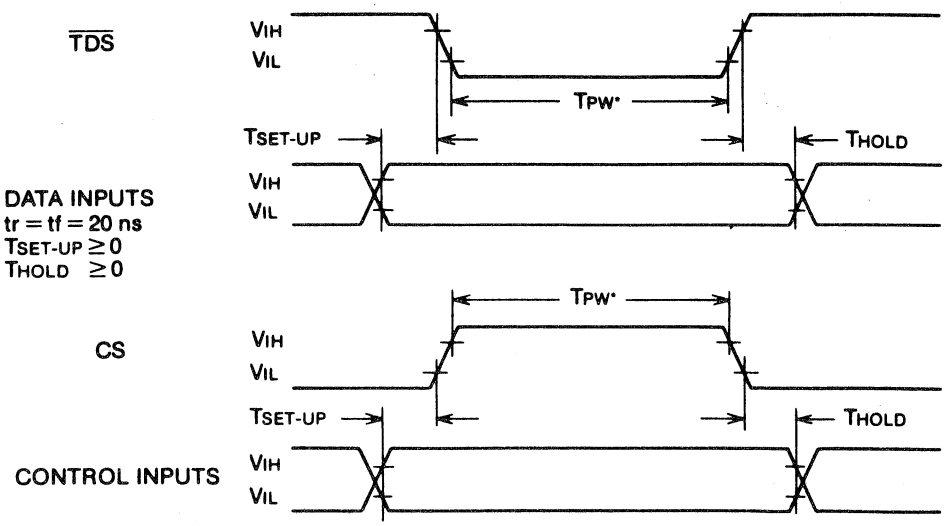
ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 4
OUTPUT CURRENT					
Leakage, I_{LO}			−1	μA	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}, All inputs = V_{CC}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25° C
CLOCK FREQUENCY					
(COM2502, COM2017)	DC		400	KHz	RCP, TCP
(COM2502H, COM2017H)	DC		640	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			350	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			350	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			350	ns	$\overline{RDE}$, $\overline{SWE}$

**Not more than one output should be shorted at a time.

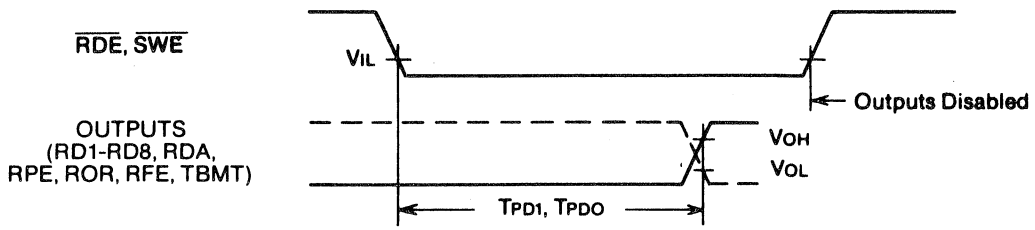
NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.
2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.
3. The tri-state output has 3 states: 1) low impedance to V_{CC} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms. The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.
4. Under steady state conditions no current flows for TTL or MOS interfacing. (COM 2502 or COM 2502/H)

DATA/CONTROL TIMING DIAGRAM

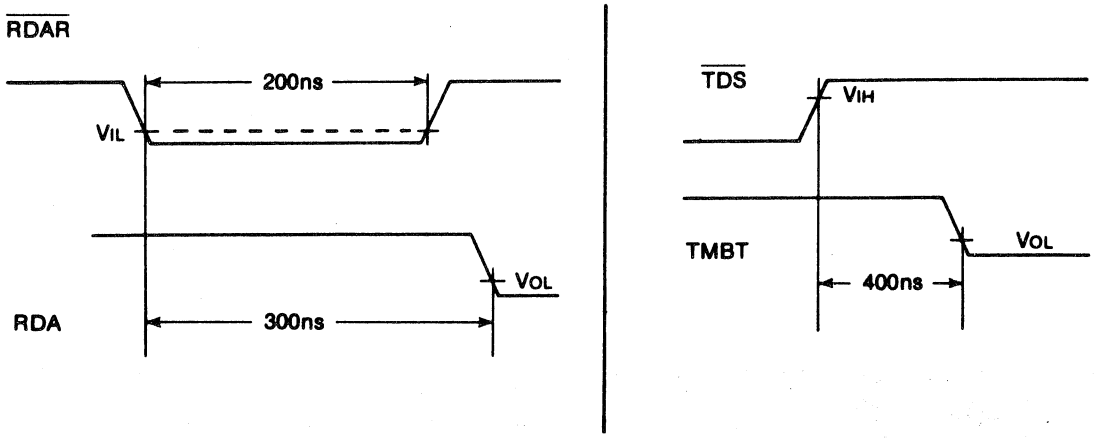


*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

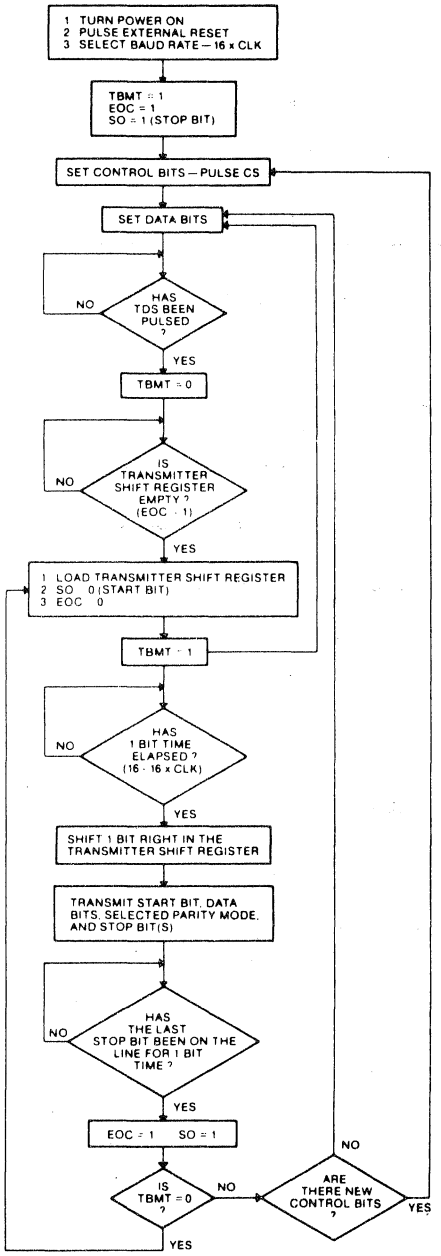
OUTPUT TIMING DIAGRAM



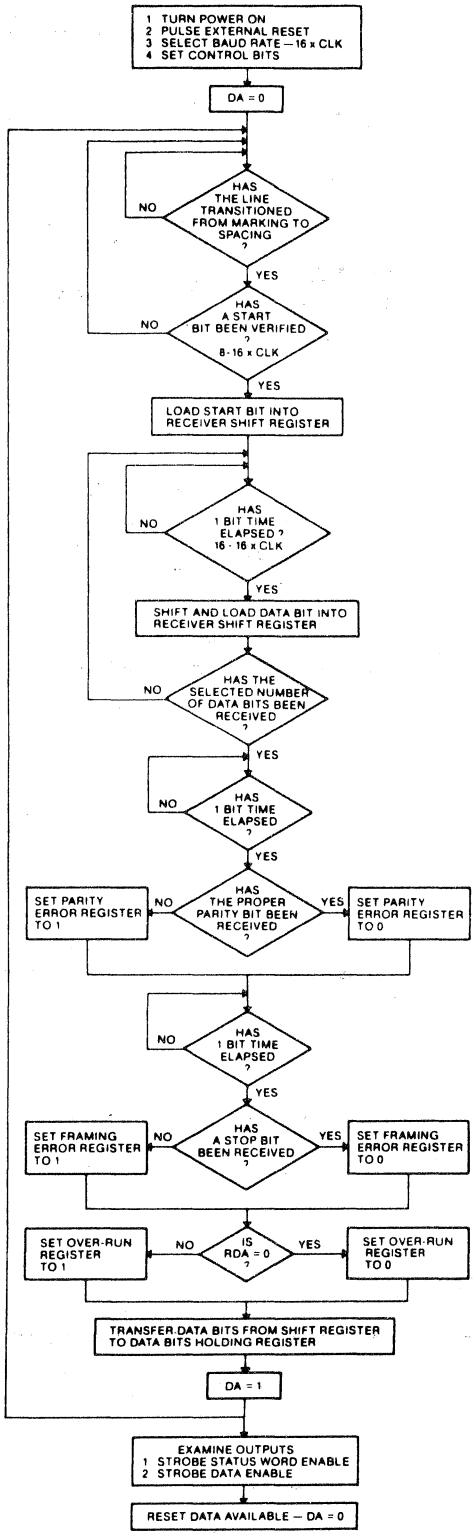
NOTE: Waveform drawings not to scale for clarity.



FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



APPENIX D

KEYBOARD MATRIX

912C/920C

Below is the matrix ("schematic") that is expected on the keyboard attached to connector P1. The character interpretation is actually a firmware decision.

COLUMN		#0	#1	#2	#3	#4	#5	#6	#7
PIN#		8	9	10	11	12	13	14	15
ROW #0	20	N	$ 4	R	. G	LINE FEED	BLOCK CONV	\	
#1	16	X	ESC	TAB	A	I	L	_ -	Z
#2	21	M	% 5	T	H			* 8	
#3	17	C	! 1	Q	S	O	: ;	+ =	CLEAR
#4	22	< ,	^ 6	Y	J	" '	? /	(9	
#5	18	V	@ 2	W	D	P	ENTER	0	DEL
#6	23	> .	& 7	U	K	BERAK	SPACE BAR	BACK SPACE	HOME
#7	19	B	# 3	E	F	] [	RETURN	~ `	} {
#8	26					BACK TAB	SEND PAGE	SEND LINE	PAGE ERASE
#9	25	LINE ERA	LINE DEL	LINE INS	CHAR DEL	CHAR INS	F11	F10	F9
#10	24	F8	F7	F6	F5	F4	F3	F2	F1
#11	7								

ALPHA LOCK	3
SHIFT	4
FUNCT	5
CTRL	6
GROUND	1,2

APPENDIX D

KEYBOARD MATRIX

912B/920B

Below is the matrix ("schematic") that is expected on the keyboard attached to connector P1. The character interpretation is actually a firmware decision.

COLUMN		#Ø	#1	#2	#3	#4	#5	#6	#7
PIN # →		8	9	10	11	12	13	14	15
ROW #Ø	20	N	4	R	G	CR	PAGE	]	→
#1	16	X	TAB	ESC	A	I	L	;	Z
#2	21	M	5	T	H	PRINT	←	8	↑
#3	17	C	1	Q	S	O	:	-	CLEAR
#4	22	,	6	Y	J	RUB	/	9	↓
#5	18	V	2	W	D	P	@	Ø	CLR TAB
#6	23	.	7	U	K	BREAK	SP	^	HOME
#7	19	B	3	E	F	LF	\	[	PROT
#8	26								
#9	25					BRK TAB	SND PAI	SD LIN	PG ERA
#10	24	LIN ERA	LIN DEL	LIN INS	CHR DEL	CHR INS	F11	F10	F9
#11	7	F8	F7	F6	F5	F4	F3	F2	F1

ALPHA	3
SHFT	4
FUNC	5
CTL	6
GROUND	1,2

APPENDIX E

CONNECTOR LISTS

P1 KEYBOARD CONNECTOR (See also Appendix D)

PIN	
1	Ground for Keyboard
2	" " "
3	Input from keyboard ALPHA KEY Bit 6 of 40C to 40F
4	" " " SHFT KEY " 4 " " "
5	" " " FUNC KEY " 2 " " "
6	" " " CTL KEY " 3 " " "
7	Input from keyboard Matrix Bit 5 of 40F
8	Output to keyboard Matrix Column Bit 0 of Port 1
9	Output to keyboard Matrix Column Bit 1 of Port 1
10	Output to keyboard Matrix Column Bit 2 of Port 1
11	Output to keyboard Matrix Column Bit 3 of Port 1
12	Output to keyboard Matrix Column Bit 4 of Port 1
13	Output to keyboard Matrix Column Bit 5 of Port 1
14	Output to keyboard Matrix Column Bit 6 of Port 1
15	Output to keyboard Matrix Column Bit 7 of Port 1
16	Input from keyboard Matrix Bit 1 of 40C
17	Input from keyboard Matrix Bit 1 of 40D
18	Input from keyboard Matrix Bit 1 of 40E
19	Input from keyboard Matrix Bit 1 of 40F
20	Input from keyboard Matrix Bit 0 of 40C
21	Input from keyboard Matrix Bit 0 of 40D
22	Input from keyboard Matrix Bit 0 of 40E
23	Input from keyboard Matrix Bit 0 of 40F
24	Input from keyboard Matrix Bit 5 of 40E

P1	KEYBOARD CONNECTOR (Continued)	
25	Input from keyboard Matrix	Bit 5 of 4ØD
26	Input from keyboard Matrix	Bit 5 of 4ØC

P2	VIDEO CONNECTOR	
PIN 1	+HSYNC	
2	"KEY"	
3	VIDEO SHIELD GROUND	
4	+VIDEO	
5	-VSYNC	
6	+TTL VIDEO (or -COMPSYNC with S2-10, 11 open)	

P3	COMPUTER PORT	
PIN 1		
2	TXD (RS232)	Transmit Data, Output
3	RCVD (RS232)	Receive Data, Input
4	RTS (RS232)	Request to Send, Output
5	CTS (RS232)	Clear to Send, Input
6	DCR2 (RS232)	"Data Carrier Ready, (S5-2, 13), Input
7	GROUND	
8	DCR1 (RS232)	"Data Carrier Ready" (S5-1, 14), Input
9		
10		
11		
12	RXD1 (TTY)	Current Loop Receive Data 1, Input
13	TXD2 (TTY)	Current Loop Transmit Data 2, (Return) Output
14		
15		
16		
17		

P3 COMPUTER PORT (Continued)

PIN		
18		
19		
20	DTR (RS232)	Data Terminal Ready (S5-3, 12 and S5-4,11), Output
21		
22		
23		
24	RXD2 (TTY)	Current Loop Receive Data 2 (Returns) Input
25	TXD1 (TTY)	Current Loop Transmit Data 1, Output

P4 PRINTER PORT

PIN		
1		
2		
3	PRT DATA (RS232)	Transmit Data, Output
4		
5		
6	TERM RDY2 (RS232)	"Terminal Ready" (W12), Output
7	GROUND	
8	TERM RDY1 (RS232)	"Terminal Ready" (W13), Output
9		
10		
11		
12		
13		
14		
15		
16		
17		

P4 PRINTER PORT (Continued)

PIN 18		
19		
20	+PRTRDY (RS232)	Printer Ready, Input
21		
22		
23		
24		
25		

P5 POWER SUPPLY CONNECTOR

PIN 1	-12V
2	"KEY"
3	GROUND
4	+5V
5	+12V

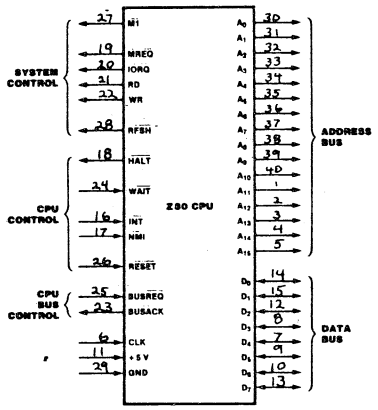
P7

PIN 1	Speaker 8Ω
2	" "

Zilog

Z8400
Z80® CPU Central Processing Unit

Features



Pin Descriptions

A_0-A_{15}. *Address Bus* (output, active High, 3-state). A_0-A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

$\overline{BUSACK}$. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ have entered their high-impedance states. The external circuitry can now control these lines.

$\overline{BUSREQ}$. *Bus Request* (input, active Low). Bus Request has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. $\overline{BUSREQ}$ forces the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ to go to a high-impedance state so that other devices can control these lines. $\overline{BUSREQ}$ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{BUSREQ}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0-D_7. *Data Bus* (input/output, active High, 3-state). D_0-D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

$\overline{HALT}$. *Halt State* (output, active Low). $\overline{HALT}$ indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

$\overline{INT}$. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{IORQ}$. *Input/Output Request* (output, active Low, 3-state). $\overline{IORQ}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{IORQ}$ is also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{M1}$. *Machine Cycle One* (output, active Low). $\overline{M1}$, together with $\overline{MREQ}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{M1}$, together with $\overline{IORQ}$, indicates an interrupt acknowledge cycle.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{NMI}$. *Non-Maskable Interrupt* (input, active Low). $\overline{NMI}$ has a higher priority than $\overline{INT}$. $\overline{NMI}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

$\overline{RD}$. *Memory Read* (output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

$\overline{RFSH}$. *Refresh* (output, active Low). $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

$\overline{WAIT}$. *Wait* (input, active Low). $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{WR}$. *Memory Write* (output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The *Z80 CPU Technical Manual* (03-0029-01) and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchanges, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts
- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r'	r ← r'	•	•	X	X	•	•	01 r r'		1	1	4	r, r' Reg. 000 B
LD r, n	r ← n	•	•	X	X	•	•	00 r 110 — n —		2	2	7	001 C
LD r, (HL)	r ← (HL)	•	•	X	X	•	•	01 r 110		1	2	7	010 D
LD r, (IX+d)	r ← (IX+d)	•	•	X	X	•	•	11 011 101 01 r 101 — d —	DD	3	5	19	011 E 100 H 101 L
LD r, (IY+d)	r ← (IY+d)	•	•	X	X	•	•	11 111 101 01 r 110 — d —	FD	3	5	19	111 A
LD (HL), r	(HL) ← r	•	•	X	X	•	•	01 110 r		1	2	7	
LD (IX+d), r	(IX+d) ← r	•	•	X	X	•	•	11 011 101 01 110 r — d —	DD	3	5	19	
LD (IY+d), r	(IY+d) ← r	•	•	X	X	•	•	11 111 101 01 110 r — d —	FD	3	5	19	
LD (HL), n	(HL) ← n	•	•	X	X	•	•	00 110 110 — n —	36	2	3	10	
LD (IX+d), n	(IX+d) ← n	•	•	X	X	•	•	11 011 101 00 110 110 — d — — n —	DD 36	4	5	19	
LD (IY+d), n	(IY+d) ← n	•	•	X	X	•	•	11 111 101 00 110 110 — d — — n —	FD 36	4	5	19	
LD A, (BC)	A ← (BC)	•	•	X	X	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	X	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	X	•	•	00 111 010 — n — — n —	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	X	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	X	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	X	•	•	00 110 010 — n — — n —	32	3	4	13	
LD A, I	A ← I	↕	↕	X	0	X	IFF	11 101 101 01 010 111	ED 57	2	2	9	
LD A, R	A ← R	↕	↕	X	0	X	IFF	11 101 101 01 011 111	ED 5F	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	•	11 101 101 01 000 111	ED 47	2	2	9
LD R, A	R ← A	•	•	X	•	X	•	•	11 101 101 01 001 111	ED 4F	2	2	9

NOTES: r, r' means any of the registers A, B, C, D, E, H, L.
IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.

For an explanation of flag notation and symbols for mnemonic tables, see Symbolic Notation section following tables.

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	•	•	00 dd0 001 ← n → ← n →	3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LD IX, nn	IX ← nn	•	•	X	•	•	•	11 011 101 DD 00 100 001 21 ← n → ← n →	4	4	14	
LD IY, nn	IY ← nn	•	•	X	•	•	•	11 111 101 FD 00 100 001 21 ← n → ← n →	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	•	•	•	00 101 010 2A ← n → ← n →	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	•	•	•	11 101 101 ED 01 dd1 011 ← n → ← n →	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	•	•	•	11 011 101 DD 00 101 010 2A ← n → ← n →	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	•	•	•	11 111 101 FD 00 101 010 2A ← n → ← n →	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	•	•	•	00 100 010 22 ← n → ← n →	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	•	•	•	11 101 101 ED 01 dd0 011 ← n → ← n →	4	6	20	
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	•	•	X	•	•	•	11 011 101 DD 00 100 010 22 ← n → ← n →	4	6	20	
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	•	•	X	•	•	•	11 111 101 FD 00 100 010 22 ← n → ← n →	4	6	20	
LD SP, HL	SP ← HL	•	•	X	•	•	•	11 111 001 F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	•	•	•	11 011 101 DD 11 111 001 F9	2	2	10	
LD SP, IY	SP ← IY	•	•	X	•	•	•	11 111 101 FD 11 111 001 F9	2	2	10	
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H SP ← SP − 2	•	•	X	•	•	•	11 qq0 101	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H SP ← SP − 2	•	•	X	•	•	•	11 011 101 DD 11 100 101 E5	2	4	15	
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H SP ← SP − 2	•	•	X	•	•	•	11 111 101 FD 11 100 101 E5	2	4	15	
POP qq	qq_H ← (SP + 1) qq_L ← (SP) SP ← SP + 2	•	•	X	•	•	•	11 qq0 001	1	3	10	
POP IX	IX_H ← (SP + 1) IX_L ← (SP) SP ← SP + 2	•	•	X	•	•	•	11 011 101 DD 11 100 001 E1	2	4	14	
POP IY	IY_H ← (SP + 1) IY_L ← (SP) SP ← SP + 2	•	•	X	•	•	•	11 111 101 FD 11 100 001 E1	2	4	14	

NOTES: dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively.
e.g., BC_L = C, AF_H = A.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	•	11 101 011 EB	1	1	4	
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	•	00 001 000 08	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	X	•	X	•	•	•	11 011 001 D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	•	11 100 011 E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 011 E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 011 E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	•	•	X	①	0	X	I	0	•	11 101 101 ED 10 100 000 A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 101 101 ED 10 110 000 B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

NOTE: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.

Exchange, Block Transfer, Block Search Groups (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	•	•	X	0	X	① 1	0	•	11 101 101 ED 10 101 000 A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	① 0	0	•	11 101 101 ED 10 111 000 B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	② I	I	X	I	X	① I	I	•	11 101 101 ED 10 100 001 A1	2	4	16	
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	② I	I	X	I	X	① I	I	•	11 101 101 ED 10 110 001 B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	② I	I	X	I	X	① I	I	•	11 101 101 ED 10 101 001 A9	2	4	16	
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	② I	I	X	I	X	① I	I	•	11 101 101 ED 10 111 001 B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.
② Z flag is 1 if A = (HL), otherwise Z = 0.

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	I	I	X	I	X	V	0	I	10 000 r	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A, n	A ← A + n	I	I	X	I	X	V	0	I	11 000 110 ← n →	2	2	7	
ADD A, (HL)	A ← A + (HL)	I	I	X	I	X	V	0	I	10 000 110	1	2	7	
ADD A, (IX + d)	A ← A + (IX + d)	I	I	X	I	X	V	0	I	11 011 101 DD 10 000 110 ← d →	3	5	19	
ADD A, (IY + d)	A ← A + (IY + d)	I	I	X	I	X	V	0	I	11 111 101 FD 10 000 110 ← d →	3	5	19	
ADC A, s	A ← A + s + CY	I	I	X	I	X	V	0	I	001				s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the 000 in the ADD set above.
SUB s	A ← A − s	I	I	X	I	X	V	1	I	010				
SBC A, s	A ← A − s − CY	I	I	X	I	X	V	1	I	011				
AND s	A ← A ∧ s	I	I	X	1	X	P	0	0	100				
OR s	A ← A ∨ s	I	I	X	0	X	P	0	0	110				
XOR s	A ← A ⊕ s	I	I	X	0	X	P	0	0	101				
CP s	A − s	I	I	X	I	X	V	1	I	111				
INC r	r ← r + 1	I	I	X	I	X	V	0	•	00 r 100	1	1	4	
INC (HL)	(HL) ← (HL) + 1	I	I	X	I	X	V	0	•	00 110 100	1	3	11	
INC (IX + d)	(IX + d) ← (IX + d) + 1	I	I	X	I	X	V	0	•	11 011 101 DD 00 110 100 ← d →	3	6	23	
INC (IY + d)	(IY + d) ← (IY + d) + 1	I	I	X	I	X	V	0	•	11 111 101 FD 00 110 100 ← d →	3	6	23	
DEC m	m ← m − 1	I	I	X	I	X	V	1	•	101				m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	P	•	↕	00 100 111	27	1	1	4	Decimal adjust accumulator.
CPL	A ← $\overline{A}$	•	•	X	X	•	•	00 101 111	2F	1	1	4	Complement accumulator (one's complement).
NEG	A ← 0 − A	↕	↕	X	V	1	↕	11 101 101 01 000 100	ED 44	2	2	8	Negate acc. (two's complement)
CCF	CY ← $\overline{CY}$	•	•	X	X	0	↕	00 111 111	3F	1	1	4	Complement carry flag.
SCF	CY ← 1	•	•	X	X	0	1	00 110 111	37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	X	•	•	00 000 000	00	1	1	4	
HALT	CPU halted	•	•	X	X	•	•	01 110 110	76	1	1	4	
DI *	IFF ← 0	•	•	X	X	•	•	11 110 011	F3	1	1	4	
EI *	IFF ← 1	•	•	X	X	•	•	11 111 011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	X	•	•	11 101 101 01 000 110	ED 46	2	2	8	
IM 1	Set interrupt mode 1	•	•	X	X	•	•	11 101 101 01 010 110	ED 56	2	2	8	
IM 2	Set interrupt mode 2	•	•	X	X	•	•	11 101 101 01 011 110	ED 5E	2	2	8	

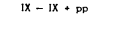
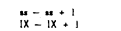
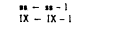
NOTES: IFF indicates the interrupt enable flip flop
CY indicates the carry flip flop
* indicates interrupts are not sampled at the end of EI or DI

16-Bit Arithmetic Group

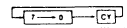
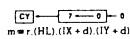
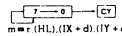
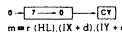
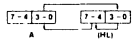
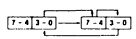
Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	00 ss1 001		1	3	11	ss Reg. 00 BC 01 DE 10 HL 11 SP
ADC HL, ss	HL ← HL + ss + CY	↕	↕	X	X	V	0	11 101 101 01 ss1 010	ED	2	4	15	
SBC HL, ss	HL ← HL − ss − CY	↕	↕	X	X	V	1	11 101 101 01 ss0 010	ED	2	4	15	
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	11 011 101 01 pp1 001	DD	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	11 111 101 00 rr1 001	FD	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INC ss	ss ← ss + 1	•	•	X	•	X	•	00 ss0 011		1	1	6	
INC IX	IX ← IX + 1	•	•	X	•	X	•	11 011 101 00 100 011	DD 23	2	2	10	
INC IY	IY ← IY + 1	•	•	X	•	X	•	11 111 101 00 100 011	FD 23	2	2	10	
DEC ss	ss ← ss − 1	•	•	X	•	X	•	00 ss1 011		1	1	6	
DEC IX	IX ← IX − 1	•	•	X	•	X	•	11 011 101 00 101 011	DD 2B	2	2	10	
DEC IY	IY ← IY − 1	•	•	X	•	X	•	11 111 101 00 101 011	FD 2B	2	2	10	

NOTES: ss is any of the register pairs BC, DE, HL, SP
pp is any of the register pairs BC, DE, IX, SP
rr is any of the register pairs BC, DE, IY, SP

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		•	•	X	0	X	•	0	↕	00 000 111	07	1	1	4	Rotate left circular accumulator.
RLA		•	•	X	0	X	•	0	↕	00 010 111	17	1	1	4	Rotate left accumulator
RRCA		•	•	X	0	X	•	0	↕	00 001 111	0F	1	1	4	Rotate right circular accumulator
RRA		•	•	X	0	X	•	0	↕	00 011 111	1F	1	1	4	Rotate right accumulator
RLC r		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 r	CB	2	2	8	Rotate left circular register r
RLC (HL)		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 110	CB	2	4	15	r Reg 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX + d)	 r (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	11 011 101 11 001 011 ← d → 00 000 110	DD CB	4	6	23	
RLC (IY + d)		↕	↕	X	0	X	P	0	↕	11 111 101 11 001 011 ← d → 00 000 110	FD CB	4	6	23	
RL m	m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	010					Instruction format and states are as shown for RLC's. To form new opcode replace 000 of RLC's with shown code.
RRC m	 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	001					

Rotate and Shift Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RR m	 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	011					
SLA m	 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	100					
SRA m	 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	101					
SRL m	 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	111					
RLD		↕	↕	X	0	X	P	0	•	11 101 101 01 101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL).
RRD		↕	↕	X	0	X	P	0	•	11 101 101 01 100 111	ED 67	2	5	18	The content of the upper half of the accumulator is unaffected

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
BIT b, r	Z ← $\overline{r_b}$	X	↕	X	1	X	X	0	•	11 001 011 01 b r	CB	2	2	8	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A b Bit Tested 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
BIT b, (HL)	Z ← $\overline{(HL)_b}$	X	↕	X	1	X	X	0	•	11 001 011 01 b 110	CB	2	3	12	
BIT b, (IX + d)$_b$	Z ← $\overline{(IX+d)_b}$	X	↕	X	1	X	X	0	•	11 011 101 11 001 011 ← d → 01 b 110	DD CB	4	5	20	
BIT b, (IY + d)$_b$	Z ← $\overline{(IY+d)_b}$	X	↕	X	1	X	X	0	•	11 111 101 11 001 011 ← d → 01 b 110	FD CB	4	5	20	
SET b, r	r_b ← 1	•	•	X	•	X	•	•	•	11 001 011 11 b r	CB	2	2	8	
SET b, (HL)	$(HL)_b$ ← 1	•	•	X	•	X	•	•	•	11 001 011 11 b 110	CB	2	4	15	
SET b, (IX + d)	(IX + d)$_b$ ← 1	•	•	X	•	X	•	•	•	11 011 101 11 001 011 ← d → 11 b 110	DD CB	4	6	23	
SET b, (IY + d)	(IY + d)$_b$ ← 1	•	•	X	•	X	•	•	•	11 111 101 11 001 011 ← d → 11 b 110	FD CB	4	6	23	
RES b, m	m_b ← 0 m = r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	•	•	10					To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

NOTES: The notation m_b indicates bit b (0 to 7) of location m

Jump Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011 ← n → ← n →	C3	3	3	10	
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010 ← n → ← n →		3	3	10	cc Condition 000 NZ non-zero 001 Z zero 010 NC non-carry 011 C carry 100 PO parity odd 101 PE parity even 110 P sign positive 111 M sign negative
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00 011 000 ← e − 2 →	18	2	3	12	
JR C, e	If C = 0, continue If C = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 111 000 ← e − 2 →	38	2 2	2 3	7 12	If condition not met. If condition is met.
JR NC, e	If C = 1, continue If C = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 110 000 ← e − 2 →	30	2 2	2 3	7 12	If condition not met. If condition is met.
JP Z, e	If Z = 0, continue If Z = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 101 000 ← e − 2 →	28	2 2	2 3	7 12	If condition not met. If condition is met.
JR NZ, e	If Z = 1, continue If Z = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 100 000 ← e − 2 →	20	2 2	2 3	7 12	If condition not met. If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101 11 101 001	DD E9	2	2	8	

Jump Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 101 001 E9	2	2	8	
DJNZ, e	B ← B - 1 If B = 0, continue	•	•	X	•	X	•	•	•	00 010 000 10 – e - 2 –	2	2	8	If B = 0.
	If B ≠ 0, PC ← PC + e										2	3	13	If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range < -126, 129 >.
e - 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

Call and Return Group

CALL nn	(SP - 1) ← PC_H (SP - 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 CD – n – – n –	3	5	17	
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	11 cc 100 – n – – n –	3	3	10	If cc is false.
											3	5	17	If cc is true.
RET	PC_L ← (SP) PC_H ← (SP + 1)	•	•	X	•	X	•	•	•	11 001 001 C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	11 cc 000	1	1	5	If cc is false.
											1	3	11	If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 001 101 4D	2	4	14	
RETN[1]	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 101 45	2	4	14	
RST p	(SP - 1) ← PC_H (SP - 2) ← PC_L PC_H ← 0 PC_L ← p	•	•	X	•	X	•	•	•	11 t 111	1	3	11	

cc	Condition
000	NZ non-zero
001	Z zero
010	NC non-carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

NOTE: [1]RETN loads IFF_2 → IFF_1

Input and Output Group

IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11 011 011 DB – n –	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
IN r, (C)	r ← (C) if r = 110 only the flags will be affected	↕	↕	X	↕	X	P	0	•	11 101 101 ED 01 r 000	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INI	(HL) ← (C) B ← B - 1 HL ← HL + 1	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 100 010 A2	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INIR	(HL) ← (C) B ← B - 1 HL ← HL + 1 Repeat until B = 0	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 110 010 B2	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	
IND	(HL) ← (C) B ← B - 1 HL ← HL - 1	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 101 010 AA	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INDR	(HL) ← (C) B ← B - 1 HL ← HL - 1 Repeat until B = 0	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 111 010 BA	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11 010 011 D3 – n –	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 101 101 ED 01 r 001	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTI	(C) ← (HL) B ← B - 1 HL ← HL + 1	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 100 011 A3	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OTIR	(C) ← (HL) B ← B - 1 HL ← HL + 1 Repeat until B = 0	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 110 011 B3	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	
OUTD	(C) ← (HL) B ← B - 1 HL ← HL - 1	X	↕ ①	X	X	X	↕	•		11 101 101 ED 10 101 011 AB	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

NOTE: ① If the result of B - 1 is zero the Z flag is set, otherwise it is reset.

Input and Output Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
OTDR	(C) ← (HL) B ← B - 1 HL ← HL - 1 Repeat until B = 0	X	↕	X	X	X	↕	•	11 101 101 ED 10 111 011	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
									2	4 (If B = 0)	16	

Summary of Flag Operation

Instruction	D_7 S	Z		H		P/V	N	D_0 C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	1	X	P	0	0	Logical operations
OR s; XOR s	↕	↕	X	0	X	P	0	0	
INC s	↕	↕	X	↕	X	V	0	•	8-bit increment.
DEC s	↕	↕	X	↕	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RLA, RLCA, RRA, RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator.
RL m, RLC m, RR m; RRC m, SLA m; SRA m, SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD, RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	↕	Complement carry.
IN r (C)	↕	↕	X	0	X	P	0	•	Input register indirect.
INI, IND, OUTI, OUTD	X	↕	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0 otherwise Z = 0.
INIR, INDR, OTIR, OTDR	X	1	X	X	X	X	1	•	
LDI, LDD	X	X	X	0	X	↕	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR, LDDR	X	X	X	0	X	0	0	•	
CPI, CPIR, CPD, CPDR	X	↕	X	X	X	↕	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I; LD A, R	↕	↕	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

Symbolic Notation

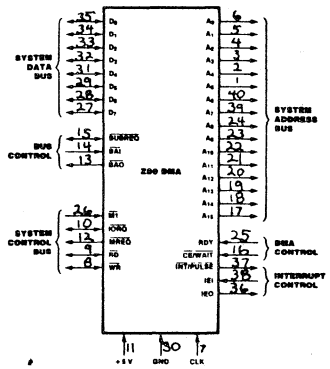
Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >.
nn	16-bit value in range < 0, 65535 >.

Zilog

Z8410
Z80® DMA Direct Memory Access Controller

Features



Pin Description

A_0-A_{15}. *System Address Bus* (output, 3-state). Addresses generated by the DMA are sent to both source and destination ports (main memory or I/O peripherals) on these lines.

$\overline{BAI}$. *Bus Acknowledge In* (input, active Low). Signals that the system buses have been released for DMA control. In multiple-DMA configurations, the $\overline{BAI}$ pin of the highest priority DMA is normally connected to the Bus Acknowledge pin of the CPU. Lower-priority DMAs have their $\overline{BAI}$ connected to the $\overline{BAO}$ of a higher-priority DMA.

$\overline{BAO}$. *Bus Acknowledge Out* (output, active Low). In a multiple-DMA configuration, this pin signals that no other higher-priority DMA has requested the system buses. $\overline{BAI}$ and $\overline{BAO}$ form a daisy chain for multiple-DMA priority resolution over bus control.

$\overline{BUSREQ}$. *Bus Request* (bidirectional, active Low, open drain). As an output, it sends requests for control of the system address bus, data bus and control bus to the CPU. As an input, when multiple DMAs are strung together in a priority daisy chain via $\overline{BAI}$ and $\overline{BAO}$, it senses when another DMA has requested the buses and causes this DMA to refrain from bus requesting until the other DMA is finished. Because it is a bidirectional pin, there cannot be any buffers between this DMA and any other DMA. It can, however, have a buffer between it and the CPU because it is unidirectional into the CPU. A pull-up resistor is connected to this pin.

$\overline{CE}$/$\overline{WAIT}$. *Chip Enable and Wait* (input, active Low). Normally this functions only as a $\overline{CE}$ line, but it can also be programmed to serve a $\overline{WAIT}$ function. As a $\overline{CE}$ line from the CPU, it becomes active when $\overline{WR}$ and $\overline{IORQ}$ are active and the I/O port address on the system address bus is the DMA's address, thereby allowing a transfer of control or command bytes from the CPU to the DMA. As a $\overline{WAIT}$ line from memory or I/O devices, after the DMA has received a bus-request acknowledge from the CPU, it causes wait states to be inserted in the DMA's operation cycles thereby slowing the DMA to a speed that matches the memory or I/O device.

CLK. *System Clock* (input). Standard Z-80 single-phase clock at 2.5 MHz (Z-80 DMA) or 4.0 MHz (Z-80A DMA). For slower system clocks, a TTL gate with a pullup resistor may be adequate to meet the timing and voltage level specification. For higher-speed systems, use a clock driver with an active pullup to meet the V_{IH} specification and risetime requirements. In all cases there should be a resistive pullup to the power supply of 10K ohms (max) to ensure proper power when the DMA is reset.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Commands from the CPU, DMA status, and data from memory or I/O peripherals are transferred on these lines.

IEI. *Interrupt Enable In* (input, active High). This is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this DMA. Thus, this signal blocks lower-priority devices from interrupting while a higher-priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$/PULSE. *Interrupt Request* (output, active Low, open drain). This requests a CPU interrupt. The CPU acknowledges the interrupt by pulling its $\overline{IORQ}$ output Low during an $\overline{M1}$ cycle. It is typically connected to the $\overline{INT}$ pin of the CPU with a pullup resistor and tied to all other $\overline{INT}$ pins in the system. This pin can also be used to generate periodic pulses to an external device. It can be used this way only when the DMA is bus master (i.e., the CPU's $\overline{BUSREQ}$ and $\overline{BUSACK}$ lines are both Low and the CPU cannot see interrupts).

$\overline{IORQ}$. *Input/Output Request* (bidirectional, active Low, 3-state). As an input, this indicates that the lower half of the address bus holds a valid I/O port address for transfer of control or status bytes from or to the CPU, respectively; this DMA is the addressed port if its $\overline{CE}$ pin and its $\overline{WR}$ or $\overline{RD}$ pins are simultaneously active. As an output, after the DMA has taken control of the system buses, it indicates that the 8-bit or 16-bit address bus holds a valid port address for another I/O device involved in a DMA transfer of data. When $\overline{IORQ}$ and $\overline{M1}$ are both active simultaneously, an interrupt acknowledge is indicated.

$\overline{M1}$. *Machine Cycle One* (input, active Low). Indicates that the current CPU machine cycle is an instruction fetch. It is used by the DMA to decode the return-from-interrupt instruction (RETI) (ED-4D) sent by the CPU. During two-byte instruction fetches, $\overline{M1}$ is active as each opcode byte is fetched. An interrupt acknowledge is indicated when both $\overline{M1}$ and $\overline{IORQ}$ are active.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). This indicates that the address bus holds a valid address for a memory read or write operation. After the DMA has taken control of the system buses, it indicates a DMA transfer request from or to memory.

$\overline{RD}$. *Read* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to read status bytes from the DMA's read registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled read from a memory or I/O port address.

RDY. *Ready* (input, programmable active Low or High). This is monitored by the DMA to determine when a peripheral device associated with a DMA port is ready for a read or write operation. Depending on the mode of DMA operation (Byte, Burst or Continuous), the RDY line indirectly controls DMA activity by causing the $\overline{BUSREQ}$ line to go Low or High.

$\overline{WR}$. *Write* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to write control or command bytes to the DMA write registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled write to a memory or I/O port address.

Programming

The Z-80 DMA has two programmable fundamental states: (1) an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and (2) a disabled state, in which it can initiate neither bus requests nor data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state. Program commands can be written to it by the CPU in either state, but this automatically puts the DMA in the disabled state, which is maintained until an enable command is issued by the CPU. The CPU must program the DMA in advance of any data search or transfer by addressing it as an I/O port and sending a sequence of control bytes using an Output instruction (such as OTIR for the Z-80 CPU).

Writing. Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (1's) to one or more of that base register's associated registers.

This is illustrated in Figure 8b. In this figure, the sequence in which associated registers within a group can be written to is shown by the vertical position of the associated registers. For example, if a byte written to the DMA contains the bits that identify WR0 (bits D0, D1 and D7), and also contains 1's in the bit positions that point to the associated "Port A Starting Address (low byte)" and "Port A Starting Address (high byte)," then the next two bytes written to the DMA will be stored in these two registers, in that order.

Reading. The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction (such as INIR for the Z-80 CPU). The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6. However, the register read in this sequence is determined by programming the Read Mask in WR6. The sequence of reading is initialized by writing an Initiate Read Sequence or Set Read Status command to WR6. After a Reset DMA, the sequence must be initialized with the Initiate Read Sequence command or a Read Status command. The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or Read Status command.

Fixed-Address Programming. A special circumstance arises when programming a destination port to have a fixed address. The load command in WR6 only loads a fixed address to a port selected as the source, not to a port selected as the destination. Therefore, a fixed destination address must be loaded by temporarily declaring it a fixed-source address and subsequently declaring the true source as such, thereby implicitly making the other a destination.

The following example illustrates the steps in this procedure, assuming that transfers are to occur from a variable-address source (Port A) to a fixed-address destination (Port B):

1. Temporarily declare Port B as source in WR0.
2. Load Port B address in WR6.
3. Declare Port A as source in WR0.

Programming (Continued)

4. Load Port A address in WR6.
5. Enable DMA in WR6.

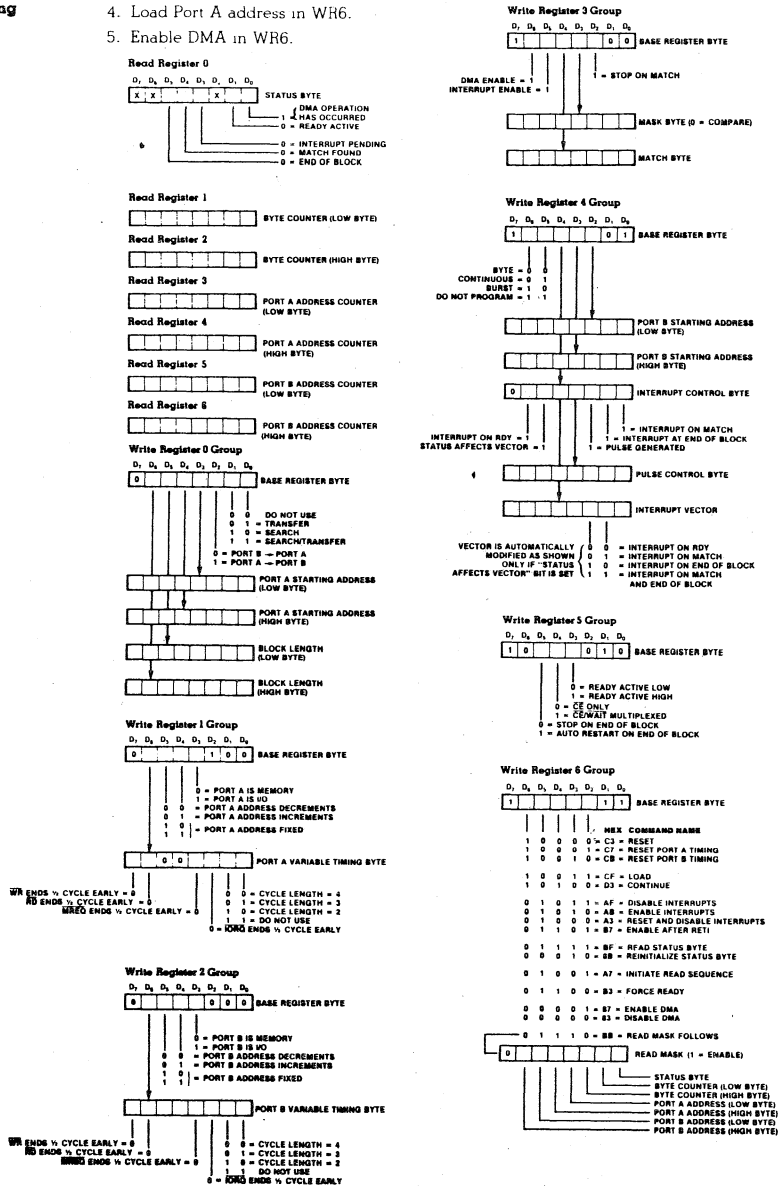
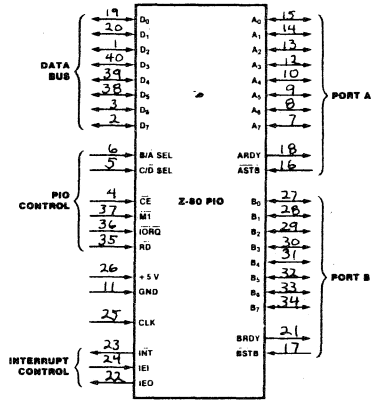


Figure 8b. Write Registers

Zilog

Z8420
Z80® PIO Parallel Input/Output Controller

Features



Pin Description

A_0-A_7. *Port A Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port A of the PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

ARDY. *Register A Ready* (output, active High). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

Input Mode. This signal is active when the Port A input register is empty and ready to accept data from the peripheral device.

Bidirectional Mode. This signal is active when data is available in the Port A output register for transfer to the peripheral device. In this mode, data is not placed on the Port A data bus, unless $\overline{ASTB}$ is active.

Control Mode. This signal is disabled and forced to a Low state.

$\overline{ASTB}$. *Port A Strobe Pulse From Peripheral Device* (input, active Low). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

Input Mode. The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

Bidirectional Mode. When this signal is active, data from the Port A output register is gated onto the Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

Control Mode. The strobe is inhibited internally.

B_0-B_7. *Port B Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port B and a peripheral device. The Port B data bus can supply 1.5 mA at 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

B/$\overline{A}$. *Port B Or A Select* (input, High = B). This pin defines which port is accessed during a data transfer between the CPU and the PIO. A Low on this pin selects Port A; a High selects Port B. Often address bit A_0 from the CPU is used for this selection function.

BRDY. *Register B Ready* (output, active High). This signal is similar to ARDY, except that in the Port A bidirectional mode this signal is High when the Port A input register is empty and ready to accept data from the peripheral device.

$\overline{BSTB}$. *Port B Strobe Pulse From Peripheral Device* (input, active Low). This signal is similar to $\overline{ASTB}$, except that in the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

C/$\overline{D}$. *Control Or Data Select* (input, High = C). This pin defines the type of data transfer to be performed between the CPU and the PIO. A High on this pin during a CPU write to the PIO causes the Z-80 data bus to be interpreted as a *command* for the port selected by the B/$\overline{A}$ Select line. A Low on this pin means that the Z-80 data bus is being used to transfer data between the CPU and the PIO. Often address bit A_1 from the CPU is used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally decoded from four I/O port numbers for Ports A and B, data, and control.

CLK. *System Clock* (input). The Z-80 PIO uses the standard single-phase Z-80 system clock.

D_0-D_7. *Z-80 CPU Data Bus* (bidirectional, 3-state). This bus is used to transfer all data and commands between the Z-80 CPU and the Z-80 PIO. D_0 is the least significant bit.

IEI. *Interrupt Enable In* (input, active High). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A High level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

Pin Description (Continued)

IEO. *Interrupt Enable Out* (output, active High). The IEO signal is the other signal required to form a daisy chain priority scheme. It is High only if IEI is High and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When $\overline{INT}$ is active the Z-80 PIO is requesting an interrupt from the Z-80 CPU.

$\overline{IORQ}$. *Input/Output Request* (input from Z-80 CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the Z-80 CPU and the Z-80 PIO. When $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are active, the port addressed by B/$\overline{A}$ transfers data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not, the port addressed by B/$\overline{A}$ is written into from the CPU with either data or control information, as specified by C/$\overline{D}$. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt; the interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from CPU, active Low). This signal is used as a sync pulse to control several internal PIO operations. When both the $\overline{M1}$ and $\overline{RD}$ signals are active, the Z-80 CPU is fetching an instruction from memory. Conversely, when both $\overline{M1}$ and $\overline{IORQ}$ are active, the CPU is acknowledging an interrupt. In addition, $\overline{M1}$ has two other functions within the Z-80 PIO: it synchronizes the PIO interrupt logic; when $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO is reset.

$\overline{RD}$. *Read Cycle Status* (input from Z-80 CPU, active Low). If $\overline{RD}$ is active, or an I/O operation is in progress, $\overline{RD}$ is used with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$ to transfer data from the Z-80 PIO to the Z-80 CPU.

Programming

Mode 0, 1, or 2. *(Byte Input, Output, or Bidirectional).* Programming a port for Mode 0, 1, or 2 requires two words per port. These words are:

A Mode Control Word. Selects the port operating mode (Figure 6). This word may be written any time.

An Interrupt Vector. The Z-80 PIO is designed for use with the Z-80 CPU in interrupt Mode 2 (Figure 7). When interrupts are enabled, the PIO must provide an interrupt vector.

Mode 3. *(Bit Input/Output).* Programming a port for Mode 3 operation requires a control word, a vector (if interrupts are enabled), and three additional words, described as follows:

I/O Register Control. When Mode 3 is selected, the mode control word must be followed by another control word that sets the I/O control register, which in turn defines which port lines are inputs and which are outputs (Figure 8).

Interrupt Control Word. In Mode 3, handshake is not used. Interrupts are generated as a logic function of the input signal levels. The interrupt control word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), and OR (if any one of the input bits changes to the active level, an interrupt is triggered). Bit D_6 sets the logic function, as shown in Figure 9. The active level of the input bits can be set either High or Low. The active level is controlled by Bit D_5.

Mask Control Word. This word sets the mask control register, allowing any unused bits to be masked off. If any bits are to be masked, then D_4 must be set. When D_4 is set, the next word written to the port must be a mask control word (Figure 10).

Interrupt Disable. There is one other control word which can be used to enable or disable a port interrupt. It can be used without changing the rest of the interrupt control word (Figure 11).

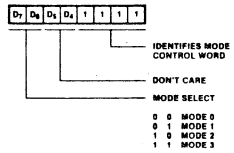


Figure 6. Mode Control Word

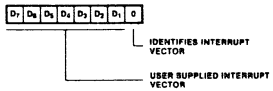


Figure 7. Interrupt Vector Word

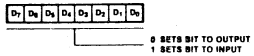


Figure 8. I/O Register Control Word

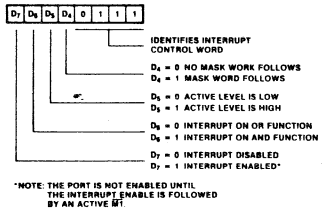


Figure 9. Interrupt Control Word

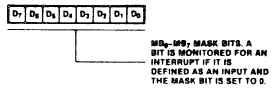


Figure 10. Mask Control Word

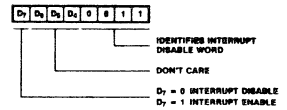
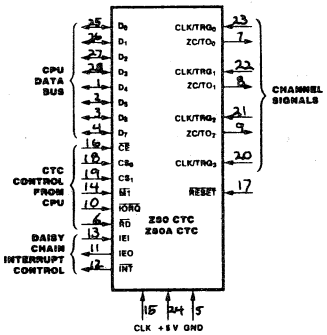


Figure 11. Interrupt Disable Word

Zilog

Z8430
Z80® CTC Counter/ Timer Circuit

Features



Pin Description

$\overline{CE}$. *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the down-counter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

CLK. *System Clock* (input). Standard single-phase Z-80 system clock.

CLK/TRG_0-CLK/TRG_3. *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z-80 CTC channels. In counter mode, every active edge on this pin decrements the down-counter. In timer mode, an active edge starts the timer.

CS_0-CS_1. *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A_0 and A_1).

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z-80 CPU and the Z-80 CTC.

$\overline{IEI}$. *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z-80 CPU.

IEO. *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z-80 CPU is not servicing an interrupt from any Z-80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). Low when any Z-80 CTC channel that has been programmed to enable interrupts has a zero-count condition in its down-counter.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). Used with $\overline{CE}$ and $\overline{RD}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC. During a write cycle, $\overline{IORQ}$ and $\overline{CE}$ are active and $\overline{RD}$ inactive. The Z-80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active $\overline{RD}$ signal. In a read cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ are active; the contents of the down-counter are read by the Z-80 CPU. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z-80 data bus.

$\overline{M1}$. *Machine Cycle One* (input from CPU, active Low). When $\overline{M1}$ and $\overline{IORQ}$ are active, the Z-80 CPU is acknowledging an interrupt. The Z-80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ($\overline{INT}$).

$\overline{RD}$. *Read Cycle Status* (input, active Low). Used in conjunction with $\overline{IORQ}$ and $\overline{CE}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC.

$\overline{RESET}$. *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the Interrupt outputs go inactive; IEO reflects IEI; D_0–D_7 go to the high-impedance state.

ZC/TO_0-ZC/TO_2. *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z-80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the down-counter decrements to zero.

Programming Each Z-80 CTC channel must be programmed prior to operation. Programming consists of writing two words to the I/O port that corresponds to the desired channel. The first word is a control word that selects the operating mode and other parameters; the second word is a time constant, which is a binary data word with a value from 1 to 256. A time constant word must be preceded by a channel control word.

After initialization, channels may be reprogrammed at any time. If updated control and time constant words are written to a channel during the count operation, the count continues to zero before the new time constant is loaded into the counter.

If the interrupt on any Z-80 CTC channel is enabled, the programming procedure should also include an interrupt vector. Only one vector is required for all four channels, because the interrupt logic automatically modifies the vector for the channel requesting service.

A control word is identified by a 1 in bit 0. A 0 in bit 2 indicates a time constant word is to follow. Interrupt vectors are always addressed to Channel 0, and identified by a 0 in bit 0.

Addressing. During programming, channels are addressed with the channel select pins CS_1 and CS_2. A 2-bit binary code selects the appropriate channel as shown in the following table.

Channel	CS_1	CS_0
0	0	0
1	0	1
2	1	0
3	1	1

Reset. The CTC has both hardware and software resets. The hardware reset terminates all down-counts and disables all CTC interrupts by resetting the interrupt bits in the control registers. In addition, the ZC/TO and Interrupt outputs go inactive, IEO reflects IEI, and D_0-D_7 go to the high-impedance state. All channels must be completely reprogrammed after a hardware reset.

The software reset is controlled by bit 1 in the channel control word. When a channel receives a software reset, it stops counting. When a software reset is used, the other bits in the control word also change the contents of the channel control register. After a software reset a new time constant word must be written to the same channel.

If the channel control word has both bits D_1 and D_2 set to 1, the addressed channel stops operating, pending a new time constant word. The channel is ready to resume after the new constant is programmed. In timer mode, if D_3 = 0, operation is triggered automatically when the time constant word is loaded.

Channel Control Word Programming. The channel control word is shown in Figure 5. It sets the modes and parameters described below.

Interrupt Enable. D_7 enables the interrupt, so that an interrupt output ($\overline{INT}$) is generated at zero count. Interrupts may be programmed in either mode and may be enabled or disabled at any time.

Operating Mode. D_6 selects either timer or counter mode.

Prescaler Factor. (Timer Mode Only). D_5 selects factor—either 16 or 256.

Trigger Slope. D_4 selects the active edge or slope of the CLK/TRG input pulses. Note that reprogramming the CLK/TRG slope during operation is equivalent to issuing an active edge. If the trigger slope is changed by a control word update while a channel is pending operation in timer mode, the result is the same as a CLK/TRG pulse and the timer starts. Similarly, if the channel is in counter mode, the counter decrements.

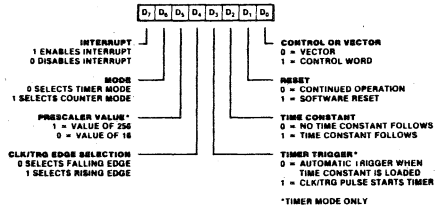


Figure 5. Channel Control Word

Programming (Continued) **Trigger Mode (Timer Mode Only).** D_3 selects the trigger mode for timer operation. When D_3 is reset to 0, the timer is triggered automatically. The time constant word is programmed during an I/O write operation, which takes one machine cycle. At the end of the write operation there is a setup delay of one clock period. The timer starts automatically (decrements) on the rising edge of the second clock pulse (T_2) of the machine cycle following the write operation. Once started, the timer runs continuously. At zero count the timer reloads automatically and continues counting without interruption or delay, until stopped by a reset.

When D_3 is set to 1, the timer is triggered externally through the CLK/TRG input. The time constant word is programmed during an I/O write operation, which takes one machine cycle. The timer is ready for operation on the rising edge of the second clock pulse (T_2) of the following machine cycle. Note that the first timer decrement follows the active edge of the CLK/TRG pulse by a delay time of one clock cycle if a minimum setup time to the rising edge of clock is met. If this minimum is not met, the delay is extended by another clock period. Consequently, for immediate triggering, the CLK/TRG input must precede T_2 by one clock cycle plus its minimum setup time. If the minimum time is not met, the timer will start on the third clock cycle (T_3).

Once started the timer operates continuously, without interruption or delay, until stopped by a reset.

Time Constant to Follow. A 1 in D_2 indicates that the next word addressed to the selected channel is a time constant data word for the time constant register. The time constant word may be written at any time.

A 0 in D_2 indicates no time constant word is to follow. This is ordinarily used when the channel is already in operation and the new channel control word is an update. A channel will not operate without a time constant value. The only way to write a time constant value is to write a control word with D_2 set.

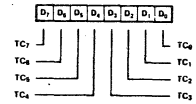


Figure 6. Time Constant Word

Software Reset. Setting D_1 to 1 causes a software reset, which is described in the Reset section.

Control Word. Setting D_0 to 1 identifies the word as a control word.

Time Constant Programming. Before a channel can start counting it must receive a time constant word from the CPU. During programming or reprogramming, a channel control word in which bit 2 is set must precede the time constant word to indicate that the next word is a time constant. The time constant word can be any value from 1 to 256 (Figure 6). Note that 00_{16} is interpreted as 256.

In timer mode, the time interval is controlled by three factors:

- The system clock period (ϕ)
- The prescaler factor (P), which multiplies the interval by either 16 or 256
- The time constant (T), which is programmed into the time constant register

Consequently, the time interval is the product of $\phi \times P \times T$. The minimum timer resolution is $16 \times \phi$ (4 μs with a 4 MHz clock). The maximum timer interval is $256 \times \phi \times 256$ (16.4 ms with a 4 MHz clock). For longer intervals timers may be cascaded.

Interrupt Vector Programming. If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D_0 of the vector word is always zero, to distinguish the vector from a channel control word. D_1 and D_2 are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector (Figure 7). Channel 0 has the highest priority.

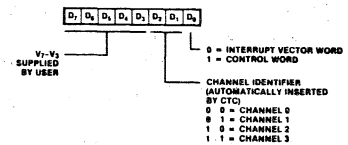
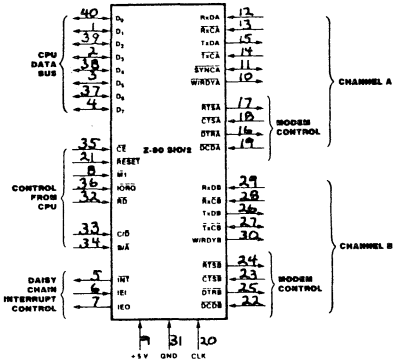


Figure 7. Interrupt Vector Word

Zilog

Z8440
Z80® SIO Serial Input/Output Controller

Features



Pin Description

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

B/$\overline{A}$. *Channel A Or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. *Control Or Data Select* (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The SIO uses the standard Z-80 System Clock to synchronize internal signals. This is a single-phase clock.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z-80 SIO. D_0 is the least significant bit.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into Z-80 SIO. They can also be programmed as general-purpose outputs.

In the Z-80 SIO/1 bonding option, $\overline{DTRB}$ is omitted.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with

Pin Description (Continued)

B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. If $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from Z-80 CPU, active Low). When $\overline{M1}$ is active and $\overline{RD}$ is also active, the Z-80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z-80 CPU.

$\overline{RxCA}$, $\overline{RxCB}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of $\overline{RxC}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the Z-80 SIO/0 bonding option, $\overline{RxCB}$ is bonded together with $\overline{TxCB}$.

$\overline{RD}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. *Receive Data* (inputs, active High). Serial data at TTL levels.

$\overline{RESET}$. *Reset* (input, active Low). A Low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

$\overline{RTSA}$, $\overline{RTSB}$. *Request To Send* (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{RTS}$ output goes Low. When the RTS bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{SYNCA}$, $\overline{SYNCB}$. *Synchronization* (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z-80 SIO/2 bonding option, $\overline{SYNCB}$ is omitted.

$\overline{TxCA}$, $\overline{TxCB}$. *Transmitter Clocks* (inputs). In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation.

In the Z-80 SIO/0 bonding option, $\overline{TxCB}$ is bonded together with $\overline{RxCB}$.

TxDA, TxDB. *Transmit Data* (outputs, active High). Serial data at TTL levels. TxD changes from the falling edge of $\overline{TxC}$.

$\overline{W/RDYA}$, $\overline{W/RDYB}$. *Wait/Ready A, Wait/Ready B* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally-modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must not be combined with the pointing to any register.

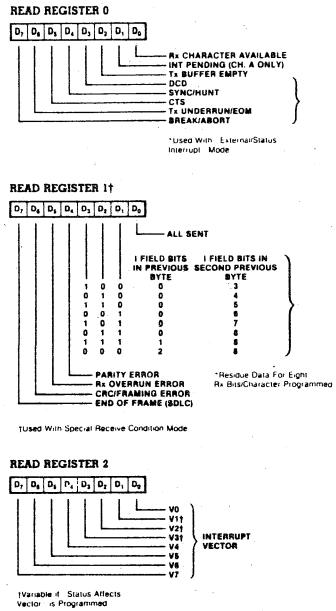


Figure 13. Read Register Bit Functions

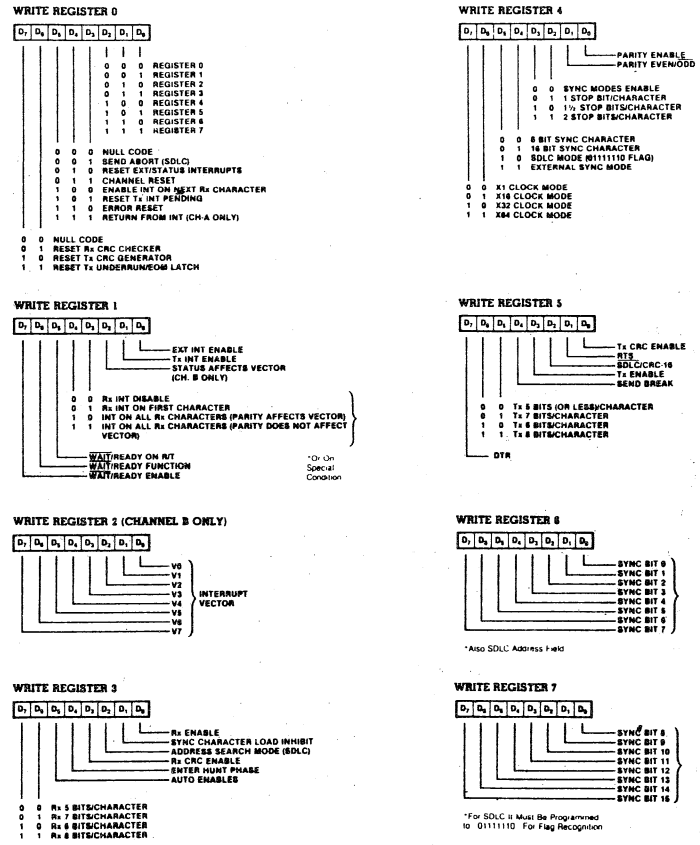


Figure 14. Write Register Bit Functions

SINGLE CHIP 8-BIT MICROCOMPUTER

N-CHANNEL SILICON GATE MOS

TMP8049P/TMP8049P-6
TMP8039P/TMP8039P-6

GENERAL DESCRIPTION

TMP8049P/TMP8039P is an 8-bit single chip microcomputer fabricated with N-channel Silicon Gate Mos process.

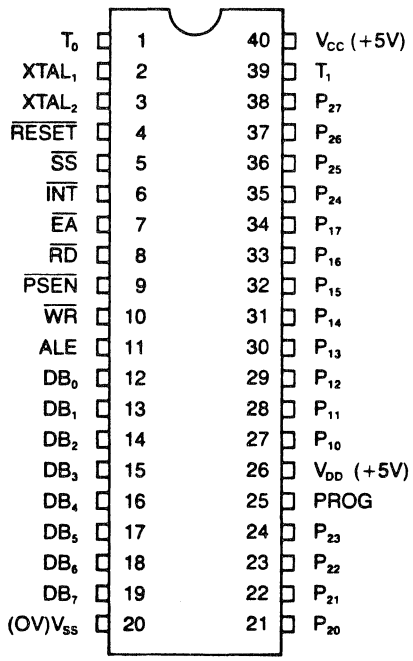
TMP8048P contains all the basic factors of computer, such as CPU, data memory (RAM), program memory (mask ROM), I/O ports and timer/counter.

TMP8039P is the equivalent processor of TMP8049P without internal program memory. TMP8049P-6/ TMP8039P-6 is a lower speed (6MHz) version of 11MHz TMP8049P/TMP8039P.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in Single Package
- Single 5V Supply
- 1.36μsec Cycle All Instructions 1 or 2 Cycle
- Easy Expandable Memory and I/O
- Pin Compatible with TMP8048P
- Software Compatible with TMP 8048P
- 2k x 8 ROM, 128 x 8 RAM, 27 I/O Lines
- Interval Timer/Event Counter
- Compatible with Industry Standard 8049

PIN CONNECTIONS (TOP VIEW)



PIN NAMES & PIN DESCRIPTION

V_{SS} (Power Supply)	Circuit GND potential
V_{DD} (Power Supply)	+5V during operation Low power standby pin.
V_{CC} (Power Supply)	+5V during operation
PROG (Output)	Control signal for I/O expander.
$P_{10} \sim P_{17}$ (Input/Output)	8-bit quasi-bidirectional port (Internal Pullup ≈ 50kΩ)
$P_{20} \sim P_{27}$ (Input/Output)	8-bit quasi-directional port (Internal Pullup ≈ 50kΩ)
	$P_{20} \sim P_{23}$ contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus.
$DB_0 \sim DB_7$ (Input/Output, 3-State)	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched.
	Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction under control of ALE, RD, and WR.
T_0 (Input/Output)	Input pin testable using the conditional transfer instructions JTO and JNTO. T_0 can be designated as a clock output/using ENTO CLK instruction. T_0 is also used during programming
T_1 (Input)	Input pin testable using the JT_1, and JNT_1 instructions. Can be designated the event counter input using the STRT CNT instruction.
$\overline{INT}$ (Input)	External interrupt input. This is level interrupt signal, therefore INT has to be kept at low level until the interrupt request is accepted. INT also functions as a test flag for the conditional jump.
$\overline{RD}$ (Output)	Strobe signal for read when external area is accessed, (active low).
$\overline{WR}$ (Output)	Strobe signal for write when external data area is accessed, (active low)
$\overline{RESET}$ (Input)	Reset input. RESET is active with low level to perform the initialization of chip, and when high level is applied the program starts from address 0.
$\overline{ALE}$ (Output)	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.
	The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$ (output)	Program Store Enable. This output occurs only during a fetch to external program memory. (active low)
$\overline{SS}$ (Input)	Single step input (active low) When low level is applied, CPU is placed in the WAIT state after completing the execution of currently being executed instruction.
	In this case ALE is held at the high level and when the external program area is accessed, the address executed next is output on DB_0 through DB_7 and P_{20} through P_{23}.
$\overline{EA}$ (Input)	External address designation input. When +5 volt level is applied, the internal program is disabled and the external program is accessed from address 0. EA is also used for designating the verify (read) mode of the internal program by applying +12 volt level.
$XTAL_1$ (Input)	One side of crystal input for internal oscillator. Also input for external source.
$XTAL_2$ (Input)	Other side of crystal input. Also input for external source. (Both $XTAL_1$ and $XTAL_2$ should be driven with a push-pull source.)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

CRT 9007
μPC FAMILY

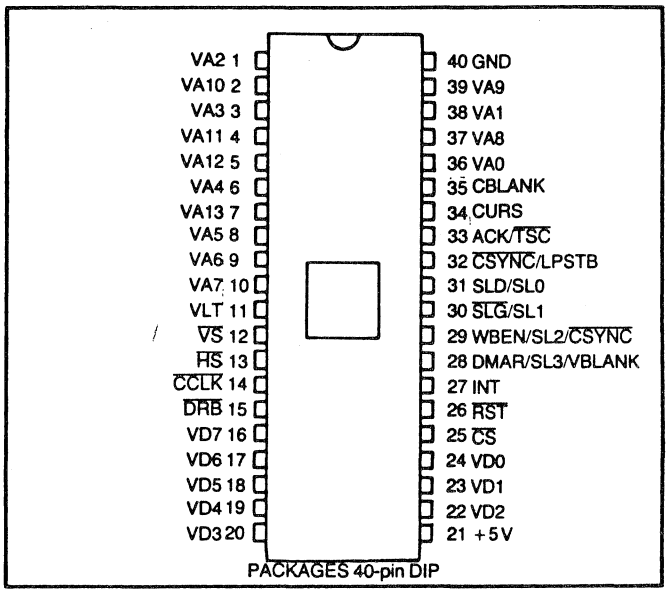
PRELIMINARY

CRT Video Processor and Controller
VPAC™

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch — Horizontal (Negative or Positive)
    — Vertical
  - Sync Width — Horizontal (1-128 Character Times)
    — Vertical (2-256 Scan Lines)
  - Back Porch — Horizontal
    — Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGES 40-pin DIP

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

GENERAL DESCRIPTION

The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".

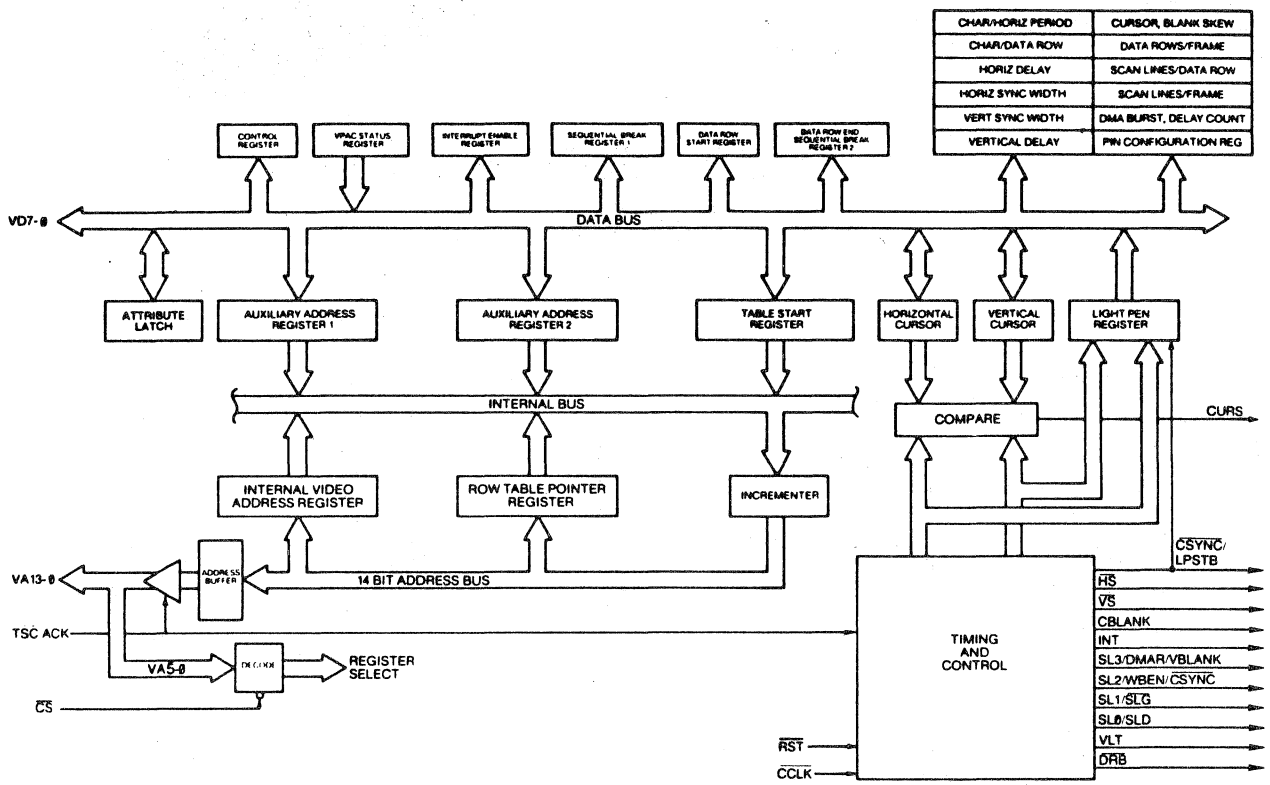


FIGURE 1: CRT 9007 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional. —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.
25	Chip strobe	$\overline{CS}$	Input; this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.
26	Reset	$\overline{RST}$	Input; this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync ($\overline{HS}$) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.
27	Interrupt	INT	Output; an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock ($\overline{CCLK}$) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	$\overline{VS}$	Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$).
13	Horizontal Sync	$\overline{HS}$	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$).
14	Character Clock	$\overline{CCLK}$	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	$\overline{DRB}$	Output; this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation.
34	Cursor	CURS	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SL0 are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	$\overline{CSYNC}$	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats.
30	Scan Line Gate	$\overline{SLG}$	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with SLD (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	SLD	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	$\overline{TSC}$	Input; this signal, when active low, places VA13-VA0 in their high impedance state.

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately [(N-1)/N] × 100 where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

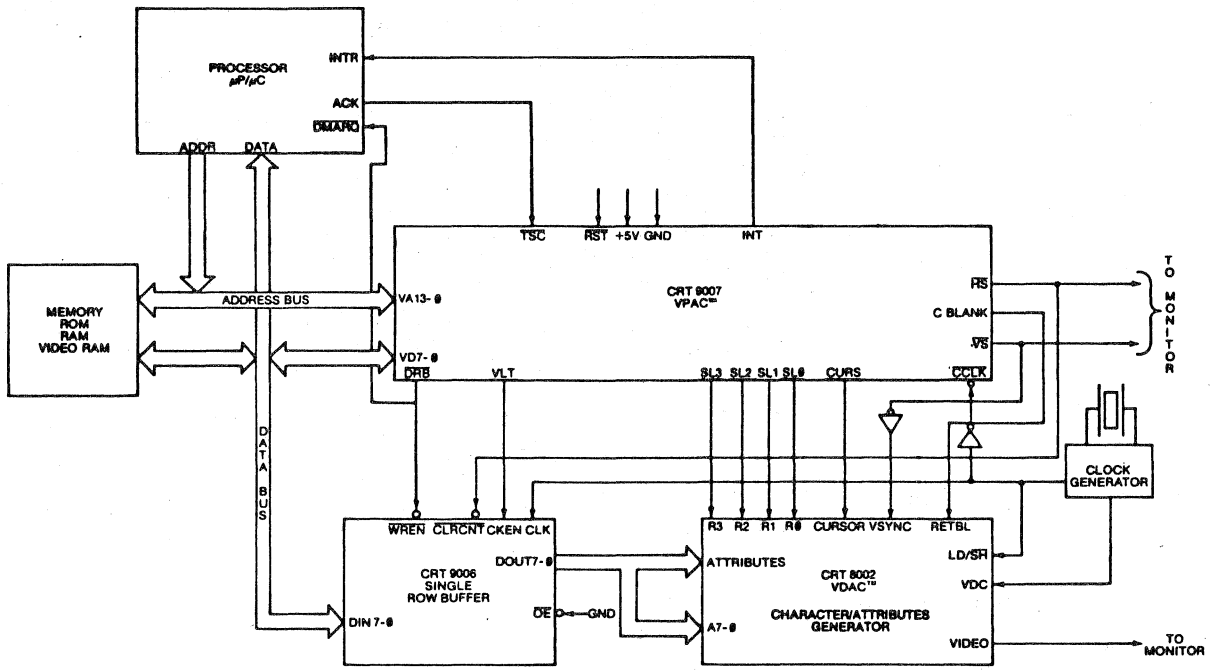


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

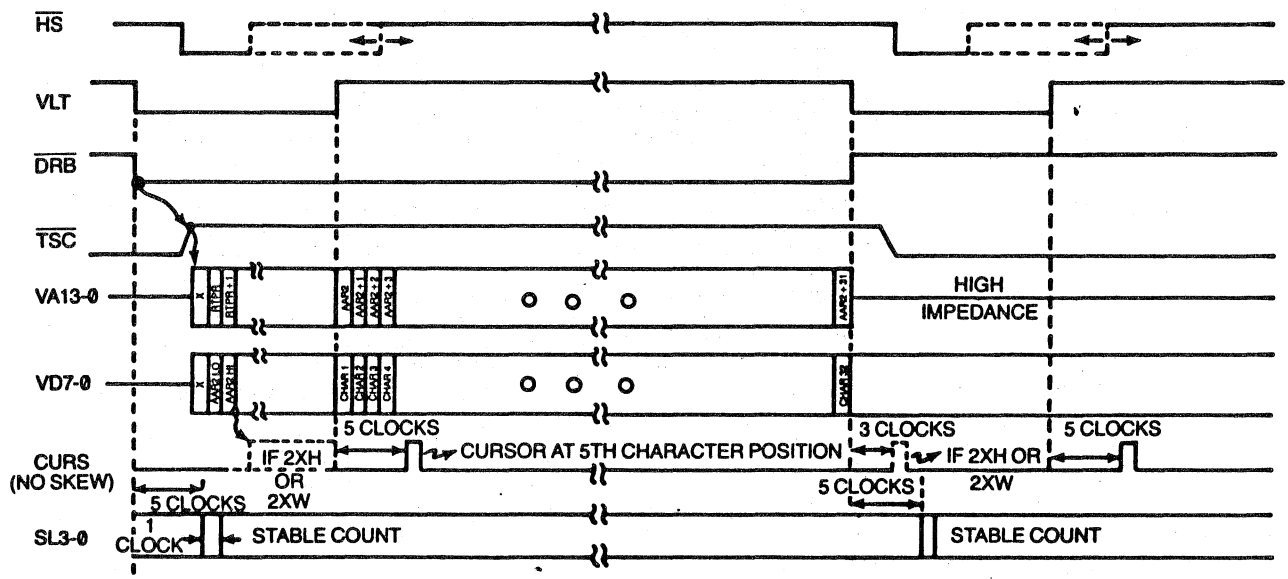


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

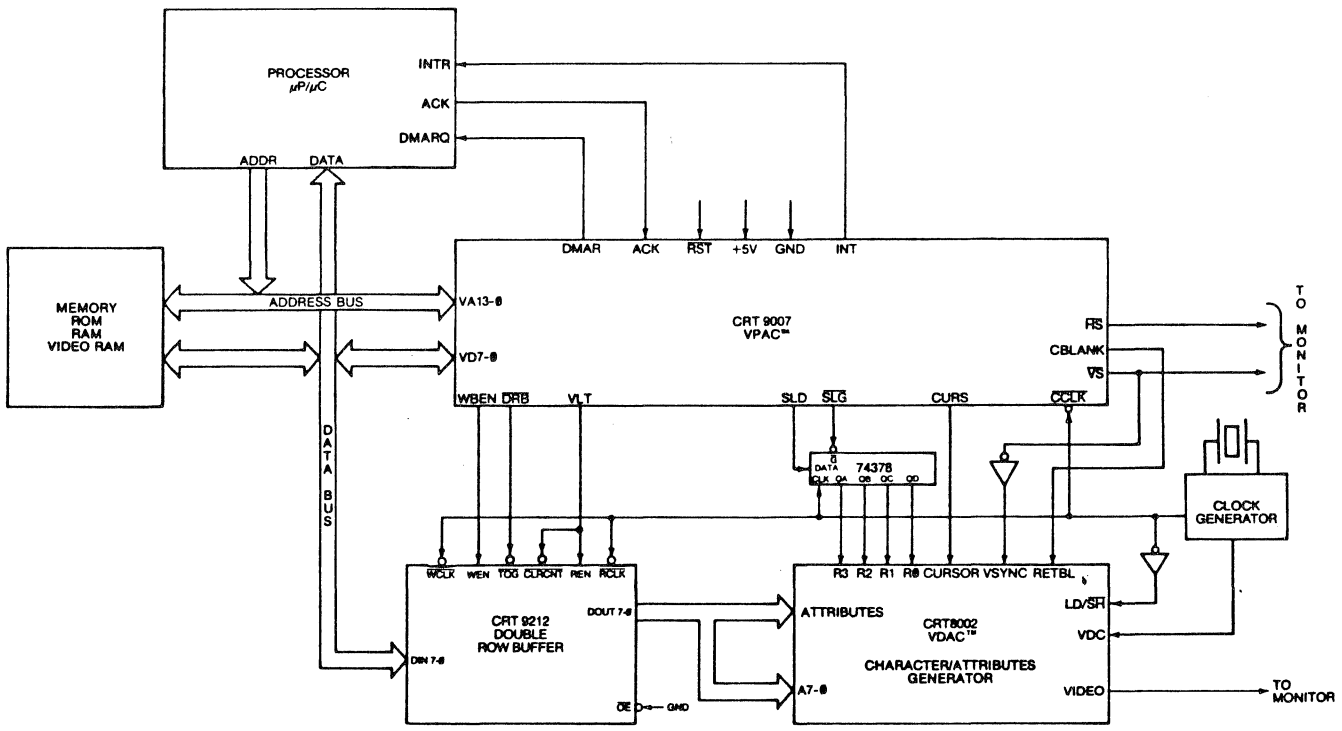


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

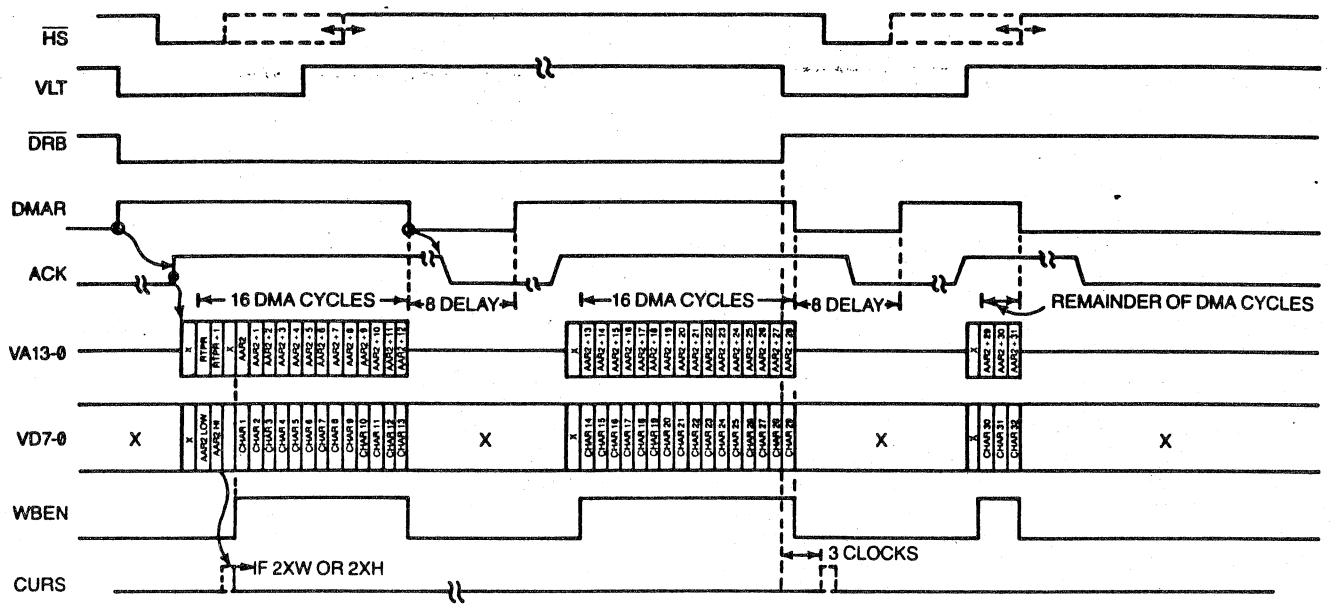


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

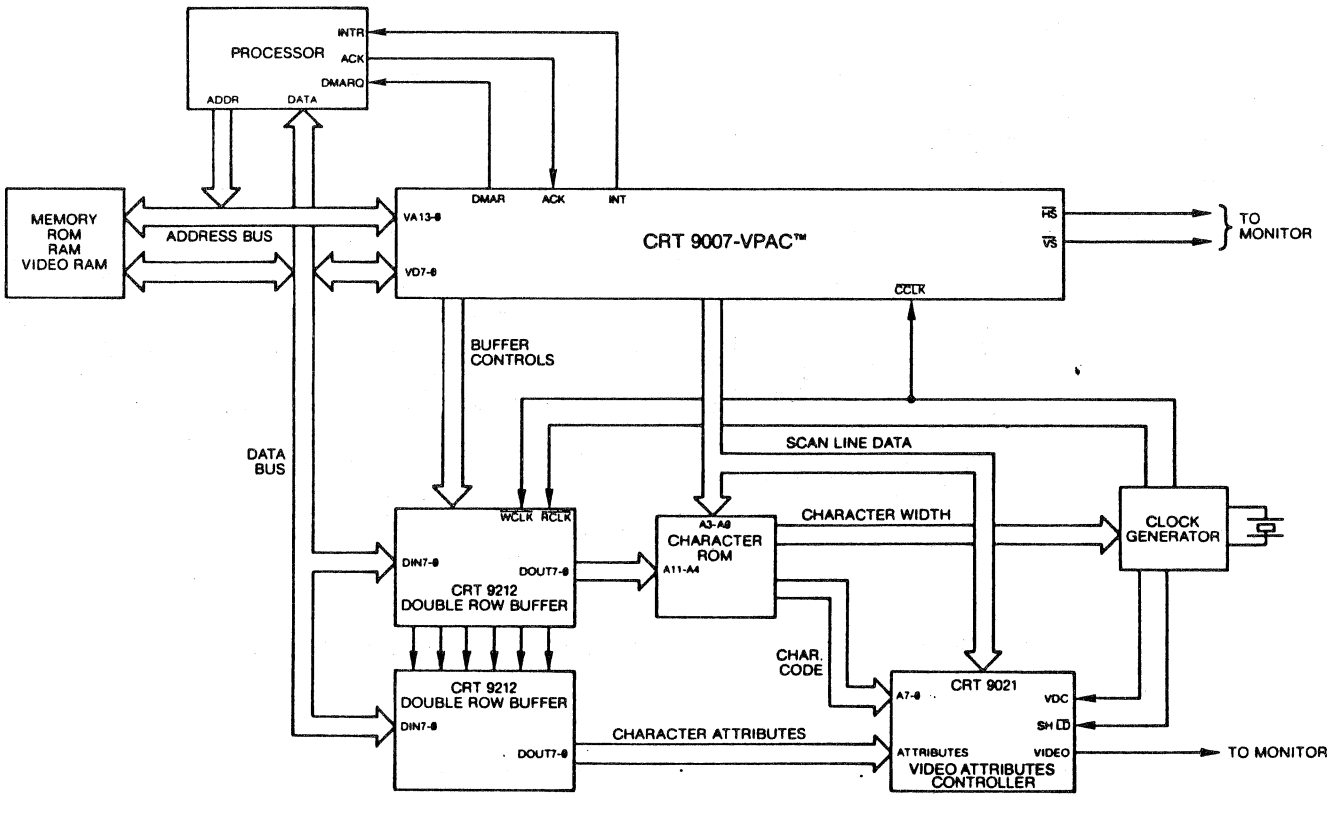


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

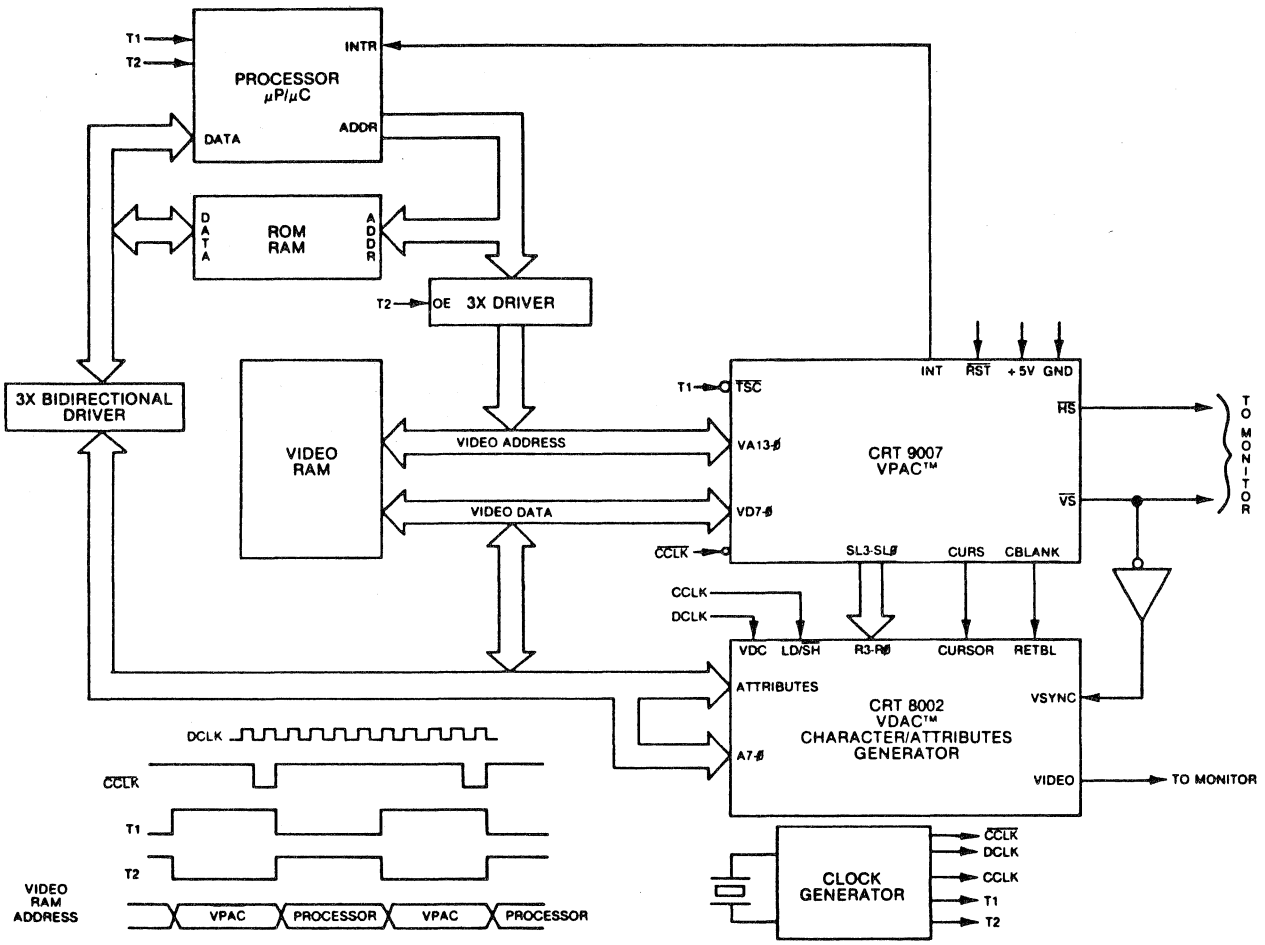


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

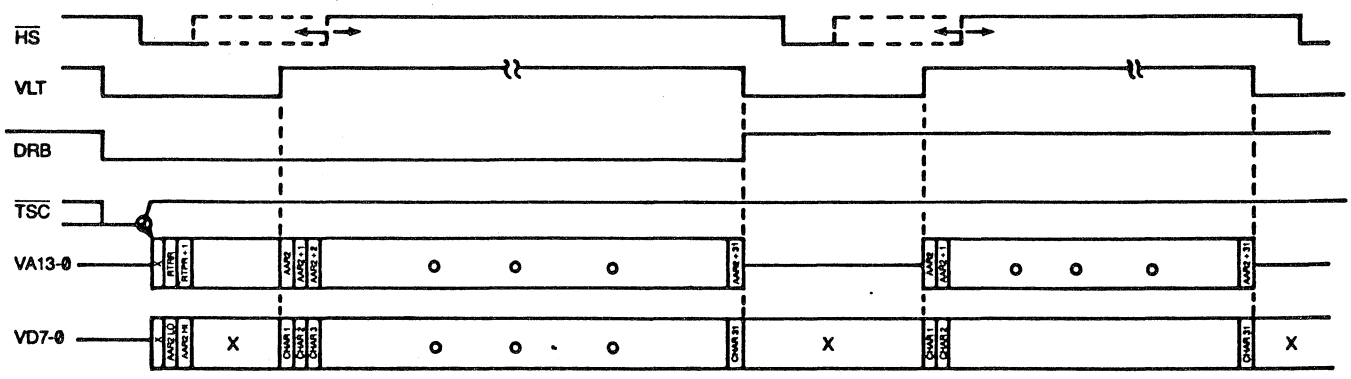


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

Memory Address (typ)	Memory Data (8 bits)
0D00	Attribute 0
0D01	Character 0
0D02	Attribute 1
0D03	Character 1
0 0 0	0 0 0
2N	Attribute N
2N + 1	Character N

Figure 13: Attribute Assemble Memory Organization

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

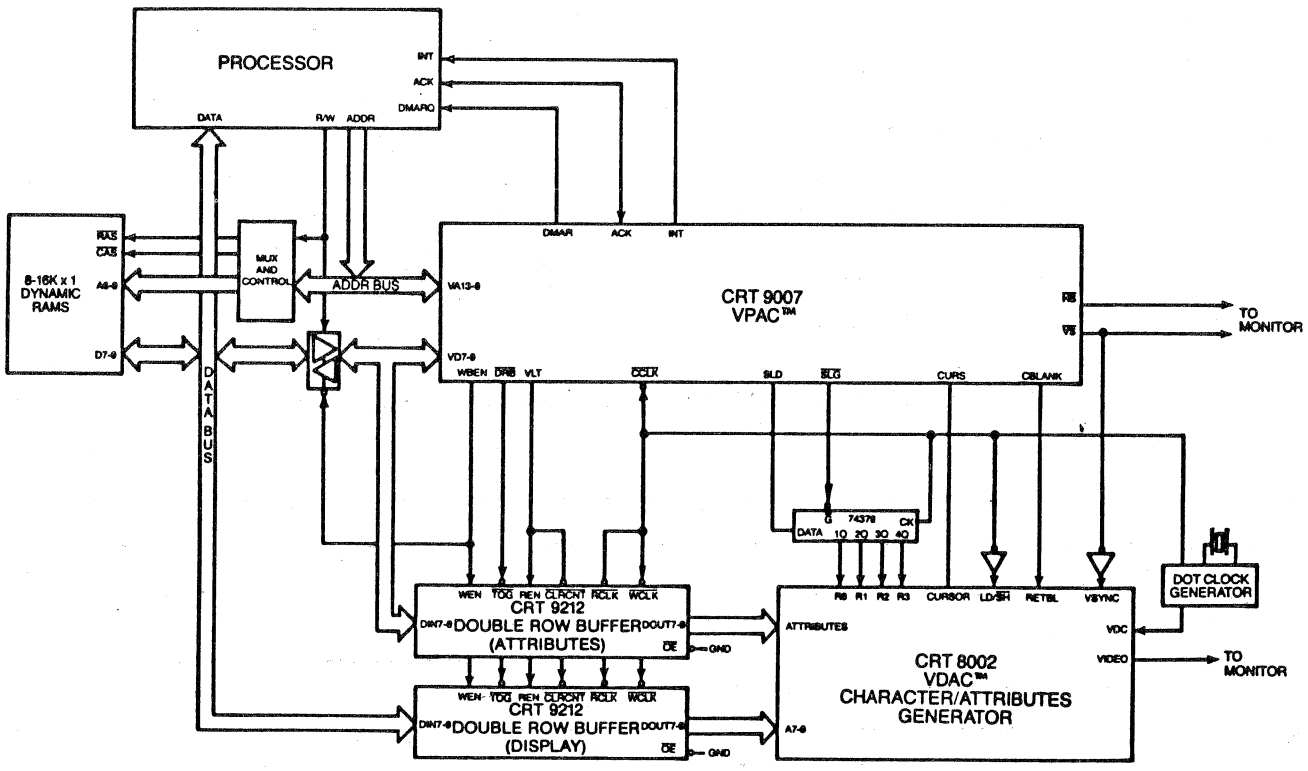
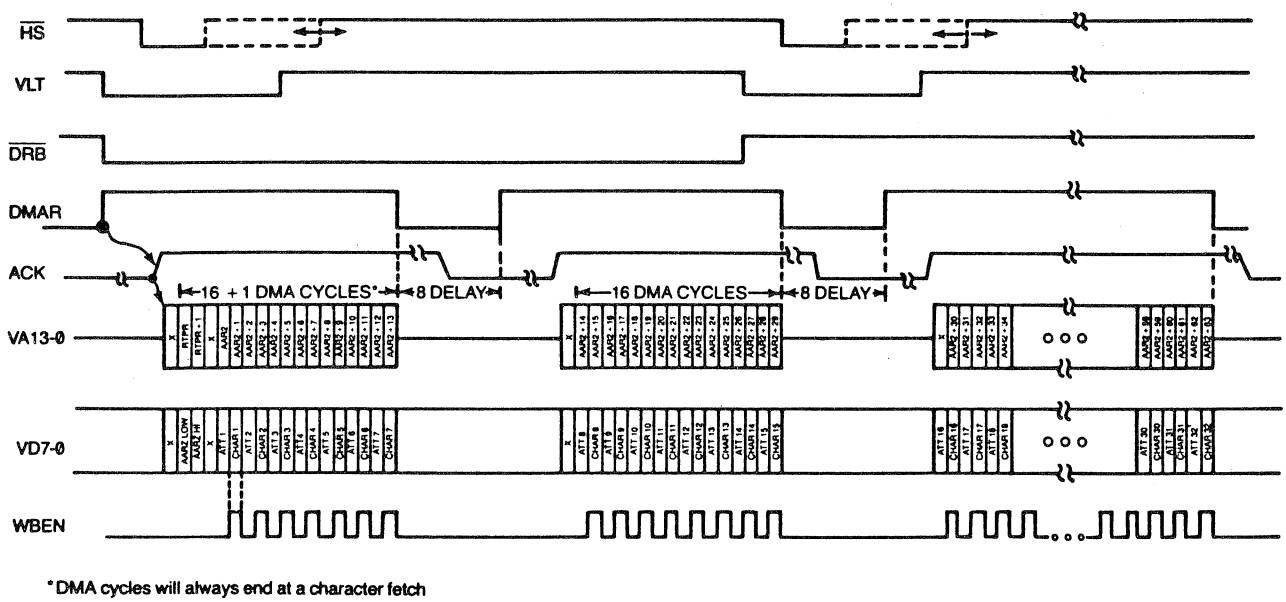


FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE

Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).



*DMA cycles will always end at a character fetch

FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)

Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

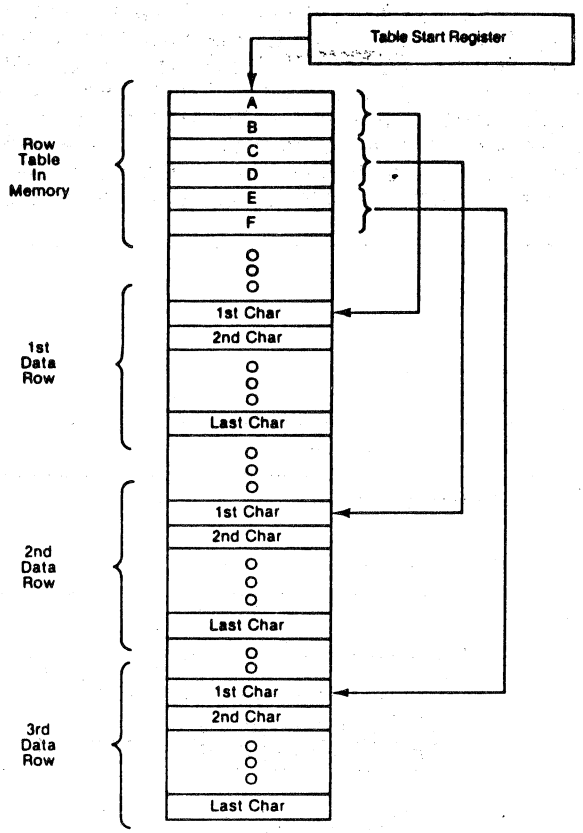


FIGURE 16:
CONTIGUOUS ROW TABLE ADDRESS FORMAT

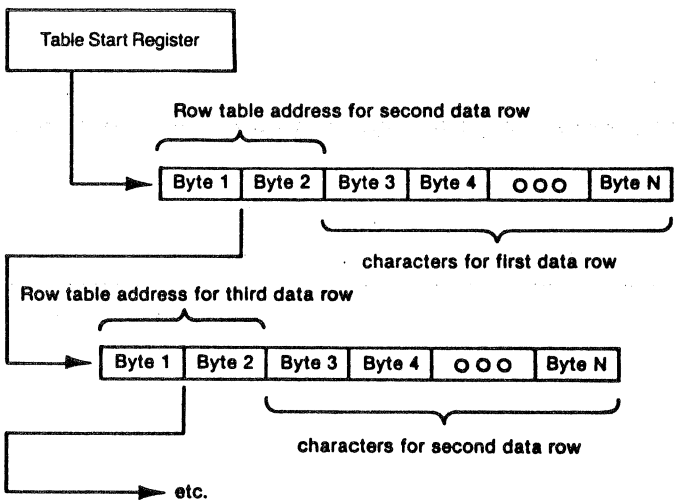


FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT

Sequential Addressing

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range	
0	1000 to 104 F	
1	1050 to 109F	
2	10A0 to 10EF	
3	2000 to 204F	(Break 1)
4	2050 to 209F	
5	20A0 to 20EF	
6	0800 to 084F	(Break 2)
7	0850 to 089F	
8	08A0 to 08EF	
	O	
	O	
	O	

Figure 18: Sequential Addressing Example With Two Breaks

Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or SLG, SLD) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 CCLK's after VLT trailing edge and stays active for exactly 1 CCLK assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 CCLK's to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can never stand alone and is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER 0 rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N-1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

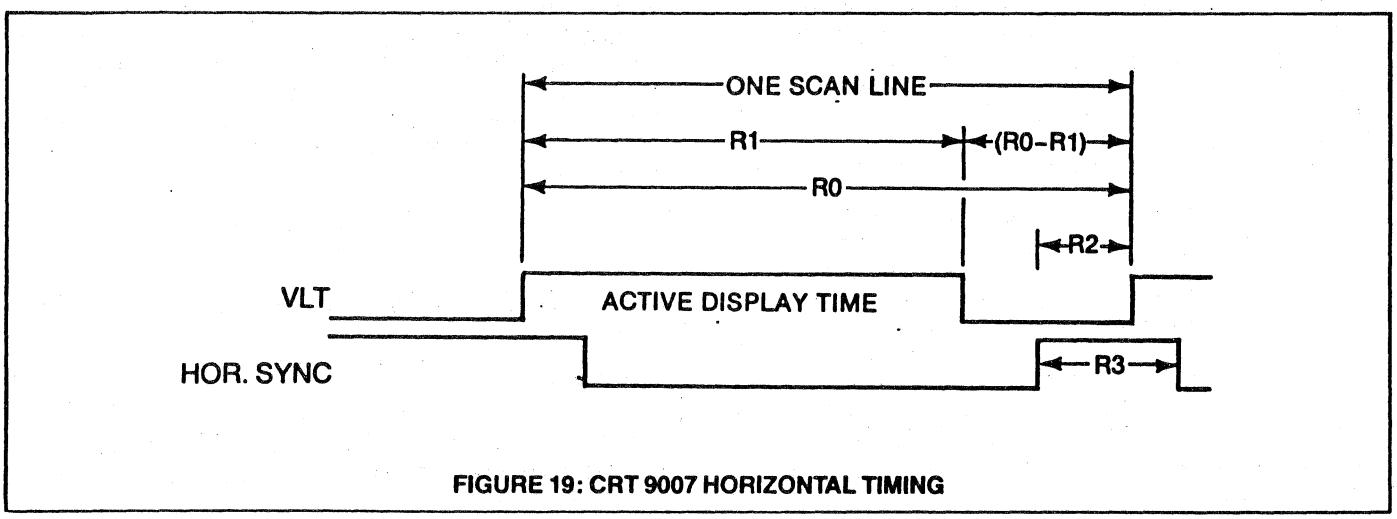


FIGURE 19: CRT 9007 HORIZONTAL TIMING

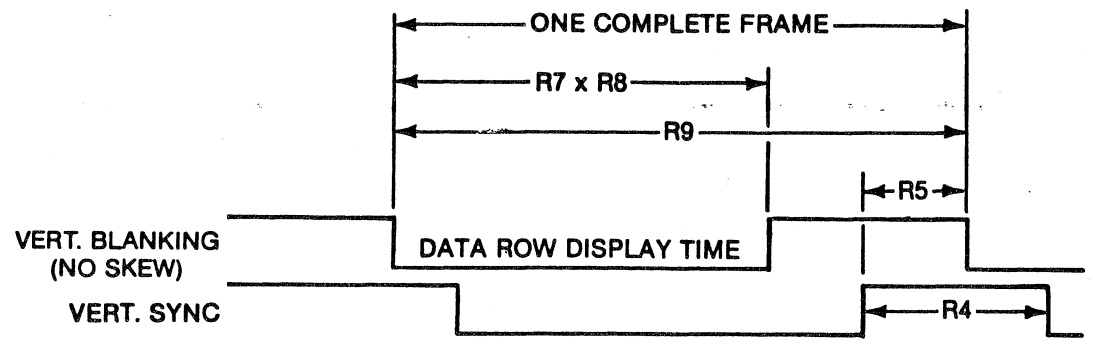


FIGURE 20: CRT 9007 VERTICAL TIMING

PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	$\overline{SLG}$	SLD	$\overline{CSYNC}$	ACK
1	1	DMAR	WBEN	$\overline{SLG}$	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	$\overline{CSYNC}$	TSC
1	0	SL3	$\overline{SL2}$	SL1	SL0	LPSTB	TSC
1	1	VBLANK	$\overline{CSYNC}$	$\overline{SLG}$	SLD	LPSTB	TSC
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur (4 × 1 = 4) and when programmed with 1111 the maximum DMA Burst will occur (4 × 16 = 64). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the $\overline{DRB}$ (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

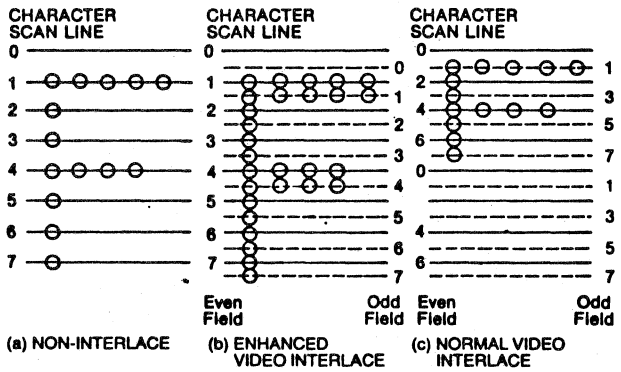


FIGURE 21: CRT 9007 INTERLACE MODES

TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. One break is allowed in the sequential addressing scheme as defined by SEQUENTIAL BREAK REGISTER 1 (R10) and AUXILIARY ADDRESS REGISTER 1 (RE and RF).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the $\overline{RST}$ input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
$\overline{VD}$7-0	High impedance
$\overline{HS}$	High
$\overline{VS}$	High
CBLANK	High
CUS	Low
$\overline{VLT}$	Low
$\overline{DRB}$	High
INT	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

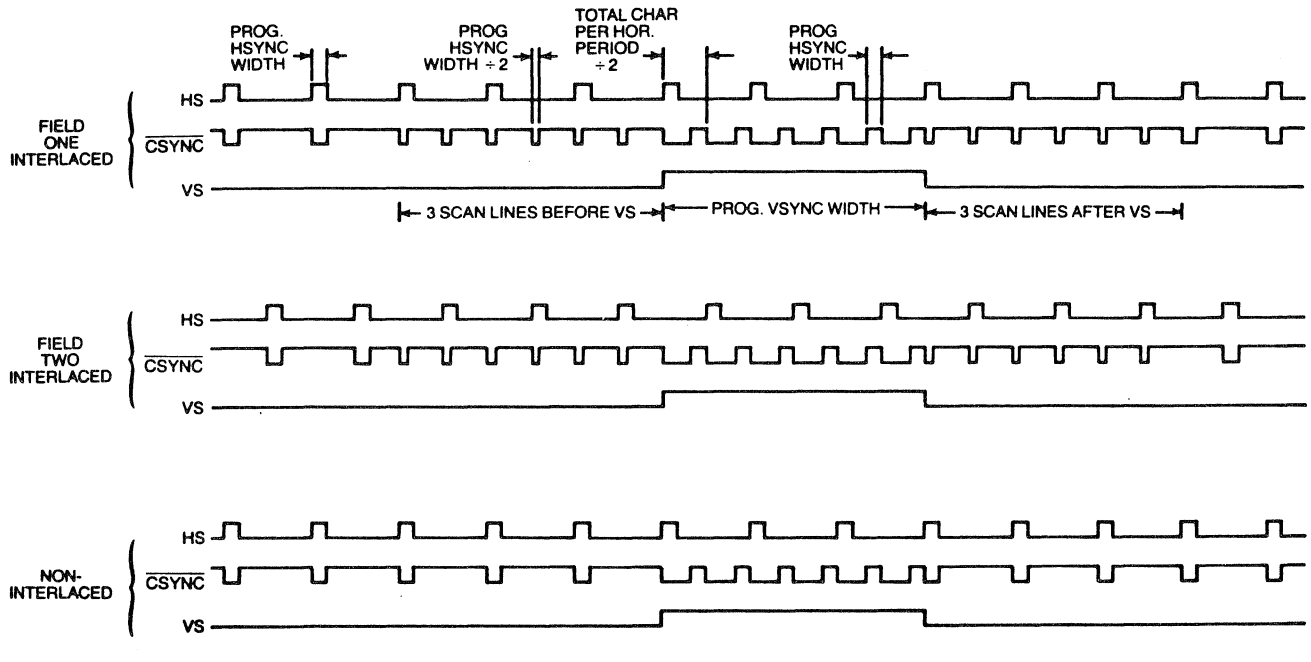


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

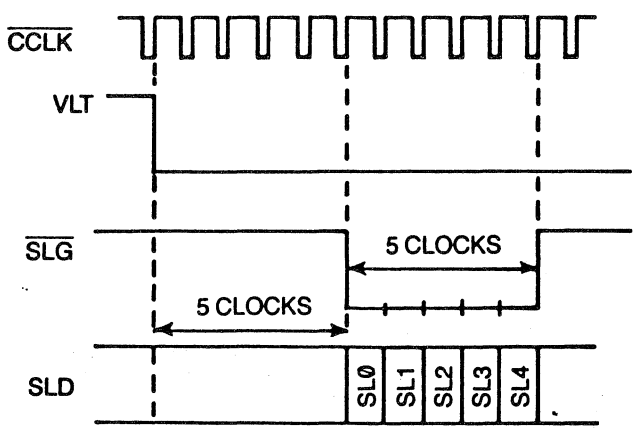


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

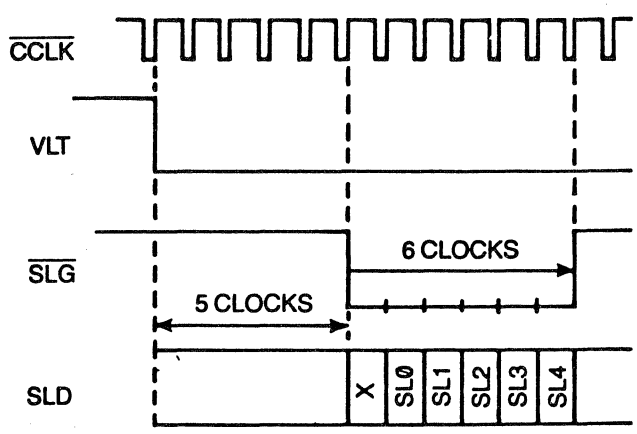


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE, DOUBLE HEIGHT OR DOUBLE WIDTH CHARACTERS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +15V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2.0			V	all inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input
	Output voltage					
V_{OL}	Low			0.4	V	$I_{OL} = 1.6$ mA
V_{OH}	High	2.4			V	$I_{OH} = 40\mu A$
	Input leakage current					
I_{L1}				10	μA	$0 \leq V_{IN} \leq V_{CC}$; excluding $\overline{CCLK}$
I_{L2}				50	μA	$0 \leq V_{IN} \leq V_{CC}$; for $\overline{CCLK}$
	Input capacitance					
C_{IN1}			10		pF	all inputs except $\overline{CCLK}$
C_{IN2}			25		pF	$\overline{CCLK}$ input
	Power supply current					
I_{CC}			100		mA	

AC ELECTRICAL CHARACTERISTICS[3] $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Clock					
t_{CY}	clock period	250			ns	
t_{CKL}	clock low	23			ns	
t_{CKH}	clock high	203			ns	
t_{CKR}	clock rise time			10	ns	measured from 10% to 90% points
t_{CKF}	clock fall time			10	ns	measured from 90% to 10% points
	Output delay[1]					
t_{D1}				125	ns	
t_{D2}				125	ns	
t_{D3}				150	ns	
t_{D4}				150	ns	
t_{VA}				100	ns	measured to the 2.3V or 0.5V level on VA13-VA0
t_{DSL}				500	ns	
t_{D5}				185	ns	
t_{D6}				185	ns	
t_{DSY}				185	ns	
t_{VDS}		50			ns	valid for loading auxiliary address register 2 or the attribute latch
t_{VDH}		0			ns	
t_{VD0}				185	ns	$C_L = 50pF$
t_{SLG}				185	ns	
t_{SLD}				185	ns	
	Processor Read/write[2]					
t_{AS}		100			ns	
t_{AH}		0			ns	
t_{PW}		155			ns	
t_{PDS}		100			ns	
t_{PDH}		0			ns	
t_{PDA}				140	ns	
t_{PDH}		10		50	ns	
t_{IRR}				400	ns	
	Miscellaneous timing					
t_{ATS}				125	ns	measured from the 0.4V level of ACK or $\overline{TSC}$ falling edge
t_{RW}				$4t_{CY}$	ns	measured from the 0.4V level falling edge to 0.4V level rising edge

NOTE:
1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.

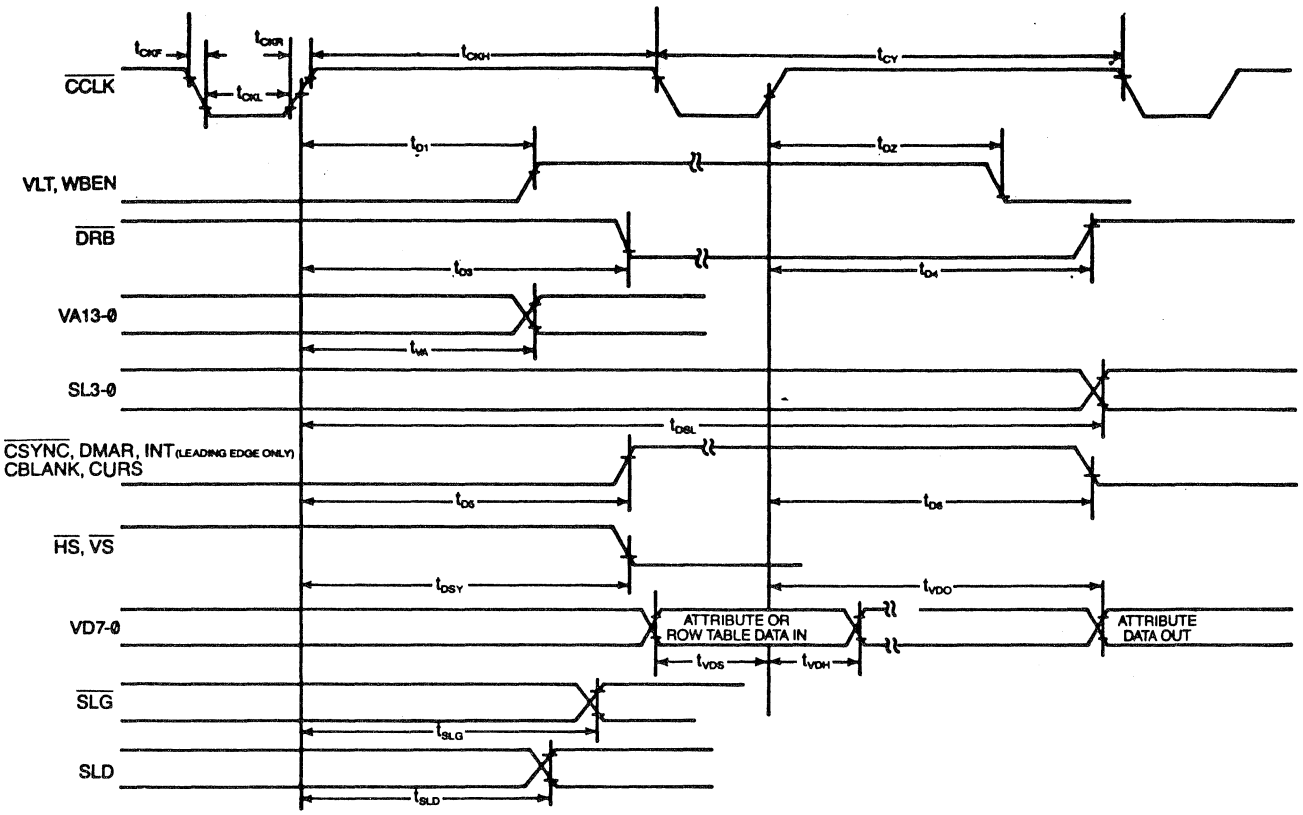


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

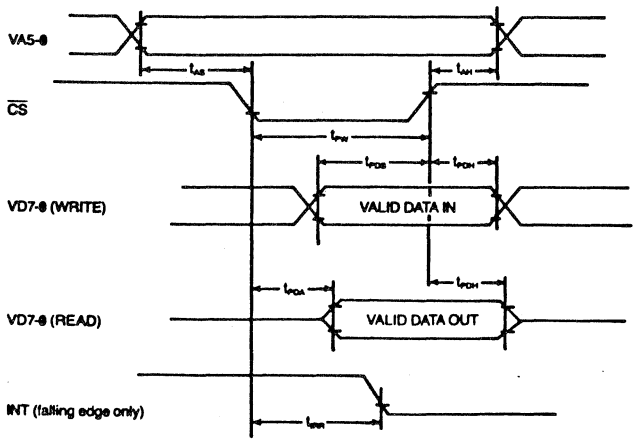
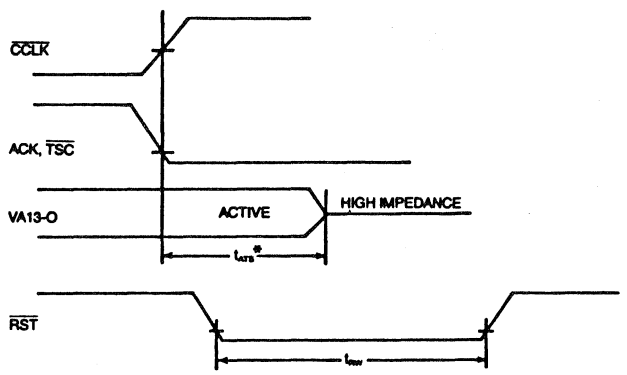


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{ARS} is controlled directly from ACK or $\overline{TSC}$ or from the particular $\overline{CCLK}$ that ends a DMA burst cycle.

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	0	0	0	0	MSB	CHARACTERS PER HORIZONTAL PERIOD						LSB	R0
WRITE	0	0	0	0	0	1	MSB	CHARACTERS PER DATA ROW						LSB	R1
WRITE	0	0	0	0	1	0	MSB	HORIZONTAL DELAY						LSB	R2
WRITE	0	0	0	0	1	1	MSB	HORIZONTAL SYNC WIDTH						LSB	R3
WRITE	0	0	0	1	0	0	MSB	VERTICAL SYNC WIDTH						LSB	R4
WRITE	0	0	0	1	0	1	MSB	VERTICAL DELAY						LSB	R5
WRITE	0	0	0	1	1	0	PIN CONFIG-URATION	CURSOR SKEW MSB			LSB	BLANK SKEW MSB		LSB	R6
WRITE	0	0	0	1	1	1	MSB	VISIBLE DATA ROWS PER FRAME						LSB	R7
WRITE	0	0	1	0	0	0	SCAN LINES/FRAME (B10))	(B8)	MSB	SCAN LINES PER DATA ROW				LSB	R8
WRITE	0	0	1	0	0	1	(B7)	SCAN LINES PER FRAME						LSB (B0)	R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	1	0	1	0	DMA DIS-ABLE	DMA BURST DELAY MSBA		LSB	DMA BURST COUNT MSB			LSB	RA
WRITE	0	0	1	0	1	1	X	PB/SS	INTERLACE MODES		OPERATION MODES			2XC/1XC	RB
WRITE	0	0	1	1	0	0	MSB	TABLE START REGISTER (LS BYTE)						LSB	RC
WRITE	0	0	1	1	0	1	ADDRESS MODE	TABLE STRT REGISTER (MS BYTE) MSB						LSB	RD
WRITE	0	0	1	1	1	0	MSB	AUXILIARY ADDRESS REGISTER 1 (LS BYTE)						LSB	RE
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB						LSB	RF
WRITE	0	1	0	0	0	0	MSB	SEQUENTIAL BREAK REGISTER 1						LSB	R10
WRITE	0	1	0	0	0	1	MSB	DATA ROW START REGISTER						LSB	R11
WRITE	0	1	0	0	1	0	MSB	DATA ROW END/SEQUENTIAL BREAK REGISTER 2						LSB	R12
WRITE	0	1	0	0	1	1	MSB	AUXILIARY ADDRESS REGISTER 2 (LS BYTE)						LSB	R13
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB						LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	VA5	VA4	VA3	VA2	VA1	VA0	D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW	OFFSET VALUE MSB					LSB	0	R17
WRITE	0	1	1	0	0	0	MSB	VERTICAL CURSOR REGISTER (ROW COORD.)						LSB	R18 or R19
READ	1	1	1	0	0	0									
WRITE	0	1	1	0	0	1	MSB	HORIZONTAL CURSOR REGISTER (COL. COORD.)						LSB	R19 or R39
READ	1	1	1	0	0	1									
WRITE	0	1	1	0	1	0	X	VER-TICAL RE-TRACE	LIGHT PEN	INTERRUPT ENABLE REGISTER X	X	X	X	FRAME TIMER	R1A
READ	1	1	1	0	1	0	INT PEND-ING	VER-TICAL RE-TRACE	LIGHT PEN	STATUS REGISTER		ODD/ EVEN	X	FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB	VERTICAL LIGHT PEN REGISTER (ROW COORD.)						LSB	R3B
READ	1	1	1	1	0	0	MSB	HORIZONTAL LIGHT PEN REGISTER (COL. COORD.)						LSB	R3C

Table 3c: Cursor, Light Pen, Offset, and Status Registers

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11787
(516) 273-3100 TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

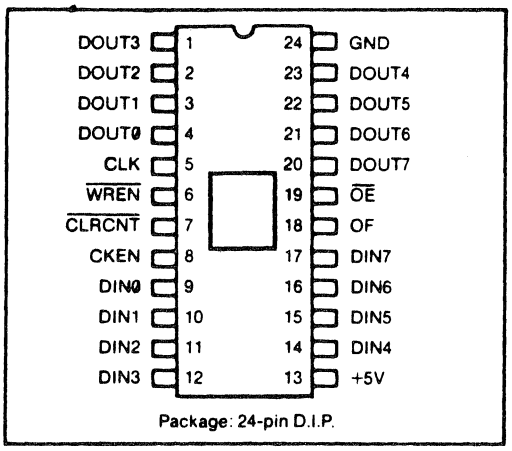
CRT 9006-135
CRT 9006-83*
μPC FAMILY

Single Row Buffer
SRB

FEATURES:

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Provides 8 Bit Wide Variable Length Serial Memory
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row — ...64, 80, 132,... up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- ☐ Three-State Outputs
- ☐ 4MHz Typical Read/Write Data Rate
- ☐ Static Operation
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 24 Pin Dual In Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible Inputs and Outputs
- ☐ Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



Package: 24-pin D.I.P.

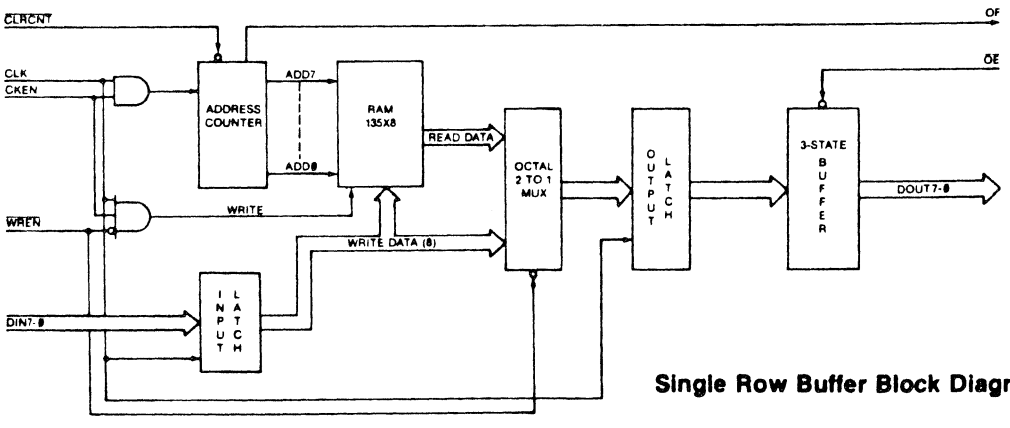
APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

SECTION IV

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable (WREN) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



Single Row Buffer Block Diagram

*FOR FUTURE RELEASE

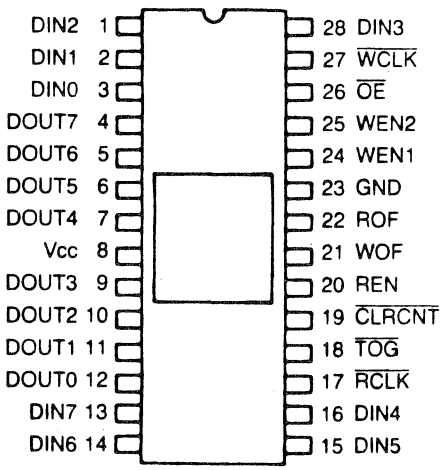
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Double Row Buffer
DRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 28 Pin Dual-In-Line Package
- ☐ + 5 Volt Only Power Supply
- ☐ TTL Compatible

GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

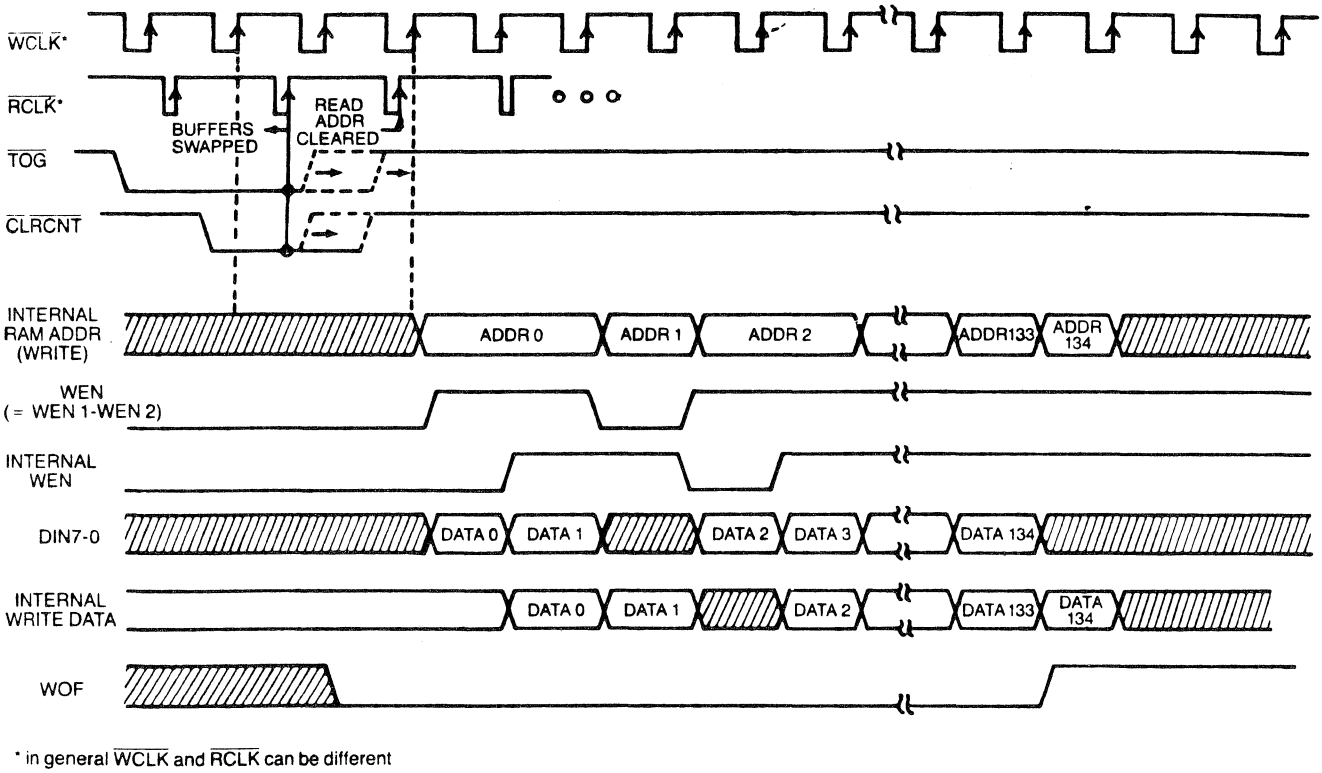
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	
High Level V_{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	µA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	µA	excluding WEN1
High Leakage I_{LH2}			400	µA	WEN1
Low Leakage I_{LL2}			400	µA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

AC CHARACTERISTICS[1]

t_{CYW}	250			ns	Write clock period
t_{CYR}	250			ns	Read clock period
t_{CKH}	200		DC	ns	
t_{CKL}	30			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{RCLK}$
t_{DH}	0			ns	referenced to $\overline{RCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50 pF; referenced from $\overline{WCLK}$
t_{DOFF}			175	ns	
t_{DON}			175	ns	
t_{OF}[3]			175	ns	C_L = 30 pF
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[4]		$1t_{CYW}$			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).



* in general $\overline{WCLK}$ and $\overline{RCLK}$ can be different

FIGURE 3: CRT 9212 DOUBLE ROW BUFFER WRITE TIMING

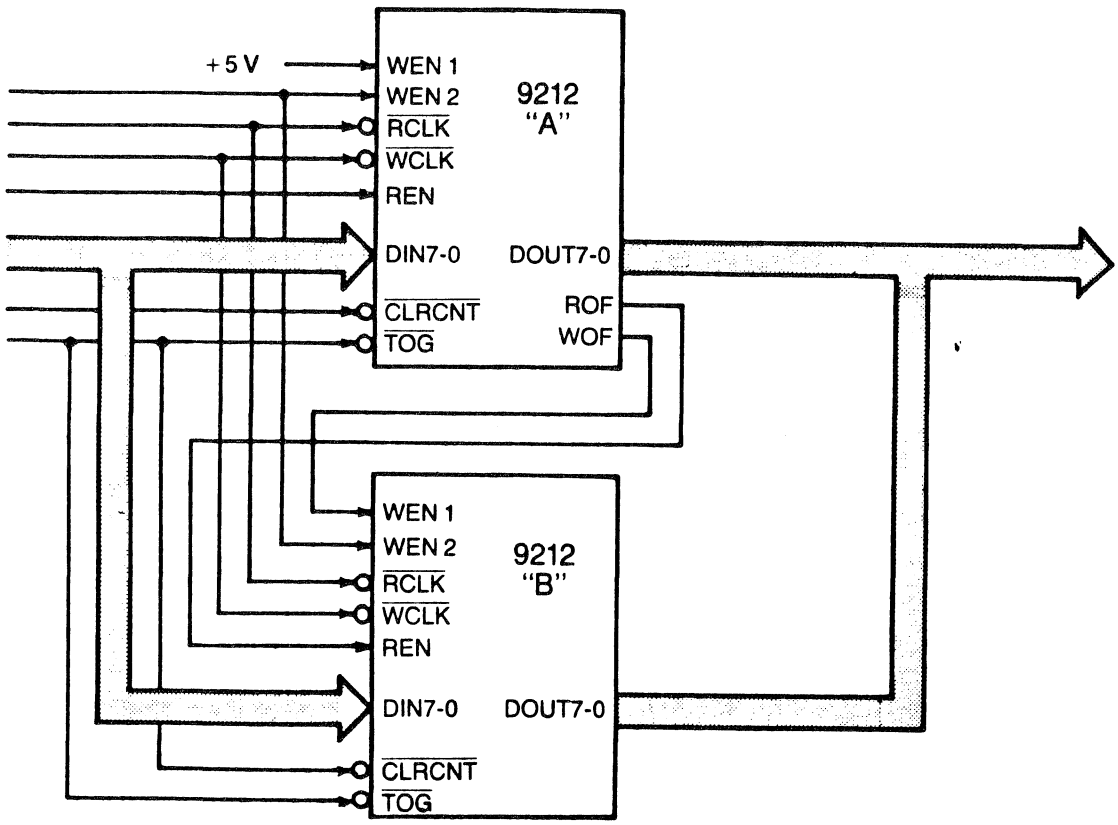


FIGURE 4: CRT 9212 CASCADED CONFIGURATION FOR DATA ROW LENGTHS UP TO 270 CHARACTERS

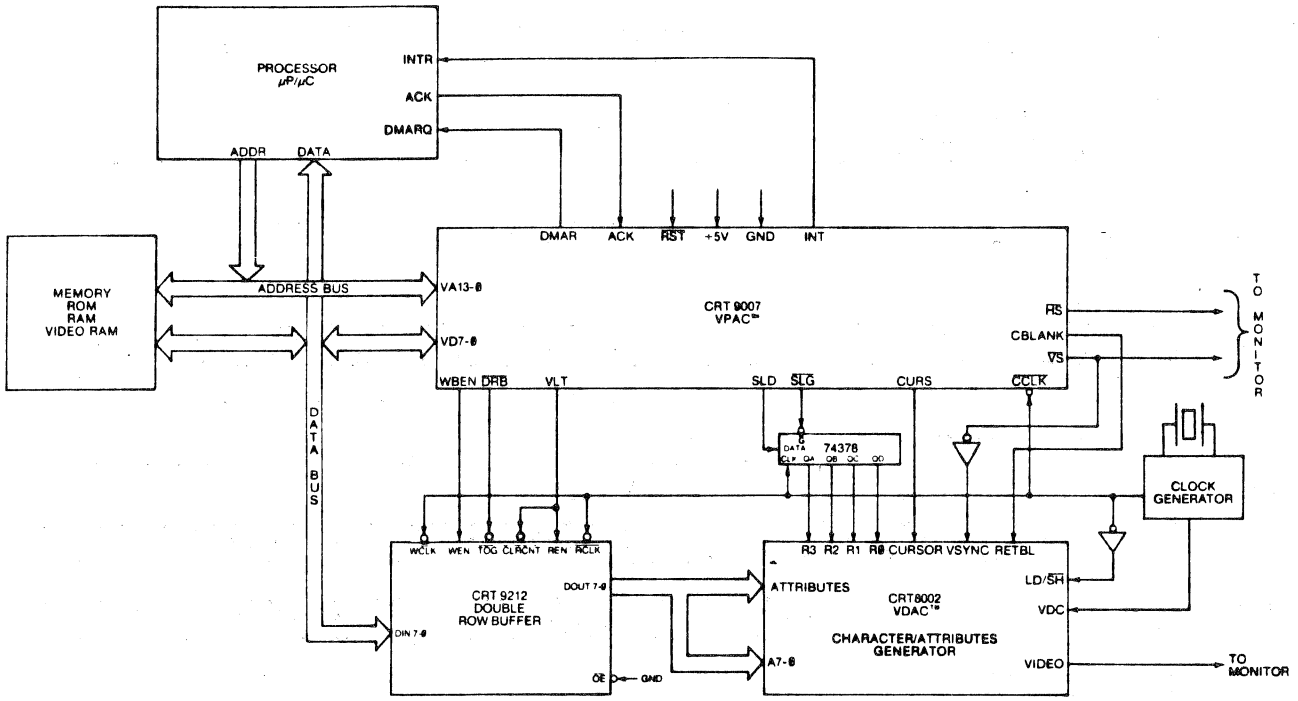


FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™

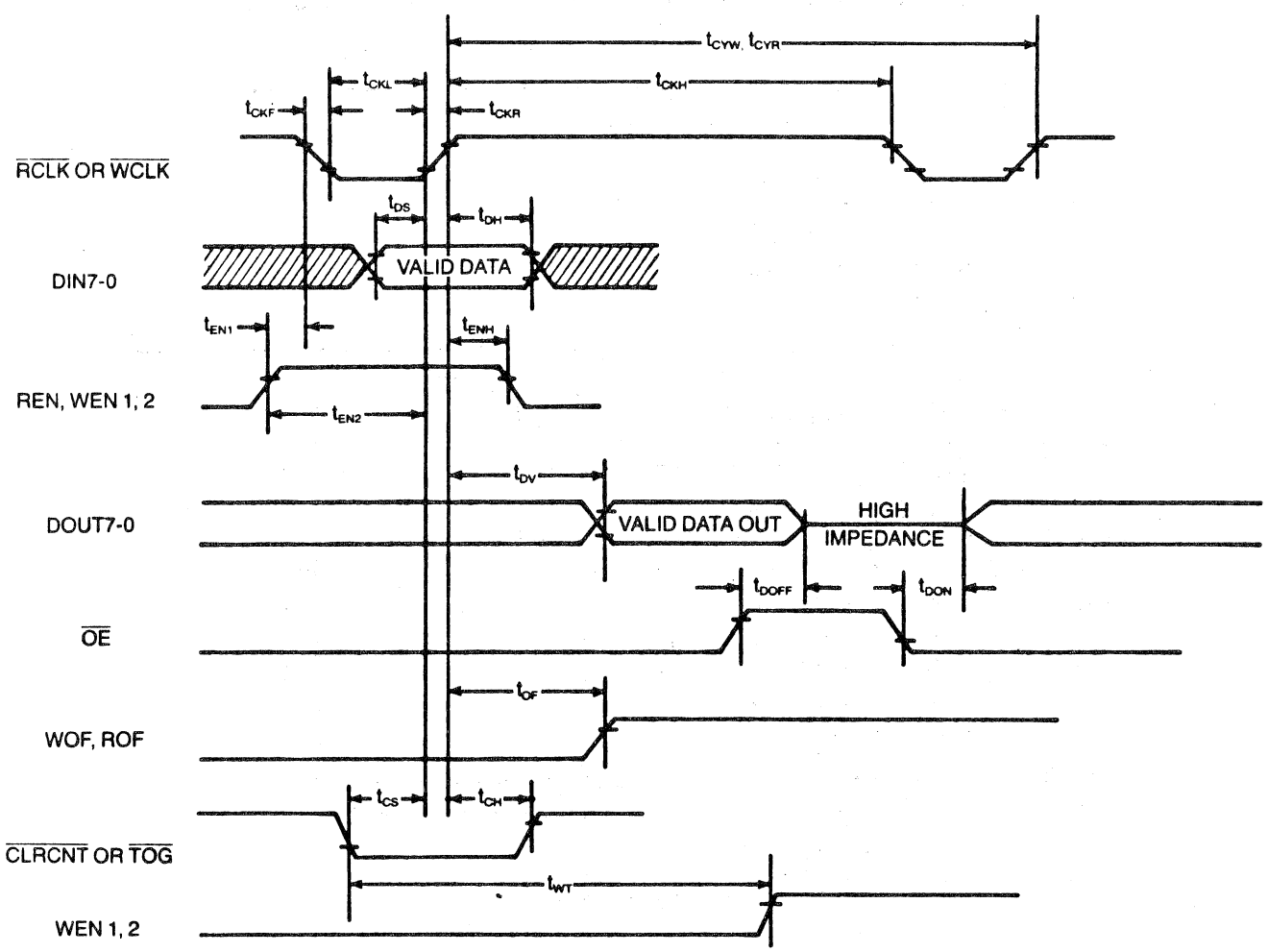


FIGURE 6: CRT 9212 I/O TIMING

DESCRIPTION OF PIN FUNCTIONS

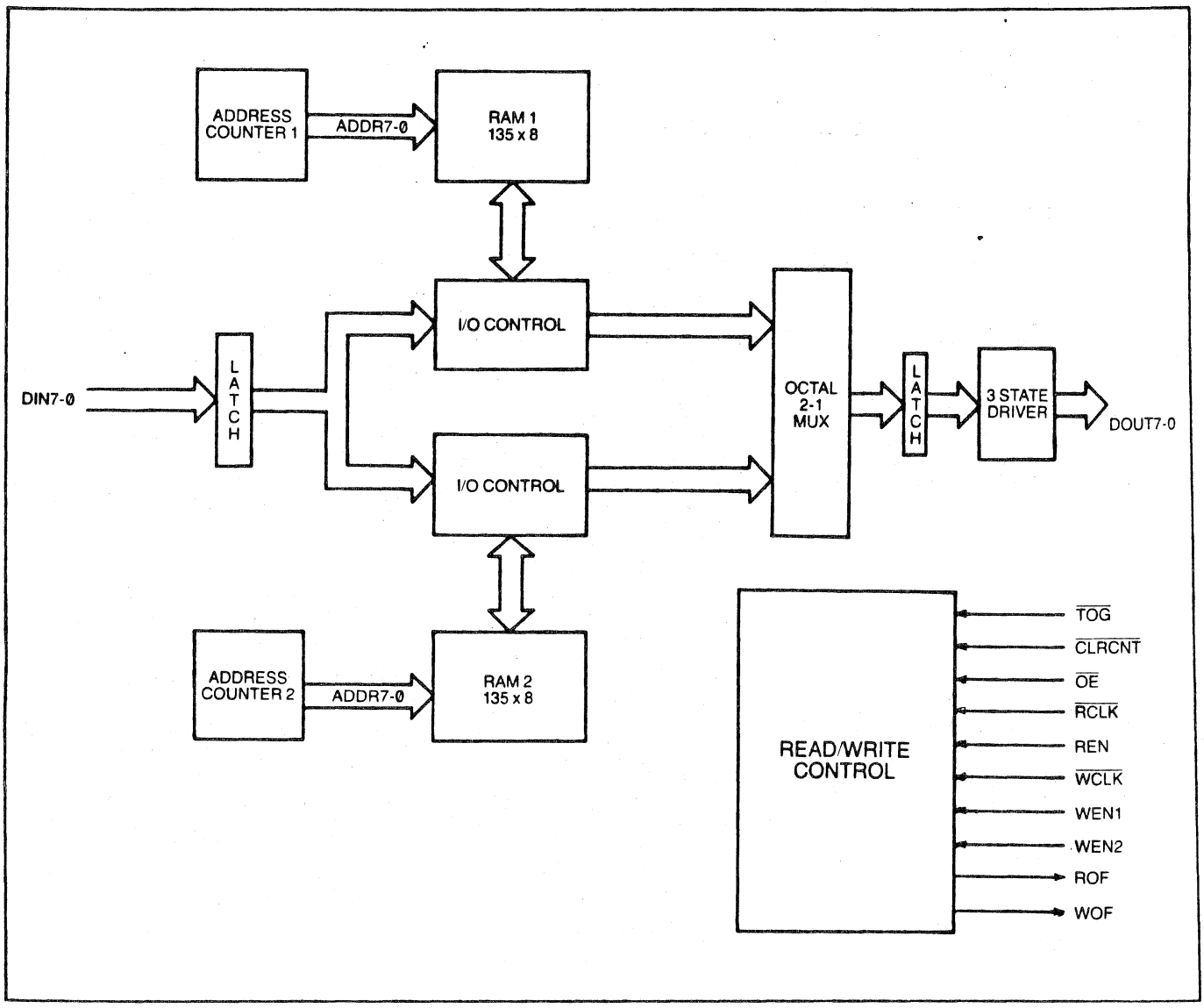
PIN NO.	NAME	SYMBOL	FUNCTION
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN0-DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	$\overline{RCLK}$	$\overline{RCLK}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	Toggle Signal	$\overline{TOG}$	$\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and CLRCNT are low.
19	Clear Counter	$\overline{CLRCNT}$	Clear Counter clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of $\overline{RCLK}$ after ROF goes high. See figure 4.
24, 25	Write Enable	WEN1, WEN 2	WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	$\overline{OE}$	When the $\overline{OE}$ input is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state. $\overline{OE}$ has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	$\overline{WCLK}$	$\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{CC}	+5 Volt supply
23	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN 2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.



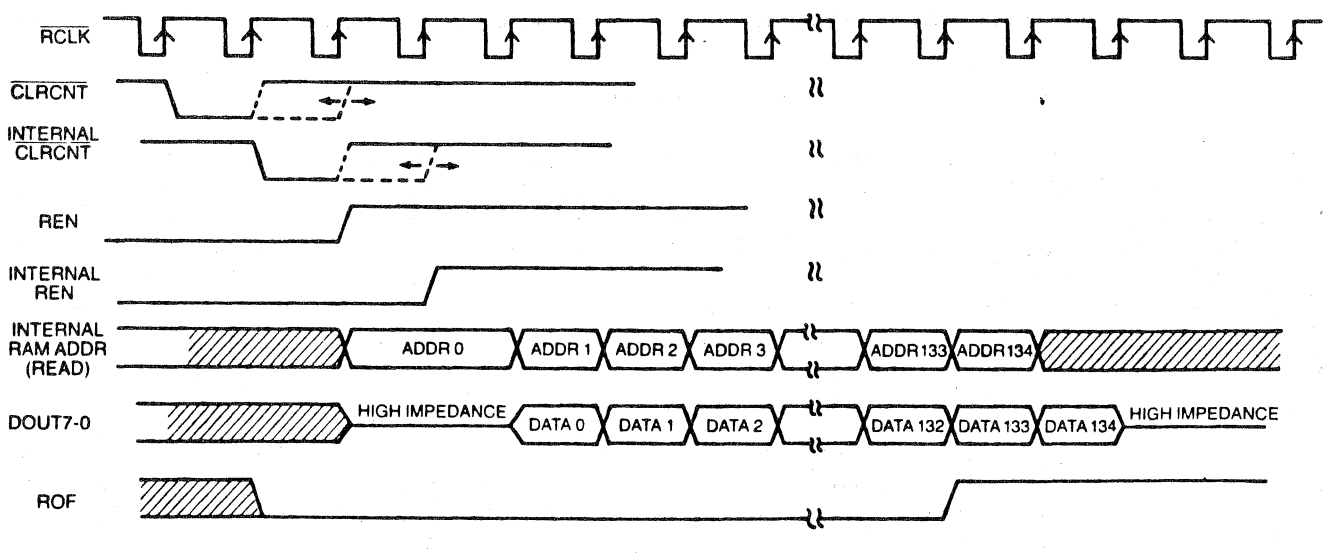


FIGURE 2: CRT 9212 DOUBLE ROW BUFFER READ TIMING