# Architectural Features 15

This volume describes the basic features and operation of embedded Pentium® processors:

- Embedded Pentium processors with maximum operating frequencies of 100, 133, and 166 MHz
- Embedded Pentium processors with Voltage Reduction Technology with a maximum operating frequency of 133 MHz
- Embedded Pentium processors with MMX™ technology with maximum operating frequencies of 200 and 233 MHz
- Low-power embedded Pentium processors with MMX™ technology with maximum operating frequencies of 166 and 266 MHz

The general terms “processor,” “embedded Pentium processor,” and “embedded Pentium processor family” are used throughout this manual to refer to the embedded Pentium processor, the embedded Pentium processor with Voltage Reduction Technology, the embedded Pentium processor with MMX technology, and the low-power embedded Pentium processor with MMX technology together. Some of the features or functions described using these terms, however, may not be available on each processor type. Refer to the datasheet for each product to determine whether a specific feature is offered.

In some instances, the names “embedded Pentium processor (at 100/133/166 MHz),” “embedded Pentium processor with Voltage Reduction Technology,” “embedded Pentium processor with MMX technology,” and “low-power embedded Pentium processor with MMX technology” are used in this manual to distinguish between processors when specific differences exist.

See “Related Documents” on page 1-5 for a list of datasheets and other documents that describe the operation of Pentium processors.

## 15.1 Processor Features Overview

The embedded Pentium processor supports the features of previous Intel® architecture processors and provides significant enhancements, including the following (refer to the datasheet for a specific list of features supported by each processor):

- Superscalar architecture
- Dynamic branch prediction
- Pipelined Floating-Point Unit
- Improved instruction execution time
- Separate code and data caches
- Writeback MESI protocol in the data cache
- 64-bit data bus
- Bus cycle pipelining
- Address parity

- Internal parity checking
- Functional redundancy checking and lock-step operation
- Execution tracing
- Performance monitoring
- IEEE 1149.1 boundary scan
- System Management Mode
- Virtual Mode extensions
- Dual processing support
- Advanced SL power management features
- Fractional bus operation
- On-chip local APIC device

In addition, the embedded Pentium processor with MMX technology offers the following enhancements over the embedded Pentium processor:

- Support for Intel MMX technology
- Dual power supplies—separate $V_{CC2}$ (core) and $V_{CC3}$ (I/O) voltage inputs
- Separate 16-Kbyte, 4-way set-associative code and data caches, each with improved fully associative TLBs
- Pool of four write buffers used by both execution pipelines
- Enhanced branch prediction algorithm
- New Fetch pipeline stage between Prefetch and Instruction Decode

The following features are supported by the embedded Pentium processor, but are not supported by the embedded Pentium processor with MMX technology:

- Functional redundancy checking and lock-step operation
- Support for the Intel 82498/82493 and 82497/82492 cache chipset products
- Split line accesses to the code cache

The following feature is supported by the embedded Pentium processor with MMX technology, but is not supported by the low-power embedded Pentium processor with MMX technology:

- Dual processing support

## 15.2 Component Introduction

The application instruction set of the embedded Pentium processor family includes the complete instruction set of existing Intel Architecture processors to ensure backward compatibility, with extensions to accommodate the additional functionality of the embedded Pentium processor. All application software written for the Intel386™ and Intel486™ microprocessors runs on the embedded Pentium processor without modification. The on-chip Memory Management Unit (MMU) is completely compatible with Intel386 and Intel486 processors.

The embedded Pentium processor with MMX technology adds 57 new instructions and four new data types to accelerate the performance of multimedia and communications software. MMX technology is based on the SIMD technique—Single Instruction, Multiple data—which enables increased performance on a wide variety of multimedia and communications applications. To take advantage of the MMX instructions, software modifications must be made. When the MMX instructions are not used, no hardware or software modifications are needed.

The two instruction pipelines and the floating-point unit on the embedded Pentium processor are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

The embedded Pentium processor with MMX technology adds the Fetch pipeline stage between the Prefetch and Instruction decode stages, which increases the performance capability of the processor. The embedded Pentium processor with MMX technology doubles the number of write buffers available to be used by the dual pipelines.

Branch prediction is implemented in the embedded Pentium processor. To support this, the processor has two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the Branch Target Buffer (BTB) so the needed code is almost always prefetched before it is needed for execution. The branch prediction algorithm has been enhanced on the embedded Pentium processor with MMX technology for increased accuracy.

The embedded Pentium processor includes separate code and data caches integrated on chip to meet its performance goals. Each cache on the embedded Pentium processor with MMX technology is 16 Kbytes in size, and is four-way set associative. The caches on the embedded Pentium processor (at 100/133/166 MHz) are each 8 Kbytes and two-way set-associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write protected cache. The code cache tags of the embedded Pentium processor (at 100/133/166 MHz) are also triple ported to support snooping and split-line accesses. The embedded Pentium processor with MMX technology does not support split line accesses to the code cache. As such, its code cache tags are dual ported. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The embedded Pentium processor has a 64-bit data bus and supports burst read and burst writeback cycles. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Memory Management Unit contains optional extensions to the architecture that allow four-Mbyte page sizes.

The embedded Pentium processor has added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

The embedded Pentium processor features functional redundancy checking to provide maximum error detection of the processor and the interface to the processor. When functional redundancy checking is used, a second processor, the "checker" is used to execute in lockstep with the "master" processor. The checker samples the master's outputs, compares those values with the values it computes internally, and asserts an error signal when a mismatch occurs. The embedded Pentium processor with MMX technology does not support functional redundancy checking.

As more and more functions are integrated on-chip, the complexity of board-level testing is increased. To address this, the embedded Pentium processor has increased test and debug capability by implementing IEEE Boundary Scan (Standard 1149.1).

System management mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the Virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a Virtual 8086 monitor.

Figure 15-1 is a block diagram overview of the embedded Pentium processor with MMX technology including the two instruction pipelines, the "u" pipe and the "v" pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instruction.

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated TLB to translate linear addresses to the physical addresses used by the data cache.

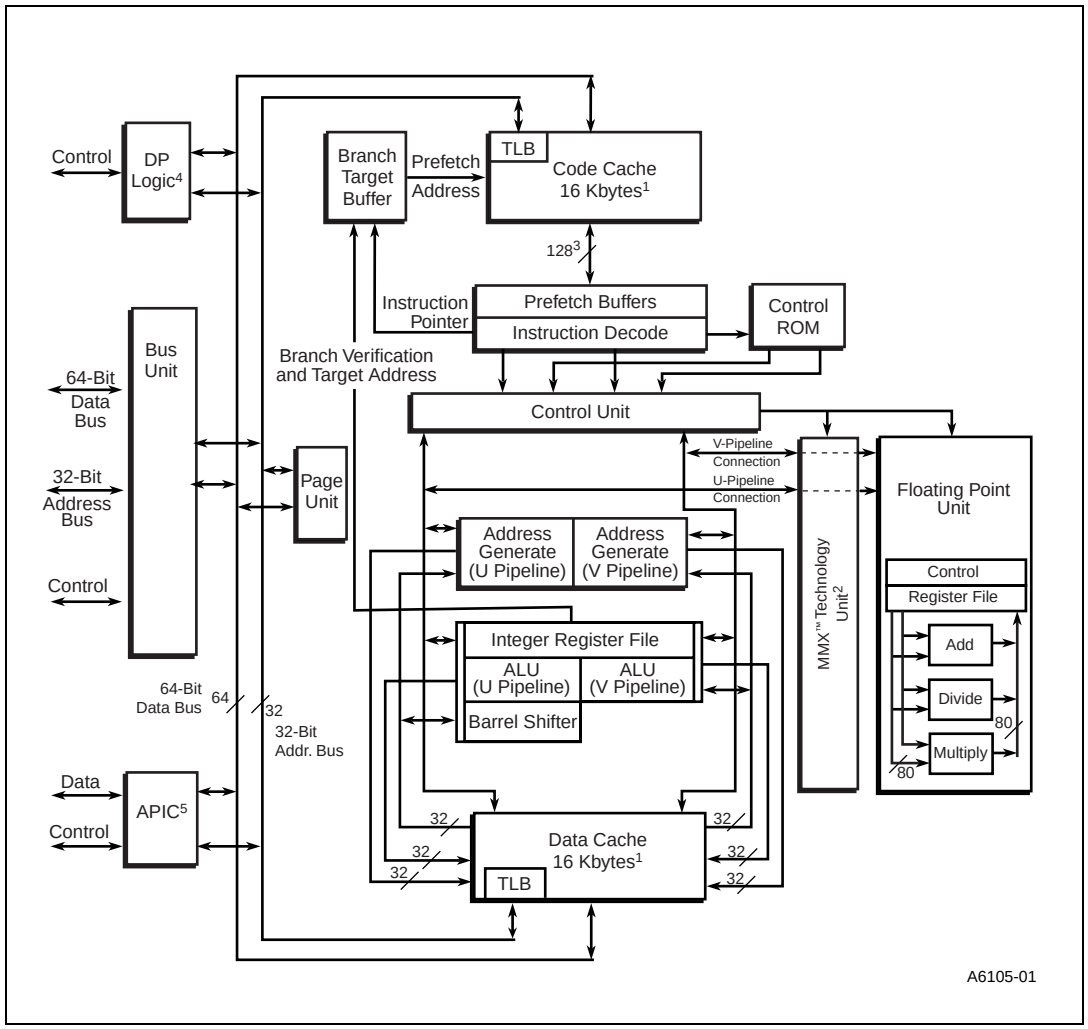
The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the embedded Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit contains two parallel decoders which decode and issue up to the next two sequential instructions into the execution pipeline. The control ROM contains the microcode that controls the sequence of operations performed by the processor. The control unit has direct control over both pipelines.

The embedded Pentium processor contains a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of Intel architecture-based processors.

The embedded Pentium processor includes features to support multi-processor systems, namely an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

**Figure 15-1. Embedded Pentium® Processor Block Diagram**




**NOTES:**
1. The Code and Data caches are each 8 Kbytes in size on the embedded Pentium® processor (at 100/133/166 MHz).
2. The MMX Technology Unit is present only on the embedded Pentium processor with MMX™ technology.
3. The internal instruction bus is 256 bits wide on the embedded Pentium processor.
4. Dual processing is not present on the embedded Pentium processor with Voltage Reduction Technology or the low-power embedded Pentium processor with MMX technology.
5. The APIC is not present on the embedded Pentium processor with Voltage Reduction Technology.

The dual processor configuration allows two embedded Pentium processors to share a single L2 cache for a low-cost symmetric multi-processor system. The two processors appear to the system as a single embedded Pentium processor. Multiprocessor operating systems properly schedule computing tasks between the two processors. This scheduling of tasks is transparent to software applications and the end-user. Logic built into the processors support a “glueless” interface for easy system design. Through a private bus, the two embedded Pentium processors arbitrate for the external bus and maintain cache coherency. The embedded Pentium processor can also be used in a conventional multi-processor system in which one L2 cache is dedicated to each processor.

In this document, in order to distinguish between two embedded Pentium processors in dual processing mode, one processor is referred to as the Primary processor and the other as the Dual processor. Note that this is a different concept than that of “master” and “checker” processors described in the discussion on functional redundancy.

Dual processing is supported in a system only when both processors are operating at identical core and bus frequencies and are the same type of processor. Within these restrictions, two processors of different steppings may operate together in a system. See Chapter 16, “Component Operation” for more details about Dual processing.

The embedded Pentium processor is produced on Intel’s advanced silicon technology. The embedded Pentium processor also includes SL enhanced power management features. When the clock to the embedded Pentium processor is stopped, power dissipation is virtually eliminated. The low $V_{CC}$ operating voltages and SL enhanced power management features make the embedded Pentium processor a good choice for energy-efficient designs.

The embedded Pentium processor supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies. See the datasheet for the bus-to-core frequency ratios supported by a specific member of the embedded Pentium processor family.