Mobile Intel® Pentium® 4 Processor-M and Intel® 852GM Chipset Platform

Design Guide Update

April 2005

Notice: The Intel® 852GM chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 305341-002

Contents

Revision History

Revision Number	Description	Revision Date
-001	Initial Release	December 2004
-002	Updates Include: Clarification on USB ESD protection	April 2005

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Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® Pentium® 4 Processor-M and Intel® 852GM Chipset Platform Design Guide* Document Number 252338. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2003. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types. However, only the detail for new material is included in this document. Both the public design guide document and this design guide update document are required to allow the users to have a complete list of information types and the associated details. This design guide update document will contain information that has not been previously published.

Affected Documents

Document Title/Document Number	Document Location
Intel® Pentium® M Processor and Intel® 852GM Chipset Platform Design Guide, 252338-003	http://www.intel.com/design/mobile/desguide/252338.htm

Related Documents

Document Title	Document Location
Intel® 852GM Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	http://www.intel.com/design/mobile/datashts/252407.htm
Intel® 82801DB I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	http://www.intel.com/design/mobile/datashts/252337.htm

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 852GM chipset.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Tables of Changes

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	System Memory SMVREF design update

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
1	Doc	Correction on buffer pin-out/connection for CRT VSYNC/HSYNC
2	Doc	Correction on pin-out/connection for Processor power

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Clarification on CPURST# pull-up resistor value at ITP connector
2	Doc	Correction on HLSTB signal name
3	Doc	CRT VSYNC/HSYNC design update
4	Doc	Clarification on USB ESD protection

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General Design Considerations

1. System Memory SMVREF Design Update

SMVREF is required to be on during S3. Without valid SMVREF to GMCH, CKE lines may float high during S3. Section 11.5.3.5 “DDR SMRCOMP and VTT 1.25-V Supply Disable in S3/Suspend” should be updated as follows.

*SMRCOMP and VTT 1.25V supplies can be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require resistive compensation during suspend. However, the 2.5-V VCCSM power pins of the GMCH, the **SMVREF** pin of the GMCH, and the VDD power pins of the DDR memory devices are required to be on in S3 state. Note that **some DDR memory devices may or may not require a valid reference voltage during suspend.** It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met.*

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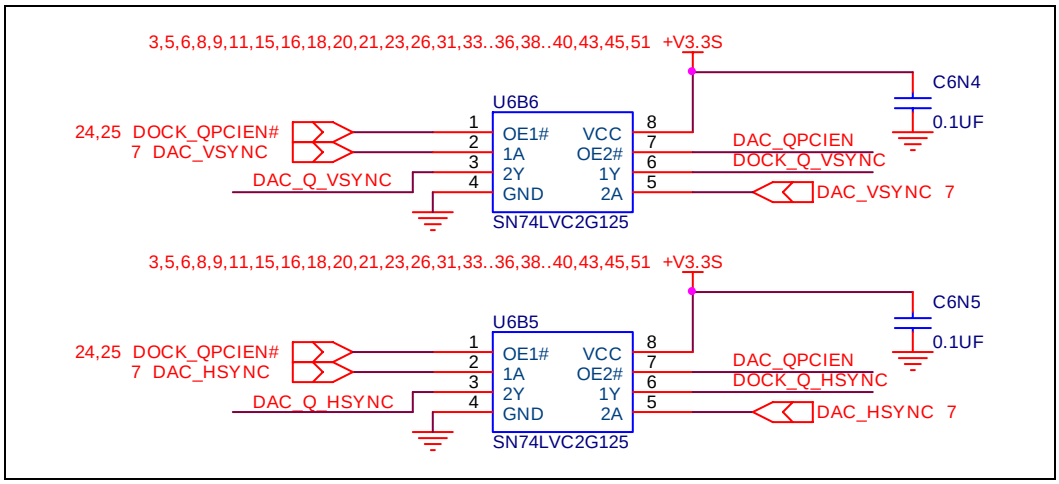
Schematic, Layout, and Routing Updates

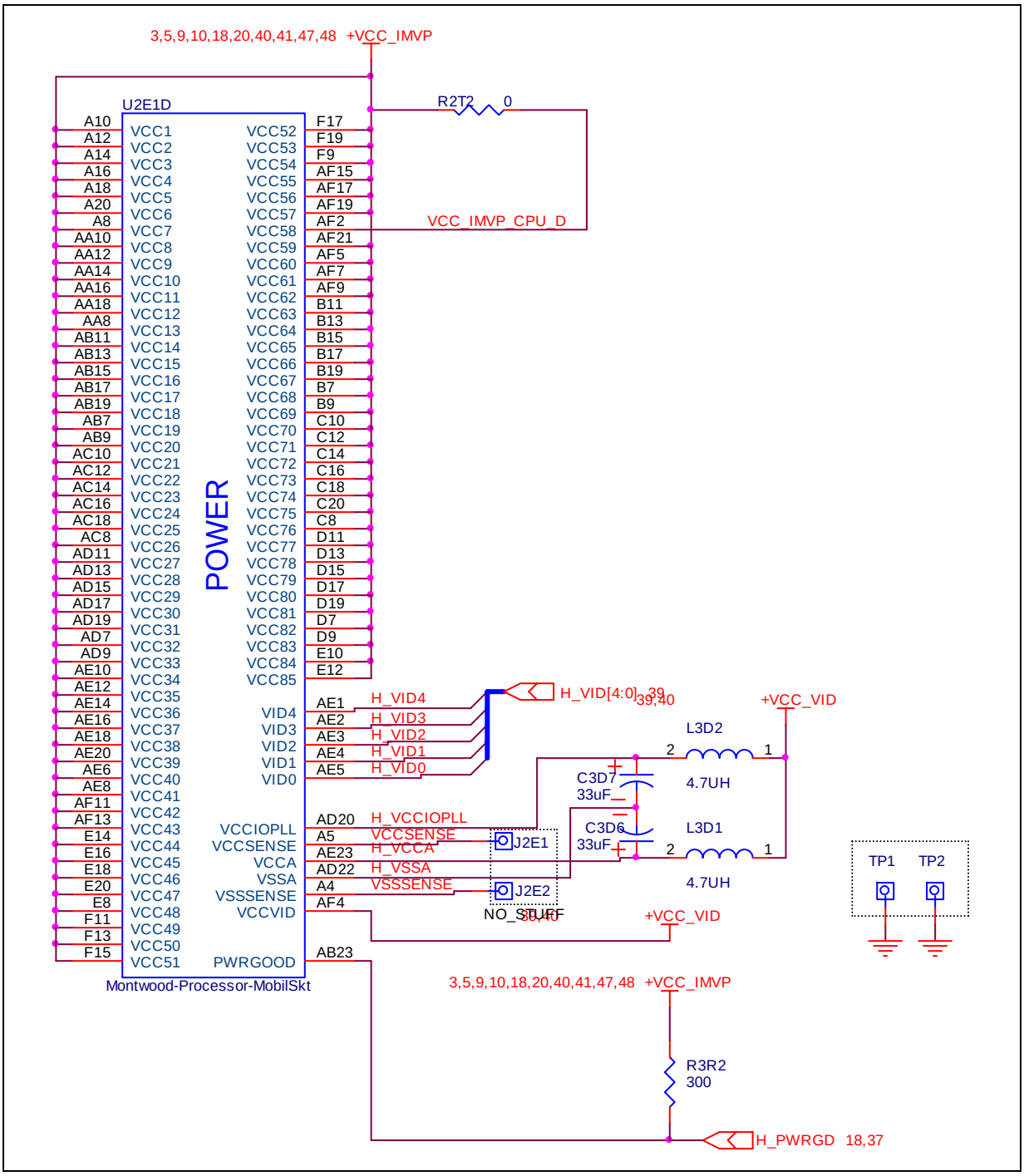
1. Correction on Buffer Pinout/Connection for CRT VSYNC/HSYNC

Schematics net connections for CRT VSYNC/HSYNC to onboard VGA connector and docking connector via SN74LVC2G125 should be corrected as follows (schematics sheet 17).



2. Correction on Pinout/Connection for Processor Power

Schematics net connections for VCCA and VCCIOPLL for the Processor power should be corrected as follows (schematics sheet 4).


3,5,9,10,18,20,40,41,47,48 +VCC_IMVP
U2E1D
R2T2 0
VCC_IMVP_CPU_D
POWER
Montwood-Processor-MobilSkt
H_VID[4:0] 39
39,40
+VCC_VID
L3D2
4.7UH
C3D7
33uF
C3D6
33uF
L3D1
4.7UH
J2E1
J2E2
NO_STUFF
TP1
TP2
3,5,9,10,18,20,40,41,47,48 +VCC_IMVP
R3R2
300
H_PWRGD 18,37

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Documentation Changes

1. Clarification on CPURST# Pull-Up Resistor Value at ITP Connector

CPURST# pull-up resistor value at ITP connector should change from 51 Ω to 220 Ω ±5%. The tables in sections 13.4.1 and 13.4.2 should be changed accordingly.

13.4.1 Resistor Recommendations

RESET#	220 Ω pull-up to VCCP			**If ITP700FLEX is Used**: RESET# connects from processor to GMCH and then forks out to ITP700 FLEX, with pull-up and series damping resistor placed next to ITP. Second pull-up may be required at ITP if there is noise issues on the signal.	

13.4.2 In Target Probe (ITP)

Pin Name	System Pull-up /Pull-down	Series Termination Resistor (Ω)	Notes	✓
RESET#	220 Ω pull-up to VCCP If USING ITP700FLEX	150 Ω from pull-up to ITP700FLEX	See Notes in Section 13.4.1	

2. Correction on HLSTB Signal Name

Hub interface strobe names listed in Table 41 should be “HLSTB”

Hub Interface Signals Internal Layer Routing Summary

Signal	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HL[10:0]	6”	4	8	± 100	Differential HLSTB pair	20	
HLSTB HLSTB#	6”	4	8	± 100	Data lines	20	HLSTB and HLSTB# must be ± 10 mils of each other.

3. CRT VSYNC/HSYNC Design Update

New / updated recommendations are provided for HSYNC/VSYNC isolation buffer / switch implementations. Customers need to ensure that there is no back-drive on these signals from the monitors and that electrical specifications are met at both the buffer and at the VGA connectors. Section 7.1.6 “HSYNC and VSYNC Design Considerations” should be updated as follows.

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3-V outputs from the GMCH. Some monitors have been found to drive HSYNC and VSYNC signals during reset. Because these signals are used as straps on the 852GM/GME and 852GM/GME, the GMCH can enter an illegal state under these conditions. In order to prevent these signals from being driven to the GMCH during reset, system designers must utilize appropriate logic to ensure the GMCH is isolated from any monitor driving HSYNC or VSYNC while PCI_RST# is active. Appropriate logic is required between the GMCH and the VGA connector (both the on-board VGA connector and the VGA connector at the docking station).

Intel’s recommended solution is to use an analog switch (i.e. discrete FET, Q-buffer) to switch these signals between the on-board VGA connector and the docking connector. In this case, footprints for a series resistor and an optional capacitor are needed on each of these signals to meet the VESA electrical specifications for video signals. Resistor and capacitor values of 39 ohm and 33 pF respectively are used on the CRB. These values were calculated based on the GMCH buffer strength and board routing. Customers are advised to perform a signal integrity check specific to their board topology, to determine the appropriate resistor and capacitor values for their platforms.

An alternative option is to use a unidirectional buffer on each of these signals. For each of the HSYNC and VSYNC signals, a footprint for a series resistor must be placed between the GMCH and the unidirectional buffer to prevent excessive overshoot and undershoot at the input of the buffer. Consideration should also be taken in designing the filter circuit on the output of these buffers to ensure that the VESA electrical specifications for video signals are met at both the on-board VGA connector as well as on the docking station. Customers are strongly encouraged to perform complete signal integrity validation at the input of the buffer and at the VGA connectors.

4. Clarification on USB ESD Protection

Added reference to USB ESD Application Note.

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn’t work for USB 2.0 due to the much higher signal rate of high-speed data. ESD protection is needed for USB lines. Refer to the *Intel® ICH Family USB ESD Considerations Application Note* for ESD protection implementation guidelines. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 108. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

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